TXU0104 / TXUN0104 シュミット トリガ入力、3 ステート出力、4 ビット固定方向電圧レベル トランスレータ

1 特長

- 完全に構成可能なデュアル レール設計により、各ポートは 1.1V～5.5V で動作可能
- 3.3V から 5.0V への変換時に最高 200Mbps をサポート
- シュミット トリガ入力により低速またはノイズの多い入力に対応
- 入力に静的プルダウン抵抗を内蔵することで、チャネルがフローティングになることを防止
- 高い駆動能力 (5V で最大 12mA)
- 低消費電力
  - 最大 2.5µA (25℃)
  - 最大 6µA (-40℃～125℃)
- V_{CC} 絶縁および V_{CC} 切断 ($I_{off-float}$) 機能
  - どちらかの V_{CC} 入力を 100mV 未満に下げる、または切り離すと、すべての出力が無効化され高インピーダンス化
- I_{off} により部分的パワーダウン モードでの動作をサポート
- 制御ロジック (OE) に $V_{CC(MIN)}$ 回路を備えているため、A ポートと B ポートのどちら側からも制御可能
- TXU0104 はアクティブ HIGH OE をサポートし、TXUN0104 はアクティブ LOW $\overline{OE}$ をサポート
- TXB ファミリのレベル シフタとピン互換
- 一般的なアプリケーションをサポートする他のバリアントで使用可能:TXU0204、TXU0304
- 動作温度範囲:-40℃～+125℃
- JESD 78、Class II 準拠で 100mA 超のラッチアップ性能
- JESD 22 を上回る ESD 保護
  - 人体モデルで 2500V
  - 荷電デバイス モデルで 1500V

2 アプリケーション

- 低速またはノイズの多い入力信号の除去
- インジケータ LED または ブザーの駆動
- メカニカル・スイッチのデバウンス
- 汎用 I/O レベル・シフト
- プッシュプル・レベル・シフト (UART、SPI、JTAG など)

3 概要

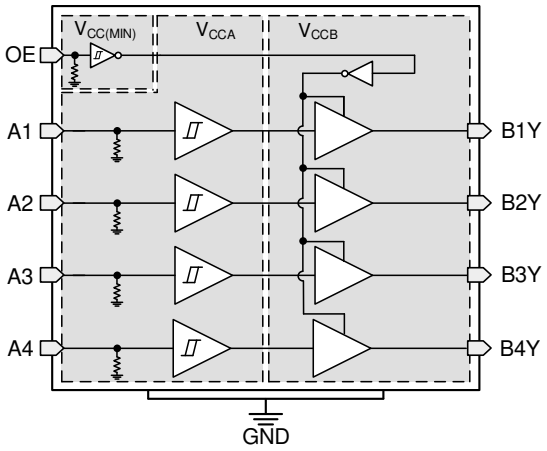
TXU0104 / TXUN0104 は、4 ビット、2 電源の非反転固定方向電圧レベル変換デバイスです。Ax ピンは V_{CCA} ロジック レベルを基準にし、OE ピンは V_{CCA} ロジック レベルと V_{CCB} ロジック レベルのいずれかを基準にでき、Bx ピンは V_{CCB} ロジック レベルを基準にします。A ポートは 1.1V～5.5V の範囲の入力電圧に対応し、B ポートも 1.1V～5.5V の範囲の入力電圧に対応しています。OE をいずれかの電源を基準として High に設定すると、A から B、または B から A に固定方向のデータ伝送を発生させることができます。OE を Low に設定すると、すべての出力ピンは高インピーダンス状態になります。TXU0104 と TXUN0104 の唯一の違いは、OE/$\overline{OE}$ 信号がそれぞれアクティブ High とアクティブ Low であることです。制御ロジックの動作の概要については、「セクション 7.4」を参照してください。

パッケージ情報

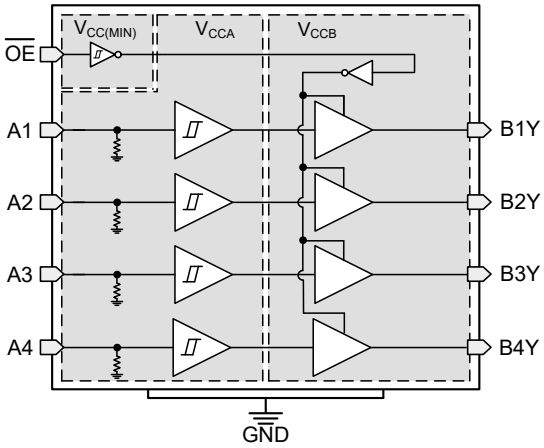
部品番号	パッケージ (1)	パッケージ サイズ (2)
TXU0104	BQA (VQFN、14)	3.00mm × 2.50mm
	PW (TSSOP、14)	5.00mm × 4.40mm
	RUT (UQFN、12)	2.00mm × 1.70mm
	DTR (X2SON、12)	1.70mm × 1.00mm
TXUN0104	RUT (UQFN、12)	2.00mm × 1.70mm

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。



TXU0104 機能ブロック図



TXUN0104 の機能ブロック図

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4 Pin Configuration and Functions

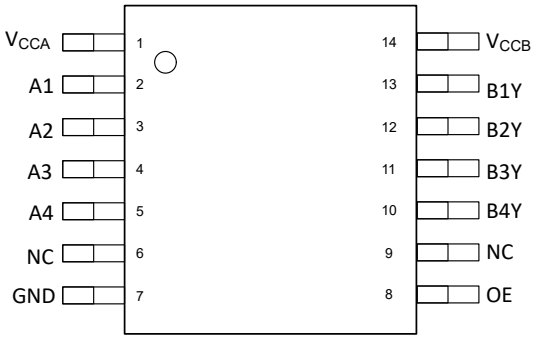


図 4-1. PW 14-Pin TSSOP Top View

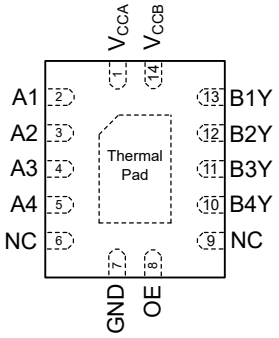


図 4-2. BQA Package 14-Pin VQFN Transparent Top View

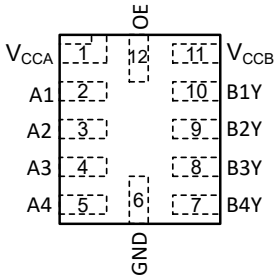


図 4-3. RUT Package 12-Pin UQFN Transparent Top View

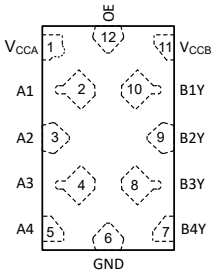


図 4-4. DTR Package 12-Pin X2SON Transparent Top View

表 4-1. TXU0104 Pin Functions

PIN			I/O	DESCRIPTION
Name	PW, BQA	RUT, DTR		
A1	2	2	I	Input A1. Referenced to V_{CCA}.
A2	3	3	I	Input A2. Referenced to V_{CCA}.
A3	4	4	I	Input A3. Referenced to V_{CCA}.
A4	5	5	I	Input A4. Referenced to V_{CCA}.
B1Y	13	10	O	Output B1. Referenced to V_{CCB}.
B2Y	12	9	O	Output B2. Referenced to V_{CCB}.
B3Y	11	8	O	Output B3. Referenced to V_{CCB}.
B4Y	10	7	O	Output B4. Referenced to V_{CCB}.
GND	7	6	—	Ground
NC	6, 9		—	No internal connection.
OE	8	12	I	Output Enable. Pull to GND to place all outputs in high-impedance mode. Pull to V_{CCA} or V_{CCB} to enable all outputs.
V_{CCA}	1	1	—	A-port supply voltage. 1.1V ≤ V_{CCA} ≤ 5.5V
V_{CCB}	14	11	—	B-port supply voltage. 1.1V ≤ V_{CCB} ≤ 5.5V
PAD	—		—	Thermal pad. May be grounded (recommended) or left floating.

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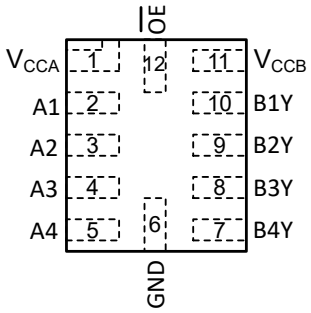


図 4-5. RUT Package, 12-Pin UQFN (Transparent Top View) (TXUN0104)

表 4-2. TXUN0104 Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
A1	2	I	Input A1. Referenced to V_{CCA}.
A2	3	I	Input A2. Referenced to V_{CCA}.
A3	4	I	Input A3. Referenced to V_{CCA}.
A4	5	I	Input A4. Referenced to V_{CCA}.
B1Y	10	O	Output B1. Referenced to V_{CCB}.
B2Y	9	O	Output B1. Referenced to V_{CCB}.
B3Y	8	O	Output B1. Referenced to V_{CCB}.
B4Y	7	O	Output B1. Referenced to V_{CCB}.
GND	6	-	Ground
$\overline{OE}$	12	I	Output Enable (active-low). Pull to V_{CCA} or V_{CCB} to place all outputs in high-impedance mode. Pull to GND to enable all outputs.
V_{CCA}	1	-	A-port supply voltage. 1.1V ≤ V_{CCA} ≤ 5.5V
V_{CCB}	11	-	B-port supply voltage. 1.1V ≤ V_{CCB} ≤ 5.5V

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage A		–0.5	6.5	V
V_{CCB}	Supply voltage B		–0.5	6.5	V
V_I	Input Voltage(2)	I/O Ports (A Port)	–0.5	6.5	V
		I/O Ports (B Port)	–0.5	6.5	
		OE	–0.5	6.5	
V_O	Voltage applied to any output in the high-impedance or power-off state(2)	A Port	–0.5	6.5	V
		B Port	–0.5	6.5	
V_O	Voltage applied to any output in the high or low state(2) (3)	A Port	–0.5	V_{CCA} + 0.5	V
		B Port	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	V_I < 0	–20		mA
I_{OK}	Output clamp current	V_O < 0	–20		mA
I_O	Continuous output current		–25	25	mA
	Continuous current through V_{CC} or GND		–100	100	mA
T_j	Junction Temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *セクション 5.1* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *セクション 5.3* Exposure beyond the limits listed in *セクション 5.3* may affect device reliability.
(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 6.5V maximum if the output current rating is observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

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5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1) (2) (3)

				MIN	MAX	UNIT
V_{CCA}	Supply voltage A			1.08	5.5	V
V_{CCB}	Supply voltage B			1.08	5.5	V
I_{OH}	High-level output current		V_{CCO} = 1.1V		–1.5	mA
			V_{CCO} = 1.4V		–3	
			V_{CCO} = 1.65V		–4.5	
			V_{CCO} = 2.3V		–8	
			V_{CCO} = 3V		–10	
			V_{CCO} = 4.5V		–12	
I_{OL}	Low-level output current		V_{CCO} = 1.1V		1.5	mA
			V_{CCO} = 1.4V		3	
			V_{CCO} = 1.65V		4.5	
			V_{CCO} = 2.3V		8	
			V_{CCO} = 3V		10	
			V_{CCO} = 4.5V		12	
V_I	Input voltage (3)			0	5.5	V
V_O	Output voltage	Active State		0	V_{CCO}	V
		Tri-State		0	5.5	
T_A	Operating free-air temperature			–40	125	°C

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All control inputs and data I/Os of this device have weak pulldowns to ensure the line is not floating when undefined external to the device. The input leakage from these weak pulldowns is defined by the I_I specification indicated under Electrical Characteristics

5.4 Thermal Information

THERMAL METRIC(1)		TXU0104/TXUN0104				UNIT
		PW TSSOP)	BQA WQFN)	RUT (UQFN)	DTR (X2SON)	
		14 PINS	14 PINS	12 PINS	12 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	135.8	87.2	171.9	176.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	65.0	90.0	100.4	84.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	78.8	56.0	97.1	99.1	°C/W
Y_{JT}	Junction-to-top characterization parameter	15.6	9.8	10.9	2.6	°C/W
Y_{JB}	Junction-to-board characterization parameter	78.2	56.0	95.5	98.9	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case (bottom) thermal resistance	N/A	33.0	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)(1) (2)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	Operating free-air temperature (T_A)									UNIT
					25°C			–40°C to 85°C			–40°C to 125°C			
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{T+}	Positive-going input-threshold voltage	Data Inputs (Ax, Bx) (Referenced to V_{CCI})	1.1V	1.1V				0.44		0.88	0.44		0.88	V
			1.4V	1.4V				0.60		0.98	0.60		0.98	
			1.65V	1.65V				0.76		1.13	0.76		1.13	
			2.3V	2.3V				1.08		1.56	1.08		1.56	
			3V	3V				1.48		1.92	1.48		1.92	
			4.5V	4.5V				2.19		2.74	2.19		2.74	
			5.5V	5.5V				2.65		3.33	2.65		3.33	
		OE (Referenced to V_{CCA} or V_{CCB})	1.1V	1.1V				0.44		0.88	0.44		0.88	V
			1.4V	1.4V				0.60		0.98	0.60		0.98	
			1.65V	1.65V				0.76		1.13	0.76		1.13	
			2.3V	2.3V				1.08		1.56	1.08		1.56	
			3V	3V				1.48		1.92	1.48		1.92	
			4.5V	4.5V				2.19		2.74	2.19		2.74	
			5.5V	5.5V				2.65		3.33	2.65		3.33	
V_{T-}	Negative-going input-threshold voltage	Data Inputs (Ax, Bx) (Referenced to V_{CCI})	1.1V	1.1V				0.17		0.48	0.17		0.48	V
			1.4V	1.4V				0.28		0.59	0.28		0.59	
			1.65V	1.65V				0.35		0.69	0.35		0.69	
			2.3V	2.3V				0.56		0.97	0.56		0.97	
			3V	3V				0.89		1.5	0.89		1.5	
			4.5V	4.5V				1.51		1.97	1.51		1.97	
			5.5V	5.5V				1.88		2.4	1.88		2.4	
		OE (Referenced to V_{CCA} or V_{CCB})	1.1V	1.1V				0.17		0.48	0.17		0.48	V
			1.4V	1.4V				0.28		0.59	0.28		0.59	
			1.65V	1.65V				0.35		0.69	0.35		0.69	
			2.3V	2.3V				0.56		0.97	0.56		0.97	
			3V	3V				0.89		1.5	0.89		1.5	
			4.5V	4.5V				1.51		1.97	1.51		1.97	
			5.5V	5.5V				1.88		2.46	1.88		2.46	

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over operating free-air temperature range (unless otherwise noted)(1) (2)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	Operating free-air temperature (T_A)									UNIT
					25°C			–40°C to 85°C			–40°C to 125°C			
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
ΔV_T	Input-threshold hysteresis ($V_{T+} - V_{T-}$)	Data Inputs (Ax, Bx) (Referenced to V_{CCI})	1.1V	1.1V				0.20		0.40	0.20		0.40	V
			1.4V	1.4V				0.25		0.50	0.25		0.50	
			1.65V	1.65V				0.30		0.55	0.30		0.55	
			2.3V	2.3V				0.38		0.65	0.38		0.65	
			3V	3V				0.46		0.72	0.46		0.72	
			4.5V	4.5V				0.58		0.93	0.58		0.93	
			5.5V	5.5V				0.69		1.06	0.69		1.06	
		OE (Referenced to V_{CCA} or V_{CCB})	1.1V	1.1V				0.15		0.41	0.15		0.41	V
			1.4V	1.4V				0.20		0.50	0.20		0.50	
			1.65V	1.65V				0.23		0.55	0.23		0.55	
			2.3V	2.3V				0.32		0.65	0.32		0.65	
			3V	3V				0.39		0.72	0.39		0.72	
			4.5V	4.5V				0.57		0.97	0.57		0.97	
			5.5V	5.5V				0.69		1.18	0.69		1.18	
V_{OH}	High-level output voltage (3)	I_{OH} = –0.1mA	1.1V – 5.5V	1.1V – 5.5V				Vcco - 0.1			Vcco - 0.1			V
		I_{OH} = –0.5mA	1.1V	1.1V				0.82			0.82			
		I_{OH} = –3mA	1.4V	1.4V				1.0			1.0			
		I_{OH} = –4.5mA	1.65V	1.65V				1.2			1.2			
		I_{OH} = –8mA	2.3V	2.3V				1.7			1.7			
		I_{OH} = –10mA	3V	3V				2.2			2.2			
		I_{OH} = –12mA	4.5V	4.5V				3.7			3.7			
V_{OL}	Low-level output voltage (4)	I_{OL} = 0.1mA	1.1V – 5.5V	1.1V – 5.5V						0.1			0.1	V
		I_{OL} = 0.5mA	1.1V	1.1V						0.27			0.27	
		I_{OL} = 3mA	1.4V	1.4V						0.35			0.35	
		I_{OL} = 4.5mA	1.65V	1.65V						0.45			0.45	
		I_{OL} = 8mA	2.3V	2.3V						0.7			0.7	
		I_{OL} = 10 mA	3V	3V						0.8			0.8	
		I_{OL} = 8mA	4.5V	4.5V						0.55			0.55	
		I_{OL} = 12mA	4.5V	4.5V						0.8			0.8	
I_I	Input leakage current	OE $V_I = V_{CC}$ or GND	1.1V – 5.5V	1.1V – 5.5V	-0.1		1.5	-0.1		1.5	-0.1		2	µA
		Data Inputs (Ax, Bx) $V_I = V_{CCI}$ or GND	1.1V – 5.5V	1.1V – 5.5V	-0.1		1.5	-0.1		1.5	-2		2	µA
I_{off}	Partial power down current	A Port or B Port V_I or V_O = 0V - 5.5 V	0 V	0 V - 5.5V	-1.5		1.5	-2		2	-2.5		2.5	µA
			0V - 5.5V	0V	-1.5		1.5	-2		2	-2.5		2.5	
$I_{off-float}$	Floating supply Partial power down current	A Port or B Port V_I or V_O = GND	Floating(5)	0 V - 5.5V	-1.5		1.5	-2		2	-2.5		2.5	µA
			0 V - 5.5V	Floating(5)	-1.5		1.5	-2		2	-2.5		2.5	
I_{OZ}	Tri-state output current	A or B Port: $V_I = V_{CCI}$ or GND $V_O = V_{CCO}$ or GND OE = GND	1.1V – 5.5V	1.1V – 5.5V	-0.3		0.3	-1		1	-2		2	µA

over operating free-air temperature range (unless otherwise noted)(1) (2)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	Operating free-air temperature (T_A)									UNIT
					25°C			–40°C to 85°C			–40°C to 125°C			
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{CCA}	V_{CCA} supply current	V_I = V_{CCI} or GND I_O = 0	1.1V – 5.5V	1.1V – 5.5V			1.5			2.5			6	µA
			0V	5.5V	-0.3			-1			-1			
			5.5V	0V			1			1.5			3	
		V_I = GND I_O = 0	5.5V	Floating(5)			1.5			7			15	
I_{CCB}	V_{CCB} supply current	V_I = V_{CCI} or GND I_O = 0	1.1V – 5.5V	1.1V – 5.5V			1.5			2.5			6	µA
			0V	5.5V			1			1.5			3	
			5.5V	0V	-0.3			-1			-1			
		V_I = GND I_O = 0	Floating(5)	5.5V			1.5			7			15	
I_{CCA} + I_{CCB}	Combined supply current	V_I = V_{CCI} or GND I_O = 0	1.1V – 5.5V	1.1V – 5.5V			2.5			3			6	µA
C_i	Control Input Capacitance	V_I = 3.3V or GND	3.3V	3.3V		2.75			3			3.5		pF
C_{io}	Data I/O Capacitance	OE = GND, V_O = 1.65V DC +1MHz -16dBm sine wave	3.3V	3.3V		3			4			4		pF

(1) V_{CCI} is the V_{CC} associated with the input port
(2) V_{CCO} is the V_{CC} associated with the output port
(3) Tested at V_I = $V_{T+(MAX)}$
(4) Tested at V_I = $V_{T-(MIN)}$
(5) Floating is defined as a node that is both not actively driven by an external device and has leakage not exeeding 10nA

5.6 Switching Characteristics: T_{sk}, T_{MAX}

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CCI}	V_{CCO}	Operating free-air temperature (T_A)			UNIT
					-40°C to 125°C			
					MIN	TYP	MAX	
T_{MAX} - Maximum Data Rate	50% Duty Cycle Input One channel switching 20% of pulse > 0.7*V_{CCO} 20% of pulse < 0.3*V_{CCO}	Up Translation	3.0V - 3.6V	4.5V - 5.5V	200			Mbps
			1.65V - 1.95V	4.5V - 5.5V	150			
			1.1V - 1.3V	4.5V - 5.5V	30			
			1.65V - 1.95V	3.0V - 3.6V	100			
			1.1V - 1.3V	3.0V - 3.6 V	30			
			1.1V - 1.3V	1.65V - 1.95V	20			
		Down Translation	4.5V - 5.5V	3.0V - 3.6V	125			
			4.5V - 5.5V	1.65V - 1.95V	50			
			4.5V - 5.5V	1.1V - 1.3V	10			
			3.0V - 3.6V	1.65V - 1.95V	50			
			3.0V - 3.6V	1.1V - 1.3V	10			
			1.65V - 1.95V	1.1V - 1.3V	10			

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over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CCI}	V_{CCO}	Operating free-air temperature (T_A) -40°C to 125°C MIN	TYP	MAX	UNIT
t_{sk} - Output skew	Timing skew between any switching outputs on the rising or falling edge	Up Translation	3.0V - 3.6V	4.5V - 5.5V			3	ns
			1.65V - 1.95V	4.5V - 5.5V			10	
			1.1V - 1.3V	4.5V - 5.5V			42	
			1.65V - 1.95V	3.0V - 3.6V			8	
			1.1V - 1.3V	3.0V - 3.6V			42	
			1.1V - 1.3V	1.65V - 1.95V			45	
		Down Translation	4.5V - 5.5V	3.0V - 3.6V			3	
			4.5V - 5.5V	1.65V - 1.95V			10	
			4.5V - 5.5V	1.1V - 1.3V			42	
			3.0V - 3.6V	1.65V - 1.95V			8	
			3.0V - 3.6V	1.1V - 1.3V			42	
			1.65V - 1.95V	1.1V - 1.3V			45	

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5.7 Switching Characteristics, V_{CCA} = 1.2 ± 0.1V

See Figure 7-1 and Table 7-1 for test circuit and loading. See Figure 7-2, Figure 7-3, and Figure 7-4 for measurement waveforms.

PARAMETER		FROM	TO	TEST CONDITIONS	B-Port Supply Voltage (V_{CCB})																		UNIT
					1.2 ± 0.1V			1.5 ± 0.1V			1.8 ± 0.15V			2.5 ± 0.2V			3.3 ± 0.3V			5.0 ± 0.5V			
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	Propagation delay	A	B	-40°C to 85°C	3.3		96	0.5		43	0.5		37	0.5		32	0.5		30	0.5		31	ns
				-40°C to 125°C	5.7		60	3		39	1.4		33	0.5		28	0.5		27	0.5		26	
		B	A	-40°C to 85°C	3.3		95	1.9		80	0.5		75	0.5		70	0.5		69	0.5		69	
				-40°C to 125°C	5.7		60	4.1		51	2.9		48	1.8		45	1.5		44	1.3		44	
t_{dis}	Disable time	OE	A	-40°C to 85°C	28.8		133	28.5		130	28.4		133	28.8		137	28.4		143	18.7		211	ns
				-40°C to 125°C	43.3		133	43.3		130	43.7		130	44.7		131	45.4		134	31.8		140	
		OE	B	-40°C to 85°C	32.5		150	27.6		117	25.8		110	22.5		104	22.1		112	20.1		181	
				-40°C to 125°C	48.3		149	43.2		120	40.8		113	36.8		104	36.5		107	33.8		111	
t_{en}	Enable time	OE	A	-40°C to 85°C	24.1		237	22.1		229	21.4		230	21.3		232	21.7		235	22.7		244	ns
				-40°C to 125°C	34.9		156	33.3		167	32		169	31.7		173	32		177	34.2		187	
		OE	B	-40°C to 85°C	21.3		237	14.3		152	11.2		140	8.8		130	8.2		130	8.4		132	
				-40°C to 125°C	29.8		143	23		116	18.6		107	15.4		97	14.5		97	14.8		103	

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5.8 Switching Characteristics, V_{CCA} = 1.5 ± 0.1V

See Figure 7-1 and Table 7-1 for test circuit and loading. See Figure 7-2, Figure 7-3, and Figure 7-4 for measurement waveforms.

PARAMETER		FROM	TO	TEST CONDITIONS	B-Port Supply Voltage (V_{CCB})																		UNIT
					1.2 ± 0.1V			1.5 ± 0.1V			1.8 ± 0.15V			2.5 ± 0.2V			3.3 ± 0.3V			5.0 ± 0.5V			
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	Propagation delay	A	B	-40°C to 85°C	1.9		80	0.5		31	0.5		25	0.5		19	0.5		17	0.5		15	ns
				-40°C to 125°C	4.1		51	1.6		31	0.5		25	0.5		20	0.5		18	0.5		16	
		B	A	-40°C to 85°C	0.5		43	0.5		31	0.5		28	0.5		26	0.5		25	0.5		24	
				-40°C to 125°C	3		39	1.6		31	0.5		28	0.5		26	0.5		25	0.5		24	
t_{dis}	Disable time	OE	A	-40°C to 85°C	20		91	19		82	18.8		81	19.2		82	19.6		83	12.2		87	ns
				-40°C to 125°C	34.9		95	32.6		86	32.8		85	33.4		87	34.2		88	24.6		92	
		OE	B	-40°C to 85°C	27.4		127	21.7		91	19.9		82	16.3		71	15.9		71	13.7		70	
				-40°C to 125°C	44.4		130	36.7		95	34.7		86	30.2		75	29.8		75	26.6		74	
t_{en}	Enable time	OE	A	-40°C to 85°C	14.9		102	14.4		86	13.5		88	12.7		90	12.6		92	13.2		97	ns
				-40°C to 125°C	25.5		102	25.2		89	24.1		91	22.8		93	22.8		86	23.5		100	
		OE	B	-40°C to 85°C	17.9		175	12.7		80	9.1		69	6.1		57	4.9		53	4.5		54	
				-40°C to 125°C	26.6		135	21		81	16.8		71	12.5		60	10.8		56	10.4		57	

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5.9 Switching Characteristics, V_{CCA} = 1.8 ± 0.15V

See Figure 7-1 and Table 7-1 for test circuit and loading. See Figure 7-2, Figure 7-3, and Figure 7-4 for measurement waveforms.

PARAMETER		FROM	TO	TEST CONDITIONS	B-Port Supply Voltage (V_{CCB})																		UNIT
					1.2 ± 0.1V			1.5 ± 0.1V			1.8 ± 0.15V			2.5 ± 0.2V			3.3 ± 0.3V			5.0 ± 0.5V			
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	Propagation delay	A	B	-40°C to 85°C	0.5		75	0.5		28	0.5		22	0.5		17	0.5		14	0.5		12	ns
				-40°C to 125°C	2.9		48	0.5		28	0.5		23	0.5		17	0.5		15	0.5		13	
		B	A	-40°C to 85°C	0.5		37	0.5		25	0.5		22	0.5		19	0.5		19	0.5		18	
				-40°C to 125°C	1.4		33	0.5		25	0.5		23	0.5		20	0.5		19	0.5		19	
t_{dis}	Disable time	OE	A	-40°C to 85°C	17.2		79	14.7		67	14.5		65	14.3		65	14.4		66	8.5		68	ns
				-40°C to 125°C	30.9		83	28		71	26.6		69	27.5		70	27.2		71	20		73	
		OE	B	-40°C to 85°C	25.4		121	18.7		81	16.5		71	12.8		60	12.5		58	9.8		55	
				-40°C to 125°C	41.7		123	34		86	30.3		76	26.2		64	25.3		62	21.8		59	
t_{en}	Enable time	OE	A	-40°C to 85°C	10.9		88	9.5		66	9.4		63	8.6		65	8.2		66	8.1		69	ns
				-40°C to 125°C	20.3		87	19		69	18.9		67	17.6		68	17.1		70	17.1		73	
		OE	B	-40°C to 85°C	16.7		177	10.4		75	8.1		58	4.9		46	3.3		42	2.2		39	
				-40°C to 125°C	25.1		135	18.7		77	15.5		60	11		49	8.7		44	7.3		42	

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5.10 Switching Characteristics, V_{CCA} = 2.5 ± 0.2V

See Figure 7-1 and Table 7-1 for test circuit and loading. See Figure 7-2, Figure 7-3, and Figure 7-4 for measurement waveforms.

PARAMETER		FROM	TO	TEST CONDITIONS	B-Port Supply Voltage (V_{CCB})																		UNIT
					1.2 ± 0.1V			1.5 ± 0.1V			1.8 ± 0.15V			2.5 ± 0.2V			3.3 ± 0.3V			5.0 ± 0.5V			
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	Propagation delay	A	B	-40°C to 85°C	0.5		70	0.5		26	0.5		20	0.5		14	0.5		12	0.5		9	ns
				-40°C to 125°C	1.8		45	0.5		26	0.5		20	0.5		14	0.5		12	0.5		10	
		B	A	-40°C to 85°C	0.5		32	0.5		19	0.5		17	0.5		14	0.5		13	0.5		13	
				-40°C to 125°C	0.5		28	0.5		20	0.5		17	0.5		14	0.5		13	0.5		13	
t_{dis}	Disable time	OE	A	-40°C to 85°C	12.9		65	10.5		51	9		51	8.1		43	8.4		44	5		45	ns
				-40°C to 125°C	24.9		68	21.8		55	19.7		50	18.2		47	18.6		48	15		49	
		OE	B	-40°C to 85°C	23.2		112	16.5		74	14		61	9		46	9.1		44	6.4		39	
				-40°C to 125°C	38.7		115	30.9		79	27.1		66	21.6		51	20.5		48	16.8		43	
t_{en}	Enable time	OE	A	-40°C to 85°C	7.9		80	5.9		50	5.1		44	4.7		39	4.4		40	3.7		41	ns
				-40°C to 125°C	15.6		74	13.5		53	12.4		47	12		42	11.5		43	10.8		44	
		OE	B	-40°C to 85°C	16.3		183	9.2		74	6		54	4		36	2.1		31	0.5		27	
				-40°C to 125°C	24.4		139	17.2		76	13		57	9.8		38	7.1		33	4.7		29	

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5.11 Switching Characteristics, V_{CCA} = 3.3 ± 0.3V

See Figure 7-1 and Table 7-1 for test circuit and loading. See Figure 7-2, Figure 7-3, and Figure 7-4 for measurement waveforms.

PARAMETER		FROM	TO	TEST CONDITIONS	B-Port Supply Voltage (V_{CCB})																		UNIT
					1.2 ± 0.1V			1.5 ± 0.1V			1.8 ± 0.15V			2.5 ± 0.2V			3.3 ± 0.3V			5.0 ± 0.5V			
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	Propagation delay	A	B	-40°C to 85°C	0.5		69	0.5		25	0.5		19	0.5		13	0.5		11	0.5		8	ns
				-40°C to 125°C	1.5		44	0.5		25	0.5		19	0.5		13	0.5		11	0.5		9	
		B	A	-40°C to 85°C	0.5		30	0.5		17	0.5		14	0.5		12	0.5		11	0.5		10	
				-40°C to 125°C	0.5		27	0.5		18	0.5		15	0.5		12	0.5		11	0.5		10	
t_{dis}	Disable time	OE	A	-40°C to 85°C	12.9		62	10.1		47	8.7		42	6.9		39	6.6		39	6.9		40	ns
				-40°C to 125°C	24		65	20.6		51	18.4		46	15.7		40	15.3		39	15.9		40	
		OE	B	-40°C to 85°C	22.7		109	15.7		71	13.2		59	8.5		42	7.6		38	4.7		34	
				-40°C to 125°C	37.6		111	29.5		75	25.4		63	19.2		46	18.5		42	14.2		36	
t_{en}	Enable time	OE	A	-40°C to 85°C	6.6		85	4.2		45	3		37	2.4		31	2.2		30	1.7		30	ns
				-40°C to 125°C	13.6		72	10.9		47	9.3		40	8.2		33	8.1		32	7.5		33	
		OE	B	-40°C to 85°C	16.3		192	8.9		76	5.4		55	2.6		34	1.8		27	0.5		22	
				-40°C to 125°C	24.3		144	16.7		78	12.2		57	8		36	6.6		29	3.7		24	

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5.12 Switching Characteristics, V_{CCA} = 5.0 ± 0.5V

See Figure 7-1 and Table 7-1 for test circuit and loading. See Figure 7-2, Figure 7-3, and Figure 7-4 for measurement waveforms.

PARAMETER		FROM	TO	TEST CONDITIONS	B-Port Supply Voltage (V_{CCB})														UNIT
					1.2 ± 0.1V			1.5 ± 0.1V			1.8 ± 0.15V			2.5 ± 0.2V			3.3 ± 0.3V			5.0 ± 0.5V			
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	Propagation delay	A	B	-40°C to 85°C	0.5		69	0.5		24	0.5		18	0.5		13	0.5		10	0.5		8	ns
				-40°C to 125°C	1.3		44	0.5		24	0.5		19	0.5		13	0.5		11	0.5		8	
		B	A	-40°C to 85°C	0.5		31	0.5		15	0.5		12	0.5		9	0.5		8	0.5		8	
				-40°C to 125°C	0.5		26	0.5		16	0.5		13	0.5		10	0.5		9	0.5		8	
t_{dis}	Disable time	OE	A	-40°C to 85°C	10.8		58	7.7		42	5.9		36	4.2		31	3.4		30	2.8		26	ns
				-40°C to 125°C	20.8		61	17		46	14.5		40	11.8		33	10.4		31	9.6		29	
		OE	B	-40°C to 85°C	9.7		109	5.9		69	13.2		56	8.4		40	6.9		36	3.7		29	
				-40°C to 125°C	37.4		111	29.2		73	24.6		60	18.1		43	16.4		39	12.2		31	
t_{en}	Enable time	OE	A	-40°C to 85°C	6		102	2.8		44	1.2		33	0.5		25	0.5		22	0.5		21	ns
				-40°C to 125°C	12.4		81	8.8		46	6.5		36	4.7		27	4.2		24	4.4		23	
		OE	B	-40°C to 85°C	16.7		212	8.8		82	4.8		58	1.6		35	0.5		26	0.5		19	
				-40°C to 125°C	24.8		158	16.7		83	11.7		60	6.9		37	4.7		28	3.5		21	

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5.13 Operating Characteristics

T_A = 25℃ (1)

PARAMETER		Test Conditions	Supply Voltage (V_{CCB} = V_{CCA})						UNIT
			1.2 ± 0.1V	1.5 ± 0.1V	1.8 ± 0.15V	2.5 ± 0.2V	3.3 ± 0.3V	5.0 ± 0.5V	
			TYP	TYP	TYP	TYP	TYP	TYP	
C_{pdA} (2)	A to B: outputs enabled	A Port C_L = 0, R_L = Open f = 10MHz t_{rise} = t_{fall} = 1 ns	2	2	2	2	2	3	pF
	A to B: outputs disabled		2	2	2	2	2	3	
	B to A: outputs enabled		12	12	12	13	13	16	
	B to A: outputs disabled		2	2	2	2	2	3	
C_{pdB} (3)	A to B: outputs enabled	B Port C_L = 0, R_L = Open f = 10MHz t_{rise} = t_{fall} = 1ns	12	12	12	13	13	16	pF
	A to B: outputs disabled		2	2	2	2	2	3	
	B to A: outputs enabled		2	2	2	2	2	3	
	B to A: outputs disabled		2	2	2	2	2	3	

(1) For additional information about how power dissipation capacitance affects power consumption, see the CMOS Power Consumption and C_{pd} Calculation application report
(2) A-Port power dissipation capacitance per transceiver
(3) B-Port power dissipation capacitance per transceiver

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5.14 Typical Characteristics

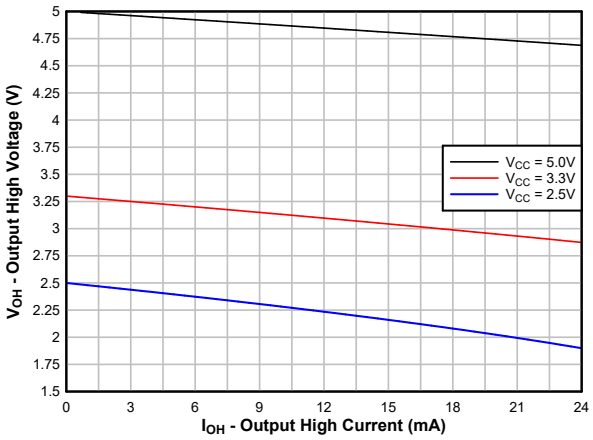


図 5-1. Typical (T_A=25°C) Output High Voltage (V_{OH}) vs Source Current (I_{OH})

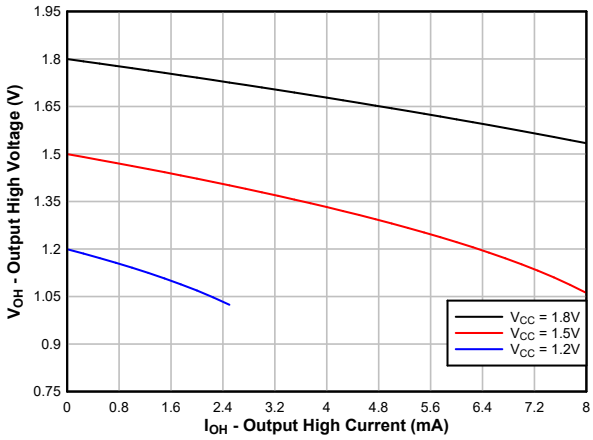


図 5-2. Typical (T_A=25°C) Output High Voltage (V_{OH}) vs Source Current (I_{OH})

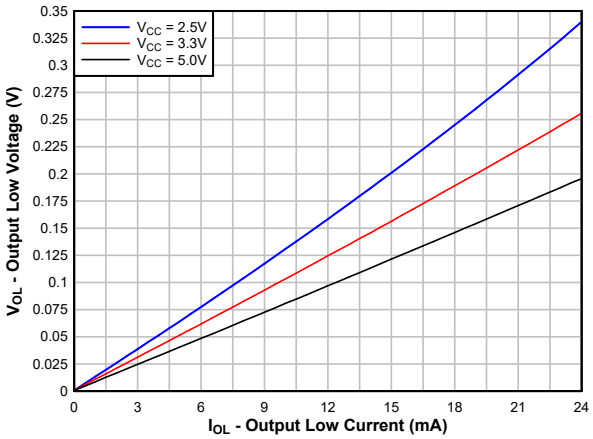


図 5-3. Typical (T_A=25°C) Output Low Voltage (V_{OL}) vs Sink Current (I_{OL})

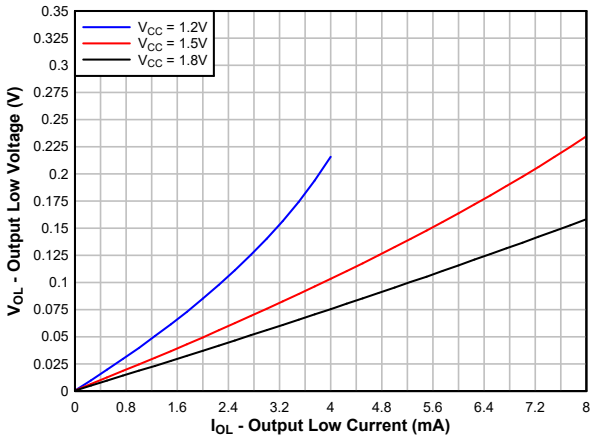


図 5-4. Typical (T_A=25°C) Output Low Voltage (V_{OL}) vs Sink Current (I_{OL})

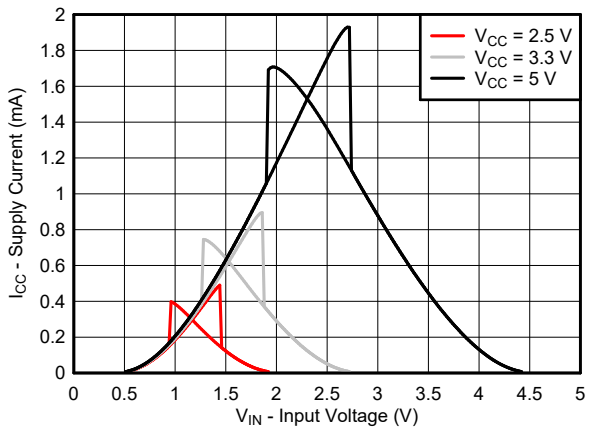


図 5-5. Typical (T_A=25°C) Supply Current (I_{CC}) vs Input Voltage (V_{IN})

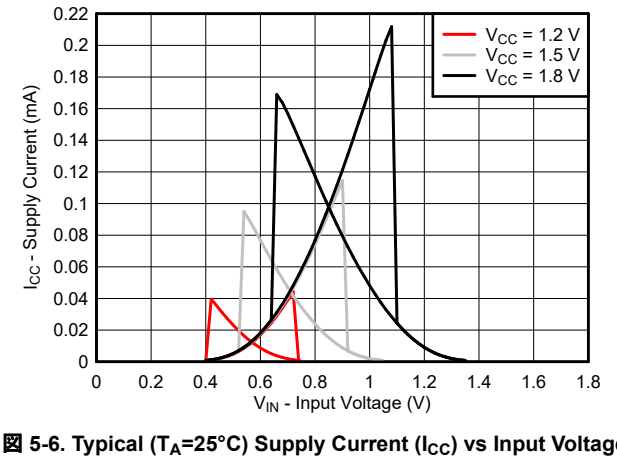


図 5-6. Typical (T_A=25°C) Supply Current (I_{CC}) vs Input Voltage (V_{IN})

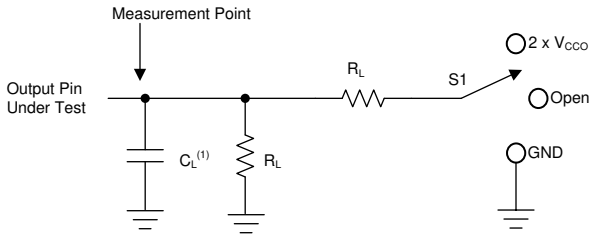
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6 Parameter Measurement Information

6.1 Load Circuit and Voltage Waveforms

Unless otherwise noted, generators supply all input pulses that have the following characteristics:

- f = 1MHz
- Z_O = 50Ω
- Δt/ΔV ≤ 1ns/V

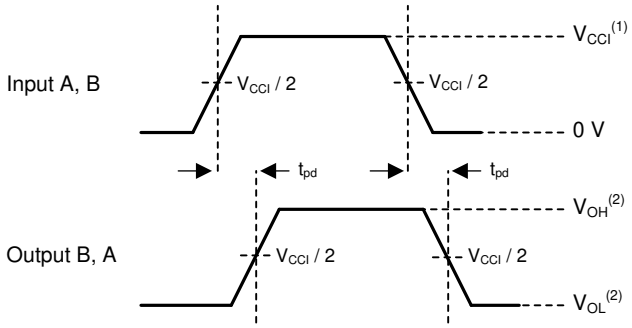


A. C_L includes probe and jig capacitance.

図 6-1. Load Circuit

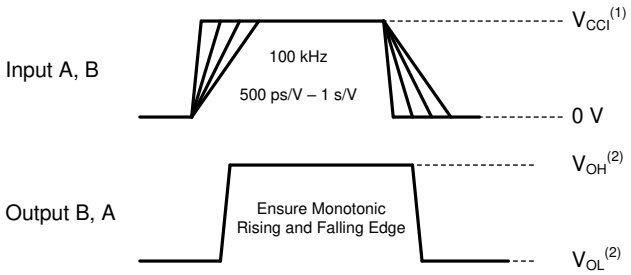
表 6-1. Load Circuit Conditions

Parameter		V_{CCO}	R_L	C_L	S_1	V_{TP}
t_{pd}	Propagation (delay) time	1.1V – 5.5V	10kΩ	5pF	Open	N/A
t_{en}, t_{dis}	Enable time, disable time	1.1V – 1.6V	10kΩ	5pF	2 × V_{CCO}	0.1V
		1.65V – 2.7V	10kΩ	5pF	2 × V_{CCO}	0.15V
		3.0V – 5.5V	10kΩ	5pF	2 × V_{CCO}	0.3V
t_{en}, t_{dis}	Enable time, disable time	1.1V – 1.6V	10kΩ	5pF	GND	0.1V
		1.65V – 2.7V	10kΩ	5pF	GND	0.15V
		3.0V – 5.5V	10kΩ	5pF	GND	0.3V



1. V_{CCI} is the supply pin associated with the input port.
2. V_{OH} and V_{OL} are typical output voltage levels that occur with specified R_L, C_L, and S_1

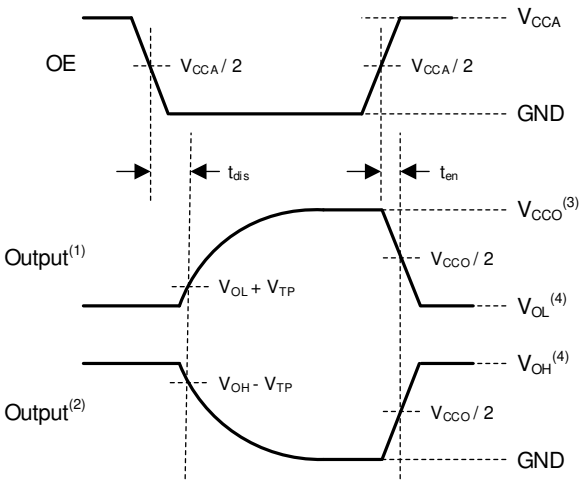
図 6-2. Propagation Delay



1. V_{CCI} is the supply pin associated with the input port.
2. V_{OH} and V_{OL} are typical output voltage levels that occur with specified R_L, C_L, and S_1

図 6-3. Input Transition Rise and Fall Rate

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1. Output waveform on the condition that input is driven to a valid Logic Low.
2. Output waveform on the condition that input is driven to a valid Logic High.
3. V_{CCO} is the supply pin associated with the output port.
4. V_{OH} and V_{OL} are typical output voltage levels with specified R_L, C_L, and S_1.

図 6-4. Enable Time And Disable Time

7 Detailed Description

7.1 Overview

The TXU0104 / TXUN0104 is a 4-bit translating transceiver that uses two individually configurable power-supply rails. The device is operational with V_{CCA} and V_{CCB} supplies as low as 1.1V and as high as 5.5V. Additionally, the device can be operated with V_{CCA} = V_{CCB}. The A port is designed to track V_{CCA}, and the B port is designed to track V_{CCB}.

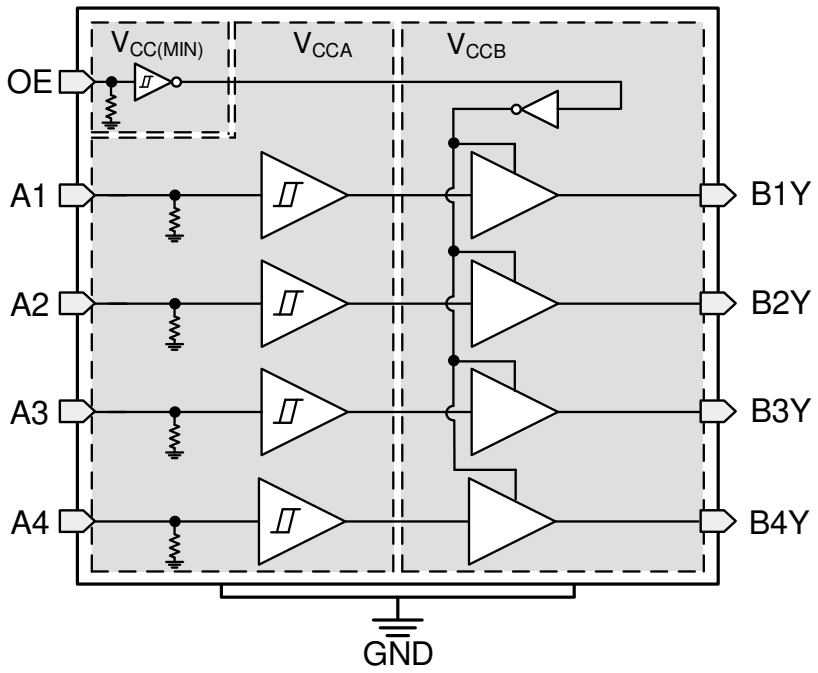
The TXU0104 / TXUN0104 device is designed for asynchronous communication between data buses, and transmits data with fixed direction from the A bus to the B bus on some channels and from the B bus to the A bus on the remaining channels. The output-enable input is used to disable the outputs so the buses are effectively isolated. The output-enable pin of the TXU0104 / TXUN0104 can be referenced to either V_{CCA} or V_{CCB}. On the TXU0104, the OE pin can be left floating or externally pulled down to ground to ensure the high-impedance state of the level shifter outputs during power up or power down. On the TXUN0104, the $\overline{OE}$ pin needs to be externally pulled up to VCC to ensure the high-impedance state of the level shifter outputs during power up or power down.

This device is fully specified for partial-power-down applications using the I_{off} current. The I_{off} protection circuitry ensures that no excessive current is drawn from or sourced into an input or output while the device is powered down.

The VCC isolation or VCC disconnect feature ensures that if either VCC is less than 100 mV or disconnected with the complementary supply within recommended operating conditions, outputs are disabled and set to the high-impedance state while the supply current is maintained. The $I_{off-float}$ circuitry ensures that no excessive current is drawn from or sourced into an input or output while the supply is floating.

Glitch-free power supply sequencing allows either supply rail to be powered on or off in any order while providing robust power sequencing performance.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 CMOS Schmitt-Trigger Inputs with Integrated Pulldowns

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the セクション 5.5. The worst case resistance is calculated with the maximum input voltage, given in the セクション 5.1, and the maximum input leakage current, given in the Electrical Characteristics, using ohm's law (R = V ÷ I).

The Schmitt-trigger input architecture provides hysteresis as defined by ΔV_T in the Electrical Characteristics, which makes this device extremely tolerant to slow or noisy inputs. Driving the inputs slowly will increase dynamic current consumption of the device. See Understanding Schmitt Triggers for additional information regarding Schmitt-trigger inputs.

7.3.1.1 Inputs with Integrated Static Pull-Down Resistors

This device has 5MΩ typical integrated weak pull-downs for each input. This feature allows all inputs to be left floating without the concern for unstable outputs or increased current consumption. This also helps to reduce external component count for applications where not all channels are used or need to be fixed low. If an external pull-up is required, it should be no larger than 1MΩ to avoid contention with the 5MΩ internal pull-down.

7.3.2 Control Logic (OE / $\overline{OE}$) with $V_{CC(MIN)}$ Circuitry

The output-enable input (OE / $\overline{OE}$) is used to disable the outputs so the buses are effectively isolated. The output-enable pin of the TXU0x04 has $V_{CC(MIN)}$ circuitry, which allows the OE / $\overline{OE}$ pins to operate with the lower supply voltage. The *Over-Voltage Tolerant Inputs* feature allows the OE / $\overline{OE}$ pins to operate with the higher supply voltage. This combination means that the enable pin can be referenced to either V_{CCA} or V_{CCB} supply. Multiple permutations of each device are possible since the controller can be placed on either the A or B port and can still control the enable pin.

7.3.3 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. セクション 5.1 defines the electrical and thermal limits that must be followed at all times.

7.3.4 Partial Power Down (I_{off})

The inputs and outputs for this device enter a high-impedance state when the device is powered down, inhibiting current backflow into the device. The I_{off} in the セクション 5.5 specifies the maximum leakage into or out of any input or output pin on the device.

7.3.5 VCC Isolation and V_{CC} Disconnect

The outputs for this device are disabled and enter a high-impedance state when either supply is <100 mV or left floating (disconnected), with the complementary supply within recommended operating conditions. It is recommended that the inputs are kept low before floating (disconnecting) either supply.

The $I_{CCx(floating)}$ in the セクション 5.5 specifies the maximum supply current. The $I_{off(float)}$ in the セクション 5.5 specifies the maximum leakage into or out of any input or output pin on the device.

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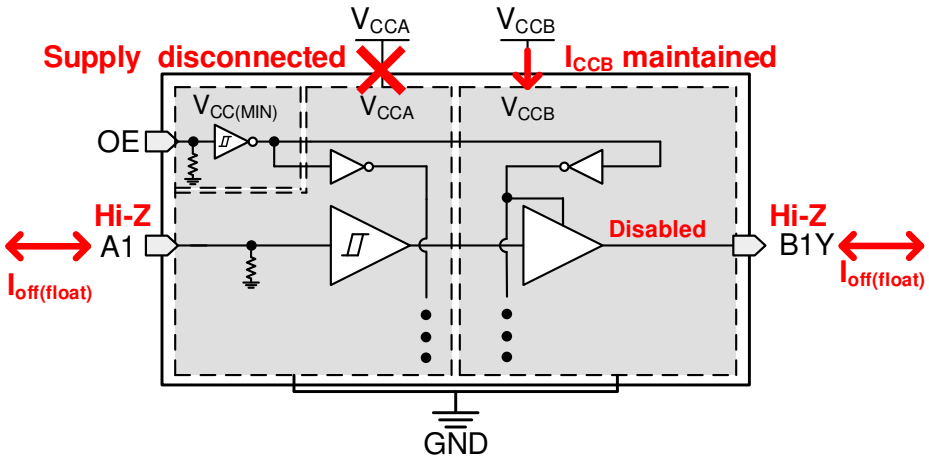


図 7-1. V_{CC} Disconnect Feature (TXU0104)

7.3.6 Over-Voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the セクション 5.3.

7.3.7 Glitch-Free Power Supply Sequencing

Either supply rail may be powered on or off in any order without producing a glitch on the inputs or outputs (that is, where the output erroneously transitions to VCC when it should be held low or vice versa). Glitches of this nature can be misinterpreted by a peripheral as a valid data bit, which could trigger a false device reset of the peripheral, a false device configuration of the peripheral, or even a false data initialization by the peripheral.

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7.3.8 Negative Clamping Diodes

図 7-2 depicts the inputs and outputs to this device that have negative clamping diodes.

> **注意**
>
> Voltages beyond the values specified in the セクション 5.1 table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

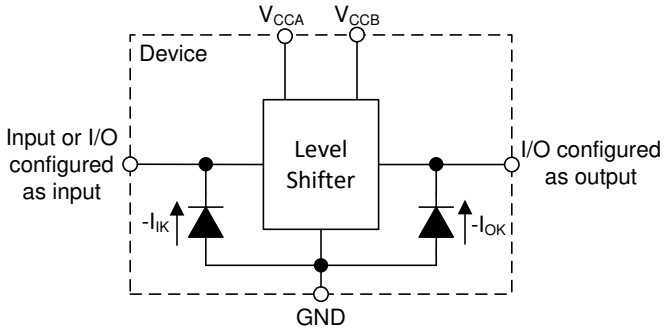


図 7-2. Electrical Placement of Clamping Diodes for Each Input and Output

7.3.9 Fully Configurable Dual-Rail Design

The V_{CCA} and V_{CCB} pins can be supplied at any voltage from 1.1V to 5.5V, making the device suitable for translating between any of the voltage nodes (1.2V, 1.5V, 1.8V, 3.3V, and 5.0V).

7.3.10 Supports High-Speed Translation

The TXU0104 / TXUN0104 device can support high data-rate applications. The translated signal data rate can be up to 200 Mbps when the signal is translated from 3.3 V to 5.0 V.

7.4 Device Functional Modes

表 7-1. Function Table

CONTROL INPUTS		Port Status		OPERATION
OE (TXU0104)	$\overline{OE}$ (TXUN0104)	Input	Output	
H	L	L	L	Unidirectional non-inverting voltage translation
H	L	H	H	Unidirectional non-inverting voltage translation
L	H	X	Hi-Z	Isolation

8 Application and Implementation

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8.1 Application Information

The TXU0104 / TXUN0104 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The TXU0104 / TXUN0104 device is ideal for use in applications where a push-pull driver is connected to the data Inputs. The maximum data rate can be up to 200Mbps when device translates a signal from 3.3V to 5.0V.

8.2 Typical Application

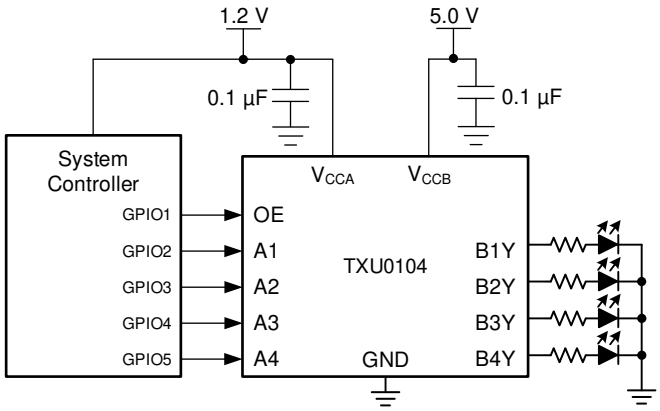


図 8-1. TXU0104 LED Driver Application

8.2.1 Design Requirements

Use the parameters listed in 表 8-1 for this design example.

表 8-1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES
Input voltage range	1.1V to 5.5V
Output voltage range	1.1V to 5.5V

8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the TXU0104 device to determine the input voltage range. For a valid logic-high, the value must exceed the positive-going input-threshold voltage (V_{T+}) of the input port. For a valid logic low the value must be less than the negative-going input-threshold voltage (V_{T-}) of the input port.
- Output voltage range
  - Use the supply voltage of the device that the TXU0104 device is driving to determine the output voltage range.

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8.2.3 Application Curve

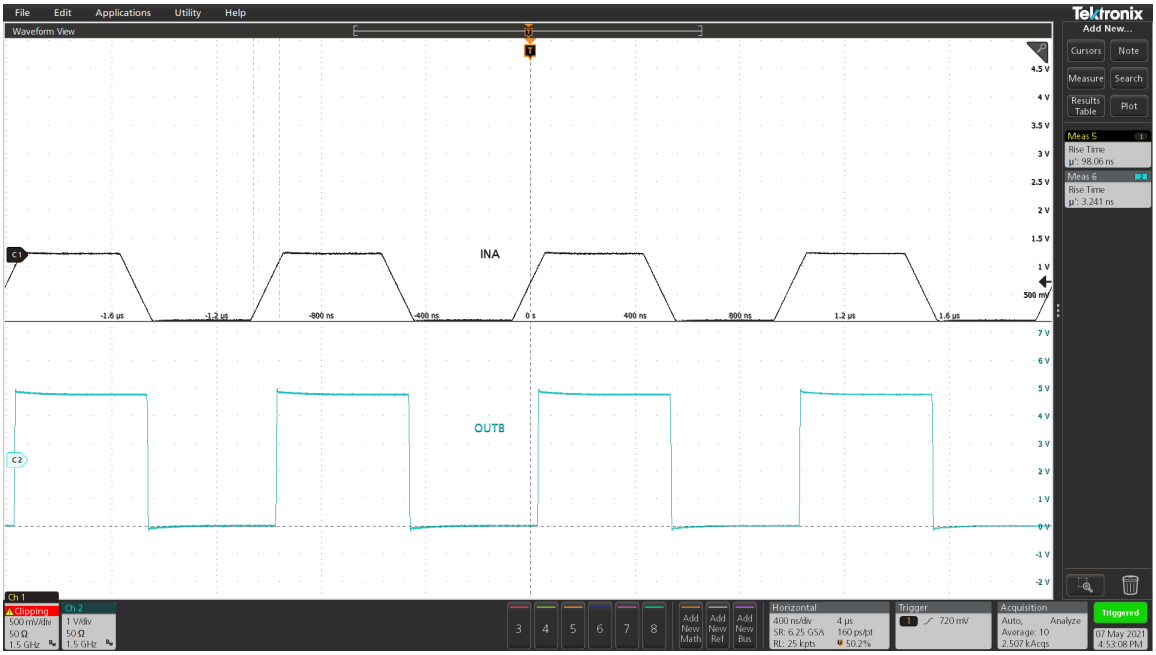


図 8-2. Up Translation at 1MHz (1.2V to 5V)

8.3 Power Supply Recommendations

Always apply a ground reference to the GND pins first. This device is designed for glitch free power sequencing without any supply sequencing requirements such as ramp order or ramp rate.

セクション 7.3.7 describes how this device was designed with various power supply sequencing methods in mind to help prevent unintended triggering of downstream devices.

8.4 Layout

8.4.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines are recommended:

- Use bypass capacitors on the power supply pins and place them as close to the device as possible. A 0.1µF capacitor is recommended, but transient performance can be improved by having 1µF and 0.1µF capacitors in parallel as bypass capacitors.
- The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing.

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8.4.2 Layout Example

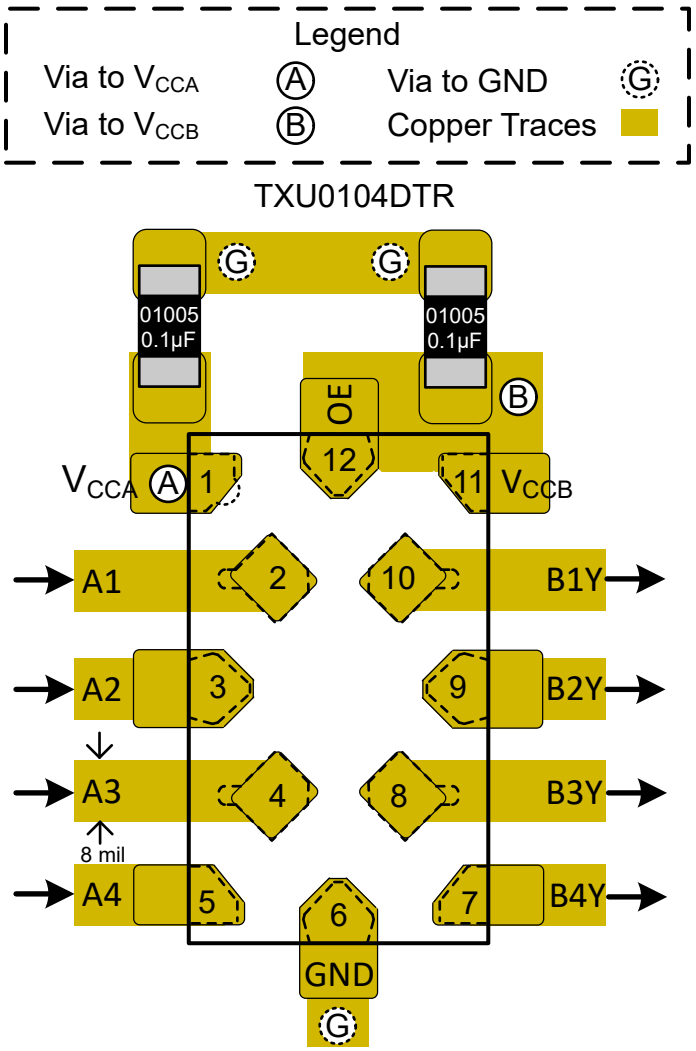


図 8-3. Layout Example – TXU0104

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9 Device and Documentation Support

9.1 Device Support

9.2 Documentation Support

9.2.1 Related Documentation

- Texas Instruments, *Understanding Schmitt Triggers* application report
- Texas Instruments, *CMOS Power Consumption and C_{pd} Calculation* application report

9.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (September 2021) to Revision B (February 2025)	Page
• データシート全体にわたって TXUN0104 情報を追加	1

Changes from Revision * (May 2021) to Revision A (September 2021)	Page
• TXU0104BQA、TXU0104RUT、TXU0104DTR デバイスのステータスを「*製品プレビュー*」から「*量産データ*」	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TXU0104BQAR	Active	Production	WQFN (BQA) | 14	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	TX0104
TXU0104BQAR.A	Active	Production	WQFN (BQA) | 14	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	TX0104
TXU0104BQARG4	Active	Production	WQFN (BQA) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TX0104
TXU0104BQARG4.A	Active	Production	WQFN (BQA) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TX0104
TXU0104DTRR	Active	Production	X2QFN (DTR) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1KJ
TXU0104DTRR.A	Active	Production	X2QFN (DTR) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1KJ
TXU0104DTRRG4.A	Active	Production	X2QFN (DTR) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1KJ
TXU0104PWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	TXU0104
TXU0104PWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TXU0104
TXU0104PWRG4	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TXU0104
TXU0104PWRG4.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TXU0104
TXU0104RUTR	Active	Production	UQFN (RUT) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1J4
TXU0104RUTR.A	Active	Production	UQFN (RUT) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1J4
TXU0104RUTRG4.A	Active	Production	UQFN (RUT) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1J4
TXUN0104RUTR	Active	Production	UQFN (RUT) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1UE
TXUN0104RUTR.A	Active	Production	UQFN (RUT) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1UE

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TXU0104 :

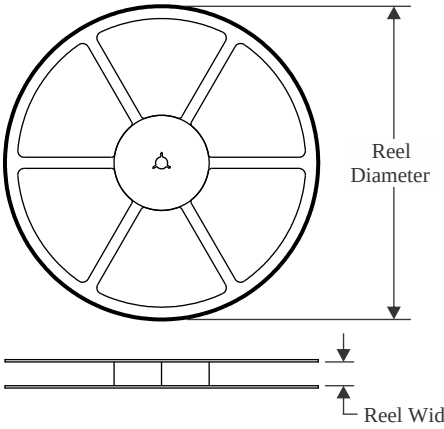
- Automotive : TXU0104-Q1

NOTE: Qualified Version Definitions:

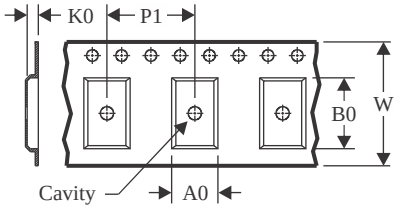
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

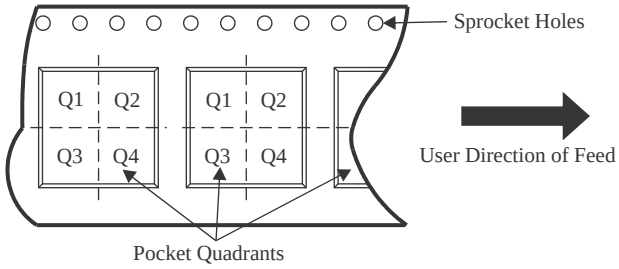


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

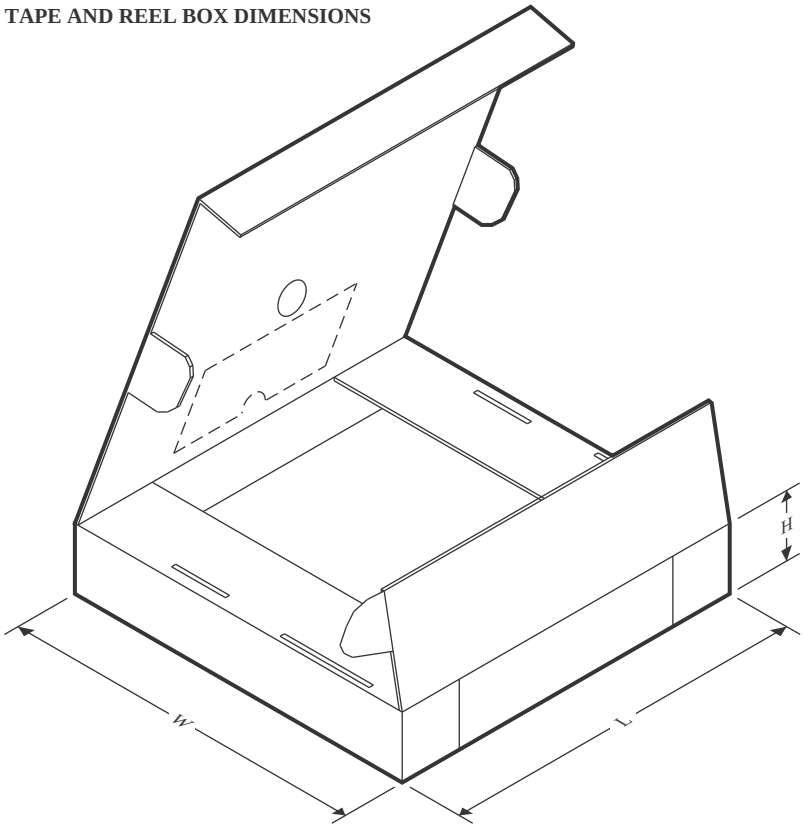
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXU0104BQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
TXU0104BQARG4	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
TXU0104DTRR	X2QFN	DTR	12	3000	180.0	9.5	1.18	1.88	0.53	4.0	8.0	Q1
TXU0104PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TXU0104PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TXU0104PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.3	1.6	8.0	12.0	Q1
TXU0104PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TXU0104RUTR	UQFN	RUT	12	3000	180.0	9.5	1.9	2.2	0.7	4.0	8.0	Q1
TXUN0104RUTR	UQFN	RUT	12	3000	180.0	8.4	2.0	2.3	0.75	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

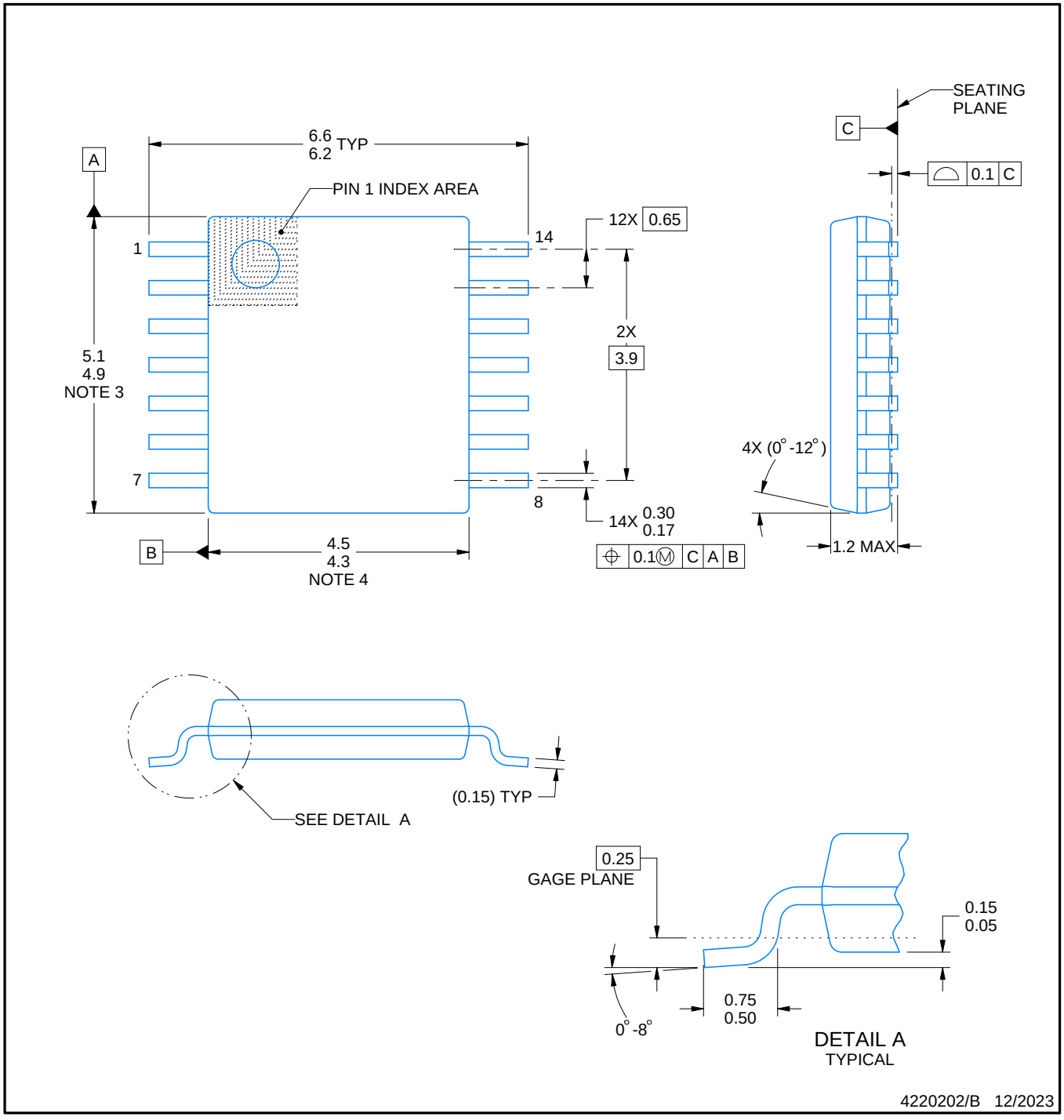
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXU0104BQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
TXU0104BQARG4	WQFN	BQA	14	3000	210.0	185.0	35.0
TXU0104DTRR	X2QFN	DTR	12	3000	189.0	185.0	36.0
TXU0104PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TXU0104PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
TXU0104PWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TXU0104PWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0
TXU0104RUTR	UQFN	RUT	12	3000	189.0	185.0	36.0
TXUN0104RUTR	UQFN	RUT	12	3000	210.0	185.0	35.0

PACKAGE OUTLINE

PW0014A

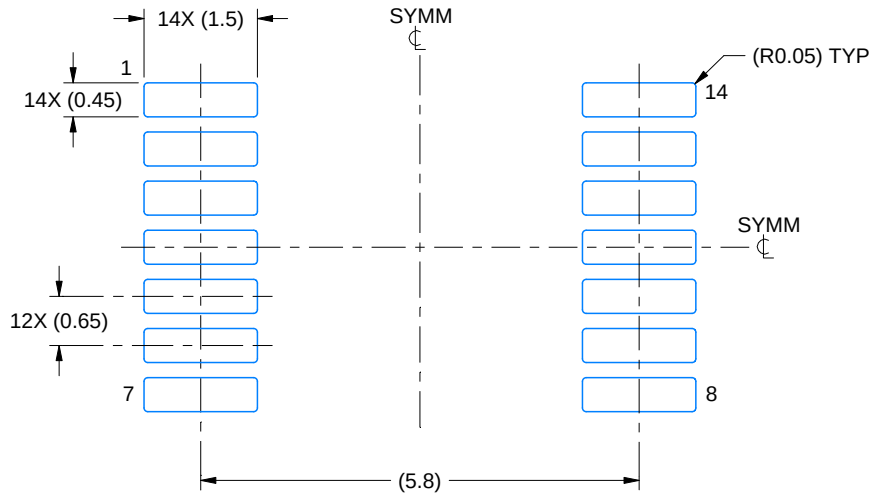
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

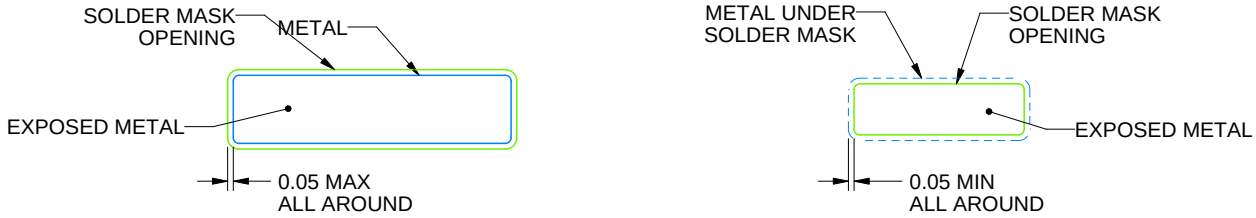


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

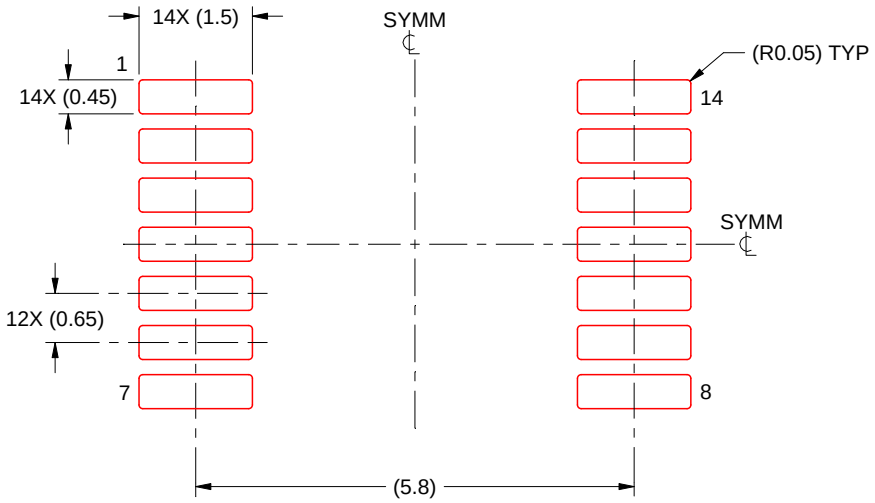


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

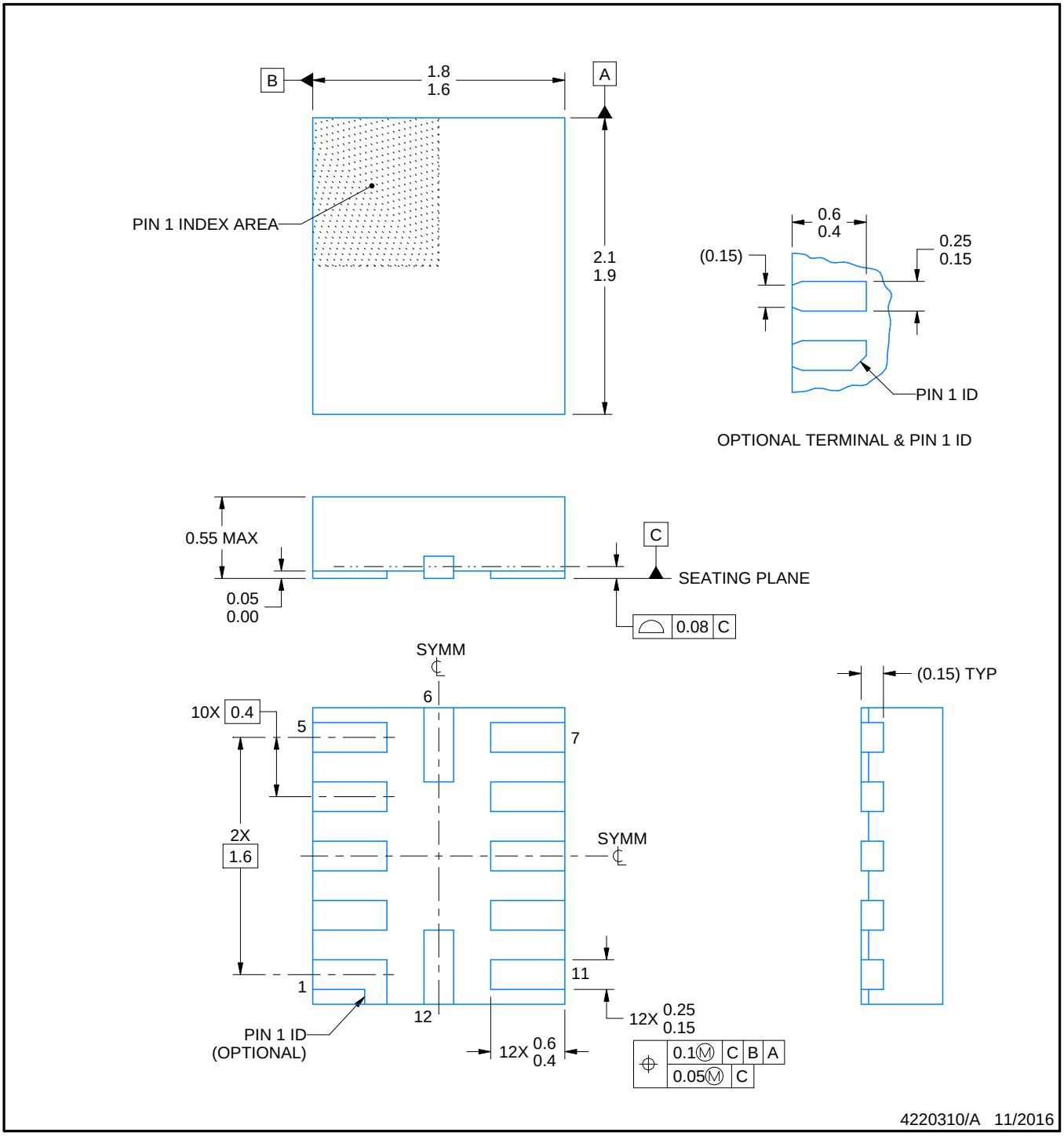
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RUT0012A

PACKAGE OUTLINE

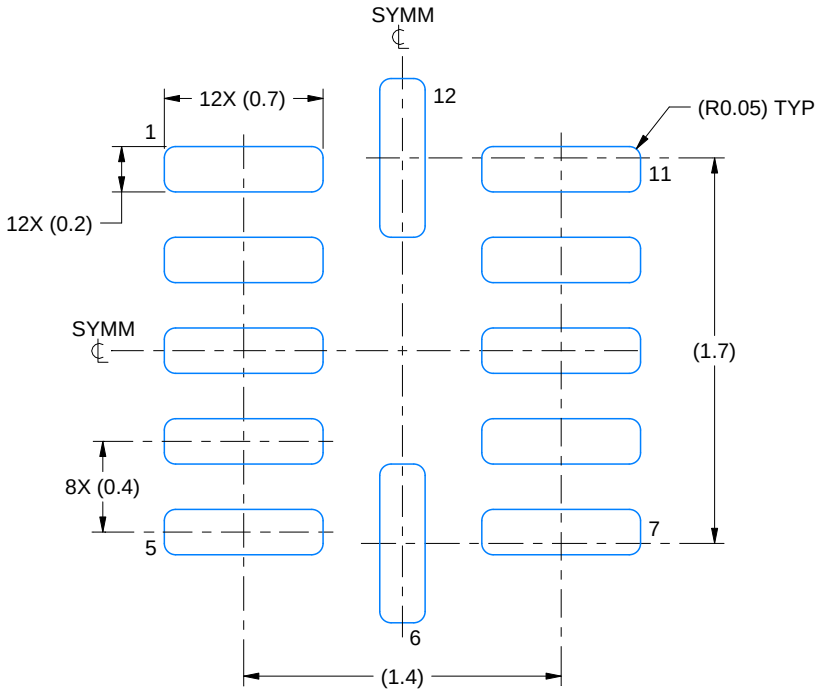
UQFN - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

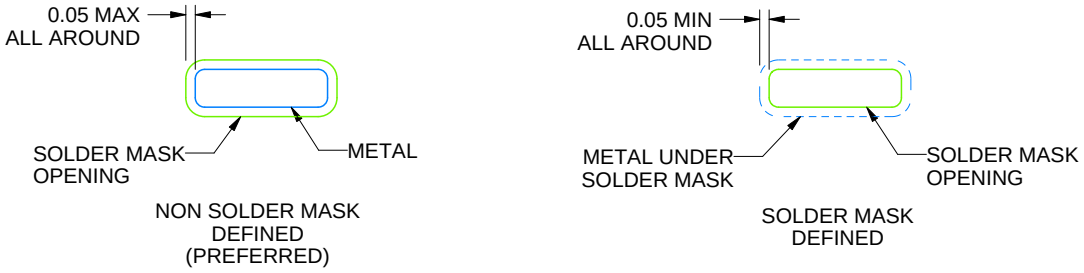


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X

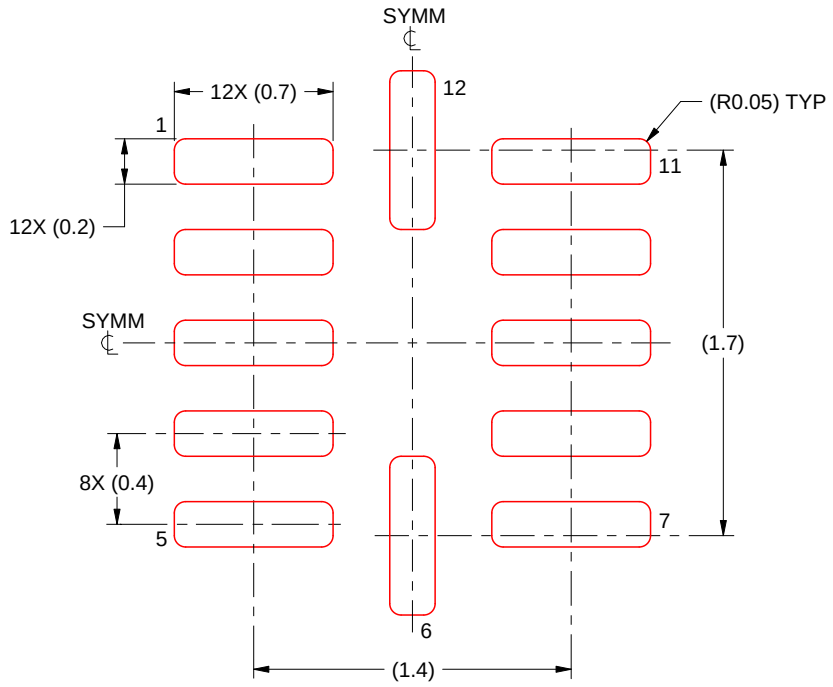


SOLDER MASK DETAILS

4220310/A 11/2016

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 30X

4220310/A 11/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

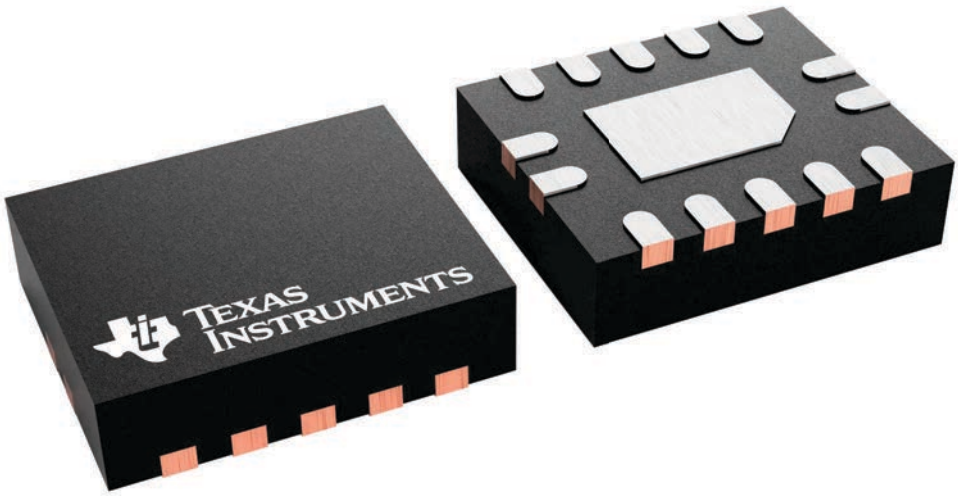
BQA 14

WQFN - 0.8 mm max height

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

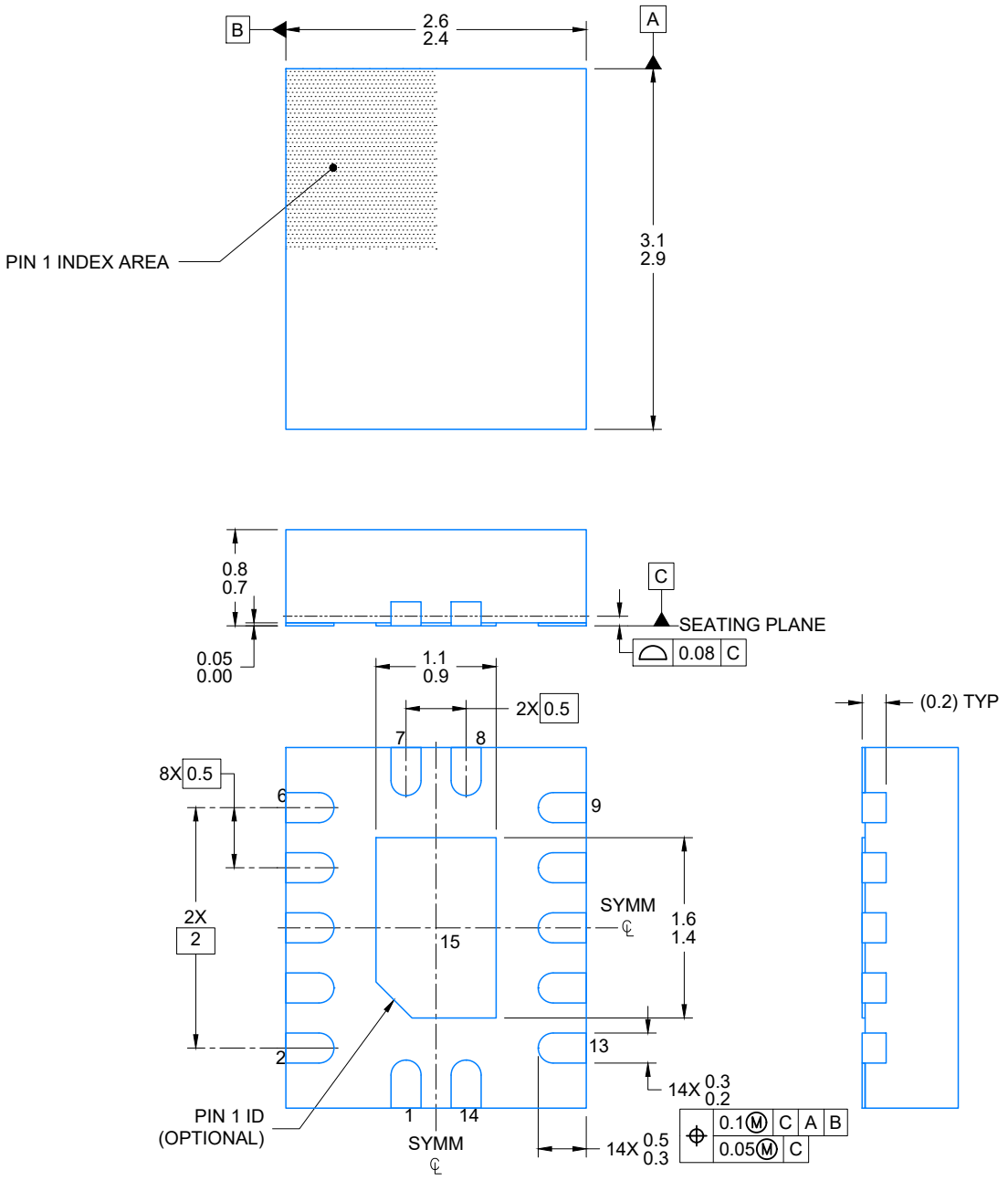


PACKAGE OUTLINE

BQA0014A

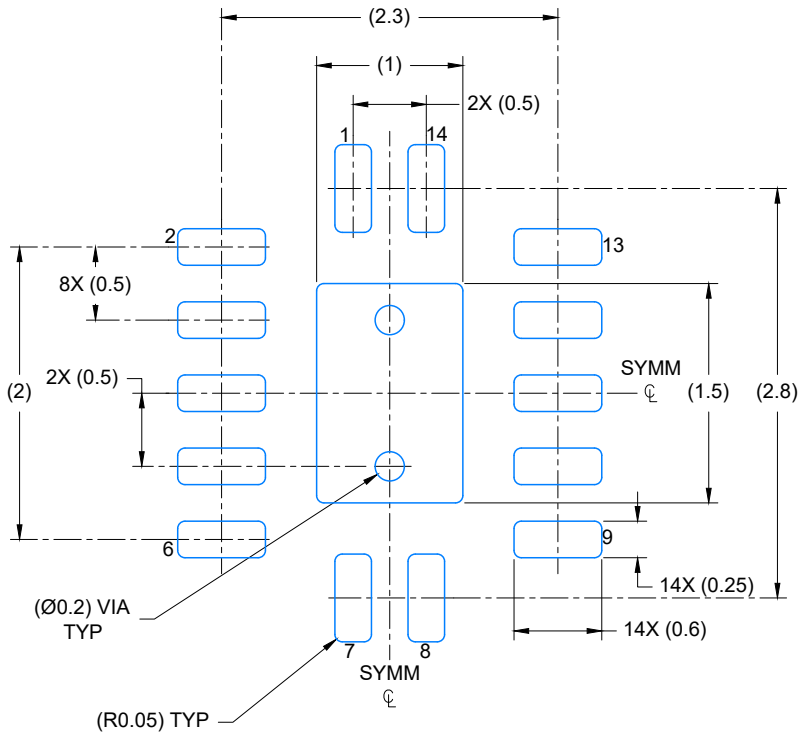
WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD

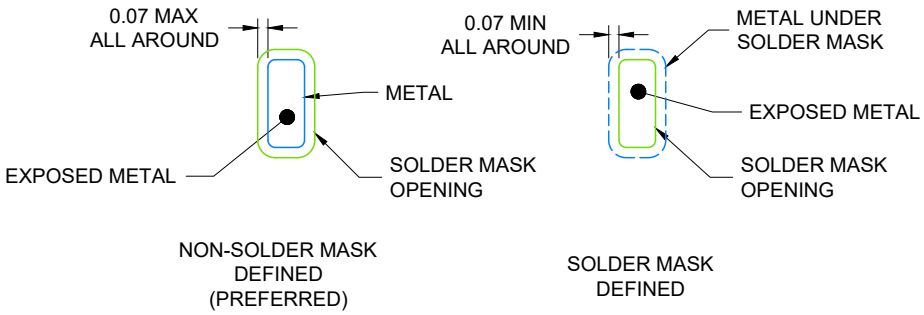


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



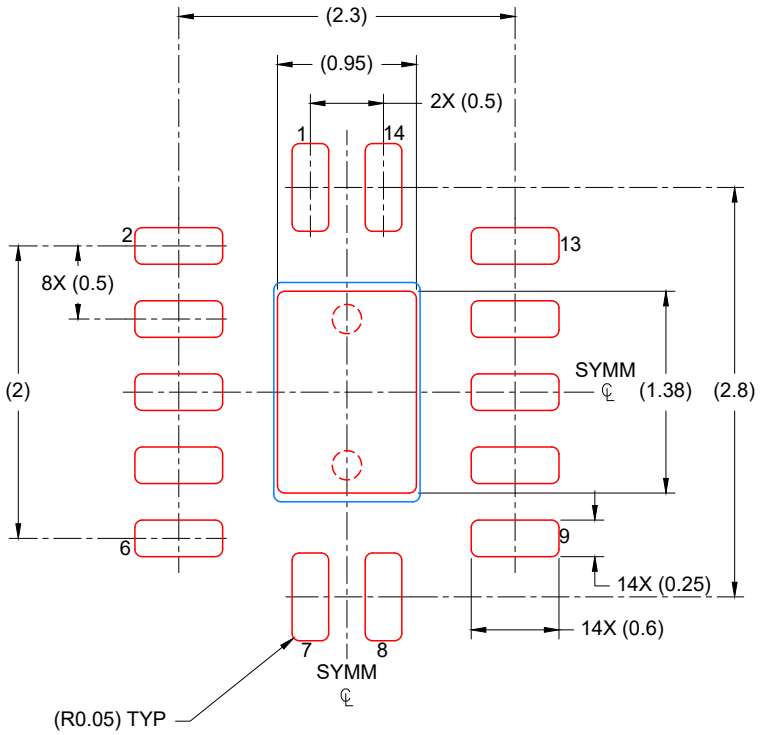
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224636/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
88% PRINTED COVERAGE BY AREA
SCALE: 20X

4224636/A 11/2018

NOTES: (continued)

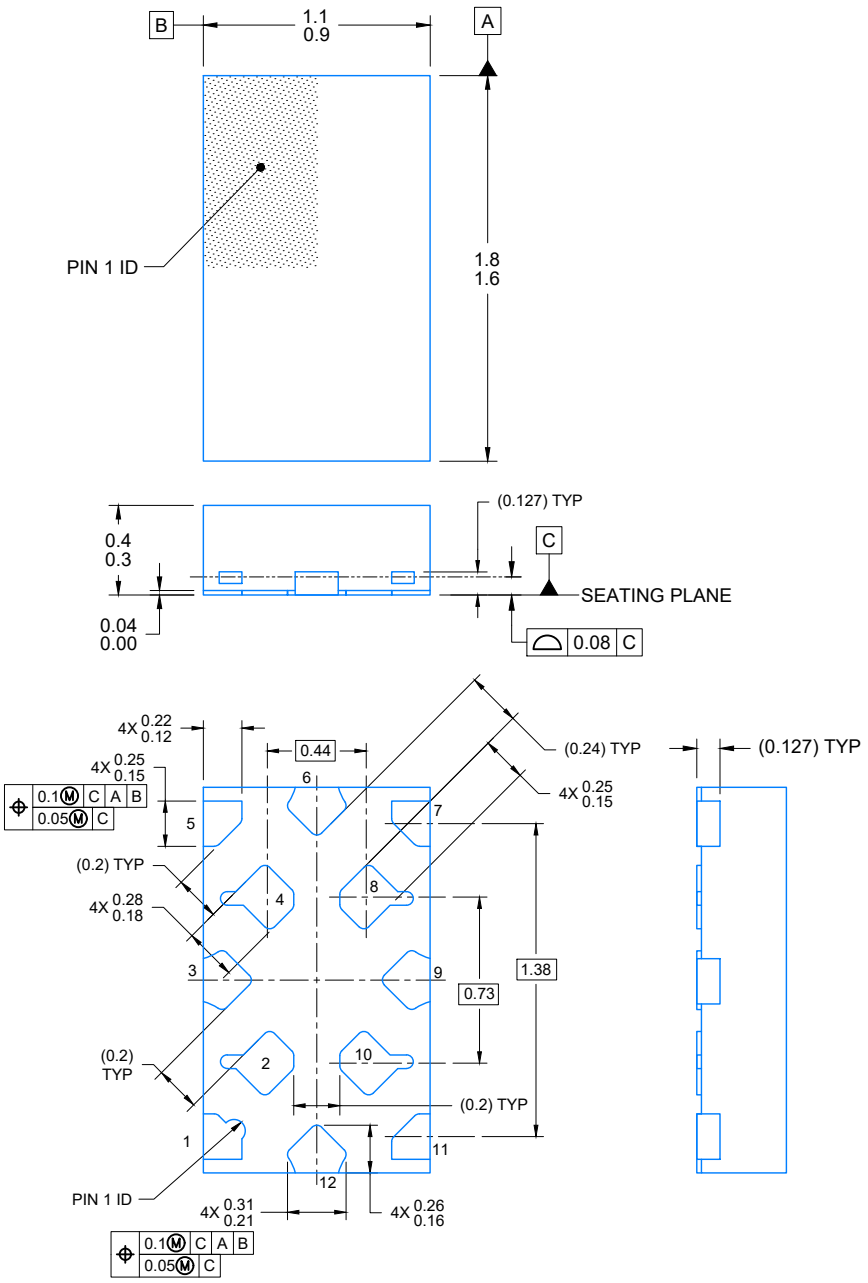
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DTR0012A

X2QFN - 0.4 mm max height

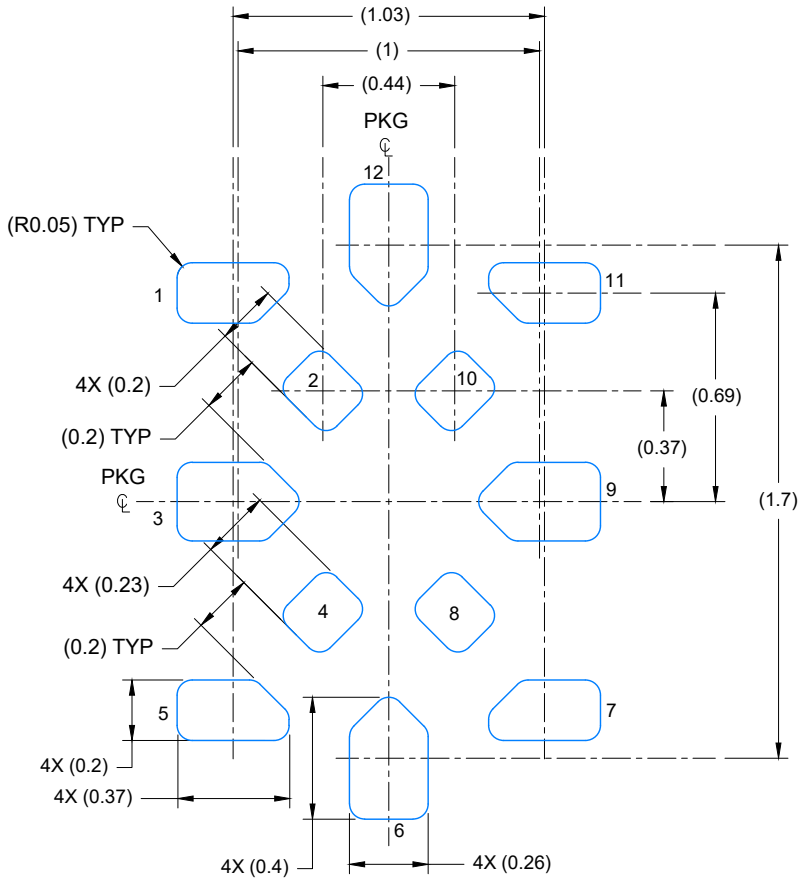
PLASTIC QUAD FLATPACK-NO LEAD



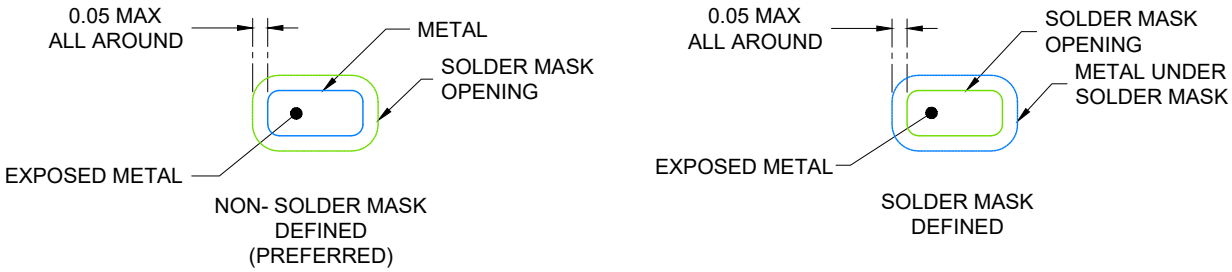
4226527/B 04/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 40X

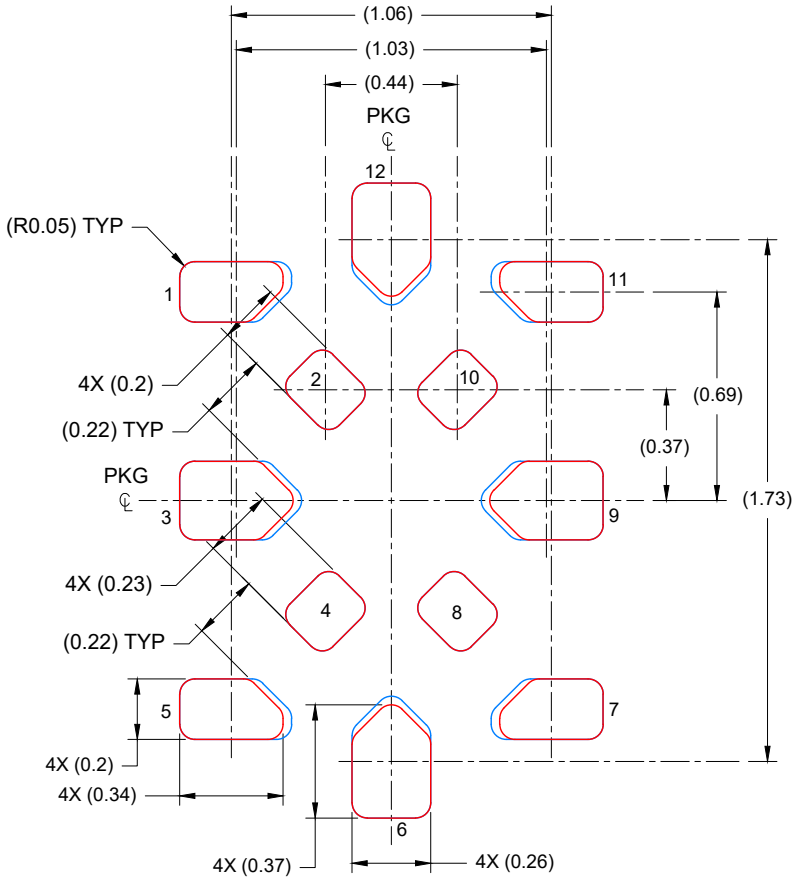


SOLDER MASK DETAILS
NOT TO SCALE

4226527/B 04/2021

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE

BASED ON 0.1 mm THICK STENCIL

SCALE: 40X

4226527/B 04/2021

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月