UC1843A-SP QML Class V、放射線耐性強化の電流モード PWM コントローラ

1 特長

- QML Class V (QMLV)認定済み、SMD 5962-86704
- 5962**P**8670409Vxx
  - 吸収線量(TID) 30krad(Si)までの放射線耐性保証(RHA)
  - MIL-STD-883テスト手法1019.9段落3.13.3.bの定義に従い、1.5xのOver TestにおいてLDR (10 mrad(Si)/s)で45kradの機能および規定のPost-Radiationパラメータ制限に合格
  - 低線量率の感受性を示すが、30kradの合計線量レベルにおいて、MIL-STD-883, TM1019で許容されるPre-Radiationの電気的制限範囲内を維持
- **オフラインおよびDC/DCコンバータ用に最適化**
- **低いスタートアップ電流(0.5mA未満)**
- **トリムされた発振器放電電流**
- **自動的なフィードフォワード補償**
- **パルス単位の電流制限**
- **拡張された負荷応答特性**
- **ヒステリシス付きの低電圧誤動作防止(UVLO)**
- **ダブル・パルス抑制**
- **大電流トーテムポール出力**
- **内部トリム付きのバンドギャップ参照**
- 500kHzでの動作
- 低R_Oのエラー・アンプ

2 アプリケーション

- DC/DCコンバータ
- **各種のトポロジをサポート**
  - フライバック、フォワード、降圧、昇圧
  - 外部インターフェイス回路付きのプッシュプル、ハーフブリッジ、フルブリッジ
- **軍事用温度範囲(-55℃～125℃)で利用可能**

3 概要

UC1843A-SPコントロールICは、UC184xファミリとピン互換の放射線強化版です。このデバイスは、電流モード・スイッチング・モード電源のコントロールに必要な特性を提供し、機能が拡張されています。スタートアップ電流は0.5mA未満に規定され、発振器放電は8.3mAにトリムされています。UVLO時には、5V以上のV_{CC}について、出力ステージは1.2V未満で最低10mAをシンクします。

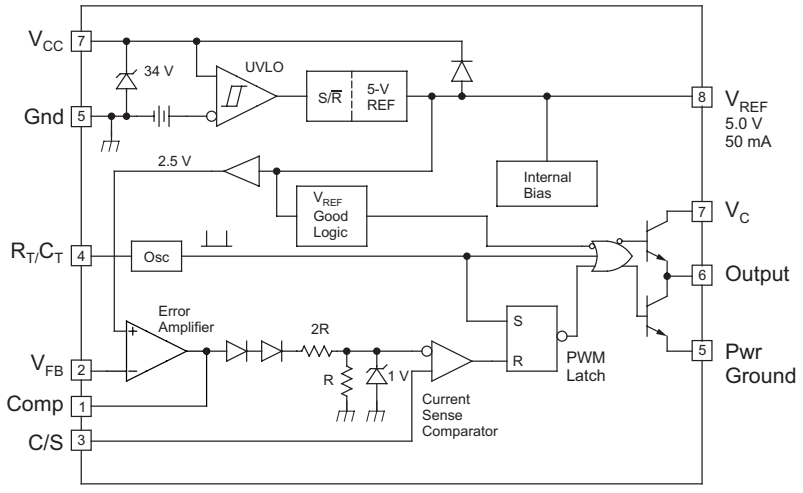
*デバイス比較表*には、このファミリのメンバ間の相違点が示されています。放射線強化版が利用可能かどうか、および注文方法については、各製品のデータシートを参照してください。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
UC1843A-SP	CDIP (8)	6.67mm×9.60mm
	LCCC (20)	8.89mm×8.89mm
	CFP (10)	6.48mm×7.02mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

概略回路図



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4 改訂履歴

2016年12月発行のものから更新 **Page**

- Changed the *Pin Configuration* images ... 3
- Changed CT (pF) To: CT (µF) in Equation 1 ... 15

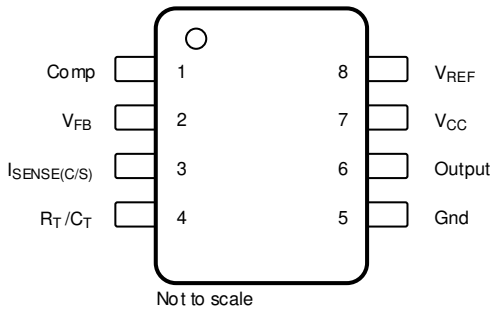
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5 Device Comparison Table

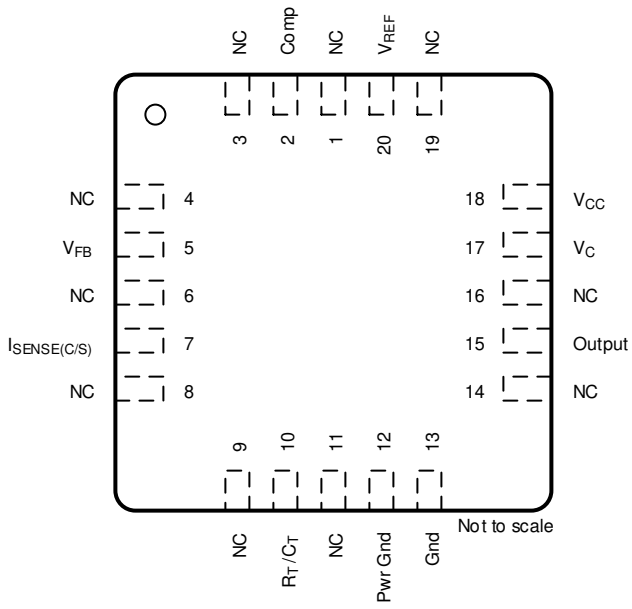
PART NO.	UVLO ON	UVLO OFF	MAXIMUM DUTY CYCLE
UC1842A	16 V	10 V	<100%
UC1843A	8.5 V	7.9 V	<100%
UC1844A	16 V	10 V	<50%

6 Pin Configuration and Functions

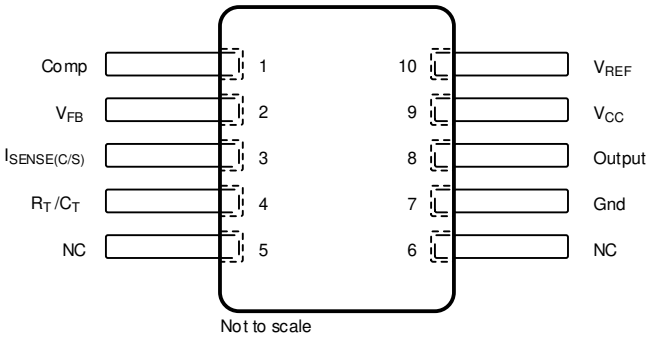
JG Package
8-Pin CDIP
Top View



FK Package
20-Pin LCCC
Top View



HKU Package
10-Pin CFP
Top View



Pin Functions

PIN				I/O	DESCRIPTION
NAME	CDIP	LCCC	CFP		
Comp	1	2	1	I	Error amplifier output.
V_{FB}	2	5	2	I	Voltage feedback input to error amplifier.
$I_{SENSE(C/S)}$	3	7	3	I	Current sense comparator input pin.
R_T/C_T	4	10	4	I	RC time constant input to oscillator.
NC	—	1, 3, 4, 6, 8, 9, 11, 14, 16, 19	5, 6	—	No connect.
Pwr Gnd	—	12	—	—	Output section ground.
Gnd	5	13	7	—	Ground.
Output	6	15	8	O	Regulated output.
V_C	—	17	—	—	Output section supply voltage.
V_{CC}	7	18	9	—	Unregulated supply voltage.
V_{REF}	8	20	10	O	5-V internally generated reference.

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7 Specifications

7.1 Absolute Maximum Ratings[1][2]

over operating free-air temperature (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage, low-impedance source		30	V
V_I	Input voltage (V_{FB}, I_{SENSE})	–0.3	6.3	V
	Supply current	Self limiting		
I_O	Output current		±1	A
	Error amplifier output sink current		10	mA
	Output energy (capacitive load)		5	μJ
P_D	Power dissipation (T_A = 25°C)		1	W
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground. Currents are positive in, negative out of the specified terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±4000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (T_A = T_J = –55°C to 125°C), unless otherwise noted

		MIN	MAX	UNIT
V_{CC}	Supply voltage	12	25	V
	Sink/source output current (continuous or time average)	0	200	mA
	Reference load current	0	20	mA

7.4 Thermal Information

THERMAL METRIC[1]		UC1843A-SP			UNIT
		JG (CDIP)	FK (LCCC)	HKU (CFP)	
		8 PINS	20 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	103	—	51.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	9.6	9.0	6.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	69.2	—	31.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	13.9	—	5.42	°C/W
ψ_{JB}	Junction-to-board characterization parameter	73	—	31	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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7.5 Electrical Characteristics

V_{CC} = 15 V(1), R_T = 10 kΩ, C_T = 3.3 nF, T_A = T_J = –55°C to 125°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
REFERENCE						
Output voltage	T_J = 25°C, I_O = 1 mA		4.95	5	5.06	V
Line regulation	V_{IN} = 12 to 25 V			6	20	mV
Load regulation	I_O = 1 to 20 mA			6	25	mV
Temperature stability(2)(3)				0.2	0.4	mV/°C
Total output variation(2)	Over line, load, and temperature		4.9		5.1	V
Output noise voltage	10 Hz ≤ f ≤ 10 kHz, T_J = 25°C			50		μV
Long-term stability	1000 hours, T_A = 125°C(2)			5	25	mV
Short-circuit output current			–30	–100	–180	mA
OSCILLATOR						
Initial accuracy	T_J = 25°C(4)		47	52	57	kHz
Voltage stability	V_{CC} = 12 to 25 V			0.2%	1%	
Temperature stability	T_J = –55°C to 125°C(2)			5%		
Amplitude peak-to-peak	V pin 4(2)			1.7		V
Discharge current	V pin 4 = 2 V(5)	T_J = 25°C	7.8	8.3	8.8	mA
		T_J = Full range	7.5		8.8	mA
ERROR AMPLIFIER						
Input voltage	V_{Comp} = 2.5 V		2.45	2.50	2.55	V
Input bias current				–0.3	–1	μA
Open-loop voltage gain	V_O = 2 to 4 V		65	90		dB
Unity-gain bandwidth	T_J = 25°C(2)		0.7	1		MHz
PSRR	V_{CC} = 12 to 25 V		60	70		dB
Output sink current	V_{FB} = 2.7 V, V_{Comp} = 1.1 V		2	6		mA
Output source current	V_{FB} = 2.3 V, V_{Comp} = 5 V		–0.5	–0.8		mA
High-level output voltage	V_{FB} = 2.3 V, R_L = 15 kΩ to ground		5	6		V
Low-level output voltage	V_{FB} = 2.7 V, R_L = 15 kΩ to V_{REF}			0.7	1.1	V
CURRENT SENSE						
Gain(6)(7)			2.85	3	3.15	V/V
Maximum input signal	V_{Comp} = 5 V(6)		0.9	1	1.1	V
PSRR	V_{CC} = 12 to 25 V(6)			70		dB
Input bias current				–2	–10	μA
Delay to output	V_{ISENSE} = 0 to 2 V(2)			150	300	ns

(1) Adjust V_{CC} above the start threshold before setting at 15 V.
(2) Parameters ensured by design and/or characterization, if not production tested.
(3) Temperature stability, sometimes referred to as average temperature coefficient, is described by the equation: Temperature Stability = V_{REF} (max) – V_{REF} (min) / T_J (max) – T_J (min). V_{REF} (max) and V_{REF} (min) are the maximum and minimum reference voltage measured over the appropriate temperature range. Note that the extremes in voltage do not necessarily occur at the extremes in temperature.
(4) Output frequency equals oscillator frequency for the UC1842A-SP and UC1843A-SP.
(5) This parameter is measured with R_T = 10 kΩ to V_{REF}. This contributes approximately 300 μA of current to the measurement. The total current flowing into the R_T or C_T pin will be approximately 300 μA higher than the measured value.
(6) Parameter measured at trip point of latch with V_{FB} = 0 V.
(7) Gain defined as: G = ΔV_{Comp} / ΔV_{ISENSE}; V_{ISENSE} = 0 to 0.8 V.

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Electrical Characteristics (continued)

V_{CC} = 15 V[1], R_T = 10 kΩ, C_T = 3.3 nF, T_A = T_J = –55°C to 125°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT					
Output low-level voltage	I_{SINK} = 20 mA		0.1	0.4	V
	I_{SINK} = 200 mA		1.5	2.2	
Output high-level voltage	I_{SOURCE} = –20 mA	13	13.5		V
	I_{SOURCE} = –200 mA	12	13.5		
Rise time	C_L = 1 nF, T_J = 25°C[2]		50	150	ns
Fall time	C_L = 1 nF, T_J = 25°C[2]		50	150	ns
UVLO saturation	V_{CC} = 5 V, I_{SINK} = 10 mA		0.7	1.2	V
UNDERVOLTAGE LOCKOUT					
Start threshold		7.8	8.4	9	V
Minimum operation voltage after turnon		7	7.6	8.2	V
PWM					
Maximum duty cycle		94%	96%	100%	
Minimum duty cycle				0%	
TOTAL STANDBY CURRENT					
Start-up current			0.3	0.5	mA
Operating supply current	V_{FB} = V_{ISENSE} = 0 V		11	17	mA
V_{CC} Zener voltage	I_{CC} = 25 mA	30	34		V

7.6 Typical Characteristics

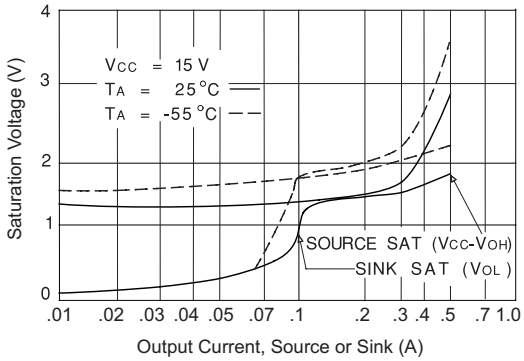


Figure 1. Output Saturation Characteristics

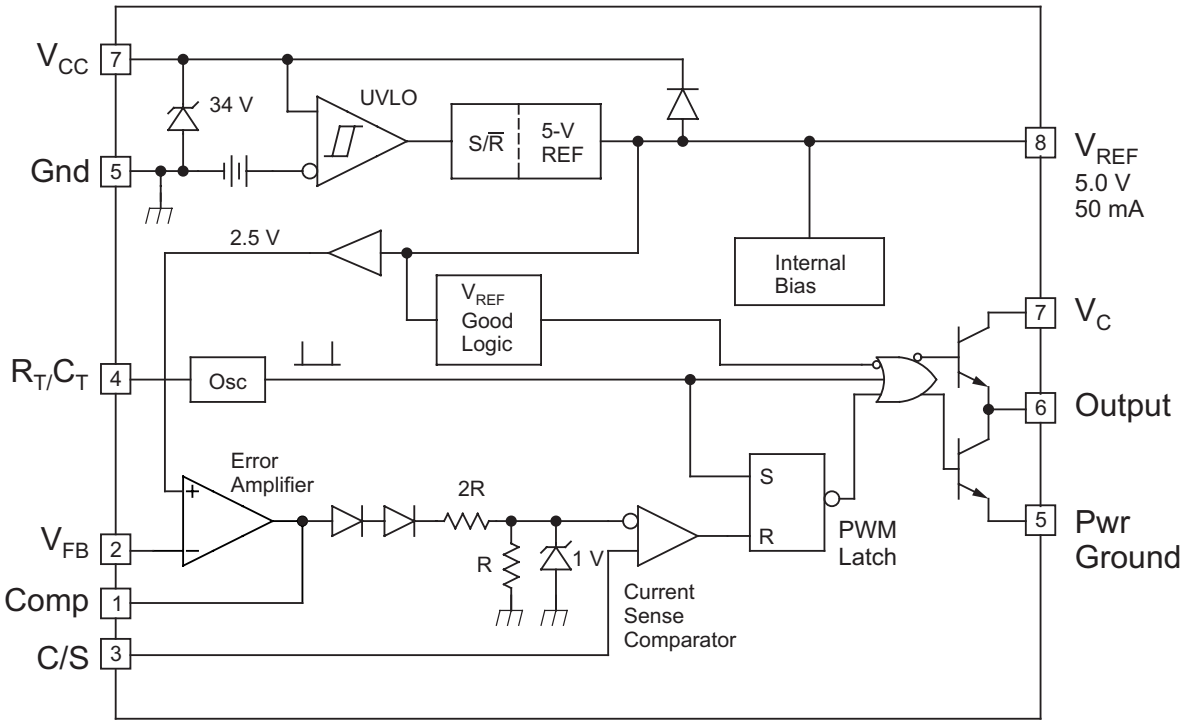
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8 Detailed Description

8.1 Overview

The UC1843A-SP control IC is a pin-for-pin compatible improved version of the UC184x family. Providing the necessary characteristics to control current-mode switched-mode power supplies, this device has improved features. Start-up current is specified to be less than 0.5 mA and oscillator discharge is trimmed to 8.3 mA. During UVLO, the output stage can sink at least 10 mA at less than 1.2 V for V_{CC} over 5 V.

8.2 Functional Block Diagram



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8.3 Feature Description

UC1843A-SP is a current mode controller, used to support various topologies such as forward, flyback, buck, boost and using an external interface circuit will also support half-bridge, full-bridge, and push-pull configurations.

Figure 2 shows the two-loop current-mode control system in a typical buck regulator application. A clock signal initiates power pulses at a fixed frequency. The termination of each pulse occurs when an analog of the inductor current reaches a threshold established by the error signal. In this way, the error signal actually controls peak inductor current. This contrasts with conventional schemes in which the error signal directly controls pulse width without regard to inductor current.

Several performance advantages result from the use of current-mode control. First, an input voltage feed-forward characteristic is achieved; that is, the control circuit instantaneously corrects for input voltage variations without using up any of the error amplifier's dynamic range. Therefore, line regulation is excellent and the error amplifier can be dedicated to correcting for load variations exclusively.

Feature Description (continued)

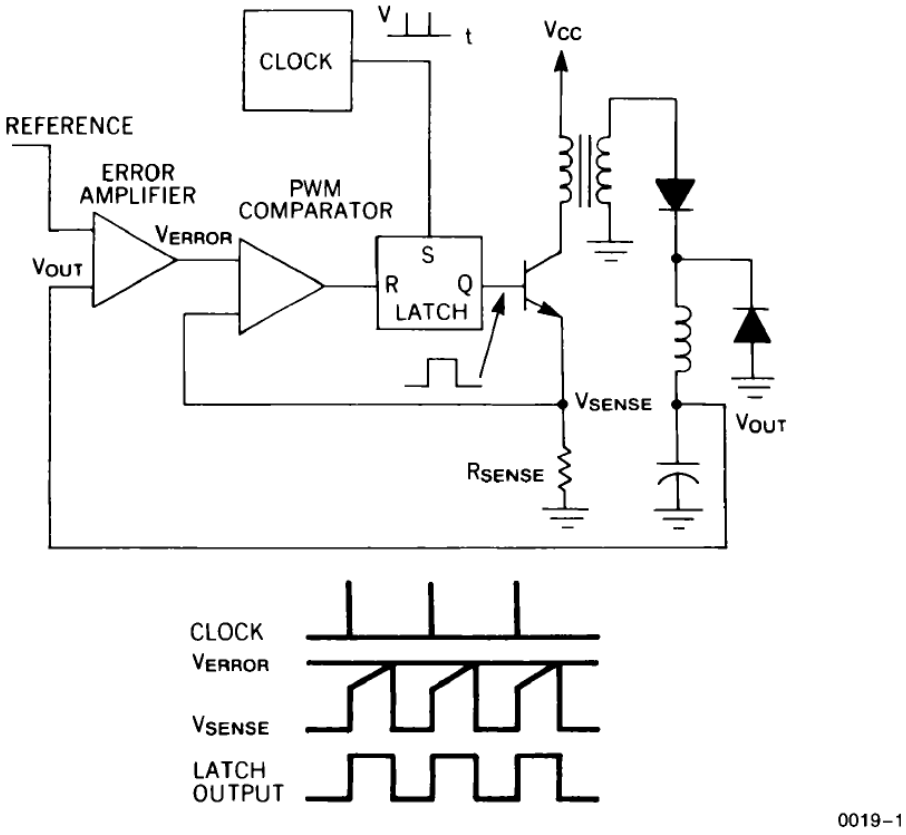


Figure 2. Two-Loop Current-Mode Control System

For converters in which inductor current is continuous, controlling peak current is nearly equivalent to controlling average current. Therefore, when such converters employ current-mode control, the inductor can be treated as an error-voltage-controlled-current-source for the purposes of small-signal analysis (see Figure 3). The two-pole control-to-output frequency response of these converters is reduced to a single-pole (filter capacitor in parallel with load) response. One result is that the error amplifier compensation can be designed to yield a stable closed-loop converter response with greater gain bandwidth than would be possible with pulse-width control, giving the supply improved small-signal dynamic response to changing loads. A second result is that the error amplifier compensation circuit becomes simpler, as shown in Figure 4.

Capacitor Ci and resistor Ri, in Figure 4(A), add a low-frequency zero, which cancels one of the two control-to-output poles of non-current-mode converters. For large signal load changes, in which converter response is limited by inductor slew rate, the error amplifier saturates while the inductor is catching up with the load. During this time, Ci charges to an abnormal level. When the inductor current reaches its required level, the voltage on Ci causes a corresponding error in supply output voltage. The recovery time is $R_{iz}C_i$, which may be long. However, the compensation network of Figure 4(B) can be used where current-mode control has eliminated the inductor pole. Large-signal dynamic response is then greatly improved due to the absence of Ci.

Current limiting is greatly simplified with current-mode control. Pulse-by-pulse limiting is, of course, inherent in the control scheme. Furthermore, an upper limit on the peak current can be established by simply clamping the error voltage. Accurate current limiting allows optimization of magnetic and power semiconductor elements while ensuring reliable supply operation.

Finally, current-mode controlled power stages can be operated in parallel with equal current sharing. This opens the possibility of a modular approach to power supply design.

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Feature Description (continued)

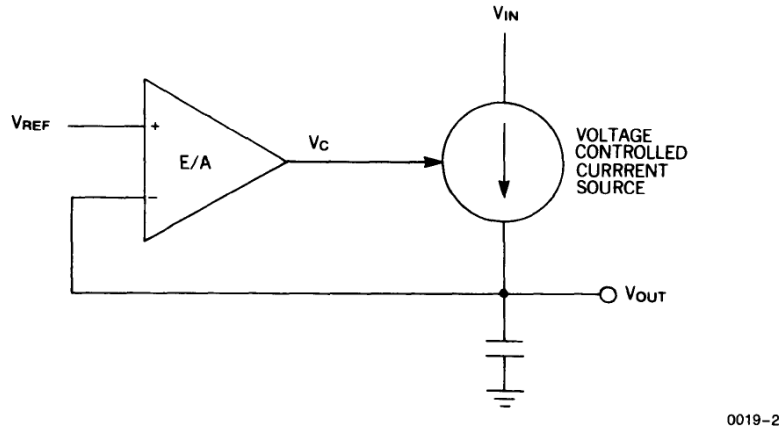
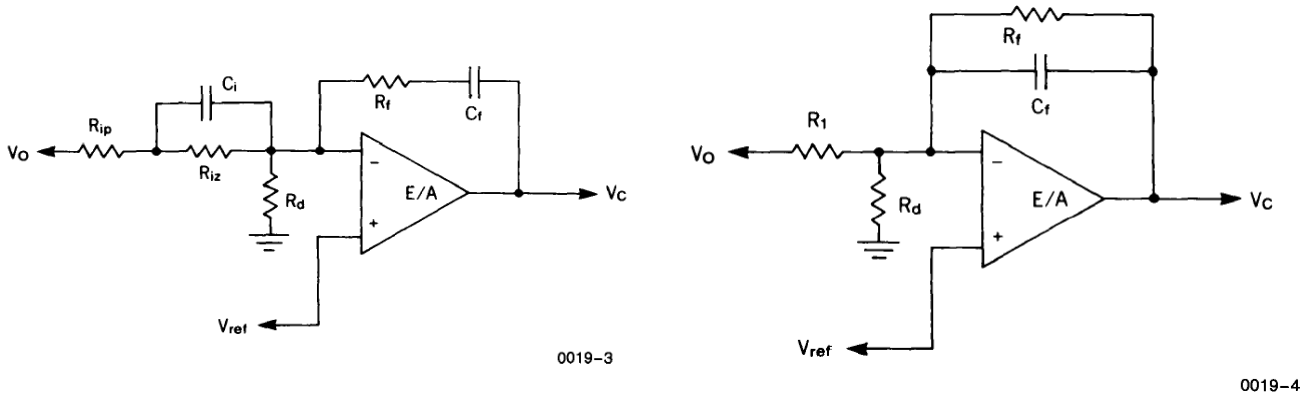


Figure 3. Inductor Looks Like a Current Source to Small Signals



A. Direct duty cycle control

B. Current mode control

Figure 4. Required Error Amplifier Compensation for Continuous Inductor Current Designs

8.3.1 UVLO

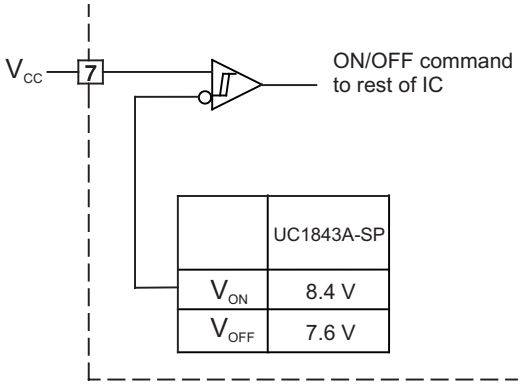
The UVLO circuit ensures that V_{CC} is adequate to make the UC1843A-SP fully operational before enabling the output stage. Figure 5 shows that the UVLO turnon and turnoff thresholds are fixed internally at 16 V and 10 V, respectively. The 6-V hysteresis prevents V_{CC} oscillations during power sequencing.

Figure 6 shows supply current requirements. Start-up current is < 1 mA for efficient bootstrapping from the rectified input of an off-line converter, as shown in Figure 7. During normal circuit operation, V_{CC} is developed from auxiliary winding, WAux, with D_1 and C_{IN}. However, at start-up, C_{IN} must be charged to 16 V through R_{IN}. With a start-up current of 1 mA, R_{IN} can be as large as 100 kΩ and still charge C_{IN} when VAc = 90-V RMS (low line). Power dissipation in R_{IN} would then be less than 350 mW even under high line (VAc = 130-V RMS) conditions.

During UVLO, the output driver is in a low state. While it does not exhibit the same saturation characteristics as normal operation, it can easily sink 1 mA, enough to ensure the MOSFET is held off.

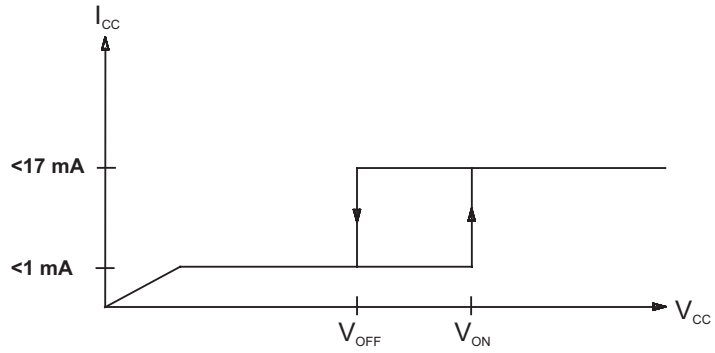
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Feature Description (continued)



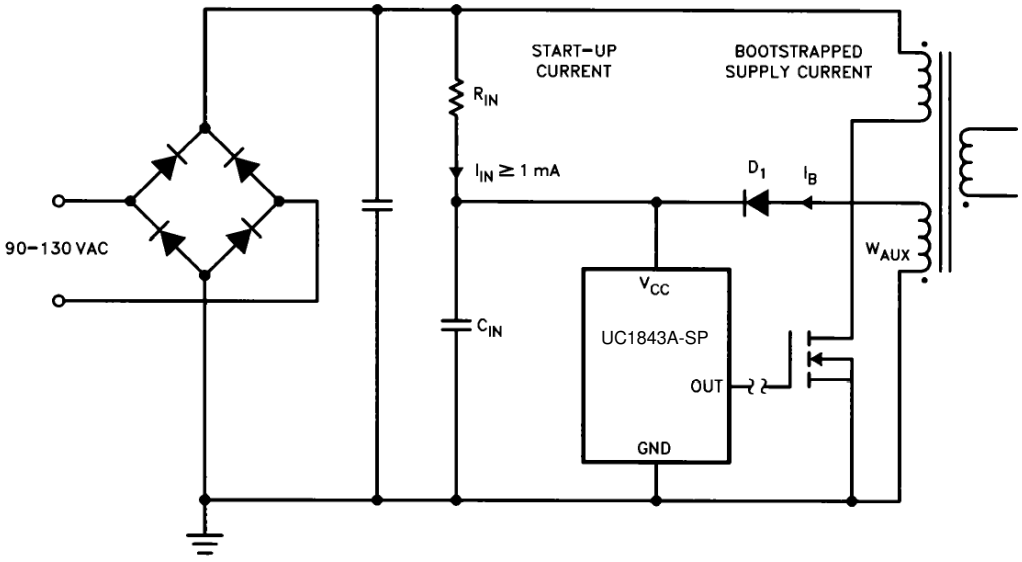
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Figure 5. UVLO Turnon TurnOff Threshold



During UVLO, the output driver is biased to sink minor amounts of current.

Figure 6. Supply Current Requirements



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Figure 7. Providing Power to the UC1843A-SP

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Feature Description (continued)

8.3.2 Reference

As highlighted in the *Functional Block Diagram*, UC1843A-SP incorporates a 5-V internal reference regulator with ±2% set point variation over temperature.

8.3.3 Totem-Pole Output

The UC1843A-SP PWM has a single totem-pole output which can be operated to ±1-A peak for driving MOSFET gates, and a +200 mA average current for bipolar power U-100A transistors. Cross conduction between the output transistors is minimal, the average added power with V_{IN} = 30 V is only 80 mW at 200 kHz.

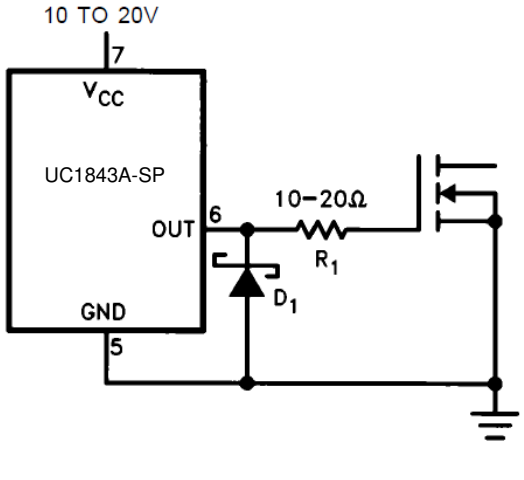
Limiting the peak current through the IC is accomplished by placing a resistor between the totem-pole output and the gate of the MOSFET. The value is determined by dividing the totem-pole collector voltage V_C by the peak current rating of the IC's totem-pole. Without this resistor, the peak current is limited only by the dV/dT rate of the totem-pole switching and the FET gate capacitance.

The use of a Schottky diode from the PWM output to ground prevents the output voltage from going excessively below ground, causing instabilities within the IC. To be effective, the diode selected should have a forward drop of less than 0.3 V at 200 mA. Most 1- to 3-A Schottky diodes exhibit these traits above room temperature. Placing the diode as physically close to the PWM as possible enhances circuit performance. Implementation of the complete drive scheme is shown in Figure 8 through Figure 10. Transformer-driven circuits also require the use of the Schottky diodes to prevent a similar set of circumstances from occurring on the PWM output. The ringing below ground is greatly enhanced by the transformer leakage inductance and parasitic capacitance, in addition to the magnetizing inductance and FET gate capacitance. Circuit implementation is similar to the previous example.

Figure 8 through Figure 10 show suggested circuits for driving MOSFETs and bipolar transistors with the UC1843A-SP output. The simple circuit of Figure 8 can be used when the control IC is not electrically isolated from the MOSFET turnon and turnoff to ±1 A. It also provides damping for a parasitic tank circuit formed by the FET input capacitance and series wiring inductance. Schottky diode, D_1, prevents the output of the IC from going far below ground during turnoff.

Figure 9 shows an isolated MOSFET drive circuit which is appropriate when the drive signal must be level shifted or transmitted across an isolation boundary. Bipolar transistors can be driven efficiently with the circuit of Figure 10. Resistors R_1 and R_2 fix the on-state base current while capacitor C_I provides a negative base current pulse to remove stored charge at turnoff.

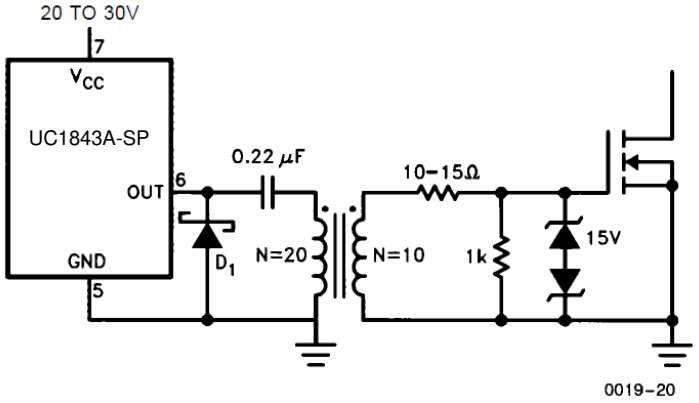
Because the UC1843A-SP series has only a single output, an interface circuit is needed to control push-pull, half-bridge, or full-bridge topologies. The UC1706 dual output driver with internal toggle flip-flop performs this function. *Typical Application* shows a typical application for these two ICs. Increased drive capability for driving numerous FETs in parallel, or other loads can be accomplished using one of the UC1705/6/7 driver ICs.



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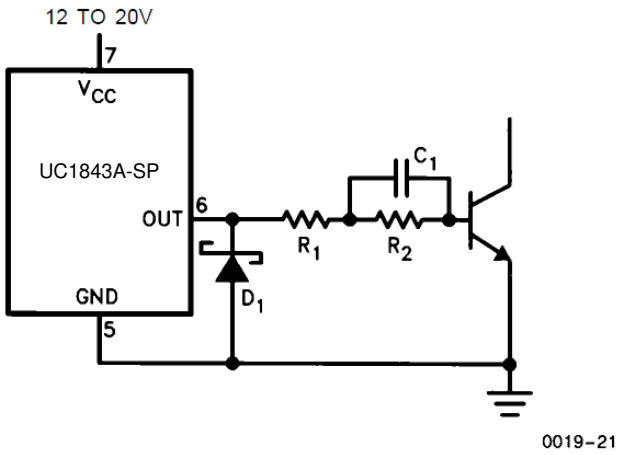
Figure 8. Direct MOSFET Drive

Feature Description (continued)



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Figure 9. Isolated MOSFET Drive



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Figure 10. Bipolar Drive With Negative turnoff Bias

8.4 Device Functional Modes

The UC1843A-SP uses fixed frequency, peak current mode control. An internal oscillator initiates the turn on of the driver to high-side power switch. The external power switch current is sensed through an external resistor and is compared via internal comparator. The voltage generated at the COMP pin is stepped down via internal resistors (as shown in the functional block diagram). When the sensed current reaches the stepped down COMP voltage, the high-side power switch is turned off.

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9 Application and Implementation

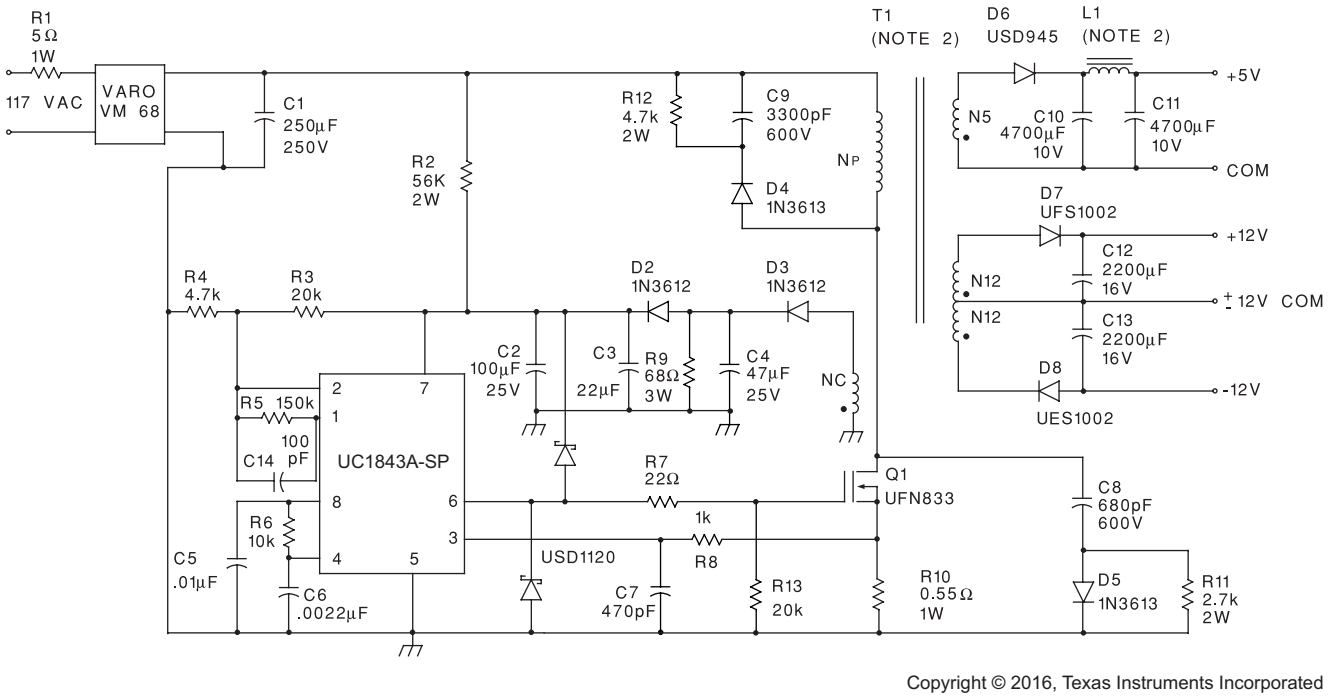
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

UC1843A-SP can be used as a controller to design various topologies such as buck, boost, flyback, and forward. Using an external interphase circuit can also support push-pull, half-bridge and full-bridge topologies.

9.2 Typical Application



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Figure 11. Typical Application Schematic

9.2.1 Design Requirements

See Table 1 for parameter values.

Table 1. Design Parameters(1)

DESIGN PARAMETER	VALUE
Input voltage	95 VAC to 130 VAC
Line isolation	3750 V
Switching frequency	40 kHz
Efficiency (full load)	70%
Output voltage (A)	+5 V, ±5%; 1-A to 4-A load; Ripple voltage: 50-mV P-P max
Output voltage (B)	+12 V, ±3%; 0.1-A to 0.3-A load; Ripple voltage: 100-mV P-P max
Output voltage (C)	–12 V, ±3%; 0.1-A to 0.3-A load; Ripple voltage: 100-mV P-P max

(1) See Figure 11 for reference.

9.2.2 Detailed Design Procedure

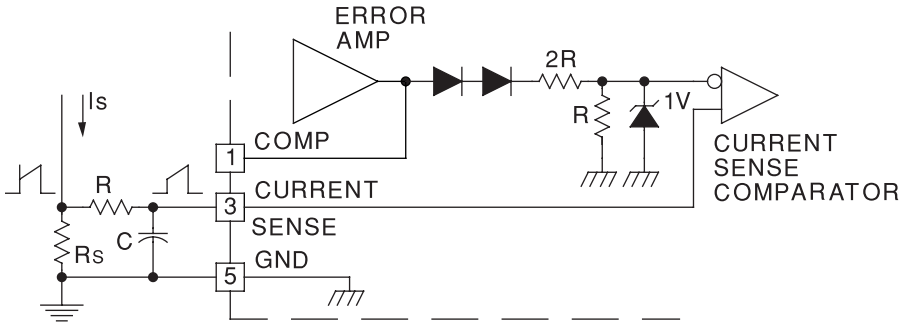
See Table 2 for component values.

Table 2. Components(1)

COMPONENT	VALUE
R1	5 Ω, 1 W
R2	56 kΩ, 2 W
R3	20 kΩ
R4	4.7 kΩ
R5	150 kΩ
R6	10 kΩ
R7	22 Ω
R8	1 kΩ
R9	68 Ω
R10	0.55 Ω, 1 W
R11	2.7 kΩ, 2 W
R12	4.7 kΩ, 2 W
R13	20 kΩ
C1	250 µF, 250 V
C2	100 µF, 25 V
C3	22 µF
C4	47 µF, 25 V
C5	0.1 µF
C6	0.0022 µF
C7	470 pF
C8	680 pF, 600 V
C9	3300 pF, 600 V
C10	4700 µF, 10 V
C11	4700 µF, 10 V
C12	2200 µF, 10 V
C13	2200 µF, 10 V
C14	100 pF
D2	1N3612
D3	1N3612
D4	1N3613
D5	1N3613
D6	USD945
D7	UFS1002
D8	UES1002
Q1	UFN833

(1) See Figure 11 for reference.

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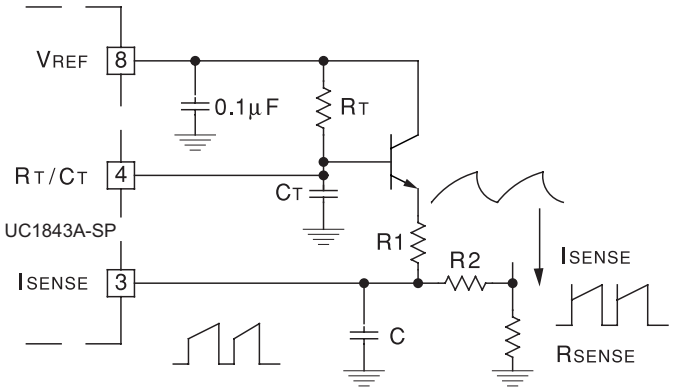


Peak Current (Is) is determined by the formula:

$$I_{SMAX} = \frac{1.0\ V}{R_S}$$

A small RC filter may be required to suppress switch transients.

Figure 12. Current-Sense Circuit



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NOTE: A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converters requiring duty cycles over 50%.

Capacitor, C, forms a filter with R2 to suppress the leading edge switch spikes.

Figure 13. Slope Compensation

9.2.2.1 Oscillator

The UC1843A-SP oscillator is programmed as shown in Figure 15. Timing capacitor C_T is charged from VREF (5 V) through the timing resistor R_T, and discharged by an internal current source. The first step in selecting the oscillator components is to determine the required circuit dead time. Once obtained, Figure 16 is used to pinpoint the nearest standard value of C_T for a given dead time. Next, the appropriate R_T value is interpolated using the parameters for C_T and oscillator frequency. Figure 17 shows the R_T/C_T combinations versus oscillator frequency. The timing resistor can be calculated from the following formula.

$$f_{osc}\ (kHz) = \frac{1.72}{RT\ (k\Omega) \times CT\ (\mu F)} \quad (1)$$

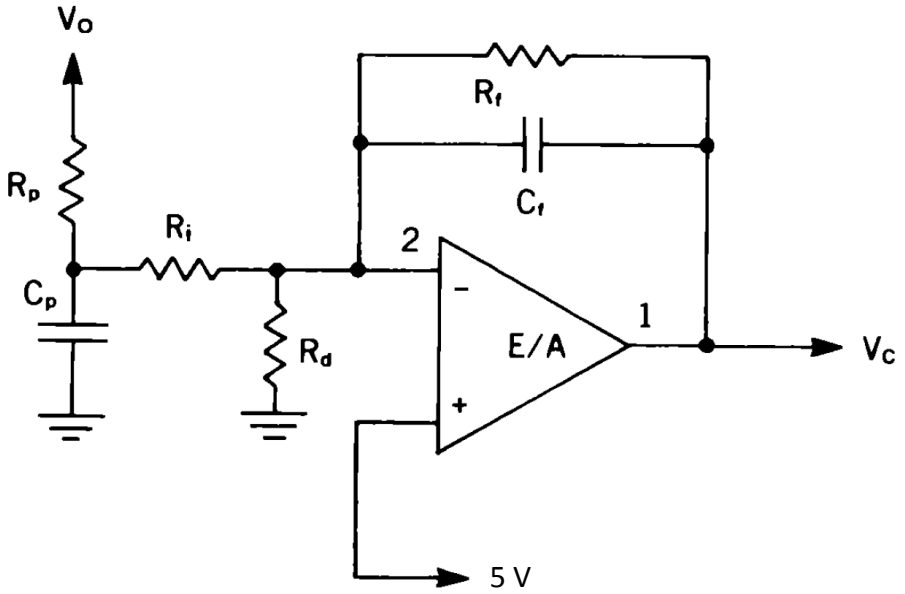


Figure 14. E/A Compensation Circuit for Continuous Boost and Flyback Topologies

The UC1843A-SP has an internal divide-by-two flip-flop driven by the oscillator for a 50% maximum duty cycle. Therefore, their oscillators must be set to run at twice the desired power supply switching frequency.

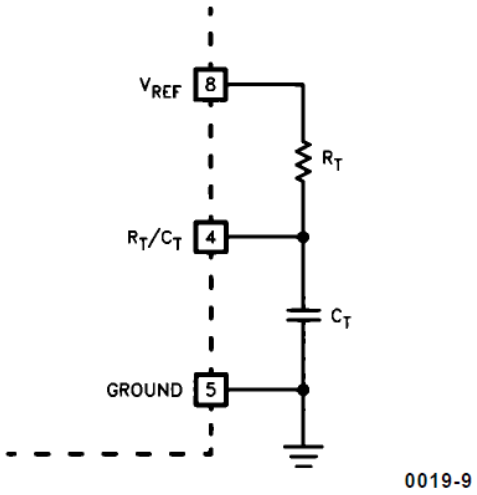


Figure 15. Oscillator Programming

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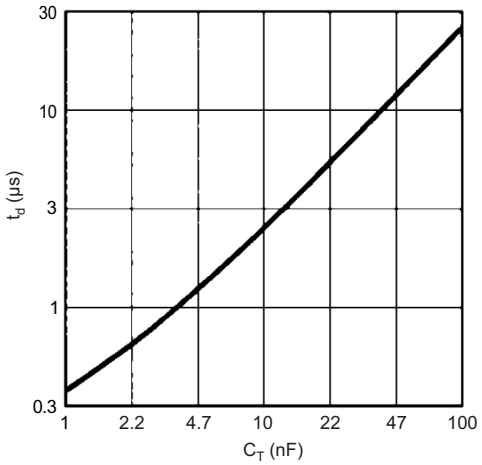


Figure 16. Dead Time vs C_T (R_T > 5 kΩ)

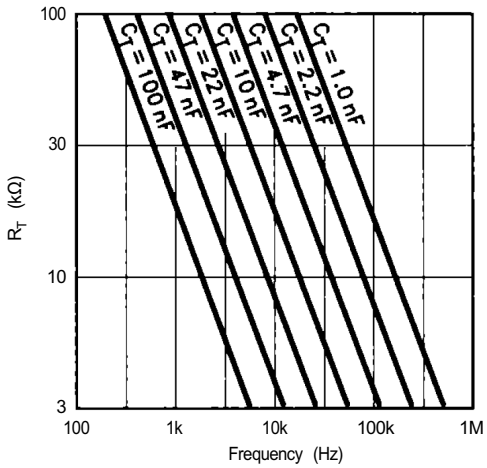


Figure 17. Timing Resistance vs Frequency

9.2.2.2 Current Sensing and Limiting

The UC1843A-SP current sense input is configured as shown in Figure 18. Current-to-voltage conversion is done externally with ground-referenced resistor R_S. Under normal operation, the peak voltage across R_S is controlled by the E/A according to the following relation:

$$I_P = \frac{V_C - 1.4\ V}{3\ R_S}$$

where

- V_C = Control voltage = E/A output voltage (2)

R_S can be connected to the power circuit directly or through a current transformer, as Figure 18 shows. While a direct connection is simpler, a transformer can reduce power dissipation in R_S, reduce errors caused by the base current, and provide level shifting to eliminate the restraint of ground-referenced sensing. The relation between V_C and peak current in the power stage is given by:

$$i_{(pk)} = N\left(\frac{V_{R_S(pk)}}{R_S}\right) = \frac{N}{3\ R_S}(V_C - 1.4\ V)$$

where

- N = Current sense transformer turns ratio = 1 when transformer not used. (3)

For purposes of small-signal analysis, the control-to-sensed-current gain is:

$$\frac{i_{(pk)}}{V_C} = \frac{N}{3\ R_S} \quad (4)$$

When sensing current in series with the power transistor, as shown in Figure 18, the current waveform often has a large spike at its leading edge. This spike is due to rectifier recovery and/or inter-winding capacitance in the power transformer. If unattenuated, this transient can prematurely terminate the output pulse. As shown, a simple RC filter is usually adequate to suppress this spike. The RC time constant should be approximately equal to the current spike duration (usually a few hundred nanoseconds).

The inverting input to the UC1843A-SP current-sense comparator is internally clamped to 1 V (Figure 18). Current limiting occurs if the voltage at pin 3 reaches this threshold value, that is, the current limit is defined by:

$$i_{max} = \frac{N \times 1\ V}{R_S} \quad (5)$$

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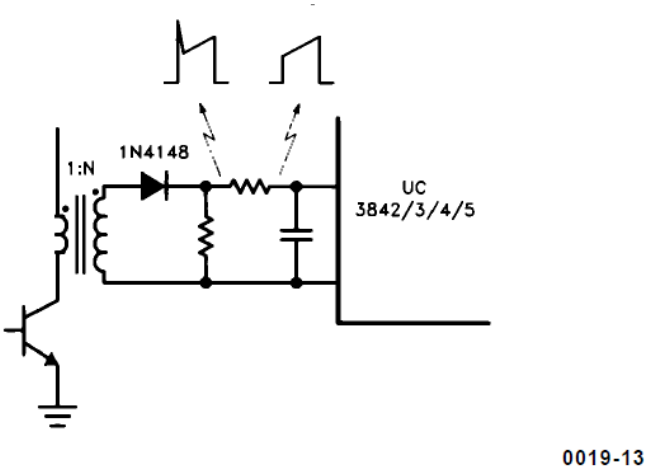


Figure 18. Transformer-Coupled Current Sensing

9.2.2.3 Error Amplifier

The error amplifier (E/A) configuration is shown in Figure 19. The non-inverting input is not brought out to a pin, but is internally biased to 5 V ±2%. The E/A output is available at pin 1 for external compensation, allowing the user to control the converter's closed-loop frequency response.

Figure 20 shows an E/A compensation circuit suitable for stabilizing any current-mode controlled topology except for flyback and boost converters operating with inductor current. The feedback components add a pole to the loop transfer function at $f_p = ½ \pi R_F$. R_F and C_F are chosen so that this pole cancels the zero of the output filter capacitor ESR in the power circuit. R_I and R_F fix the low-frequency gain. They are chosen to provide as much gain as possible while still allowing the pole formed by the output filter capacitor and load to roll off the loop gain to unity (0 dB) at $f \approx f_{SWITCHING} / 4$. This technique ensures converter stability while providing good dynamic response.

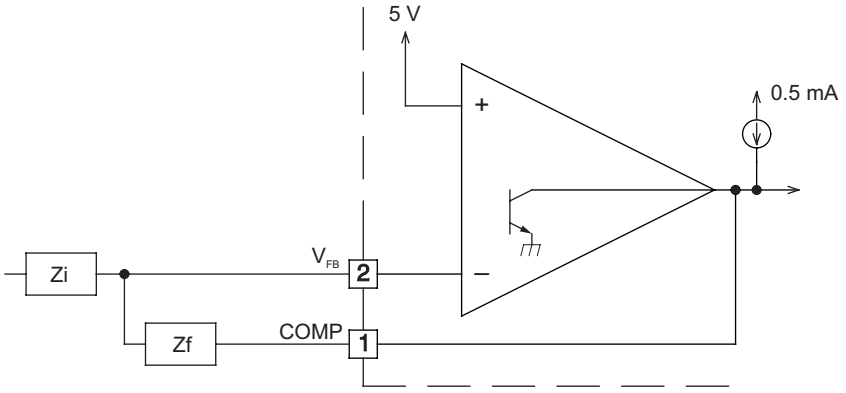


Figure 19. E/A Configuration

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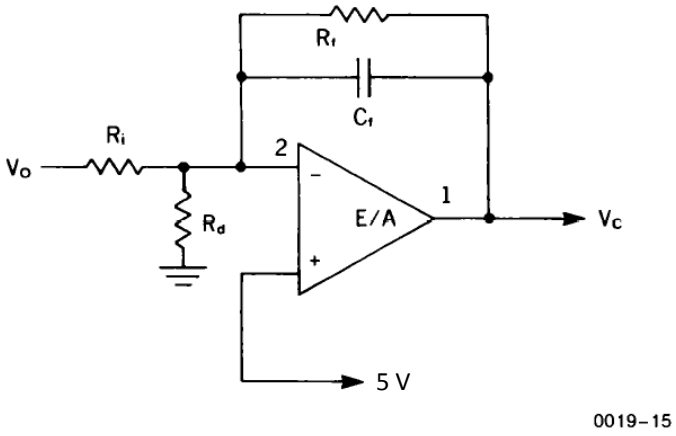


Figure 20. Compensation

The E/A output sources 0.5 mA and sinks 2 mA. A lower limit for RF is given by:

$$R_{F(MIN)} \approx \frac{V_{EA\,OUT\,(MAX)} - 2.5\ V}{0.5\ mA} = \frac{6\ V - 2.5\ V}{0.5\ mA} = 7\ k\Omega \quad (6)$$

E/A input bias current (2-µA max) flows through R_I, resulting in a DC error in output voltage (VO) given by:

$$\Delta V_{O(MAX)} = (2\ \mu A)\ R_I \quad (7)$$

Therefore, the designer should keep the value of R_I, as low as possible.

Figure 21 shows the open-loop frequency response of the UC1843A-SP E/A. The gain represents an upper limit on the gain of the compensated E/A. Phase lag increases rapidly as frequency exceeds 1 MHz due to second-order poles at about 10 MHz and above.

Continuous-inductor-current boost and flyback converters each have a right-half-plane zero in their transfer function. An additional compensation pole is needed to roll off loop gain at a frequency less than that of the RHP zero. R_P and C_P in the circuit of Figure 14 provide this pole.

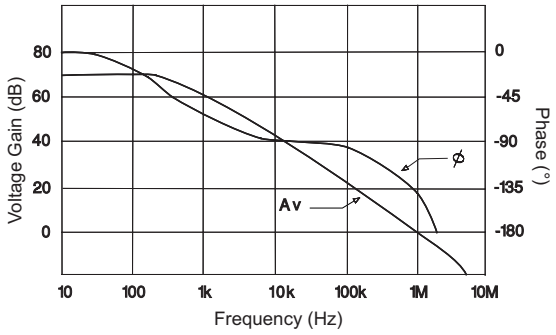


Figure 21. Error Amplifier Open-Loop Frequency Response

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9.2.3 Application Curves

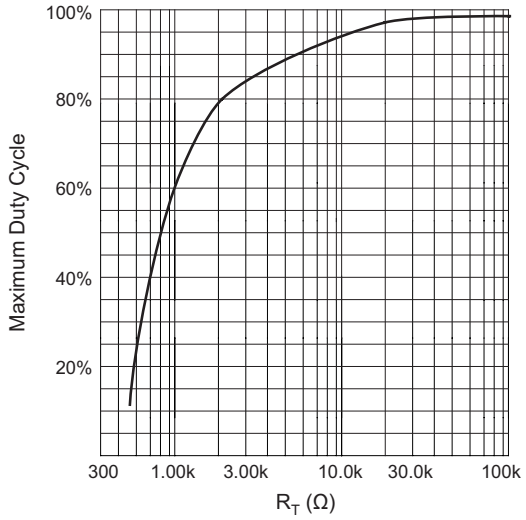


Figure 22. Oscillator Frequency vs Timing Resistance

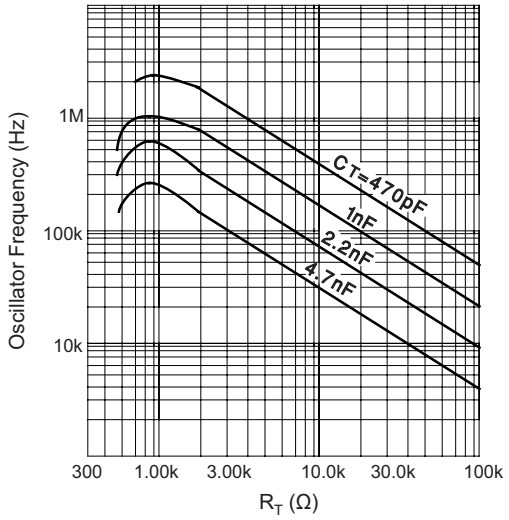
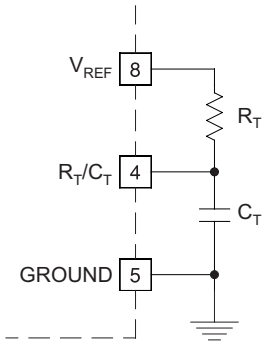


Figure 23. Maximum Duty Cycle vs Timing Resistor



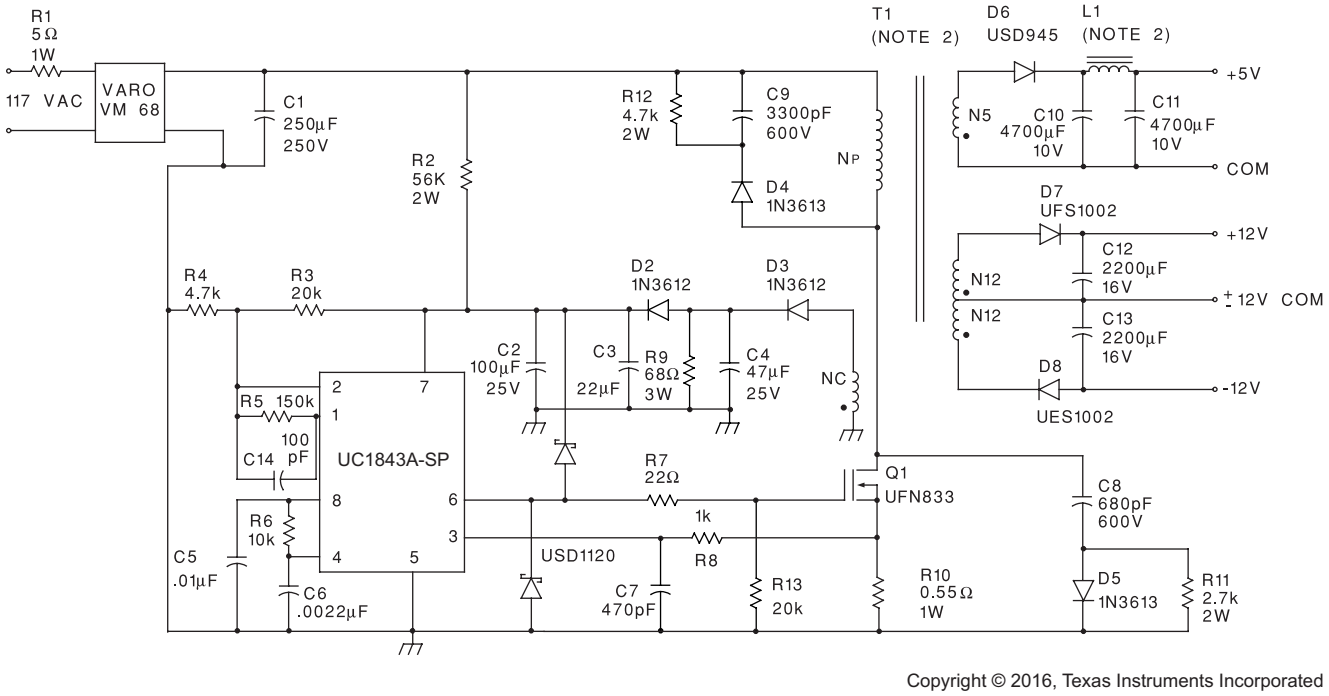
For $R_T > 5k$ $f \approx 1.72 / (R_T C_T)$

Figure 24. Oscillation Schematic

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10 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 8 V and 40 V. This input supply should be well regulated. If the input supply is located more than a few inches from the UC1843A-SP converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. A tantalum capacitor with a value of 47 µF is a typical choice; however, this may vary depending upon the output power being delivered.



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Power supply specifications:

1. Input voltage: 95 VAC to 130 VAC (50 Hz/60 Hz)
2. Line isolation: 3750 V
3. Switching frequency: 40 kHz
4. Efficiency full load: 70%
5. Output voltage:
   a. +5 V, ±5%; 1- to 4-A load, ripple voltage: 50 mVP-P max
   b. +12 V, ±3%; 0.1- to 0.3-A load, ripple voltage: 100 mVP-P max
   c. –12 V, ±3%; 0.1- to 0.3-A load, ripple voltage: 100 mVP-P max

Figure 25. Offline Flyback Regulator

11 Layout

11.1 Layout Guidelines

Always try to use a low-EMI inductor with a ferrite-type closed core. Some examples would be toroid and encased E core inductors. Open core can be used if they have low-EMI characteristics and are located a farther away from the low-power traces and components. Make the poles perpendicular to the PCB as well if using an open core. Stick cores usually emit the most unwanted noise.

Layout Guidelines (continued)

11.1.1 Feedback Traces

Try to run the feedback trace as far as possible from the inductor and noisy power traces. The designer should also make the feedback trace as direct as possible and somewhat thick. These two guidelines sometimes involve a trade-off, but keeping the trace away from inductor EMI and other noise sources is the more critical guideline. Run the feedback trace on the side of the PCB opposite of the inductor with a ground plane separating the two.

11.1.2 Input/Output Capacitors

When using a low-value ceramic input filter capacitor, locate it as close as possible to the VIN pin of the IC. This eliminates as much trace inductance effects as possible and gives the internal IC rail a cleaner voltage supply. Some designs require the use of a feed-forward capacitor connected from the output to the feedback pin as well, usually for stability reasons. In this case, it should also be positioned as close as possible to the IC. Using surface mount capacitors also reduces lead length and lessens the chance of noise coupling into the effective antenna created by through-hole components.

11.1.3 Compensation Components

External compensation components for stability should also be placed close to the IC. TI recommends to also use surface mount components for the same reasons discussed for the filter capacitors. These should not be located very close to the inductor either.

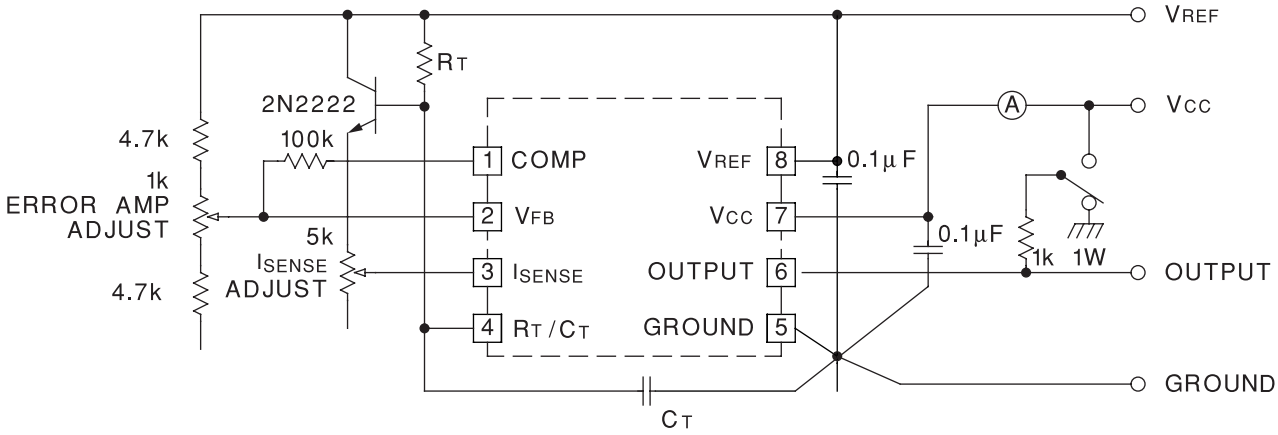
11.1.4 Traces and Ground Planes

Make all of the power (high-current) traces as short, direct, and thick as possible. It is good practice on a standard PCB to make the traces an absolute minimum of 15 mils (0.381 mm) per ampere. The inductor, output capacitors, and output diode should be as close as possible to each other. This helps reduce the EMI radiated by the power traces due to the high-switching currents through them. This also reduces lead inductance and resistance, which in turn reduces noise spikes, ringing, and resistive losses that produce voltage errors. The grounds of the IC, input capacitors, output capacitors, and output diode (if applicable) should be connected close together directly to a ground plane. It would also be a good idea to have a ground plane on both sides of the PCB. This reduces noise by reducing ground loop errors and absorbing more of the EMI radiated by the inductor.

For multi-layer boards with more than two layers, a ground plane can be used to separate the power plane (where the power traces and components are) and the signal plane (where the feedback and compensation and components are) for improved performance. On multi-layer boards, vias are required to connect traces and different planes. It is a good practice to use one standard via per 200 mA of current if the trace needs to conduct a significant amount of current from one plane to the other. Arrange the components so that the switching current loops curl in the same direction. Due to the way switching regulators operate, there are two power states: one state when the switch is on and one when the switch is off. During each state there is a current loop made by the power components that are currently conducting. Place the power components so that during each of the two states the current loop is conducting in the same direction. This prevents magnetic field reversal caused by the traces between the two half-cycles and reduces radiated EMI.

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11.2 Layout Example



High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in a single point ground. The transistor and 5k potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

Figure 26. Open-Loop Laboratory Test Fixture

12 デバイスおよびドキュメントのサポート

12.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.2 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-8670406VPA	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8670406VPA UC1843A
5962-8670406VPA.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8670406VPA UC1843A
5962-8670406VXA	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8670406VXA UC1843AL QMLV
5962-8670406VXA.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8670406VXA UC1843AL QMLV
5962-8670409VPA	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8670409VPA UC1843A-SP
5962-8670409VPA.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8670409VPA UC1843A-SP
5962P8670409VPA	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	P8670409VPA UC1843A-SP
5962P8670409VPA.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	P8670409VPA UC1843A-SP
5962P8670409VYC	Active	Production	CFP (HKU) | 10	25 | TUBE	ROHS Exempt	NIAU	N/A for Pkg Type	-55 to 125	P8670409VYC UC1843A-SP
5962P8670409VYC.A	Active	Production	CFP (HKU) | 10	25 | TUBE	ROHS Exempt	NIAU	N/A for Pkg Type	-55 to 125	P8670409VYC UC1843A-SP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF UC1843A-SP :

- Catalog : UC1843A
- Enhanced Product : UC1843A-EP

NOTE: Qualified Version Definitions:

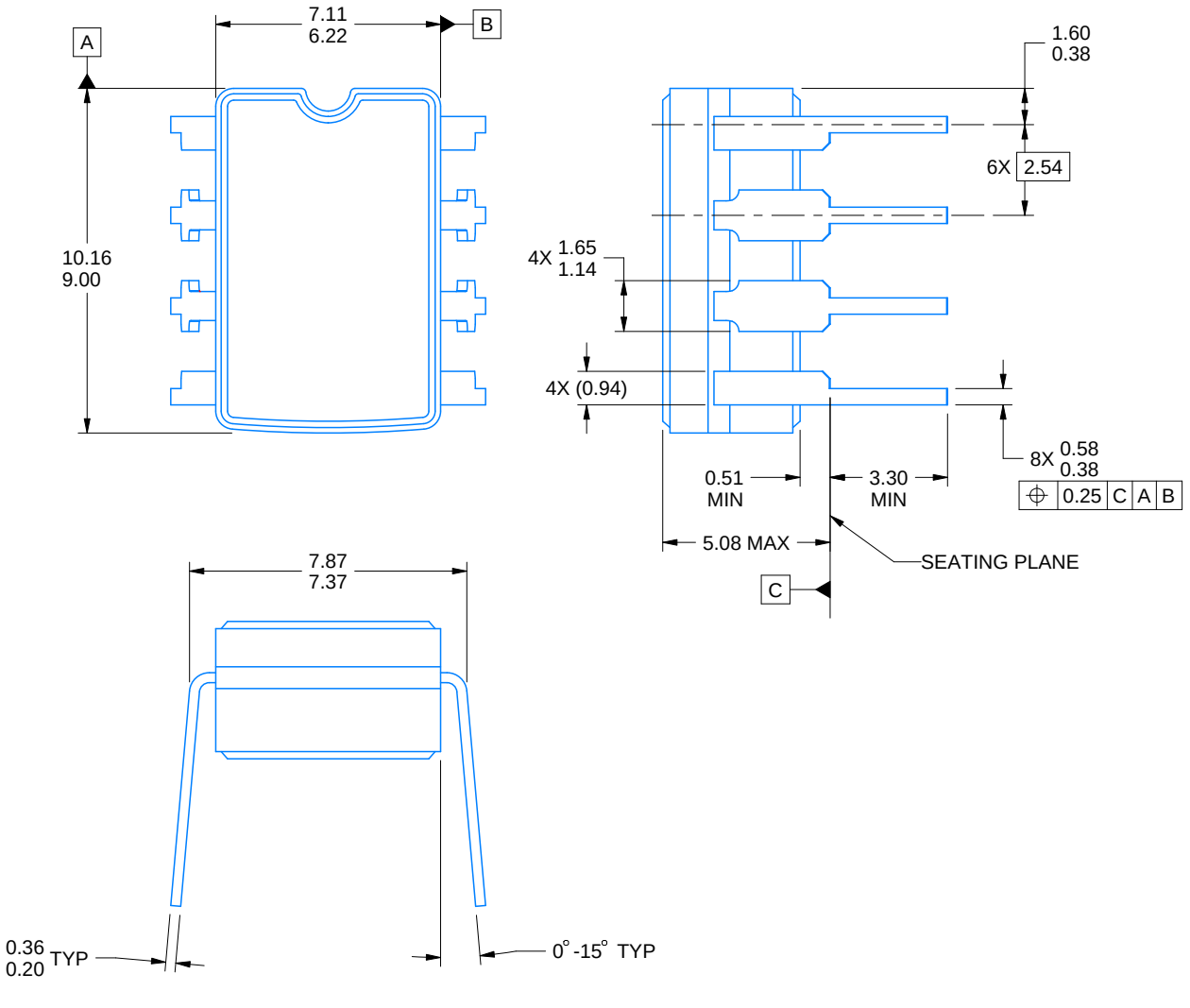
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

PACKAGE OUTLINE

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



4230036/A 09/2023

NOTES:

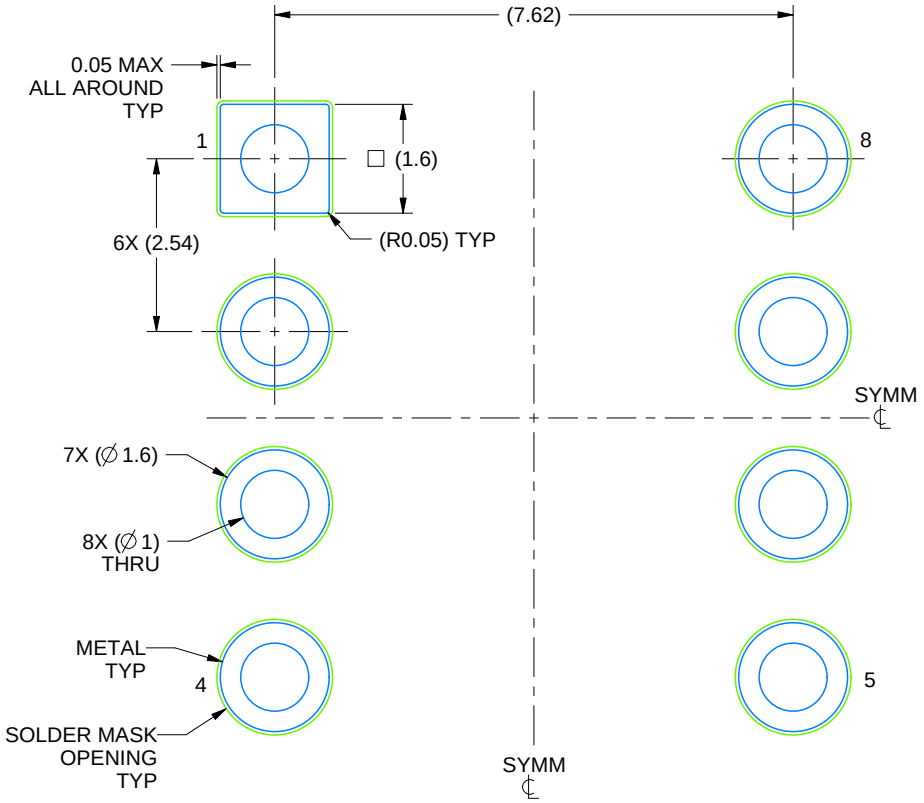
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package can be hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification.
5. Falls within MIL STD 1835 GDIP1-T8

EXAMPLE BOARD LAYOUT

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



LAND PATTERN EXAMPLE
NON SOLDER MASK DEFINED
SCALE: 9X

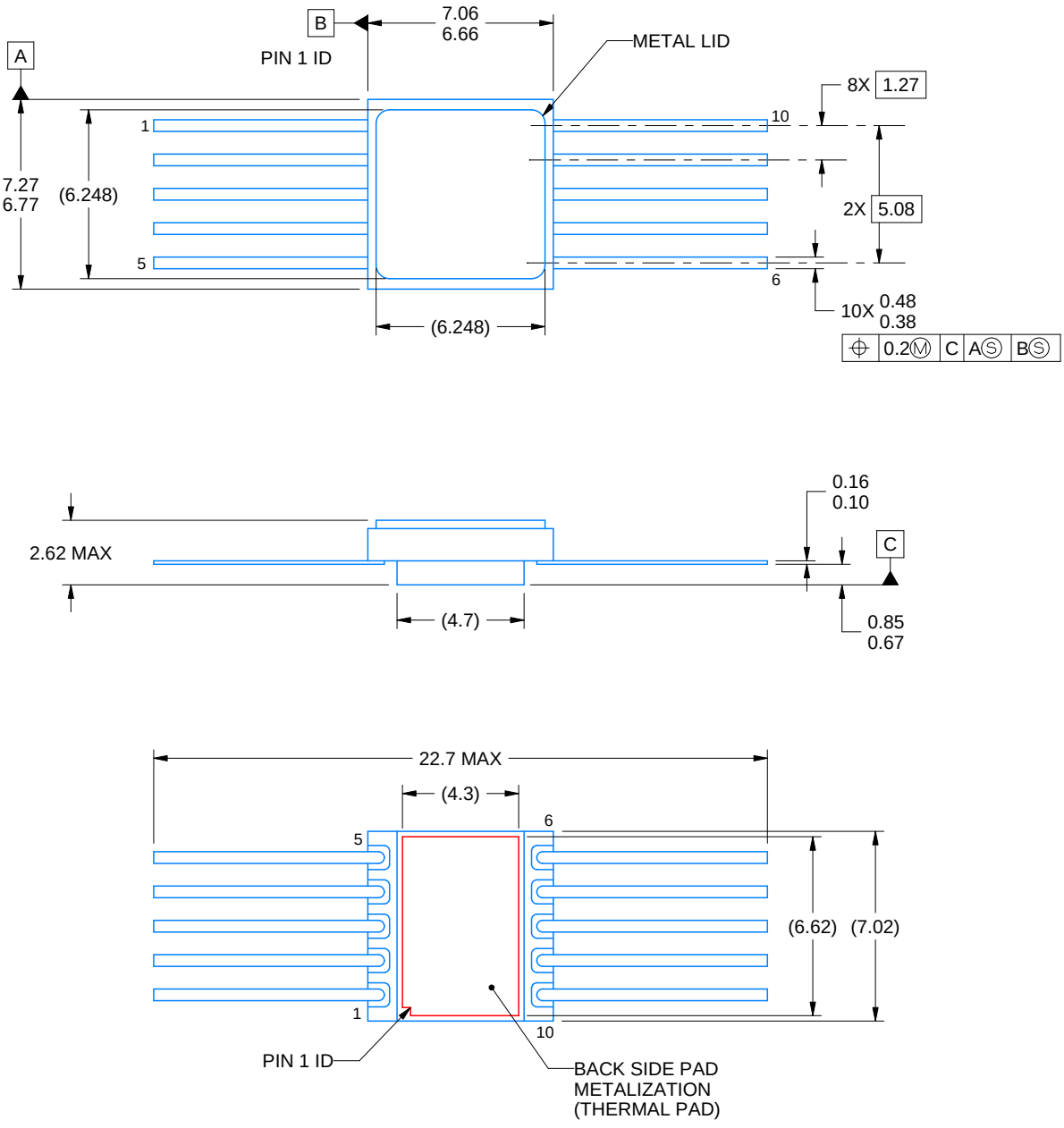
4230036/A 09/2023

PACKAGE OUTLINE

HKU0010A

CFP - 2.63mm max height

CERAMIC DUAL FLATPACK



4226200/A 09/2020

NOTES:

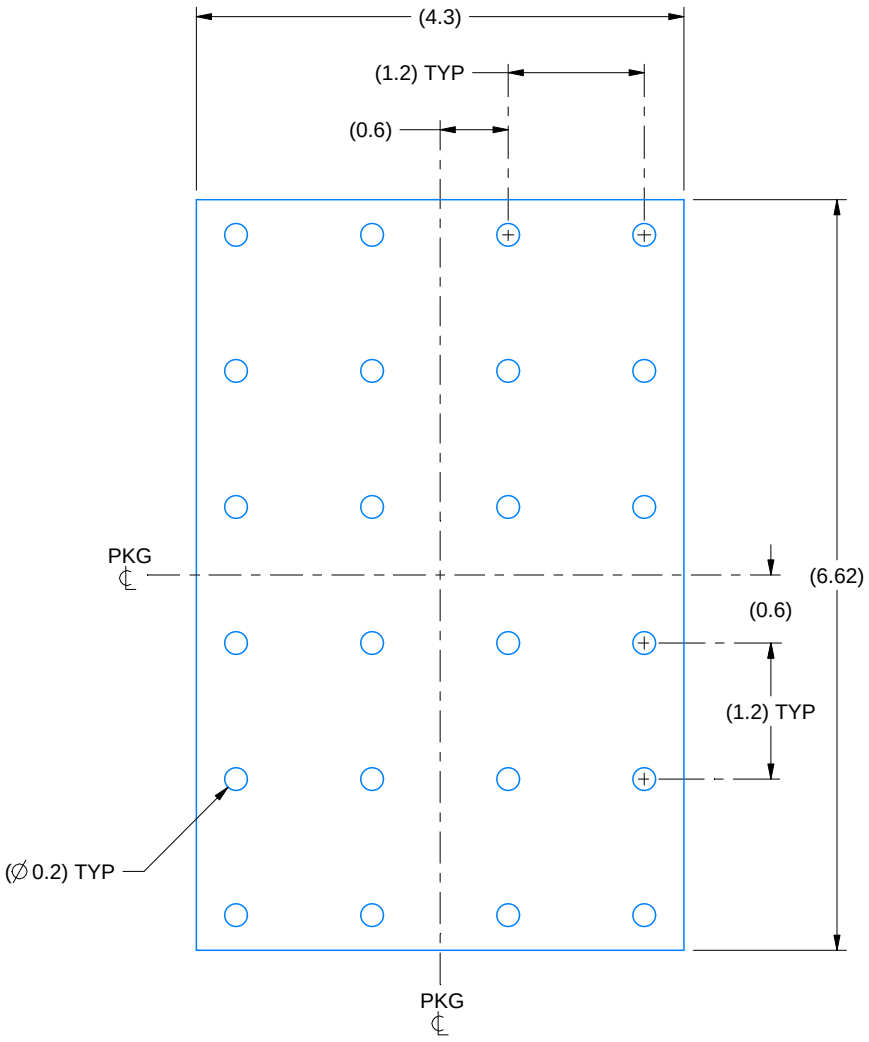
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid.
4. The terminals are gold plated.
5. This drawing does not comply with MIL STD 1835. Do not use this package for compliant product.
6. Metal lid is connected to back side pad metalization.

EXAMPLE BOARD LAYOUT

HKU0010A

CFP - 2.63mm max height

CERAMIC DUAL FLATPACK



HEATSINK LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

GENERIC PACKAGE VIEW

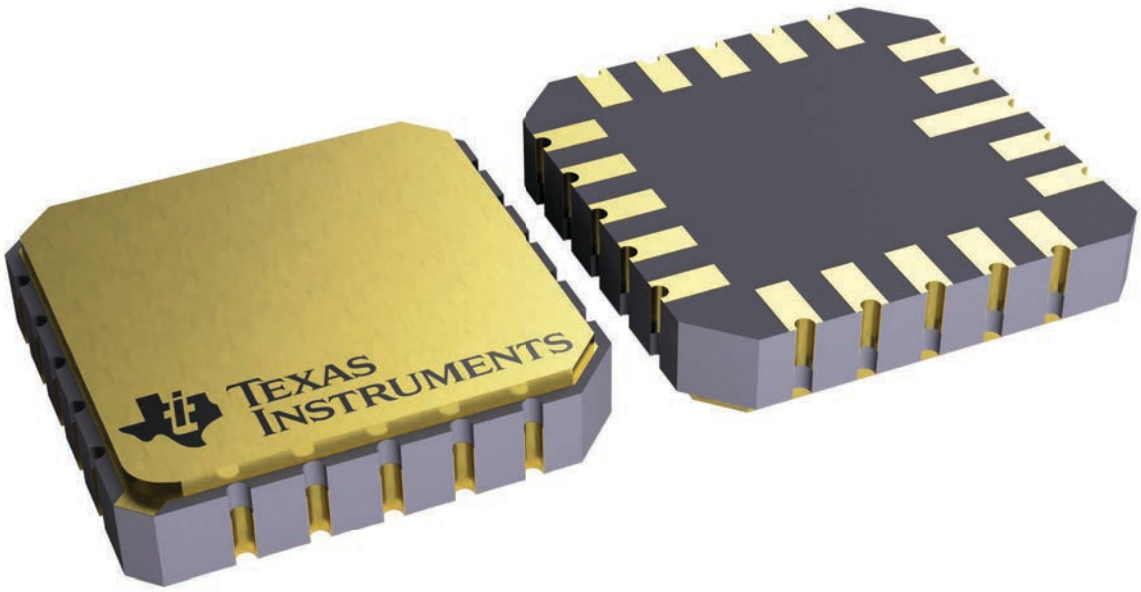
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

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