UCC21220、UCC21220A ノイズ耐性の高い 4A、6A、2 チャネルの基本および機能絶縁型ゲート ドライバ

1 特長

- 汎用:デュアル ローサイド、デュアル ハイサイド、またはハーフ ブリッジ ドライバ
- 基本および機能絶縁をサポート
- 125V/ns を超える CMTI
- 最大 4A のピーク ソース、6A のピーク シンク出力
- スイッチング パラメータ:
  - 33ns (標準値) の伝搬遅延
  - 最大パルス幅歪み:5ns
  - 最大 VDD 電源オン遅延:10µs
- 最大 25V の VDD 出力駆動電源
  - 5V および 8V VDD UVLO オプション
- 接合部温度範囲 (T_j) -40℃～150℃
- ナロー ボディ SOIC-16 (D) パッケージ
- TTL および CMOS 互換の入力
- 安全関連認証:
  - DIN EN IEC 60747-17 (VDE 0884-17) に準拠した絶縁耐圧:4242V_{PK} (予定)
  - UL 1577 に準拠した絶縁耐性:3000V_{RMS} (1 分間) (予定)
  - GB4943.1-2022 準拠の CQC 認定 (予定)

2 アプリケーション

- サーバー電源
- ソーラー インバータ、ソーラー パワー オプティマイザ
- テレコム用ブリック コンバータ
- ワイヤレス インフラ
- 産業用オートメーションおよびロボティクス

3 概要

UCC21220 および UCC21220A デバイスは、ピーク ソース電流が 4A 、ピーク シンク電流が 6A の基本および機能絶縁型デュアル チャネル ゲート ドライバです。これらのデバイスは、PFC、絶縁型 DC/DC、同期整流アプリケーションのパワー MOSFET および GaNFET を駆動するよう設計されており、高速なスイッチング性能と、125V/ns を超える同相過渡耐性 (CMTI) による堅牢なグランド バウンス保護機能を備えています。

これらのデバイスは、2 つのローサイド ドライバ、2 つのハイサイド ドライバ、ハーフブリッジ ドライバのいずれかとして構成できます。出力の遅延ばらつきが非常に小さいため、2 つの出力を並列接続することで、重負荷条件用に駆動能力を 2 倍にした 1 つのドライバを構成できます。

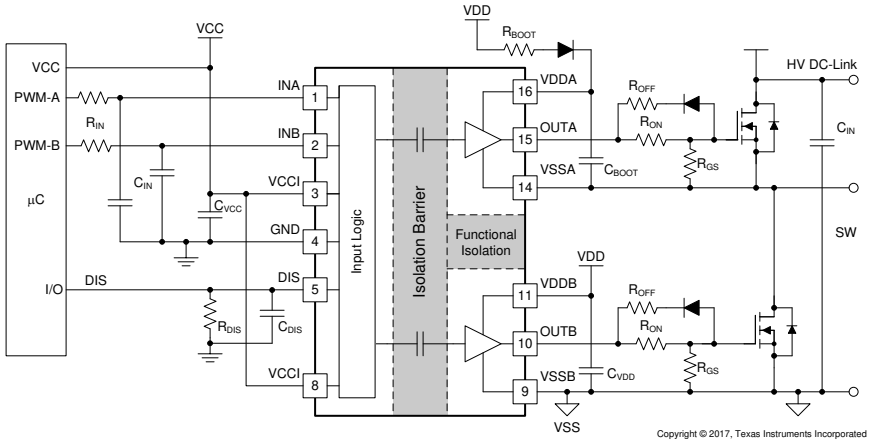
保護機能には、以下のものがあります。DIS ピンを High に設定すると、両方の出力が同時にシャットダウンされます。すべての電源には低電圧誤動作防止 (UVLO) 機能があり、またアクティブ プルダウン保護機能により、電源オフまたはフローティング時に出力が 2V 未満にクランプされます。

これらの機能により、広範な電力アプリケーションにおいて高効率、高電力密度、高い堅牢性を実現します。

製品情報

部品番号 (2)	パッケージ (1)	UVLO
UCC21220	D (SOIC 16)	8 V
UCC21220A	D (SOIC 16)	5 V

(1) 供給されているすべてのパッケージについては、セクション 14 を参照してください。
(2) デバイスの詳細な比較については、セクション 4 を参照してください。



代表的なアプリケーション

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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4 Device Comparison Table

DEVICE OPTIONS	UVLO	RECOMMENDED VDD SUPPLY MINIMUM	PACKAGE
UCC21220D	8-V	9.2-V	Narrow Body SOIC-16
UCC21220AD	5-V	6.5-V	Narrow Body SOIC-16

5 Pin Configuration and Functions

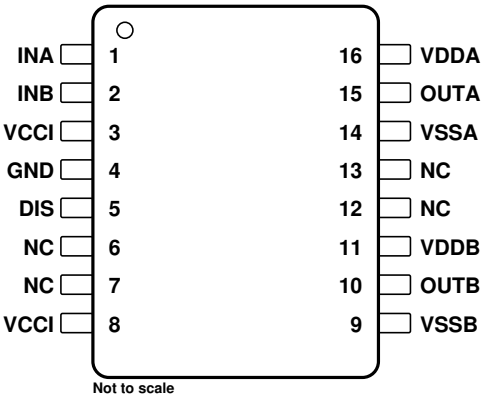

図 5-1. D Package 16-Pin SOIC Top View

表 5-1. Pin Functions

PIN	NO.	TYPE(1)	DESCRIPTION
DIS	5	I	Disables both driver outputs if asserted high or left open, enables if set low. This pin is pulled high internally if left open. It is recommended to tie this pin to ground if not used to achieve better noise immunity. Bypass using a ≈ 1-nF low ESR/ESL capacitor close to DIS pin when connecting to a µC with distance.
GND	4	P	Primary-side ground reference. All signals in the primary side are referenced to this ground.
INA	1	I	Input signal for A channel. INA input has a TTL/CMOS compatible input threshold. This pin is pulled low internally if left open. It is recommended to tie this pin to ground if not used to achieve better noise immunity.
INB	2	I	Input signal for B channel. INB input has a TTL/CMOS compatible input threshold. This pin is pulled low internally if left open. It is recommended to tie this pin to ground if not used to achieve better noise immunity.
NC	6		No internal connection
	7		
	12		
	13		
OUTA	15	O	Output of driver A. Connect to the gate of the A channel FET or IGBT.
OUTB	10	O	Output of driver B. Connect to the gate of the B channel FET or IGBT.
VCCI	3	P	Primary-side supply voltage. Locally decoupled to GND using a low ESR/ESL capacitor located as close to the device as possible.
VCCI	8	P	This pin is internally shorted to pin 3.
VDDA	16	P	Secondary-side power for driver A. Locally decoupled to VSSA using a low ESR/ESL capacitor located as close to the device as possible.
VDDB	11	P	Secondary-side power for driver B. Locally decoupled to VSSB using a low ESR/ESL capacitor located as close to the device as possible.
VSSA	14	P	Ground for secondary-side driver A. Ground reference for secondary side A channel.
VSSB	9	P	Ground for secondary-side driver B. Ground reference for secondary side B channel.

(1) P = power, G = ground, I = input, O = output

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input bias pin supply voltage	VCCI to GND	–0.3	6	V
Driver bias supply	VDDA-VSSA, VDDB-VSSB	–0.3	30	V
Output signal voltage	OUTA to VSSA, OUTB to VSSB	–0.3	V_{VDDA}+0.3, V_{VDDB}+0.3	V
	OUTA to VSSA, OUTB to VSSB, Transient for 200 ns(3)	–2	V_{VDDA}+0.3, V_{VDDB}+0.3	V
Input signal voltage	INA, INB, DIS to GND	–0.3	V_{VCCI}+0.3	V
Junction temperature, T_J (2)		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) To help maintain the recommended operating conditions for T_J, see the セクション 6.4.
(3) Values are verified by characterization and are not production tested.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
VCCI	VCCI Input supply voltage		3	5.5	V
VDDA, VDDB	Driver output bias supply	UCC21220 – 8V UVLO Version	9.2	25	V
		UCC21220A – 5V UVLO Version	6.5	25	V
T_J	Junction Temperature		–40	150	°C

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6.4 Thermal Information

THERMAL METRIC[1]		UCC21220, UCC21220A	UNIT
		D (SOIC)	
		16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	80.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	36.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	45	°C/W
ψ_{JT}	Junction-to-top characterization parameter	28	°C/W
ψ_{JB}	Junction-to-board characterization parameter	44.3	°C/W

(1) For more information about traditional and new thermal metrics, see the application report, *Semiconductor and IC Package Thermal Metrics* (SPRA953).

6.5 Power Ratings

			VALUE	UNIT
P_D	Power dissipation	VCCI = 5 V, VDDA/B = 20 V, INA/B = 3.3 V, 460kHz 50% duty cycle square wave 2.2-nF load, T_J=150°C, T_A=25°C	950	mW
P_{DI}	Power dissipation by transmitter side		50	mW
P_{DA}, P_{DB}	Power dissipation by each driver side		450	mW

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6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
CLR	External clearance(1)	Shortest pin-to-pin distance through air	> 4	mm
CPG	External creepage(1)	Shortest pin-to-pin distance across the package surface	> 4	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>17	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 400	V
	Material group		II	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 150 V_{RMS}	I-IV	
		Rated mains voltage ≤ 300 V_{RMS}	I-III	
		Rated mains voltage ≤ 600 V_{RMS}	I-II	
DIN EN IEC 60747-17 (VDE 0884-17)(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1200(6)	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage (sine wave); time dependent dielectric breakdown (TDDB) test;	850(6)	V_{RMS}
		DC Voltage	1200(6)	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production)	4242	V_{PK}
V_{IMP}	Maximum inpulse voltage	Tested in air, 1.2/50-µs waveform per IEC 62368-1	5000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(3)	$V_{IOSM} \geq 1.3 \times V_{IMP}$; Tested in oil (qualification test), 1.2/50-µs waveform per IEC 62368-1	6500	V_{PK}
q_{pd}	Apparent charge(4)	Method a, After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	<5	pC
		Method a, After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	<5	
		Method b1; At routine test (100% production) and preconditioning (type test) $V_{ini} = 1.2 \times V_{IOTM}$; t_{ini} = 1 s; $V_{pd(m)} = 1.5 \times V_{IORM}$, t_m = 1 s	<5	
C_{IO}	Barrier capacitance, input to output(5)	V_{IO} = 0.4 sin (2πft), f =1 MHz	~1.2	pF
R_{IO}	Isolation resistance, input to output(5)	V_{IO} = 500 V at T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500 V at 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500 V at T_S =150°C	> 10^9	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$ = 3000 V_{RMS}, t = 60 s. (qualification), $V_{TEST} = 1.2 \times V_{ISO}$ = 3600 V_{RMS}, t = 1 s (100% production)	3000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.
(2) This coupler is suitable for basic electrical insulation only within the maximum operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-pin device.
(6) System isolation working voltages need to be verified according to application parameters.

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6.7 Safety-Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	SIDE	MIN	TYP	MAX	UNIT
I_S	Safety output supply current	$R_{\theta JA}$ = 80.2°C/W, $V_{VDDA/B}$ = 15 V, T_J = 150°C, T_A = 25°C See 図 6-1	DRIVER A, DRIVER B			50	mA
		$R_{\theta JA}$ = 80.2°C/W, $V_{VDDA/B}$ = 25 V, T_J = 150°C, T_A = 25°C See 図 6-1				30	
P_S	Safety supply power	$R_{\theta JA}$ = 80.2°C/W, T_J = 150°C, T_A = 25°C See 図 6-2	INPUT			50	mW
			DRIVER A			750	
			DRIVER B			750	
			TOTAL			1550	
T_S	Safety temperature(1)					150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.

The junction-to-air thermal resistance, $R_{\theta JA}$, in the *セクション 6.4* table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.

$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.

$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

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6.8 Electrical Characteristics

V_{VCCI} = 3.3 V or 5.0 V, 0.1-µF capacitor from VCCI to GND and 1uF capacitor from VDDA/B to VSSA/B, V_{VDDA} = V_{VDDB} = 12 V, 1-µF capacitor from VDDA and VDDB to VSSA and VSSB, T_A = –40°C to +125°C, unless otherwise noted(1) (2).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENTS						
I_{VCCI}	VCCI quiescent current	V_{INA} = 0 V, V_{INB} = 0 V		1.4	2.0	mA
I_{VDDA}, I_{VDDB}	VDDA and VDDB quiescent current	V_{INA} = 0 V, V_{INB} = 0 V		1.2	2.0	mA
I_{VCCI}	VCCI operating current	(f = 500 kHz) current per channel		2.7	3.2	mA
I_{VDDA}, I_{VDDB}	VDDA and VDDB operating current	(f = 500 kHz) current per channel, V_{VDDA}, V_{VDDB} = 12 V		2.7	4.4	mA
VCC SUPPLY VOLTAGE UNDERVOLTAGE THRESHOLDS						
V_{VCCI_ON}	UVLO Rising threshold		2.55	2.7	2.85	V
V_{VCCI_OFF}	UVLO Falling threshold		2.35	2.5	2.65	V
V_{VCCI_HYS}	UVLO Threshold hysteresis			0.2		V
UCC21220A VDD SUPPLY VOLTAGE UNDERVOLTAGE THRESHOLDS (5-V UVLO Version)						
V_{VDDA_ON}, V_{VDDB_ON}	UVLO Rising threshold		5.7	6.0	6.3	V
V_{VDDA_OFF}, V_{VDDB_OFF}	UVLO Falling threshold		5.4	5.7	6.0	V
V_{VDDA_HYS}, V_{VDDB_HYS}	UVLO Threshold hysteresis			0.3		V
UCC21220 VDD SUPPLY VOLTAGE UNDERVOLTAGE THRESHOLDS (8-V UVLO Version)						
V_{VDDA_ON}, V_{VDDB_ON}	UVLO Rising threshold		7.7	8.5	8.9	V
V_{VDDA_OFF}, V_{VDDB_OFF}	UVLO Falling threshold		7.2	7.9	8.4	V
V_{VDDA_HYS}, V_{VDDB_HYS}	UVLO Threshold hysteresis			0.6		V
INA, INB AND DISABLE						
V_{INAH}, V_{INBH}, V_{DISH}	Input high threshold voltage			2	2.3	V
V_{INAL}, V_{INBL}, V_{DISL}	Input low threshold voltage		0.8	1		V
V_{INA_HYS}, V_{INB_HYS}, V_{DIS_HYS}	Input threshold hysteresis			1		V
OUTPUT						
I_{OA+}, I_{OB+}	Peak output source current	C_{VDD} = 10 µF, C_{LOAD} = 0.22 µF, f = 1 kHz, bench measurement		-4		A
I_{OA-}, I_{OB-}	Peak output sink current	C_{VDD} = 10 µF, C_{LOAD} = 0.22 µF, f = 1 kHz, bench measurement		6		A
R_{OHA}, R_{OHB}	Output resistance at high state	I_{OUT} = –5 mA, R_{OHA}, R_{OHB} do not represent drive pull-up performance. See t_{RISE} in セクション 6.9 and セクション 8.3.4 for more details.		5		Ω
R_{OLA}, R_{OLB}	Output resistance at low state	I_{OUT} = 5 mA		0.55		Ω
V_{OAPDA}, V_{OAPDB}	Driver output (V_{OUTA}, V_{OUTB}) active pull down	V_{VDDA} and V_{VDDB} unpowered, I_{OUTA}, I_{OUTB} = 200 mA		1.6	2	V

(1) Current direction in the testing conditions are defined to be positive into the pin and negative out of the specified terminal (unless otherwise noted).

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(2) Parameters that has only typical values, are not production tested and guaranteed by design.

6.9 Switching Characteristics

V_{VCCI} = 3.3 V or 5.5 V, 0.1-µF capacitor from VCCI to GND, V_{VDDA} = V_{VDDB} = 12 V, 1-µF capacitor from VDDA and VDDB to VSSA and VSSB, load capacitance C_{OUT} = 0 pF, T_J = –40°C to +125°C, unless otherwise noted(1).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{RISE}	Output rise time, see 図 7-4	C_{VDD} = 10 µF, C_{OUT} = 1.8 nF, V_{VDDA}, V_{VDDB} = 12 V, f = 1 kHz		8		ns
t_{FALL}	Output fall time, see 図 7-4	C_{VDD} = 10 µF, C_{OUT} = 1.8 nF , V_{VDDA}, V_{VDDB} = 12 V, f = 1 kHz		8		ns
t_{PWmin}	Minimum input pulse width that passes to output, see 図 7-1 and 図 7-2	Output does not change the state if input signal less than t_{PWmin}	4	12	30	ns
t_{PDHL}	Propagation delay at falling edge, see 図 7-3	INx high threshold, V_{INH}, to 10% of the output	26	33	45	ns
t_{PDLH}	Propagation delay at rising edge, see 図 7-3	INx low threshold, V_{INL}, to 90% of the output	26	33	45	ns
t_{PWD}	Pulse width distortion in each channel, see 図 7-3	$\lvert t_{PDLHA} - t_{PDHLA} \rvert$, $\lvert t_{PDLHB} - t_{PDHLB} \rvert$			5	ns
t_{DM}	Propagation delays matching, $\lvert t_{PDLHA} - t_{PDLHB} \rvert$, $\lvert t_{PDHLA} - t_{PDHLB} \rvert$, see 図 7-3	Input Pulse Width = 100ns, 500kHz, T_J = -40°C to -10°C $\lvert t_{PDLHA} - t_{PDLHB} \rvert$, $\lvert t_{PDHLA} - t_{PDHLB} \rvert$			6.5	ns
		Input Pulse Width = 100ns, 500kHz, T_J = -10°C to +150°C $\lvert t_{PDLHA} - t_{PDLHB} \rvert$, $\lvert t_{PDHLA} - t_{PDHLB} \rvert$			5	ns
$t_{VCCI+ to OUT}$	VCCI Power-up Delay Time: UVLO Rise to OUTA, OUTB, See 図 7-6	INA or INB tied to VCCI	18	42	80	µs
$t_{VDD+ to OUT}$	VDDA, VDDB Power-up Delay Time: UVLO Rise to OUTA, OUTB See 図 7-7	INA or INB tied to VCCI			10	µs
$\lvert CM_H \rvert$	High-level common-mode transient immunity (See セクション 7.6)	Slew rate of GND vs. VSSA/B, INA and INB both are tied to GND or VCCI; V_{CM}=1000 V;	125			V/ns
$\lvert CM_L \rvert$	Low-level common-mode transient immunity (See セクション 7.6)	Slew rate of GND vs. VSSA/B, INA and INB both are tied to GND or VCCI; V_{CM}=1000 V;	125			V/ns

(1) Parameters that has only typical values, are not production tested and guaranteed by design.

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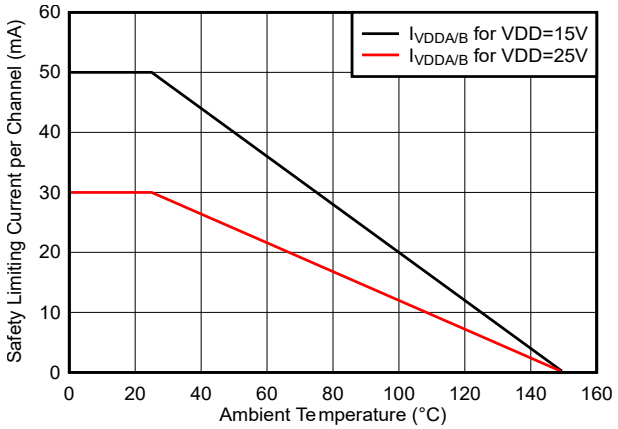
6.10 Thermal Derating Curves



Current in Each Channel with Both Channels Running Simultaneously

図 6-1. Thermal Derating Curve for Limiting Current Per VDE

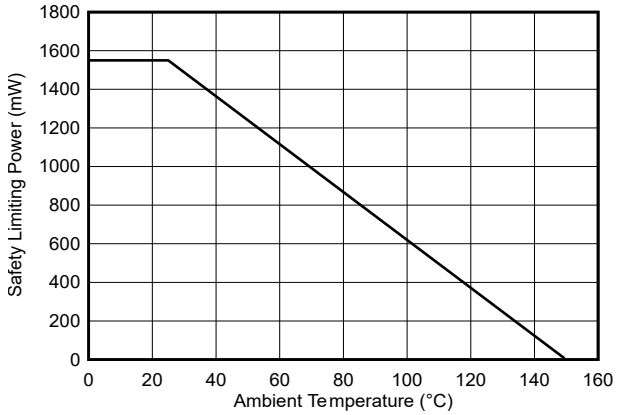


図 6-2. Thermal Derating Curve for Limiting Power Per VDE

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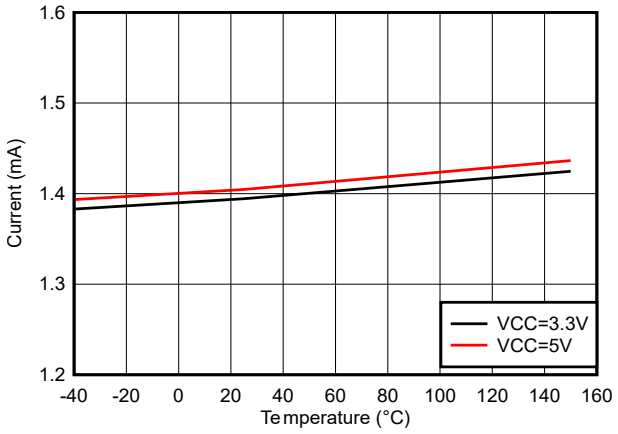
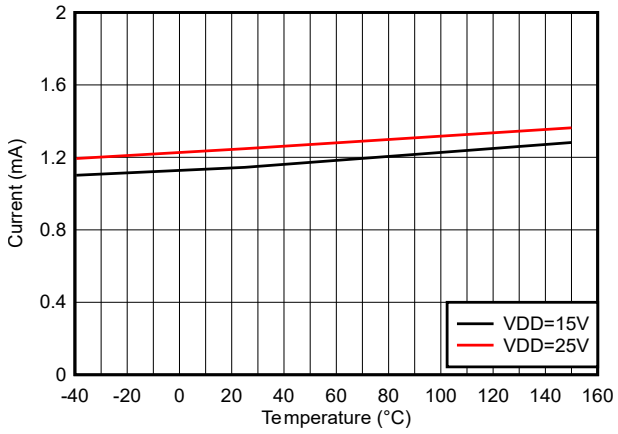
6.11 Typical Characteristics

VDDA = VDDB = 15 V, VCCI = 3.3 V, T_A = 25°C, C_L=0pF unless otherwise noted.



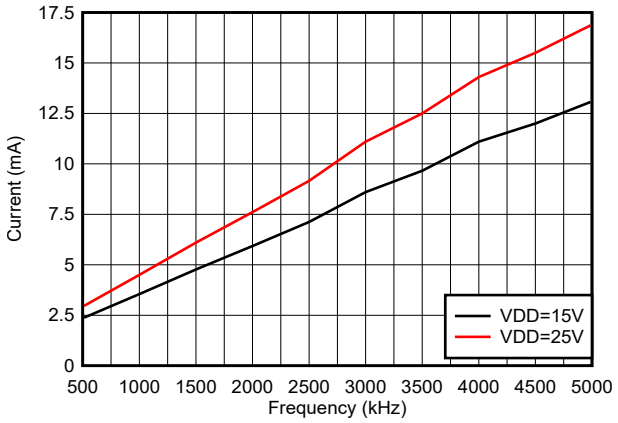
No Load INA = INB = GND

図 6-3. VCCI Quiescent Current



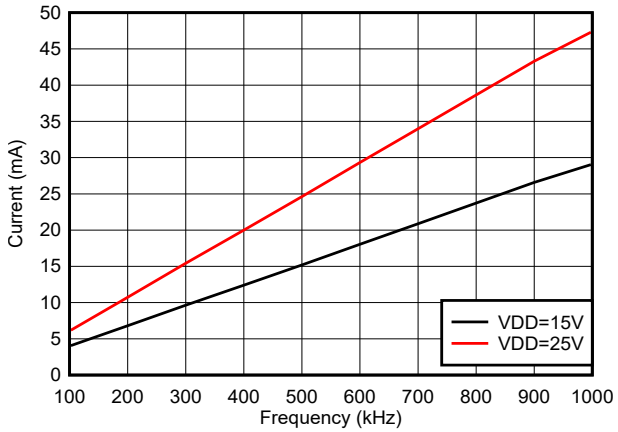
No Load INA = INB = GND

図 6-4. VDD Per Channel Quiescent Current (I_{VDDA}, I_{VDDB})



No Load

図 6-5. VDD Per Channel Operating Current - $I_{VDDA/B}$



1nF Load INA and INB both switching

図 6-6. Per Channel Operating Current ($I_{VDDA/B}$) vs Frequency

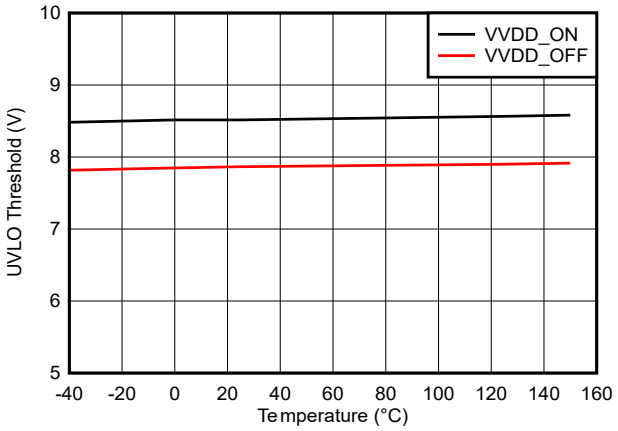


図 6-7. 8-V VDD UVLO Threshold Voltage

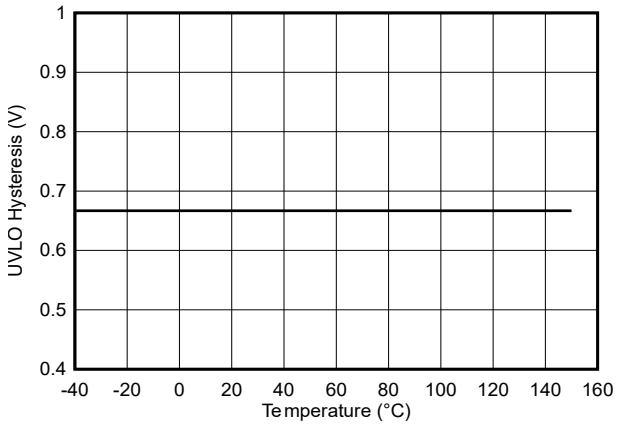


図 6-8. 8-V VDD UVLO Threshold Hysteresis

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6.11 Typical Characteristics (continued)

VDDA = VDDB = 15 V, VCCI = 3.3 V, T_A = 25°C, C_L=0pF unless otherwise noted.

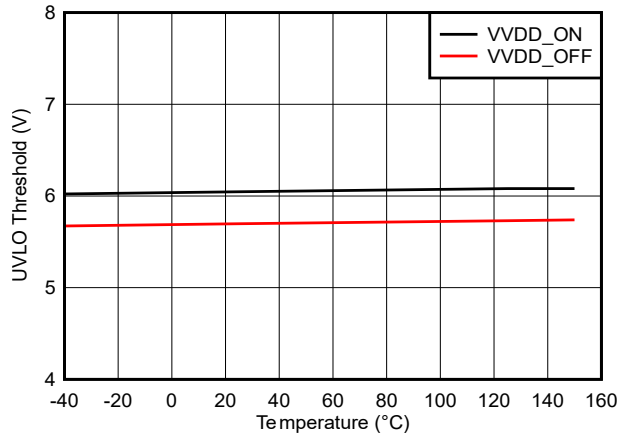

図 6-9. 5-V VDD UVLO Threshold Voltage

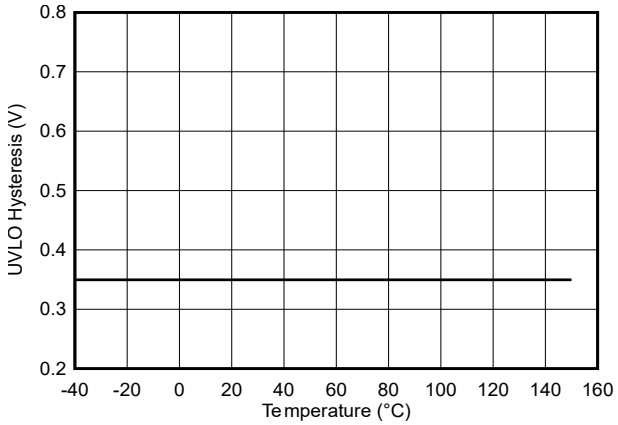

図 6-10. 5-V VDD UVLO Threshold Hysteresis

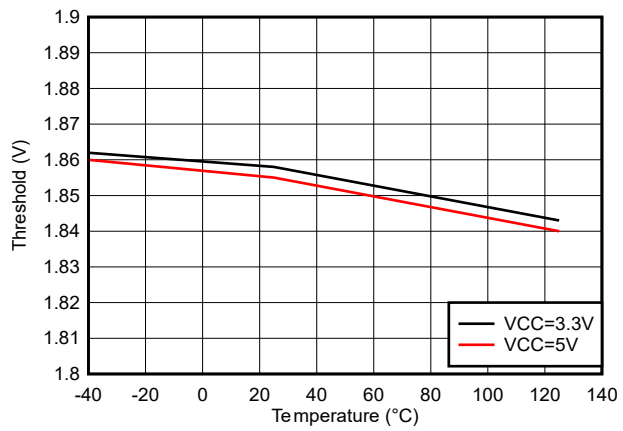

図 6-11. INA/INB/DIS High Threshold Voltage

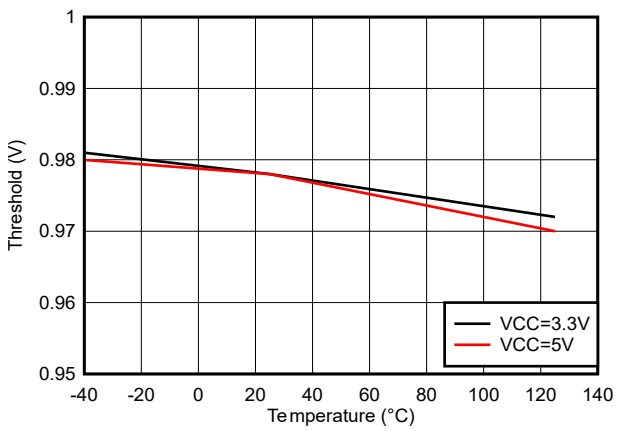

図 6-12. INA/INB/DIS Low Threshold Voltage

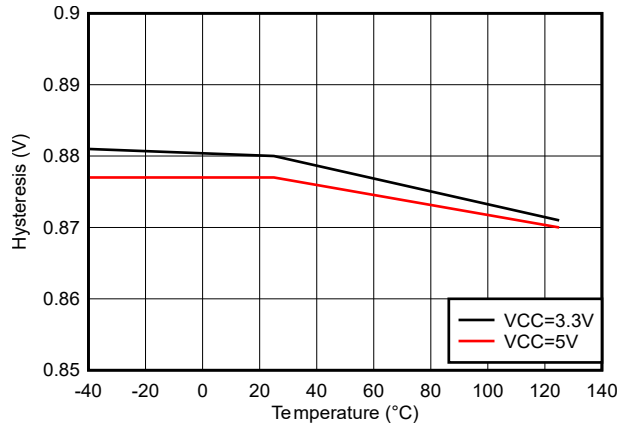

図 6-13. INA/INB/DIS High and Low Threshold Hysteresis

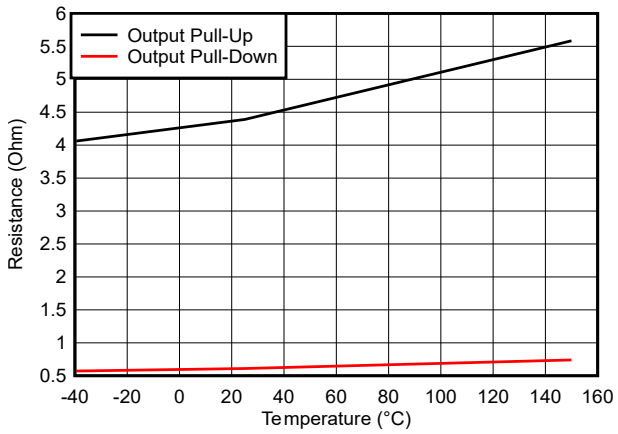

図 6-14. OUT Pullup and Pulldown Resistance

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6.11 Typical Characteristics (continued)

VDDA = VDDB = 15 V, VCCI = 3.3 V, T_A = 25°C, C_L=0pF unless otherwise noted.

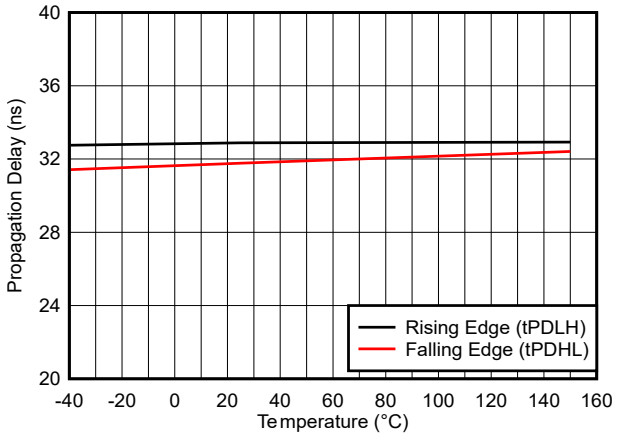

図 6-15. Propagation Delay, Rising Edge, and Falling Edge

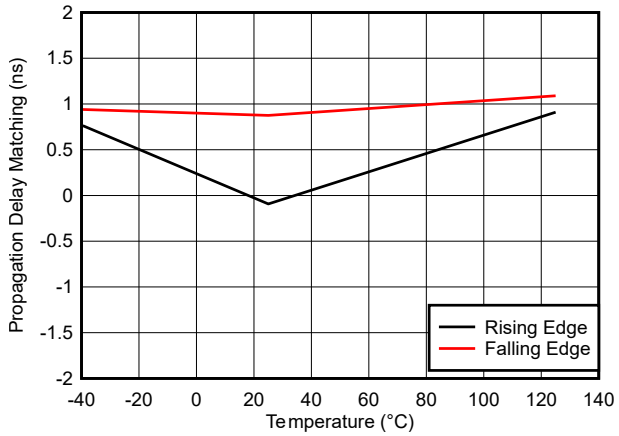

図 6-16. Propagation Delay Matching, Rising Edge, and Falling Edge

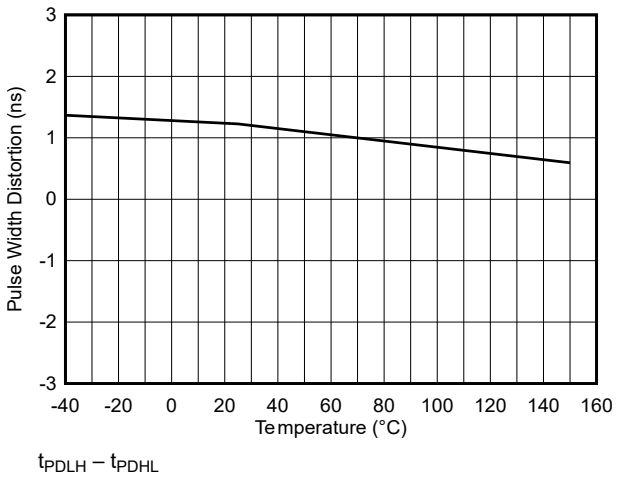

図 6-17. Pulse Width Distortion vs Temperature

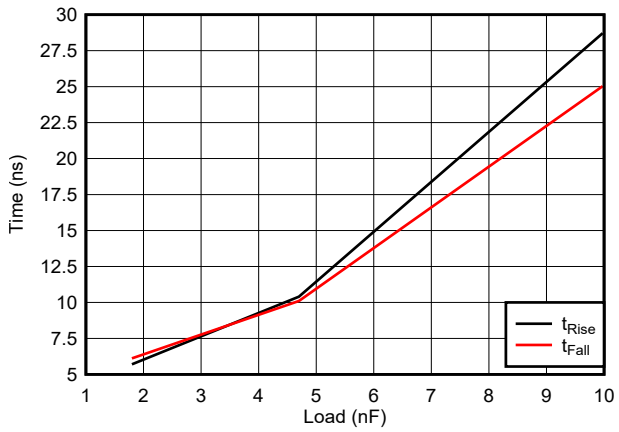

図 6-18. Rise Time and Fall Time vs Load (VDD = 15V)

7 Parameter Measurement Information

7.1 Minimum Pulses

To change the output stage on OUTA or OUTB, one has to assert longer pulses than $t_{PW(min)}$, typically 12 ns, to guarantee an output state change. see 図 7-1 and 図 7-2 for detailed information of the operation of deglitch filter.

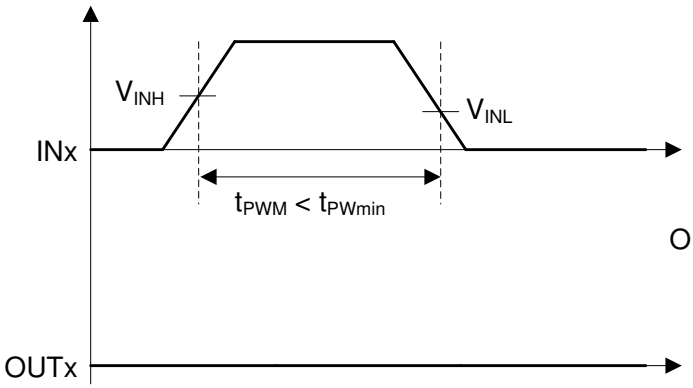

図 7-1. Deglitch Filter – Turn ON

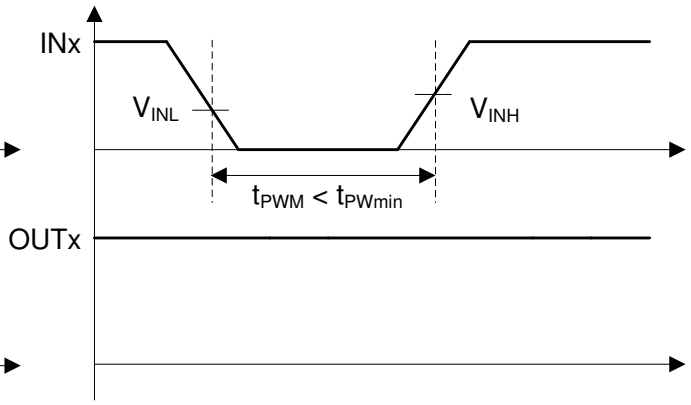

図 7-2. Deglitch Filter – Turn OFF

7.2 Propagation Delay and Pulse Width Distortion

図 7-3 shows how one calculates pulse width distortion (t_{PWD}) and delay matching (t_{DM}) from the propagation delays of channels A and B. It can be measured by ensuring that both inputs are in phase.

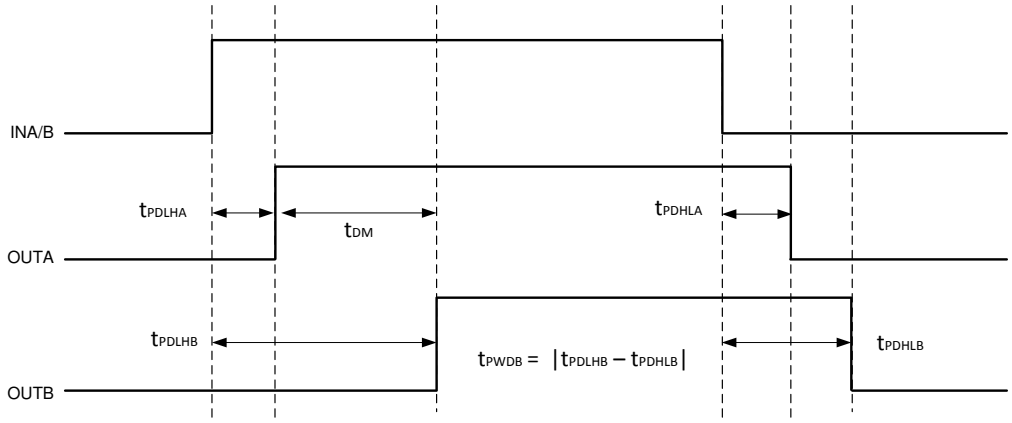

図 7-3. Delay Matching and Pulse Width Distortion

7.3 Rising and Falling Time

図 7-4 shows the criteria for measuring rising (t_{RISE}) and falling (t_{FALL}) times. For more information on how short rising and falling times are achieved, see セクション 8.3.4.

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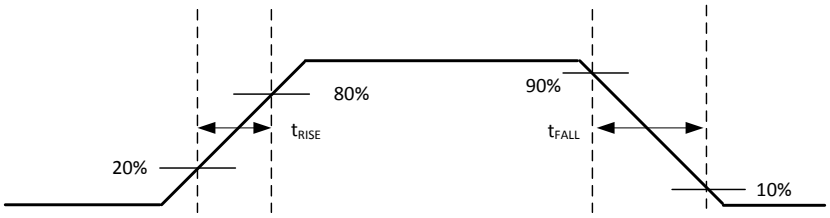

図 7-4. Rising and Falling Time Criteria

7.4 Input and Disable Response Time

図 7-5 shows the response time of the disable function. For more information, see セクション 8.4.1.

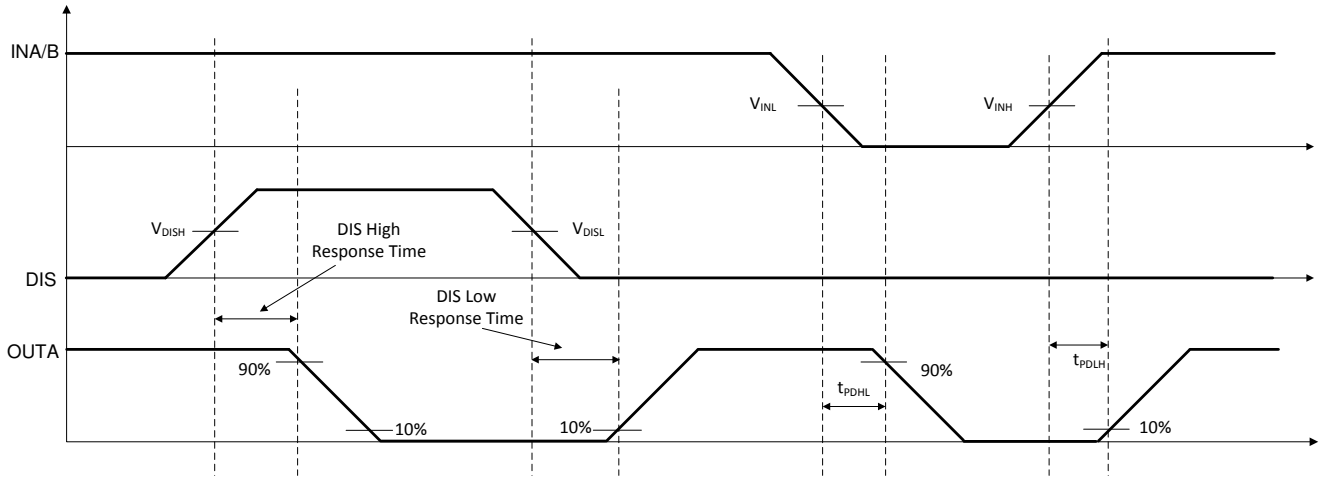

図 7-5. Disable Pin Timing

7.5 Power-up UVLO Delay to OUTPUT

Before the driver is ready to deliver a proper output state, there is a power-up delay from the UVLO rising edge to output and it is defined as $t_{VCCI+\ to\ OUT}$ for VCCI UVLO, which is 42 µs typically, and $t_{VDD+\ to\ OUT}$ for VDD UVLO, which is 10 µs maximum. It is recommended to consider proper margin before launching PWM signal after the driver VCCI and VDD bias supply is ready. 図 7-6 and 図 7-7 show the power-up UVLO delay timing diagram for VCCI and VDD.

If INA or INB are active before VCCI or VDD have crossed above their respective on thresholds, the output will not update until $t_{VCCI+\ to\ OUT}$ or $t_{VDD+\ to\ OUT}$ after VCCI or VDD crossing its UVLO rising threshold. However, when either VCCI or VDD receive a voltage less than their respective off thresholds, there is <2µs delay, depending on the voltage slew rate on the supply pins, before the outputs are held low. This asymmetric delay is designed to ensure safe operation during VCCI or VDD brownouts.

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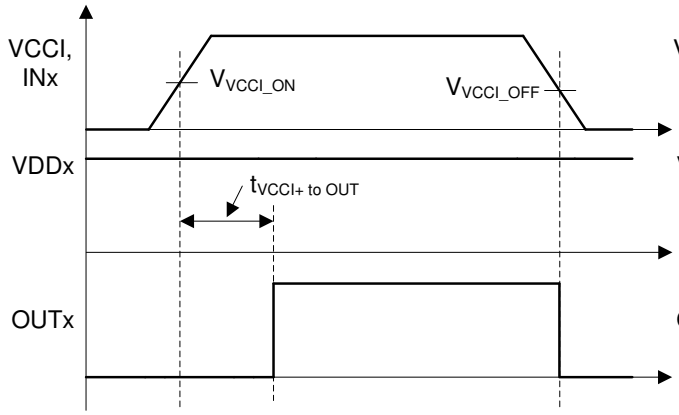

図 7-6. VCCI Power-up UVLO Delay

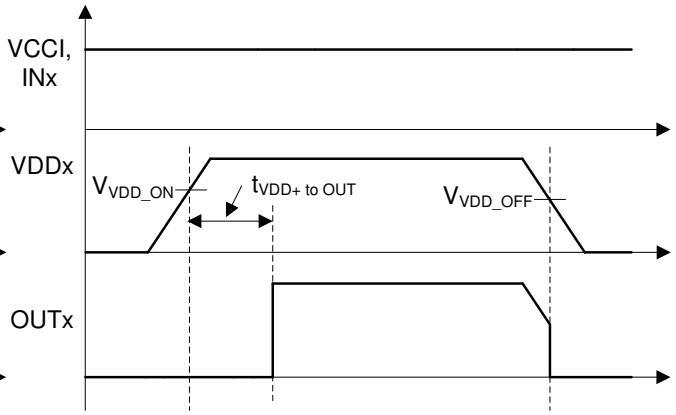

図 7-7. VDDA/B Power-up UVLO Delay

7.6 CMTI Testing

図 7-8 is a simplified diagram of the CMTI testing configuration.

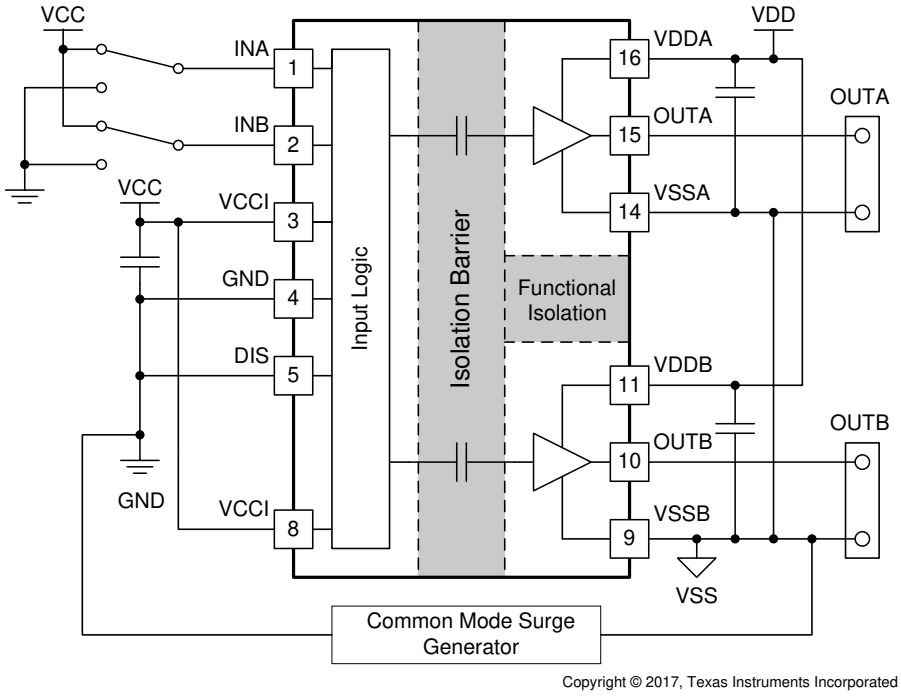

図 7-8. Simplified CMTI Testing Setup

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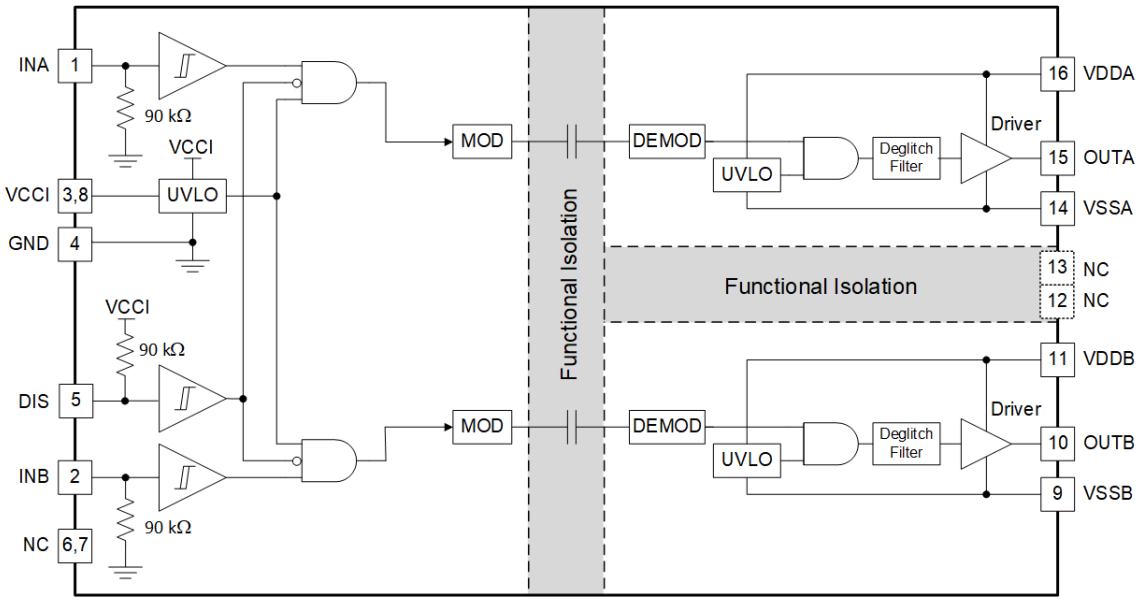
8 Detailed Description

8.1 Overview

In order to switch power transistors rapidly and reduce switching power losses, high-current gate drivers are often placed between the output of control devices and the gates of power transistors. There are several instances where controllers are not capable of delivering sufficient current to drive the gates of power transistors. This is especially the case with digital controllers, since the input signal from the digital controller is often a 3.3-V logic signal capable of only delivering a few mA.

The UCC21220, UCC21220A are flexible dual gate drivers which can be configured to fit a variety of power supply and motor drive topologies, as well as drive several types of transistors. UCC21220 and UCC21220A have many features that allow it to integrate well with control circuitry and protect the gates it drives such as: disable pin, and under voltage lock out (UVLO) for both input and output voltages. The UCC21220, UCC21220A also hold its outputs low when the inputs are left open or when the input pulse is not wide enough. The driver inputs are CMOS and TTL compatible for interfacing with digital and analog power controllers alike. Each channel is controlled by its respective input pins (INA and INB), allowing full and independent control of each of the outputs.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 VDD, VCCI, and Under Voltage Lock Out (UVLO)

The UCC21220 and UCC21220A have an internal under voltage lock out (UVLO) protection feature on the supply circuit blocks between the VDD and VSS pins for both outputs. When the VDD bias voltage is lower than V_{VDD_ON} at device start-up or lower than V_{VDD_OFF} after start-up, the VDD UVLO feature holds the effected output low, regardless of the status of the input pins (INA and INB).

When the output stages of the driver are in an unbiased or UVLO condition, the driver outputs are held low by an active clamp circuit that limits the voltage rise on the driver outputs (Illustrated in 図 8-1). In this condition, the upper PMOS is resistively held off by R_{Hi-Z} while the lower NMOS gate is tied to the driver output through R_{CLAMP}. In this configuration, the output is effectively clamped to the threshold voltage of the lower NMOS device, typically around 1.5V, when no bias power is available.

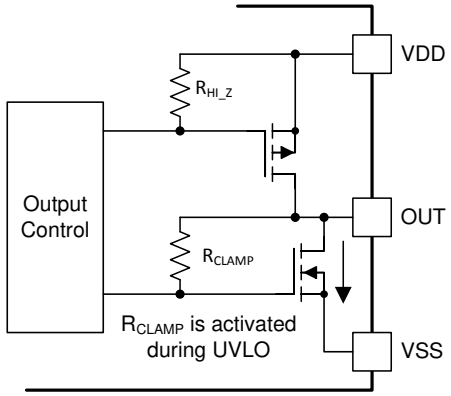


図 8-1. Simplified Representation of Active Pull Down Feature

The VDD UVLO protection has a hysteresis feature (V_{VDD_HYS}). This hysteresis prevents chatter when there is ground noise from the power supply. Also this allows the device to accept small drops in bias voltage, which is bound to happen when the device starts switching and operating current consumption increases suddenly.

The input side of the UCC21220 and UCC21220A also have an internal under voltage lock out (UVLO) protection feature. The device isn't active unless the voltage, VCCI, is going to exceed V_{VCCI_ON} on start up. And a signal will cease to be delivered when that pin receives a voltage less than V_{VCCI_OFF}. And, just like the UVLO for VDD, there is hystersis (V_{VCCI_HYS}) to ensure stable operation.

表 8-1. VCCI UVLO Feature Logic

CONDITION	INPUTS		OUTPUTS	
	INA	INB	OUTA	OUTB
VCCI-GND < V_{VCCI_ON} during device start up	H	L	L	L
VCCI-GND < V_{VCCI_ON} during device start up	L	H	L	L
VCCI-GND < V_{VCCI_ON} during device start up	H	H	L	L
VCCI-GND < V_{VCCI_ON} during device start up	L	L	L	L
VCCI-GND < V_{VCCI_OFF} after device start up	H	L	L	L
VCCI-GND < V_{VCCI_OFF} after device start up	L	H	L	L
VCCI-GND < V_{VCCI_OFF} after device start up	H	H	L	L
VCCI-GND < V_{VCCI_OFF} after device start up	L	L	L	L

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表 8-2. VDD UVLO Feature Logic

CONDITION	INPUTS		OUTPUTS	
	INA	INB	OUTA	OUTB
VDD-VSS < V_{VDD_ON} during device start up	H	L	L	L
VDD-VSS < V_{VDD_ON} during device start up	L	H	L	L
VDD-VSS < V_{VDD_ON} during device start up	H	H	L	L
VDD-VSS < V_{VDD_ON} during device start up	L	L	L	L
VDD-VSS < V_{VDD_OFF} after device start up	H	L	L	L
VDD-VSS < V_{VDD_OFF} after device start up	L	H	L	L
VDD-VSS < V_{VDD_OFF} after device start up	H	H	L	L
VDD-VSS < V_{VDD_OFF} after device start up	L	L	L	L

8.3.2 Input and Output Logic Table

表 8-3. INPUT/OUTPUT Logic Table (1)

Assume VCCI, VDDA, VDDB are powered up (see セクション 8.3.1 for more information on UVLO operation modes), 表 8-3 shows the operation with INA, INB and DIS and the corresponding output state.

INPUTS		DIS	OUTPUTS		NOTE
INA	INB		OUTA	OUTB	
L	L	L	L	L	Disables both driver outputs if asserted high, enables if set low or left open. This pin is pulled low internally if left open. It is recommended to tie this pin to ground if not used to achieve better noise immunity. Bypass using a ≈1nF low ESR/ESL capacitor close to DIS pin when connecting to a µC with distance.
L	H	L	L	H	
H	L	L	H	L	
H	H	L	H	H	
Left Open	Left Open	L	L	L	It is recommended to tie INA/INB to ground if not used to achieve better noise immunity.
X	X	H or Left Open	L	L	-

(1) "X" means L, H or left open.

8.3.3 Input Stage

The input pins (INA, INB, and DIS) of UCC21220 and UCC21220A are based on a TTL and CMOS compatible input-threshold logic that is totally isolated from the VDD supply voltage. The input pins are easy to drive with logic-level control signals (such as those from 3.3-V micro-controllers), since the UCC21220 and UCC21220A have a typical high threshold (V_{INAH}) of 2 V and a typical low threshold of 1 V, which vary little with temperature (see 図 6-8 and 図 6-13). A wide hysterisis (V_{INA_HYS}) of 1 V makes for good noise immunity and stable operation. If any of the inputs are ever left open, internal pull-down resistors force the pin low. These resistors are typically 90 kΩ for INA/B. However, it is still recommended to ground an input if it is not being used.

Since the input side of UCC21220 or UCC21220A are isolated from the output drivers, the input signal amplitude can be larger or smaller than VDD, provided that it doesn't exceed the recommended limit. This allows greater flexibility when integrating with control signal sources, and allows the user to choose the most efficient VDD for their MOSFET/IGBT gate. That said, the amplitude of any signal applied to INA or INB must *never* be at a voltage higher than VCCI.

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8.3.4 Output Stage

The UCC21220 and UCC21220A output stages feature a pull-up structure which delivers the highest peak-source current when it is most needed, during the Miller plateau region of the power-switch turn on transition (when the power switch drain or collector voltage experiences dV/dt). The output stage pull-up structure features a P-channel MOSFET and an additional *Pull-Up* N-channel MOSFET in parallel. The function of the N-channel MOSFET is to provide a boost in the peak-sourcing current, enabling fast turn on. This is accomplished by briefly turning on the N-channel MOSFET during a narrow instant when the output is changing states from low to high. The on-resistance of this N-channel MOSFET (R_{NMOS}) is approximately 1.47 Ω when activated.

The R_{OH} parameter is a DC measurement and it is representative of the on-resistance of the P-channel device only. This is because the *Pull-Up* N-channel device is held in the off state in DC condition and is turned on only for a brief instant when the output is changing states from low to high. Therefore the effective resistance of the UCC21220 and UCC21220A pull-up stage during this brief turn-on phase is much lower than what is represented by the R_{OH} parameter.

The pull-down structure of the UCC21220 and UCC21220A are composed of an N-channel MOSFET. The R_{OL} parameter, which is also a DC measurement, is representative of the impedance of the pull-down state in the device. Both outputs of the UCC21220 and UCC21220A are capable of delivering 4-A peak source and 6-A peak sink current pulses. The output voltage swings between VDD and VSS provides rail-to-rail operation, thanks to the MOS-out stage which delivers very low drop-out.

To ensure robust and reliable operation of gate drivers, pay special attention to the minimum pulse width. The minimum pulse width shown in the electrical characteristics table describes the minimum input pulse that would be passed to the output in an unloaded driver. This is dictated by the deglitch filter present in the driver IC. An input ON or OFF pulse width longer than the maximum specification is needed to guarantee an output state change and avoid potential shoot-through. With a loaded driver, extra precaution must be taken to ensure robust operation of the system. During gate switching, if the output state changes before the driver completes each transition, a non-zero current switching event occurs. Combined with layout parasitics, non-zero current switching can cause internal rail overshoot and EOS damage of the gate driver. Thus, a minimum output width is needed for reliable system operation. This minimum output pulse width is dependent on several factors: gate capacitance, VDD supply voltage, gate resistance, and PCB layout parasitics. The minimum pulse width for robust operation might be magnitudes larger than the minimum pulse width shown in the electrical characteristics table. System-level study should be carried out to determine the minimum output pulse width required for each system.

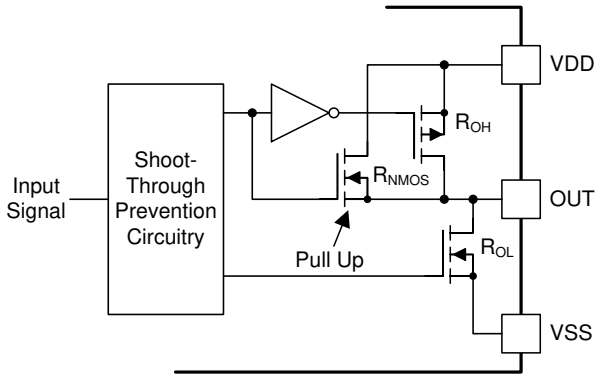

図 8-2. Output Stage

8.3.5 Diode Structure in UCC21220 and UCC21220A

図 8-3 illustrates the multiple diodes involved in the ESD protection components. This provides a pictorial representation of the absolute maximum rating for the device.

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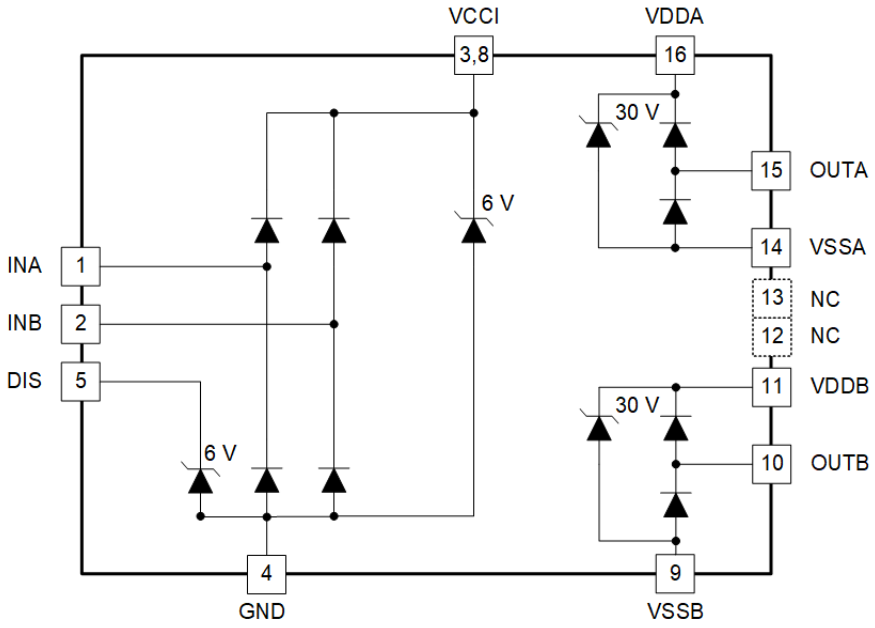

図 8-3. ESD Structure

8.4 Device Functional Modes

8.4.1 Disable Pin

Setting the DIS pin high (or left floating) shuts down both outputs simultaneously. Grounding the DIS pin allows UCC21220 and UCC21220A to operate normally. The DIS pin is quite responsive, as far as propagation delay and other switching parameters are concerned. The DIS pin is only functional (and necessary) when VCCI stays above the UVLO threshold. It is recommended to tie this pin to GND if the DIS pin is not used to achieve better noise immunity, and it is recommended to bypass using a ≈1nF low ESR/ESL capacitor close to DIS pin when connecting DIS pin to a micro controller with distance.

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9 Application and Implementation

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9.1 Application Information

The UCC21220 and UCC21220A effectively combine both isolation and buffer-drive functions. The flexible, universal capability of the UCC21220 (with up to 5.5-V VCCI and 18-V VDDA/VDDB) allows the device to be used as a low-side, high-side, high-side/low-side or half-bridge driver for MOSFETs, IGBTs or GaN transistor. With integrated components, advanced protection features (UVLO and disable) and optimized switching performance; the UCC21220 and UCC21220A enable designers to build smaller, more robust designs for enterprise, telecom, automotive, and industrial applications with a faster time to market.

9.2 Typical Application

The circuit in 図 9-1 shows a reference design with UCC21220 or UCC21220A driving a typical half-bridge configuration which could be used in several popular power converter topologies such as synchronous buck, synchronous boost, half-bridge/full bridge isolated topologies, and 3-phase motor drive applications.

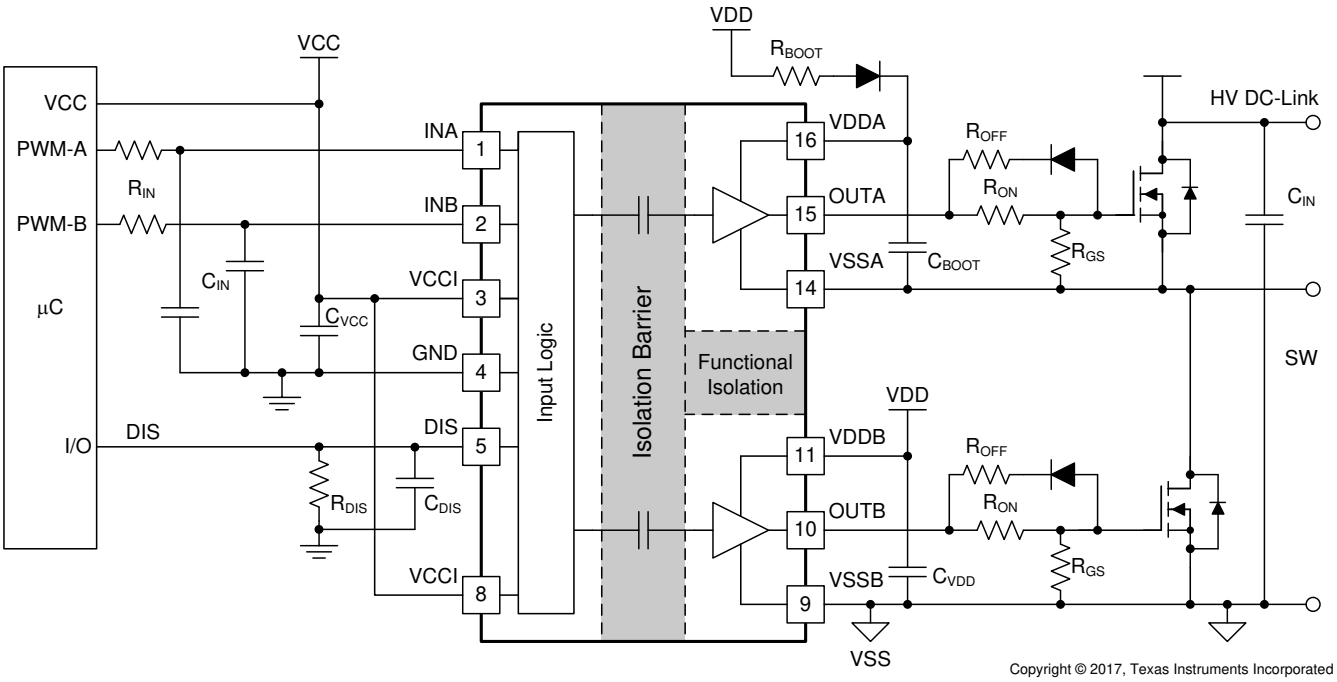

図 9-1. Typical Application Schematic

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9.2.1 Design Requirements

表 9-1 lists reference design parameters for the example application: UCC21220 or UCC21220A driving 650-V MOSFETs in a high side-low side configuration.

表 9-1. UCC21220 and UCC21220A Design Requirements

PARAMETER	VALUE	UNITS
Power transistor	IPP65R150CFD	-
VCC	5.0	V
VDD	12	V
Input signal amplitude	3.3	V
Switching frequency (f_s)	100	kHz
DC link voltage	400	V

9.2.2 Detailed Design Procedure

9.2.2.1 Designing INA/INB Input Filter

It is recommended that users avoid shaping the signals to the gate driver in an attempt to slow down (or delay) the signal at the output. However, a small input R_{IN}-C_{IN} filter can be used to filter out the ringing introduced by non-ideal layout or long PCB traces.

Such a filter should use an R_{IN} in the range of 0 Ω to100 Ω and a C_{IN} between 10 pF and 100 pF. In the example, an R_{IN} = 51 Ω and a C_{IN} = 33 pF are selected, with a corner frequency of approximately 100 MHz.

When selecting these components, it is important to pay attention to the trade-off between good noise immunity and propagation delay.

9.2.2.2 Select External Bootstrap Diode and its Series Resistor

The bootstrap capacitor is charged by VDD through an external bootstrap diode every cycle when the low side transistor turns on. Charging the capacitor involves high-peak currents, and therefore transient power dissipation in the bootstrap diode may be significant. Conduction loss also depends on the diode's forward voltage drop. Both the diode conduction losses and reverse recovery losses contribute to the total losses in the gate driver circuit.

When selecting external bootstrap diodes, it is recommended that one chose high voltage, fast recovery diodes or SiC Schottky diodes with a low forward voltage drop and low junction capacitance in order to minimize the loss introduced by reverse recovery and related grounding noise bouncing. In the example, the DC-link voltage is 400 V_{DC}. The voltage rating of the bootstrap diode should be higher than the DC-link voltage with a good margin. Therefore, a 600-V ultrafast diode, MURA160T3G, is chosen in this example.

A bootstrap resistor, R_{BOOT}, is used to reduce the inrush current in D_{BOOT} and limit the ramp up slew rate of voltage of VDDA-VSSA during each switching cycle, especially when the VSSA(SW) pin has an excessive negative transient voltage. The recommended value for R_{BOOT} is between 1 Ω and 20 Ω depending on the diode used. In the example, a current limiting resistor of 2.2 Ω is selected to limit the inrush current of bootstrap diode. The estimated worst case peak current through D_{Boot} is,

$$I_{DBoot(pk)} = \frac{V_{DD} - V_{BDF}}{R_{Boot}} = \frac{12V - 1.5V}{2.7\Omega} \approx 4A \quad (1)$$

where

- V_{BDF} is the estimated bootstrap diode forward voltage drop around 4 A.

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9.2.2.3 Gate Driver Output Resistor

The external gate driver resistors, R_{ON}/R_{OFF}, are used to:

1. Limit ringing caused by parasitic inductances/capacitances.
2. Limit ringing caused by high voltage/current switching dv/dt, di/dt, and body-diode reverse recovery.
3. Fine-tune gate drive strength, i.e. peak sink and source current to optimize the switching loss.
4. Reduce electromagnetic interference (EMI).

As mentioned in セクション 8.3.4, the UCC21220 and UCC21220A have a pull-up structure with a P-channel MOSFET and an additional *pull-up* N-channel MOSFET in parallel. The combined peak source current is 4 A. Therefore, the peak source current can be predicted with 式 2 and 式 3:

$$I_{OA+} = \min\left(4A, \frac{V_{DD} - V_{BDF}}{R_{NMOS} \,||\, R_{OH} + R_{ON} + R_{GFET_Int}}\right) \tag{2}$$

$$I_{OB+} = \min\left(4A, \frac{V_{DD}}{R_{NMOS} \,||\, R_{OH} + R_{ON} + R_{GFET_Int}}\right) \tag{3}$$

where

- R_{ON}: External turn-on resistance.
- R_{GFET_INT}: Power transistor internal gate resistance, found in the power transistor datasheet.
- I_{O+} = Peak source current – The minimum value between 4 A, the gate driver peak source current, and the calculated value based on the gate drive loop resistance.

In this example:

$$I_{OA+} = \frac{V_{DD} - V_{BDF}}{R_{NMOS} \,||\, R_{OH} + R_{ON} + R_{GFET_Int}} = \frac{12V - 0.8V}{1.47\Omega \,||\, 5\Omega + 2.2\Omega + 1.5\Omega} \approx 2.3A \tag{4}$$

$$I_{OB+} = \frac{V_{DD}}{R_{NMOS} \,||\, R_{OH} + R_{ON} + R_{GFET_Int}} = \frac{12V}{1.47\Omega \,||\, 5\Omega + 2.2\Omega + 1.5\Omega} \approx 2.5A \tag{5}$$

Therefore, the high-side and low-side peak source current is 2.3 A and 2.5 A respectively. Similarly, the peak sink current can be calculated with 式 6 and 式 7:

$$I_{OA-} = \min\left(6A, \frac{V_{DD} - V_{BDF} - V_{GDF}}{R_{OL} + R_{OFF} \,||\, R_{ON} + R_{GFET_Int}}\right) \tag{6}$$

$$I_{OB-} = \min\left(6A, \frac{V_{DD} - V_{GDF}}{R_{OL} + R_{OFF} \,||\, R_{ON} + R_{GFET_Int}}\right) \tag{7}$$

where

- R_{OFF}: External turn-off resistance, R_{OFF}=0 in this example;
- V_{GDF}: The anti-parallel diode forward voltage drop which is in series with R_{OFF}. The diode in this example is an MSS1P4.

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- I_{O-}: Peak sink current – the minimum value between 6 A, the gate driver peak sink current, and the calculated value based on the gate drive loop resistance.

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In this example,

$$I_{OA-} = \frac{V_{DD} - V_{BDF} - V_{GDF}}{R_{OL} + R_{OFF} \,||\, R_{ON} + R_{GFET_Int}} = \frac{12V - 0.8V - 0.85V}{0.55\Omega + 0\Omega + 1.5\Omega} \approx 5.0A \quad (8)$$

$$I_{OB-} = \frac{V_{DD} - V_{GDF}}{R_{OL} + R_{OFF} \,||\, R_{ON} + R_{GFET_Int}} = \frac{12V - 0.85V}{0.55\Omega + 0\Omega + 1.5\Omega} \approx 5.4A \quad (9)$$

Therefore, the high-side and low-side peak sink current is 5.0 A and 5.4A respectively.

Importantly, the estimated peak current is also influenced by PCB layout and load capacitance. Parasitic inductance in the gate driver loop can slow down the peak gate drive current and introduce overshoot and undershoot. Therefore, it is strongly recommended that the gate driver loop should be minimized. On the other hand, the peak source/sink current is dominated by loop parasitics when the load capacitance (C_{ISS}) of the power transistor is very small (typically less than 1 nF), because the rising and falling time is too small and close to the parasitic ringing period.

9.2.2.4 Estimating Gate Driver Power Loss

The total loss, P_G, in the gate driver subsystem includes the power losses of the UCC21220 and UCC21220A (P_{GD}) and the power losses in the peripheral circuitry, such as the external gate drive resistor. Bootstrap diode loss is not included in P_G and not discussed in this section.

P_{GD} is the key power loss which determines the thermal safety-related limits of the UCC21220 and UCC21220A, and it can be estimated by calculating losses from several components.

The first component is the static power loss, P_{GDQ}, which includes quiescent power loss on the driver as well as driver self-power consumption when operating with a certain switching frequency. P_{GDQ} is measured on the bench with no load connected to OUTA and OUTB at a given VCCI, VDDA/VDDB, switching frequency and ambient temperature. 図 6-6 shows the operating current consumption vs. operating frequency with no load. In this example, V_{VCCI} = 5 V and V_{VDD} = 12 V. The current on each power supply, with INA/INB switching from 0 V to 3.3 V at 100 kHz is measured to be I_{VCCI} ≈ 2.5 mA, and I_{VDDA} = I_{VDDB} ≈ 1.5 mA. Therefore, the P_{GDQ} can be calculated with 式 10:

$$P_{GDQ} = V_{VCCI} \times I_{VCCI} + V_{VDDA} \times I_{DDA} + V_{VDDB} \times I_{DDB} = 50mW \quad (10)$$

The second component is switching operation loss, P_{GDO}, with a given load capacitance which the driver charges and discharges the load during each switching cycle. Total dynamic loss due to load switching, P_{GSW}, can be estimated with 式 11:

$$P_{GSW} = 2 \times V_{DD} \times Q_G \times f_{SW} \quad (11)$$

where

- Q_G is the gate charge of the power transistor.

If a split rail is used to turn on and turn off, then VDD is going to be equal to difference between the positive rail to the negative rail.

So, for this example application:

$$P_{GSW} = 2 \times 12V \times 100nC \times 100kHz = 240mW \quad (12)$$

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Q_G represents the total gate charge of the power transistor switching 480 V at 14 A provided by the datasheet, and is subject to change with different testing conditions. The UCC21220 and UCC21220A gate driver loss on the output stage, P_{GDO}, is part of P_{GSW}. P_{GDO} will be equal to P_{GSW} if the external gate driver resistances are zero, and all the gate driver loss is dissipated inside the UCC21220 and UCC21220A. If there are external turn-on and turn-off resistances, the total loss will be distributed between the gate driver pull-up/down resistances and external gate resistances. Importantly, the pull-up/down resistance is a linear and fixed resistance if the source/sink current is not saturated to 4 A/6 A, however, it will be non-linear if the source/sink current is saturated. Therefore, P_{GDO} is different in these two scenarios.

Case 1 - Linear Pull-Up/Down Resistor:

$$P_{GDO} = \frac{P_{GSW}}{2} \times \left(\frac{R_{OH} \,||\, R_{NMOS}}{R_{OH} \,||\, R_{NMOS} + R_{ON} + R_{GFET_Int}} + \frac{R_{OL}}{R_{OL} + R_{OFF} \,||\, R_{ON} + R_{GFET_Int}} \right) \tag{13}$$

In this design example, all the predicted source/sink currents are less than 4 A/6 A, therefore, the UCC21220 and UCC21220A gate driver loss can be estimated with 式 14:

$$P_{GDO} = \frac{240\text{mW}}{2} \times \left(\frac{5\Omega \,||\, 1.47\Omega}{5\Omega \,||\, 1.47\Omega + 2.2\Omega + 1.5\Omega} + \frac{0.55\Omega}{0.55\Omega + 0\Omega + 1.5\Omega} \right) \approx 60\text{mW} \tag{14}$$

Case 2 - Nonlinear Pull-Up/Down Resistor:

$$P_{GDO} = 2 \times f_{SW} \times \left[4\text{A} \times \int_0^{T_{R_Sys}} \left(V_{DD} - V_{OUTA/B}(t) \right) dt + 6\text{A} \times \int_0^{T_{F_Sys}} V_{OUTA/B}(t)\, dt \right] \tag{15}$$

where

- $V_{OUTA/B}(t)$ is the gate driver OUTA and OUTB pin voltage during the turn on and off transient, and it can be simplified that a constant current source (4 A at turn-on and 6 A at turn-off) is charging/discharging a load capacitor. Then, the $V_{OUTA/B}(t)$ waveform will be linear and the T_{R_Sys} and T_{F_Sys} can be easily predicted.

For some scenarios, if only one of the pull-up or pull-down circuits is saturated and another one is not, the P_{GDO} will be a combination of Case 1 and Case 2, and the equations can be easily identified for the pull-up and pull-down based on the above discussion. Therefore, total gate driver loss dissipated in the gate driver UCC21220 and UCC21220A, P_{GD}, is:

$$P_{GD} = P_{GDQ} + P_{GDO} \tag{16}$$

which is equal to 127 mW in the design example.

9.2.2.5 Estimating Junction Temperature

The junction temperature (T_J) of the UCC21220 and UCC21220A can be estimated with 式 17:

$$T_J = T_C + \Psi_{JT} \times P_{GD} \tag{17}$$

where

- T_C is the UCC21220 and UCC21220A case-top temperature measured with a thermocouple or some other instrument, ψ_{JT} is the junction-to-top characterization parameter from the セクション 6.4 table. Importantly, ψ_{JT}

is developed based on JEDEC standard PCB board and it is subject to change when the PCB board layout is different.

Using the junction-to-top characterization parameter (Ψ_{JT}) instead of the junction-to-case thermal resistance ($R_{\Theta JC}$) can greatly improve the accuracy of the junction temperature estimation. The majority of the thermal energy of most ICs is released into the PCB through the package leads, whereas only a small percentage of the total energy is released through the top of the case (where thermocouple measurements are usually conducted). $R_{\Theta JC}$ can only be used effectively when most of the thermal energy is released through the case, such as with metal packages or when a heatsink is applied to an IC package. In all other cases, use of $R_{\Theta JC}$ will inaccurately estimate the true junction temperature. Ψ_{JT} is experimentally derived by assuming that the amount of energy leaving through the top of the IC will be similar in both the testing environment and the application environment. As long as the recommended layout guidelines are observed, junction temperature estimates can be made accurately to within a few degrees Celsius.

For more information, see the セクション 11.1 and *Semiconductor and IC Package Thermal Metrics Application Report*.

9.2.2.6 Selecting VCCI, VDDA/B Capacitor

Bypass capacitors for VCCI, VDDA, and VDDB are essential for achieving reliable performance. It is recommended that one choose low ESR and low ESL surface-mount multi-layer ceramic capacitors (MLCC) with sufficient voltage ratings, temperature coefficients and capacitance tolerances. Importantly, DC bias on an MLCC will impact the actual capacitance value. For example, a 25-V, 1-µF X7R capacitor is measured to be only 500 nF when a DC bias of 15 V_{DC} is applied.

9.2.2.6.1 Selecting a VCCI Capacitor

A bypass capacitor connected to VCCI supports the transient current needed for the primary logic and the total current consumption, which is only a few mA. Therefore, a 25-V MLCC with over 100 nF is recommended for this application. If the bias power supply output is a relatively long distance from the VCCI pin, a tantalum or electrolytic capacitor, with a value over 1 µF, should be placed in parallel with the MLCC.

9.2.2.6.2 Selecting a VDDA (Bootstrap) Capacitor

A VDDA capacitor, also referred to as a *bootstrap capacitor* in bootstrap power supply configurations, allows for gate drive current transients up to 6 A, and needs to maintain a stable gate drive voltage for the power transistor.

The total charge needed per switching cycle can be estimated with 式 18:

$$Q_{Total} = Q_G + \frac{I_{VDD}@100kHz(\text{No Load})}{f_{SW}} = 100nC + \frac{1.5mA}{100kHz} = 115nC \quad (18)$$

where

- Q_G: Gate charge of the power transistor.
- I_{VDD}: The channel self-current consumption with no load at 100kHz.

Therefore, the absolute minimum C_{Boot} requirement is:

$$C_{Boot} = \frac{Q_{Total}}{\Delta V_{VDDA}} = \frac{115nC}{0.5V} = 230nF \quad (19)$$

where

- ΔV_{VDDA} is the voltage ripple at VDDA, which is 0.5 V in this example.

In practice, the value of C_{Boot} is greater than the calculated value. This allows for the capacitance shift caused by the DC bias voltage and for situations where the power stage would otherwise skip pulses due to load transients.

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Therefore, it is recommended to include a safety-related margin in the C_{Boot} value and place it as close to the VDD and VSS pins as possible. A 50-V 1-µF capacitor is chosen in this example.

$$C_{Boot} = 1\mu F \tag{20}$$

To further lower the AC impedance for a wide frequency range, it is recommended to have bypass capacitor with a low capacitance value, in this example a 100 nF, in parallel with C_{Boot} to optimize the transient performance.

注

Too large C_{BOOT} is not good. C_{BOOT} may not be charged within the first few cycles and V_{BOOT} could stay below UVLO. As a result, the high-side FET does not follow input signal command. Also during initial C_{BOOT} charging cycles, the bootstrap diode has highest reverse recovery current and losses.

9.2.2.6.3 Select a VDDB Capacitor

Chanel B has the same current requirements as Channel A, Therefore, a VDDB capacitor (Shown as C_{VDD} in 図 9-1) is needed. In this example with a bootstrap configuration, the VDDB capacitor will also supply current for VDDA through the bootstrap diode. A 50-V, 10-µF MLCC and a 50-V, 220-nF MLCC are chosen for C_{VDD}. If the bias power supply output is a relatively long distance from the VDDB pin, a tantalum or electrolytic capacitor with a value over 10 µF, should be used in parallel with C_{VDD}.

9.2.2.7 Application Circuits with Output Stage Negative Bias

When parasitic inductances are introduced by non-ideal PCB layout and long package leads (e.g. TO-220 and TO-247 type packages), there could be ringing in the gate-source drive voltage of the power transistor during high di/dt and dv/dt switching. If the ringing is over the threshold voltage, there is the risk of unintended turn-on and even shoot-through. Applying a negative bias on the gate drive is a popular way to keep such ringing below the threshold. Below are a few examples of implementing negative gate drive bias.

図 9-2 shows the first example with negative bias turn-off on the channel-A driver using a Zener diode on the isolated power supply output stage. The negative bias is set by the Zener diode voltage. If the isolated power supply, V_A, is equal to 17 V, the turn-off voltage will be –5.1 V and turn-on voltage will be 17 V – 5.1 V ≈ 12 V. The channel-B driver circuit is the same as channel-A, therefore, this configuration needs two power supplies for a half-bridge configuration, and there will be steady state power consumption from R_Z.

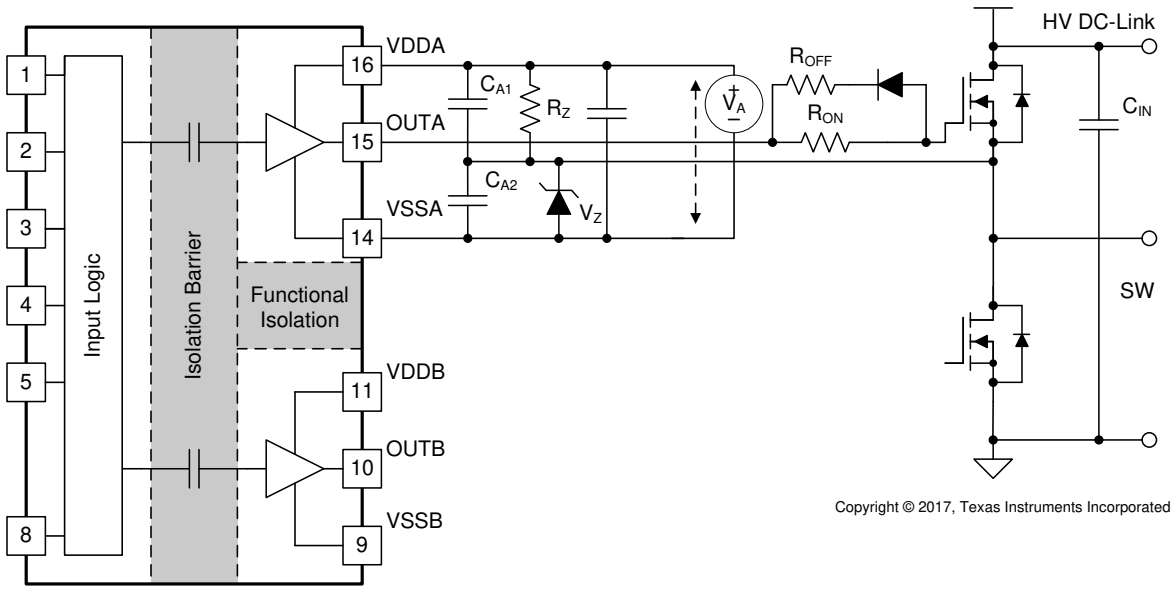

図 9-2. Negative Bias with Zener Diode on Iso-Bias Power Supply Output

図 9-3 shows another example which uses two supplies (or single-input-double-output power supply). Power supply V_{A+} determines the positive drive output voltage and $V_{A–}$ determines the negative turn-off voltage. The configuration for channel B is the same as channel A. This solution requires more power supplies than the first example, however, it provides more flexibility when setting the positive and negative rail voltages.

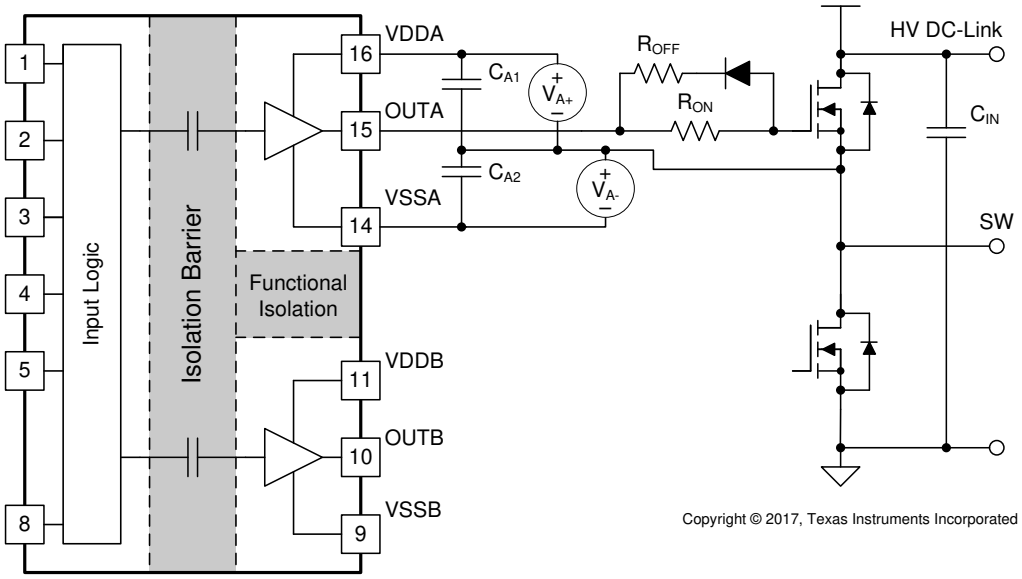

図 9-3. Negative Bias with Two Iso-Bias Power Supplies

The last example in 図 9-4 is a single power supply configuration and generates negative bias through a Zener diode in the gate drive loop. The benefit of this solution is that it only uses one power supply and the bootstrap power supply can be used for the high side drive. This design requires the least cost and design effort among the three solutions. However, this solution has limitations:

1. The negative gate drive bias is not only determined by the Zener diode, but also by the duty cycle, which means the negative bias voltage will change when the duty cycle changes. Therefore, converters with a fixed duty cycle (about 50%) such as variable frequency resonant convertors or phase shift convertors which favor this solution.
2. The high side VDDA-VSSA must maintain enough voltage to stay in the recommended power supply range, which means the low side switch must turn-on or have free-wheeling current on the body (or anti-parallel) diode for a certain period during each switching cycle to refresh the bootstrap capacitor. Therefore, a 100% duty cycle for the high side is not possible unless there is a dedicated power supply for the high side, like in the other two example circuits.

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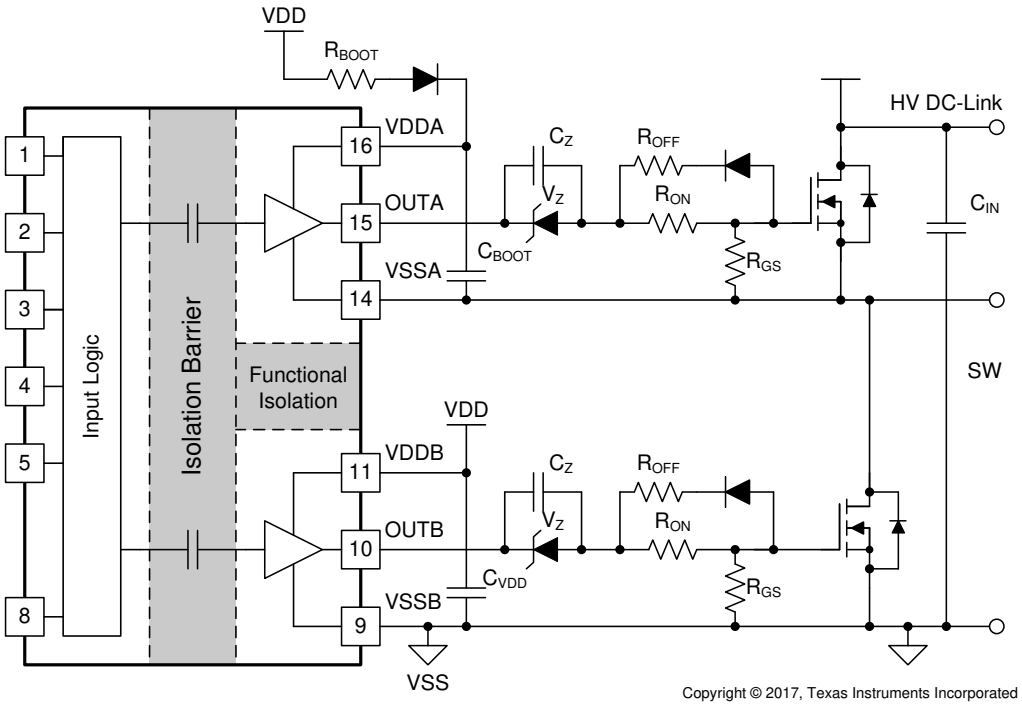

図 9-4. Negative Bias with Single Power Supply and Zener Diode in Gate Drive Path

9.2.3 Application Curves

図 9-5 and 図 9-6 shows the bench test waveforms for the design example shown in 図 9-1 under these conditions: VCC = 5.0 V, VDD = 12 V, f_{SW} = 100 kHz, $V_{DC\text{-}Link}$ = 400 V.

Channel 1 (Yellow): INA pin signal.

Channel 2 (Blue): INB pin signal.

Channel 3 (Pink): Gate-source signal on the high side power transistor.

Channel 4 (Green): Gate-source signal on the low side power transistor.

In 図 9-5, INA and INB are sent complimentary 3.3-V, 20%/80% duty-cycle signals with 200ns deadtime. The gate drive signals on the power transistor have a 200-ns dead time with 400V high voltage on the DC-Link, shown in the measurement section of 図 9-5. Note that with high voltage present, lower bandwidth differential probes are required, which limits the achievable accuracy of the measurement.

図 9-6 shows a zoomed-in version of the waveform of 図 9-5, with measurements for propagation delay and deadtime. Importantly, the output waveform is measured between the power transistors' gate and source pins, and is not measured directly from the driver's OUTA and OUTB pins.

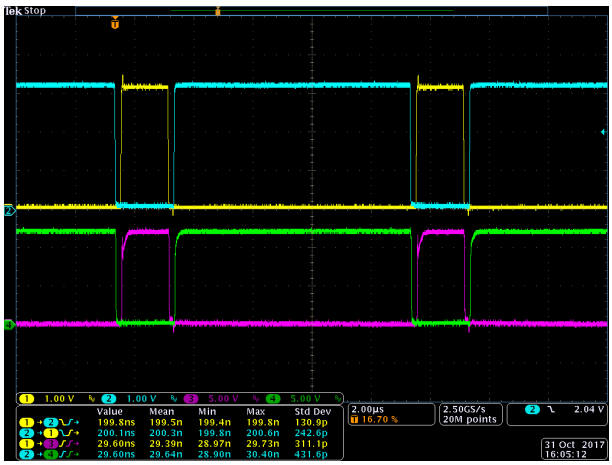

図 9-5. Bench Test Waveform for INA/B and OUTA/B

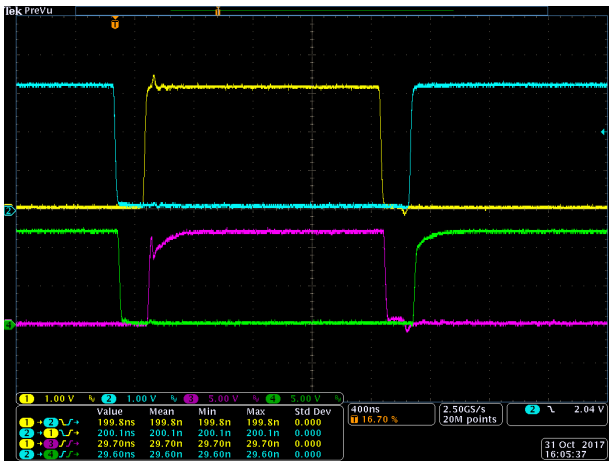

図 9-6. Zoomed-In bench-test waveform

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10 Power Supply Recommendations

The recommended input supply voltage (VCCI) for UCC21220 and UCC21220A is between 3 V and 5.5 V. The output bias supply voltage (VDDA/VDDB) range from 9.2 V to 25 V. The lower end of this bias supply range is governed by the internal undervoltage lockout (UVLO) protection feature of each device. One must not let VDD or VCCI fall below their respective UVLO thresholds (for more information on UVLO, see セクション 8.3.1). The upper end of the VDDA/VDDB range depends on the maximum gate voltage of the power device being driven by UCC21220 and UCC21220A. The UCC21220 and UCC21220A have a recommended maximum VDDA/VDDB of 25 V.

A local bypass capacitor should be placed between the VDD and VSS pins. Position this capacitor as close to the device as possible. A low ESR, ceramic surface mount capacitor is recommended. Place two capacitors, including one with a value of ≈10-µF for device biasing, and an additional ≤100-nF capacitor in parallel for high-frequency filtering.

Similarly, place a bypass capacitor between the VCCI and GND pins. Given the small amount of current drawn by the logic circuitry within the input side of UCC21220 and UCC21220A, this bypass capacitor has a minimum recommended value of 100 nF.

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11 Layout

11.1 Layout Guidelines

Consider these PCB layout guidelines for in order to achieve optimum performance for the UCC21220 and UCC21220A.

11.1.1 Component Placement Considerations

- Low-ESR and low-ESL capacitors must be connected close to the device between the VCCI and GND pins and between the VDD and VSS pins to support high peak currents when turning on the external power transistor.
- To avoid large negative transients on the switch node VSSA (HS) pin, the parasitic inductances between the source of the top transistor and the source of the bottom transistor must be minimized.
- It is recommended to bypass using a ≥1-nF low ESR/ESL capacitor, C_{DIS}, close to DIS pin when connecting to a µC with distance

11.1.2 Grounding Considerations

- It is essential to confine the high peak currents that charge and discharge the transistor gates to a minimal physical area. This will decrease the loop inductance and minimize noise on the gate terminals of the transistors. The gate driver must be placed as close as possible to the transistors.
- Pay attention to high current path that includes the bootstrap capacitor, bootstrap diode, local VSSB-referenced bypass capacitor, and the low-side transistor body/anti-parallel diode. The bootstrap capacitor is recharged on a cycle-by-cycle basis through the bootstrap diode by the VDD bypass capacitor. This recharging occurs in a short time interval and involves a high peak current. Minimizing this loop length and area on the circuit board is important for ensuring reliable operation.

11.1.3 High-Voltage Considerations

- To ensure isolation performance between the primary and secondary side, one should avoid placing any PCB traces or copper below the driver device. A PCB cutout is recommended in order to prevent contamination that may compromise the UCC21220 and UCC21220A isolation performance.
- For half-bridge, or high-side/low-side configurations, one should try to increase the clearance distance of the PCB layout between the high and low-side PCB traces.

11.1.4 Thermal Considerations

- A large amount of power may be dissipated by the UCC21220 and UCC21220A if the driving voltage is high, the load is heavy, or the switching frequency is high (refer to セクション 9.2.2.4 for more details). Proper PCB layout can help dissipate heat from the device to the PCB and minimize junction to board thermal impedance (θ_{JB}).
- Increasing the PCB copper connecting to VDDA, VDDB, VSSA and VSSB pins is recommended, with priority on maximizing the connection to VSSA and VSSB (see 図 11-2 and 図 11-3). However, high voltage PCB considerations mentioned above must be maintained.
- If there are multiple layers in the system, it is also recommended to connect the VDDA, VDDB, VSSA and VSSB pins to internal ground or power planes through multiple vias of adequate size. Ensure that no traces or coppers from different high-voltage planes overlap.

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11.2 Layout Example

図 11-1 shows a 2-layer PCB layout example with the signals and key components labeled.

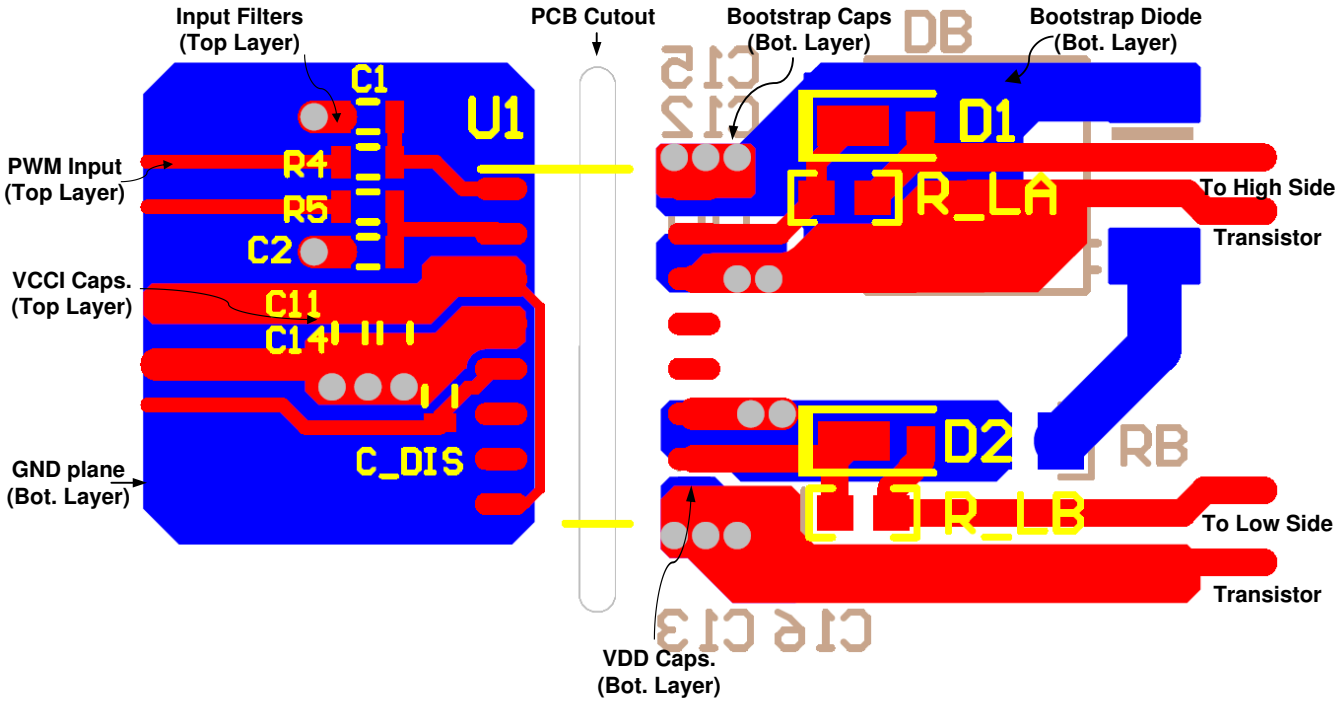

図 11-1. Layout Example

図 11-2 and 図 11-3 shows top and bottom layer traces and copper.

注

There are no PCB traces or copper between the primary and secondary side, which ensures isolation performance.

PCB traces between the high-side and low-side gate drivers in the output stage are increased to maximize the creepage distance for high-voltage operation, which will also minimize cross-talk between the switching node VSSA (SW), where high dv/dt may exist, and the low-side gate drive due to the parasitic capacitance coupling.

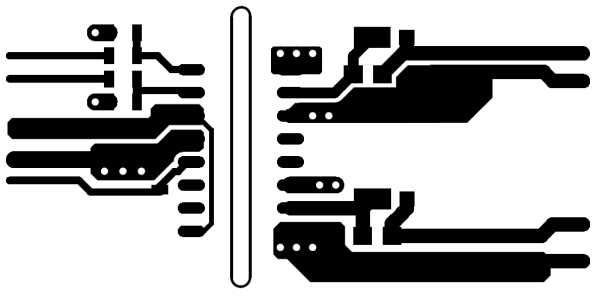

図 11-2. Top Layer Traces and Copper

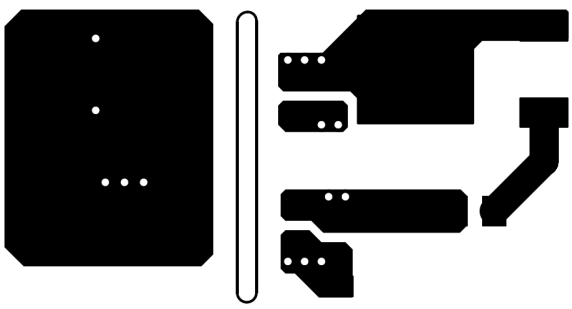

図 11-3. Bottom Layer Traces and Copper

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図 11-4 and 図 11-5 are 3D layout pictures with top view and bottom views.

注

The location of the PCB cutout between the primary side and secondary sides, which ensures isolation performance.

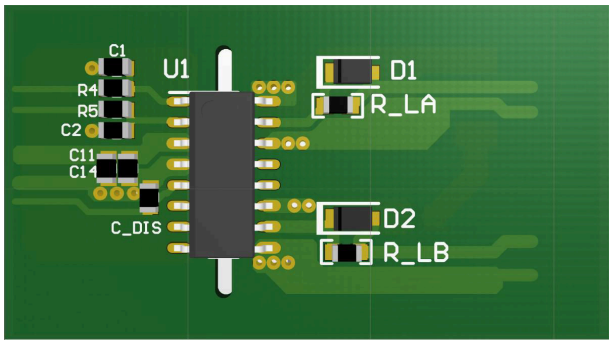

図 11-4. 3-D PCB Top View

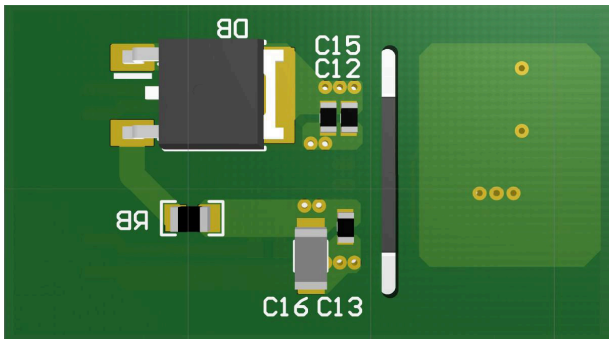

図 11-5. 3-D PCB Bottom View

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12 Device and Documentation Support

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12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- Isolation Glossary

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 サポート・リソース

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12.7 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

13 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision F (February 2024) to Revision G (November 2024)	Page
• 「特長」セクションをデバイスの特性を反映するように更新	1
• CMTI を 100V/ns 超から 125V/ns 超に変更	1
• 最大伝搬遅延を 40ns から標準値 33ns に変更	1
• 最大遅延マッチングの箇条書き項目を削除	1
• 最大パルス幅歪みを 5.5ns から 5ns に変更	1
• 最大 VDD 電源オン遅延を 35µs から 10µs に変更	1
• 最大 VDD 出力駆動電源を 18V から 25V に変更	1
• 動作温度範囲を接合部温度範囲に変更	1

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- 5ns より短い入力パルスを除去するという箇条書き項目を削除 1
- 認定を最新の標準に更新 1
- CMTI を 100V/ns 超から 125V/ns 超に変更 1
- 入力が短い過渡電圧を除去し、入出力が電圧スパイクに耐えるという文を削除 1
- アクティブ プルダウンを 2.1V (最大値) から 2V (最大値) 変更 1
- Changed 5V UVLO recommended VDD supply minimum from 6V to 6.5V 3
- Changed DIS pin description; leaving DIS pin open would disable the device 3
- Changed VDDA-VSSA and VDDB-VSSB absmax from 20V to 30V 4
- Changed all -0.5V minimum to -0.3V to keep consistent with newly released datasheets 4
- Changed all absolute maximum value from supply+0.5V to supply+0.3V to keep consistent with newly released datasheets 4
- Deleted input signal voltage transient spec 4
- Updated ESD spec from HBM = ±4000 and CDM = ±1500 to HBM = ±2000 and CDM = ±1000 to match ESD industry standards 4
- Changed VDDA-VSSA and VDDB-VSSB recommended max from 18V to 25V 4
- Changed 5V-UVLO recommended minimum VDDA/B voltage from 6V to 6.5V 4
- Deleted ambient temperature spec 4
- Changed junction temperature max from 130°C to 150°C 4
- Updated thermal values from RθJA = 68.5°C/W, RθJC(top) = 30.5°C/W, RθJB = 22.8°C/W, ψJT = 17.1°C/W, ψJB = 22.5°C/W to RθJA = 80.2°C/W, RθJC(top) = 36.6°C/W, RθJB = 45°C/W, ψJT = 28°C/W, ψJB = 44.3°C/W 5
- Updated values from PD = 1825mW, PDI = 15mW, PDA/PDB = 905mW to PD = 950mW, PDI = 50mW, PDA/PDB = 450mW. Changed test conditions. 5
- Updated DIN EN IEC to the latest standard, updated insulation voltage values 6
- Updated barrier capacitance value 6
- Deleted safety-related certifications section, certification ongoing 6
- Changed IS testing condition. Changed IS value from 75mA (with VDDA/B=12V) to 50mA (with VDDA/B=15V) and 30mA (with VDDA/B=25V). 7
- Updated safety-limiting values from PS = 15mW/905mW/905mW/1825mW to PS = 50mW/750mW/750mW/1550mW 7
- Updated IVCCI quiescent current spec Typ value from 1.5mA to 1.4mA 8
- Updated IVDDA/IVDDB quiescent current spec Typ from 1.0mA to 1.2mA and Max value from 1.8mA to 2.0mA 8
- Updated IVCCI operating current Typ value from 2.5mA to 2.7mA and added Max value 3.2mA 8
- Updated IVDDA/IVDDB operating current Typ value from 2.5mA to 2.7mA and added Max value 4.4mA. Deleted Cload from test condition. 8
- Updated values from Rising threshold Min = 5.0V, Typ = 5.5V, Max = 5.9V to Min = 5.7V, Typ = 6.0V, Max = 6.3V 8
- Updated values from Falling threshold Min = 4.7V, Typ = 5.2V, Max = 5.6V to Min = 5.4V, Typ = 5.7V, Max = 6.0V 8
- Updated values from Rising threshold Min = 8V, Typ = 8.5V, Max = 9V to Min = 7.7V, Typ = 8.5V, Max = 8.9V 8
- Updated values from Falling threshold Min = 7.5V, Typ = 8V, Max = 8.5V to Min = 7.2V, Typ = 7.9V, Max = 8.4V 8
- Updated 8-V UVLO hysteresis typ = 0.5V to 0.6V 8
- Updated Input high threshold Typ = 1.8V, Max = 2V to Typ = 2V, Max = 2.3V. Deleted Min spec 8
- Deleted Input low threshold voltage Max spec 8
- Updated Input threshold hysteresis Typ = 0.8V to Typ = 1V 8
- Updated peak current test condition to 0.22uF load capacitance. Changed peak output source current direction 8
- Updated output resistance test condition from ±10mA to ±5mA 8
- Deleted output voltage at high/low state specs 8
- Updated active pull-down Typ = 1.75V, Max = 2.1V to Typ = 1.6V, Max = 2V 8

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- Changed output rise time Typ from 5ns to 8ns. Deleted Max value.....9
- Changed output fall time Typ from 6ns to 8ns. Deleted Max value.....9
- Changed minimum pulse width from Typ = 10ns, Max = 20ns to Min = 4ns, Typ = 12ns, Max = 30ns.....9
- Changed propagation delay TPDHL and TPDLH from Typ=28ns, Max = 40ns to Min = 26ns, Typ = 33ns, Max = 45ns.....9
- Changed pulse width distortion max from 5.5ns to 5ns.....9
- Changed propagation delay matching from Max = 5ns to Max = 6.5ns from TJ = -40C to -10C and Max = 5ns from TJ = -10C to 150C.....9
- Changed VCCI power-up delay from Typ = 40us, Max = 59us to Min = 18us, Typ = 42us, Max = 80us.....9
- Deleted VDD power up delay Typ 22us and changed Max from 35us to 10us.....9
- Updated CMTI from Min = 100V/ns to 125V/ns.....9
- Updated thermal curves to match updated characteristics.....10
- Updated typical char plots to show device characteristics 11
- Deleted language on deglitch filter. Changed minimum pulse width from typical 10ns to 12ns.....14
- Updated UVLO delay to match new specs.....15
- Updated functional block diagram to reflect device characteristics.....17
- Changed logic table; leaving DIS pin open disables the driver.....19
- Updated input stage section to match new specs.....19
- Added paragraph on minimum pulse width to Output Stage section.....20
- Updated ESD structure diagram to reflect device characteristics.....20
- Updated device operation mode when DIS is floating. Added recommendation of bypass capacitor.....21
- Changed maximum VDDA/VDDB from 18V to 25V.....33

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Changes from Revision E (May 2019) to Revision F (February 2024)	Page
• Changed CTI and Material Group values in insulation specifications and added table note	6

Changes from Revision D (December 2018) to Revision E (May 2019)	Page
• 「特長」、「アプリケーション」、「概要」セクションを変更	1
• 「機能図」から「代表的なアプリケーション」に変更	1
• Added maximum VCCI Power-up Delay Time: UVLO Rise to OUTA, OUTB	9
• Added maximum VDDA, VDDB Power-up Delay Time: UVLO Rise to OUTA, OUTB	9

Changes from Revision C (August 2018) to Revision D (December 2018)	Page
• UCC21220A のマーケティング ステータスを製品プレビューから初期リリースに変更。	1

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC21220AD	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-40 to 125	21220A
UCC21220ADR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	-	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	21220A
UCC21220ADR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	-	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	21220A
UCC21220DR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	21220
UCC21220DR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	21220

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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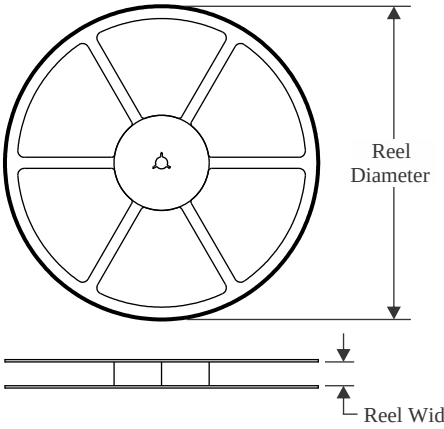
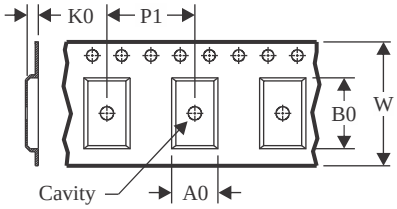
TAPE AND REEL INFORMATION

REEL DIMENSIONS

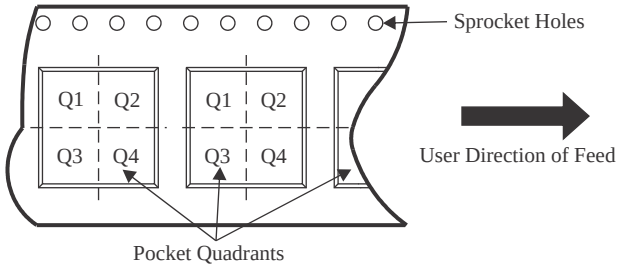


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

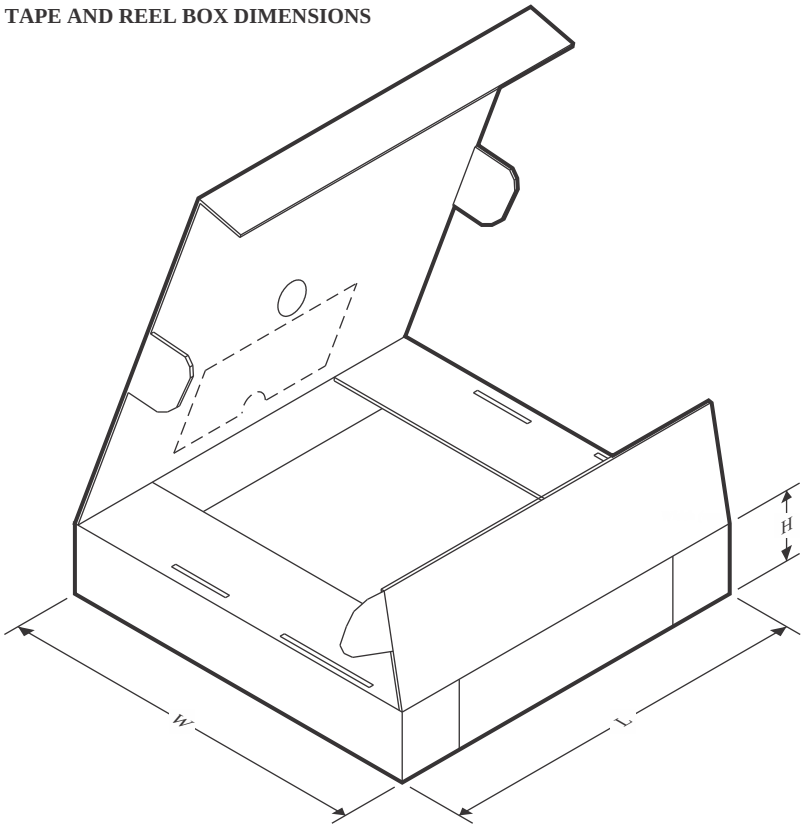
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC21220ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
UCC21220DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

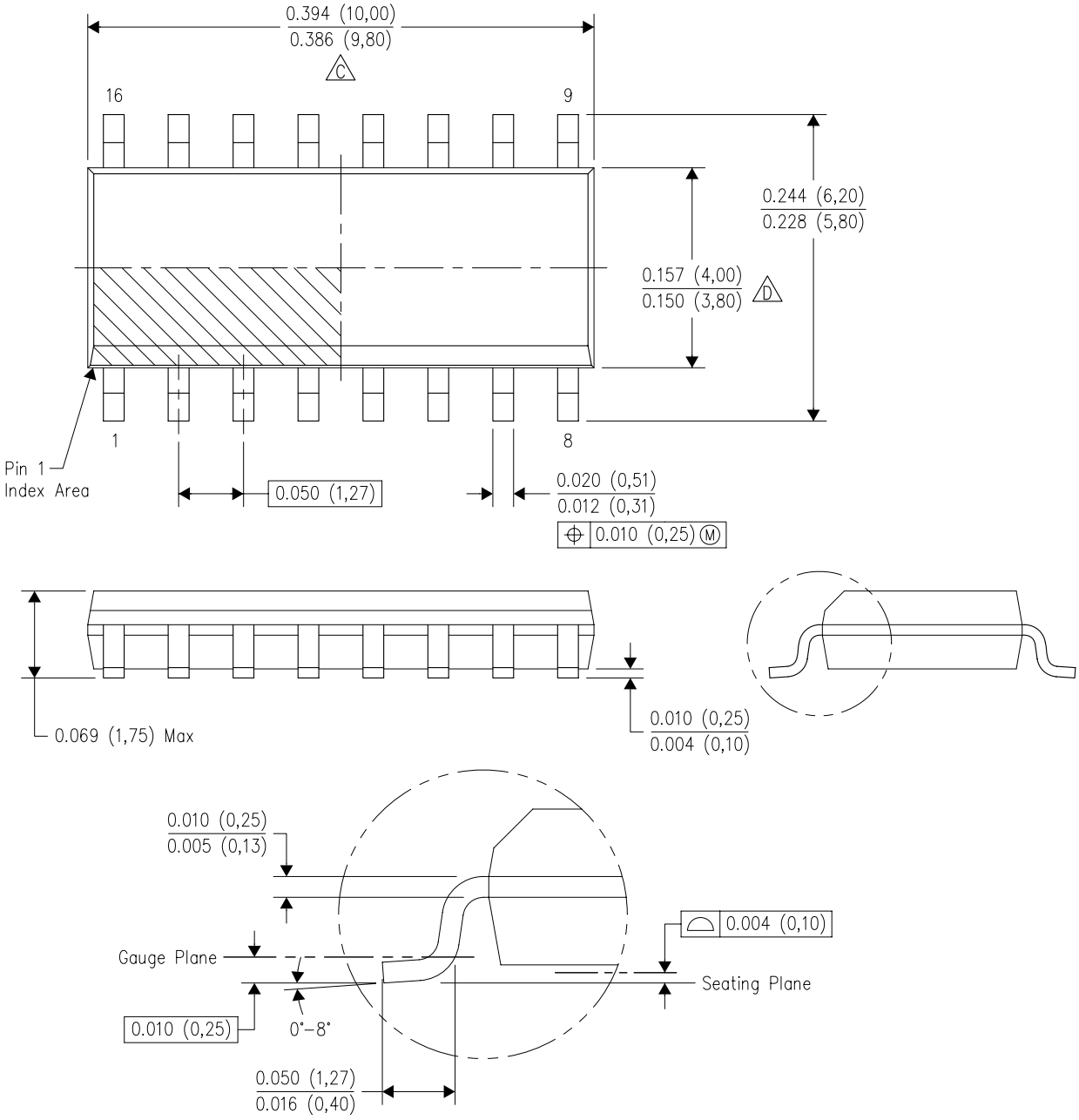
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC21220ADR	SOIC	D	16	2500	350.0	350.0	43.0
UCC21220DR	SOIC	D	16	2500	353.0	353.0	32.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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