

# UCC21231 4A ソース、6A シンク、高速、デュアル チャネル絶縁型ゲートドライバ、薄型 SON パッケージ

## 1 特長

- 汎用:デュアル ローサイド、デュアル ハイサイド、またはハーフブリッジドライバ
- 最大 4A/6A のピークソース/シンク出力
- 基本絶縁定格電圧: 1.6KV<sub>RMS</sub>
- 125V/ns を超える同相過渡耐性 (CMTI)
- スイッチング パラメータ:
  - 伝搬遅延時間: 33ns (代表値)
  - 最大パルス幅歪み: 5ns
  - 最大 VDD 電源オン遅延: 10μs
- 最大 25V VDD 出力駆動電源、5V VDD UVLO 保護付き
- あらゆる電源に対応する UVLO 保護
- 高速なイネーブルによる電源シーケンス
- 1.2mm を超える間隔の 4 × 4mm SON パッケージ:
  - 各チャネルの下にサーマルパッド
  - 14.1°C/W R<sub>θJB</sub>
- 接合部温度範囲: -40~+150°C

## 2 アプリケーション

- サーバー、テレコム、および産業用インフラストラクチャ
- AC/DC および DC/DC 電源
- 無停電電源 (UPS)

## 3 概要

UCC21231 は、デッド タイムをプログラムでき、広い温度範囲に対応する絶縁型デュアル チャネル ゲートドライバファミリです。極端な温度条件下でも安定した性能を提供

し、堅牢性に優れています。ピーク電流はソース 4A、シンク 6A で、パワー MOSFET、GaN トランジスタを駆動するように設計されています。

UCC21231 は、2 つのローサイドドライバ、2 つのハイサイドドライバ、または 1 つのハーフブリッジドライバとして構成可能です。入力側は、1.6kVRMS の絶縁バリアによって 2 つの出力ドライバと分離されており、同相過渡耐性 (CMTI) は 125V/ns 以上です。

保護機能として、抵抗によりプログラム可能なデッドタイム、両方の出力を同時にシャットダウンするイネーブル機能、5ns 未満の入力過渡を除去する内蔵グリッチ除去フィルタ、入力 / 出力ピンでの最大 -2V、最長 200ns のスパイクに対する負電圧耐性があります。すべての電源が UVLO 機能を備えています。

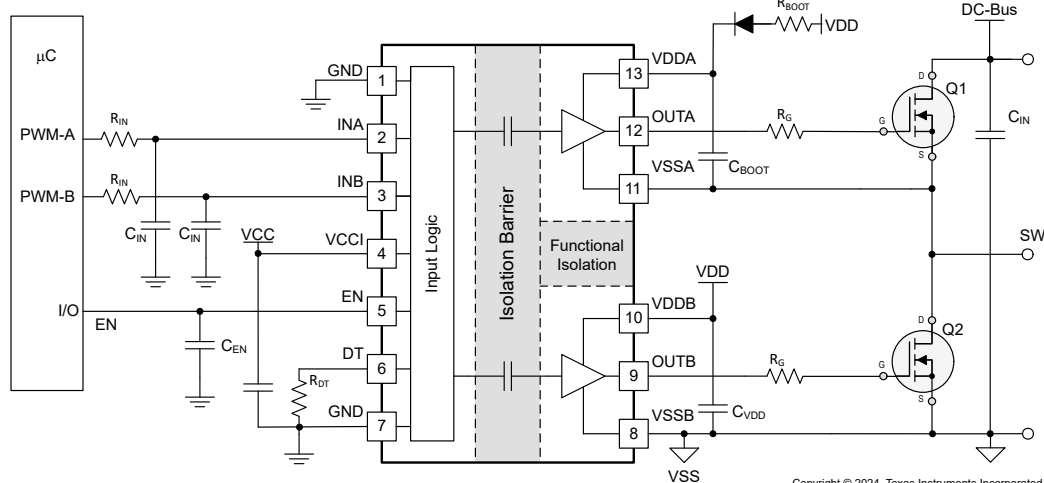
UCC21231 デバイスは、最大 25V の VDD 電源電圧に対応できます。VCCI 入力範囲が 3V~5.5V と広いため、このドライバはデジタルコントローラとの接続に適しています。すべての電源電圧ピンには、低電圧誤動作防止 (UVLO) 機能が搭載されています。

これらの高度な機能により、UCC21231 は広範な電力アプリケーションにおいて高効率、高電力密度、および堅牢性を実現します。

### 製品情報

部品番号	パッケージ (1)	REC.VDD 電源電圧の最小値
UCC21231ADLGR	DLG (WSON 13)	6.7V

(1) 供給されているすべてのパッケージについては、[セクション 13](#) を参照してください。



代表的なアプリケーション回路図



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## 4 Pin Configuration and Functions

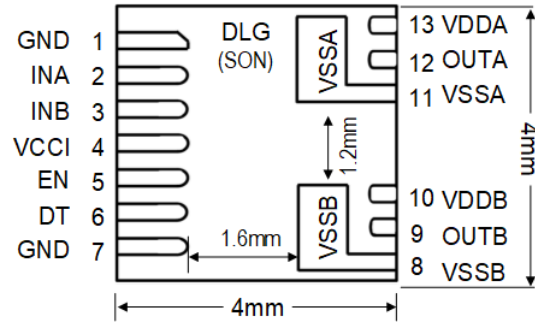


図 4-1. DLG Package 13-Pin SON Top View

表 4-1. Pin Functions

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
INA	2	I	Input signal for A channel. INA input has a TTL/CMOS compatible input threshold. This pin is pulled low internally if left open. It is recommended to use an RC filter on INA, with R = 10 Ω to 100 Ω and C = 10 pF to 100 pF.
INB	3	I	Input signal for B channel. INB input has a TTL/CMOS compatible input threshold. This pin is pulled low internally if left open. It is recommended to use an RC filter on INB, with R = 10 Ω to 100 Ω and C = 10 pF to 100 pF.
VCCI	4	P	Primary-side supply voltage. Locally decoupled to GND using a low ESR/ESL capacitor located as close to the device as possible.
GND	1, 7	G	Primary-side ground reference. All signals in the primary side are referenced to this ground.
EN	5	I	Enable both driver outputs if asserted high, disable the output if set low. It is recommended to tie this pin to VCCI if not used to achieve better noise immunity. This pin is internally pulled low if left floating. It is recommended to use an RC filter on EN, with R = 0 Ω to 100 Ω and C = 100 pF to 1000 pF.
DT	6	I	DT pin configurations: <ul style="list-style-type: none"> <li>DT pin float or short to VCCI disables dead time interlock function</li> <li>Place 1.7-kΩ to 100-kΩ resistor (RDT) between DT and GND to set minimum dead time between driver outputs</li> <li>Place 0-Ω to 150-Ω resistor, or short DT pin to GND to have two outputs interlocked</li> </ul>
VDDA	13	P	Secondary-side power for driver A. Locally decoupled to VSSA using a low ESR/ESL capacitor located as close to the device as possible.
OUTA	12	O	Output of driver A. Connect to the gate of the A channel transistor.
VSSA	11	G	Ground for secondary-side driver A. Ground reference for secondary side A channel.
VDDB	10	P	Secondary-side power for driver B. Locally decoupled to VSSB using low ESR/ESL capacitor located as close to the device as possible.
OUTB	9	O	Output of driver B. Connect to the gate of the B channel transistor.
VSSB	8	G	Ground for secondary-side driver B. Ground reference for secondary side B channel.

(1) P =Power, G= Ground, I= Input, O= Output

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CCI</sub> to GND	Input bias supply voltage	−0.3	6	V
V <sub>DDA</sub> , V <sub>ddb</sub> to V <sub>SS</sub>	Output bias supply voltage	−0.3	30	V
O <sub>UTA</sub> to V <sub>SSA</sub> , O <sub>UTB</sub> to V <sub>SSB</sub>	Output signal DC voltage	−0.3	V <sub>DDA</sub> /B + 0.3	V
	Output signal transient voltage for 200-ns	−2	V <sub>DDA</sub> /B + 0.3	V
INA, INB to GND PWM to GND	Input signal DC voltage	−0.3	V <sub>CCI</sub> + 0.3 <sup>(2)</sup>	V
DT, EN to GND		−0.3	V <sub>CCI</sub> + 0.3 <sup>(2)</sup>	V
Channel to channel isolation voltage	V <sub>SSA</sub> -V <sub>SSB</sub>   in DLG package		700	V
T <sub>J</sub>	Junction temperature	−40	150	°C
T <sub>stg</sub>	Storage temperature	−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Maximum voltage must not exceed 6 V.

### 5.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup>	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>CCI</sub>	Input bias pin supply voltage	3.0		5.5	V
V <sub>DDA</sub> , V <sub>ddb</sub>	UCC21231 - 5V UVLO Output bias supply voltage, V <sub>DDA</sub> -V <sub>SSA</sub> , V <sub>ddb</sub> -V <sub>SSB</sub>	6.5		25	V
T <sub>A</sub>	Ambient temperature	−40		125	°C
T <sub>J</sub>	Junction temperature	−40		150	°C

### 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		UCC21231	UNIT
		DLG	
		13 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	44	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	46.6	°C/W
R <sub>θJC(bottom)</sub>	Junction-to-case (bottom) thermal resistance	19.4	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	14.1	°C/W
Ψ <sub>JT</sub>	Junction-to-top(center) characterization parameter	12.4	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	14	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 5.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$P_D$	Maximum power dissipation (both sides)	$V_{CC1} = 5V$ , $V_{DDA}/V_{ddb} = 20V$ , $I_{NA/B} = 3.3V$ , 460kHz 50% duty cycle square wave, $C_L = 2.2nF$ , $T_A = 25^\circ C$			950	mW
$P_{DI}$	Maximum power dissipation by transmitter side				50	mW
$P_{DA}$ , $P_{DB}$	Maximum power dissipation by each driver side				450	mW

## 5.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
General				
CLR	External clearance <sup>(1)</sup>	Shortest terminal-to-terminal distance through air	>1.6	mm
CPG	External Creepage <sup>(1)</sup>	Shortest terminal-to-terminal distance across the package surface	>1.6	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>17	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 400	V
	Material Group	According to IEC 60664-1	II	
	Overvoltage category	Rated mains voltage ≤ 150 V <sub>RMS</sub>	I-III	
		Rated mains voltage ≤ 300 V <sub>RMS</sub>	I-II	
DIN EN IEC 60747-17 (VDE 0884-17) <sup>(2)</sup>				
V <sub>IORM</sub>	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	453	V <sub>PK</sub>
V <sub>IOWM</sub>	Maximum isolation working voltage	AC voltage (sine wave); time-dependent dielectric breakdown (TDDb) test	320	V <sub>RMS</sub>
		DC voltage	453	V <sub>DC</sub>
V <sub>IOTM</sub>	Maximum transient isolation voltage	V <sub>TEST</sub> = V <sub>IOTM</sub> , t = 60 s (qualification) V <sub>TEST</sub> = 1.2 × V <sub>IOTM</sub> , t = 1 s (100% production)	2263	V <sub>PK</sub>
V <sub>IMP</sub>	Maximum impulse voltage <sup>(3)</sup>	Tested in air, 1.2/50-μs waveform per IEC 62368-1	2667	V <sub>PK</sub>
V <sub>IOSM</sub>	Maximum surge isolation voltage <sup>(3)</sup>	V <sub>IOSM</sub> ≥ 1.3 × V <sub>IMP</sub> ; Tested in oil (qualification test); 1.2/50-μs waveform per IEC 62368-1	3500	V <sub>PK</sub>
q <sub>pd</sub>	Apparent charge <sup>(4)</sup>	Method a: After I/O safety test subgroup 2/3; V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 60 s; V <sub>pd(m)</sub> = 1.2 × V <sub>IORM</sub> , t <sub>m</sub> = 10 s	≤5	pC
		Method a: After environmental tests subgroup 1, V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 60 s; V <sub>pd(m)</sub> = 1.3 × V <sub>IORM</sub> , t <sub>m</sub> = 10 s	≤5	
		Method b: At routine test (100% production) and preconditioning (type test), V <sub>ini</sub> = 1.2 × V <sub>IOTM</sub> , t <sub>ini</sub> = 1 s; V <sub>pd(m)</sub> = 1.5 × V <sub>IORM</sub> , t <sub>m</sub> = 1 s (method b1) or V <sub>pd(m)</sub> = V <sub>ini</sub> , t <sub>m</sub> = t <sub>ini</sub> (method b2)	≤5	
C <sub>IO</sub>	Barrier capacitance, input to output <sup>(5)</sup>	V <sub>IO</sub> = 0.4 × sin (2πft), f = 1 MHz	~1.2	pF
R <sub>IO</sub>	Insulation resistance, input to output <sup>(6)</sup>	V <sub>IO</sub> = 500 V, T <sub>A</sub> = 25°C	>10 <sup>12</sup>	Ω
		V <sub>IO</sub> = 500 V, 100°C ≤ T <sub>A</sub> ≤ 125°C	>10 <sup>11</sup>	
		V <sub>IO</sub> = 500 V at T <sub>S</sub> = 150°C	>10 <sup>9</sup>	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V <sub>ISO</sub>	Withstand isolation voltage for UCC2155x	V <sub>TEST</sub> = V <sub>ISO</sub> , t = 60 s (qualification), V <sub>TEST</sub> = 1.2 × V <sub>ISO</sub> , t = 1 s (100% production)	1600	V <sub>RMS</sub>

- (1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed-circuit board are used to help increase these specifications.
- (2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Testing is carried out in air to determine the surge immunity of the package
- (4) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier
- (5) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (6) All pins on each side of the barrier tied together creating a two-pin device.

## 5.7 Safety Limiting Values

PARAMETER		TEST CONDITIONS	SIDE	MIN	TYP	MAX	UNIT
I <sub>S</sub>	Safety input, output, or supply current	R <sub>qJA</sub> = 44°C/W, V <sub>DD</sub> - V <sub>SS</sub> = 15 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C	DRIVER A, DRIVER B			90	mA
		R <sub>qJA</sub> = 44°C/W, V <sub>DD</sub> - V <sub>SS</sub> = 25 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C				55	
P <sub>S</sub>	Safety input, output, or total power	R <sub>qJA</sub> = 44°C/W, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C	INPUT			50	mW
			DRIVER A			1375	mW
			DRIVER B			1375	mW
			TOTAL			2800	mW
T <sub>S</sub>	Maximum safety temperature <sup>(1)</sup>					150	°C

- (1) The maximum safety temperature, T<sub>S</sub>, has the same value as the maximum junction temperature, T<sub>J</sub>, specified for the device. The I<sub>S</sub> and P<sub>S</sub> parameters represent the safety current and safety power respectively. The maximum limits of I<sub>S</sub> and P<sub>S</sub> should not be exceeded. These limits vary with the ambient temperature, T<sub>A</sub>.  
The junction-to-air thermal resistance, R<sub>qJA</sub>, in the *Thermal Information* table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:  
T<sub>J</sub> = T<sub>A</sub> + R<sub>qJA</sub> × P, where P is the power dissipated in the device.  
T<sub>J(max)</sub> = T<sub>S</sub> = T<sub>A</sub> + R<sub>qJA</sub> × P<sub>S</sub>, where T<sub>J(max)</sub> is the maximum allowed junction temperature.  
P<sub>S</sub> = I<sub>S</sub> × V<sub>I</sub>, where V<sub>I</sub> is the maximum supply voltage.

## 5.8 Electrical Characteristics

$V_{VCCI} = 3.3\text{ V}$  or  $5.0\text{ V}$ ,  $0.1\text{-}\mu\text{F}$  capacitance from  $V_{CCI}$  to GND,  $V_{VDDx} = 12\text{ V}$ ,  $1.1\text{-}\mu\text{F}$  capacitance from  $V_{DDA}$  and  $V_{ddb}$  to  $V_{SSA}$  and  $V_{SSB}$ , DT pin floating, EN = VCC or DIS = GND,  $T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ,  $C_L = 0\text{ pF}$ , unless otherwise noted <sup>(1)</sup>

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENTS						
I <sub>VCC</sub>	VCC quiescent current	V <sub>INx</sub> = 0 V, EN = VCC; VCC=3.3V		1.4	2	mA
		V <sub>INx</sub> = 0 V, EN = VCC; VCC=5V		1.4	2	
		V <sub>INx</sub> = VCC, EN = VCC; VCC=3.3V		4.2	4.8	
		V <sub>INx</sub> = VCC, EN = VCC; VCC=5V		4.2	4.8	
		V <sub>INx</sub> PWM at 0V to VCC at f <sub>SW</sub> = 500kHz, EN = VCC; VCC=3.3V		2.7	3.2	
		V <sub>INx</sub> PWM at 0V to VCC at f <sub>SW</sub> = 500kHz, EN = VCC; VCC=5V		2.7	3.2	
I <sub>VDDx</sub>	VDDx quiescent current	V <sub>INx</sub> = 0 V, EN = VCC;		1.2	2	mA
		V <sub>INx</sub> = 0 V, EN = VCC; VDD=25V		1.4	2.3	
		V <sub>INx</sub> = VCC, EN = VCC;		1.4	2.2	
		V <sub>INx</sub> = VCC, EN = VCC; VDD=25V		1.5	2.5	
		V <sub>INx</sub> PWM at 0V to VCC at f <sub>SW</sub> = 500kHz, EN = VCC;		2.7	4.4	
		V <sub>INx</sub> PWM at 0V to VCC at f <sub>SW</sub> = 500kHz, EN = VCC; VDD=25V		2.7	4.4	
VCC SUPPLY VOLTAGE UNDERVOLTAGE THRESHOLDS						
V <sub>VCC_ON</sub>	VCC UVLO Rising Threshold		2.55	2.7	2.85	V
V <sub>VCC_OFF</sub>	VCC UVLO Falling Threshold		2.35	2.5	2.65	
V <sub>VCC_HYS</sub>	VCC UVLO Threshold Hysteresis			0.2		
t <sub>VCC+ to OUT</sub>	VCC UVLO ON Delay		18	42	80	μs
t <sub>VCC- to OUT</sub>	VCC UVLO OFF Delay		0.5	1.2	7	
t <sub>VCCFIL</sub>	VCC UVLO Deglitch Filter		0.4	0.9	3.1	
VDD SUPPLY VOLTAGE UNDERVOLTAGE THRESHOLDS AND DELAY						
V <sub>VDD_ON</sub>	VDDx UVLO Rising Threshold	5-V UVLO	5.7	6.0	6.3	V
V <sub>VDD_OFF</sub>	VDDx UVLO Falling Threshold		5.4	5.7	6.0	
V <sub>VDD_HYS</sub>	VDDx UVLO Threshold Hysteresis			0.30		
t <sub>VDD+ to OUT</sub>	VDDx UVLO ON Delay				10	μs
t <sub>VDD- to OUT</sub>	VDDx UVLO OFF Delay		0.1	0.5	2	
t <sub>VDDFIL</sub>	VDDx UVLO Deglitch Filter		0.1	0.17		
INA, INB, AND EN						
V <sub>INxH</sub> , V <sub>ENH</sub>	Input High Threshold Voltage			2	2.3	V
V <sub>INxL</sub> , V <sub>ENL</sub>	Input Low Threshold Voltage		0.8	1		
V <sub>INx_HYS</sub> , V <sub>EN_HYS</sub>	Input Threshold Hysteresis			1		
R <sub>INxD</sub>	INx Pin Pull Down Resistance	INx = 3.3V	50	90	185	kΩ
R <sub>ENU</sub>	EN Pin Pull Down Resistance	DIS = 3.3V	50	90	185	kΩ
OUTPUT DRIVER STAGE						
I <sub>O+</sub>	Peak Output Source Current	C <sub>VDDx</sub> = 10 μF, C <sub>L</sub> = 0.22 μF, f = 1 kHz		−4		A
I <sub>O−</sub>	Peak Output Sink Current	C <sub>VDDx</sub> = 10 μF, C <sub>L</sub> = 0.22 μF, f = 1 kHz		6		A
R <sub>OH</sub>	Pull up resistance	I <sub>OUTx</sub> = −0.05A		5		Ω
R <sub>OL</sub>	Pull down resistance	I <sub>OUTx</sub> = 0.05A		0.55		
ACTIVE PULL-DOWN						
V <sub>OUTPD</sub>	Output Active Pull Down on OUTx	I <sub>OUT</sub> = 200mA, VDDx floating and unpowered.		1.6	2	V
V <sub>OUTPD</sub>	Output Active Pull Down on OUTx	I <sub>OUT</sub> = 200mA, C <sub>VDD</sub> =100nF and unpowered.		1.6	2	V
DEADTIME AND OVERLAP PROGRAMMING						



## 5.8 Electrical Characteristics (続き)

$V_{VCCI} = 3.3\text{ V}$  or  $5.0\text{ V}$ ,  $0.1\text{-}\mu\text{F}$  capacitance from  $V_{CCI}$  to GND,  $V_{VDDX} = 12\text{ V}$ ,  $1.1\text{-}\mu\text{F}$  capacitance from  $V_{DDA}$  and  $V_{VDD}$  to  $V_{SSA}$  and  $V_{SSB}$ , DT pin floating, EN = VCC or DIS = GND,  $T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ,  $C_L = 0\text{ pF}$ , unless otherwise noted <sup>(1)</sup>

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DT <sub>S</sub>	Disable DT Function	DT pin open or pull DT pin to VCC	Output overlapping determined by INA, INB			-
	Deadtime Programming for $R_{DT} \leq 0.15\text{ k}\Omega$	$R_{DT} = 0\text{--}0.15\text{ k}\Omega$	-6	0.2	6	ns
	Deadtime Programming for $1.7\text{ k}\Omega \leq R_{DT} \leq 100\text{ k}\Omega$ DT (ns) = $8.6 \times R_{DT}(\text{k}\Omega) + 13$	$R_{DT} = 10\text{ k}\Omega$	86	99	112	ns
		$R_{DT} = 20\text{ k}\Omega$	167	185	203	
		$R_{DT} = 50\text{ k}\Omega$	399	443	487	

(1) Current direction in the testing conditions are defined to be positive into the pin and negative out of the specified terminal (unless otherwise noted)

## 5.9 Switching Characteristics

$V_{VCCI} = 3.3\text{ V}$  or  $5.0\text{ V}$ ,  $0.1\text{-}\mu\text{F}$  capacitance from  $V_{CCI}$  to GND,  $V_{VDDX} = 12\text{ V}$ ,  $1.1\text{-}\mu\text{F}$  capacitance from  $V_{DDA}$  and  $V_{VDD}$  to  $V_{SSA}$  and  $V_{SSB}$ , DT pin floating, EN = VCC or DIS = GND,  $T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ,  $C_L = 0\text{ pF}$ , unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>RISE</sub>	Output Rise Time	C <sub>L</sub> =1.8nF, VDDx=12V, 20% to 80%	8			ns
		C <sub>L</sub> =1.8nF, VDDx=25V, 20% to 80%	8			
t <sub>FALL</sub>	Output Fall Time	C <sub>L</sub> =1.8nF, VDDx=12V, 10% to 90%	8			ns
		C <sub>L</sub> =1.8nF, VDDx=25V, 10% to 90%	8			
t <sub>PDLH</sub>	Propagation Delay – Low to High	Input Pulse Width = 100ns, 500kHz, measure with Input VIH to output 10%	26	33	45	ns
t <sub>PDHL</sub>	Propagation Delay – High to Low	Input Pulse Width = 100ns, 500kHz, measure with Input VIL to output 90%	26	33	45	ns
t <sub>PD_EN_HL</sub>	EN Response Delay – High to Low	t <sub>EN/DIS_FIL</sub> = 20 ns (typ), VDD=VDD_ON+0.2V and above, Input Pulse Width = 100ns, 500kHz	27	48	80	ns
t <sub>PD_EN_LH</sub>	EN Response Delay – Low to High		27	48	80	ns
t <sub>PWmin</sub>	Minimum Input Pulse Width That Passes to Output	VDD=VDD_ON+0.2V and above	4	12	30	ns
t <sub>DM</sub>	Propagation Delay Matching for Dual Channel Driver	Input Pulse Width = 100ns, 500kHz, T <sub>J</sub> = -40°C to -10°C;  t <sub>PDLHA</sub> – t <sub>PDLHB</sub>  ,  t <sub>PDHLA</sub> – t <sub>PDHLB</sub>	0		6.5	ns
		Input Pulse Width = 100ns, 500kHz, T <sub>J</sub> = -10°C to +150°C;  t <sub>PDLHA</sub> – t <sub>PDLHB</sub>  ,  t <sub>PDHLA</sub> – t <sub>PDHLB</sub>	0		5	ns
t <sub>PWD</sub>	Pulse Width Distortion	Input Pulse Width = 100ns, 500kHz  t <sub>PDLHA</sub> – t <sub>PDHLA</sub>  ,  t <sub>PDLHB</sub> – t <sub>PDHLB</sub>	0		5	ns
CM <sub>H</sub>	High-level Common Mode Transient Immunity	V <sub>CM</sub> = 1500V	125			V/ns
CM <sub>L</sub>	Low-level Common Mode Transient Immunity		125			V/ns

## 5.10 Insulation Characteristics Curves

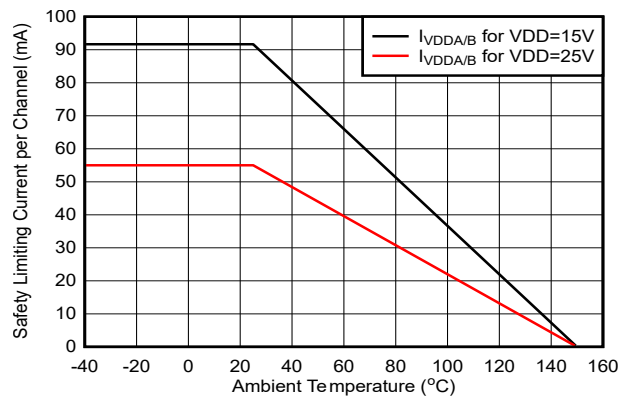


図 5-1. Thermal Derating Curve for Safety Limiting Current (current in each channel with both channels running simultaneously)

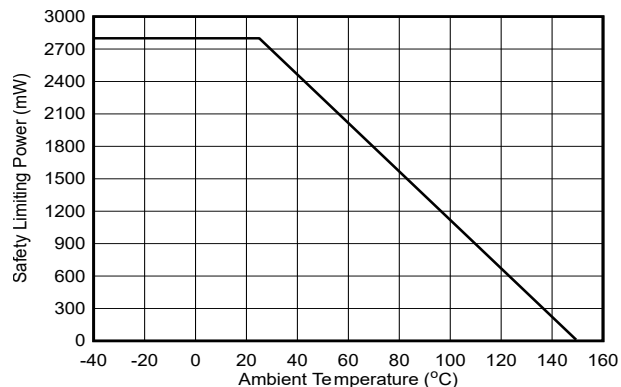


図 5-2. Thermal Derating Curve for Safety Limiting Power

## 5.11 Typical Characteristics

VDDA = VDD = 15 V, VCCI = 3.3 V, T<sub>A</sub> = 25°C, No load unless otherwise noted.

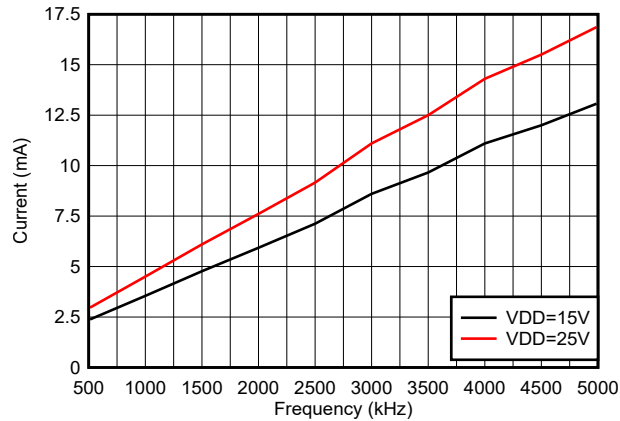


Figure 5-3. Per Channel Current Consumption ( $I_{VDDA/B}$ ) vs Frequency (no load, VDD = 15V or 25V)

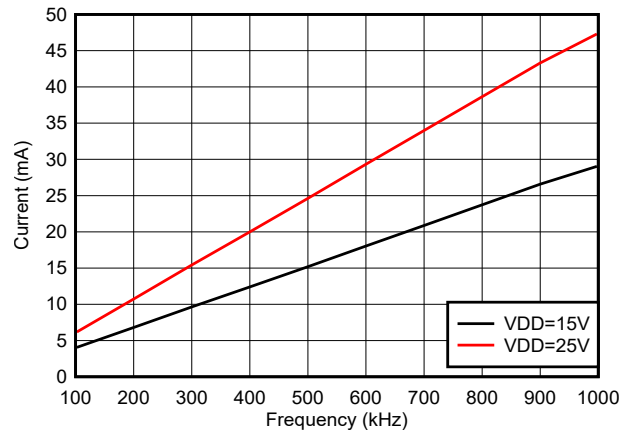


Figure 5-4. Per Channel Current Consumption ( $I_{VDDA/B}$ ) vs Frequency (1-nF load, VDD = 15V or 25V)

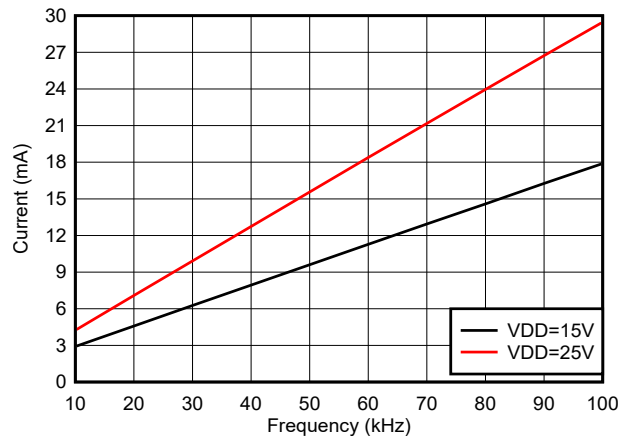


Figure 5-5. Per Channel Current Consumption ( $I_{VDDA/B}$ ) vs Frequency (10-nF load, VDD = 15V or 25V)

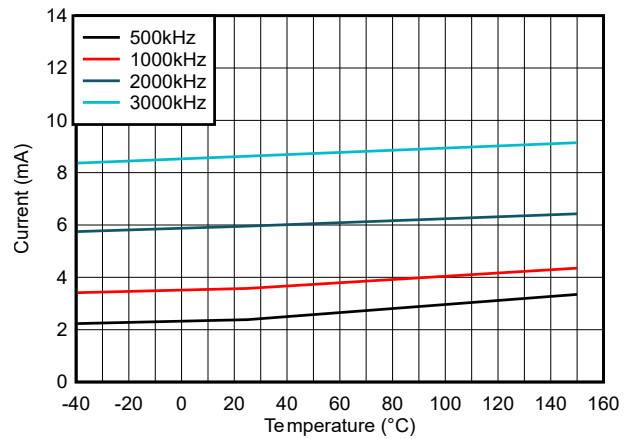


Figure 5-6. Per Channel ( $I_{VDDA/B}$ ) Supply Current vs Temperature (no load, different switching frequencies)

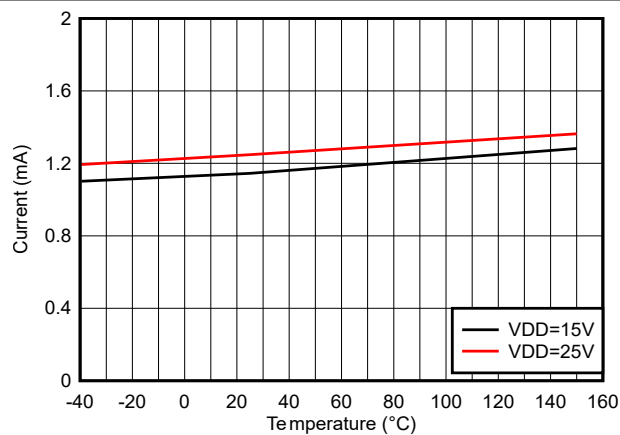


Figure 5-7. Per Channel ( $I_{VDDA/B}$ ) Quiescent Supply Current vs Temperature (no load, input low, no switching)

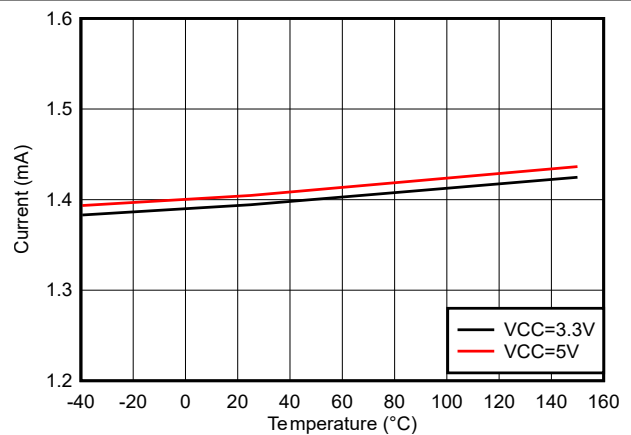


Figure 5-8.  $I_{VCCI}$  Quiescent Supply Current vs Temperature (no load, input low, no switching)

## 5.11 Typical Characteristics (continued)

VDDA = VDDB = 15 V, VCCI = 3.3 V,  $T_A = 25^\circ\text{C}$ , No load unless otherwise noted.

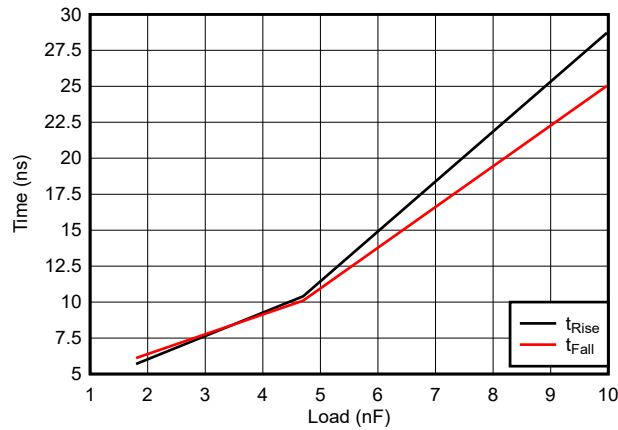


Figure 5-9. Rising and Falling Times vs Load (VDD = 15V)

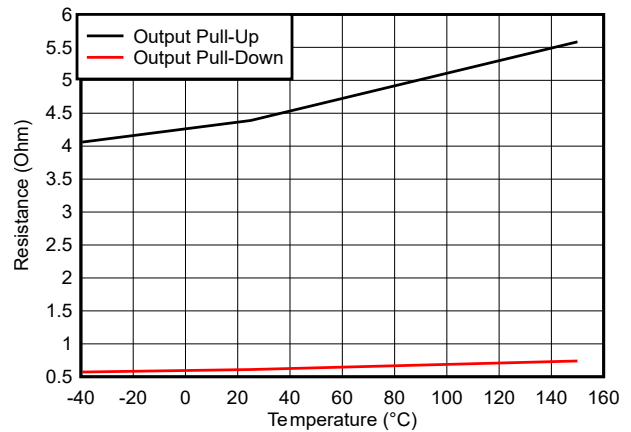


Figure 5-10. Output Resistance vs Temperature

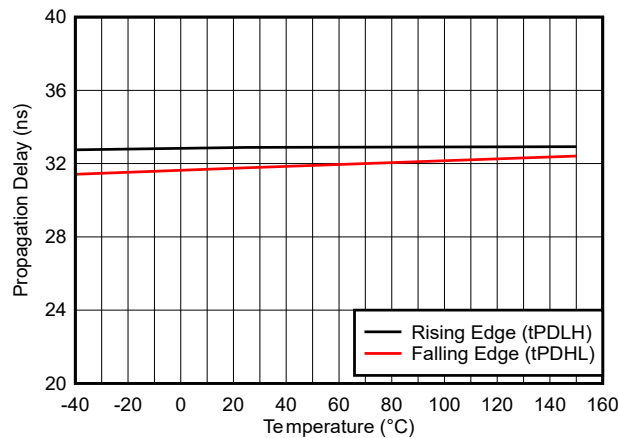


Figure 5-11. Propagation Delay vs Temperature

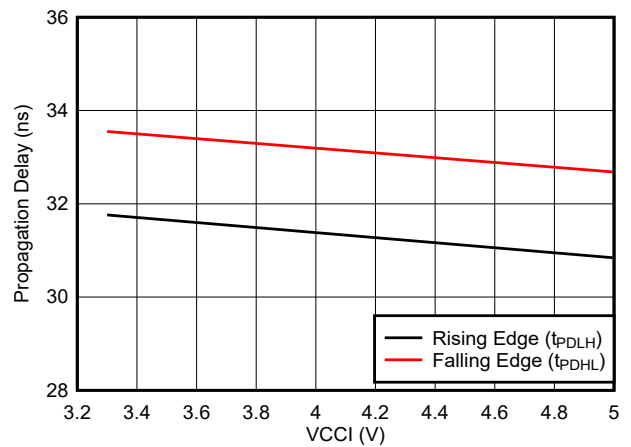


Figure 5-12. Propagation Delay vs VCCI

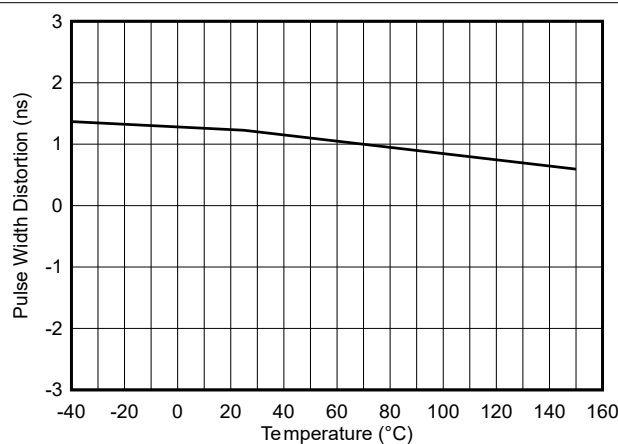


Figure 5-13. Pulse Width Distortion vs Temperature

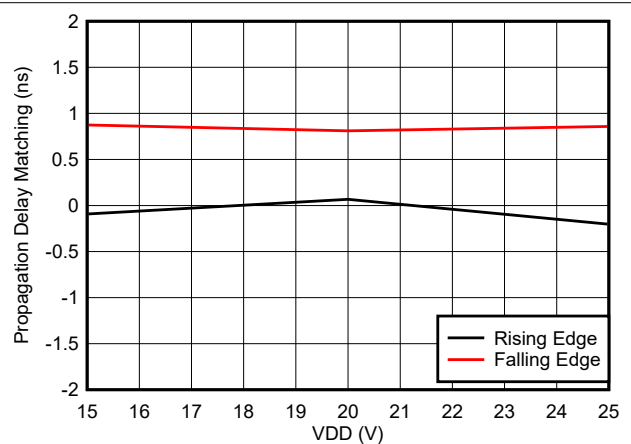


Figure 5-14. Propagation Delay Matching ( $t_{\text{DM}}$ ) vs VDD

## 5.11 Typical Characteristics (continued)

VDDA = VDDDB = 15 V, VCCI = 3.3 V, T<sub>A</sub> = 25°C, No load unless otherwise noted.

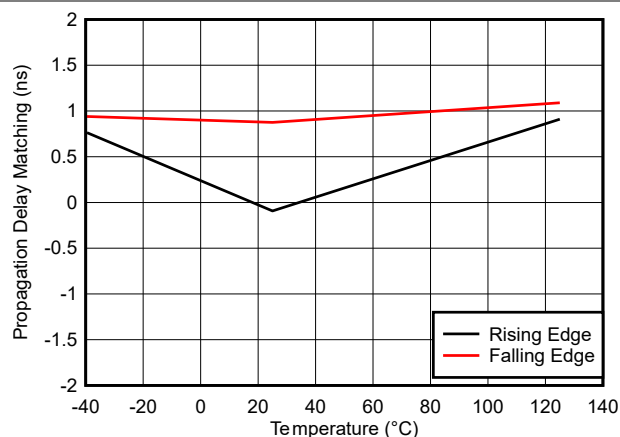


図 5-15. Propagation Delay Matching (t<sub>DM</sub>) vs Temperature

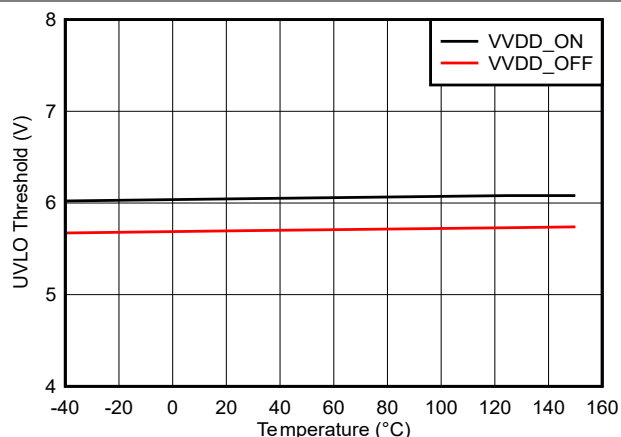


図 5-16. VDD 5-V UVLO Threshold vs Temperature

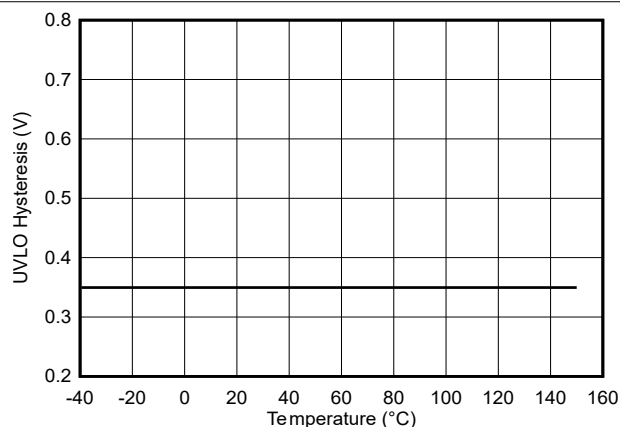


図 5-17. VDD 5-V UVLO Hysteresis vs Temperature

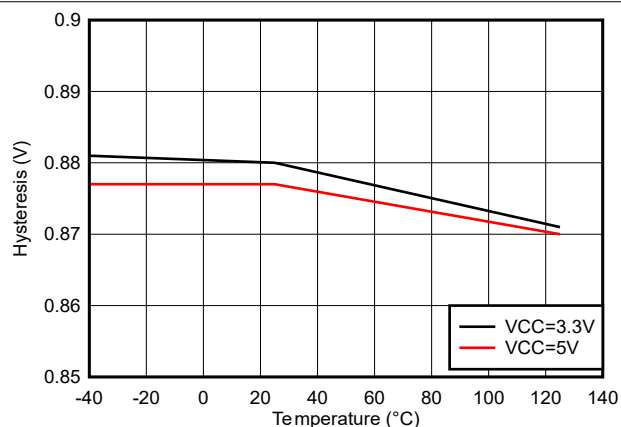


図 5-18. IN/EN Hysteresis vs Temperature

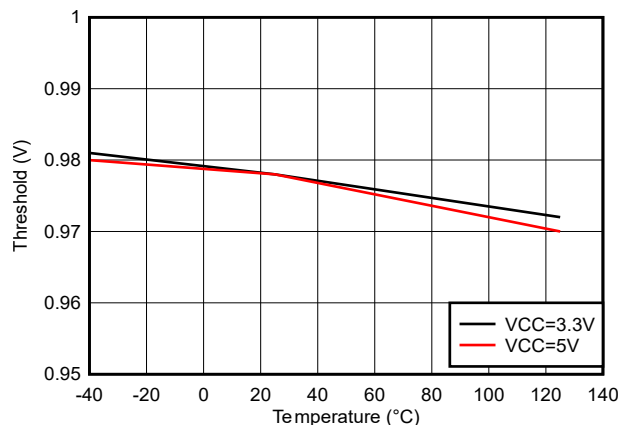


図 5-19. IN/EN Low Threshold

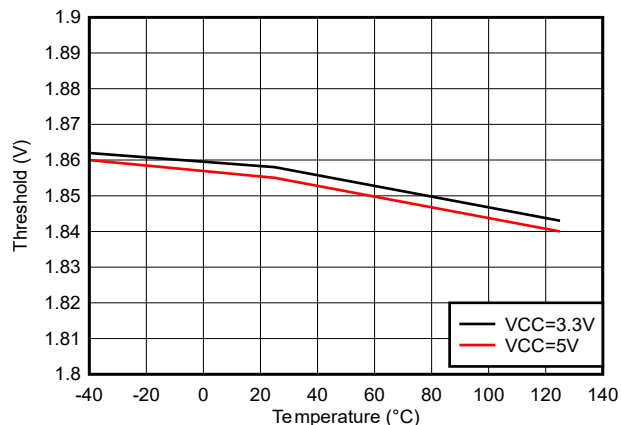


図 5-20. IN/EN High Threshold

## 5.11 Typical Characteristics (continued)

VDDA = VDDb = 15 V, VCCI = 3.3 V,  $T_A = 25^\circ\text{C}$ , No load unless otherwise noted.

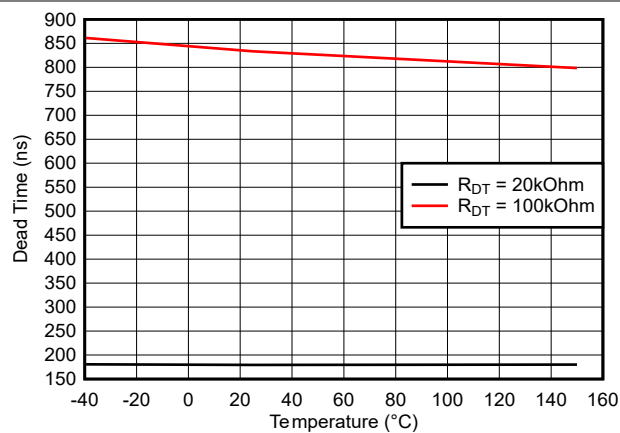


Figure 5-21. Dead Time vs Temperature (with  $R_{DT} = 20\text{k}\Omega$  and  $100\text{k}\Omega$ )

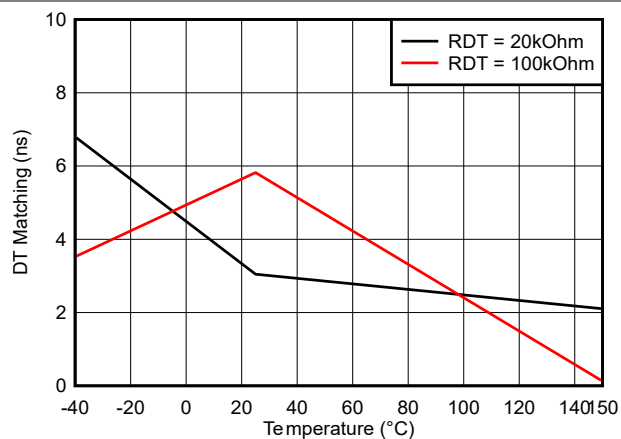


Figure 5-22. Dead Time Matching vs Temperature (with  $R_{DT} = 20\text{k}\Omega$  and  $100\text{k}\Omega$ )

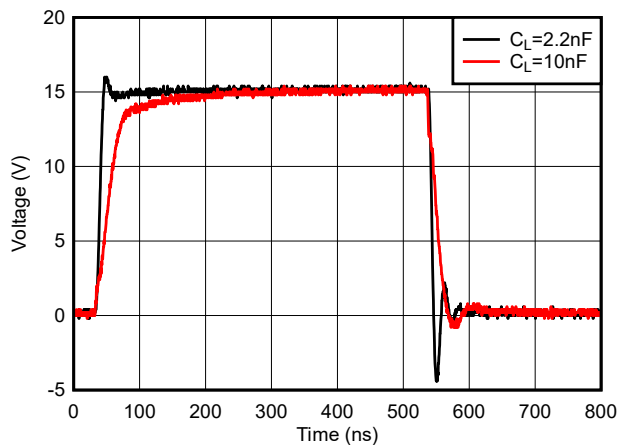


Figure 5-23. Typical Output Waveforms

## 6 Parameter Measurement Information

### 6.1 Propagation Delay and Pulse Width Distortion

Figure 6-1 shows how one calculates pulse width distortion ( $t_{PWD}$ ) and delay matching ( $t_{DM}$ ) from the propagation delays of channels A and B. It can be measured by ensuring that both inputs are in phase and disabling the dead time function by shorting the DT Pin to VCC.

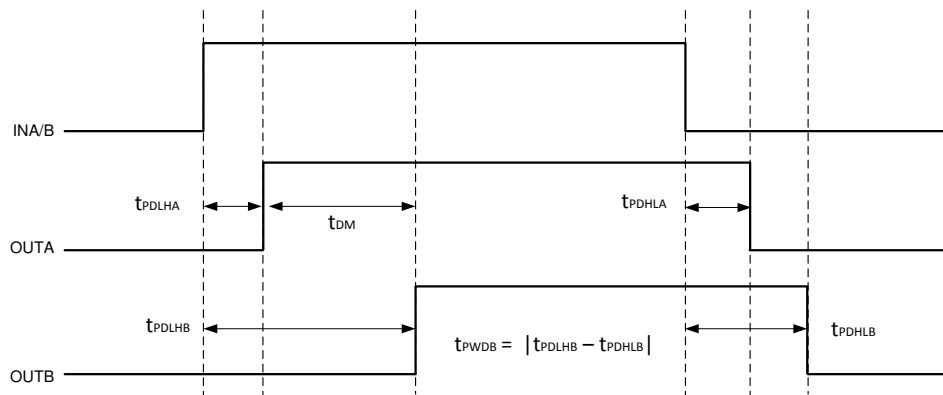


Figure 6-1. Overlapping Inputs, Dead Time Disabled

### 6.2 Rising and Falling Time

Figure 6-2 shows the criteria for measuring rising ( $t_{RISE}$ ) and falling ( $t_{FALL}$ ) times. For more information on how short rising and falling times are achieved see [セクション 7.3.4](#).

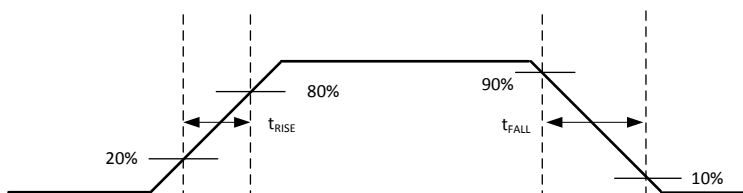


Figure 6-2. Rising and Falling Time Criteria

### 6.3 Input and Enable Response Time

Figure 6-3 shows the response time of the enable function. It is recommended to bypass using a  $\approx 1\text{nF}$  low ESR/ESL capacitor close to EN pin when connecting EN pin to a micro controller with distance. For more information, see [セクション 7.4.1](#).

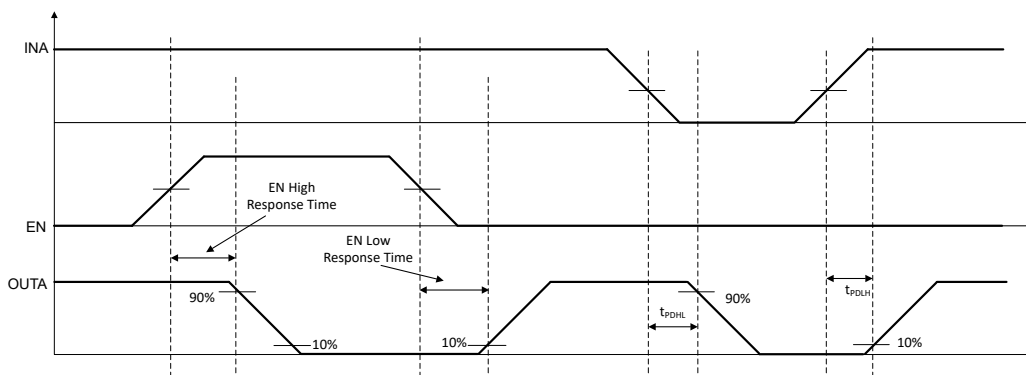


Figure 6-3. Enable Pin Timing

## 6.4 Programmable Dead Time

Leaving the DT pin open or tying it to GND through an appropriate resistor ( $R_{DT}$ ) sets a dead-time interval. For more details on dead time, refer to [セクション 7.4.2](#).

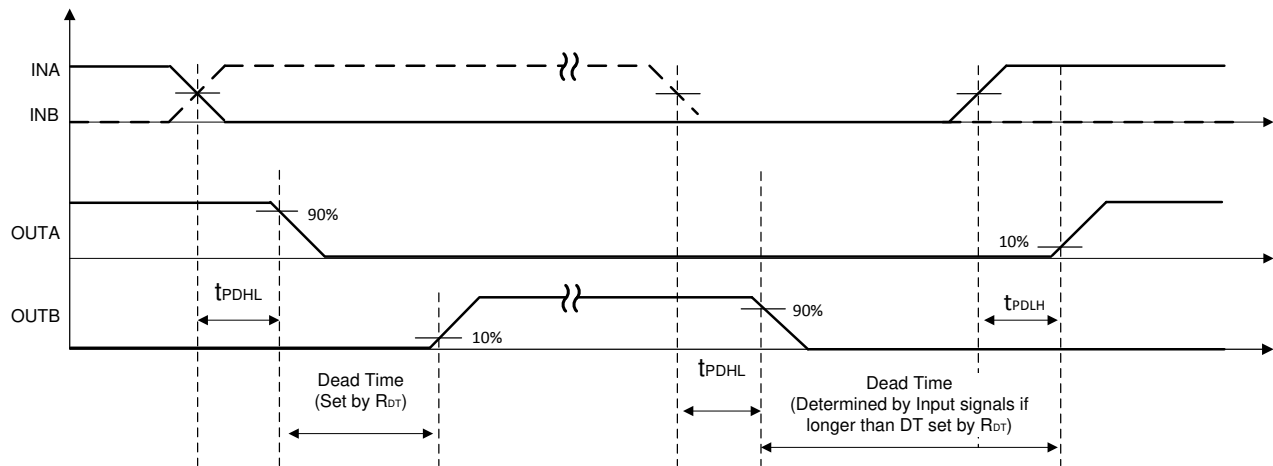


図 6-4. Dead-Time Switching Parameters

## 6.5 Power-up UVLO Delay to OUTPUT

Before the driver is ready to deliver a proper output state, there is a power-up delay from the UVLO rising edge to output and it is defined as  $t_{V_{CCI+} \text{ to } OUT}$  for VCCI UVLO (typically 40us) and  $t_{V_{DD+} \text{ to } OUT}$  for VDD UVLO (typically 5us). It is recommended to consider proper margin before launching PWM signal after the driver's VCCI and VDD bias supply is ready. 図 6-5 and 図 6-6 show the power-up UVLO delay timing diagram for VCCI and VDD.

If INA or INB are active before VCCI or VDD have crossed above their respective on thresholds, the output will not update until  $t_{V_{CCI+} \text{ to } OUT}$  or  $t_{V_{DD+} \text{ to } OUT}$  after VCCI or VDD crossing its UVLO rising threshold. However, when either VCCI or VDD receive a voltage less than their respective off thresholds, there is  $<2\mu s$  delay, depending on the voltage slew rate on the supply pins, before the outputs are held low. This asymmetric delay is designed to ensure safe operation during VCCI or VDD brownouts.

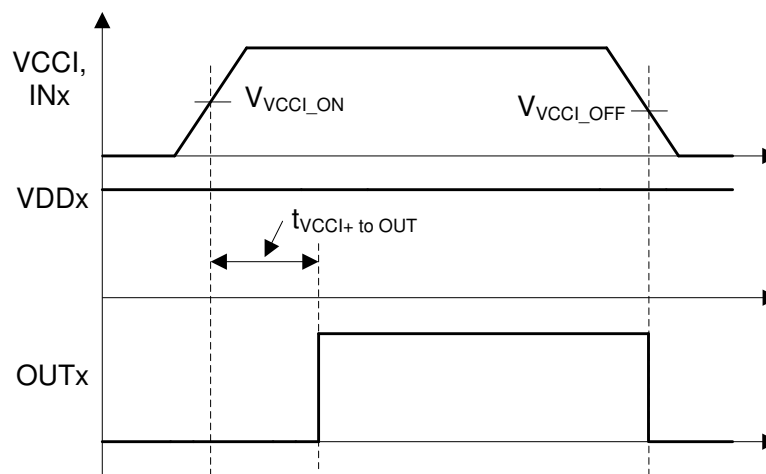


図 6-5. VCCI Power-up UVLO Delay



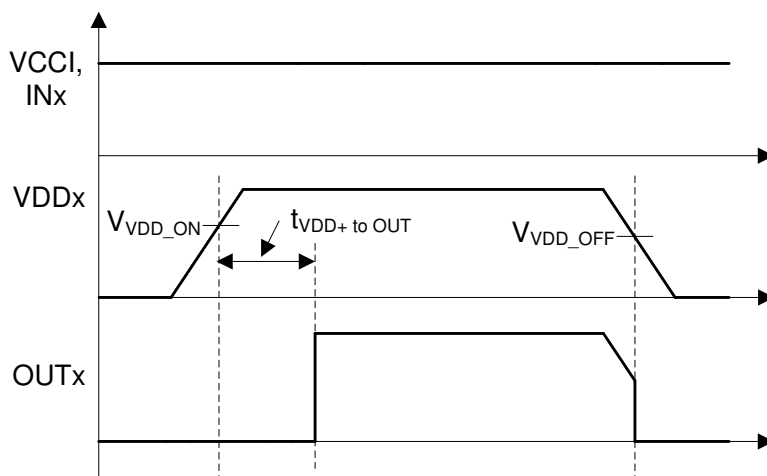


図 6-6. VDDA/B Power-up UVLO Delay

## 6.6 CMTI Testing

Figure 6-7 is a simplified diagram of the CMTI testing configuration.

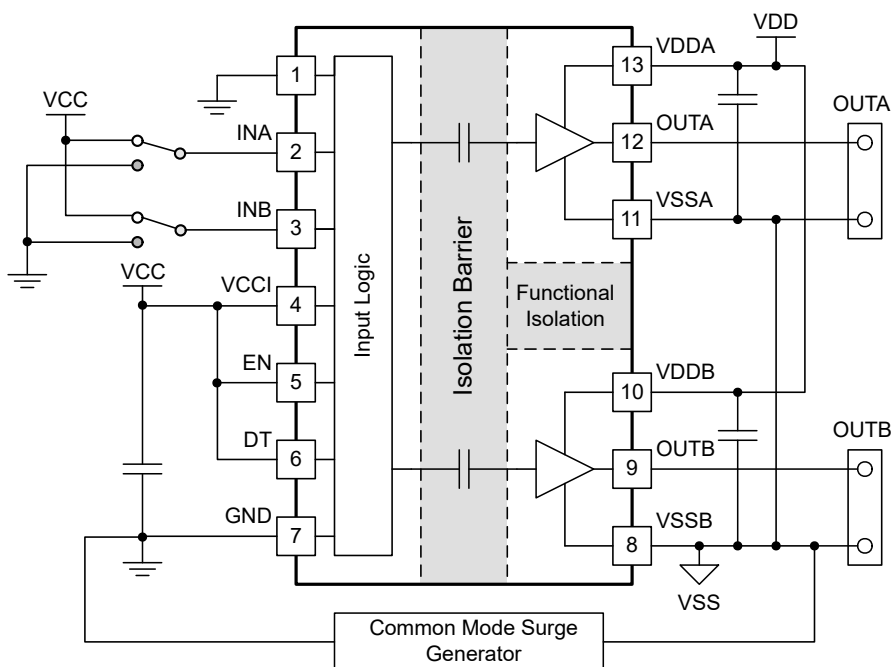


Figure 6-7. Simplified CMTI Testing Setup

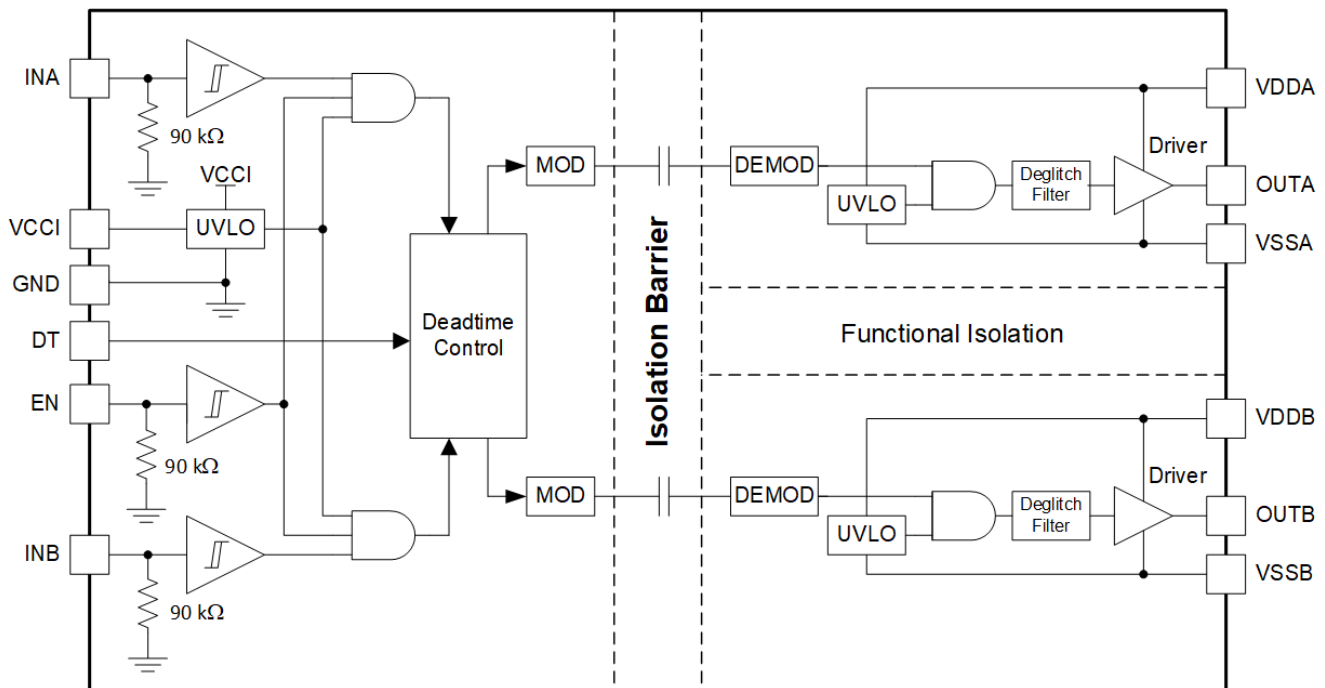
## 7 Detailed Description

### 7.1 Overview

In order to switch power transistors rapidly and reduce switching power losses, high-current gate drivers are often placed between the output of control devices and the gates of power transistors. There are several instances where controllers are not capable of delivering sufficient current to drive the gates of power transistors. This is especially the case with digital controllers, since the input signal from the digital controller is often a 3.3-V logic signal capable of only delivering a few mA.

The UCC21231 is a flexible dual gate driver which can be configured to fit a variety of power supply and motor drive topologies, as well as drive several types of transistors, including SiC MOSFETs. The device has many features that allow it to integrate well with control circuitry and protect the gates it drives such as: resistor-programmable dead time (DT) control, a EN pin, and under voltage lock out (UVLO) for both input and output voltages. The UCC21231 also hold its outputs low when the inputs are left open or when the input pulse is not wide enough. The driver inputs are CMOS and TTL compatible for interfacing to digital and analog power controllers alike. Each channel is controlled by its respective input pins (INA and INB), allowing full and independent control of each of the outputs.

### 7.2 Functional Block Diagram

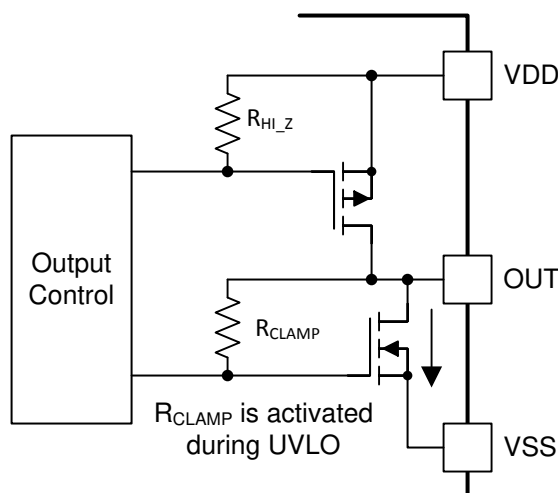


## 7.3 Feature Description

### 7.3.1 VDD, VCCI, and Undervoltage Lock Out (UVLO)

The UCC21231 has an internal undervoltage lock out (UVLO) protection feature on the supply circuit blocks between the VDD and VSS pins for both outputs. When the VDD bias voltage is lower than  $V_{VDD\_ON}$  at device start-up or lower than  $V_{VDD\_OFF}$  after start-up, the VDD UVLO feature holds the effected output low, regardless of the status of the input pins (INA and INB).

When the output stages of the driver are in an unbiased or UVLO condition, the driver outputs are held low by an active clamp circuit that limits the voltage rise on the driver outputs (Illustrated in [Figure 7-1](#)). In this condition, the upper PMOS is resistively held off by  $R_{HI\_Z}$  while the lower NMOS gate is tied to the driver output through  $R_{CLAMP}$ . In this configuration, the output is effectively clamped to the threshold voltage of the lower NMOS device, typically around 1.5 V, when no bias power is available.



**Figure 7-1. Simplified Representation of Active Pulldown Feature**

The VDD UVLO protection has a hysteresis feature ( $V_{VDD\_HYS}$ ). This hysteresis prevents chatter when there is ground noise from the power supply. Also this allows the device to accept small drops in bias voltage, which is bound to happen when the device starts switching and operating current consumption increases suddenly.

The input side of the UCC21231 also has an internal undervoltage lock out (UVLO) protection feature. The device isn't active unless the voltage, VCCI, is going to exceed  $V_{VCCI\_ON}$  on start up. And a signal will cease to be delivered when that pin receives a voltage less than  $V_{VCCI\_OFF}$ . And, just like the UVLO for VDD, there is hysteresis ( $V_{VCCI\_HYS}$ ) to ensure stable operation.

All versions of the UCC21231 can withstand an absolute maximum of 30 V for VDD, and 5.5 V for VCCI.

**表 7-1. UCC21231 VCCI UVLO Feature Logic**

CONDITION	INPUTS		OUTPUTS	
	INA	INB	OUTA	OUTB
VCCI-GND < V <sub>VCCI_ON</sub> during device start up	H	L	L	L
VCCI-GND < V <sub>VCCI_ON</sub> during device start up	L	H	L	L
VCCI-GND < V <sub>VCCI_ON</sub> during device start up	H	H	L	L
VCCI-GND < V <sub>VCCI_ON</sub> during device start up	L	L	L	L
VCCI-GND < V <sub>VCCI_OFF</sub> after device start up	H	L	L	L
VCCI-GND < V <sub>VCCI_OFF</sub> after device start up	L	H	L	L
VCCI-GND < V <sub>VCCI_OFF</sub> after device start up	H	H	L	L
VCCI-GND < V <sub>VCCI_OFF</sub> after device start up	L	L	L	L

**表 7-2. UCC21231 VDD UVLO Feature Logic**

CONDITION	INPUTS		OUTPUTS	
	INA	INB	OUTA	OUTB
VDD-VSS < V <sub>VDD_ON</sub> during device start up	H	L	L	L
VDD-VSS < V <sub>VDD_ON</sub> during device start up	L	H	L	L
VDD-VSS < V <sub>VDD_ON</sub> during device start up	H	H	L	L
VDD-VSS < V <sub>VDD_ON</sub> during device start up	L	L	L	L
VDD-VSS < V <sub>VDD_OFF</sub> after device start up	H	L	L	L
VDD-VSS < V <sub>VDD_OFF</sub> after device start up	L	H	L	L
VDD-VSS < V <sub>VDD_OFF</sub> after device start up	H	H	L	L
VDD-VSS < V <sub>VDD_OFF</sub> after device start up	L	L	L	L

### 7.3.2 Input and Output Logic Table

**表 7-3. INPUT/OUTPUT Logic Table <sup>(1)</sup>**

Assume VCCI, VDDA, VDDDB are powered up. See [セクション 7.3.1](#) for more information on UVLO operation modes.

INPUTS		EN	OUTPUTS		NOTE
INA	INB		OUTA	OUTB	
L	L	H	L	L	If Dead Time function is used, output transitions occur after the dead time expires. See <a href="#">セクション 7.4.2</a>
L	H	H	L	H	
H	L	H	H	L	
H	H	H	L	L	
H	H	H	H	H	DT pin left open or tied to VCCI
Left Open	Left Open	H	L	L	-
X	X	Low or Left Open	L	L	-

(1) "X" means L, H or left open.

### 7.3.3 Input Stage

The input pins (INA, INB, and EN) of the UCC21231 are based on a TTL and CMOS compatible input-threshold logic that is totally isolated from the VDD supply voltage. The input pins are easy to drive with logic-level control signals (such as those from 3.3-V micro-controllers), since the UCC21231 has typical high threshold (V<sub>INAH</sub>) of 2.0 V and a typical low threshold of 1 V. A wide hysteresis (V<sub>INAHYS</sub>) of 1 V makes for good noise immunity and stable operation. If any of the inputs are ever left open, internal pull-down resistors force the pin low. These

resistors are typically 90 k $\Omega$  (see [セクション 7.2](#)). However, it is still recommended to ground an input if it is not being used.

Since the input side of the UCC21231 is isolated from the output drivers, the input signal amplitude can be larger or smaller than VDD, provided that it doesn't exceed the recommended limit. This allows greater flexibility when integrating with control signal sources, and allows the user to choose the most efficient VDD for their chosen gate. That said, the amplitude of any signal applied to INA or INB must *never* be at a voltage higher than VCCI.

### 7.3.4 Output Stage

The UCC21231 output stages feature a pull-up structure which delivers the highest peak-source current when it is most needed, during the Miller plateau region of the power-switch turn on transition (when the power switch drain or collector voltage experiences dV/dt). The output stage pull-up structure features a P-channel MOSFET and an additional *Pull-Up* N-channel MOSFET in parallel. The function of the N-channel MOSFET is to provide a brief boost in the peak-sourcing current, enabling fast turn on. This is accomplished by briefly turning on the N-channel MOSFET during a narrow instant when the output is changing states from low to high.

The  $R_{OH}$  parameter is a DC measurement and it is representative of the on-resistance of the P-channel device only. This is because the *Pull-Up* N-channel device is held in the off state in DC condition and is turned on only for a brief instant when the output is changing states from low to high. Therefore the effective resistance of the UCC21231 pull-up stage during this brief turn-on phase is much lower than what is represented by the  $R_{OH}$  parameter. Therefore, the value of  $R_{OH}$  belies the fast nature of the UCC21231 turn-on time.

The pull-down structure in the UCC21231 is simply composed of an N-channel MOSFET. The  $R_{OL}$  parameter, which is also a DC measurement, is representative of the impedance of the pull-down state in the device. Both outputs of the UCC21231 are capable of delivering 4-A peak source and 6-A peak sink current pulses. The output voltage swings between VDD and VSS provides rail-to-rail operation, thanks to the MOS-out stage which delivers very low drop-out.

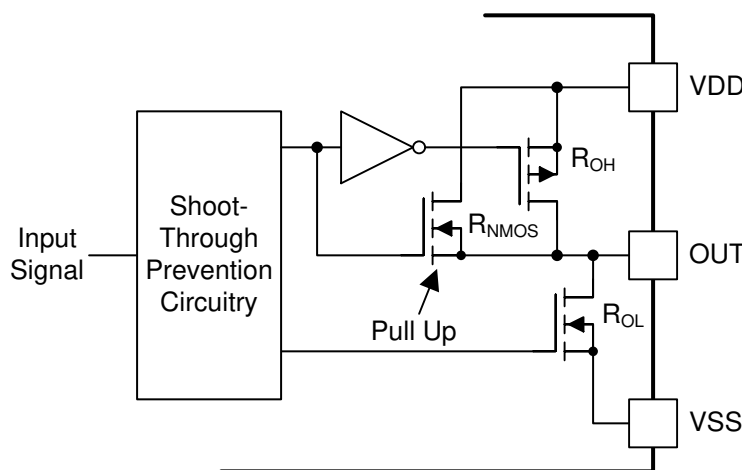


図 7-2. Output Stage

### 7.3.5 Diode Structure in the UCC21231

図 7-3 illustrates the multiple diodes involved in the ESD protection components of the UCC21231. This provides a pictorial representation of the absolute maximum rating for the device.

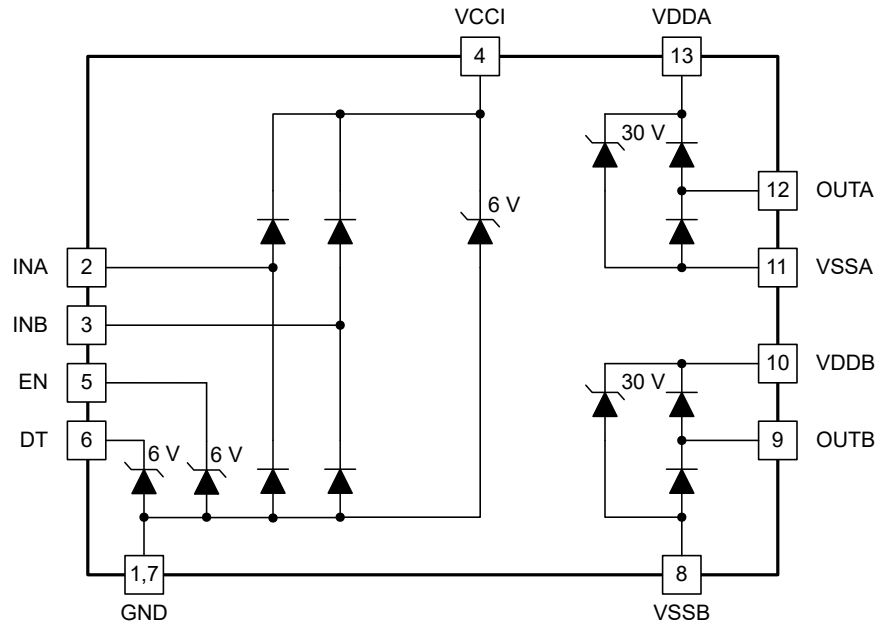


図 7-3. ESD Structure

## 7.4 Device Functional Modes

### 7.4.1 Enable Pin

Setting the EN pin low (or left open) shuts down both outputs simultaneously. Pull the EN pin high allows the UCC21231 to operate normally. The EN response time is in the range of 48 ns and quite responsive, which is as fast as propagation delay. The EN pin is only functional (and necessary) when VCCI stays above the UVLO threshold. It is recommended to tie this pin to VCCI if the EN pin is not used to achieve better noise immunity, and it is recommended to bypass using a  $\approx 1$ -nF low ESR/ESL capacitor close to EN pin when connecting EN pin to a micro controller with distance.

### 7.4.2 Programmable Dead-Time (DT) Pin

The UCC21231 allows the user to adjust dead time (DT) in the following ways:

#### 7.4.2.1 Tying the DT Pin to VCC

Outputs completely match inputs, so no dead time is asserted. This allows outputs to overlap.

#### 7.4.2.2 DT Pin Connected to a Programming Resistor between DT and GND Pins

One can program  $t_{DT}$  by placing a resistor,  $R_{DT}$ , between the DT pin and GND. The appropriate  $R_{DT}$  value can be determined from TBD, where  $R_{DT}$  is in k $\Omega$  and  $t_{DT}$  is in ns:

$$t_{DT} \approx 8.6 \times R_{DT} + 13 \quad (1)$$

DT pin current will be less than 10uA when  $R_{DT}=100\text{k}\Omega$ . It is not recommended to leave the DT pin floating.

An input signal's falling edge activates the programmed dead time for the other signal. The output signals' dead time is always set to the longer of either the driver's programmed dead time or the input signal's own dead time. If both inputs are high simultaneously, both outputs will immediately be set low. This feature is used to prevent

shoot-through, and it doesn't affect the programmed dead time setting for normal operation. Various driver dead time logic operating conditions are illustrated and explained in [セクション 7.3.2](#):

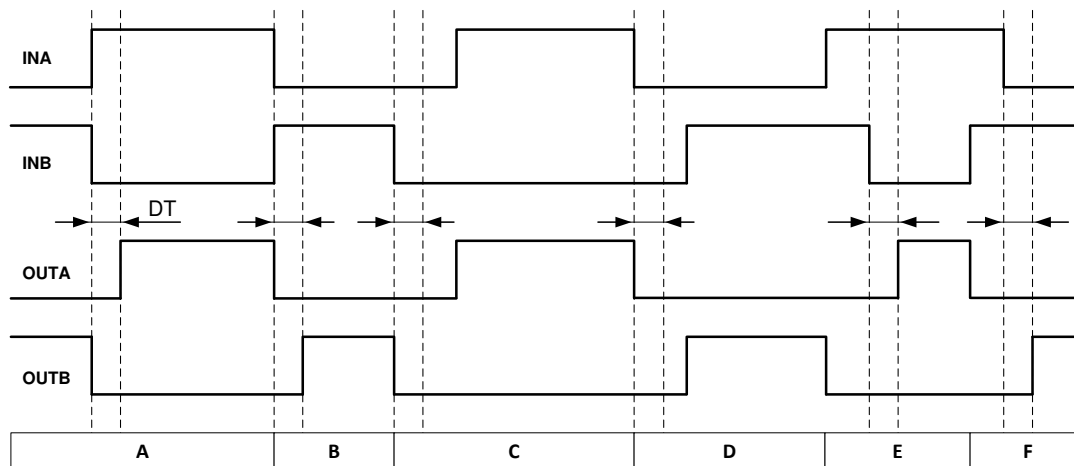


図 7-4. Input and Output Logic Relationship With Input Signals

**Condition A:** INB goes low, INA goes high. INB sets OUTB low immediately and assigns the programmed dead time to OUTA. OUTA is allowed to go high after the programmed dead time.

**Condition B:** INB goes high, INA goes low. Now INA sets OUTA low immediately and assigns the programmed dead time to OUTB. OUTB is allowed to go high after the programmed dead time.

**Condition C:** INB goes low, INA is still low. INB sets OUTB low immediately and assigns the programmed dead time for OUTA. In this case, the input signal's *own* dead time is longer than the programmed dead time. Thus, when INA goes high, it immediately sets OUTA high.

**Condition D:** INA goes low, INB is still low. INA sets OUTA low immediately and assigns the programmed dead time to OUTB. INB's *own* dead time is longer than the programmed dead time. Thus, when INB goes high, it immediately sets OUTB high.

**Condition E:** INA goes high, while INB and OUTB are still high. To avoid overshoot, INA immediately pulls OUTB low and keeps OUTA low. After some time OUTB goes low and assigns the programmed dead time to OUTA. OUTB is already low. After the programmed dead time, OUTA is allowed to go high.

**Condition F:** INB goes high, while INA and OUTA are still high. To avoid overshoot, INB immediately pulls OUTA low and keeps OUTB low. After some time OUTA goes low and assigns the programmed dead time to OUTB. OUTA is already low. After the programmed dead time, OUTB is allowed to go high.



## 8 Application and Implementation

### 注

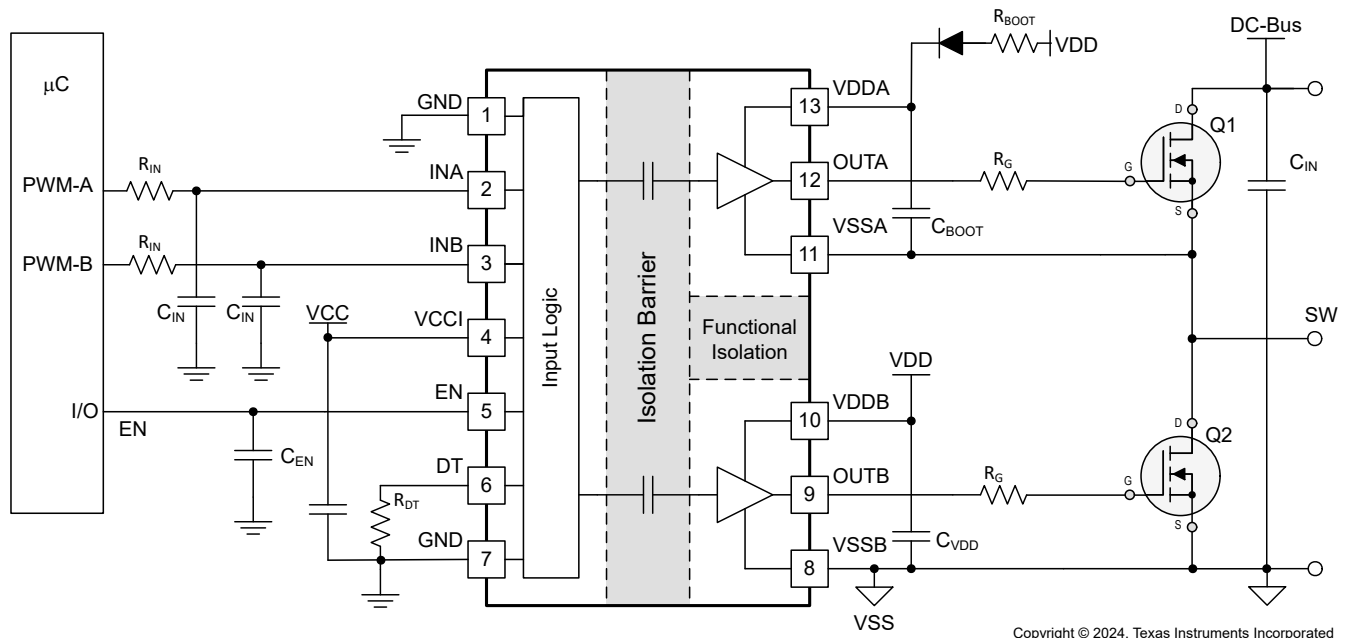
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### 8.1 Application Information

The UCC21231 effectively combines both isolation and buffer-drive functions. The flexible, universal capability of the UCC21231 (with up to 5.5-V VCCI and 25-V VDDA/Vddb) allows the device to be used as a low-side, high-side, high-side/low-side or half-bridge driver for MOSFETs, IGBTs or SiC MOSFETs. With integrated components, advanced protection features (UVLO, dead time, and enable) and optimized switching performance; the UCC21231 enables designers to build smaller, more robust designs for enterprise, telecom, automotive, and industrial applications with a faster time to market.

### 8.2 Typical Application

The circuit in [Figure 8-1](#) shows a reference design with the UCC21231 driving a typical half-bridge configuration which could be used in several popular power converter topologies such as synchronous buck, synchronous boost, half-bridge/full bridge isolated topologies, and 3-phase motor drive applications.



**Figure 8-1. Typical Application Schematic**

### 8.2.1 Design Requirements

UCC21231 is ideal to drive 100-V to 200-V MOSFETs in 48-V system design. 表 8-1 lists reference design parameters for the example application: UCC21231 driving 100-V MOSFETs in a high side-low side configuration.

**表 8-1. UCC21231 Design Requirements**

PARAMETER	VALUE	UNITS
Power transistor	CSD19535KTT	-
VCC	3.3	V
VDD	10	V
Input signal amplitude	3.3	V
Switching frequency ( $f_s$ )	200	kHz
DC link voltage	48	V

### 8.2.2 Detailed Design Procedure

#### 8.2.2.1 Designing INA/INB Input Filter

It is recommended that users avoid shaping the signals to the gate driver in an attempt to slow down (or delay) the signal at the output. However, a small input  $R_{IN}$ - $C_{IN}$  filter can be used to filter out the ringing introduced by non-ideal layout or long PCB traces.

Such a filter should use an  $R_{IN}$  in the range of 0  $\Omega$  to 100  $\Omega$  and a  $C_{IN}$  between 10 pF and 100 pF. In the example, an  $R_{IN} = 51 \Omega$  and a  $C_{IN} = 33$  pF are selected, with a corner frequency of approximately 100 MHz.

When selecting these components, it is important to pay attention to the trade-off between good noise immunity and propagation delay.

#### 8.2.2.2 Select External Bootstrap Diode and its Series Resistor

The bootstrap capacitor is charged by VDD through an external bootstrap diode every cycle when the low side transistor turns on. Charging the capacitor involves high-peak currents, and therefore transient power dissipation in the bootstrap diode may be significant. Conduction loss also depends on the diode's forward voltage drop. Both the diode conduction losses and reverse recovery losses contribute to the total losses in the gate driver circuit.

When selecting external bootstrap diodes, it is recommended that one chose high voltage, fast recovery diodes or SiC Schottky diodes with a low forward voltage drop and low junction capacitance in order to minimize the loss introduced by reverse recovery and related grounding noise bouncing. In the example, the DC-link voltage is 48 V<sub>DC</sub>. The voltage rating of the bootstrap diode should be higher than the DC-link voltage with a good margin. Therefore, a 100-V diode, STPS2H100, is chosen in this example.

When designing a bootstrap supply, it is recommended to use a bootstrap resistor,  $R_{BOOT}$ . A bootstrap resistor, is also used to reduce the inrush current in  $D_{BOOT}$  and limit the ramp up slew rate of voltage of VDDA-VSSA during each switching cycle.

Failure to limit the voltage to VDDx-VSSx to less than the Absolute Maximum Ratings of the FET and UCC21231 may result in permanent damage to the device in certain cases.

The recommended value for  $R_{BOOT}$  is between 1  $\Omega$  and 20  $\Omega$  depending on the diode used. In the example, a current limiting resistor of 5  $\Omega$  is selected to limit the inrush current of bootstrap diode. The estimated worst case peak current through  $D_{BOOT}$  is,

$$I_{DBoot(pk)} = V_{DD} - \frac{V_{BDF}}{R_{Boot}} = \frac{10 - 0.8}{5} = 1.85 \quad (2)$$

where

- $V_{BDF}$  is the estimated bootstrap diode forward voltage drop at 1.85 A.

### 8.2.2.3 Gate Driver Output Resistor

The external gate driver resistors,  $R_{ON}/R_{OFF}$ , are used to:

1. Limit ringing caused by parasitic inductances/capacitances.
2. Limit ringing caused by high voltage/current switching  $dv/dt$ ,  $di/dt$ , and body-diode reverse recovery.
3. Fine-tune gate drive strength, i.e. peak sink and source current to optimize the switching loss.
4. Reduce electromagnetic interference (EMI).

As mentioned in [セクション 7.3.4](#), the UCC21231 has a pull-up structure with a P-channel MOSFET and an additional *pull-up* N-channel MOSFET in parallel. The combined peak source current is 4 A. Therefore, the peak source current can be predicted with:

$$I_{OA+} = \min \left[ 4A, \frac{V_{DD} - V_{BDF}}{R_{NMOS} \parallel [R_{OH} + R_G + R_{GFET\_INT}]} \right] \quad (3)$$

$$I_{OA+} = \min \left[ 4A, \frac{V_{DD}}{R_{NMOS} \parallel [R_{OH} + R_G + R_{GFET\_INT}]} \right] \quad (4)$$

where

- $R_{ON}$ : External turn-on resistance.
- $R_{GFET\_INT}$ : Power transistor internal gate resistance, found in the power transistor datasheet.
- $I_{O+}$  = Peak source current – The minimum value between 4 A, the gate driver peak source current, and the calculated value based on the gate drive loop resistance.

In this example:

$$I_{OA+} = \min \left[ 4A, \frac{10 - 0.4}{1.47\Omega \parallel [5\Omega + 2\Omega + 1.4\Omega]} \right] = 2.1A \quad (5)$$

$$I_{OB+} = \min \left[ 4A, \frac{10}{1.47\Omega \parallel [5\Omega + 2\Omega + 1.4\Omega]} \right] = 2.2A \quad (6)$$

Therefore, the high-side and low-side peak source current is 2.07 A and 2.16 A respectively. Similarly, the peak sink current can be calculated with:

$$I_{OA-} = \min \left[ 6A, \frac{V_{DD} - V_{BDF} - V_{GDF}}{R_{OL} + R_G + R_{GFET\_INT}} \right] \quad (7)$$

$$I_{OA-} = \min \left[ 6A, \frac{V_{DD} - V_{GDF}}{R_{OL} + R_G + R_{GFET\_INT}} \right] \quad (8)$$

where

- $R_{OFF}$ : External turn-off resistance;
- $V_{GDF}$ : The anti-parallel diode forward voltage drop which is in series with  $R_{OFF}$ . The diode in this example is an MSS1P4.
- $I_{O-}$ : Peak sink current – the minimum value between 6 A, the gate driver peak sink current, and the calculated value based on the gate drive loop resistance.

In this example,

$$I_{OA-} = \min\left[6A, \frac{10 - 0.4 - 0.7}{0.55\Omega + 2\Omega + 1.4\Omega}\right] = 2.2A \quad (9)$$

$$I_{OA-} = \min\left[6A, \frac{10 - 0.7}{0.55\Omega + 2\Omega + 1.4\Omega}\right] = 2.3A \quad (10)$$

Therefore, the high-side and low-side peak sink current is 2.2 A and 2.3 A respectively.

Importantly, the estimated peak current is also influenced by PCB layout and load capacitance. Parasitic inductance in the gate driver loop can slow down the peak gate drive current and introduce overshoot and undershoot. Therefore, it is strongly recommended that the gate driver loop should be minimized. On the other hand, the peak source/sink current is dominated by loop parasitics when the load capacitance ( $C_{ISS}$ ) of the power transistor is very small (typically less than 1 nF), because the rising and falling time is too small and close to the parasitic ringing period.

Failure to control OUTx voltage to less than the Absolute Maximum Ratings in the datasheet (including transients) may result in permanent damage to the device in certain cases. To reduce excessive gate ringing, it is recommended to use a ferrite bead near the gate of the FET. External clamping diodes can also be added in the case of extended overshoot/undershoot, in order to clamp the OUTx voltage to the VDDx and VSSx voltages.


#### 8.2.2.4 Gate to Source Resistor Selection

A gate to source resistor,  $R_{GS}$ , is recommended to pull down the gate to the source voltage when the gate driver output is unpowered and in an indeterminate state. This resistor also helps to mitigate the risk of dv/dt induced turn-on due to Miller current before the gate driver is able to turn on and actively pull low. This resistor is typically sized between 5.1kΩ and 20kΩ, depending on the  $V_{th}$  and ratio of  $C_{GD}$  to  $C_{GS}$  of the power device.

#### 8.2.2.5 Estimate Gate Driver Power Loss

The total loss,  $P_G$ , in the gate driver subsystem includes the power losses of the UCC21231 ( $P_{GD}$ ) and the power losses in the peripheral circuitry, such as the external gate drive resistor. Bootstrap diode loss is not included in  $P_G$  and not discussed in this section.

$P_{GD}$  is the key power loss which determines the thermal safety-related limits of the UCC21231, and it can be estimated by calculating losses from several components.

The first component is the static power loss,  $P_{GDQ}$ , which includes quiescent power loss on the driver as well as driver self-power consumption when operating with a certain switching frequency.  $P_{GDQ}$  is measured on the bench with no load connected to OUTA and OUTB at a given  $V_{CCI}$ ,  $V_{DDA}/V_{DDB}$ , switching frequency and ambient temperature.  5-3 shows the per output channel current consumption vs operating frequency with no load. In this example,  $V_{VCCI} = 5\text{ V}$  and  $V_{VDD} = 10\text{ V}$ . The current on each power supply, with INA/INB switching from 0 V to 3.3 V at 200 kHz is measured to be  $I_{VCCI} = 2.5\text{ mA}$ , and  $I_{VDDA} = I_{VDDB} = 1.5\text{ mA}$ . Therefore, the  $P_{GDQ}$  can be calculated with

$$P_{GDQ} = (V_{CCI} \times I_{VCCI}) + (V_{DDA} \times I_{VDDA}) + (V_{DDB} \times I_{VDDB}) = 32mW \quad (11)$$

The second component is switching operation loss,  $P_{GDO}$ , with a given load capacitance which the driver charges and discharges the load during each switching cycle. Total dynamic loss due to load switching,  $P_{GSW}$ , can be estimated with

$$P_{GSW} = 2 \times V_{DD} \times Q_G \times f_{SW} \quad (12)$$

where

- $Q_G$  is the gate charge of the power transistor.

If a split rail is used to turn on and turn off, then VDD is going to be equal to difference between the positive rail to the negative rail.

So, for this example application:

$$P_{GSW} = 2 \times 10V \times 75nC \times 200kHz = 300mW \quad (13)$$

$Q_G$  represents the total gate charge of the power transistor switching 50 V at 100 A, and is subject to change with different testing conditions. The UCC21231 gate driver loss on the output stage,  $P_{GDO}$ , is part of  $P_{GSW}$ .  $P_{GDO}$  will be equal to  $P_{GSW}$  if the external gate driver resistances are zero, and all the gate driver loss is dissipated inside the UCC21231. If there are external turn-on and turn-off resistances, the total loss will be distributed between the gate driver pull-up/down resistances and external gate resistances. Importantly, the pull-up/down resistance is a linear and fixed resistance if the source/sink current is not saturated to 4 A/6 A, however, it will be non-linear if the source/sink current is saturated. Therefore,  $P_{GDO}$  is different in these two scenarios.

#### Case 1 - Linear Pull-Up/Down Resistor:

$$P_{GDO} = \frac{P_{GSW}}{2} \left[ \frac{R_{NMOS} || R_{OH}}{R_{NMOS} || R_{OH} + R_G + R_{GFET_{int}}} + \frac{R_{OL}}{R_{OL} + R_G + R_{GFET_{int}}} \right] \quad (14)$$

In this design example, all the predicted source/sink currents are less than 4 A/6 A, therefore, the UCC21231 gate driver loss can be estimated with:

$$TBD \quad (15)$$

#### Case 2 - Nonlinear Pull-Up/Down Resistor:

$$P_{GDO} = 2 \times f_{sw} \times \left[ 4A \times \int_0^{T_{R_{sys}}} (V_{DD} - V_{OUTA/B}(t)) dt + 6A \times \int_0^{T_{R_{sys}}} V_{OUTA/B}(t) dt \right] \quad (16)$$

where

- $V_{OUTA/B}(t)$  is the gate driver OUTA and OUTB pin voltage during the turn on and off transient, and it can be simplified that a constant current source (4 A at turn-on and 6 A at turn-off) is charging/discharging a load capacitor. Then, the  $V_{OUTA/B}(t)$  waveform will be linear and the  $T_{R_{sys}}$  and  $T_{F_{sys}}$  can be easily predicted.

For some scenarios, if only one of the pull-up or pull-down circuits is saturated and another one is not, the  $P_{GDO}$  will be a combination of Case 1 and Case 2, and the equations can be easily identified for the pull-up and pull-down based on the above discussion. Therefore, total gate driver loss dissipated in the gate driver UCC21231,  $P_{GD}$ , is:

$$P_{GD} = P_{GDQ} + P_{GDO} = 32mW + 57mW = 89mW \quad (17)$$

which is equal to 89 mW in the design example.

#### 8.2.2.6 Estimating Junction Temperature

The junction temperature ( $T_J$ ) of the UCC21231 can be estimated with:

$$T_J = T_C + \Psi_{JT} \times P_{GD} \quad (18)$$

where

- $T_C$  is the UCC21231 case-top temperature measured with a thermocouple or some other instrument, and
- $\Psi_{JT}$  is the Junction-to-top characterization parameter from the [セクション 5.4](#) table.

Using the junction-to-top characterization parameter ( $\Psi_{JT}$ ) instead of the junction-to-case thermal resistance ( $R_{\theta JC}$ ) can greatly improve the accuracy of the junction temperature estimation. The majority of the thermal energy of most ICs is released into the PCB through the package leads, whereas only a small percentage of the total energy is released through the top of the case (where thermocouple measurements are usually conducted).  $R_{\theta JC}$  can only be used effectively when most of the thermal energy is released through the case, such as with metal packages or when a heatsink is applied to an IC package. In all other cases, use of  $R_{\theta JC}$  will inaccurately estimate the true junction temperature.  $\Psi_{JT}$  is experimentally derived by assuming that the amount of energy leaving through the top of the IC will be similar in both the testing environment and the application environment. As long as the recommended layout guidelines are observed, junction temperature estimates can be made accurately to within a few degrees Celsius. For more information, see the [Semiconductor and IC Package Thermal Metrics Application Report](#).

### 8.2.2.7 Selecting VCCI, VDDA/B Capacitor

Bypass capacitors for VCCI, VDDA, and VDDDB are essential for achieving reliable performance. It is recommended that one choose low ESR and low ESL surface-mount multi-layer ceramic capacitors (MLCC) with sufficient voltage ratings, temperature coefficients and capacitance tolerances. Importantly, DC bias on an MLCC will impact the actual capacitance value. For example, a 25-V, 1- $\mu$ F X7R capacitor is measured to be only 500 nF when a DC bias of 15 V<sub>DC</sub> is applied.

#### 8.2.2.7.1 Selecting a VCCI Capacitor

A bypass capacitor connected to VCCI supports the transient current needed for the primary logic and the total current consumption, which is only a few mA. Therefore, a 50-V MLCC with over 100 nF is recommended for this application. If the bias power supply output is a relatively long distance from the VCCI pin, a tantalum or electrolytic capacitor, with a value over 1  $\mu$ F, should be placed in parallel with the MLCC.

#### 8.2.2.7.2 Selecting a VDDA (Bootstrap) Capacitor

A VDDA capacitor, also referred to as a *bootstrap capacitor* in bootstrap power supply configurations, allows for gate drive current transients up to 6 A, and needs to maintain a stable gate drive voltage for the power transistor.

The total charge needed per switching cycle can be estimated with

$$Q_{\text{Total}} = Q_G + \frac{I_{VDD@200\text{kHz (no load)}}}{f_{\text{SW}}} = 75\text{nC} + \frac{1.5\text{mA}}{200\text{kHz}} = 82.5\text{nC} \quad (19)$$

where

- $Q_{\text{Total}}$ : Total charge needed
- $Q_G$ : Gate charge of the power transistor.
- $I_{VDD}$ : The channel self-current consumption with no load at 200kHz.
- $f_{\text{SW}}$ : The switching frequency of the gate driver

Therefore, the absolute minimum  $C_{\text{Boot}}$  requirement is:

$$C_{\text{Boot}} = \frac{Q_{\text{Total}}}{\Delta V_{\text{VDDA}}} = \frac{82.5\text{ nC}}{0.5\text{ V}} = 165\text{nF} \quad (20)$$

where

- $\Delta V_{\text{VDDA}}$  is the voltage ripple at VDDA, which is 0.5 V in this example.

In practice, the value of  $C_{\text{Boot}}$  is greater than the calculated value. This allows for the capacitance shift caused by the DC bias voltage and for situations where the power stage would otherwise skip pulses due to load transients. Therefore, it is recommended to include a safety-related margin in the  $C_{\text{Boot}}$  value and place it as close to the VDD and VSS pins as possible. A 50-V 1- $\mu$ F capacitor is chosen in this example.

Care should be taken when selecting the bootstrap capacitor to ensure that the VDD to VSS voltage does not drop below the recommended minimum operating level listed in section 6.3. The value of the bootstrap capacitor

should be sized such that it can supply the initial charge to switch the power device, and then continuously supply the gate driver quiescent current for the duration of the high-side on-time.

If the high-side supply voltage drops below the UVLO falling threshold, the high-side gate driver output will turn off and switch the power device off. Uncontrolled hard-switching of power devices can cause high di/dt and high dv/dt transients on the output of the driver and may result in permanent damage to the device.

To further lower the AC impedance for a wide frequency range, it is recommended to have bypass capacitor placed very close to VDDx - VSSx pins with a low ESL/ESR. In this example a 100 nF, X7R ceramic capacitor, is placed in parallel with C<sub>BOOT</sub> to optimize the transient performance.

#### 注

Too large C<sub>BOOT</sub> is not good. C<sub>BOOT</sub> may not be charged within the first few cycles and V<sub>BOOT</sub> could stay below UVLO. As a result, the high-side FET does not follow input signal command. Also during initial C<sub>BOOT</sub> charging cycles, the bootstrap diode has highest reverse recovery current and losses.

#### 8.2.2.7.3 Select a VDDDB Capacitor

Channel B has the same current requirements as Channel A, Therefore, a VDDDB capacitor (shown as C<sub>VDD</sub> in [図 8-1](#)) is needed. In this example with a bootstrap configuration, the VDDDB capacitor will also supply current for VDDA through the bootstrap diode. A 50-V, 10-μF MLCC and a 50-V, 220-nF MLCC are chosen for C<sub>VDD</sub>. If the bias power supply output is a relatively long distance from the VDDDB pin, a tantalum or electrolytic capacitor, with a value over 10 μF, should be used in parallel with CVDD.

#### 8.2.2.8 Dead Time Setting Guidelines

For power converter topologies utilizing half-bridges, the dead time setting between the top and bottom transistor is important for preventing shoot-through during dynamic switching.

The UCC21231 dead time specification in the electrical table is defined as the time interval from 90% of one channel's falling edge to 10% of the other channel's rising edge (see [図 6-4](#)). This definition ensures that the dead time setting is independent of the load condition, and guarantees linearity through manufacture testing. However, this dead time setting may not reflect the dead time in the power converter system, since the dead time setting is dependent on the external gate drive turn-on/off resistor, DC-Link switching voltage/current, as well as the input capacitance of the load transistor.

Here is a suggestion on how to select an appropriate dead time for UCC21231:

$$DT_{\text{Setting}} = DT_{\text{Req}} + T_{\text{F\_Sys}} + T_{\text{R\_Sys}} - T_{\text{D(on)}} \quad (21)$$

where

- DT<sub>setting</sub>: UCC21231 dead time setting in ns,  $DT_{\text{Setting}} = 8.6 \times RDT(\text{in k}\Omega) + 13$ .
- DT<sub>Req</sub>: System required dead time between the real V<sub>GS</sub> signal of the top and bottom switch with enough margin, or ZVS requirement.
- T<sub>F\_Sys</sub>: In-system gate turn-off falling time at worst case of load, voltage/current conditions.
- T<sub>R\_Sys</sub>: In-system gate turn-on rising time at worst case of load, voltage/current conditions.
- T<sub>D(on)</sub>: Turn-on delay time, from 10% of the transistor gate signal to power transistor gate threshold.

It should be noted that the UCC21231 dead time setting is decided by the DT pin configuration (see [セクション 7.4.2](#)), and it cannot automatically fine-tune the dead time based on system conditions.

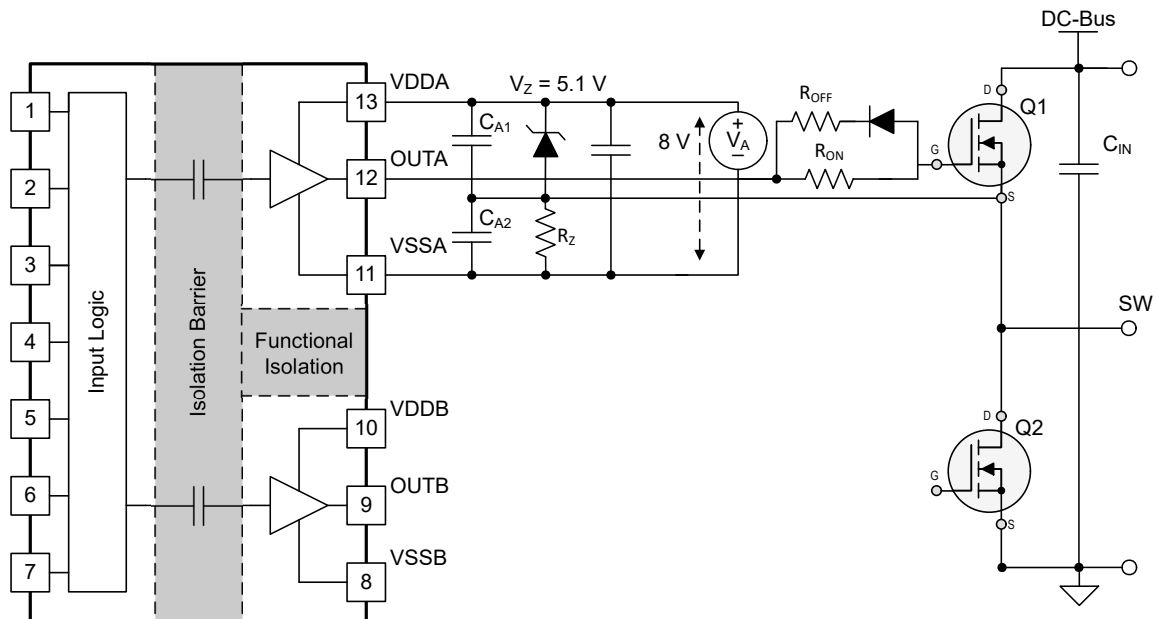


### 8.2.2.9 Application Circuits with Output Stage Negative Bias

When parasitic inductances are introduced by non-ideal PCB layout and long package leads, there could be ringing in the gate-source drive voltage of the power transistor during high di/dt and dv/dt switching. If the ringing is over the threshold voltage, there is the risk of unintended turn-on and even shoot-through. Applying a negative bias on the gate drive is a popular way to keep such ringing below the threshold. Below are a few examples of implementing negative gate drive bias.

✎ 8-2 shows the first example with negative bias turn-off on the channel-A driver using a Zener diode on the isolated power supply output stage. The positive bias is set by the Zener diode voltage. If the isolated power supply,  $V_A$ , is equal to 8 V, the turn-on voltage will be 5.1 V and turn-on voltage will be  $8\text{ V} - 5.1\text{ V} \approx 2.9\text{ V}$ . The channel-B driver circuit is the same as channel-A, therefore, this configuration needs two power supplies for a half-bridge configuration, and there will be steady state power consumption from  $R_Z$ .

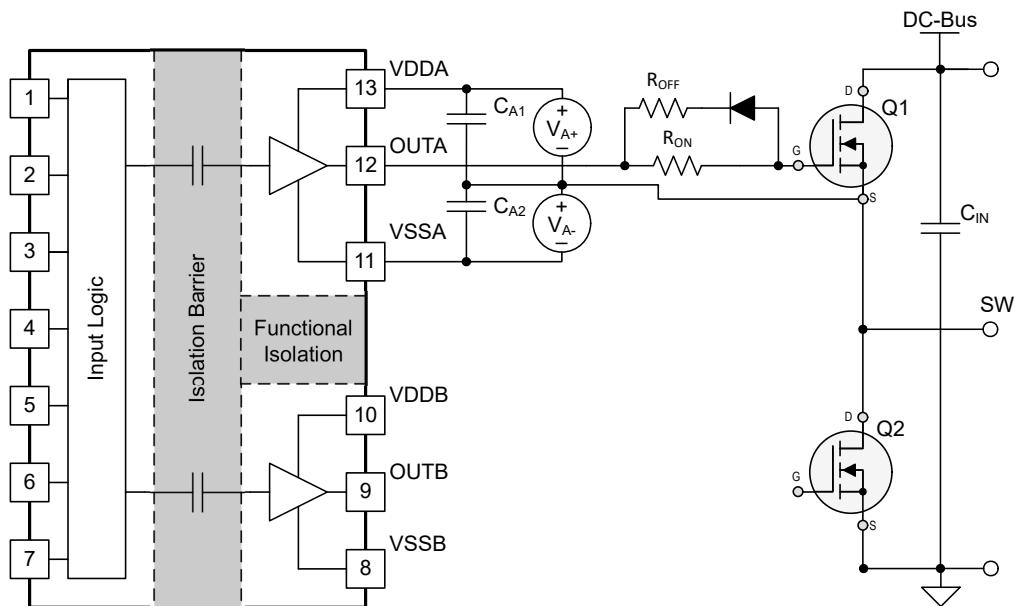
The circuit implementation in ✎ 8-2 is suitable to drive GaN HEMT devices with regulated turn-on voltage for higher gate robustness. The negative voltage also protects the GaN from false turn-on during the miller charge due to low gate threshold voltage.



✎ 8-2. Negative Bias with Zener Diode on Iso-Bias Power Supply Output



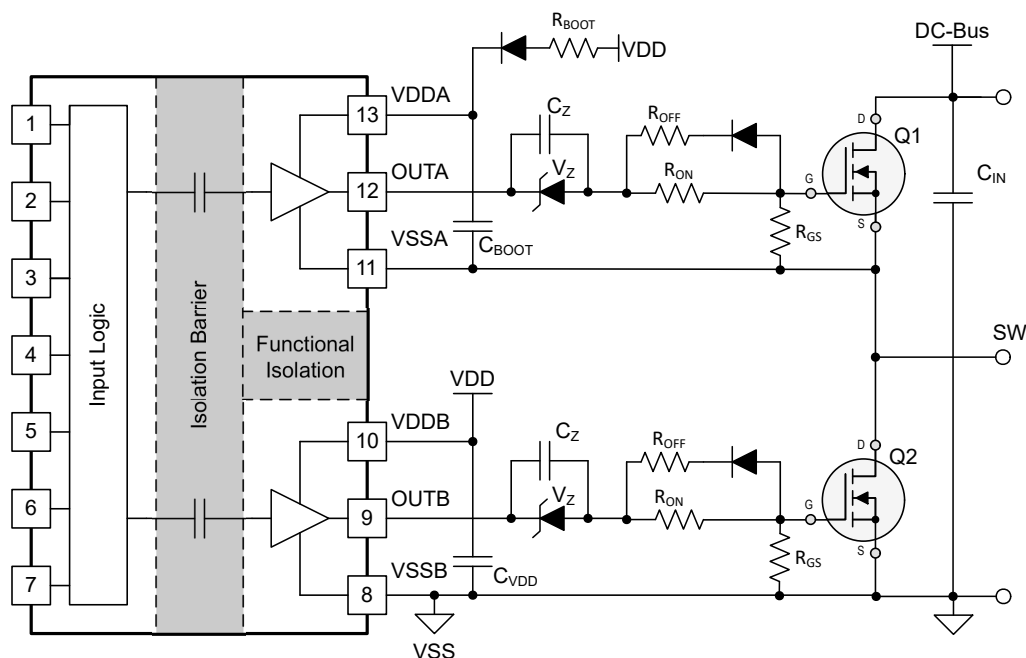
Figure 8-3 shows another example which uses two supplies (or single-input-double-output power supply). Power supply  $V_{A+}$  determines the positive drive output voltage and  $V_{A-}$  determines the negative turn-off voltage. The configuration for channel B is the same as channel A. This solution requires more power supplies than the first example, however, it provides more flexibility when setting the positive and negative rail voltages.



**Figure 8-3. Negative Bias with Two Iso-Bias Power Supplies**

The last example, shown in [Figure 8-4](#), is a single power supply configuration and generates negative bias through a Zener diode in the gate drive loop. The benefit of this solution is that it only uses one power supply and the bootstrap power supply can be used for the high side drive. This design requires the least cost and design effort among the three solutions. However, this solution has limitations:

1. The negative gate drive bias is not only determined by the Zener diode, but also by the duty cycle, which means the negative bias voltage will change when the duty cycle changes. Therefore, converters with a fixed duty cycle (~50%) such as variable frequency resonant converters or phase shift converters favor this solution.
2. The high side VDDA-VSSA must maintain enough voltage to stay in the recommended power supply range, which means the low side switch must turn-on or have free-wheeling current on the body (or anti-parallel) diode for a certain period during each switching cycle to refresh the bootstrap capacitor. Therefore, a 100% duty cycle for the high side is not possible unless there is a dedicated power supply for the high side, like in the other two example circuits.



**Figure 8-4. Negative Bias with Single Power Supply and Zener Diode in Gate Drive Path**

### 8.2.3 Application Curves

Figure 8-5 shows the bench test waveforms for the design example shown in Figure 8-1 under these conditions:  $V_{CC} = 5$  V,  $V_{DD} = 20$  V,  $f_{SW} = 100$  kHz,  $V_{DC-Link} = 0$  V.

**Channel 1 (Yellow):** UCC21231 INA pin signal.

**Channel 2 (Blue):** UCC21231 INB pin signal.

**Channel 3 (Pink):** Gate-source signal on the high side power transistor.

**Channel 4 (Green):** Gate-source signal on the low side power transistor.

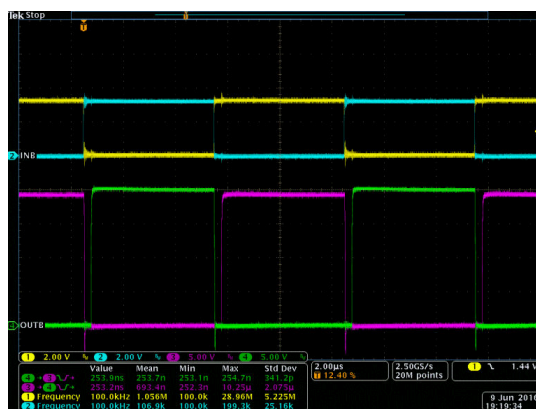


Figure 8-5. Bench Test Waveform for INA/B and OUTA/B

## 9 Power Supply Recommendations

The recommended input supply voltage (VCCI) for the UCC21231 is between 3.0 V and 5.5 V. The output bias supply voltage (VDDA/VDDDB) range depends on which version of UCC21231 one is using. The lower end of this bias supply range is governed by the internal under voltage lockout (UVLO) protection feature of each device. One mustn't let VDD or VCCI fall below their respective UVLO thresholds. The upper end of the VDDA/VDDDB range depends on the maximum gate voltage of the power device being driven by the UCC21231 have a recommended maximum VDDA/VDDDB of 25 V.

A local bypass capacitor should be placed between the VDD and VSS pins. This capacitor should be positioned as close to the device as possible. A low ESR, ceramic surface mount capacitor is recommended. It is further suggested that one place two such capacitors: one with a value of  $\approx 10\text{-}\mu\text{F}$  for device biasing, and an additional  $\leq 100\text{-nF}$  capacitor in parallel for high frequency filtering.

Similarly, a bypass capacitor should also be placed between the VCCI and GND pins. Given the small amount of current drawn by the logic circuitry within the input side of the UCC21231, this bypass capacitor has a minimum recommended value of 100 nF.

## 10 Layout

### 10.1 Layout Guidelines

One must pay close attention to PCB layout in order to achieve optimum performance for the UCC21231. Below are some key points.

#### Component Placement:

- Low-ESR and low-ESL capacitors must be connected close to the device between the VCCI and GND pins and between the VDD and VSS pins to support high peak currents when turning on the external power transistor.
- To avoid large negative transients on the switch node VSSA (HS) pin, the parasitic inductances between the source of the top transistor and the source of the bottom transistor must be minimized.
- It is recommended to place the dead-time setting resistor,  $R_{DT}$ , and its bypassing capacitor close to DT pin of the UCC21231.
- It is recommended to bypass using a  $\approx 1\text{nF}$  low ESR/ESL capacitor,  $C_{EN}$ , close to EN pin when connecting to a  $\mu\text{C}$  with distance.

#### Grounding Considerations:

- It is essential to confine the high peak currents that charge and discharge the transistor gates to a minimal physical area. This will decrease the loop inductance and minimize noise on the gate terminals of the transistors. The gate driver must be placed as close as possible to the transistors.
- Pay attention to high current path that includes the bootstrap capacitor, bootstrap diode, local VSSB-referenced bypass capacitor, and the low-side transistor body/anti-parallel diode. The bootstrap capacitor is recharged on a cycle-by-cycle basis through the bootstrap diode by the VDD bypass capacitor. This recharging occurs in a short time interval and involves a high peak current. Minimizing this loop length and area on the circuit board is important for ensuring reliable operation.

#### High-Voltage Considerations:

- To ensure isolation performance between the primary and secondary side, one should avoid placing any PCB traces or copper below the driver device. A PCB cutout is recommended in order to prevent contamination that may compromise the UCC21231's isolation performance.
- For half-bridge, or high-side/low-side configurations, where the channel A and channel B drivers could operate with a DC-link voltage up to  $1500\text{ V}_{DC}$ , one should try to increase the creepage distance of the PCB layout between the high and low-side PCB traces.

#### Thermal Considerations:

- A large amount of power may be dissipated by the UCC21231 if the driving voltage is high, the load is heavy, or the switching frequency is high (refer to [セクション 8.2.2.5](#) for more details). Proper PCB layout can help dissipate heat from the device to the PCB and minimize junction to board thermal impedance ( $\theta_{JB}$ ).
- Increasing the PCB copper connecting to VDDA, VDDDB, VSSA and VSSB pins is recommended, with priority on maximizing the connection to VSSA and VSSB (see [図 10-1](#) and [図 10-2](#)). However, high voltage PCB considerations mentioned above must be maintained.
- If there are multiple layers in the system, it is also recommended to connect the VDDA, VDDDB, VSSA and VSSB pins to internal ground or power planes through multiple vias of adequate size. However, keep in mind that there shouldn't be any traces/coppers from different high voltage planes overlapping.

## 10.2 Layout Example

A 2-layer pcb layout example is shown below. Components such as bypass capacitors are placed closely to the device pins.

注

There are no PCB traces or copper between the primary and secondary side, which ensures isolation performance.

PCB traces between the high-side and low-side gate drivers in the output stage are increased to maximize the creepage distance for high-voltage operation, which will also minimize cross-talk between the switching node VSSA (SW), where high  $dv/dt$  may exist, and the low-side gate drive due to the parasitic capacitance coupling.

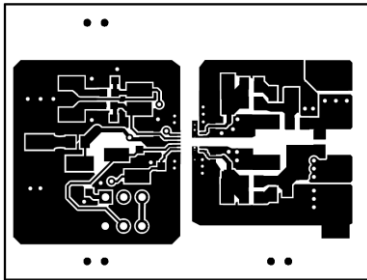


図 10-1. Top Layer Traces and Copper

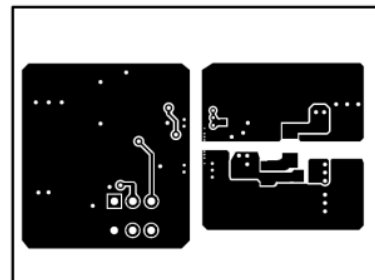


図 10-2. Bottom Layer Traces and Copper

## 11 Device and Documentation Support

### 11.1 Device Support

#### 11.1.1 サード・パーティ製品に関する免責事項

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### 11.2 Documentation Support

#### 11.2.1 Related Documentation

For related documentation see the following:

- [Semiconductor and IC Package Thermal Metrics Application Report](#)
- [Isolation Glossary](#)

### 11.3 Certifications

UL Online Certifications Directory, "[FPPT2.E181974 Nonoptical Isolating Devices - Component](#)" Certificate Number: 20160516-E181974,

VDE [Pruf- und Zertifizierungsinstitut Certification](#), Certificate of Conformity with Factory Surveillance

CQC Online Certifications Directory, "[GB4943.1-2011, Digital Isolator Certificate](#)" Certificate Number: CQC16001155011

CSA Online Certifications Directory, "[CSA Certificate of Compliance](#)" Certificate Number: 70097761, Master Contract Number: 220991

### 11.4 ドキュメントの更新通知を受け取る方法

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### 11.8 用語集

#### テキサス・インスツルメンツ用語集

この用語集には、用語や略語の一覧および定義が記載されています。

## 12 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

### Changes from Revision \* (April 2024) to Revision A (June 2024)

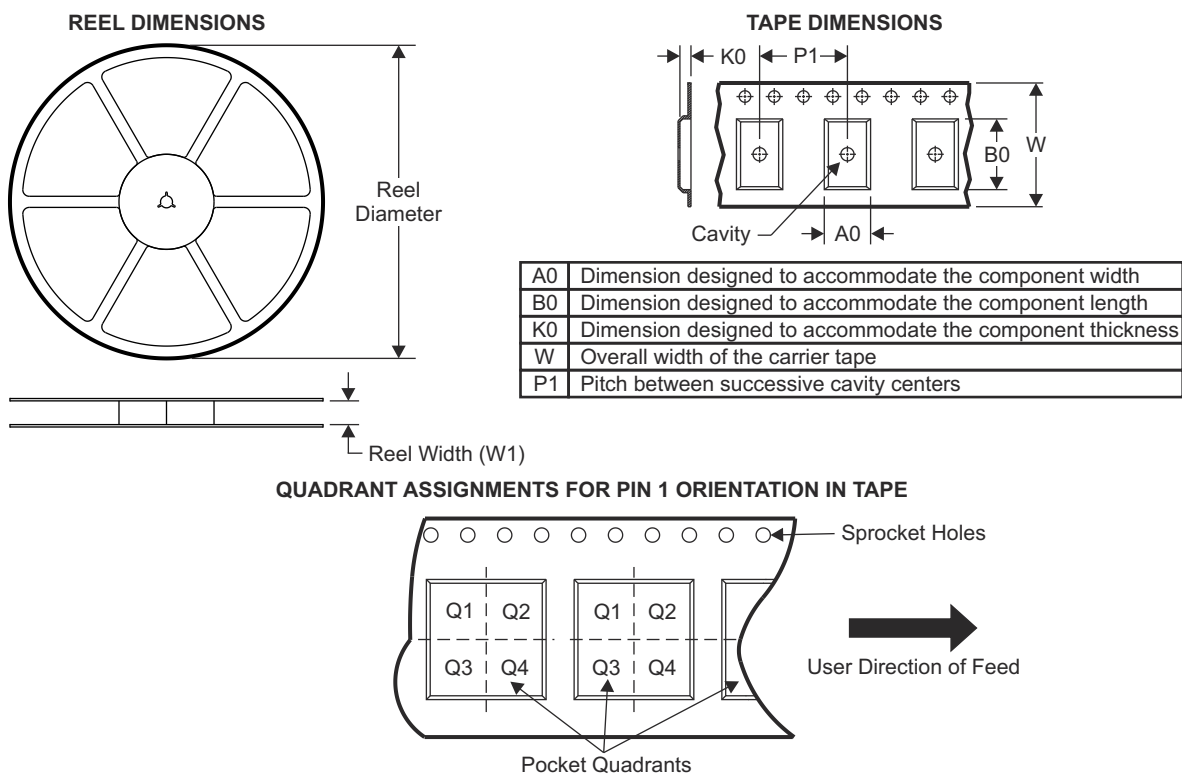
Page

- 「事前情報」から「量産データ」に変更..... 1

## 13 Mechanical, Packaging, and Orderable Information

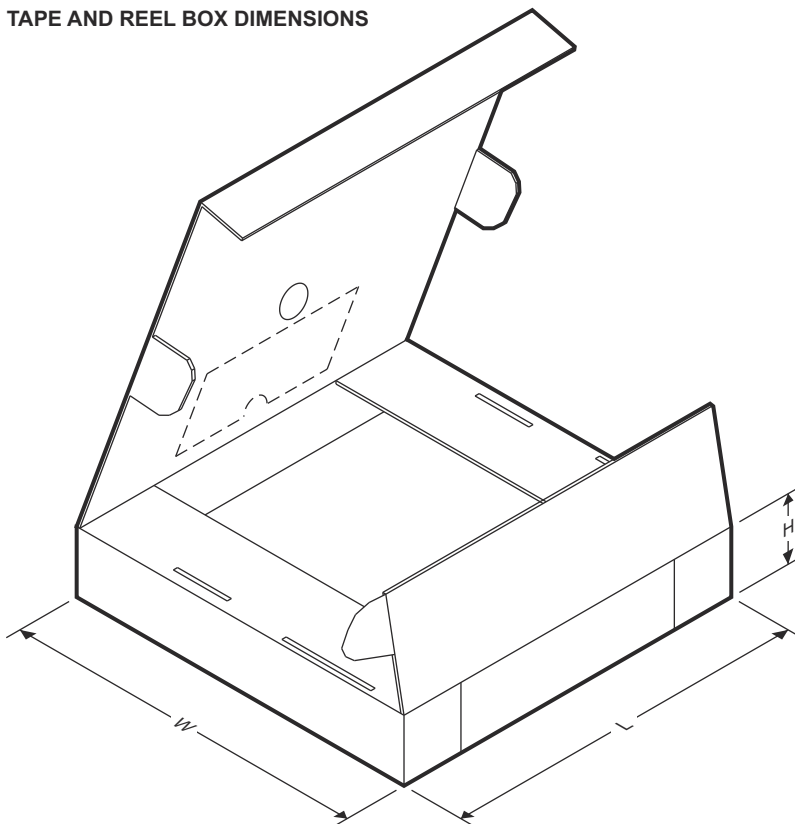
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

### 13.1 Tape and Reel Information





TAPE AND REEL BOX DIMENSIONS



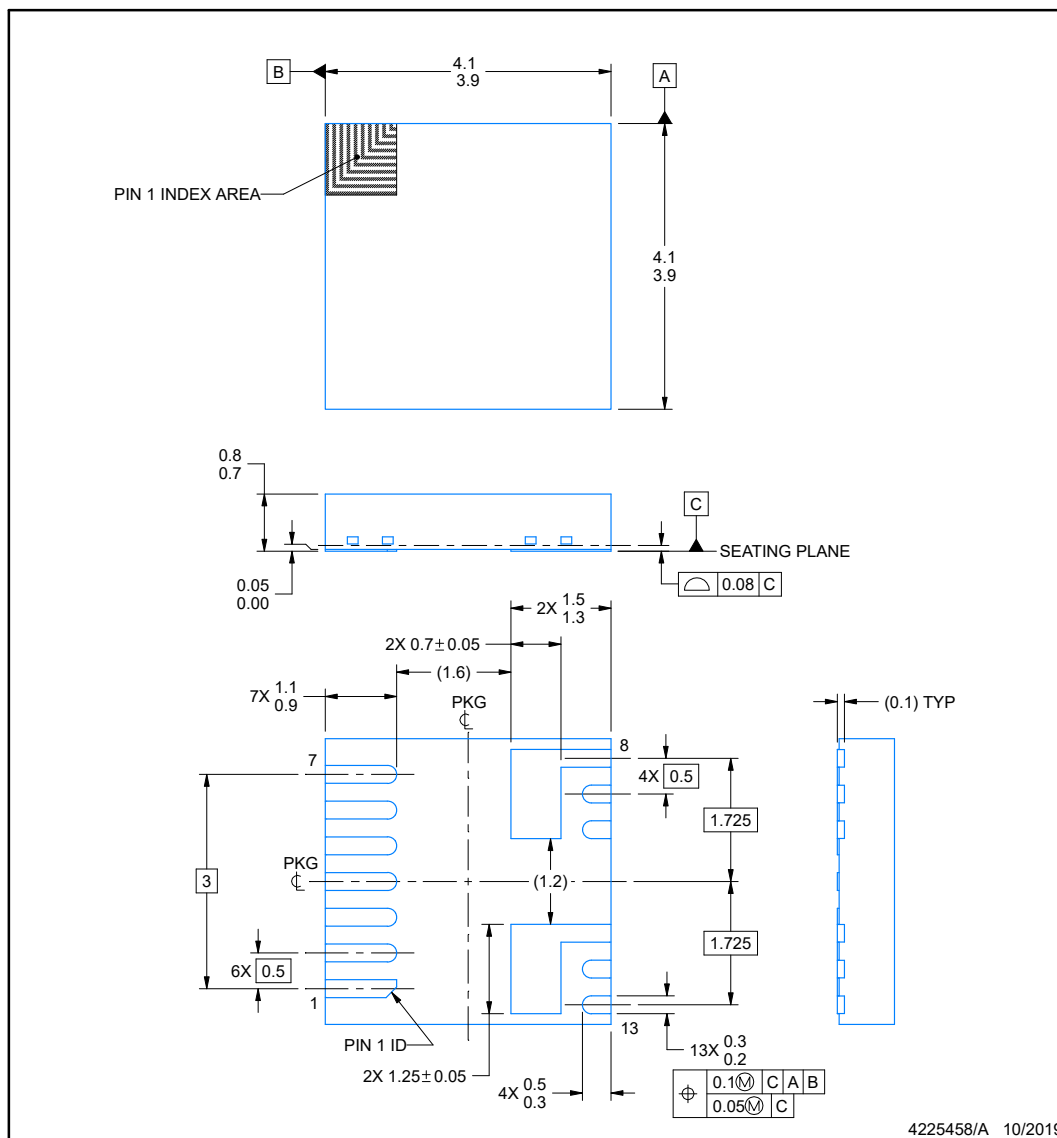
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC21231ADLGR	WSN	DLG	13	3000	350	350	43

## 13.2 Mechanical Data

### PACKAGE OUTLINE

**DLG0013A**
**WSN - 0.8 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD


**NOTES:**

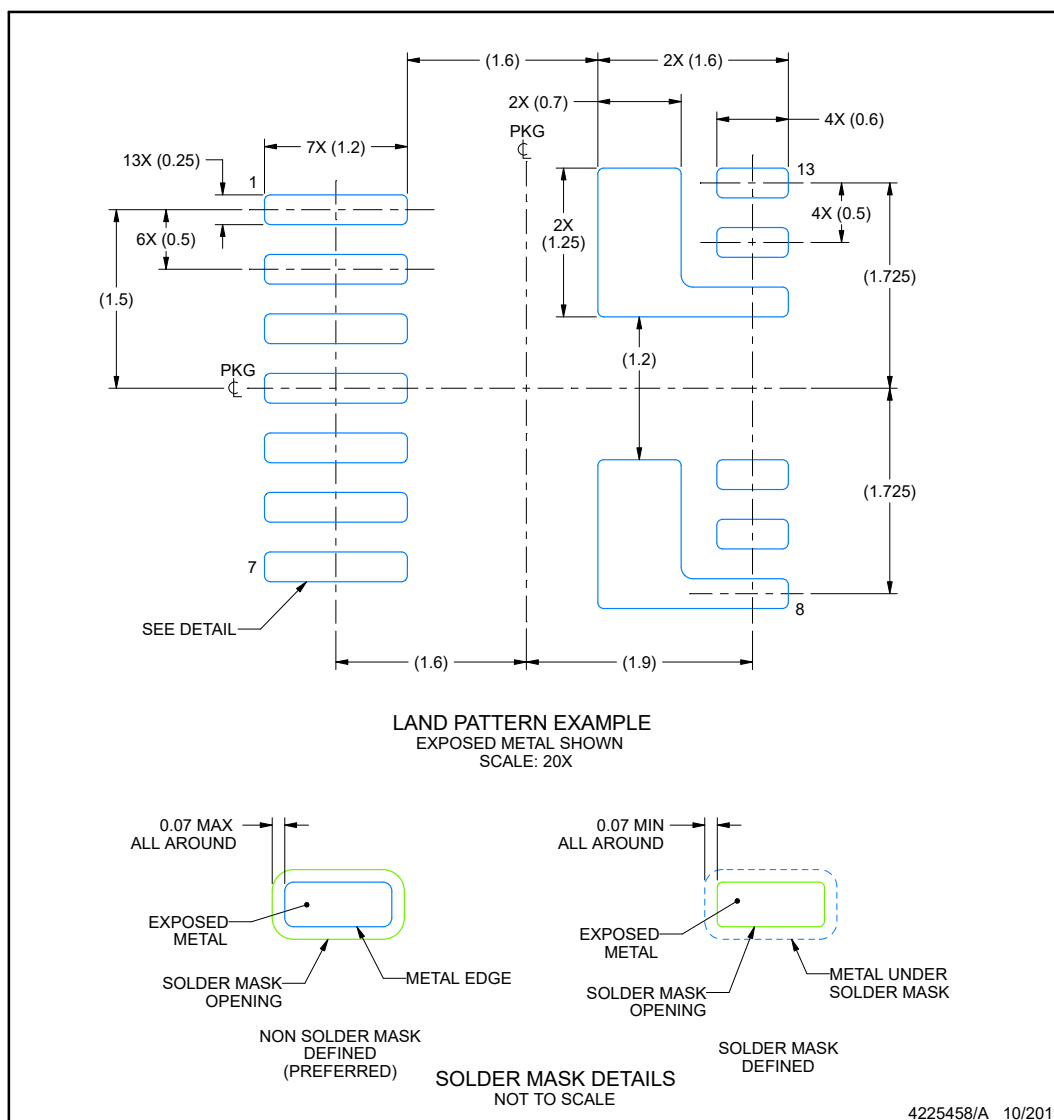
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

## EXAMPLE BOARD LAYOUT

**DLG0013A**

**WSON - 0.8 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD

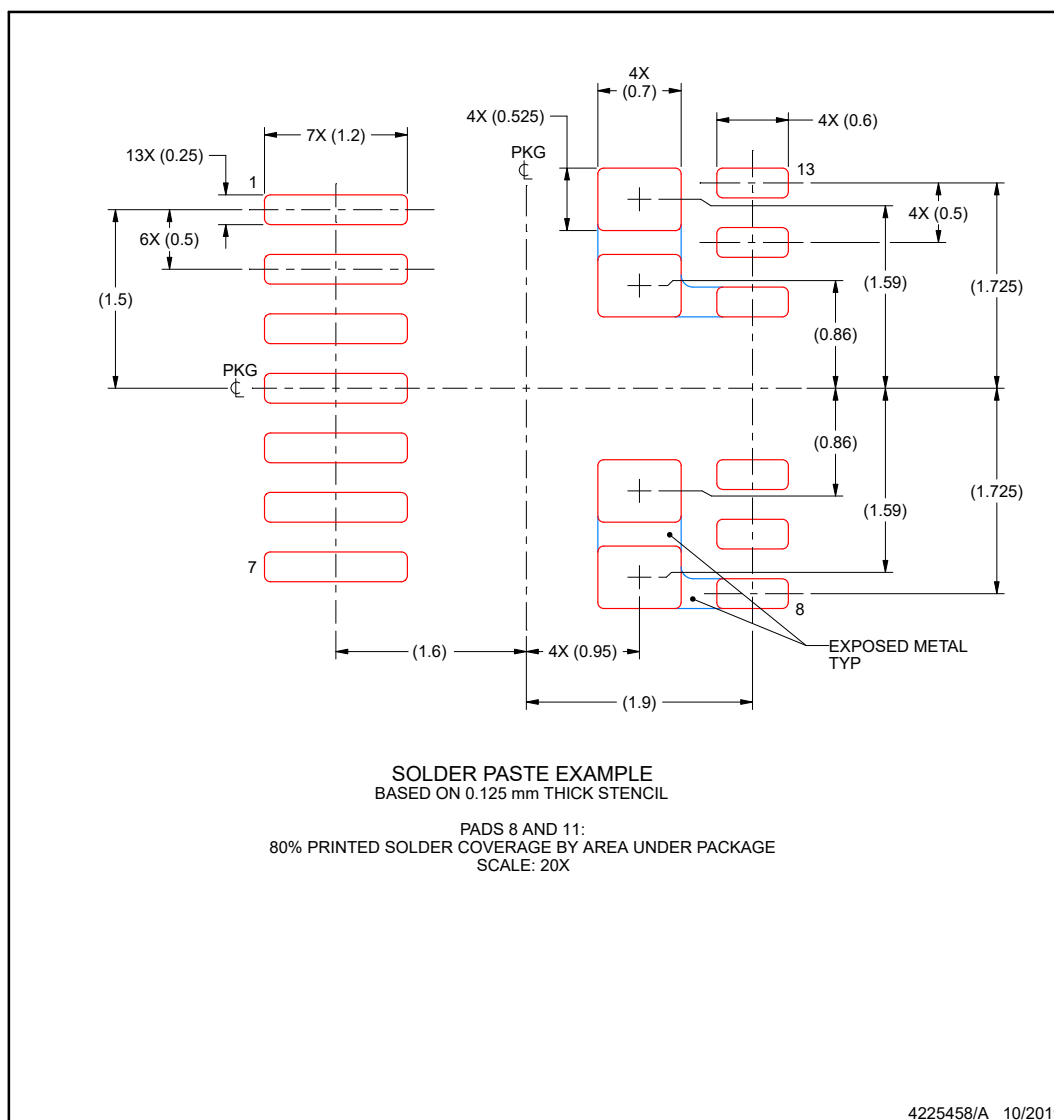


NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sl原因271](http://www.ti.com/lit/sl原因271)).

**EXAMPLE STENCIL DESIGN****DLG0013A****WSON - 0.8 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">PUCC21231ADLGR</a>	Active	Preproduction	WSO (DLG)   13	3000   LARGE T&R	-	Call TI	Call TI	-40 to 125	
PUCC21231ADLGR.A	Active	Preproduction	WSO (DLG)   13	3000   LARGE T&R	-	Call TI	Call TI	-40 to 125	
<a href="#">UCC21231ADLGR</a>	Active	Production	WSO (DLG)   13	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	U21231A DLG
UCC21231ADLGR.A	Active	Production	WSO (DLG)   13	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	U21231A DLG

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

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