UCC21759-Q1 アクティブ保護および絶縁アナログ センシング機能搭載、高 CMTI、車載用 10A ソース / シンク、SiC/IGBT 向け、基本絶縁型シングル チャネル ゲート ドライバ

1 特長

- 3kV$_{RMS}$ のシングル チャネル絶縁型ゲートドライバ
- 車載アプリケーション向けに AEC-Q100 認証済み
  - デバイス温度グレード 1:動作時周囲温度範囲 -40℃～+125℃
  - デバイス HBM ESD 分類レベル 3A
  - デバイス CDM ESD 分類レベル C3
- 最高 900V$_{pk}$ の SiC MOSFET および IGBT
- 出力駆動電圧 (VDD-VEE):33V (最大値)
- 大きなピーク駆動電流と高い CMTI
- ±10A の駆動能力と分割出力
- 最小 CMTI:150V/ns
- 200ns の応答時間による高速な DESAT 保護
- 4A の内部アクティブ ミラー クランプ
- 400mA のソフト ターンオフ (フォルト検出時)
- PWM 出力を備えた絶縁アナログ センサで
  - NTC、PTC、サーマル ダイオードによる温度センシング
  - 高電圧 DC リンクまたは相電圧
- アラーム $\overline{FLT}$ で過電流を通知、$\overline{RST}$/EN でリセット
- 信号 $\overline{RST}$/EN に高速イネーブル / ディセーブル応答
- 入力ピンの <40ns のノイズ過渡およびパルスを除去
- 12V VDD UVLO (RDY のパワー グッド付き)
- 最大 5V のオーバー / アンダーシュート過渡電圧に耐える入力 / 出力
- 伝搬遅延時間:130ns (最大値)、パルス / 部品スキュー:30ns (最大値)
- 沿面距離と空間距離が >8mm の SOIC-16 DW パッケージ
- 動作時の接合部温度:–40℃～+150℃
- 安全関連認証:
  - EN IEC 60747-17 (VDE 0884-17) に準拠した基本絶縁耐圧:4242V$_{PK}$

2 アプリケーション

- EV 用トラクション・インバータ
- オンボード充電器および充電ステーション
- HEV/EV 用 DC/DC コンバータ

3 概要

UCC21759-Q1 は、先進の保護機能、クラス最高の動的性能、堅牢性を持ち合わせ、最高 990V (DC) で動作する SiC MOSFET および IGBT 用に設計されたガルバニック絶縁型シングル チャネル ゲート ドライバです。UCC21759-Q1 は、最大 ±10A のピーク ソース / シンク電流を供給できます。

入力側は SiO_2 容量性絶縁技術によって出力側から絶縁され、最大 636V$_{RMS}$ の動作電圧に対応し、40 年を超える寿命の絶縁バリアにより 6kV$_{PK}$ のサージ耐性を備えるとともに、部品間スキューが小さく、>150V/ns の同相ノイズ耐性 (CMTI) を実現しています。

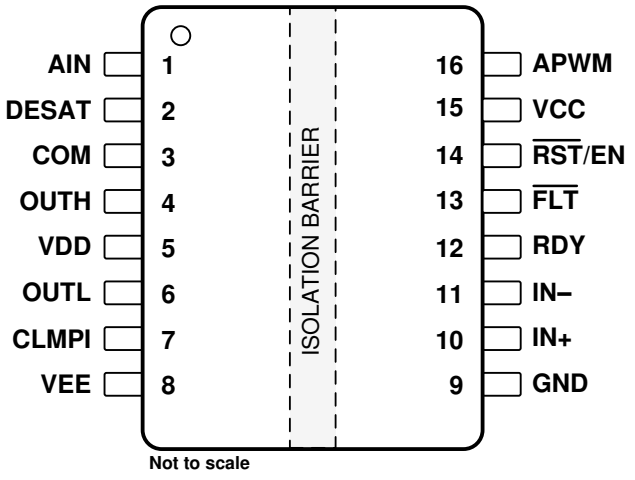
UCC21759-Q1 は、高速の過電流および短絡検出、フォルト通知、アクティブ ミラー クランプ、入力側および出力側電源 UVLO などの最新の保護機能を備えているため、SiC および IGBT パワー トランジスタを最適化できます。アナログから PWM へ信号を変換する、この絶縁型センサは、温度または電圧のセンシングを簡単に行えるため、ドライバの汎用性をさらに高め、システムの設計工数、サイズ、およびコストを簡素化できます。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
UCC21759-Q1	DW (SOIC-16)	10.3mm × 7.5mm

(1) 供給されているすべてのパッケージについては、セクション 13 を参照してください。

デバイスのピン構成



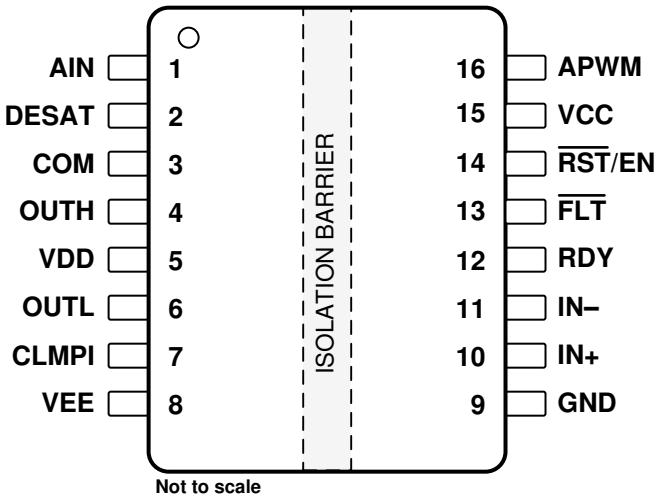
Not to scale

Table of Contents

1 特長 ... 1
2 アプリケーション ... 1
3 概要 ... 1
4 Pin Configuration and Functions ... 3
5 Specifications ... 4
5.1 Absolute Maximum Ratings ... 4
5.2 ESD Ratings ... 4
5.3 Recommended Operating Conditions ... 4
5.4 Thermal Information ... 5
5.5 Power Ratings ... 5
5.6 Insulation Specifications ... 6
5.7 Safety-Related Certifications ... 7
5.8 Safety Limiting Values ... 7
5.9 Electrical Characteristics ... 8
5.10 Switching Characteristics ... 10
5.11 Insulation Characteristics Curves ... 11
5.12 Typical Characteristics ... 12
6 Parameter Measurement Information ... 17
6.1 Propagation Delay ... 17
6.2 Input Deglitch Filter ... 18
6.3 Active Miller Clamp ... 19
6.4 Under Voltage Lockout (UVLO) ... 20
6.5 Desaturation (DESAT) Protection ... 22
7 Detailed Description ... 24
7.1 Overview ... 24
7.2 Functional Block Diagram ... 25
7.3 Feature Description ... 25
7.4 Device Functional Modes ... 32
8 Applications and Implementation ... 33
8.1 Application Information ... 33
8.2 Typical Application ... 33
9 Power Supply Recommendations ... 45
10 Layout ... 46
10.1 Layout Guidelines ... 46
10.2 Layout Example ... 47
11 Device and Documentation Support ... 48
11.1 サード・パーティ製品に関する免責事項 ... 48
11.2 Documentation Support ... 48
11.3 ドキュメントの更新通知を受け取る方法 ... 48
11.4 サポート・リソース ... 48
11.5 Trademarks ... 48
11.6 静電気放電に関する注意事項 ... 48
11.7 用語集 ... 48
12 Revision History ... 49
13 Mechanical, Packaging, and Orderable Information ... 49

Copyright © 2024 Texas Instruments Incorporated

4 Pin Configuration and Functions



Not to scale

UCC21759-Q1 DW SOIC (16) Top View

表 4-1. Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
AIN	1	I	Isolated analog sensing input, parallel a small capacitor to COM for better noise immunity. If not used, short to COM
DESAT	2	I	Desaturation current protection input. If not used, short to COM
COM	3	P	Common ground reference, connecting to emitter pin for IGBT or source pin for SiC-MOSFET
OUTH	4	O	Gate driver output pull up
VDD	5	P	Positive supply rail for gate drive voltage, Bypassing a >10μF capacitor to COM to support specified gate driver source peak current capability. Place decoupling capacitor close to the pin.
OUTL	6	O	Gate driver output pull down
CLMPI	7	O	Internal active Miller clamp, connecting this pin directly to the gate of the power transistor. If not used, short to VEE
VEE	8	P	Negative supply rail for gate drive voltage. Bypassing a >10μF capacitor to COM to support specified gate driver sink peak current capability. Place decoupling capacitor close to the pin.
GND	9	P	Input power supply and logic ground reference
IN+	10	I	Non-inverting gate driver control input. Tie to VCC if unused.
IN–	11	I	Inverting gate driver control input. If not used, short to GND
RDY	12	O	Power good for VCC-GND and VDD-COM. RDY is open drain configuration and can be paralleled with other RDY signals
$\overline{\text{FLT}}$	13	O	Active low fault alarm output upon over current or short circuit detection. $\overline{\text{FLT}}$ is in open drain configuration and can be paralleled with other faults
$\overline{\text{RST}}$/EN	14	I	The $\overline{\text{RST}}$/EN serves two purposes: 1) Enable / shutdown of the output side. The FET is turned off by a regular turn-off, if terminal EN is set to low; 2) Resets the DESAT condition signaled on $\overline{\text{FLT}}$ pin. if terminal $\overline{\text{RST}}$/EN is set to low for more than 1000ns. A reset of signal $\overline{\text{FLT}}$ is asserted at the rising edge of terminal $\overline{\text{RST}}$/EN. For automatic RESET function, this pin only serves as an EN pin. Enable / shutdown of the output side. The FET is turned off by a general turn-off, if terminal EN is set to low.
VCC	15	P	Input power supply from 3V to 5.5V, bypassing a >1μF capacitor to GND. Place decoupling capacitor close to the pin.
APWM	16	O	Isolated analog sensing PWM output. If not used, leave floating or tie a parallel capacitor to GND

(1) P = Power, G = Ground, I = Input, O = Output

Copyright © 2024 Texas Instruments Incorporated

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER			MIN	MAX	UNIT
VCC	VCC – GND		–0.3	6	V
VDD	VDD – COM		–0.3	36	V
VEE	VEE – COM		–17.5	0.3	V
V_{MAX}	VDD – VEE		–0.3	36	V
IN+, IN–, $\overline{RST}$/EN		DC	GND–0.3	VCC	V
		Transient, less than 100 ns(2)	GND–5.0	VCC+5.0	V
DESAT	Reference to COM		COM–0.3	VDD+0.3	V
AIN	Reference to COM		–0.3	5	V
OUTH, OUTL , CLMPI		DC	VEE–0.3	VDD	V
		Transient, less than 100 ns(2)	VEE–5.0	VDD+5.0	V
RDY, $\overline{FLT}$, APWM			GND–0.3	VCC	V
$I_{\overline{FLT}}$, I_{RDY}	$\overline{FLT}$, and RDY pin input current			20	mA
I_{APWM}	APWM pin output current			20	mA
T_J	Junction temperature range		–40	150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Values are verified by characterization on bench.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±4000	V
		Charged-device model (CDM), per AEC Q100-011	±1500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

PARAMETER			MIN	MAX	UNIT
VCC	VCC–GND		3.0	5.5	V
VDD	VDD–COM		13	33	V
V_{MAX}	VDD–VEE		–	33	V
IN+, IN–, $\overline{RST}$/EN	Reference to GND	High level input voltage	0.7×VCC	VCC	V
		Low level input voltage	0	0.3×VCC	
AIN	Reference to COM		0.6	4.5	V
$t_{RST/EN}$	Minimum pulse width that reset the fault		800		ns
T_A	Ambient Temperature		–40	125	°C
T_J	Junction temperature		–40	150	°C

Copyright © 2024 Texas Instruments Incorporated

5.4 Thermal Information

THERMAL METRIC[1]		UCC21759-Q1 DW (SOIC) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	68.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	27.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	32.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	32.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Power Ratings

PARAMETER		TEST CONDITIONS	Value	UNIT
P_D	Maximum power dissipation (both sides)	VCC = 5V, VDD-COM = 20V, COM-VEE = 5V, IN+/- = 5V, 150kHz, 50% Duty Cycle for 10nF load, T_a=25ºC	985	mW
P_{D1}	Maximum power dissipation by transmitter side		20	mW
P_{D2}	Maximum power dissipation by receiver side		965	mW

Copyright © 2024 Texas Instruments Incorporated

5.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest terminal-to-terminal distance through air	> 8	mm
CPG	External creepage(1)	Shortest terminal-to-terminal distance across the package surface	> 8	mm
DTI	Distance through the insulation	Minimum internal gap (Internal clearance) of the double insulation (2 × 0.0085 mm)	> 17	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material group	According to IEC 60664–1	I	
	Overvoltage Category per IEC 60664–1	Rated mains voltage ≤ 300 V_{RMS}	I-IV	
		Rated mains voltage ≤ 600 V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17):2021-10(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	900	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave) Time dependent dielectric breakdown (TDDB) test	636	V_{RMS}
		DC voltage	900	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	V_{TEST}=V_{IOTM}, t = 60 s (qualification test)	4242	V_{PK}
		V_{TEST}=1.2 x V_{IOTM}, t = 1 s (100% production test)		
V_{IOSM}	Maximum surge isolation voltage(3)	Test method per IEC 62368-1, 1.2/50 µs waveform, V_{TEST} = 1.6 × V_{IOSM} = 9600 V_{PK} (qualification)	6000	V_{PK}
q_{pd}	Apparent charge(4)	Method a: After I/O safety test subgroup 2/3, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.2 × V_{IORM}, t_m = 10 s	≤ 5	pC
		Method a: After environmental tests subgroup 1, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.6 × V_{IORM}, t_m = 10 s	≤ 5	
		Method b1: At routine test (100% production) and preconditioning (type test) V_{ini} = V_{IOTM}, t_{ini} = 1 s; $V_{pd(m)}$ = 1.875 × V_{IORM} = 3977 V_{PK}, t_m = 1 s	≤ 5	
C_{IO}	Barrier capacitance, input to output(5)	V_{IO} = 0.5 sin (2πft), f = 1 MHz	~ 1	pF
R_{IO}	Insulation resistance, input to output(5)	V_{IO} = 500 V, T_A = 25°C	≥ 10^{12}	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	≥ 10^{11}	
		V_{IO} = 500 V at T_S = 150°C	≥ 10^{9}	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	V_{TEST} = V_{ISO} = 3000 V_{RMS}, t = 60 s (qualification); V_{TEST} = 1.2 × V_{ISO}, t = 1 s (100% production)	3000	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves and ribs on the PCB are used to help increase these specifications.
(2) This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-terminal device

Copyright © 2024 Texas Instruments Incorporated

5.7 Safety-Related Certifications

VDE
Certified according to DIN EN IEC 60747-17 (VDE 0884-17):2021-10; EN IEC 60747-17:2020+AC:2021
Basic insulation Maximum transient isolation voltage, 4242 V_{PK}; Maximum repetitive peak isolation voltage, 900 V_{PK}; Maximum surge isolation voltage, 6000 V_{PK}
Certificate number: 40047657

5.8 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ =68.3°C/W, V_{DD} = 15V, V_{EE}=-5V, T_J = 150°C, T_A = 25°C			61	mA
		$R_{\theta JA}$ =68.3°C/W, V_{DD} = 20V, V_{EE}=-5V, T_J = 150°C, T_A = 25°C			49	
P_S	Safety input, output, or total power	$R_{\theta JA}$ =68.3°C/W, V_{DD} = 20V, V_{EE}=-5V, T_J = 150°C, T_A = 25°C			1220	mW
T_S	Safety temperature				150	°C

(1) The safety-limiting constraint is the maximum junction temperature specified in the data sheet. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *セクション 5.4* table is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

Copyright © 2024 Texas Instruments Incorporated

5.9 Electrical Characteristics

VCC = 3.3 V or 5.0 V, 1-µF capacitor from VCC to GND, VDD – COM = 20 V, 18 V or 15 V, COM – VEE = 0 V, 5 V, 8 V or 15 V, C_L = 100 pF, –40°C < T_J < 150°C (unless otherwise noted)(1) (2).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VCC UVLO THRESHOLD AND DELAY						
V_{VCC_ON}	VCC–GND		2.55	2.7	2.85	V
V_{VCC_OFF}			2.35	2.5	2.65	
V_{VCC_HYS}				0.2		
t_{VCCFIL}	VCC UVLO Deglitch time			10		µs
$t_{VCC+ to OUT}$	VCC UVLO on delay to output high	IN+ = VCC, IN– = GND	28	37.8	50	
$t_{VCC– to OUT}$	VCC UVLO off delay to output low		5	10	15	
$t_{VCC+ to RDY}$	VCC UVLO on delay to RDY high	$\overline{RST}$/EN = VCC	30	37.8	50	
$t_{VCC– to RDY}$	VCC UVLO off delay to RDY low		5	10	15	
VDD UVLO THRESHOLD AND DELAY						
V_{VDD_ON}	VDD–COM		10.5	12.0	12.8	V
V_{VDD_OFF}			9.9	10.7	11.8	
V_{VDD_HYS}				0.8		
t_{VDDFIL}	VDD UVLO Deglitch time			5		µs
$t_{VDD+ to OUT}$	VDD UVLO on delay to output high	IN+ = VCC, IN– = GND	2	5	8	
$t_{VDD– to OUT}$	VDD UVLO off delay to output low			5	10	
$t_{VDD+ to RDY}$	VDD UVLO on delay to RDY high	$\overline{RST}$/EN = $\overline{FLT}$=High		10	15	
$t_{VDD– to RDY}$	VDD UVLO off delay to RDY low			10	15	
VCC, VDD QUIESCENT CURRENT						
I_{VCCQ}	VCC quiescent current	OUT(H) = High, f_S = 0Hz, AIN=2V	2.5	3	4	mA
		OUT(L) = Low, f_S = 0Hz, AIN=2V	1.45	2	2.75	
I_{VDDQ}	VDD quiescent current	OUT(H) = High, f_S = 0Hz, AIN=2V	3.6	4	5.9	mA
		OUT(L) = Low, f_S = 0Hz, AIN=2V	3.1	3.7	5.3	
LOGIC INPUTS — IN+, IN– and $\overline{RST}$/EN						
V_{INH}	Input high threshold	V_{CC}=3.3V		1.85	2.31	V
V_{INL}	Input low threshold	V_{CC}=3.3V	0.99	1.52		V
V_{INHYS}	Input threshold hysteresis	V_{CC}=3.3V		0.33		V
I_{IH}	Input high level input leakage current	V_{IN} = VCC		90		µA
I_{IL}	Input low level input leakage	V_{IN} = GND		–90		µA
R_{IND}	Input pins pull down resistance	see セクション 7 for more information		55		kΩ
R_{INU}	Input pins pull up resistance	see セクション 7 for more information		55		
T_{INFIL}	IN+, IN– and $\overline{RST}$/EN deglitch (ON and OFF) filter time	f_S = 50kHz	28	40	60	ns
T_{RSTFIL}	Deglitch filter time to reset /FLT		400	650	800	ns
GATE DRIVER STAGE						
I_{OUT}, I_{OUTH}	Peak source current	C_L=0.18µF, f_S=1kHz		10		A
I_{OUT}, I_{OUTL}	Peak sink current			10		A
R_{OUTH} (3)	Output pull-up resistance	I_{OUT} = –0.1A		2.5		Ω
R_{OUTL}	Output pull-down resistance	I_{OUT} = 0.1A		0.3		Ω
V_{OUTH}	High level output voltage	I_{OUT} = –0.2A, V_{DD}=18V		17.5		V
V_{OUTL}	Low level output voltage	I_{OUT} = 0.2A		60		mV

Copyright © 2024 Texas Instruments Incorporated

5.9 Electrical Characteristics (続き)

VCC = 3.3 V or 5.0 V, 1-µF capacitor from VCC to GND, VDD – COM = 20 V, 18 V or 15 V, COM – VEE = 0 V, 5 V, 8 V or 15 V, C_L = 100 pF, –40°C < T_J < 150°C (unless otherwise noted)(1) (2).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ACTIVE PULLDOWN						
V_{OUTPD}	Output active pull down on OUT, OUTL	I_{OUTL} or I_{OUT} = 0.1×$I_{OUT(L)(tpy)}$, VDD=OPEN, VEE=COM	1.5	2	2.5	V
INTERNAL ACTIVE MILLER CLAMP						
V_{CLMPTH}	Miller clamp threshold voltage	Reference to VEE	1.5	2.0	2.5	V
V_{CLMPI}	Output low clamp voltage	I_{CLMPI} = 1A		VEE + 0.5		V
I_{CLMPI}	Output low clamp current	V_{CLMPI} = 0V, VEE = –2.5V		4		A
R_{CLMPI}	Miller clamp pull down resistance	I_{CLMPI} = 0.2A		0.6		Ω
t_{DCLMPI}	Miller clamp ON delay time	C_L = 1.8nF		15	50	ns
SHORT CIRCUIT CLAMPING						
$V_{CLP-OUT(H)}$	V_{OUT}–VDD, V_{OUTH}–VDD	OUT = Low, $I_{OUT(H)}$ = 500mA, t_{CLP}=10us		0.9		V
$V_{CLP-OUT(L)}$	V_{OUT}–VDD, V_{OUTL}–VDD	OUT = High, $I_{OUT(L)}$ = 500mA, t_{CLP}=10us		1.8		V
$V_{CLP-CLMPI}$	V_{CLMPI}–VDD	OUT = High, I_{CLMPI} = 20mA, t_{CLP}=10us		1.0		V
DESAT PROTECTION						
I_{CHG}	Blanking capacitor charge current	V_{DESAT} = 2.0V	430	500	570	µA
I_{DCHG}	Blanking capacitor discharge current	V_{DESAT} = 6.0V	10	15		mA
V_{DESAT}	Detection Threshold		8.5	9.15	9.8	V
$t_{DESATLEB}$	Leading edge blank time			200		ns
$t_{DESATFIL}$	DESAT deglitch filter		50	140	230	ns
$t_{DESATOFF}$	DESAT propagation delay to OUT(L) 90%		150	200	300	ns
$t_{DESATFLT}$	DESAT to $\overline{FLT}$ low delay		400	580	750	ns
INTERNAL SOFT TURN-OFF						
I_{STO}	Soft turn-off current on fault conditions	V_{DD}-V_{EE} = 20V, V_{OUTL}-COM = 8V	250	400	570	mA
ISOLATED TEMPERATURE SENSE AND MONITOR (AIN–APWM)						
V_{AIN}	Analog sensing voltage range		0.6		4.5	V
I_{AIN}	Internal current source	V_{AIN}=2.5V, -40°C< T_J< 150°C	196	203	209	µA
f_{APWM}	APWM output frequency	V_{AIN}=2.5V	380	400	420	kHz
BW_{AIN}	AIN–APWM bandwidth			10		kHz
D_{APWM}	APWM Dutycycle	V_{AIN} = 0.6V	86.5	88	89.5	%
		V_{AIN} = 2.5V	48.5	50	51.5	
		V_{AIN} = 4.5V	7.5	10	11.5	
$\overline{FLT}$ AND RDY REPORTING						
t_{RDYHLD}	VDD UVLO RDY low minimum holding time		0.55		1	ms
$t_{FLTMUTE}$	Output mute time on fault	Reset fault through $\overline{RST}$/EN	0.55		1	ms
R_{ODON}	Open drain output on resistance	I_{ODON} = 5mA		30		Ω
V_{ODL}	Open drain low output voltage	I_{ODON} = 5mA			0.3	V
COMMON MODE TRANSIENT IMMUNITY						
CMTI	Common-mode transient immunity		150			V/ns

(1) Current are positive into and negative out of the specified terminal.
(2) All voltages are referenced to COM unless otherwise notified.
(3) For internal PMOS only. Refer to セクション 7.3.2 for effective pull-up resistance.

Copyright © 2024 Texas Instruments Incorporated

5.10 Switching Characteristics

VCC=5.0V, 1uF capacitor from VCC to GND, VDD–COM=20V, 18V or 15V, COM–VEE = 3V, 5V or 8V, C_L=100pF, –40°C<T_J<150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PDHL}	Propagation delay time – High to Low		60	90	130	ns
t_{PDLH}	Propagation delay time – Low to High		60	90	130	
PWD	Pulse width distortion $\lvert t_{PDHL} - t_{PDLH} \rvert$				30	
t_{sk-pp}	Part to Part skew	Rising or Falling Propagation Delay			30	
t_r	Driver output rise time	C_L=10nF		33		
t_f	Driver output fall time	C_L=10nF		27		
f_{MAX}	Maximum switching frequency				1	MHz

Copyright © 2024 Texas Instruments Incorporated

5.11 Insulation Characteristics Curves

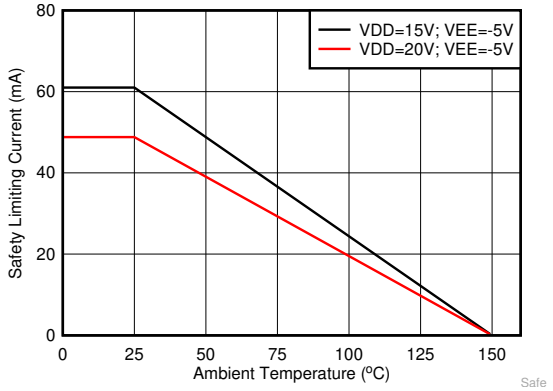


図 5-1. Thermal Derating Curve for Limiting Current per VDE

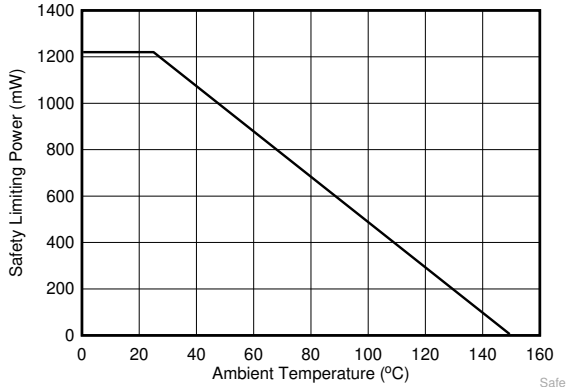


図 5-2. Thermal Derating Curve for Limiting Power per VDE

5.12 Typical Characteristics

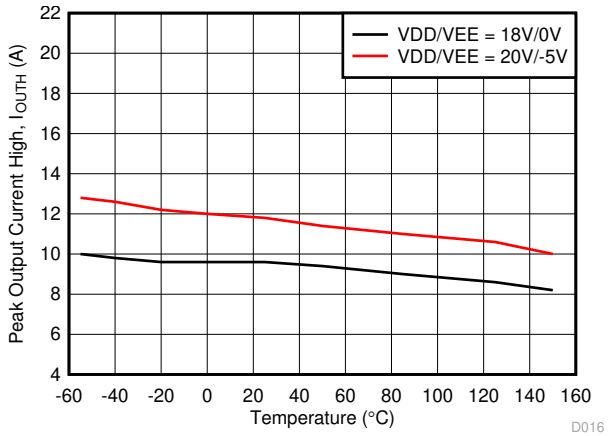


図 5-3. Output High Drive Current vs Temperature

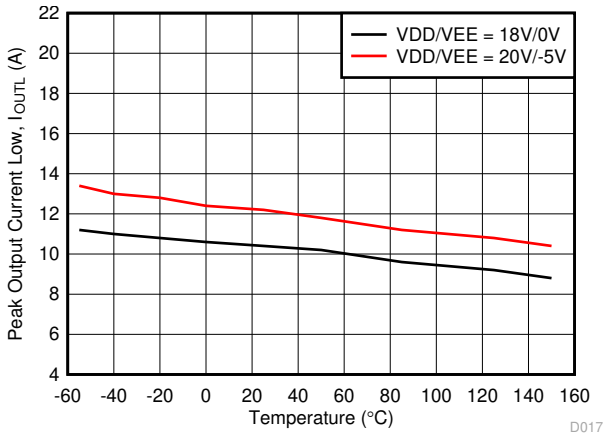


図 5-4. Output Low Driver Current vs Temperature

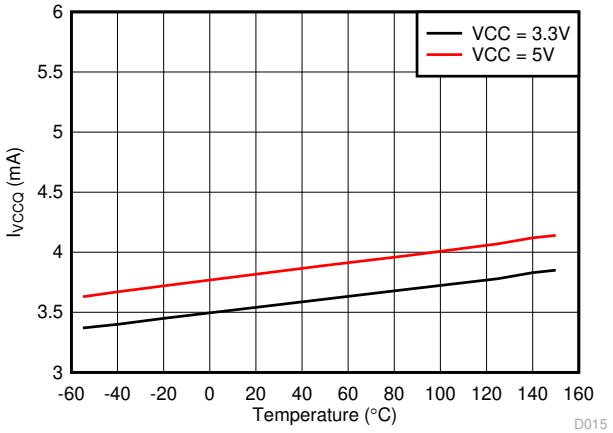


図 5-5. I_{VCCQ} Supply Current vs Temperature

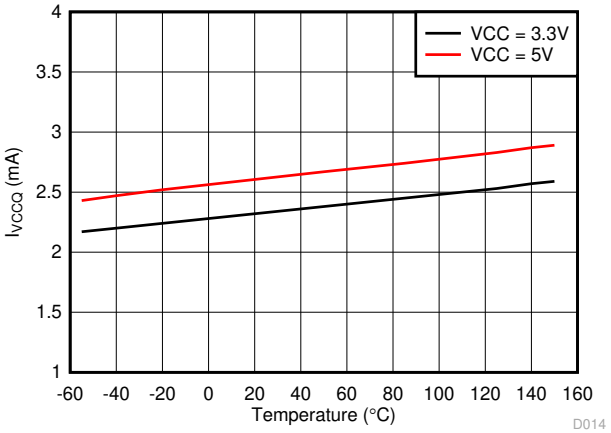


図 5-6. I_{VCCQ} Supply Current vs Temperature

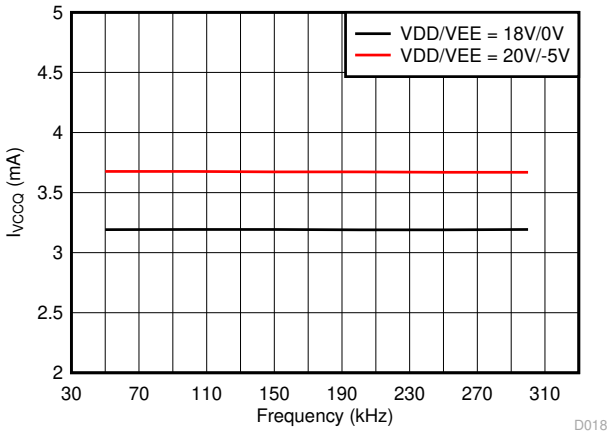


図 5-7. I_{VCCQ} Supply Current vs Input Frequency

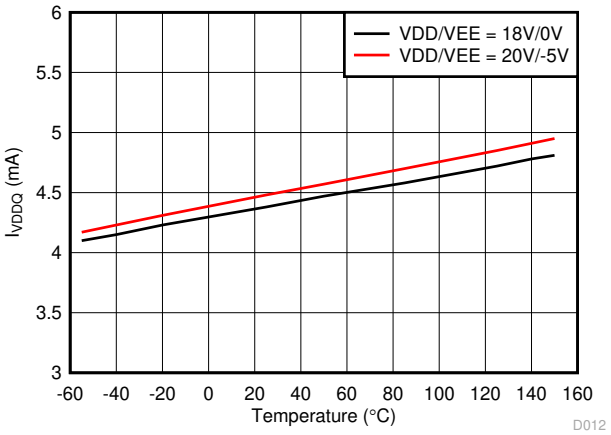
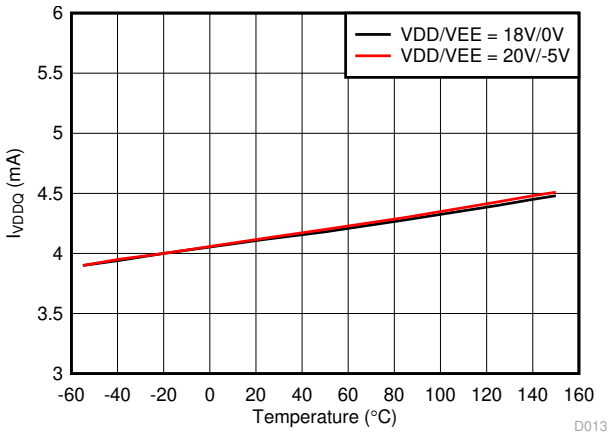


図 5-8. I_{VDDQ} Supply Current vs Temperature

Copyright © 2024 Texas Instruments Incorporated

5.12 Typical Characteristics (continued)



IN+ = Low IN- = Low

図 5-9. I_{VDDQ} Supply Current vs Temperature

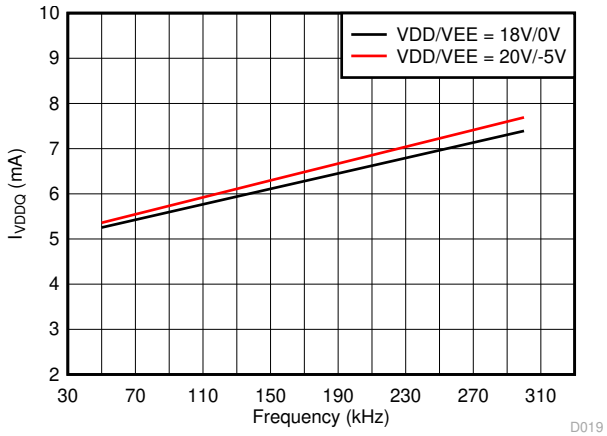


図 5-10. I_{VDDQ} Supply Current vs Input Frequency

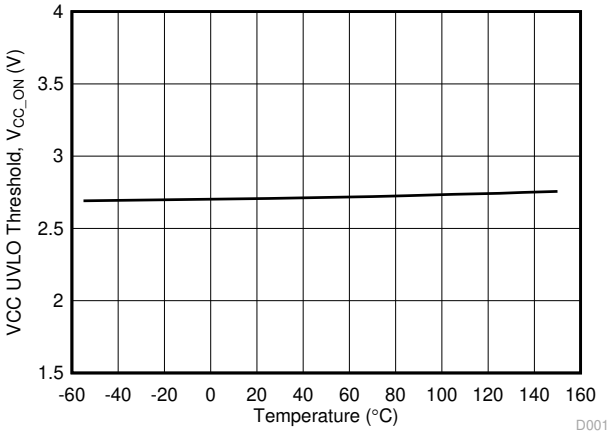


図 5-11. VCC UVLO vs Temperature

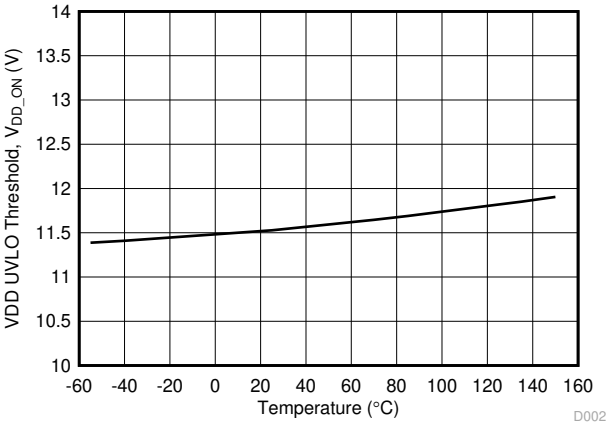
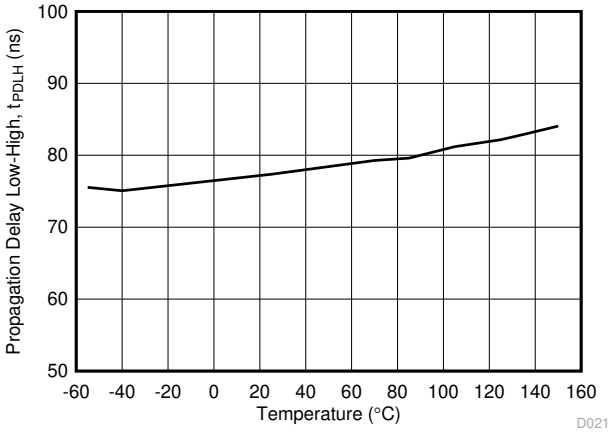
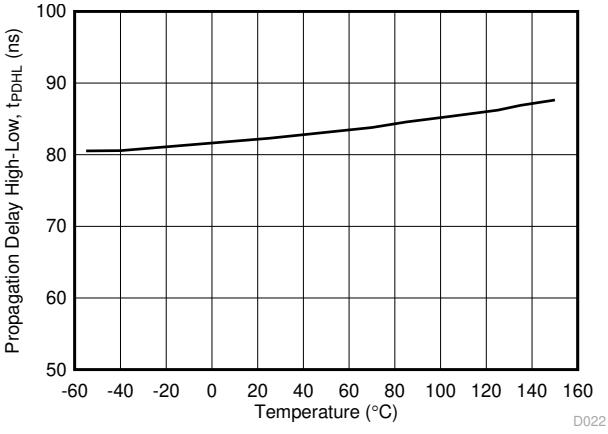


図 5-12. VDD UVLO vs Temperature



V_{CC} = 3.3V V_{DD}=18V C_L = 100pF
R_{ON} = 0Ω R_{OFF} = 0Ω

図 5-13. Propagation Delay t_{PDLH} vs Temperature

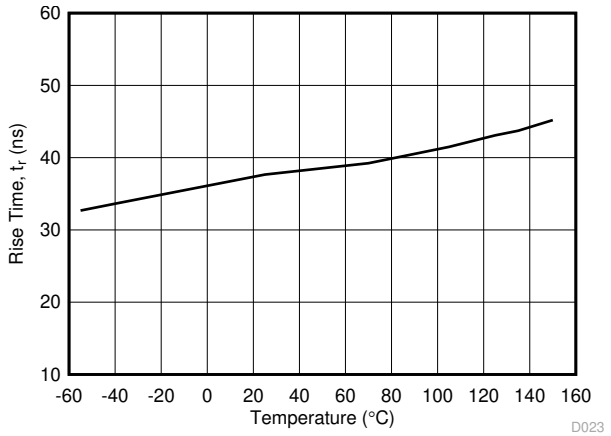


V_{CC} = 3.3V V_{DD}=18V C_L = 100pF
R_{ON} = 0Ω R_{OFF} = 0Ω

図 5-14. Propagation Delay t_{PDHL} vs Temperature

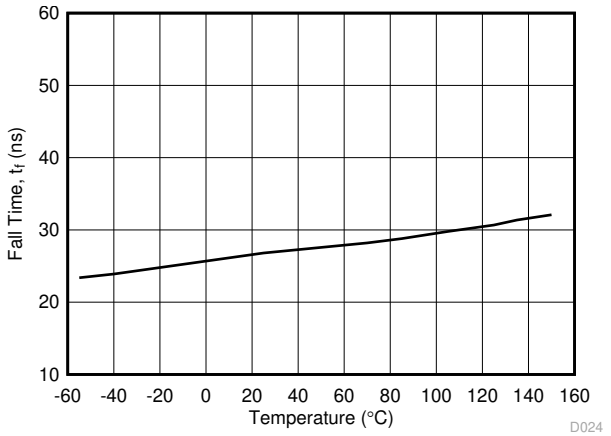
Copyright © 2024 Texas Instruments Incorporated

5.12 Typical Characteristics (continued)



V_{CC} = 3.3V V_{DD}=18V C_L = 10nF
R_{ON} = 0Ω R_{OFF} = 0Ω

図 5-15. t_r Rise Time vs Temperature



V_{CC} = 3.3V V_{DD}=18V C_L = 10nF
R_{ON} = 0Ω R_{OFF} = 0Ω

図 5-16. t_f Fall Time vs Temperature

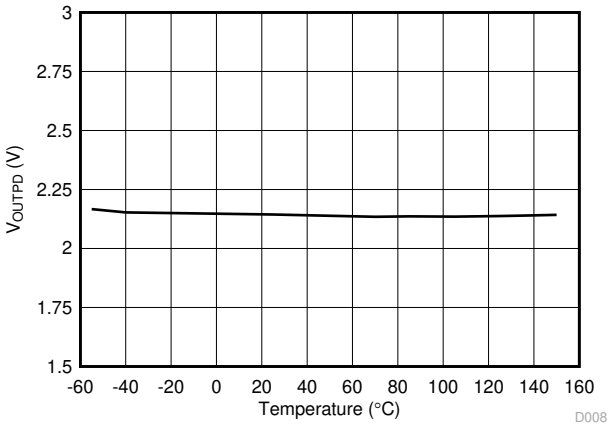


図 5-17. V_{OUTPD} Output Active Pulldown Voltage vs Temperature

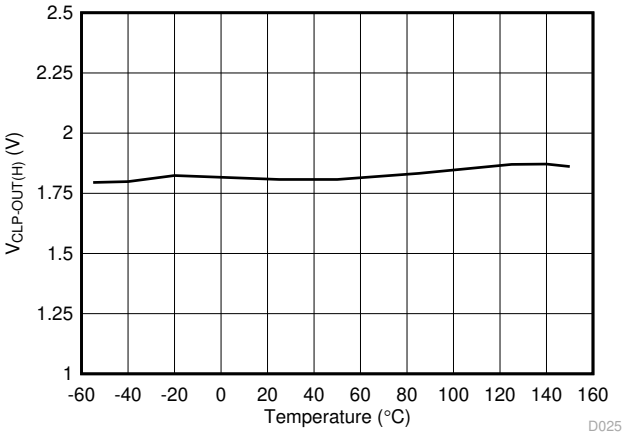


図 5-18. $V_{CLP-OUT(H)}$ Short Circuit Clamping Voltage vs Temperature

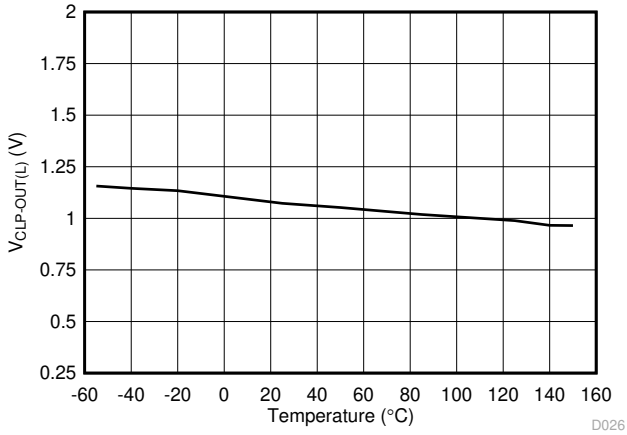


図 5-19. $V_{CLP-OUT(L)}$ Short Circuit Clamping Voltage vs Temperature

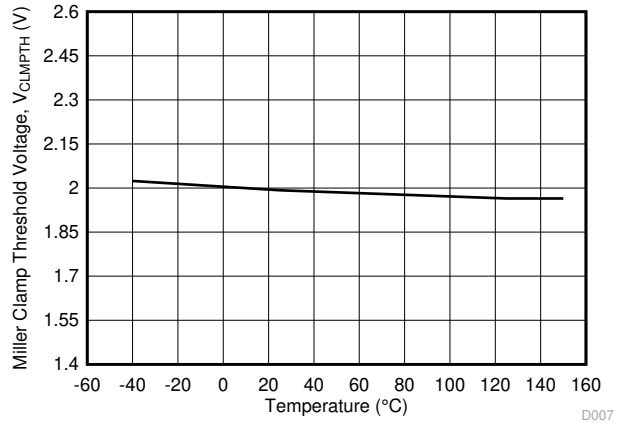


図 5-20. V_{CLMPTH} Miller Clamp Threshold Voltage vs Temperature

Copyright © 2024 Texas Instruments Incorporated

5.12 Typical Characteristics (continued)

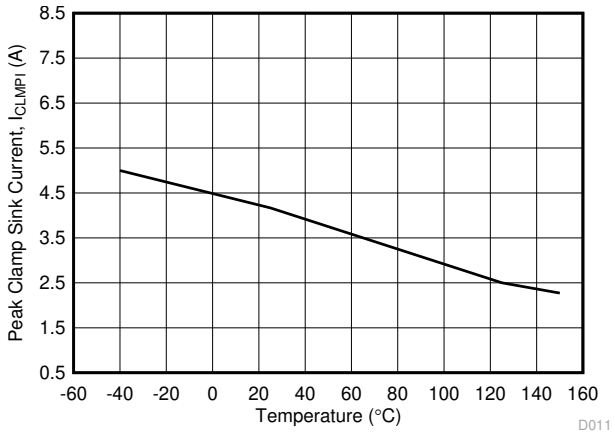


図 5-21. I_{CLMPI} Miller Clamp Sink Current vs Temperature

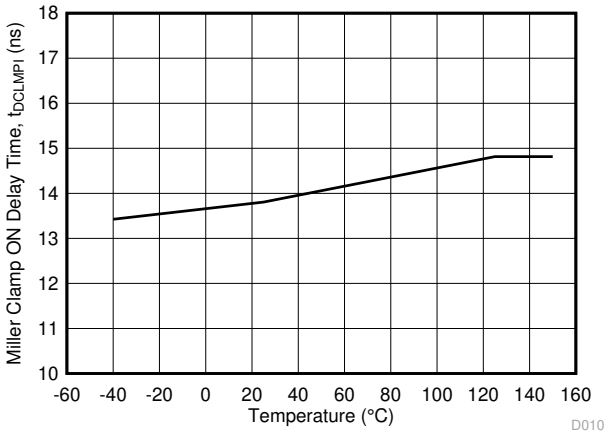


図 5-22. t_{DCLMPI} Miller Clamp ON Delay Time vs Temperature

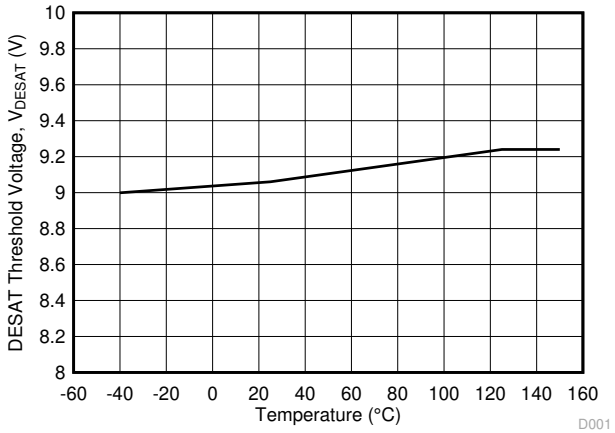


図 5-23. V_{DESAT} DESAT Threshold Voltage vs Temperature

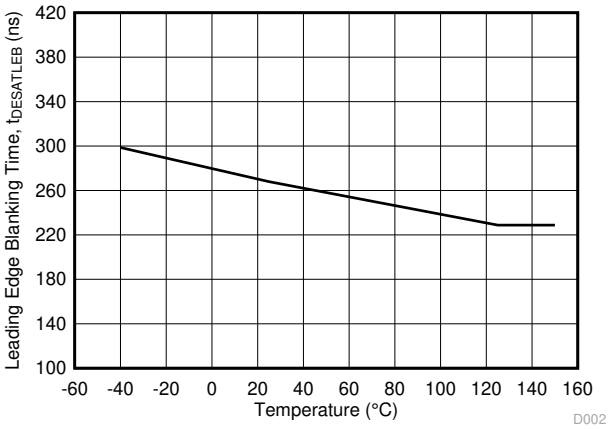


図 5-24. $t_{DESATLEB}$ DESAT Leading Edge Blanking Time vs Temperature

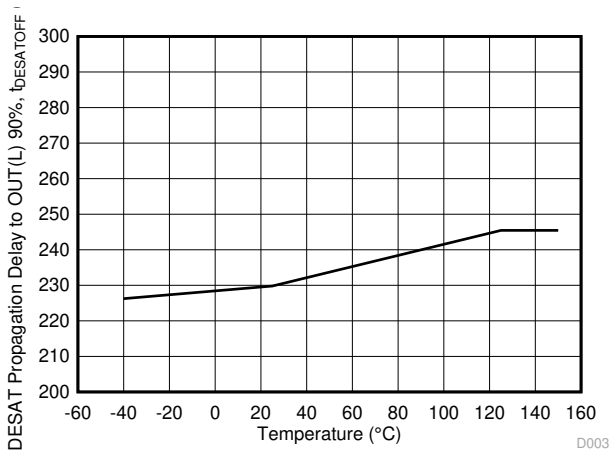


図 5-25. $t_{DESATOFF}$ DESAT Propagation Delay to OUT(L) 90% vs Temperature

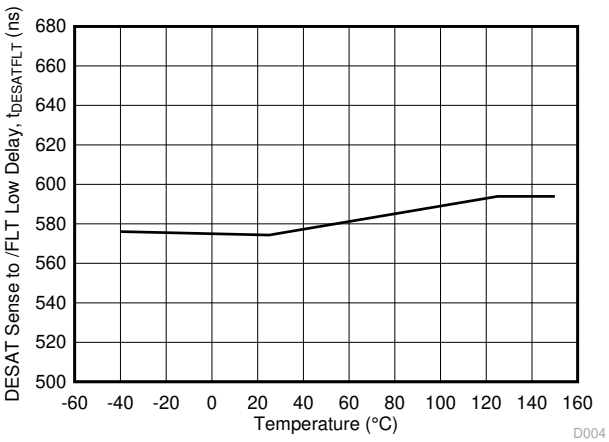


図 5-26. $t_{DESATFLT}$ DESAT Sense to /FLT Low Delay Time vs Temperature

Copyright © 2024 Texas Instruments Incorporated

5.12 Typical Characteristics (continued)

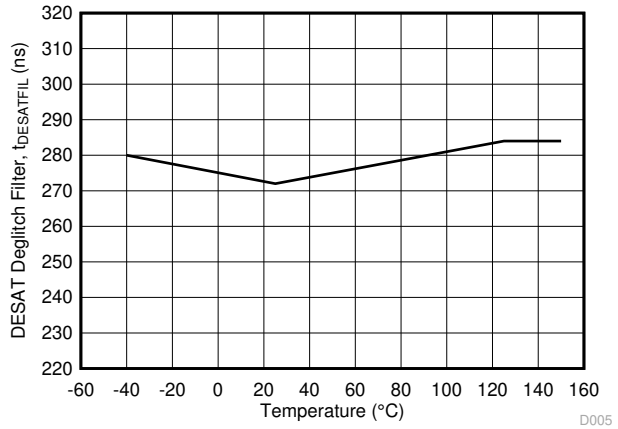


図 5-27. $t_{DESATFIL}$ DESAT Deglitch Filter vs Temperature

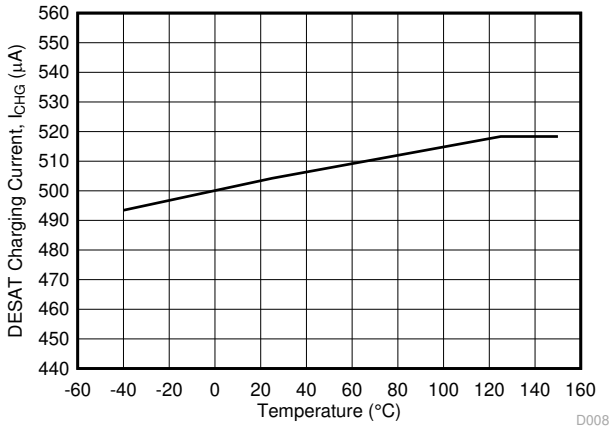


図 5-28. I_{CHG} DESAT Charging Current vs Temperature

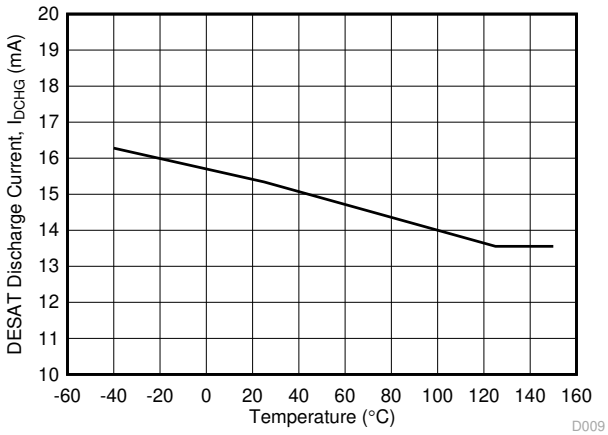


図 5-29. I_{DCHG} DESAT Discharge Current vs Temperature

Copyright © 2024 Texas Instruments Incorporated

6 Parameter Measurement Information

6.1 Propagation Delay

6.1.1 Non-Inverting and Inverting Propagation Delay

図 6-1 shows the propagation delay measurement for non-inverting configurations. 図 6-2 shows the propagation delay measurement with the inverting configurations.

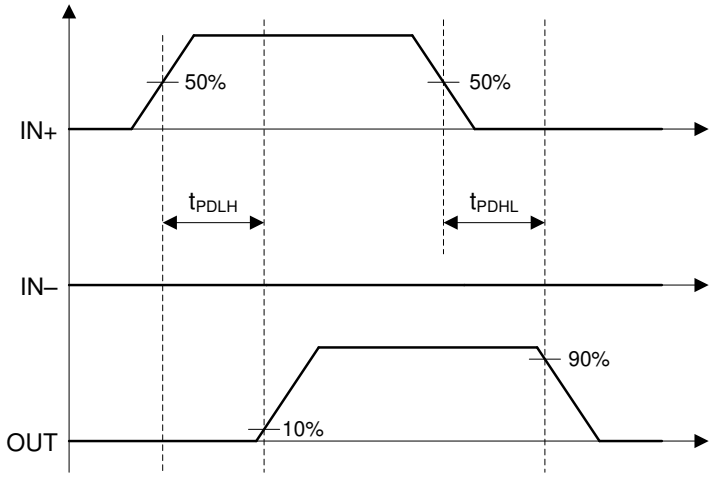


図 6-1. Non-inverting Logic Propagation Delay Measurement

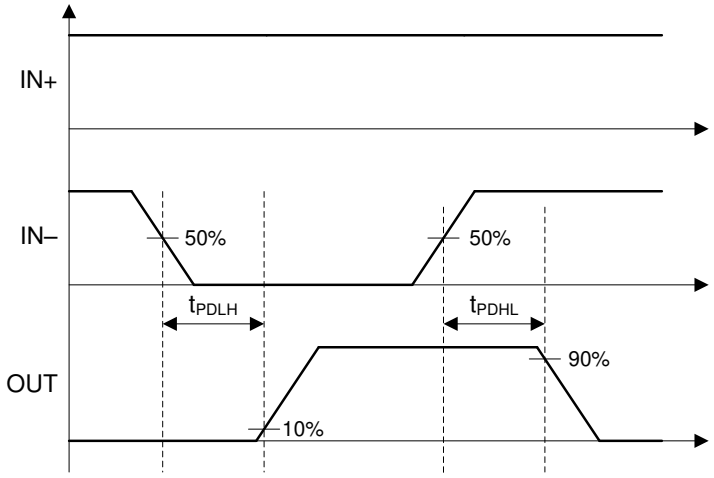


図 6-2. Inverting Logic Propagation Delay Measurement

6.2 Input Deglitch Filter

In order to increase the robustness of gate driver over noise transient and accidental small pulses on the input pins, i.e. IN+, IN–, $\overline{RST}$/EN, a 40ns deglitch filter is designed to filter out the transients and make sure there is no faulty output responses or accidental driver malfunctions. When the IN+ or IN– PWM pulse is smaller than the input deglitch filter width, T_{INFIL}, there will be no responses on OUT drive signal. 図 6-3 and 図 6-4 shows the IN+ pin ON and OFF pulse deglitch filter effect. 図 6-5 and 図 6-6 shows the IN– pin ON and OFF pulse deglitch filter effect.

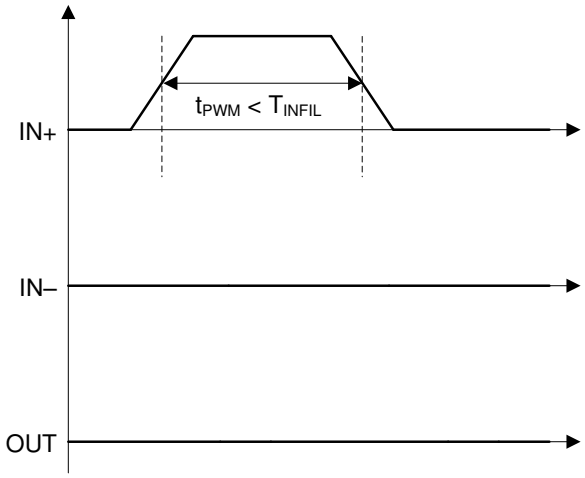


図 6-3. IN+ ON Deglitch Filter

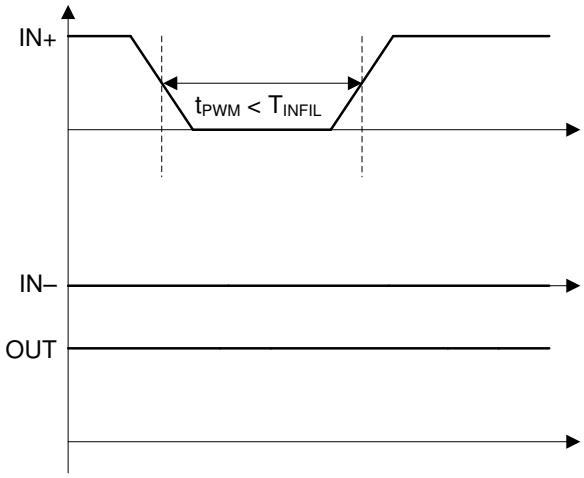


図 6-4. IN+ OFF Deglitch Filter

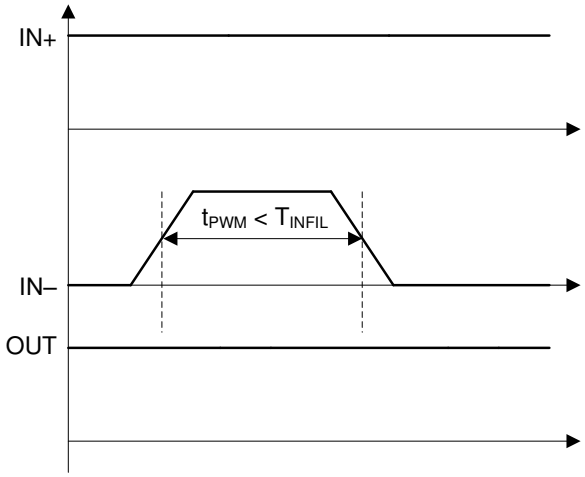


図 6-5. IN– ON Deglitch Filter

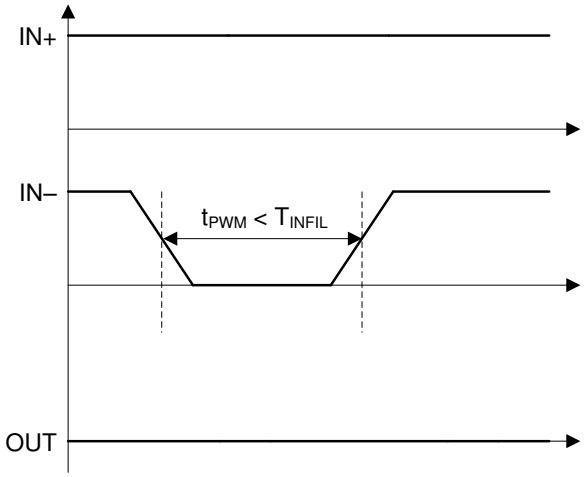


図 6-6. IN– OFF Deglitch Filter

Copyright © 2024 Texas Instruments Incorporated

6.3 Active Miller Clamp

6.3.1 Internal On-chip Active Miller Clamp

For gate driver application with unipolar bias supply or bipolar supply with small negative turn-off voltage, active Miller clamp can help add a additional low impedance path to bypass the Miller current and prevent the unintentional turn-on through the Miller capacitance. 図 6-7 shows the timing diagram for on-chip internal Miller clamp function.

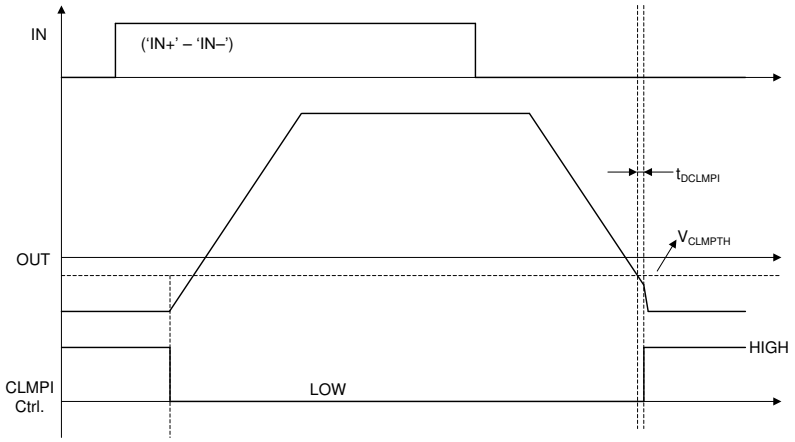


図 6-7. Timing Diagram for Internal Active Miller Clamp Function

6.4 Under Voltage Lockout (UVLO)

UVLO is one of the key protection features designed to protect the system in case of bias supply failures on VCC — primary side power supply, and VDD — secondary side power supply.

6.4.1 VCC UVLO

The VCC UVLO protection details are discussed in this section. 図 6-8 shows the timing diagram illustrating the definition of UVLO ON/OFF threshold, deglitch filter, response time, RDY and AIN–APWM.

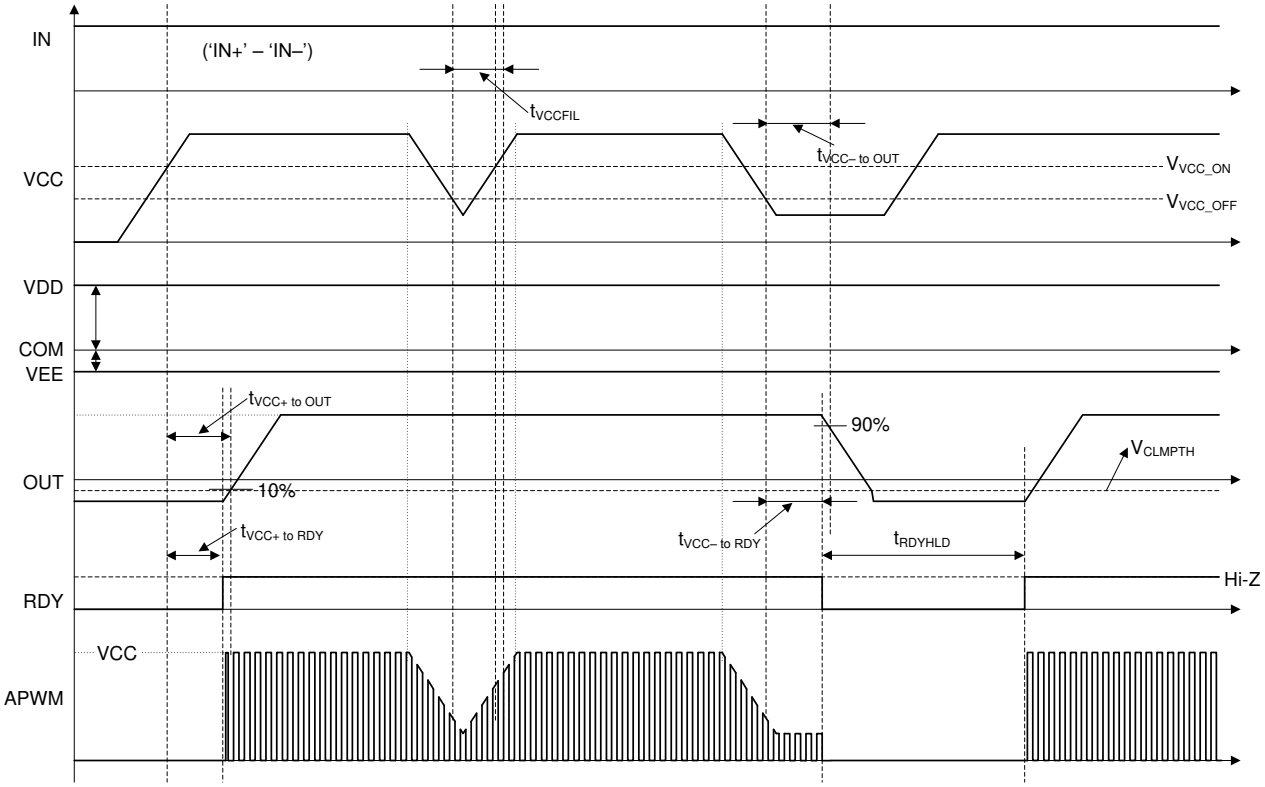


図 6-8. VCC UVLO Protection Timing Diagram

Copyright © 2024 Texas Instruments Incorporated

6.4.2 VDD UVLO

The VDD UVLO protection details are discussed in this section. 図 6-9 shows the timing diagram illustrating the definition of UVLO ON/OFF threshold, deglitch filter, response time, RDY and AIN–APWM.

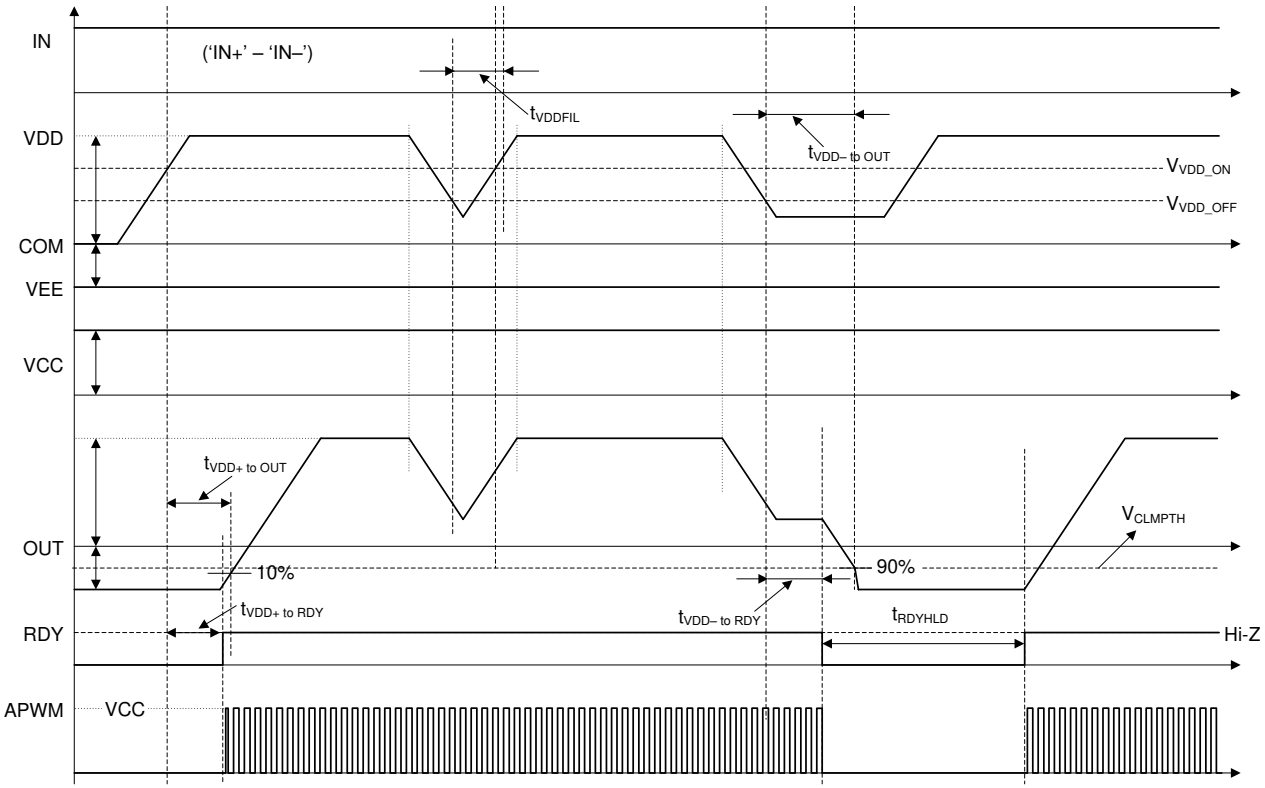


図 6-9. VDD UVLO Protection Timing Diagram

6.5 Desaturation (DESAT) Protection

6.5.1 DESAT Protection with Soft Turn-OFF

DESAT function is used to detect V_{DS} for SiC-MOSFETs or V_{CE} for IGBTs under over current conditions. 図 6-10 shows the timing diagram of DESAT operation with soft turn-off during the turning on transition.

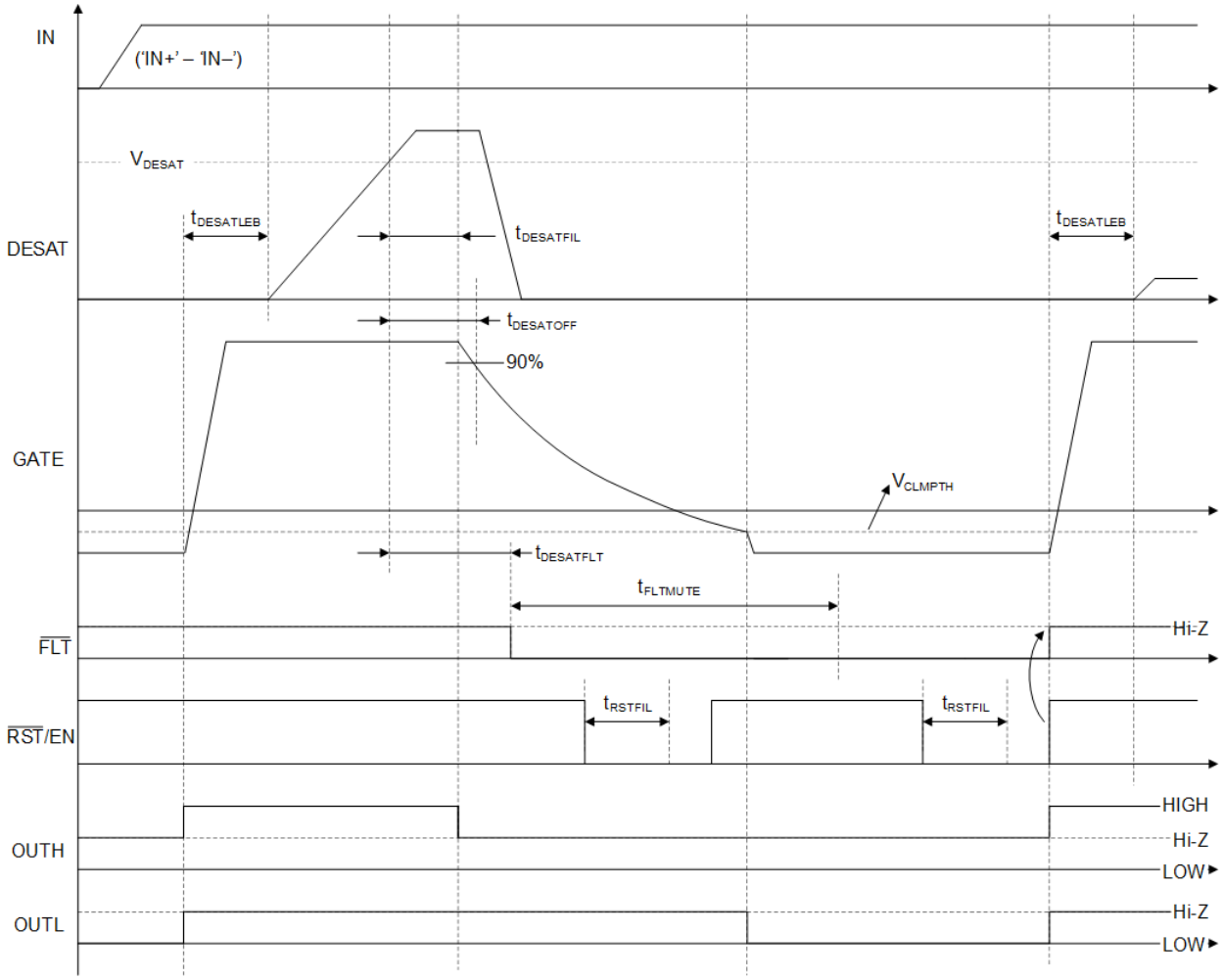


図 6-10. DESAT Protection with Soft Turn-OFF During Turn-on Transition

Copyright © 2024 Texas Instruments Incorporated

図 6-11 shows the timing diagram of DESAT protection while the power device is already turned on.

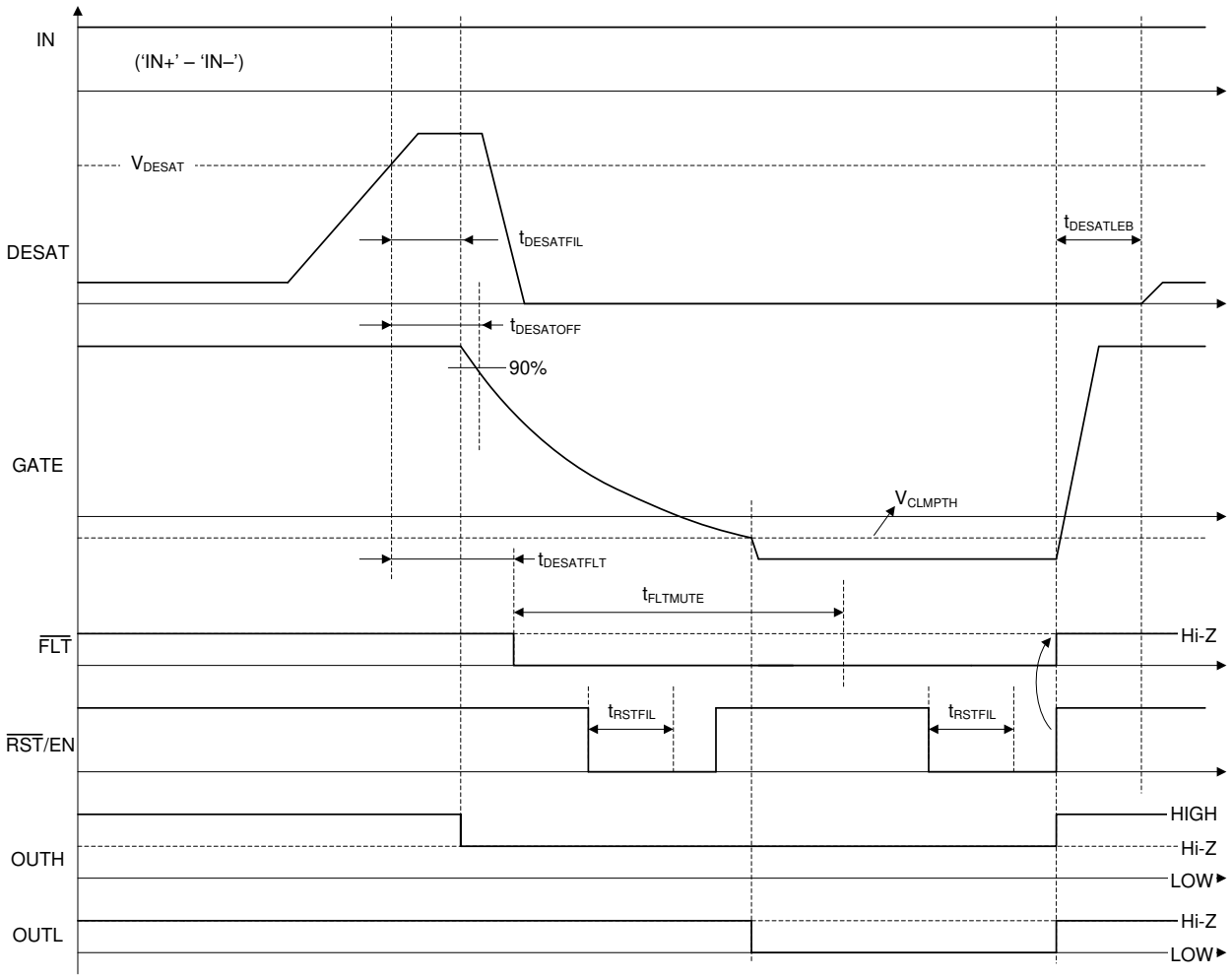


図 6-11. DESAT Protection with Soft Turn-OFF While Power Device is ON

7 Detailed Description

7.1 Overview

The UCC21759-Q1 device is an advanced isolated gate driver with state-of-art protection and sensing features for SiC MOSFETs and IGBTs. The device can support up to 900V DC operating voltage based on SiC MOSFETs and IGBTs, and can be used to above 10kW applications such as HEV/EV traction inverter, motor drive, on-board and off-board battery charger, solar inverter, etc. The galvanic isolation is implemented by the capacitive isolation technology, which can realize a reliable basic isolation between the low voltage DSP/MCU and high voltage side.

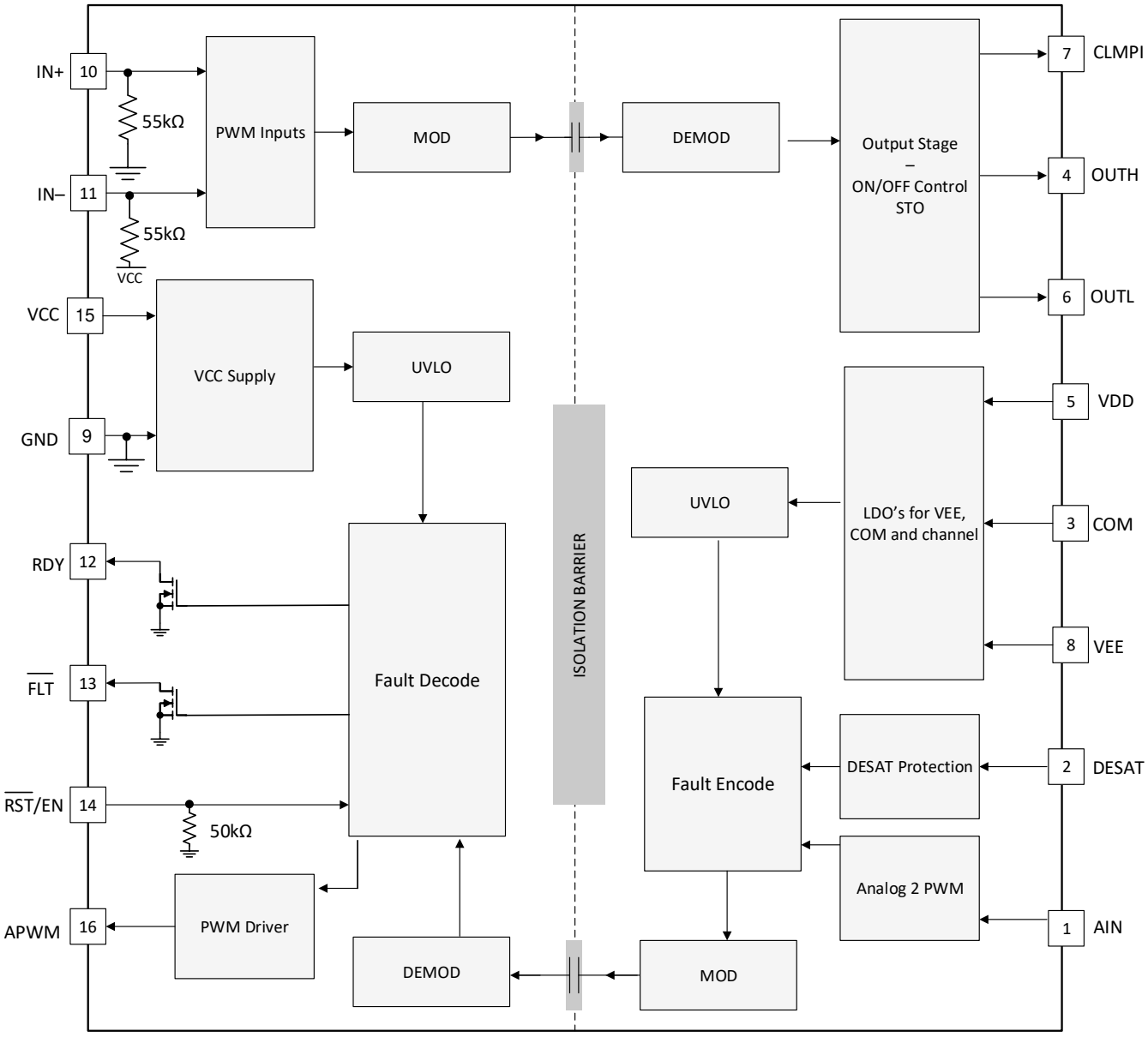
The ±10A peak sink and source current of UCC21759-Q1 can drive the SiC MOSFET modules and IGBT modules directly without an extra buffer. The driver can also be used to drive higher power modules or parallel modules with external buffer stage. The device can support up to 636-V_{RMS} working voltage with longer than 40 years isolation barrier life, 6-kV_{PK} surge immunity. The strong drive strength helps to switch the device fast and reduce the switching loss, and the 150V/ns minimum CMTI guarantees the reliability of the system with fast switching speed. The small propagation delay and part-to-part skew can minimize the deadtime setting, so the conduction loss can be reduced.

The device includes extensive protection and monitor features to increase the reliability and robustness of the SiC MOSFET and IGBT based systems. The 12V output side power supply UVLO is suitable for switches with gate voltage ≥ 15V. The active Miller clamp feature prevents the false turn on causing by Miller capacitance during fast switching. The device has the state-of-art DESAT detection time, and fault reporting function to the low voltage side DSP/MCU. The soft turn off is triggered when the DESAT fault is detected, minimizing the short circuit energy while reducing the overshoot voltage on the switches.

The isolated analog to PWM sensor can be used as switch temperature sensing, DC bus voltage sensing, auxiliary power supply sensing, etc. The PWM signal can be fed directly to DSP/MCU or through a low-pass-filter as an analog signal.

Copyright © 2024 Texas Instruments Incorporated

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Power Supply

The input side power supply VCC can support a wide voltage range from 3V to 5.5V. The device supports both unipolar and bipolar power supply on the output side, with a wide range from 13V to 33V from VDD to VEE. The negative power supply with respect to switch source or emitter is usually adopted to avoid false turn on when the other switch in the phase leg is turned on. The negative voltage is especially important for SiC MOSFET due to its fast switching speed.

7.3.2 Driver Stage

UCC21759-Q1 has ±10A peak drive strength and is suitable for high power applications. The high drive strength can drive a SiC MOSFET module, IGBT module or paralleled discrete devices directly without extra buffer stage. UCC21759-Q1 can also be used to drive higher power modules or parallel modules with extra buffer stage. Regardless of the values of VDD, the peak sink and source current can be kept at 10A. The driver features an

Copyright © 2024 Texas Instruments Incorporated

important safety function wherein, when the input pins are in floating condition, the OUTH/OUTL is held in LOW state. The split output of the driver stage is depicted in 図 7-1. The driver has rail-to-rail output by implementing a hybrid pull-up structure with a P-Channel MOSFET in parallel with an N-Channel MOSFET, and an N-Channel MOSFET to pulldown. The pull-up NMOS is the same as the pull down NMOS, so the on resistance R_{NMOS} is the same as R_{OL}. The hybrid pull-up structure delivers the highest peak-source current when it is most needed, during the Miller plateau region of the power semiconductor turn-on transient. The R_{OH} in represents the on-resistance of the pull-up P-Channel MOSFET. However, the effective pull-up resistance is much smaller than R_{OH}. Since the pull-up N-Channel MOSFET has much smaller on-resistance than the P-Channel MOSFET, the pull-up N-Channel MOSFET dominates most of the turn-on transient, until the voltage on OUTH pin is about 3V below VDD voltage. The effective resistance of the hybrid pull-up structure during this period is about 2 x R_{OL}. Then the P-Channel MOSFET pulls up the OUTH voltage to VDD rail. The low pull-up impedance results in strong drive strength during the turn-on transient, which shortens the charging time of the input capacitance of the power semiconductor and reduces the turn on switching loss.

The pull-down structure of the driver stage is implemented solely by a pull-down N-Channel MOSFET. This MOSFET can ensure the OUTL voltage be pulled down to VEE rail. The low pull-down impedance not only results in high sink current to reduce the turn-off time, but also helps to increase the noise immunity considering the Miller effect.

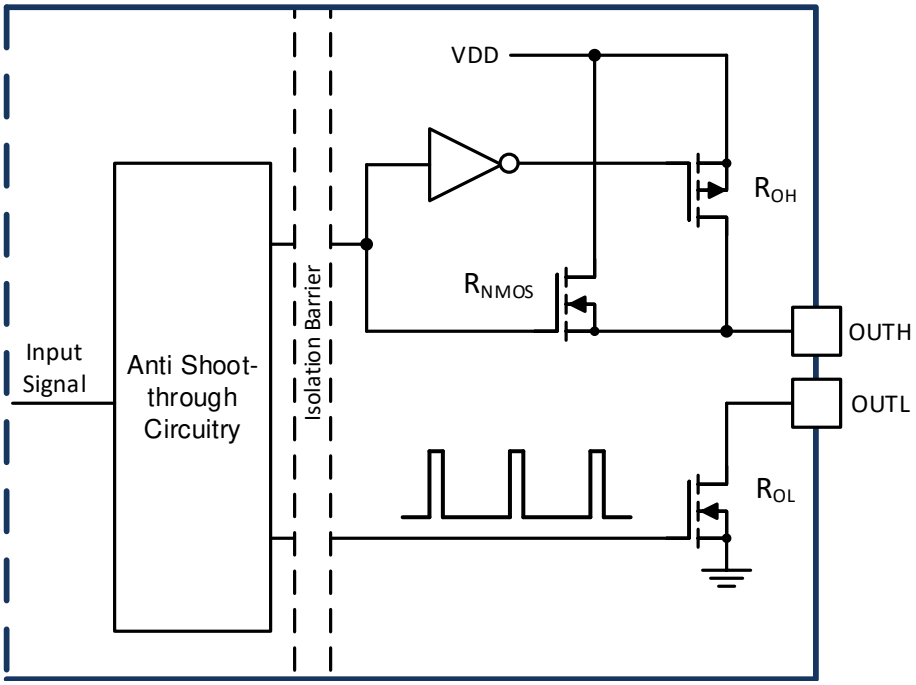


図 7-1. Gate Driver Output Stage

7.3.3 VCC and VDD Undervoltage Lockout (UVLO)

UCC21759-Q1 implements the internal UVLO protection feature for both input and output power supplies VCC and VDD. When the supply voltage is lower than the threshold voltage, the driver output is held as LOW. The output only goes HIGH when both VCC and VDD are out of the UVLO status. The UVLO protection feature not only reduces the power consumption of the driver itself during low power supply voltage condition, but also increases the efficiency of the power stage. For SiC MOSFET and IGBT, the on-resistance reduces while the gate-source voltage or gate-emitter voltage increases. If the power semiconductor is turned on with a low VDD value, the conduction loss increases significantly and can lead to a thermal issue and efficiency reduction of the power stage. UCC21759-Q1 implements 12V threshold voltage of VDD UVLO, with 800mV hysteresis. This threshold voltage is suitable for both SiC MOSFET and IGBT.

Copyright © 2024 Texas Instruments Incorporated

The UVLO protection block features with hysteresis and deglitch filter, which help to improve the noise immunity of the power supply. During the turn on and turn off switching transient, the driver sources and sinks a peak transient current from the power supply, which can result in sudden voltage drop of the power supply. With hysteresis and UVLO deglitch filter, the internal UVLO protection block will ignore small noises during the normal switching transients.

The timing diagrams of the UVLO feature of VCC and VDD are shown in 図 6-8, and 図 6-9. The RDY pin on the input side is used to indicate the power good condition. The RDY pin is open drain. During UVLO condition, the RDY pin is held in low status and connected to GND. Normally the pin is pulled up externally to VCC to indicate the power good. The AIN-APWM function stops working during the UVLO status. The APWM pin on the input side will be held LOW.

7.3.4 Active Pulldown

UCC21759-Q1 implements an active pulldown feature to ensure the OUTH/OUTL pin clamping to VEE when the VDD is open. The OUTH/OUTL pin is in high-impedance status when VDD is open, the active pulldown feature can prevent the output be false turned on before the device is back to control.

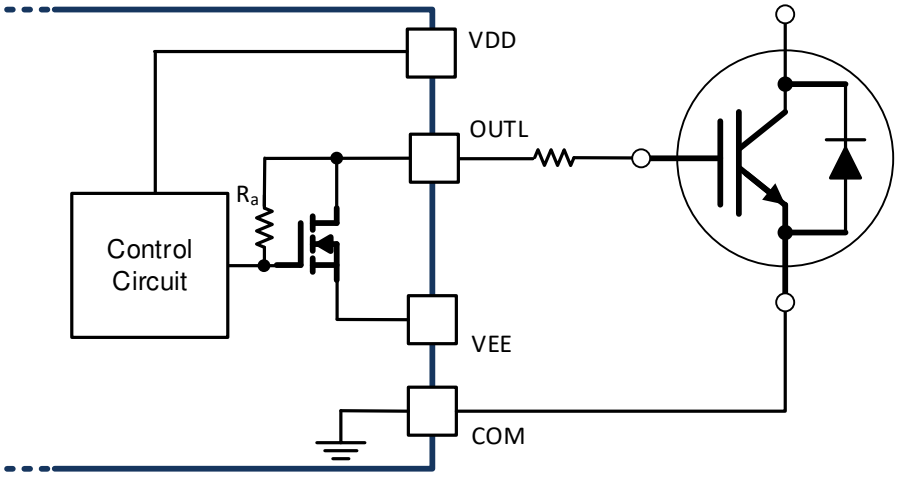


図 7-2. Active Pulldown

7.3.5 Short Circuit Clamping

During short circuit condition, the Miller capacitance can cause a current sinking to the OUTH/OUTL/CLMPI pin due to the high dV/dt and boost the OUTH/OUTL/CLMPI voltage. The short circuit clamping feature of UCC21759-Q1 can clamp the OUTH/OUTL/CLMPI pin voltage to be slightly higher than VDD, which can protect the power semiconductors from a gate-source and gate-emitter overvoltage breakdown. This feature is realized by an internal diode from the OUTH/OUTL/CLMPI to VDD.

Copyright © 2024 Texas Instruments Incorporated

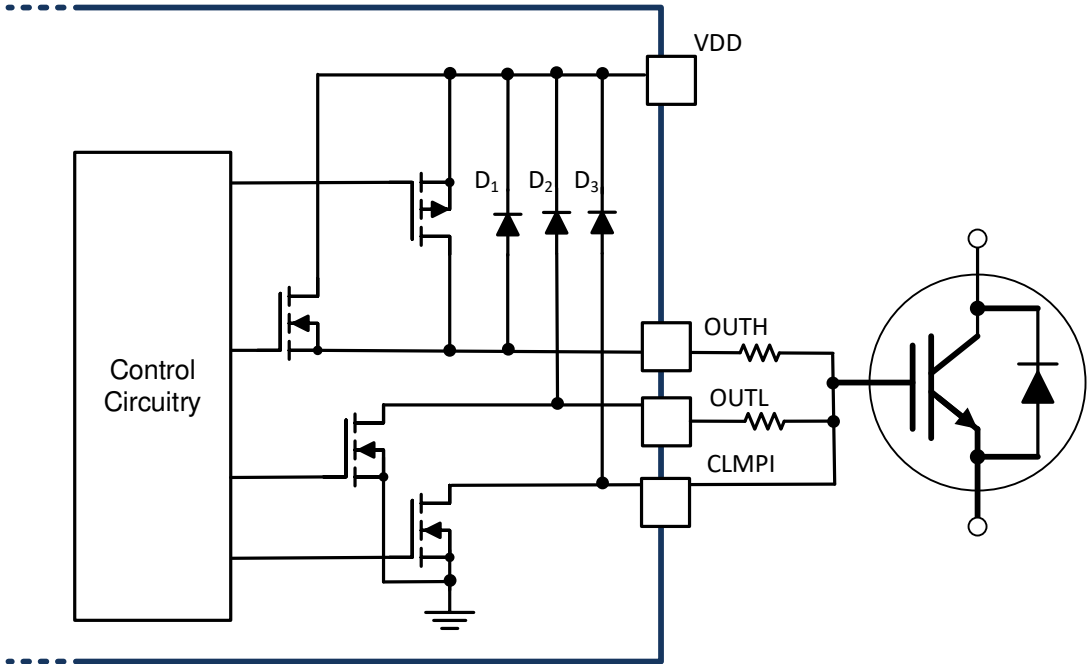


図 7-3. Short Circuit Clamping

7.3.6 Internal Active Miller Clamp

Active Miller clamp feature is important to prevent the false turn-on while the driver is in OFF state. In applications which the device can be in synchronous rectifier mode, the body diode conducts the current during the deadtime while the device is in OFF state, the drain-source or collector-emitter voltage remains the same and the dV/dt happens when the other power semiconductor of the phase leg turns on. The low internal pull-down impedance of UCC21759-Q1 can provide a strong pulldown to hold the OUTL to VEE. However, external gate resistance is usually adopted to limit the dV/dt. The Miller effect during the turn on transient of the other power semiconductor can cause a voltage drop on the external gate resistor, which boost the gate-source or gate-emitter voltage. If the voltage on V_{GS} or V_{GE} is higher than the threshold voltage of the power semiconductor, a shoot through can happen and cause catastrophic damage. The active Miller clamp feature of UCC21759-Q1 drives an internal MOSFET, which connects to the device gate. The MOSFET is triggered when the gate voltage is lower than V_{CLMPTH}, which is 2V above VEE, and creates a low impedance path to avoid the false turn on issue.

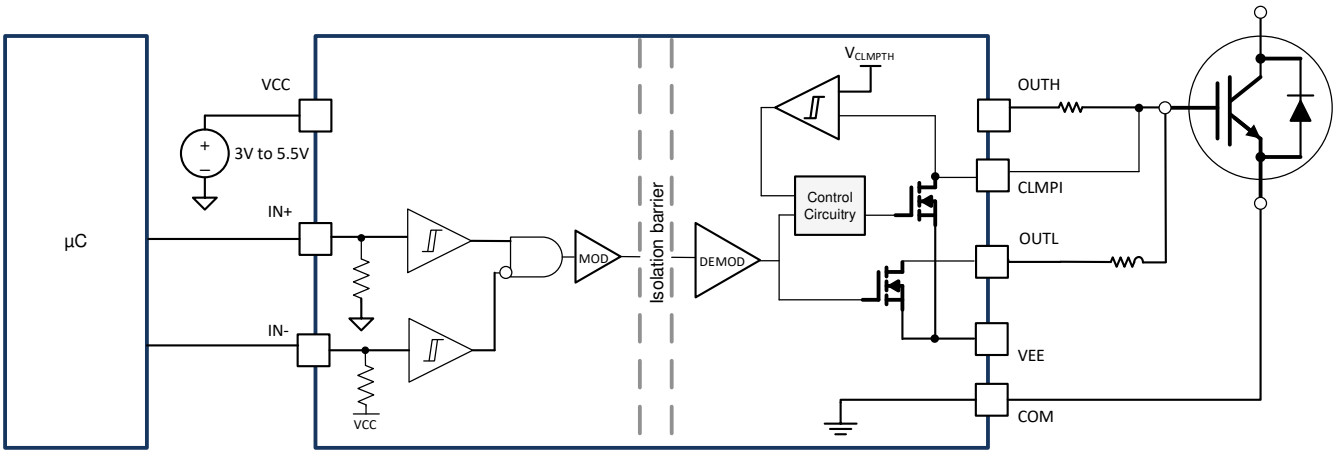


図 7-4. Active Miller Clamp

Copyright © 2024 Texas Instruments Incorporated

7.3.7 Desaturation (DESAT) Protection

The UCC21759-Q1 implements a fast overcurrent and short circuit protection feature to protect the IGBT module from catastrophic breakdown during fault. The DESAT pin of the device has a typical 9V threshold with respect to COM, source or emitter of the power semiconductor. When the input is in floating condition, or the output is held in low state, the DESAT pin is pulled down by an internal MOSFET and held in LOW state, which prevents the overcurrent and short circuit fault from false triggering. The internal current source of the DESAT pin is activated only during the driver ON state, which means the overcurrent and short circuit protection feature only works when the power semiconductor is in on state. The internal pulldown MOSFET helps to discharge the voltage of DESAT pin when the power semiconductor is turned off. UCC21759-Q1 features a 200ns internal leading edge blanking time after the OUTH switches to high state. The internal current source is activated to charge the external blanking capacitor after the internal leading edge blanking time. The typical value of the internal current source is 500µA.

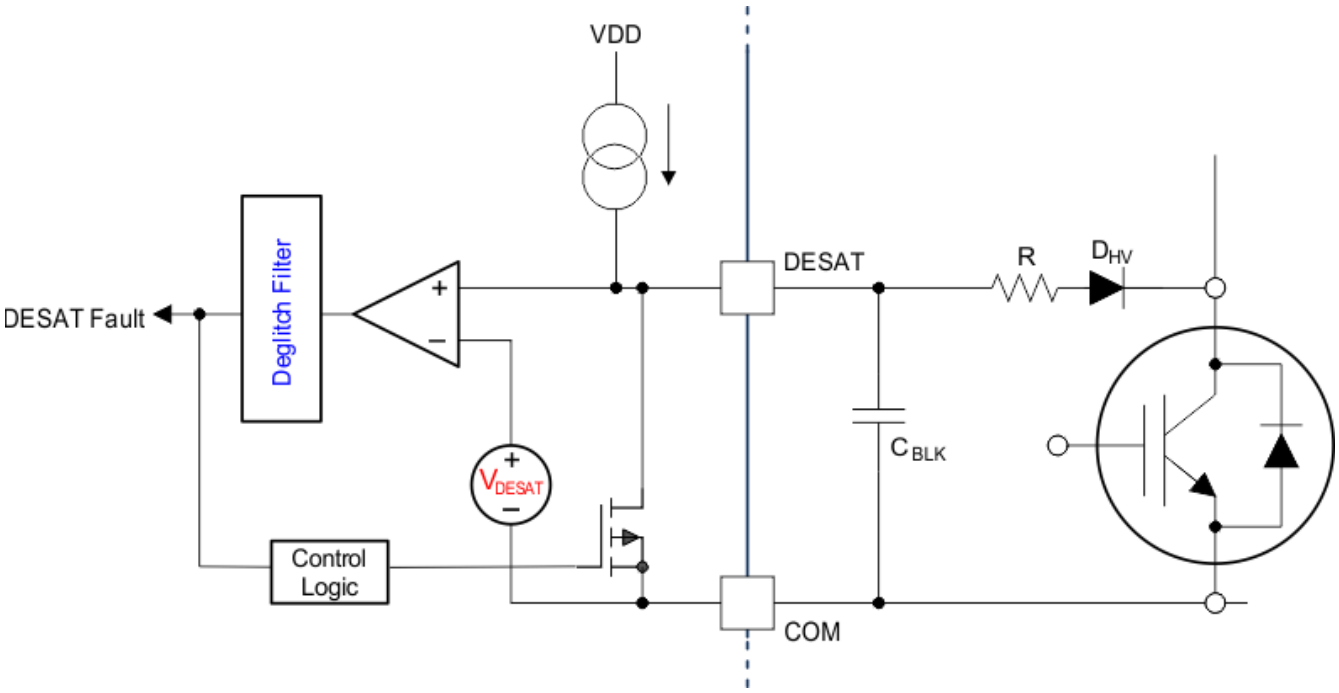


図 7-5. DESAT Protection

7.3.8 Soft Turn-off

UCC21759-Q1 initiates a soft turn-off when the overcurrent and short circuit protection is triggered. When the overcurrent and short circuit fault happens, the IGBT transits from the active region to the desaturation region very fast. The channel current is controlled by the gate voltage and decreasing in a soft manner, thus the overshoot of the IGBT is limited and prevents the overvoltage breakdown. There is a tradeoff between the overshoot voltage and short circuit energy. The turn off speed needs to be slow to limit the overshoot voltage, but the shutdown time should not be too long that the large energy dissipation can breakdown the device. The 400mA soft turn off current of UCC21759-Q1 makes sure the power switches is safely turned off during short circuit events. The timing diagram of soft turn-off shows in 図 6-10.

Copyright © 2024 Texas Instruments Incorporated

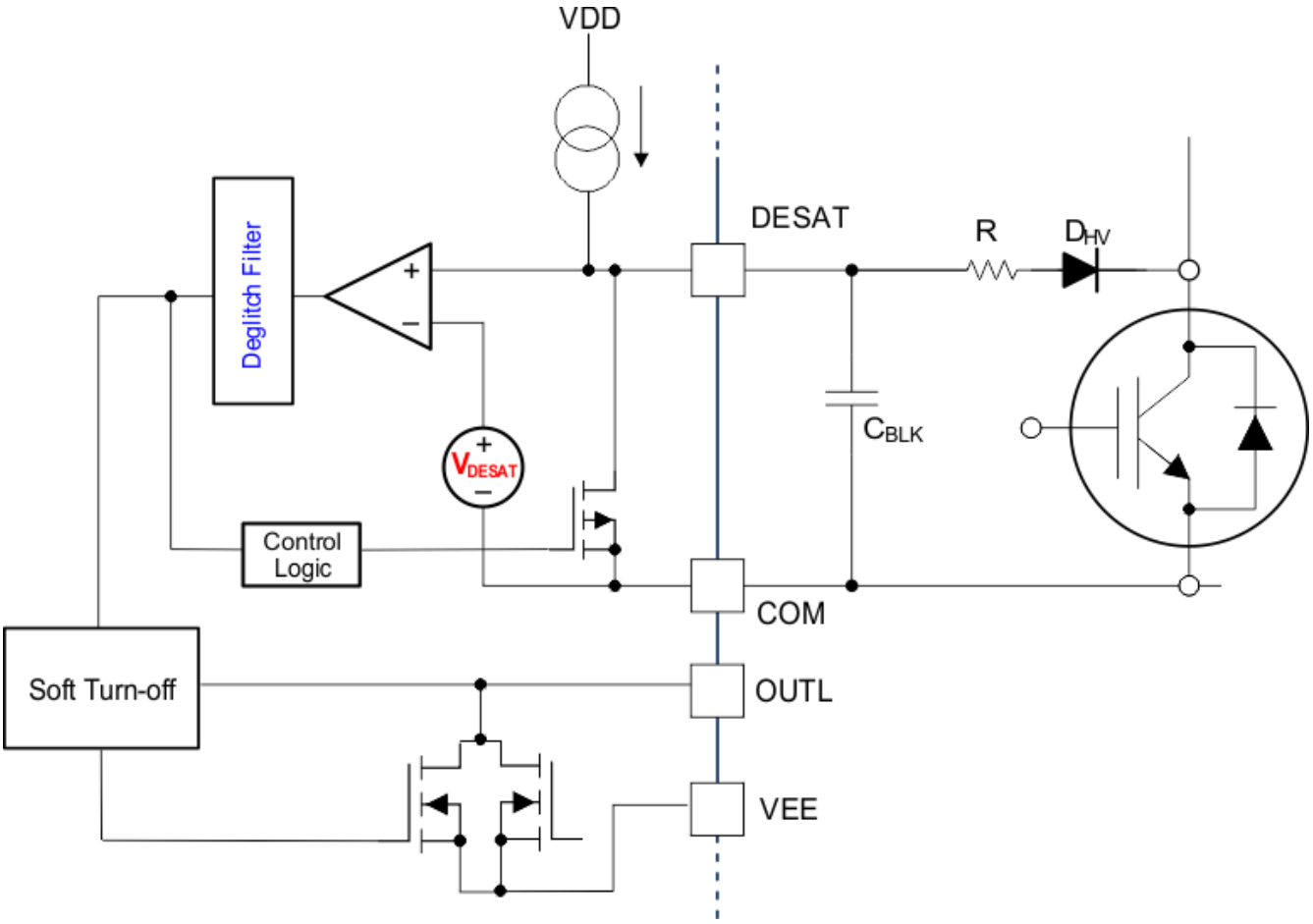


図 7-6. Soft Turn-off

7.3.9 Fault ($\overline{\text{FLT}}$, Reset and Enable ($\overline{\text{RST}}$/EN)

The $\overline{\text{FLT}}$ pin of UCC21759-Q1 is open drain and can report a fault signal to the DSP/MCU when the fault is detected through the DESAT pin. The $\overline{\text{FLT}}$ pin will be pulled down to GND after the fault is detected, and is held low until a reset signal is received from $\overline{\text{RST}}$/EN. The device has a fault mute time $t_{FLTMUTE}$, within which the device ignores any reset signal.

The $\overline{\text{RST}}$/EN is pulled down internally by a 50kΩ resistor, and is thus disabled by default when this pin is floating. It must be pulled up externally to enable the driver. The pin has two purposes:

- To reset the $\overline{\text{FLT}}$ pin. To reset, then $\overline{\text{RST}}$/EN pin is pulled low; if the pin is set and held in low state for more than t_{RSTFIL} after the mute time $t_{FLTMUTE}$, then the fault signal is reset and $\overline{\text{FLT}}$ is reset back to the high impedance status at the rising edge of the input signal at $\overline{\text{RST}}$/EN pin.
- Enable and shutdown the device. If the $\overline{\text{RST}}$/EN pin is pulled low for longer than t_{RSTFIL}, the driver will be disabled and OUTL will be activated to pull down the gate of the IGBT or SiC MOSFET. The pin must be pulled up externally to enable the part, otherwise the device is disabled by default.

7.3.10 Isolated Analog to PWM Signal Function

The UCC21759-Q1 features an isolated analog to PWM signal function from AIN to APWM pin, which allows the isolated temperature sensing, high voltage dc bus voltage sensing, etc. An internal current source I_{AIN} in AIN pin is implemented in the device to bias an external thermal diode or temperature sensing resistor. The UCC21759-Q1 encodes the voltage signal V_{AIN} to a PWM signal, passing through the basic isolation barrier, and output to APWM pin on the input side. The PWM signal can either be transferred directly to DSP/MCU to calculate the duty cycle, or filtered by a simple RC filter as an analog signal. The AIN voltage input range is from 0.6V to 4.5V,

Copyright © 2024 Texas Instruments Incorporated

and the corresponding duty cycle of the APWM output ranges from 88% to 10%. The duty cycle increases linearly from 10% to 88% while the AIN voltage decreases from 4.5V to 0.6V. This corresponds to the temperature coefficient of the negative temperature coefficient (NTC) resistor and thermal diode. When AIN is floating, the AIN voltage is 5V and the APWM operates at 400kHz with approximately 10% duty cycle. The duty cycle absolute error is ±1.5% at 0.6V and 2.5V, and is +1.5% / -2.5% at 4.5V across process and temperature. The in-system accuracy can be improved using calibration. The accuracy of the internal current source I_{AIN} is ±3% across temperature.

The isolated analog to PWM signal feature can also support other analog signal sensing, such as the high voltage dc bus voltage, etc. The internal current source I_{AIN} should be taken into account when designing the potential divider if sensing a high voltage.

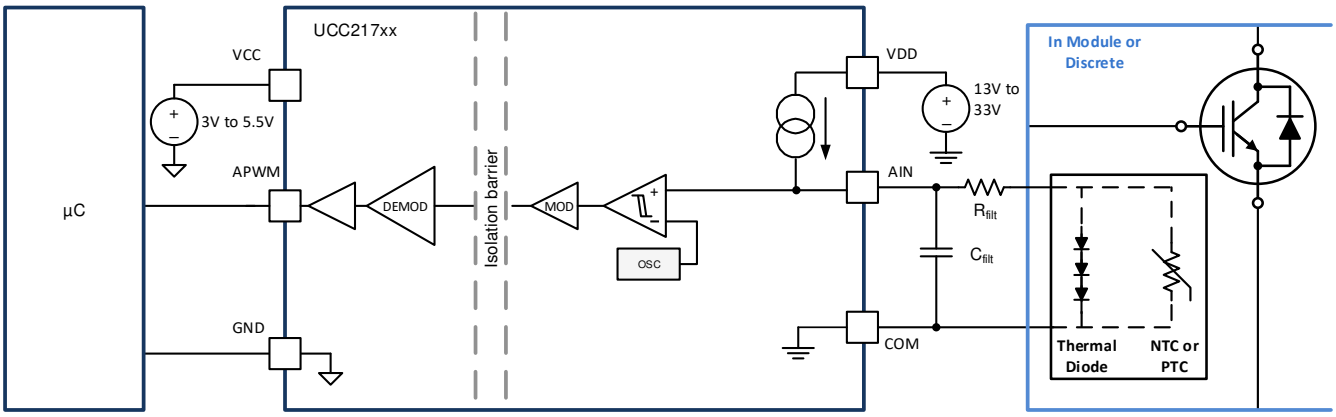


図 7-7. Isolated Analog to PWM Signal

7.4 Device Functional Modes

表 7-1 lists the device function.

表 7-1. Function Table

INPUT							OUTPUT				
VCC	VDD	VEE	IN+	IN-	$\overline{RST}$/EN	AIN	RDY	$\overline{FLT}$	OUTH/ OUTL	CLMPI	APWM
PU	PD	PU	X	X	X	X	Low	HiZ	Low	Low	Low
PD	PU	PU	X	X	X	X	Low	HiZ	Low	Low	Low
PU	PU	PU	X	X	Low	X	HiZ	HiZ	Low	Low	Low
PU	Open	PU	X	X	X	X	Low	HiZ	HiZ	HiZ	HiZ
PU	PU	Open	X	X	X	X	Low	HiZ	Low	Low	Low
PU	PU	PU	Low	X	High	X	HiZ	HiZ	Low	Low	P*
PU	PU	PU	X	High	High	X	HiZ	HiZ	Low	Low	P*
PU	PU	PU	High	High	High	X	HiZ	HiZ	Low	Low	P*
PU	PU	PU	High	Low	High	X	HiZ	HiZ	High	HiZ	P*

PU: Power Up (VCC ≥ 2.85V, VDD ≥ 13.1V, VEE ≤ 0V); PD: Power Down (VCC ≤ 2.35V, VDD ≤ 9.9V); X: Irrelevant; P*: PWM Pulse; HiZ: High Impedance

Copyright © 2024 Texas Instruments Incorporated

8 Applications and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The UCC21759-Q1 device is very versatile because of the strong drive strength, wide range of output power supply, high isolation ratings, high CMTI, and superior protection and sensing features. The 636-VRMS working voltage and 6-kV_{PK} surge immunity can support up both SiC MOSFET and IGBT modules with DC bus voltage up to 900V. The device can be used in both low power and high power applications such as the traction inverter in HEV/EV, on-board charger and charging pile, motor driver, solar inverter, industrial power supplies and etc. The device can drive the high power SiC MOSFET module, IGBT module or paralleled discrete device directly without external buffer drive circuit based on NPN/PNP bipolar transistor in totem-pole structure, which allows the driver to have more control to the power semiconductor and saves the cost and space of the board design. UCC21759-Q1 can also be used to drive very high power modules or paralleled modules with external buffer stage. The input side can support power supply and microcontroller signal from 3.3V to 5V, and the device level shifts the signal to output side through basic isolation barrier. The device has wide output power supply range from 13V to 33V and support wide range of negative power supply. This allows the driver to be used in SiC MOSFET applications, IGBT application and many others. The 12V UVLO benefits the power semiconductor with lower conduction loss and improves the system efficiency. As a basic isolated single channel driver, the device can be used to drive either a low-side or high-side driver.

UCC21759-Q1 device features extensive protection and monitoring features, which can monitor, report and protect the system from various fault conditions.

- Fast detection and protection for the overcurrent and short circuit fault. The semiconductor is shutdown when the fault is detected and $\overline{FLT}$ pin is pulled down to indicate the fault detection. The device is latched unless reset signal is received from the $\overline{RST}$/EN pin.
- Soft turn-off feature to protect the power semiconductor from catastrophic breakdown during overcurrent and short circuit fault. The shutdown energy can be controlled while the overshoot of the power semiconductor is limited.
- UVLO detection to protect the semiconductor from excessive conduction loss. Once the device is detected to be in UVLO mode, the output is pulled down and RDY pin indicates the power supply is lost. The device is back to normal operation mode once the power supply is out of the UVLO status. The power good status can be monitored from the RDY pin.
- Analog signal seensing with isolated analog to PWM signal feature. This feature allows the device to sense the temperature of the semiconductor from the thermal diode or temperature sensing resistor, or dc bus voltage with resistor divider. A PWM signal is generated on the low voltage side with basic isolated from the high voltage side. The signal can be fed back to the microcontroller for the temperature monitoring, voltage monitoring and etc.
- The active Miller clamp feature protects the power semiconductor from false turn on.
- Enable and disable function through the $\overline{RST}$/EN pin.
- Short circuit clamping.
- Active pulldown.

8.2 Typical Application

図 8-1 shows the typical application of a half bridge using two UCC21759-Q1 isolated gate drivers. The half bridge is a basic element in various power electronics applications such as traction inverter in HEV/EV to convert the DC current of the electric vehicle’s battery to the AC current to drive the electric motor in the propulsion system. The topology can also be used in motor drive applications to control the operating speed and torque of the AC motors.

Copyright © 2024 Texas Instruments Incorporated

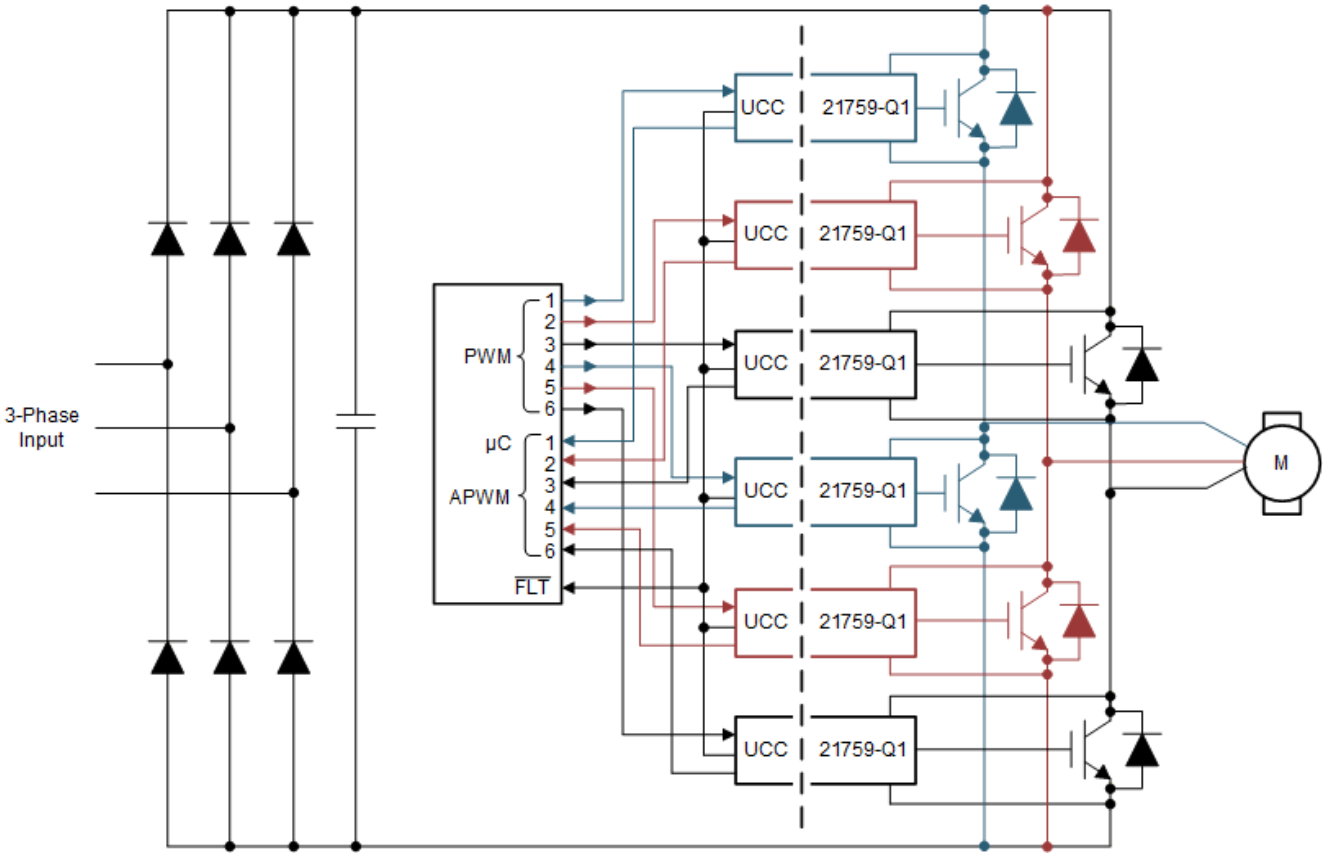


図 8-1. Typical Application Schematic

8.2.1 Design Requirements

The design of the power system for end equipment should consider some design requirements to ensure the reliable operation of UCC21759-Q1 through the load range. The design considerations include the peak source and sink current, power dissipation, overcurrent and short circuit protection, AIN-APWM function for analog signal sensing and etc.

A design example for a half bridge based on IGBT is given in this subsection. The design parameters are show in 表 8-1.

表 8-1. Design Parameters

PARAMETER	VALUE
Input Supply Voltage	5V
IN-OUT Configuration	Non-inverting
Positive Output Voltage VDD	15V
Negative Output Voltage VEE	-5V
DC Bus Voltage	800V
Peak Drain Current	300A
Switching Frequency	50kHz
Switch Type	IGBT Module

Copyright © 2024 Texas Instruments Incorporated

8.2.2 Detailed Design Procedure

8.2.2.1 Input filters for IN+, IN- and RST/EN

In the applications of traction inverter or motor drive, the power semiconductors are in hard switching mode. With the strong drive strength of UCC21759-Q1, the dV/dt can be high, especially for SiC MOSFET. Noise can not only be coupled to the gate voltage due to the parasitic inductance, but also to the input side as the non-ideal PCB layout and coupled capacitance.

UCC21759-Q1 features a 40ns internal deglitch filter to IN+, IN- and RST/EN pin. Any signal less than 40ns can be filtered out from the input pins. For noisy systems, external low pass filter can be added externally to the input pins. Adding low pass filters to IN+, IN- and RST/EN pins can effectively increase the noise immunity and increase the signal integrity. When not in use, the IN+, IN- and RST/EN pins should not be floating. IN- should be tied to GND if only IN+ is used for non-inverting input to output configuration. The purpose of the low pass filter is to filter out the high frequency noise generated by the layout parasitics. While choosing the low pass filter resistors and capacitors, both the noise immunity effect and delay time should be considered according to the system requirements.

8.2.2.2 PWM Interlock of IN+ and IN-

UCC21759-Q1 features the PWM interlock for IN+ and IN- pins, which can be used to prevent the phase leg shoot through issue. As shown in 表 7-1, the output is logic low while both IN+ and IN- are logic high. When only IN+ is used, IN- can be tied to GND. To utilize the PWM interlock function, the PWM signal of the other switch in the phase leg can be sent to the IN- pin. As shown in 図 8-2, the PWM_T is the PWM signal to top side switch, the PWM_B is the PWM signal to bottom side switch. For the top side gate driver, the PWM_T signal is given to the IN+ pin, while the PWM_B signal is given to the IN- pin; for the bottom side gate driver, the PWM_B signal is given to the IN+ pin, while PWM_T signal is given to the IN- pin. When both PWM_T and PWM_B signals are high, the outputs of both gate drivers are logic low to prevent the shoot through condition.

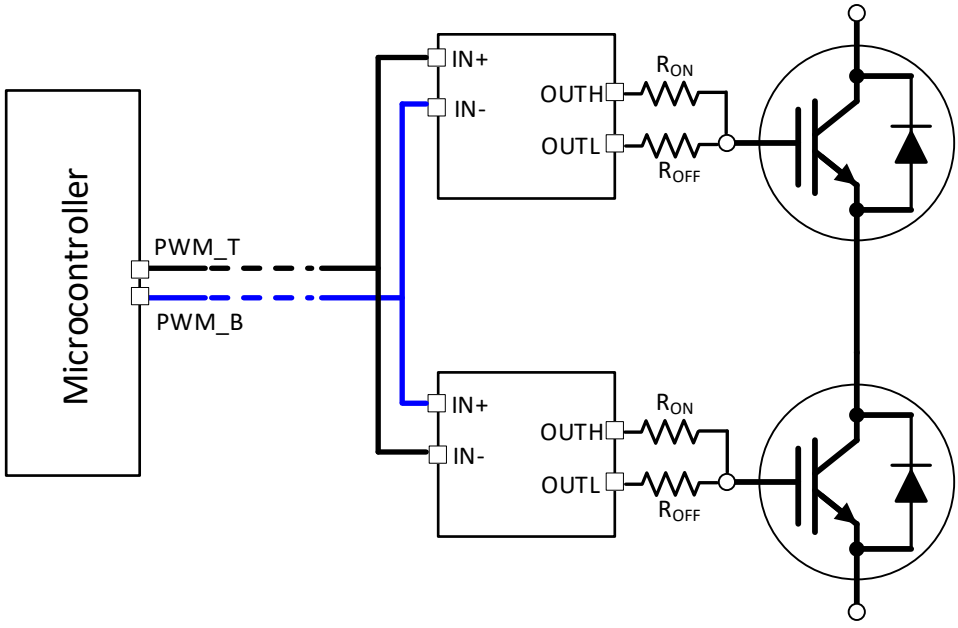


図 8-2. PWM Interlock for a Half Bridge

8.2.2.3 FLT, RDY and RST/EN Pin Circuitry

Both FLT and RDY pin are open-drain output. The RST/EN pin has 50kΩ internal pulldown resistor, so the driver is in OFF status if the RST/EN pin is not pulled up externally. A 5kΩ resistor can be used as pullup resistor for the FLT, RDY and RST/EN pins.

Copyright © 2024 Texas Instruments Incorporated

To improve the noise immunity due to the parasitic coupling and common mode noise, low pass filters can be added between the $\overline{FLT}$, RDY and $\overline{RST}$/EN pins and the microcontroller. A filter capacitor between 100pF to 300pF can be added.

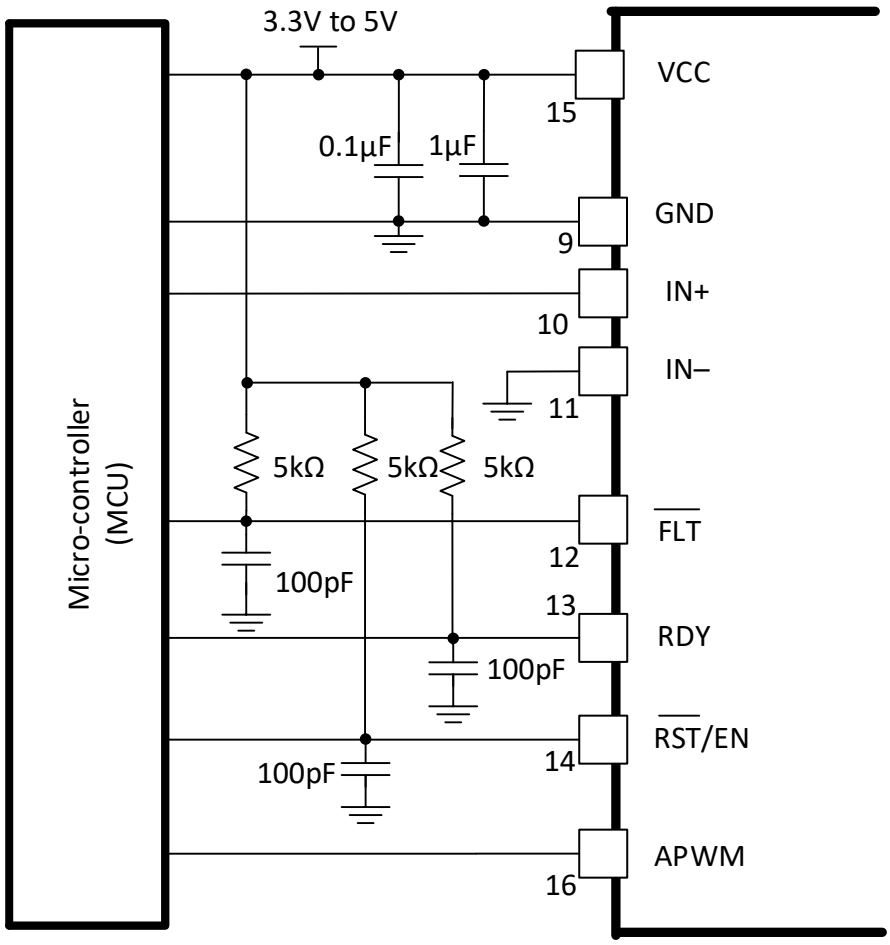


図 8-3. $\overline{FLT}$, RDY and $\overline{RST}$/EN Pins Circuitry

8.2.2.4 $\overline{RST}$/EN Pin Control

$\overline{RST}$/EN pin has two functions. It is used to enable or shutdown the outputs of the driver and to reset the fault signaled on the $\overline{FLT}$ pin after DESAT is detected. $\overline{RST}$/EN pin needs to be pulled up to enable the device; when the pin is pulled down, the device is in disabled status. By default the driver is disabled with the internal 50kΩ pulldown resistor at this pin.

When the driver is latched after DESAT is detected, the $\overline{FLT}$ pin and output are latched low and need to be reset by the $\overline{RST}$/EN pin. The microcontroller must send a signal to $\overline{RST}$/EN pin after the fault to reset the driver. The driver will not respond until after the mute time $t_{FLTMUTE}$. The reset signal must be held low for at least t_{RSTFIL} after the mute time.

This pin can also be used to automatically reset the driver. The continuous input signal IN+ or IN- can be applied to $\overline{RST}$/EN pin. There is no separate reset signal from the microcontroller when configuring the driver this way. If the PWM is applied to the non-inverting input IN+, then IN+ can also be tied to $\overline{RST}$/EN pin. If the PWM is applied to the inverting input IN-, then a NOT logic is needed between the PWM signal from the microcontroller and the $\overline{RST}$/EN pin. Using either configuration results in the driver being reset in every switching cycle without an extra control signal from microcontroller tied to $\overline{RST}$/EN pin. One must ensure the PWM off-time is greater than t_{RSTFIL} in order to reset the driver in cause of a DESAT fault.

Copyright © 2024 Texas Instruments Incorporated

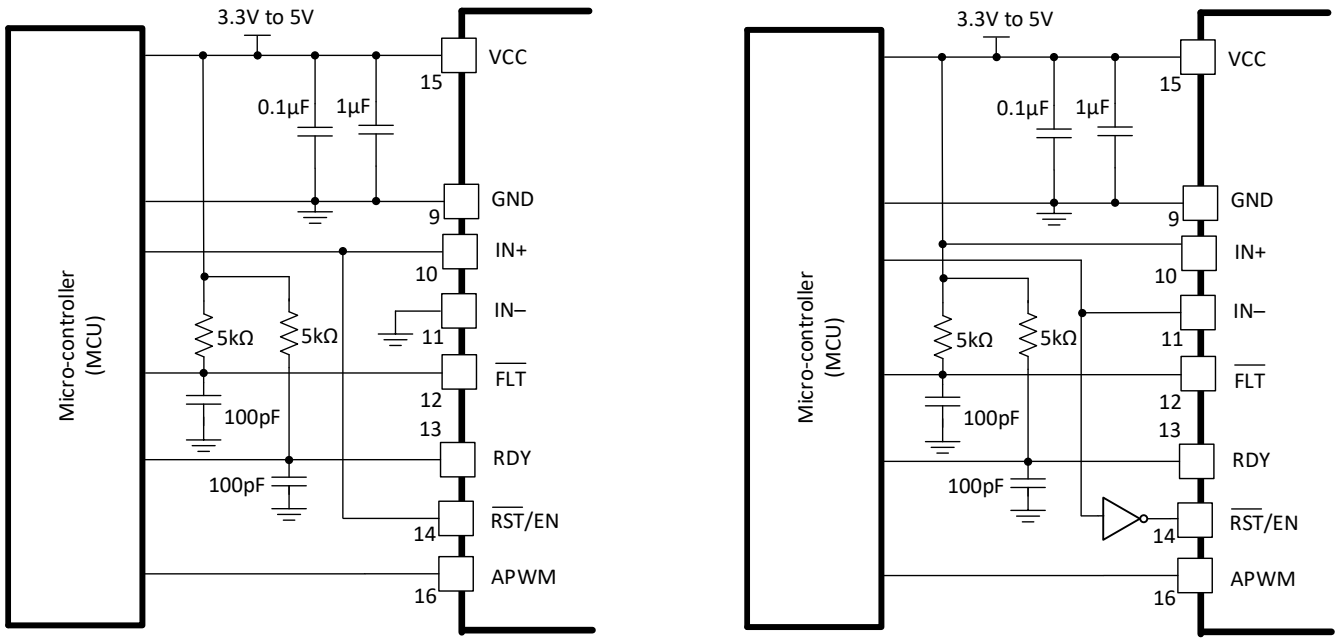


図 8-4. Automatic Reset Control

8.2.2.5 Turn-On and Turn-Off Gate Resistors

UCC21759-Q1 features split outputs OUTH and OUTL, which enables the independent control of the turn on and turn off switching speed. The turn on and turn off resistance determine the peak source and sink current, which controls the switching speed in turn. Meanwhile, the power dissipation in the gate driver should be considered to ensure the device is in the thermal limit. At first, the peak source and sink current are calculated as:

$$I_{source_pk} = \min(10A, \frac{VDD - VEE}{R_{OH_EFF} + R_{ON} + R_{G_Int}})$$

$$I_{sink_pk} = \min(10A, \frac{VDD - VEE}{R_{OL} + R_{OFF} + R_{G_Int}}) \quad (1)$$

Where

- R_{OH_EFF} is the effective internal pull up resistance of the hybrid pull-up structure, shown in 図 7-1, which is approximately 2 x R_{OL}, about 0.7 Ω. This is the dominant resistance during the switching transient of the pull up structure.
- R_{OL} is the internal pulldown resistance, about 0.3 Ω
- R_{ON} is the external turn on gate resistance
- R_{OFF} is the external turn off gate resistance
- R_{G_Int} is the internal resistance of the SiC MOSFET or IGBT module

Copyright © 2024 Texas Instruments Incorporated

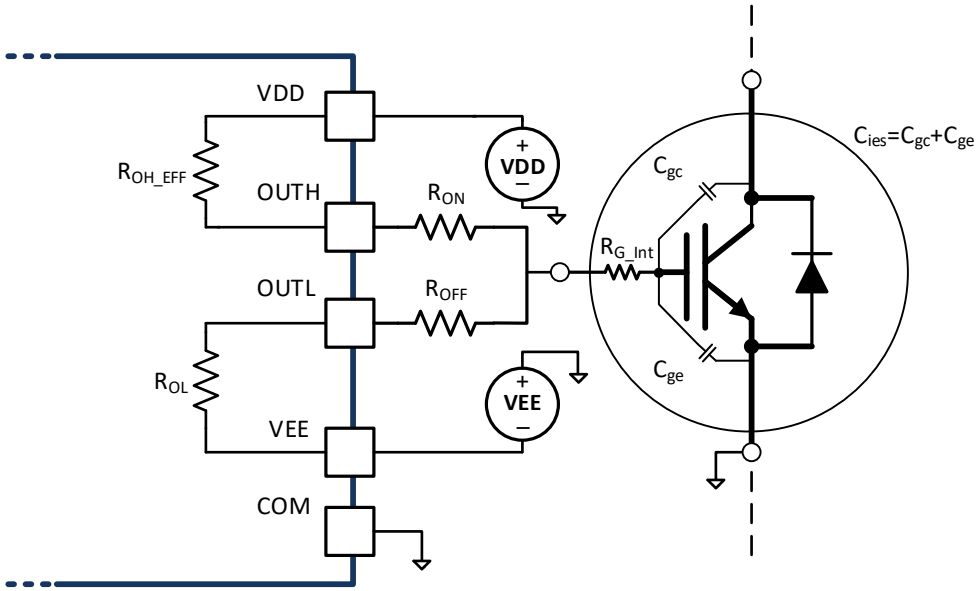


図 8-5. Output Model for Calculating Peak Gate Current

For example, for an IGBT module based system with the following parameters:

- Q_g = 3300 nC
- R_{G_Int} = 1.7 Ω
- R_{ON}=R_{OFF}= 1 Ω

The peak source and sink current in this case are:

$$I_{source_pk} = \min(10A, \frac{VDD - VEE}{R_{OH_EFF} + R_{ON} + R_{G_Int}}) \approx 5.9A$$
$$I_{sink_pk} = \min(10A, \frac{VDD - VEE}{R_{OL} + R_{OFF} + R_{G_Int}}) \approx 6.7A \quad (2)$$

Thus by using 1Ω external gate resistance, the peak source current is 5.9A, the peak sink current is 6.7A. The collector-to-emitter dV/dt during the turn on switching transient is dominated by the gate current at the Miller plateau voltage. The hybrid pullup structure ensures the peak source current at the Miller plateau voltage, unless the turn on gate resistor is too high. The faster the collector-to-emitter, V_{ce}, voltage rises to V_{DC}, the smaller the turn on switching loss is. The dV/dt can be estimated as Q_{gc}/I_{source_pk}. For the turn off switching transient, the drain-to-source dV/dt is dominated by the load current, unless the turn off gate resistor is too high. After V_{ce} reaches the dc bus voltage, the power semiconductor is in saturation mode and the channel current is controlled by V_{ge}. The peak sink current determines the dI/dt, which dominates the V_{ce} voltage overshoot accordingly. If using relatively large turn off gate resistance, the V_{ce} overshoot can be limited. The overshoot can be estimated by:

$$\Delta V_{ce} = L_{stray} \cdot I_{load} / ((R_{OFF} + R_{OL} + R_{G_Int}) \cdot C_{ies} \cdot \ln(V_{plat} / V_{th})) \quad (3)$$

Where

- L_{stray} is the stray inductance in power switching loop, as shown in 図 8-6
- I_{load} is the load current, which is the turn off current of the power semiconductor
- C_{ies} is the input capacitance of the power semiconductor
- V_{plat} is the plateau voltage of the power semiconductor
- V_{th} is the threshold voltage of the power semiconductor

Copyright © 2024 Texas Instruments Incorporated

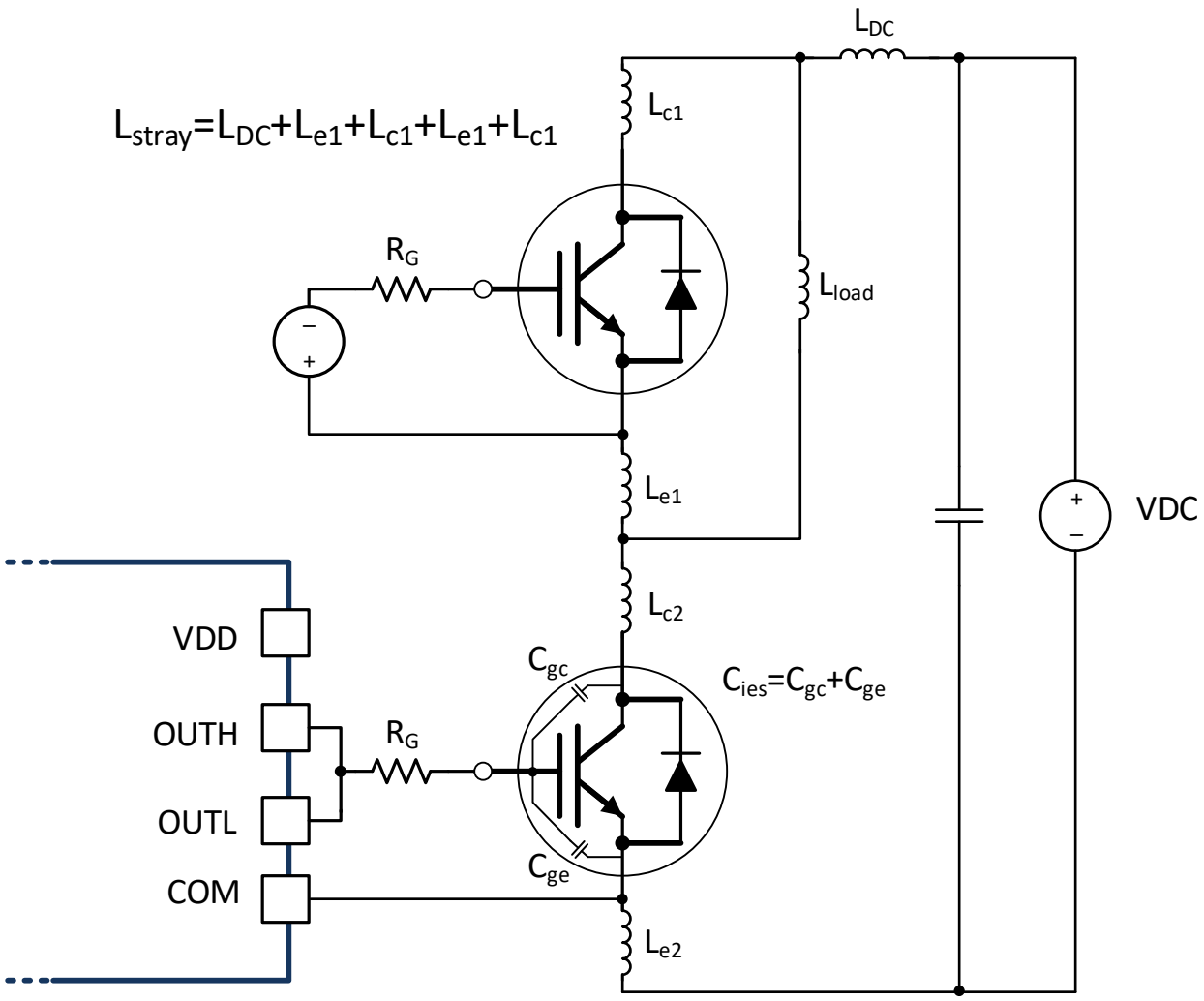


図 8-6. Stray Parasitic Inductance of IGBTs in a Half-Bridge Configuration

The power dissipation should be taken into account to maintain the gate driver within the thermal limit. The power loss of the gate driver includes the quiescent loss and the switching loss, which can be calculated as:

$$P_{DR} = P_Q + P_{SW} \tag{4}$$

P_Q is the quiescent power loss for the driver, which is I_q x (VDD-VEE) = 5mA x 20V = 0.100W. The quiescent power loss is the power consumed by the internal circuits such as the input stage, reference voltage, logic circuits, protection circuits when the driver is swithing when the driver is biased with VDD and VEE, and also the charging and discharing current of the internal circuit when the driver is switching. The power dissipation when the driver is switching can be calculated as:

$$P_{SW} = \frac{1}{2} \cdot \left(\frac{R_{OH_EFF}}{R_{OH_EFF} + R_{ON} + R_{G_Int}} + \frac{R_{OL}}{R_{OL} + R_{OFF} + R_{G_Int}} \right) \cdot (VDD - VEE) \cdot f_{sw} \cdot Q_g \tag{5}$$

Where

- Q_g is the gate charge required at the operation point to fully charge the gate voltage from VEE to VDD
- f_{sw} is the switching frequency

Copyright © 2024 Texas Instruments Incorporated

In this example, the P_{SW} can be calculated as:

$$P_{SW} = \frac{1}{2} \cdot \left(\frac{R_{OH_EFF}}{R_{OH_EFF} + R_{ON} + R_{G_Int}} + \frac{R_{OL}}{R_{OL} + R_{OFF} + R_{G_Int}} \right) \cdot (VDD - VEE) \cdot f_{sw} \cdot Q_g = 0.505W \quad (6)$$

Thus, the total power loss is:

$$P_{DR} = P_Q + P_{SW} = 0.10W + 0.505W = 0.605W \quad (7)$$

When the board temperature is 125°C, the junction temperature can be estimated as:

$$T_j = T_b + \psi_{jb} \cdot P_{DR} \approx 150\,^{\circ}C \quad (8)$$

Therefore, for the application in this example, with 125°C board temperature, the maximum switching frequency is ~50kHz to keep the gate driver in the thermal limit. By using a lower switching frequency, or increasing external gate resistance, the gate driver can be operated at a higher switching frequency.

8.2.2.6 Desaturation (DESAT) Protection

A standard desaturation circuit can be applied to the DESAT pin. If the voltage of the DESAT pin is higher than the threshold V_{DESAT}, the soft turn-off is initiated. A fault will be reported to the input side to DSP/MCU. The output is held to LOW after the fault is detected, and can only be reset by the $\overline{RST}$/EN pin. The state-of-art overcurrent and short circuit detection time helps to ensure a short shutdown time for SiC MOSFET and IGBT.

If DESAT pin is not in use, it must be tied to COM to avoid overcurrent fault false triggering.

- Fast reverse recovery high voltage diode is recommended in the desaturation circuit. A resistor is recommended in series with the high voltage diode to limit the inrush current. Multiple high voltage diodes can be placed in series to reduce the DESAT detection voltage as seen by the IGBT or SiC MOSFET based on the forward voltage drop.
- A Schottky diode is recommended from COM to DESAT to prevent driver damage caused by negative voltage.
- A Zener diode is recommended from COM to DESAT to prevent driver damage caused by positive voltage.

8.2.2.7 Isolated Analog Signal Sensing

The isolated analog signal sensing feature provides a simple isolated channel for the isolated temperature detection, voltage sensing and etc. One typical application of this function is the temperature monitor of the power semiconductor. Thermal diodes or temperature sensing resistors are integrated in the SiC MOSFET or IGBT module close to the dies to monitor the junction temperature. UCC21759-Q1 has an internal 200uA current source with ±3% accuracy across temperature, which can forward bias the thermal diodes or create a voltage drop on the temperature sensing resistors. The sensed voltage from the AIN pin is passed through the isolation barrier to the input side and transformed to a PWM signal. The duty cycle of the PWM changes linearly from 10% to 88% when the AIN voltage changes from 4.5V to 0.6V and can be represented using 式 9.

$$D_{APWM}(\%) = -20 * V_{AIN} + 100 \quad (9)$$

8.2.2.7.1 Isolated Temperature Sensing

A typical application circuit is shown in 図 8-7. To sense temperature, the AIN pin is connected to the thermal diode or thermistor which can be discrete or integrated within the power module. A low pass filter is recommended for the AIN input. Since the temperature signal does not have a high bandwidth, the low pass filter is mainly used for filtering the noise introduced by the switching of the power device, which does not require stringent control for propagation delay. The filter capacitance for C_{filt} can be chosen between 1nF to 100nF and the filter resistance R_{filt} between 1Ω to 10Ω according to the noise level.

Copyright © 2024 Texas Instruments Incorporated

The output of APWM is directly connected to the microcontroller to measure the duty cycle dependent on the voltage input at AIN, using 式 9.

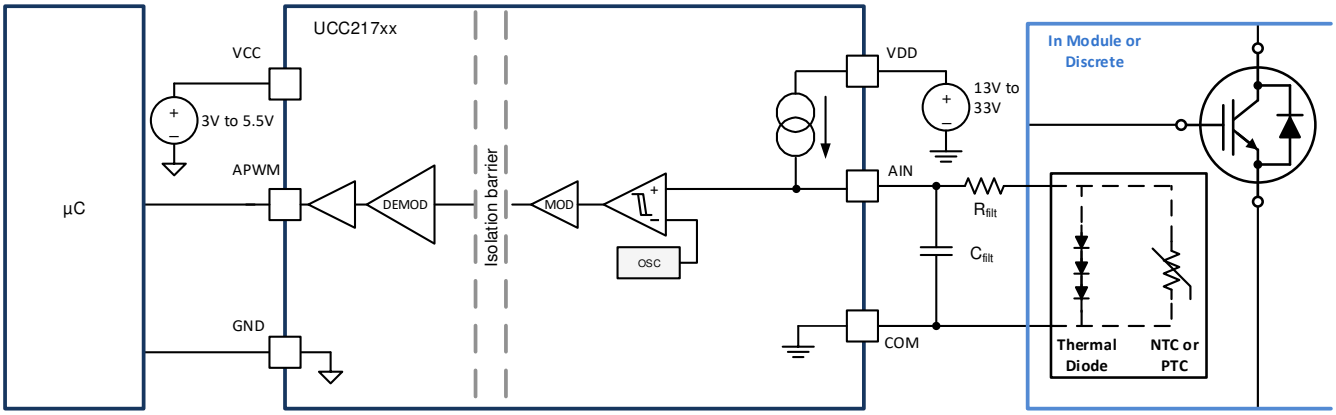


図 8-7. Thermal Diode or Thermistor Temperature Sensing Configuration

When a high-precision voltage supply for VCC is used on the primary side of UCC21759-Q1 the duty cycle output of APWM may also be filtered and the voltage measured using the microcontroller's ADC input pin, as shown in 図 8-8. The frequency of APWM is 400kHz, so the value for R_{filt_2} and C_{filt_2} should be such that the cutoff frequency is below 400kHz. Temperature does not change rapidly, thus the rise time due to the RC constant of the filter is not under a strict requirement.

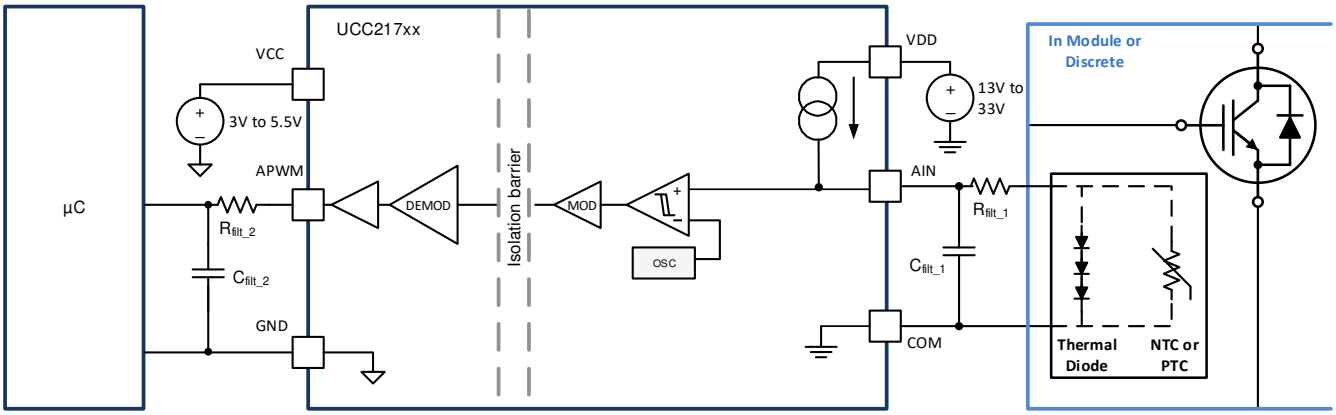


図 8-8. APWM Channel with Filtered Output

The example below shows the results using a 4.7kΩ NTC, NTCS0805E3472FMT, in series with a 3kΩ resistor and also the thermal diode using four diode-connected MMBT3904 NPN transistors. The sensed voltage of the 4 MMBT3904 thermal diodes connected in series ranges from about 2.5V to 1.6V from 25°C to 135°C, corresponding to 50% to 68% duty cycle. The sensed voltage of the NTC thermistor connected in series with the 3kΩ resistor ranges from about 1.5V to 0.6V from 25°C to 135°C, corresponding to 70% to 88% duty cycle. The voltage at VAIN of both sensors and the corresponding measured duty cycle at APWM is shown in 図 8-9.

Copyright © 2024 Texas Instruments Incorporated

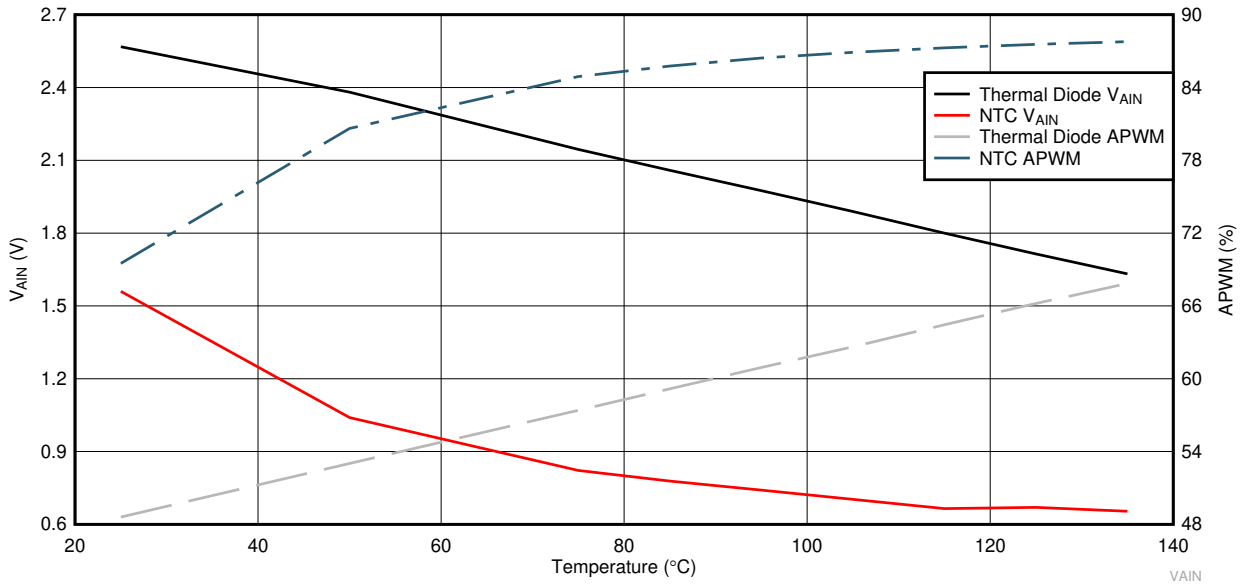


図 8-9. Thermal diode and NTC V_{AIN} and Corresponding Duty Cycle at APWM

The duty cycle output has 3% variation throughout temperature without any calibration from 0.6V to 2.5V at VAIN, as shown in 図 8-10 but with single-point calibration at 25°C, the duty accuracy can be improved to 1%, as shown in 図 8-11.

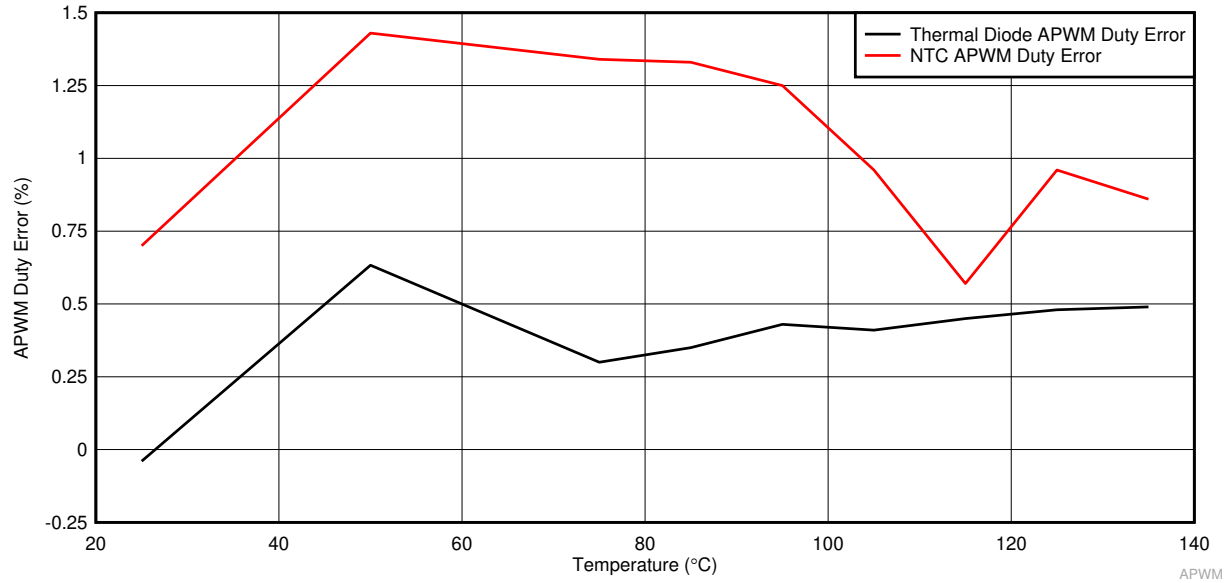


図 8-10. APWM Duty Error Without Calibration

Copyright © 2024 Texas Instruments Incorporated

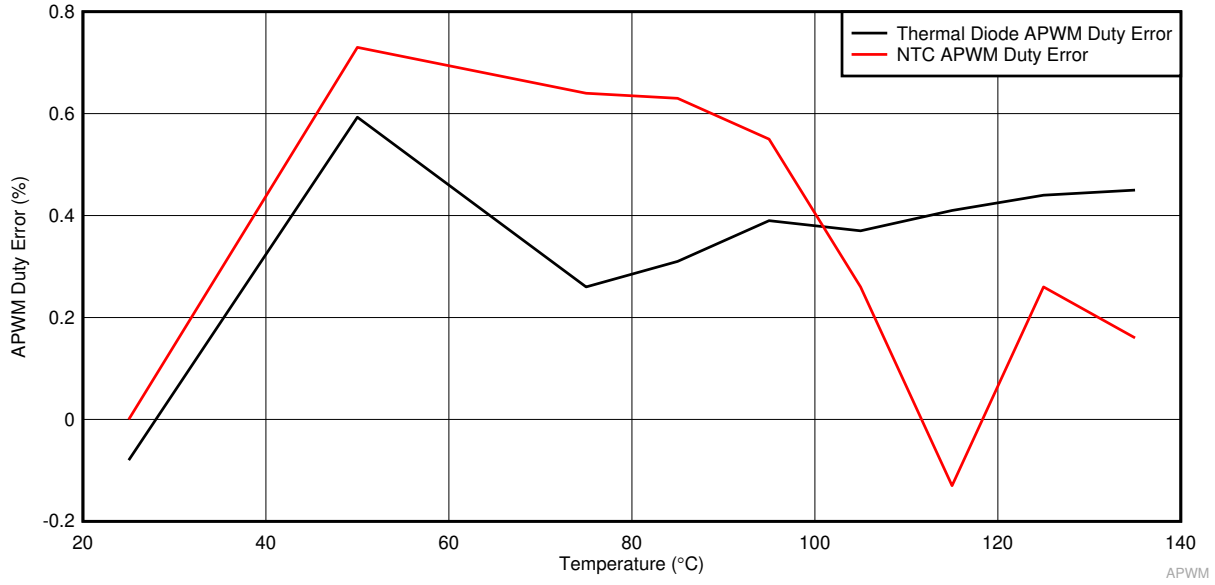


図 8-11. APWM Duty Error with Single-Point Calibration

8.2.2.7.2 Isolated DC Bus Voltage Sensing

The AIN to APWM channel may be used for other applications such as the DC-link voltage sensing, as shown in 図 8-12. The same filtering requirements as given above may be used in this case, as well. The number of attenuation resistors, R_{atten_1} through R_{atten_n}, is dependent on the voltage level and power rating of the resistor. The voltage is finally measured across R_{LV_DC} to monitor the stepped-down voltage of the HV DC-link which must fall within the voltage range of AIN from 0.6V to 4.5V. The driver should be referenced to the same point as the measurement reference, thus in the case shown below the UCC21759-Q1 is driving the lower IGBT in the half-bridge and the DC-link voltage measurement is referenced to COM. The internal current source I_{AIN} should be taken into account when designing the resistor divider. The AIN pin voltage is:

$$V_{AIN} = \frac{R_{LV_DC}}{R_{LV_DC} + \sum_{i=1}^{n} R_{atten_i}} \cdot V_{DC} + R_{LV_DC} \cdot I_{AIN} \quad (10)$$

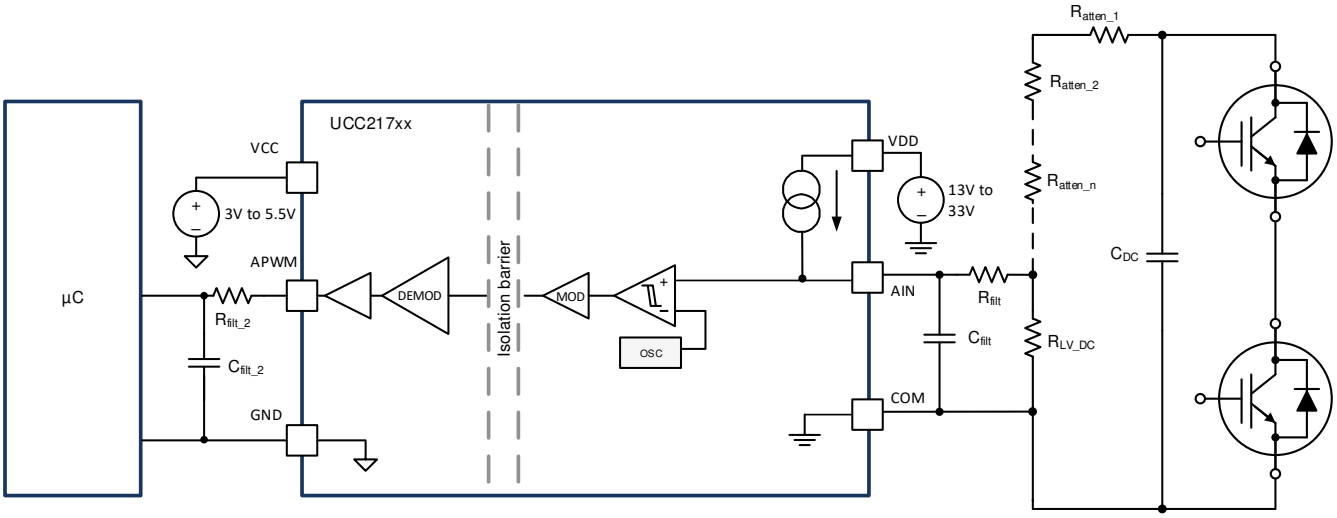


図 8-12. DC-link Voltage Sensing Configuration

8.2.2.8 Higher Output Current Using an External Current Buffer

To increase the IGBT gate drive current, a non-inverting current buffer (such as the NPN/PNP buffer shown in 図 8-13) can be used. Inverting types are not compatible with the desaturation fault protection circuitry and must be avoided. The MJD44H11/MJD45H11 pair is appropriate for peak currents up to 15 A, the D44VH10/ D45VH10 pair is up to 20 A peak.

In the case of a over-current detection, the soft turn off (STO) is activated. External components must be added to implement STO instead of normal turn off speed when an external buffer is used. C_{STO} sets the timing for soft turn off and R_{STO} limits the inrush current to below the current rating of the internal FET (10A). R_{STO} should be at least (VDD-VEE)/10. The soft turn off timing is determined by the internal current source of 400mA and the capacitor C_{STO}. C_{STO} is calculated using 式 11.

$$C_{STO} = \frac{I_{STO} \cdot t_{STO}}{VDD - VEE} \tag{11}$$

- I_{STO} is the the internal STO current source, 400mA
- t_{STO} is the desired STO timing

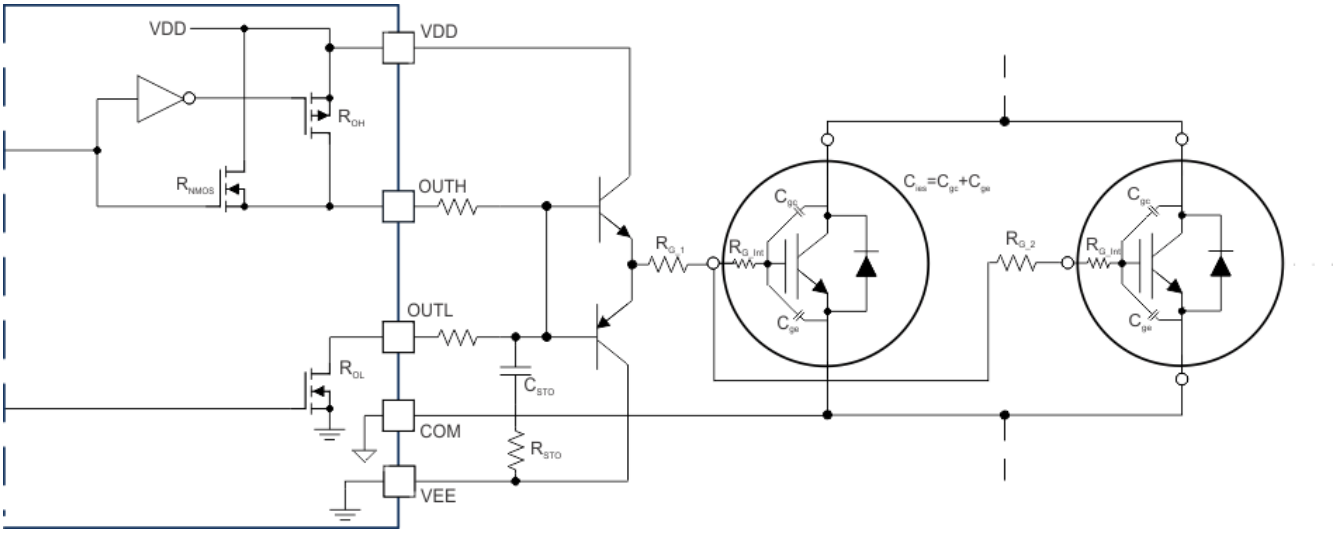


図 8-13. Current Buffer for Increased Drive Strength

Copyright © 2024 Texas Instruments Incorporated

8.2.3 Application Curves

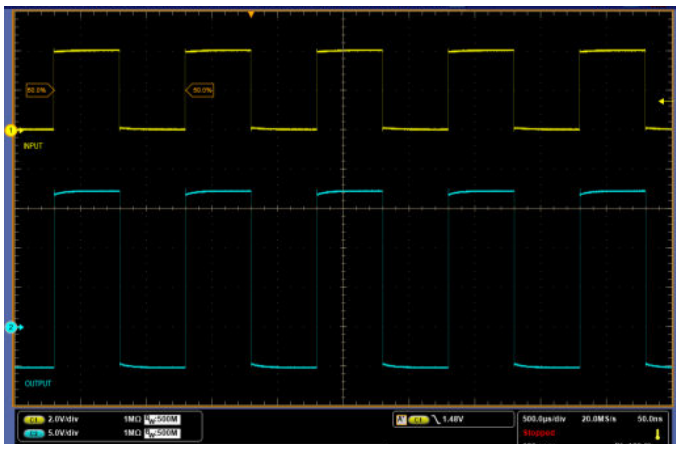


図 8-14. PWM Input (yellow) and Driver Output (blue)

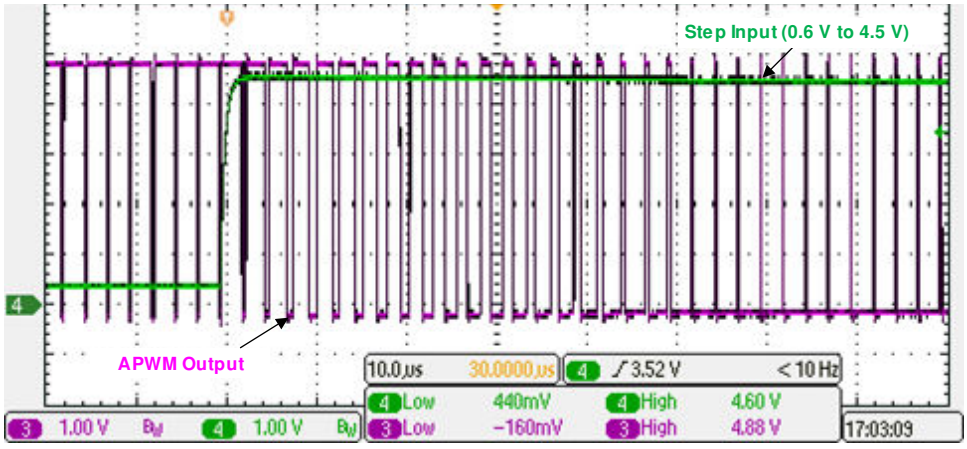


図 8-15. AIN Step Input (green) and APWM Output (pink)

9 Power Supply Recommendations

During the turn on and turn off switching transient, the peak source and sink current is provided by the VDD and VEE power supply. The large peak current is possible to drain the VDD and VEE voltage level and cause a voltage droop on the power supplies. To stabilize the power supply and ensure a reliable operation, a set of decoupling capacitors are recommended at the power supplies. Considering UCC21759-Q1 has ±10A peak drive strength and can generate high dV/dt, a 10µF bypass cap is recommended between VDD and COM, VEE and COM. A 1µF bypass cap is recommended between VCC and GND due to less current comparing with output side power supplies. A 0.1µF decoupling cap is also recommended for each power supply to filter out high frequency noise. The decoupling capacitors must be low ESR and ESL to avoid high frequency noise, and should be placed as close as possible to the VCC, VDD and VEE pins to prevent noise coupling from the system parasitics of PCB layout.

Copyright © 2024 Texas Instruments Incorporated

10 Layout

10.1 Layout Guidelines

Due to the strong drive strength of UCC21759-Q1, careful considerations must be taken in PCB design. Below are some key points:

- The driver should be placed as close as possible to the power semiconductor to reduce the parasitic inductance of the gate loop on the PCB traces
- The decoupling capacitors of the input and output power supplies should be placed as close as possible to the power supply pins. The peak current generated at each switching transient can cause high dI/dt and voltage spike on the parasitic inductance of PCB traces
- The driver COM pin should be connected to the Kelvin connection of SiC MOSFET source or IGBT emitter. If the power device does not have a split Kelvin source or emitter, the COM pin should be connected as close as possible to the source or emitter terminal of the power device package to separate the gate loop from the high power switching loop
- Use a ground plane on the input side to shield the input signals. The input signals can be distorted by the high frequency noise generated by the output side switching transients. The ground plane provides a low-inductance filter for the return current flow
- If the gate driver is used for the low side switch which the COM pin connected to the dc bus negative, use the ground plane on the output side to shield the output signals from the noise generated by the switch node; if the gate driver is used for the high side switch, which the COM pin is connected to the switch node, ground plane is not recommended
- If ground plane is not used on the output side, separate the return path of the DESAT and AIN ground loop from the gate loop ground which has large peak source and sink current
- No PCB trace or copper is allowed under the gate driver. A PCB cutout is recommended to avoid any noise coupling between the input and output side which can contaminate the isolation barrier

Copyright © 2024 Texas Instruments Incorporated

10.2 Layout Example

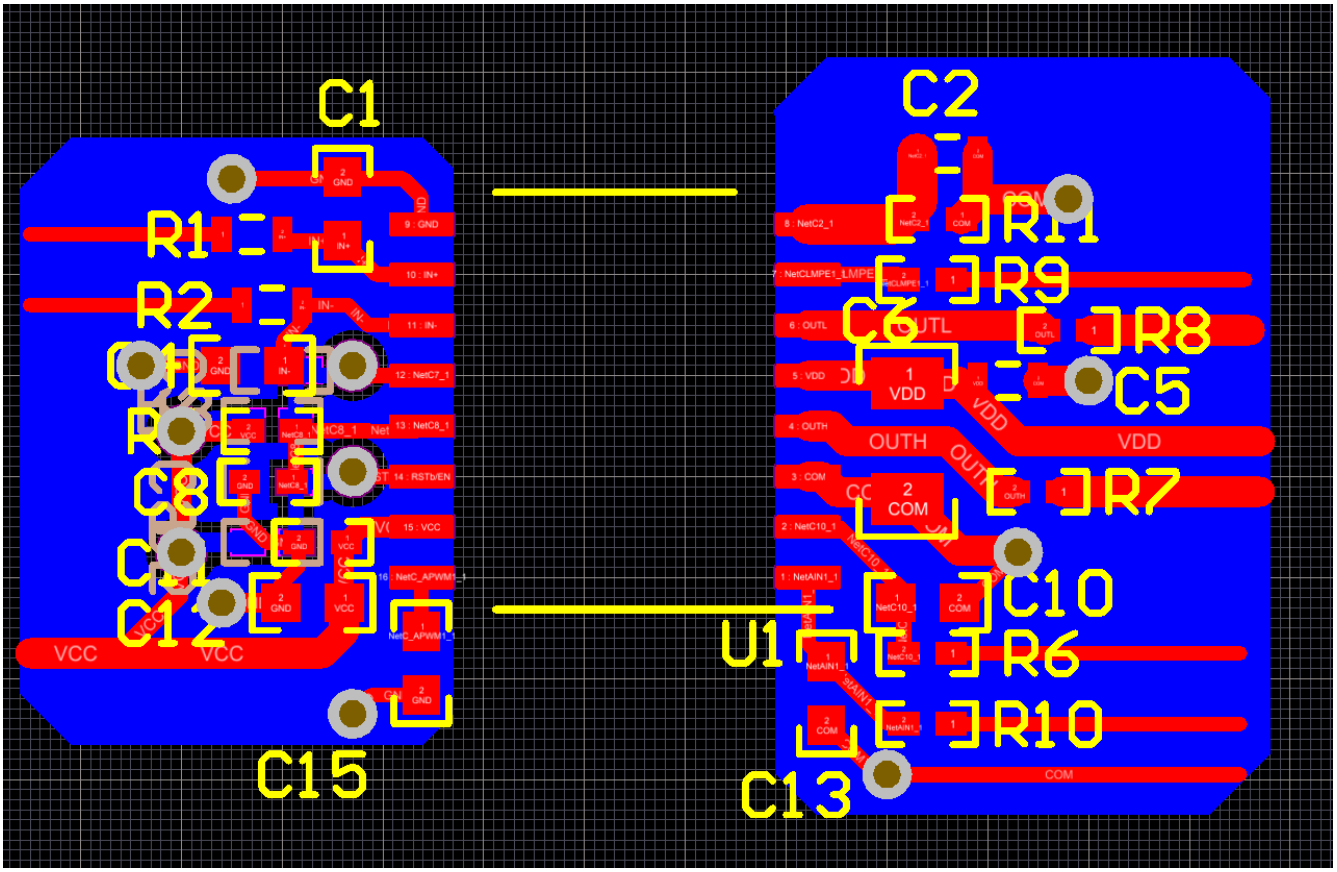


図 10-1. Layout Example

11 Device and Documentation Support

11.1 サード・パーティ製品に関する免責事項

サード・パーティ製品またはサービスに関するテキサス・インスツルメンツの出版物は、単独またはテキサス・インスツルメンツの製品、サービスと一緒に提供される場合に関係なく、サード・パーティ製品またはサービスの適合性に関する是認、サード・パーティ製品またはサービスの是認の表明を意味するものではありません。

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *Isolation Glossary*

11.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

11.4 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

11.5 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

11.6 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

Copyright © 2024 Texas Instruments Incorporated

12 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (December 2020) to Revision B (February 2024) **Page**

- タイトルに車載用を追加 1
- AEC-Q100 認定の下に副項目を追加 1
- 「特長」の安全関連の認証を変更、最新の規格に合わせて絶縁定格を変更 1
- 最新の規格に基づいて絶縁電圧を変更 1
- Added what to do with unused pins to Pin Functions Table 3
- Changed recommended value of decoupling capacitors 3
- Added recommended decoupling capacitor layout placement 3
- Changed VDE ratings per the latest standard 6
- Changed certification table according to latest standard and status 7
- Deleted short circuit clamping max condition 8
- Changed VAin lower limit to 0.6V 8
- Changed V_{CLMPI}-VDD test condition current direction 8
- Changed I_{CHG} lower limit to 430µA 8
- Added soft turn-off test condition 8
- Changed isolation voltage based on latest standard 24
- Changed DESAT protection figure 29
- Changed soft turn-off figure 29
- Added function state showing gate driver turning on. Changed RDY condition when VCC is PD. 32
- Changed isolation voltage based on latest standard 33
- Changed Current Buffer for Increased Drive Strength figure 44

Changes from Revision * (August 2020) to Revision A (December 2020) **Page**

- デバイスのピン構成を訂正 1
- Specifications included for Isolated Temperature Sense and Monitor (AIN-APWM) 8

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2024 Texas Instruments Incorporated

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、テキサス・インスツルメンツの販売条件、または ti.com やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用されるテキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC21759QDWQ1	Obsolete	Production	SOIC (DW) | 16	-	-	Call TI	Call TI	-40 to 150	UCC21759Q
UCC21759QDWRQ1	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 150	UCC21759Q
UCC21759QDWRQ1.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 150	UCC21759Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

GENERIC PACKAGE VIEW

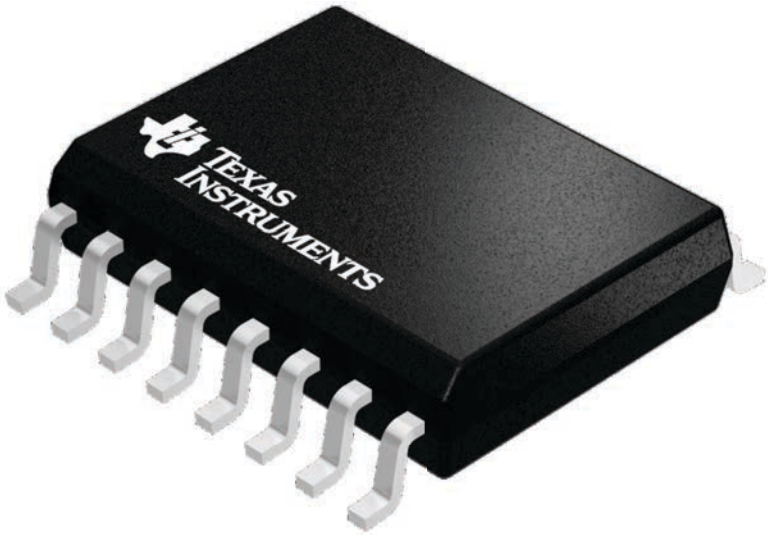
DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

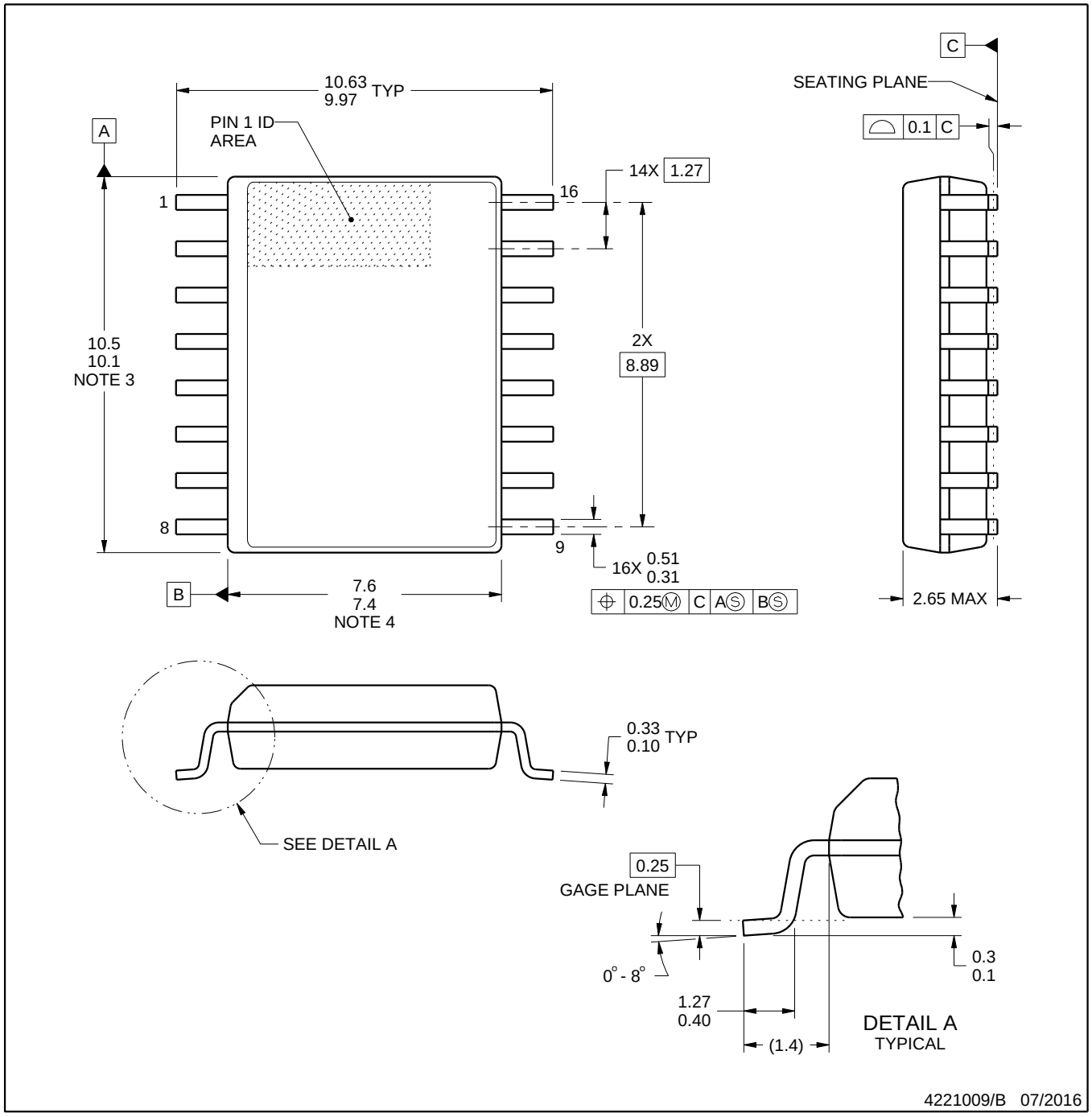
SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



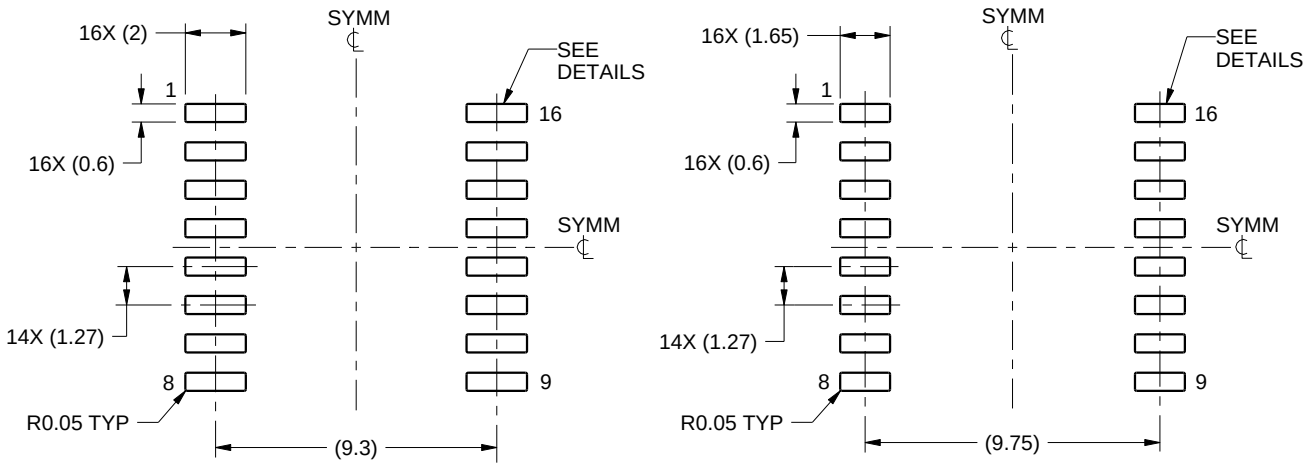
4224780/A

SOIC



NOTES:

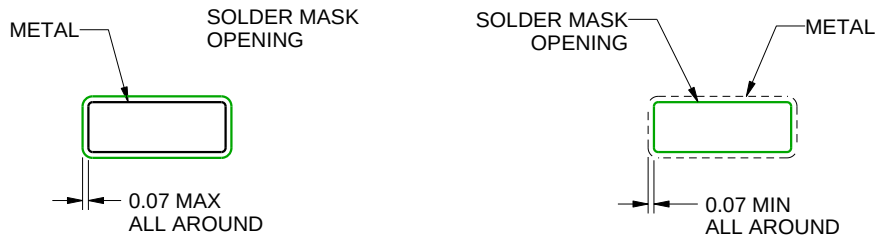
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK DEFINED

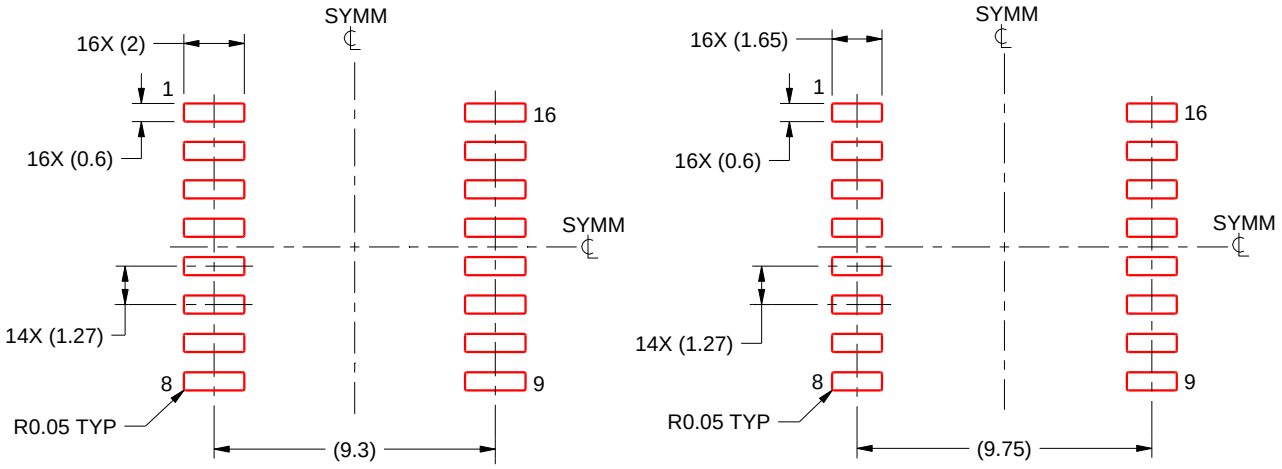
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、 TI の販売条件 、 TI の総合的な品質ガイドライン 、 ti.com または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。 TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

Copyright © 2026, Texas Instruments Incorporated

最終更新日：2025 年 10 月