UCC27200-Q1、車載、8V UVLO (低電圧ロックアウト) 機能搭載、120V、3A/3A、ハーフブリッジ ドライバ

1 特長

- 車載アプリケーション用に AEC-Q100 認定済み:デバイス温度グレード 1
- 接合部温度範囲:-40℃～+150℃
- ハイサイドおよびローサイド構成の 2 つの N チャネル MOSFET を駆動
- 最大ブート電圧:120V
- 最大 V_{DD} 電圧:20V
- オンチップ 0.65V V_F、0.65Ω R_D ブートストラップ ダイオード
- 伝搬遅延時間:22ns
- 3A シンク、3A ソース出力電流
- 立ち上がり時間 8ns、立ち下がり時間 7ns (1000pF 負荷時)
- 遅延マッチング:1ns

2 アプリケーション

- 車載用 DC/DC コンバータと OBC
- 2 輪車と 3 輪車のトラクション ドライブとバッテリ パック
- 電動パワー ステアリング (EPS)
- ワイヤレス充電
- スマート ガラス モジュール

3 説明

UCC27200-Q1 の高周波 N チャネル MOSFET ドライバは、120V のブートストラップ ダイオードと、それぞれ独立した入力を持つハイサイドおよびローサイド ドライバを搭載し、制御の柔軟性を最大限に高めています。これにより、ハーフブリッジ、フルブリッジ、2 スイッチ フォワード、およびアクティブ クランプ フォワードのコンバータで、N チャネル MOSFET 制御が可能です。ローサイドとハイサイドのゲート ドライバが独立して制御され、それぞれのオン / オフ間に 1ns でマッチングが行われます。

ブートストラップ ダイオードを内蔵しているため、外部にディスクリート ダイオードが不要です。ハイサイド ドライバとローサイド ドライバの両方に低電圧誤動作防止機能が搭載され、駆動電圧が規定のスレッショルド未満の場合は出力が強制的に Low になります。

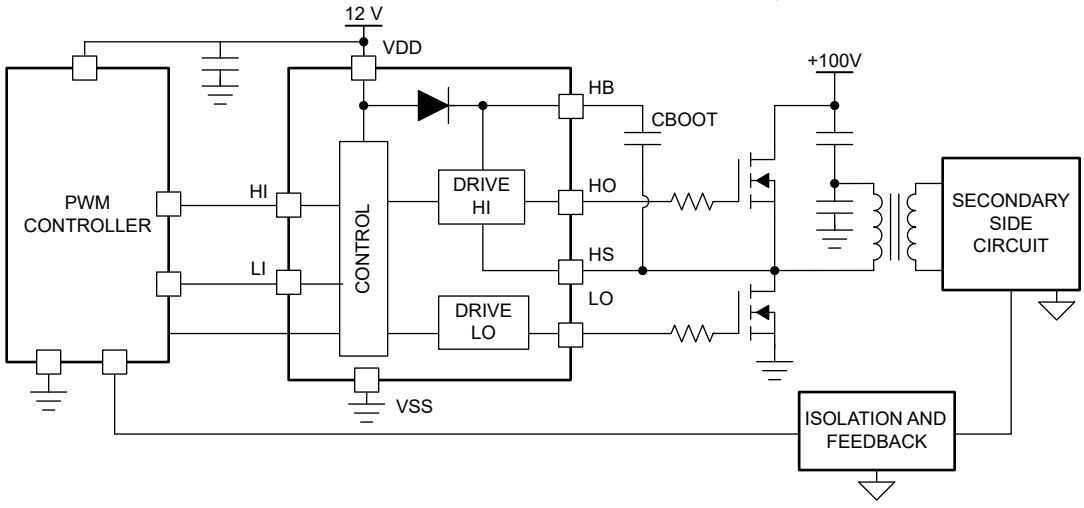
UCC27200-Q1 は、ノイズ耐性の高い CMOS 入力スレッショルドを備えています。

このデバイスは、8 ピン SO PowerPAD™ (DDA) パッケージで供給されます。

製品情報

部品番号	パッケージ (1)	本体サイズ (公称)
UCC27200-Q1	DDA (PowerPAD™ SOIC、8)	4.9mm × 3.9mm

(1) 供給されているすべてのパッケージについては、セクション 12 を参照してください。



アプリケーション概略図

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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4 Pin Configuration and Functions

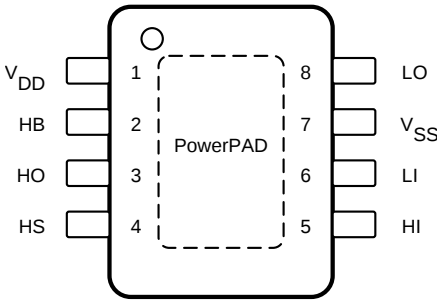

図 4-1. DDA Package 8-Pin SO With PowerPAD Top View

表 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	V_{DD}	P	Positive supply to the lower gate driver. Decouple this pin to V_{SS} (GND). Typical decoupling capacitor range is 0.22µF to 1µF.
2	HB	I	High-side bootstrap supply. The bootstrap diode is on-chip, but the external bootstrap capacitor is required. Connect positive side of the bootstrap capacitor to this pin. Typical range of HB bypass capacitor is 0.022µF to 0.1µF, however, the value is dependant on the gate charge of the high-side MOSFET.
3	HO	O	High-side output. Connect to the gate of the high-side power MOSFET.
4	HS	I	High-side source connection. Connect to source of high-side power MOSFET. Connect negative side of bootstrap capacitor to this pin.
5	HI	I	High-side input
6	LI	I	Low-side input
7	V_{SS}	O	Negative supply terminal for the device which is generally grounded
8	LO	—	Low-side output. Connect to the gate of the low-side power MOSFET.
PowerPAD™ (2)	PowerPAD™	—	Electrically referenced to V_{SS} (GND). Connect to a large thermal mass trace or GND plane to dramatically improve thermal performance.

(1) I = Input, O = Output, P = Power
(2) The thermal pad is not directly connected to any leads of the package; however, it is electrically and thermally connected to the substrate which is the ground of the device.

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5 Specifications

5.1 Absolute Maximum Ratings

Over operating free-air temperature range and all voltages are with respect to V_{ss} (unless otherwise noted).(1)

			MIN	MAX	UNIT
V_{DD}	Supply voltage		–0.3	20	V
V_{HI}, V_{LI}	Input voltages on HI and LI		–0.3	20	V
V_{LO}	Output voltage on LO	DC	–0.3	V_{DD} + 0.3	V
		Repetitive pulse < 100 ns(2)	–2	V_{DD} + 0.3	
V_{HO}	Output voltage on HO	DC	V_{HS} – 0.3	V_{HB} + 0.3	V
		Repetitive pulse < 100 ns(2)	V_{HS} – 2	V_{HB} + 0.3, (V_{HB} - V_{HS} <20)	
V_{HS}	Voltage on HS	DC	–1	120	V
		Repetitive pulse < 100 ns(2)	–5	120	
V_{HB}	Voltage on HB		–0.3	120	V
	Voltage on HB-HS		–0.3	20	V
T_J	Operating junction temperature		–40	150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Values are verified by characterization and are not production tested.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

Over operating free-air temperature range and all voltages are with respect to V_{ss} (unless otherwise noted).

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	8	12	17	V
V_{HS}	Voltage on HS	–1		105	V
	Voltage on HS (repetitive pulse < 100 ns)(1)	–5		110	
V_{HB}	Voltage on HB	V_{HS} + 8.0, V_{DD} – 1		V_{HS} + 17, 115	
SR_{HS}	Voltage slew rate on HS			50	V/ns
T_J	Operating junction temperature	–40		150	°C

(1) Values are verified by characterization and are not production tested.

5.4 Thermal Information

THERMAL METRIC(1)		UCC27200-Q1 DDA (PowerPad™ SOIC) 8 Pins	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	44.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	68.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.9	°C/W

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5.4 Thermal Information (続き)

THERMAL METRIC(1)		UCC27200-Q1 DDA (PowerPad™ SOIC) 8 Pins	UNIT
ψ_{JB}	Junction-to-board characterization parameter	20	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	8.4	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

5.5 Electrical Characteristics

V_{DD} = V_{HB} =12 V, V_{HS} = V_{SS} = 0 V, No load on LO or HO, T_A = T_J = –40°C to +150°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENTS						
I_{DD}	VDD quiescent current	V_{LI} = V_{HI} = 0 V		0.11	0.8	mA
I_{DDO}	VDD operating current	f = 500 kHz, C_{LOAD} = 0		1	3	mA
I_{HB}	Boot voltage quiescent current	V_{LI} = V_{HI} = 0 V		0.065	0.8	mA
I_{HBO}	Boot voltage operating current	f = 500 kHz, C_{LOAD} = 0		0.9	3	mA
I_{HBS}	HB to VSS quiescent current	V_{HS} = V_{HB} = 105 V		0.0005	1	µA
I_{HBSO}	HB to VSS operating current	f = 500 kHz, C_{LOAD} = 0		0.03		mA
INPUT						
V_{HIT}	Input voltage high threshold			6	8	V
V_{LIT}	Input voltage low threshold		3	5.6		V
V_{IHYS}	Input voltage hysteresis			0.4		V
R_{IN}	Input pulldown resistance	V_{IN} = 3V	100	200	350	kΩ
UNDERVOLTAGE PROTECTION (UVLO)						
V_{DDR}	VDD rising threshold		6.2	7.1	7.8	V
V_{DDHYS}	VDD threshold hysteresis			0.5		V
V_{HBR}	VHB rising threshold		5.8	6.7	7.2	V
V_{HBHYS}	VHB threshold hysteresis			0.4		V
BOOTSTRAP DIODE						
V_F	Low-current forward voltage	$I_{VDD - HB}$ = 100 µA		0.65	0.85	V
V_{FI}	High-current forward voltage	$I_{VDD - HB}$ = 100 mA		0.85	1.1	V
R_D	Dynamic resistance, ΔVF/ΔI	$I_{VDD - HB}$ = 120 mA and 100 mA		0.65	1	Ω
LO GATE DRIVER						
V_{LOL}	Low level output voltage	I_{LO} = 100 mA		0.1	0.4	V
V_{LOH}	High level output voltage	I_{LO} = -100 mA, V_{LOH} = V_{DD} – V_{LO}		0.13	0.42	V
	Peak pullup current(1)	V_{LO} = 0 V		3		A
	Peak pulldown current(1)	V_{LO} = 12 V		3		A
HO GATE DRIVER						
V_{HOL}	Low level output voltage	I_{HO} = 100 mA		0.1	0.4	V
V_{HOH}	High level output voltage	I_{HO} = –100 mA, V_{HOH} = V_{HB}- V_{HO}		0.13	0.42	V
	Peak pullup current(1)	V_{HO} = 0 V		3		A
	Peak pulldown current(1)	V_{HO} = 12 V		3		A

(1) Parameter not tested in production.

5.6 Switching Characteristics

V_{DD} = V_{HB} = 12 V, V_{HS} = V_{SS} = 0 V, No load on LO or HO, T_A = T_J = –40°C to +150°C (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PROPAGATION DELAYS					

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5.6 Switching Characteristics (続き)

V_{DD} = V_{HB} = 12 V, V_{HS} = V_{SS} = 0 V, No load on LO or HO, T_A = T_J = –40°C to +150°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DLFF}	VLI falling to VLO falling	C_{LOAD} = 0 pF, from V_{LIT} of LI to 90% of LO falling		22	50	ns
t_{DHFF}	VHI falling to VHO falling	C_{LOAD} = 0 pF, from V_{IT} of HI to 90% of HO falling		22	50	ns
t_{DLRR}	VLI rising to VLO rising	C_{LOAD} = 0 pF, from V_{HIT} of LI to 10% of LO rising		22	50	ns
t_{DHRR}	VHI rising to VHO rising	C_{LOAD} = 0 pF, from V_{HIT} of HI to 10% of HO rising		22	50	ns
DELAY MATCHING						
t_{MON}	LI ON, HI OFF			1	7	ns
t_{MOFF}	LI OFF, HI ON			1	7	ns
OUTPUT RISE AND FALL TIME						
t_{R_LO}	LO rise time	C_{LOAD} = 1000 pF, from 10% to 90%		8		ns
t_{R_HO}	HO rise time	C_{LOAD} = 1000 pF, from 10% to 90%		8		ns
t_{F_LO}	LO fall time	C_{LOAD} = 1000 pF, from 10% to 90%		7		ns
t_{F_HO}	HO fall time	C_{LOAD} = 1000 pF, from 10% to 90%		7		ns
$t_{R_LO_p1}$	LO rise time (3 V to 9 V)	C_{LOAD} = 0.1 µF, (3V to 9V)		0.26	0.6	µs
$t_{R_HO_p1}$	HO rise time (3 V to 9 V)	C_{LOAD} = 0.1 µF, (3V to 9V)		0.26	0.6	µs
$t_{F_LO_p1}$	LO fall time (9 V to 3 V)	C_{LOAD} = 0.1 µF, (9V to 3V)		0.22	0.6	µs
$t_{F_HO_p1}$	HO fall time (9 V to 3 V)	C_{LOAD} = 0.1 µF, (9V to 3V)		0.22	0.6	µs
MISCELLANEOUS						
t_{IN_PW}	Minimum input pulse width that changes the output LO				50	ns
t_{IN_PW}	Minimum input pulse width that changes the output HO				50	ns
t_{OFF_BSD}	Bootstrap diode turnoff time(1) (2)	I_F = 20 mA, I_{REV} = 0.5 A(3)		20		ns

(1) Parameter not tested in production.
(2) Typical values for T_A = 25°C.
(3) I_F: Forward current applied to bootstrap diode, I_{REV}: Reverse current applied to bootstrap diode.

5.7 Timing Diagrams

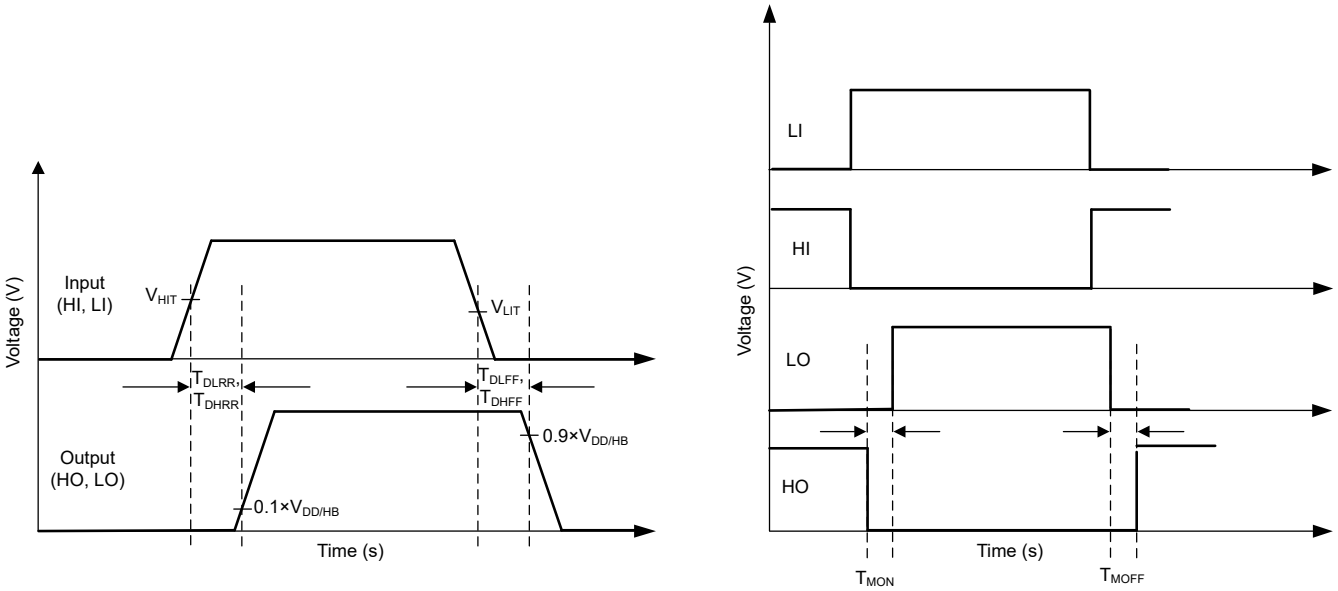

図 5-1. Timing Diagrams

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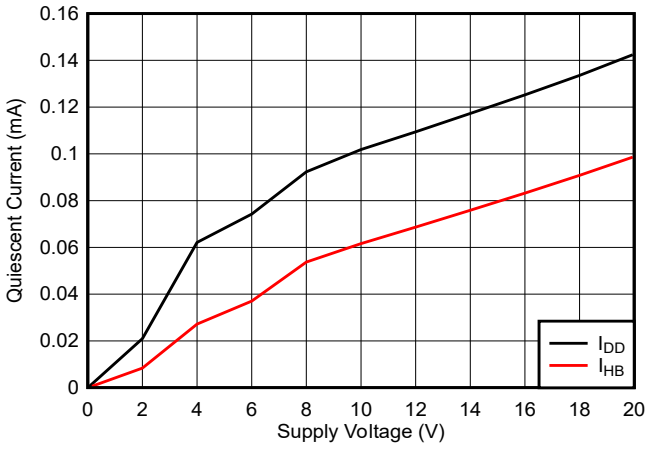
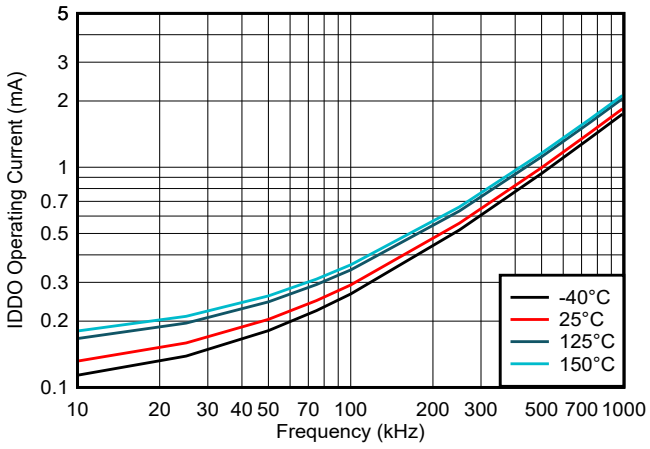
5.8 Typical Characteristics



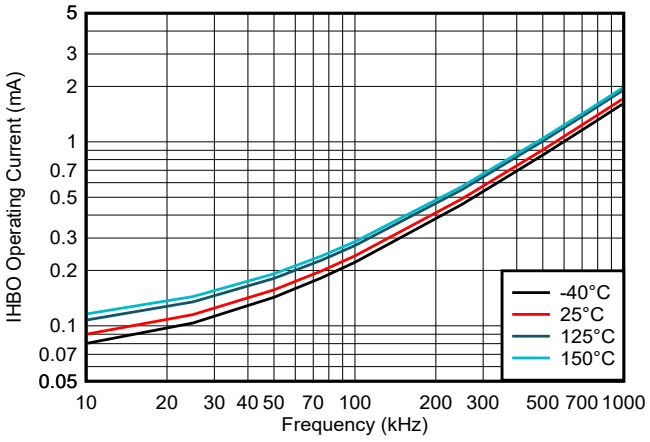
Inputs Low
T = 25°C

図 5-2. Quiescent Current vs Supply Voltage



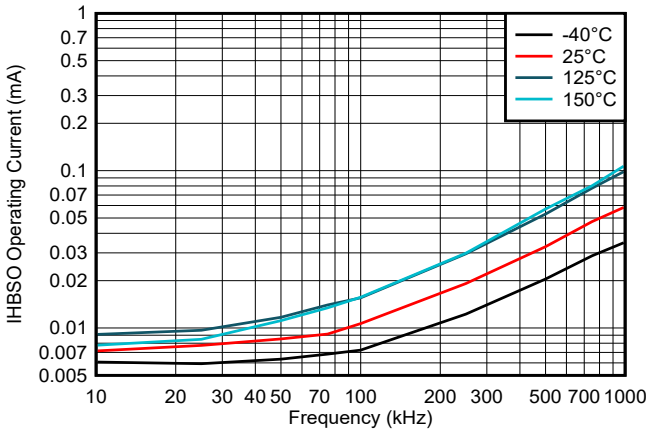
VDD = 12 V
No Load on Outputs

図 5-3. VDD Operating Current vs Frequency



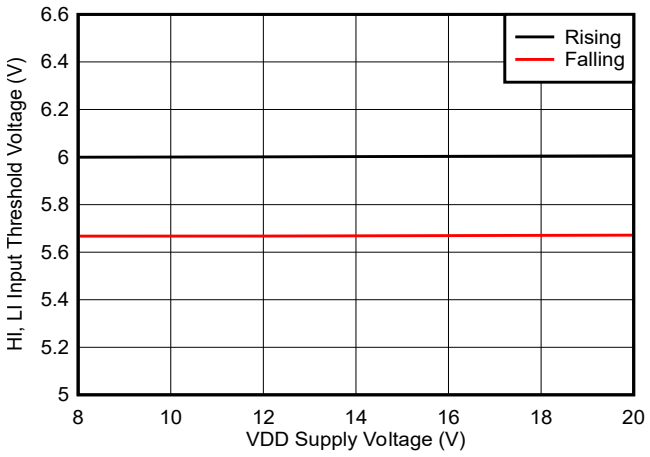
VDD = 12 V
No Load on Outputs

図 5-4. Boot Voltage Operating Current vs Frequency



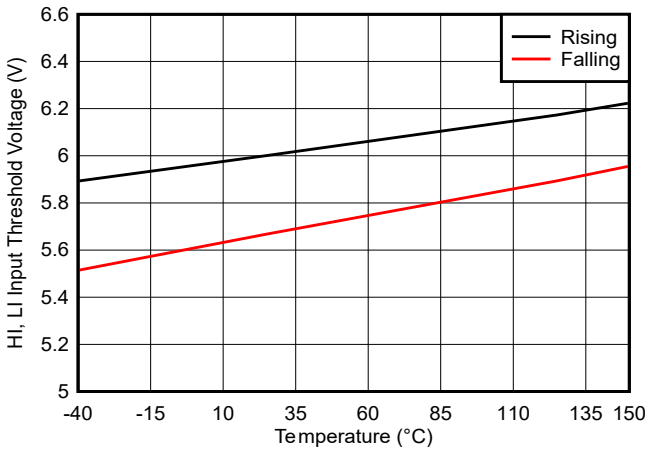
VDD = 12 V
No Load on Outputs

図 5-5. HB to VSS Operating Current vs Frequency



T = 25°C

図 5-6. Input Threshold vs Supply Voltage



VDD = 12 V

図 5-7. Input Threshold vs Temperature

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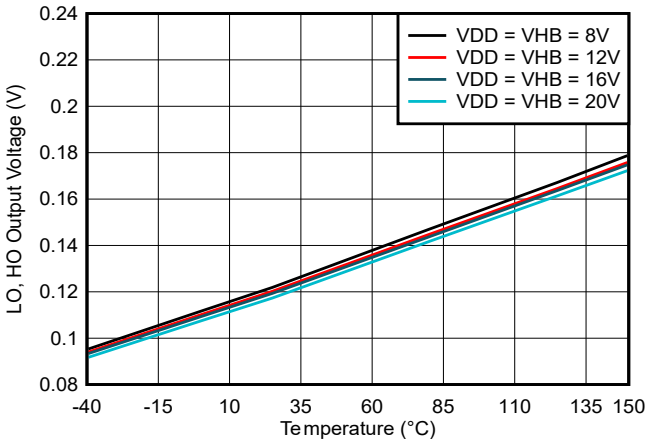
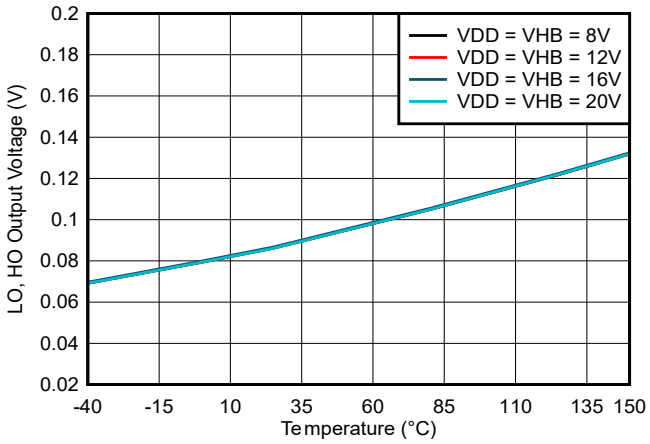
5.8 Typical Characteristics (continued)



I_{LO} = I_{HO} = –100 mA

図 5-8. LO and HO High-Level Output Voltage vs Temperature



I_{LO} = I_{HO} = 100 mA

図 5-9. LO and HO Low-Level Output Voltage vs Temperature

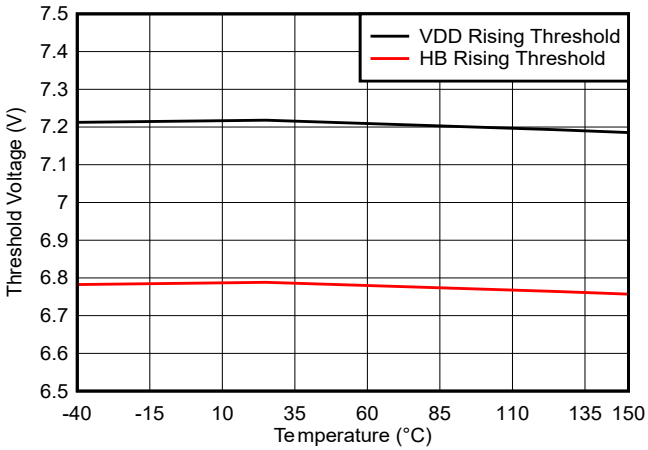


図 5-10. Undervoltage Lockout Threshold vs Temperature

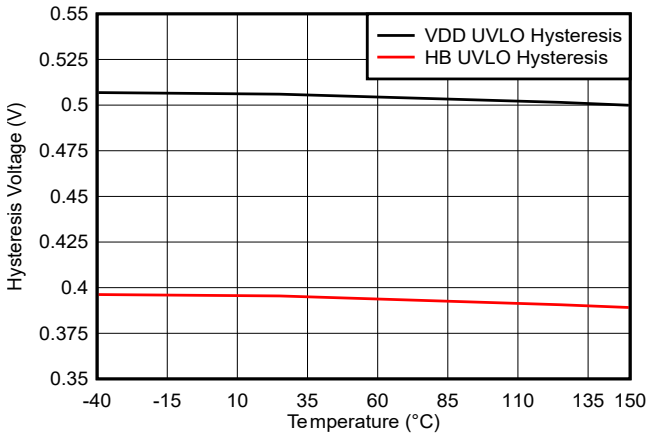
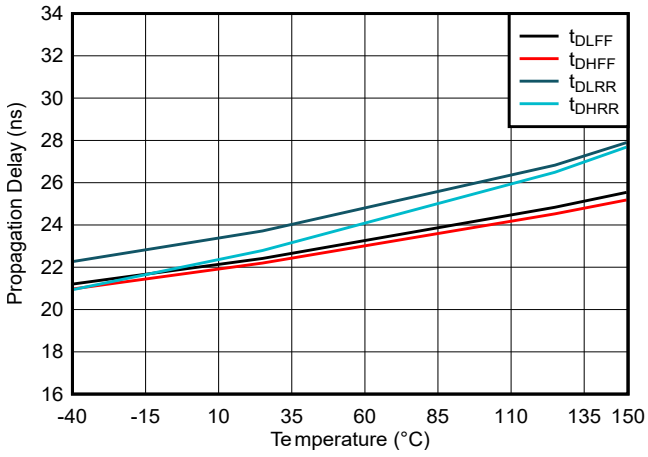
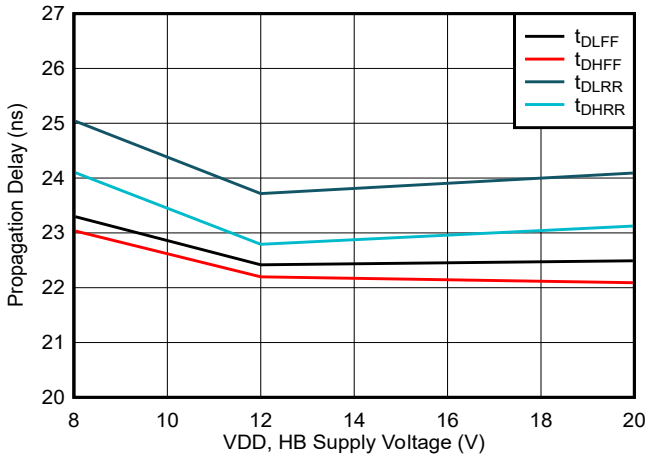


図 5-11. Undervoltage Lockout Threshold Hysteresis vs Temperature



V_{DD} = V_{HB} = 12 V

図 5-12. Propagation Delays vs Temperature



T = 25°C

図 5-13. Propagation Delay vs Supply Voltage

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5.8 Typical Characteristics (continued)

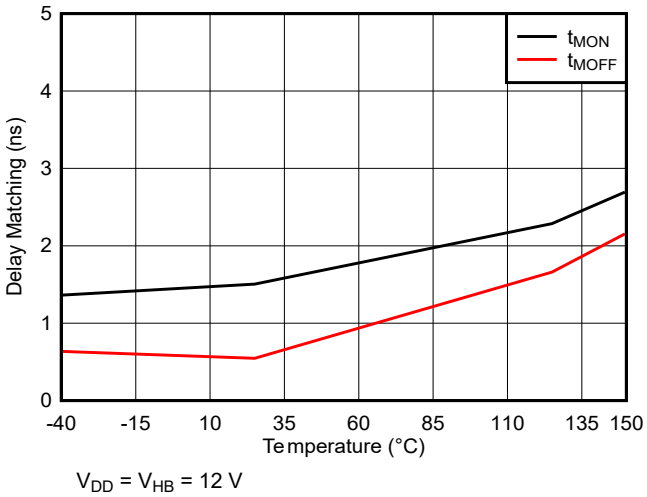

図 5-14. Delay Matching vs Temperature

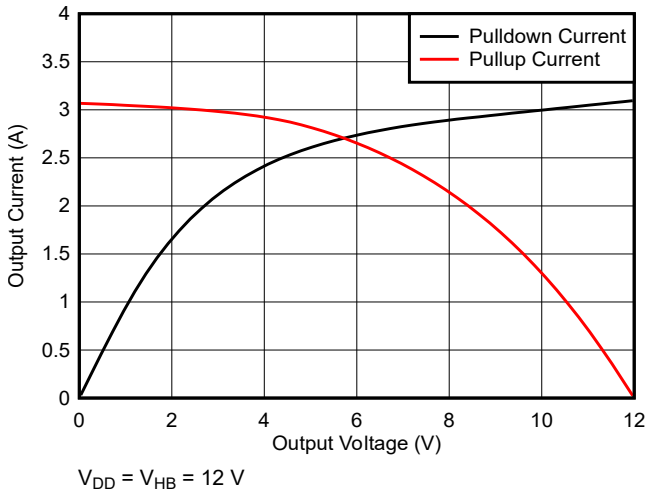

図 5-15. Output Current vs Output Voltage

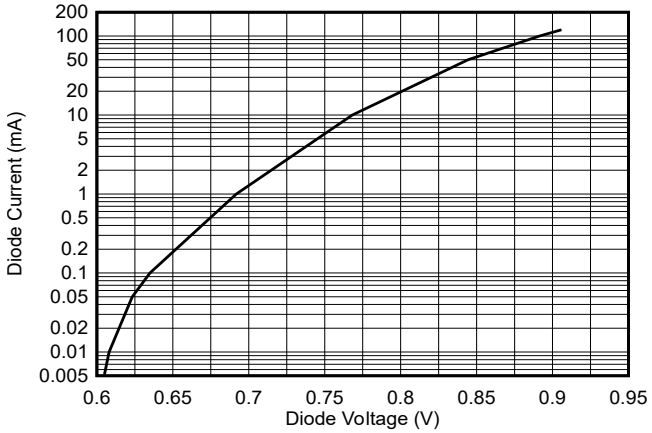

図 5-16. Diode Current vs Diode Voltage

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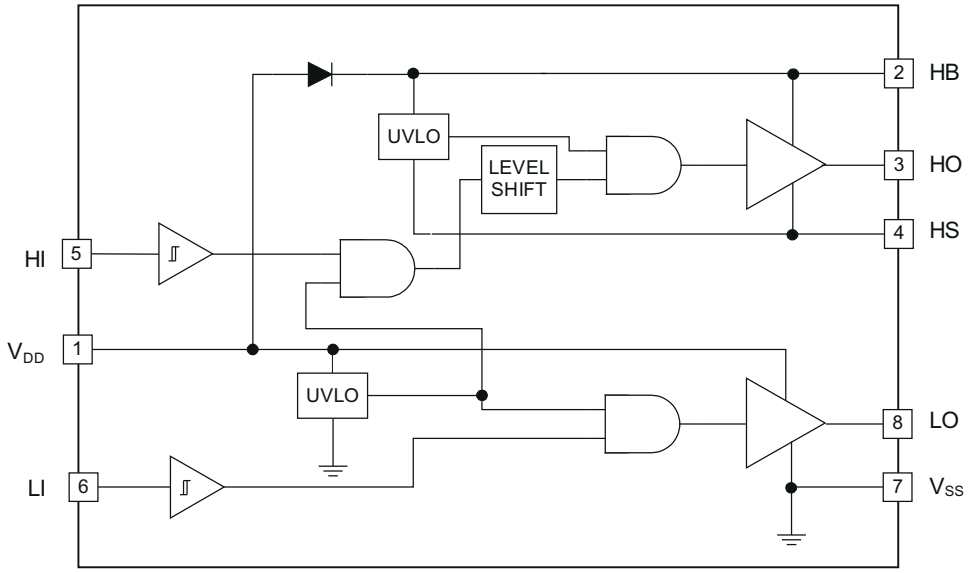
6 Detailed Description

6.1 Overview

The UCC27200-Q1 device is a high-side and low-side driver. The high-side and low-side each have independent inputs, which allow maximum flexibility of input control signals in the application. The boot diode for the high-side driver bias supply is internal to the UCC27200-Q1. This device has CMOS-compatible inputs. The high-side driver is referenced to the switch node (HS), which is typically the source pin of the high-side MOSFET and drain pin of the low-side MOSFET. The low-side driver is referenced to V_{SS}, which is typically ground. The functions contained are the input stages, UVLO protection, level shift, boot diode, and output driver stages.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Input Stages

The input stages provide the interface to the PWM output signals. The input impedance of the UCC27200-Q1 is 200kΩ nominal and input capacitance is approximately 4pF. The 200kΩ is a pulldown resistance to V_{SS} (ground). The CMOS-compatible input of the UCC27200-Q1 provides a rising threshold of 6V and a falling threshold of 5.6V. The inputs of the UCC27200-Q1 are intended to be driven from 0 to V_{DD} levels.

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6.3.2 Undervoltage Lockout (UVLO)

The bias supplies for the high-side and low-side drivers have UVLO protection. V_{DD} as well as V_{HB} to V_{HS} differential voltages are monitored. The V_{DD} UVLO disables both drivers when V_{DD} is below the specified threshold. The rising V_{DD} threshold is 7.1V with 0.5V hysteresis. The V_{HB} UVLO disables only the high-side driver when the V_{HB} to V_{HS} differential voltage is below the specified threshold. The V_{HB} UVLO rising threshold is 6.7V with 0.4V hysteresis.

6.3.3 Level Shift

The level-shift circuit is the interface from the high-side input to the high-side driver stage, which is referenced to the switch node (HS). The level shift allows control of the HO output referenced to the HS pin and provides excellent delay matching with the low-side driver.

6.3.4 Boot Diode

The boot diode necessary to generate the high-side bias is included in the UCC27200-Q1 family of drivers. The diode anode connects to V_{DD} and the cathode connects to VHB. With the VHB capacitor connected to HB and the HS pins, the V_{HB} capacitor charge refreshes every switching cycle when HS transitions to ground. The boot diode provides fast recovery times, low diode resistance, and a voltage rating margin that allow for efficient and reliable operation.

6.3.5 Output Stages

The output stages are the interface to the power MOSFETs in the power train. High-slew rate, low resistance, and high-peak current capability of both output drivers allow for efficient switching of the power MOSFETs. The low-side output stage reference is from V_{DD} to V_{SS} and the high-side output stage reference is from V_{HB} to V_{HS}.

6.4 Device Functional Modes

The device operates in normal mode and UVLO mode. See *Undervoltage Lockout (UVLO)* for information on UVLO operation mode. In the normal mode, the output state is dependent on states of the HI and LI pins. 表 6-1 lists the output states for different input pin combinations.

表 6-1. Device Logic Table

HI PIN	LI PIN	HO(1)	LO(2)
L	L	L	L
L	H	L	H
H	L	H	L
H	H	H	H

(1) HO is measured with respect to HS.
(2) LO is measured with respect to V_{SS}.

7 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

7.1 Application Information

To enable fast switching of power devices and reduce associated switching power losses, a powerful gate driver is employed between the PWM output of controllers and the gates of the power semiconductor devices. Also, gate drivers are indispensable when it is impossible for the PWM controller to directly drive the gates of the switching devices. With the advent of digital power, this situation will be often encountered because the PWM signal from the digital controller is often a 3.3V logic signal which cannot effectively turn on a power switch. Level shifting circuitry is needed to boost the 3.3V signal to the gate-drive voltage (such as 12V) to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN/PNP bipolar transistors in totem-pole arrangement, being emitter follower configurations, prove inadequate with digital power because they lack level-shifting capability. Gate drivers effectively combine both the level-shifting and buffer-drive functions. Gate drivers also find other needs such as minimizing the effect of high-frequency switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers, and controlling floating power-device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses from the controller into the driver.

7.2 Typical Application

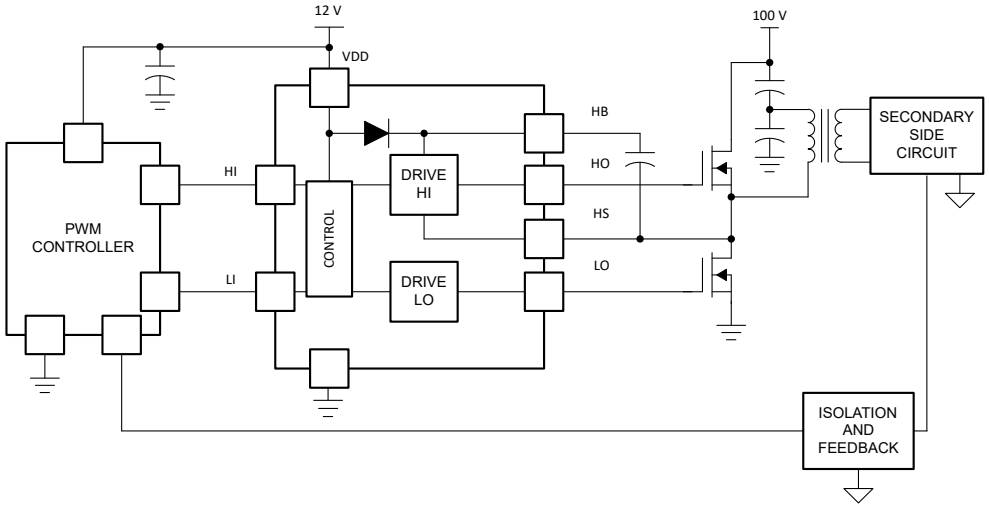

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図 7-1. UCC27200-Q1 Typical Application Diagram

7.2.1 Design Requirements

For this design example, use the parameters listed in 表 7-1.

表 7-1. Design Specifications

DESIGN PARAMETER	EXAMPLE VALUE
Supply voltage, VDD	12V
Voltage on HS, VHS	0V to 100V
Voltage on HB, VHB	12V to 112V
Output current rating, IO	–3A to 3A

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表 7-1. Design Specifications (続き)

DESIGN PARAMETER	EXAMPLE VALUE
Operating frequency	200kHz

7.2.2 Detailed Design Procedure

7.2.2.1 Input Threshold Type

The UCC27200-Q1 device features CMOS compatible input threshold logic with wide hysteresis. The threshold voltage levels are low voltage and independent of the VDD supply voltage, which allows compatibility with both logic-level input signals from microcontrollers as well as higher-voltage input signals from analog controllers. See the Electrical Characteristics table for the actual input threshold voltage levels and hysteresis specifications for the UCC27200-Q1 device.

7.2.2.2 V_{DD} Bias Supply Voltage

The bias supply voltage to be applied to the VDD pin of the device should never exceed the values listed in the Absolute Maximum Ratings table. Different power switches demand different voltage levels to be applied at the gate terminals for effective turnon and turnoff. With certain power switches, a positive gate voltage may be required for turnon and a negative gate voltage may be required for turnoff, in which case the VDD bias supply equals the voltage differential. With a wide operating range from 8V to 17V, the UCC27200-Q1 device can be used to drive a variety of power switches, such as Si MOSFETs, IGBTs, and wide-bandgap power semiconductors.

7.2.2.3 Peak Source and Sink Currents

Generally, the switching speed of the power switch during turnon and turnoff should be as fast as possible in order to minimize switching power losses. The gate driver device must be able to provide the required peak current for achieving the targeted switching speeds with the targeted power MOSFET. The system requirement for the switching speed is typically described in terms of the slew rate of the drain-to-source voltage of the power MOSFET (such as dV_{DS}/dt). For example, the system requirement might state that a SPP20N60C3 power MOSFET must be turned-on with a dV_{DS}/dt of 20V/ns or higher with a DC bus voltage of 400V in a continuous-conduction-mode (CCM) boost PFC-converter application. This type of application is an inductive hard-switching application and reducing switching power losses is critical. This requirement means that the entire drain-to-source voltage swing during power MOSFET turnon event (from 400V in the OFF state to $V_{DS(on)}$ in on state) must be completed in approximately 20ns or less. When the drain-to-source voltage swing occurs, the Miller charge of the power MOSFET (QGD parameter in the SPP20N60C3 data sheet is 33nC typical) is supplied by the peak current of gate driver. According to power MOSFET inductive switching mechanism, the gate-to-source voltage of the power MOSFET at this time is the Miller plateau voltage, which is typically a few volts higher than the threshold voltage of the power MOSFET, $V_{GS(TH)}$.

To achieve the targeted dV_{DS}/dt, the gate driver must be capable of providing the Q_{GD} charge in 20ns or less. In other words a peak current of 1.65A (= 33nC / 20ns) or higher must be provided by the gate driver. The UCC27200-Q1 gate driver is capable of providing 3A peak sourcing current which clearly exceeds the design requirement and has the capability to meet the switching speed needed. The overdrive capability provides an extra margin against part-to-part variations in the Q_{GD} parameter of the power MOSFET along with additional flexibility to insert external gate resistors and fine tune the switching speed for efficiency versus EMI optimizations. However, in practical designs the parasitic trace inductance in the gate drive circuit of the PCB will have a definitive role to play on the power MOSFET switching speed. The effect of this trace inductance is to limit the dI/dt of the output current pulse of the gate driver. In order to illustrate this, consider output current pulse waveform from the gate driver to be approximated to a triangular profile, where the area under the triangle (½ × I_{PEAK} × time) would equal the total gate charge of the power MOSFET (QG parameter in SPP20N60C3 power MOSFET datasheet = 87nC typical). If the parasitic trace inductance limits the dI/dt then a situation may occur in which the full peak current capability of the gate driver is not fully achieved in the time required to deliver the QG required for the power MOSFET switching. In other words the time parameter in the equation would dominate and the I_{PEAK} value of the current pulse would be much less than the true peak current capability of the device, while the required QG is still delivered. Because of this, the desired switching speed may not be realized,

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even when theoretical calculations indicate the gate driver is capable of achieving the targeted switching speed. Thus, placing the gate driver device very close to the power MOSFET and designing a tight gate drive-loop with minimal PCB trace inductance is important to realize the full peak-current capability of the gate driver.

7.2.2.4 Propagation Delay

The acceptable propagation delay from the gate driver is dependent on the switching frequency at which it is used and the acceptable level of pulse distortion to the system. The UCC27200-Q1 device features 22ns (typical) propagation delays, which ensures very little pulse distortion and allows operation at very high-frequencies. See the Electrical Characteristics table for the propagation and switching characteristics of the UCC27200-Q1 device.

7.2.2.5 Power Dissipation

Power dissipation of the gate driver has two portions as shown in 式 1.

$$P_{DISS} = P_{DC} + P_{SW} \quad (1)$$

Use 式 2 to calculate the DC portion of the power dissipation (PDC).

$$PDC = I_Q \times V_{DD} \quad (2)$$

where

- I_Q is the quiescent current for the driver.

The quiescent current is the current consumed by the device to bias all internal circuits such as input stage, reference voltage, logic circuits, protections, and also any current associated with switching of internal devices when the driver output changes state (such as charging and discharging of parasitic capacitances, parasitic shoot-through, and so forth). The UCC27200-Q1 features very low quiescent currents (refer to the Electrical Characteristics table) and contain internal logic to eliminate any shoot-through in the output driver stage. Thus the effect of the PDC on the total power dissipation within the gate driver can be safely assumed to be negligible. The power dissipated in the gate-driver package during switching (PSW) depends on the following factors:

- Gate charge required of the power device (usually a function of the drive voltage VG, which is very close to input bias supply voltage VDD)
- Switching frequency
- Use of external gate resistors. When a driver device is tested with a discrete, capacitive load calculating the power that is required from the bias supply is fairly simple. The energy that must be transferred from the bias supply to charge the capacitor is given by 式 3.

$$EG = ½C_{LOAD} \times V_{DD}^{\ 2} \quad (3)$$

  - where
  - C_{LOAD} is load capacitor
  - V_{DD} is bias voltage feeding the driver

There is an equal amount of energy dissipated when the capacitor is charged and when it is discharged. This leads to a total power loss given by 式 4.

$$PG = C_{LOAD} \times V_{DD}^{\ 2} \times f_{SW} \quad (4)$$

where

- f_{SW} is the switching frequency

The switching load presented by a power MOSFET/IGBT is converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Most manufacturers provide specifications of typical and maximum gate

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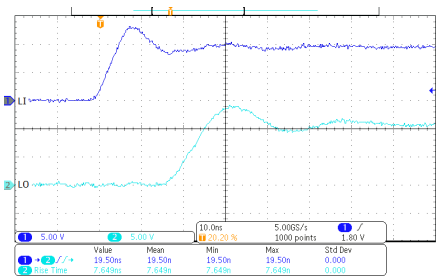
charge, in nC, to switch the device under specified conditions. Using the gate charge Qg, determine the power that must be dissipated when switching a capacitor which is calculated using the equation $Q_G = C_{LOAD} \times V_{DD}$ to provide 式 5 for power.

$$P_G = C_{LOAD} \times V_{DD}^{\ 2} \times f_{SW} = Q_G \times V_{DD} \times f_{SW} \quad (5)$$

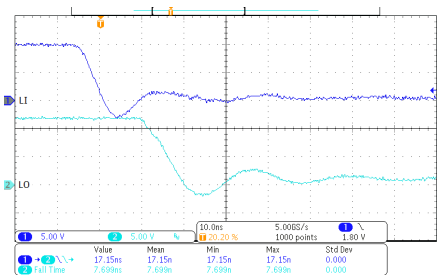
This power P_G is dissipated in the resistive elements of the circuit when the MOSFET/IGBT is being turned on and off. Half of the total power is dissipated when the load capacitor is charged during turnon, and the other half is dissipated when the load capacitor is discharged during turnoff. When no external gate resistor is employed between the driver and MOSFET/IGBT, this power is completely dissipated inside the driver package. With the use of external gate-drive resistors, the power dissipation is shared between the internal resistance of driver and external gate resistor.

7.2.3 Application Curves



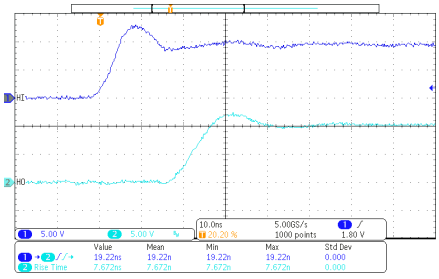
C_L = 1nF V_{DD} = 12 V

図 7-2. LO Rise Time and LI to LO Turn-on Propagation Delay



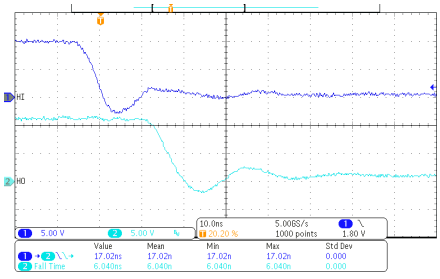
C_L = 1nF V_{DD} = 12V

図 7-3. LO Fall Time and LI to LO Turn-off Propagation Delay



C_L = 1nF V_{DD} = 12V

図 7-4. HO Rise Time and HI to HO Turn-on Propagation Delay



C_L = 1nF V_{DD} = 12V

図 7-5. HO Fall Time and HI to HO Turn-off Propagation Delay

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8 Power Supply Recommendations

The bias supply voltage range for which the device is recommended to operate is from 8V to 17V. The lower end of this range is governed by the internal undervoltage-lockout (UVLO) protection feature on the V_{DD} pin supply circuit blocks. Whenever the driver is in UVLO condition when the V_{DD} pin voltage is below the $V_{(ON)}$ supply start threshold, this feature holds the output low, regardless of the status of the inputs. The upper end of this range is driven by the 20V absolute maximum voltage rating of the V_{DD} pin of the device (which is a stress rating). Keeping a 3V margin to allow for transient voltage spikes, the maximum recommended voltage for the V_{DD} pin is 17V. The UVLO protection feature also involves a hysteresis function, which means that when the V_{DD} pin bias voltage has exceeded the threshold voltage and device begins to operate, and if the voltage drops, then the device continues to deliver normal functionality unless the voltage drop exceeds the hysteresis specification $V_{DD(hys)}$. Therefore, ensuring that, while operating at or near the 8V range, the voltage ripple on the auxiliary power supply output is smaller than the hysteresis specification of the device is important to avoid triggering device shutdown. During system shutdown, the device operation continues until the V_{DD} pin voltage has dropped below the $V_{(OFF)}$ threshold, which must be accounted for while evaluating system shutdown timing design requirements. Likewise, at system start-up the device does not begin operation until the V_{DD} pin voltage has exceeded the $V_{(ON)}$ threshold.

The quiescent current consumed by the internal circuit blocks of the device is supplied through the V_{DD} pin. Although this fact is well known, it is important to recognize that the charge for source current pulses delivered by the LO pin is also supplied through the same V_{DD} pin. As a result, every time a current is sourced out of the LO pin, a corresponding current pulse is delivered into the device through the V_{DD} pin. Thus, ensure that a local bypass capacitor is provided between the V_{DD} and GND pins and located as close to the device as possible for the purpose of decoupling is important. A low ESR, ceramic surface-mount capacitor is required. TI recommends using a capacitor in the range from 0.22µF to 4.7µF between V_{DD} and GND. In a similar manner, the current pulses delivered by the HO pin are sourced from the HB pin. Therefore, TI recommends placing a 0.022µF to 0.1µF local decoupling capacitor between the HB and HS pins.

9 Layout

9.1 Layout Guidelines

To improve the switching characteristics and efficiency of a design, the following layout rules must be followed.

- Locate the driver as close as possible to the MOSFETs.
- Locate the V_{DD} and V_{HB} (bootstrap) capacitors as close as possible to the driver.
- Pay close attention to the GND trace. Use the thermal pad of the DDA package as GND by connecting it to the V_{SS} pin (GND).

注

The GND trace from the driver goes directly to the source of the MOSFET, but must not be in the high-current path of the MOSFET(S) drain or source current.

- Use similar rules for the HS node as for GND for the high-side driver.
- Use wide traces for LO and HO closely following the associated GND or HS traces. Where possible, widths of 60mil to 100mil are preferred.
- Use two or more vias if the driver outputs or SW node must be routed from one layer to another. For GND, consider the number of vias of the thermal pad requirements of the thermal pad requirements as well as parasitic inductance.
- Avoid L_I and H_I (driver input) going close to the HS node or any other high dV/dT traces that can induce significant noise into the relatively high-impedance leads.
- Keep in mind that a poor layout can cause a significant drop in efficiency versus a good PCB layout and can even lead to decreased reliability of the whole system.

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9.2 Layout Example

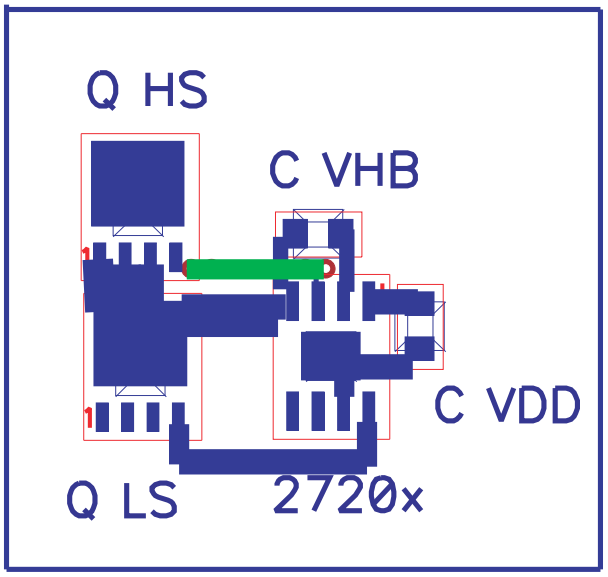

図 9-1. Example Component Placement

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For more related documentation, see the following:

- *PowerPAD™ Thermally Enhanced Package* (SLMA002)
- *PowerPAD™ Made Easy* (SLMA004)

10.2 ドキュメントの更新通知を受け取る方法

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11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (August 2016) to Revision D (July 2024) **Page**

- デバイスの主な特長を反映するようにドキュメントのタイトルを変更。また、このデータシートは 1 つの型番のみに対応しているため、デバイスの型番を変更 (修正前：UCC2720x-Q1。修正後：UCC27200-Q1)。デバイスの特性を反映するように仕様の一部を更新。このデータシートから UCC27201-Q1 デバイスの記述を削除 1
- ドキュメント全体にわたって表、図、相互参照の採番方法を更新 1
- 「特長」セクションを変更：1) 最新の TI データシート標準に従うように HBM および CDM ESD 分類レベルを削除。2) 接合部温度範囲の仕様を変更 (修正前：-40℃～140℃。修正後：–40℃～150℃)。4) 伝搬遅延の標準値を変更 (修正前：20ns。修正後：22ns)。5)「1MHz を超える動作」の記述を削除 (このスイッチング周波数は規定のパラメータではないため)。6) ブートストラップ ダイオード抵抗の標準値を変更 (修正前：0.6Ω。修正後：0.65Ω) 1
- 「アプリケーション」セクションを更新して代表的なアプリケーションの上位 5 つを記載 1
- 「概要」セクションを変更して、UCC2720x-Q1 を UCC27200-Q1 に置き換え、UCC27201-Q1 の記述を削除 1
- Changed Pin Functions table with a change to the power pad description. 3
- Updated Absolute Maximum Ratings section to remove "Power dissipation at TA = 25°C" and "Lead temperature (soldering, 10s)". Power dissipation can be calculated with thermal metrics in "Thermal Information" table. 4
- Updated Recommended Operating Conditions: Operating Junction Temperature maximum changed from 140°C to 150°C, and removed Operating Ambient Temperature. 4
- Updated Thermal Information section to reflect device characteristics. 4
- Updated Supply Currents specifications in the Electrical Characteristics table: 1) I_{DD} typical changed (From: 0.4mA. To: 0.11mA). 2) UC27200-Q1 I_{DDO} typical changed (From: 2.5mA. To: 1mA). 3) UCC27200-Q1 I_{DDO} maximum changed (From: 4mA. To: 3mA. 4) I_{HB} typical changed (From: 0.4mA. To: 0.065mA). 5) I_{HBO} typical changed (From: 2.5mA. To: 0.9mA). 6) I_{HBO} maximum changed (From: 4mA. To: 3mA). 7) I_{HBS} test condition changed to match V_{HS} maximum recommended operating conditions (From: 110V. To: 105V). 8) I_{HBSO} typical changed (From: 0.1mA. To: 0.03mA). 4
- Updated Input specifications in the Electrical Characteristics table: 1) UCC27200-Q1 V_{HIT} typical changed (From: 5.8V. To: 6V). 2) UCC27200-Q1 V_{LIT} typical changed (From: 5.4V. To: 5.6V). 4
- Updated Bootstrap diode specifications in the Electrical Characteristics table: 1) R_D test conditions changed (From: 100mA and 80mA. To: 120mA and 100mA). 2) R_D typical changed (From: 0.6Ω. To: 0.65Ω). 4
- Updated LO/HO Gate Driver specifications in the Electrical Characteristics table: 1) V_{LOL} typical changed (From 0.18V. To 0.1V). 2) V_{LOH} typical changed (From: 0.25V. To: 0.13V). 4
- Removed specifications with test conditions "-40°C to 125°C T_J", since all parameters are specified from -40°C to 150°C T_J (unless otherwise noted). Changed Propagation Delays typical specification (From: 20ns. To: 22ns). 4
- Updated Output Rise and Fall Time specifications: 1) t_R typical changed (From: 0.35us. To: 0.26us). 2) t_F typical changed (From: 0.3us. To: 0.22us). 4
- Updated all plots in Typical Characteristics section to reflect the device's typical specification. 7
- Updated Typical Application section to display a different application diagram and detailed design procedure since information in legacy data sheet had an outdated circuit with obsolete part numbers. 12
- Changed application curves to display propagation delay and rise/fall time plots. 15
- Updated Power Supply Recommendations section to fix 3 typos. 16

Changes from Revision B (March 2016) to Revision C (August 2016) **Page**

- 「特長」セクションのデバイス温度グレードをグレード 0 (–40℃～150℃) からグレード 1 (–40℃～125℃) に変更 1
- Added the *Receiving Notification of Documentation Updates* section 18

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Changes from Revision A (November 2008) to Revision B (March 2016) **Page**

- 「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加 1
- AEC-Q100 認定の箇条書きを追加 1
- デバイス番号 UCC2720x および UCC27200 を UCC2720x-Q1 および UCC27200-Q1 に変更 1
- Moved references from *Additional References* section to *Related Documentation* section 18

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC27200QDDARQ1	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 150	27200Q
UCC27200QDDARQ1.A	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	27200Q
UCC27200QDDARQ1.B	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	27200Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF UCC27200-Q1 :

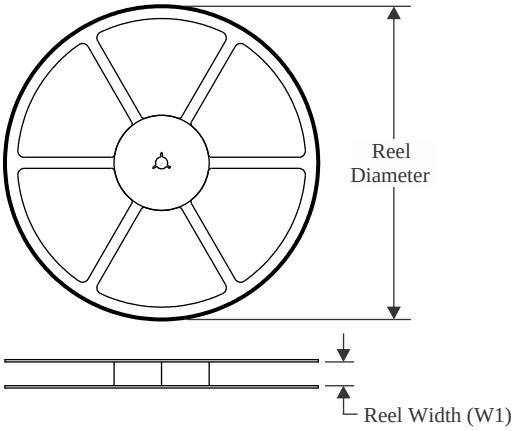
- Catalog : UCC27200

NOTE: Qualified Version Definitions:

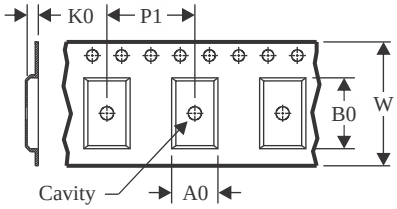
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

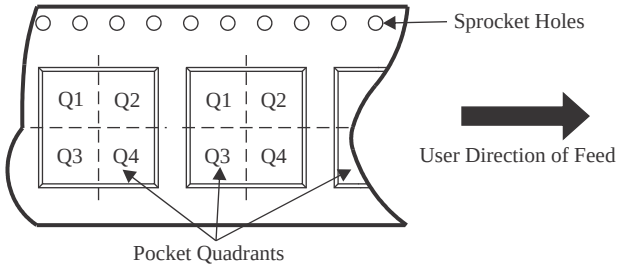


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

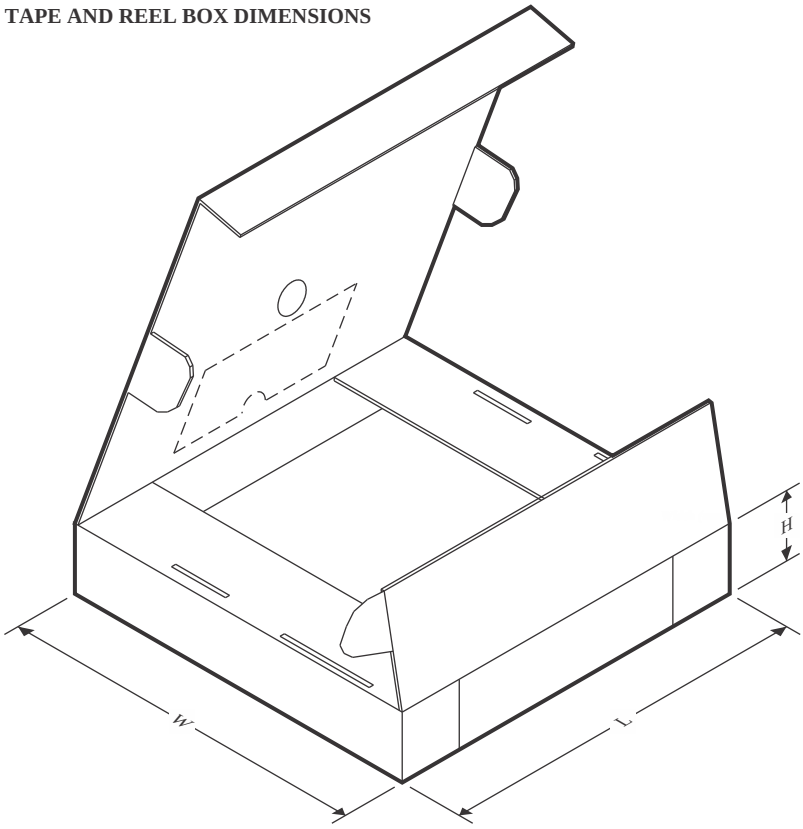
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27200QDDARQ1	SO PowerPAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

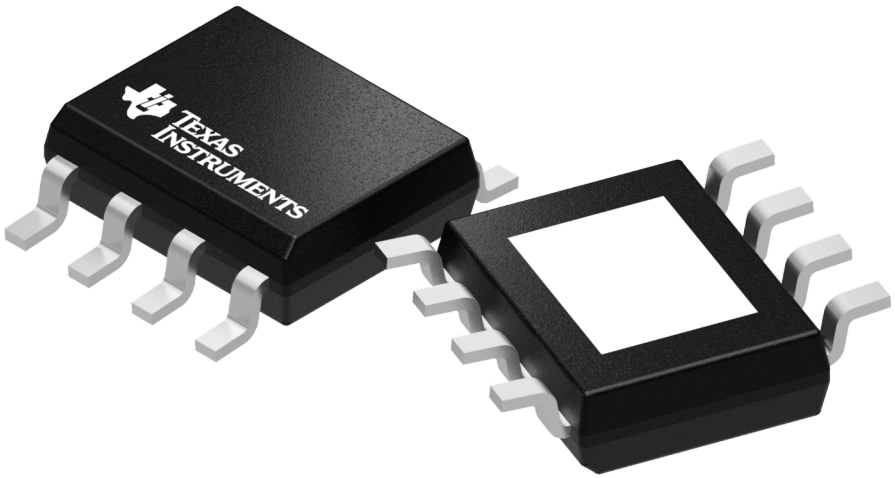


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27200QDDARQ1	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0

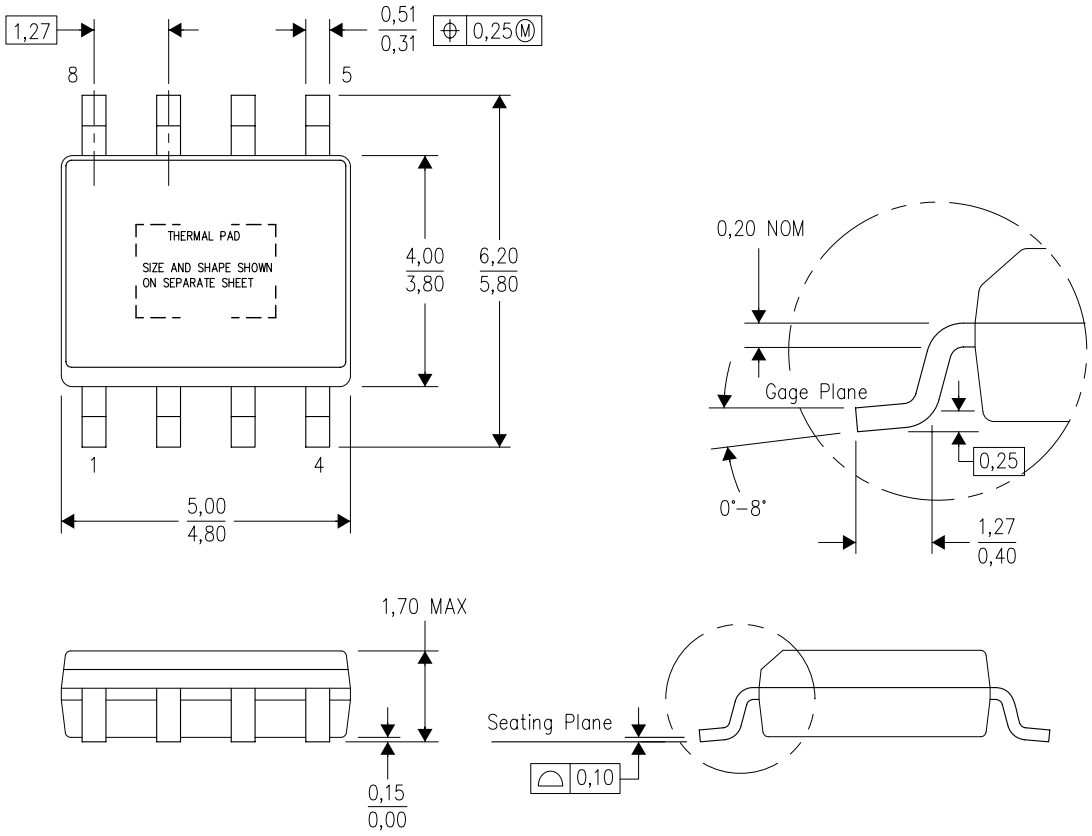
DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS–012 variation BA

PowerPAD is a trademark of Texas Instruments.

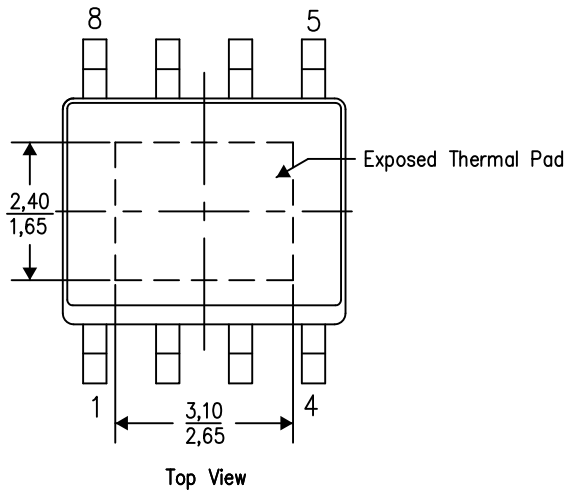
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



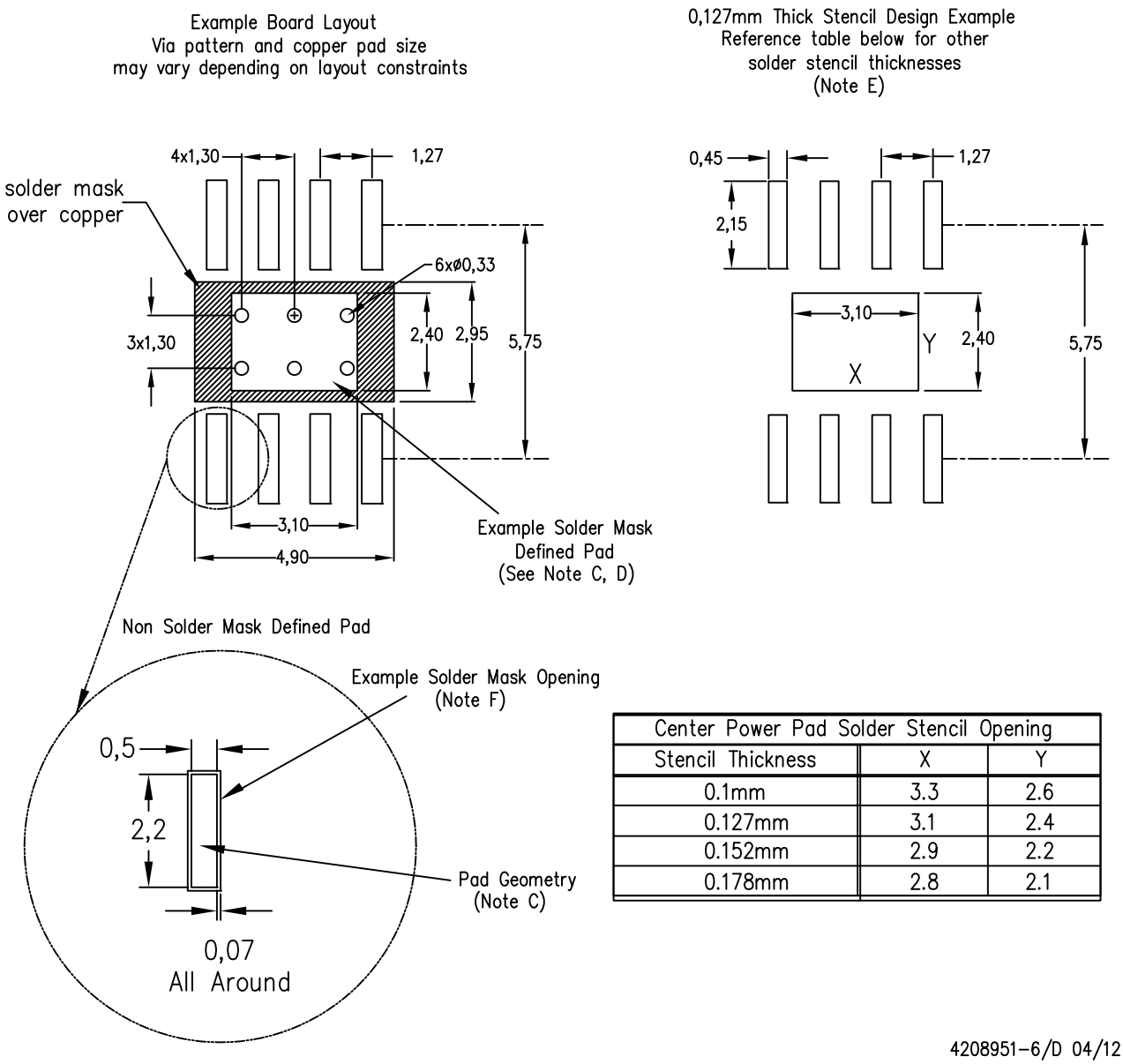
Exposed Thermal Pad Dimensions

4206322–6/L 05/12

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.3	2.6
0.127mm	3.1	2.4
0.152mm	2.9	2.2
0.178mm	2.8	2.1

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

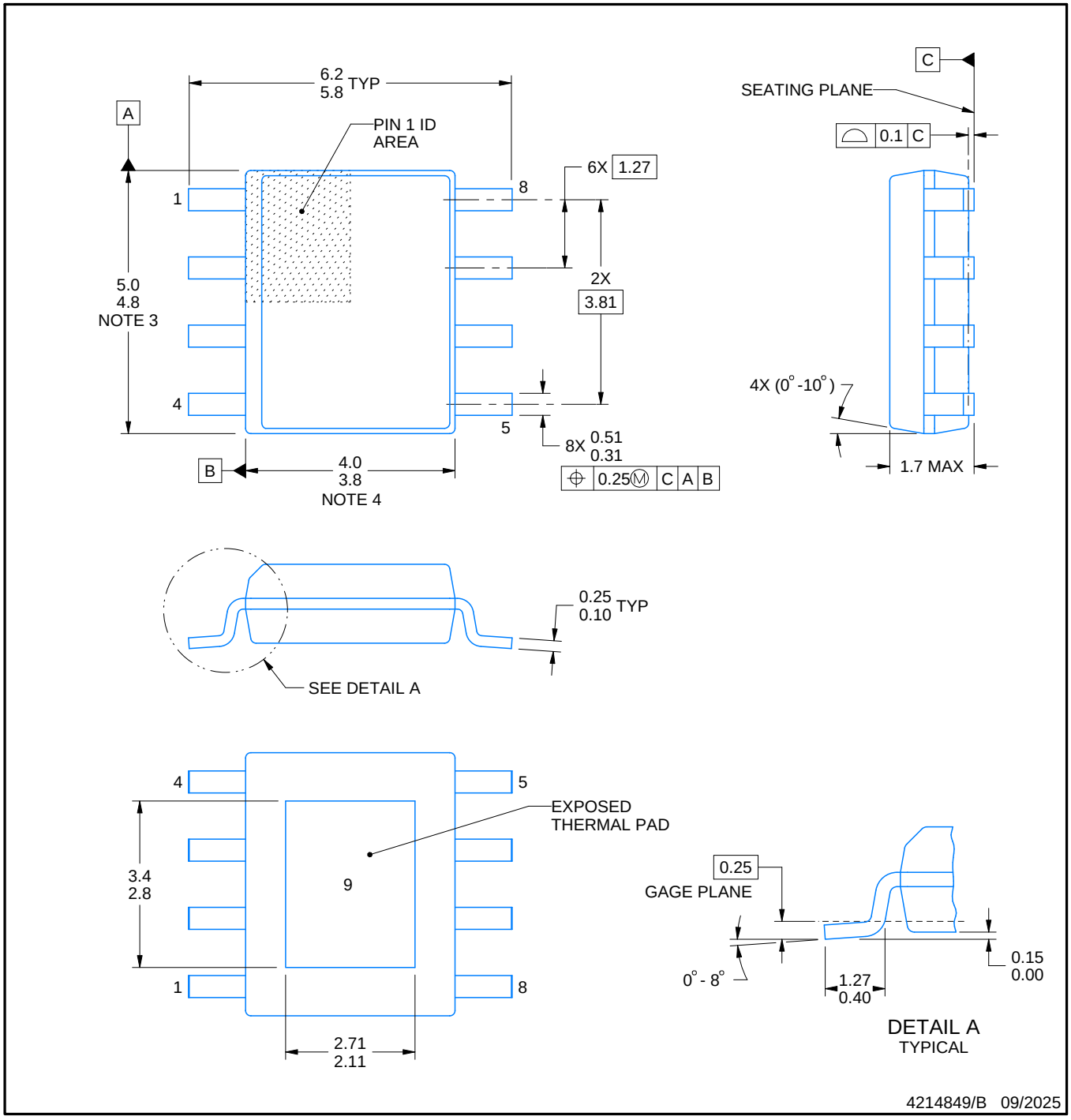
PowerPAD is a trademark of Texas Instruments.

PACKAGE OUTLINE

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

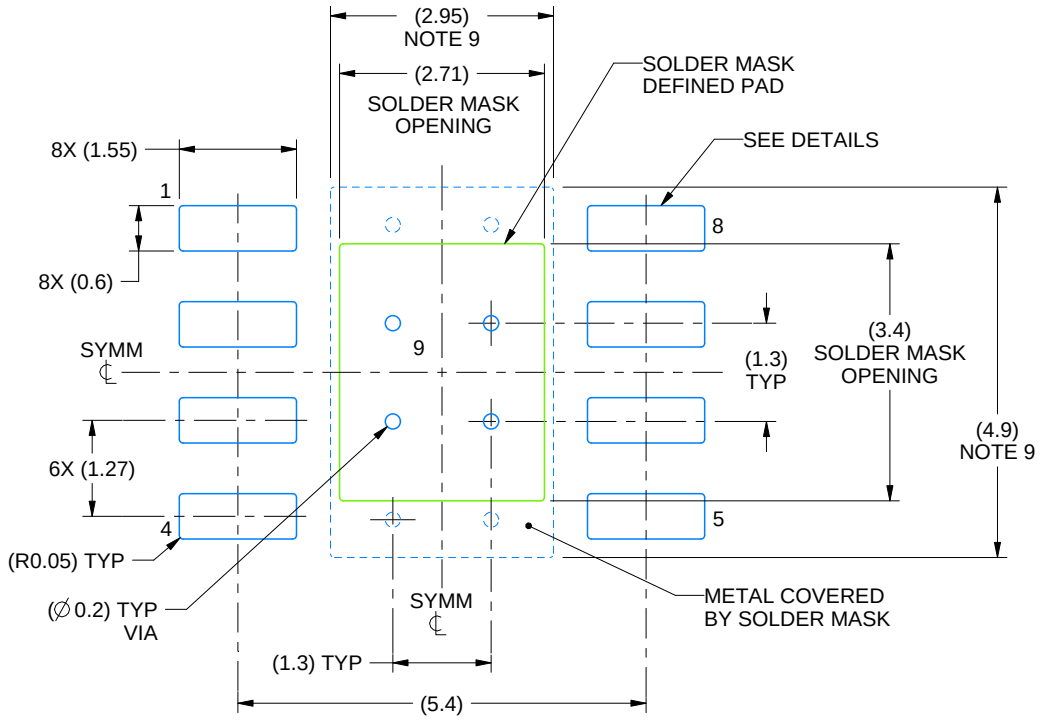
PLASTIC SMALL OUTLINE



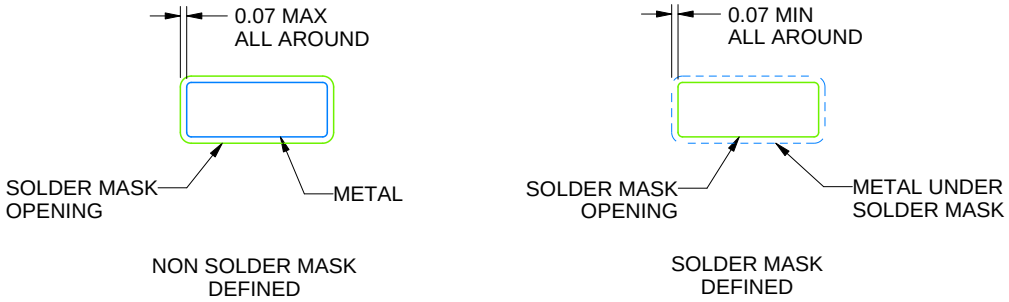
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
PADS 1-8

4214849/B 09/2025

NOTES: (continued)

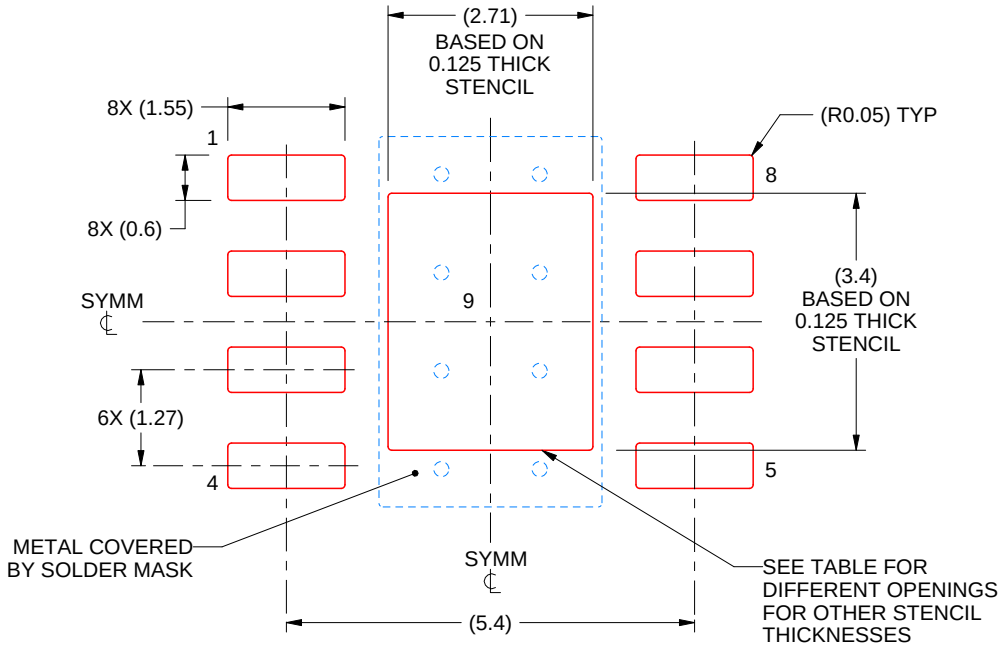
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.03 X 3.80
0.125	2.71 X 3.40 (SHOWN)
0.150	2.47 X 3.10
0.175	2.29 X 2.87

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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