UCC2732x-Q1 イネーブル付、シングル 9A、高速ローサイド MOSFET ドライバ

1 特長

- 車載アプリケーション用に認定済み
- 下記内容で AEC-Q100 認定済み:
  - デバイス温度グレード 1:-40°C～125°C の周囲動作温度範囲
  - デバイス HBM ESD 分類レベル 2
  - デバイス CDM ESD 分類レベル C6
- イネーブル機能を追加した業界標準のピン配置
- TrueDrive™ テクノロジを使用したミラー プラトー領域で ±9A の大電流駆動能力
- 独自のバイポーラおよび CMOS 出力段を使用した効率的な定電流ソース
- 電源電圧から独立した TTL/CMOS 互換入力
- 標準立ち上がり時間 20ns、標準立ち下がり時間 15ns (10nF 負荷時)
- 標準伝播遅延時間:25ns(入力立ち下がり時)、35ns(入力立ち上がり時)
- 電源電圧:4V～15V
- 熱特性が強化された MSOP PowerPAD™ パッケージで供給
- TrueDrive 出力アーキテクチャ、バイポーラおよび CMOS トランジスタを並列に使用

2 アプリケーション

- スイッチ・モード電源
- DC/DC コンバータ
- モーター・コントローラ
- ライン・ドライバ
- Class-D スイッチング アンプ
- パルス トランス ドライバ

3 概要

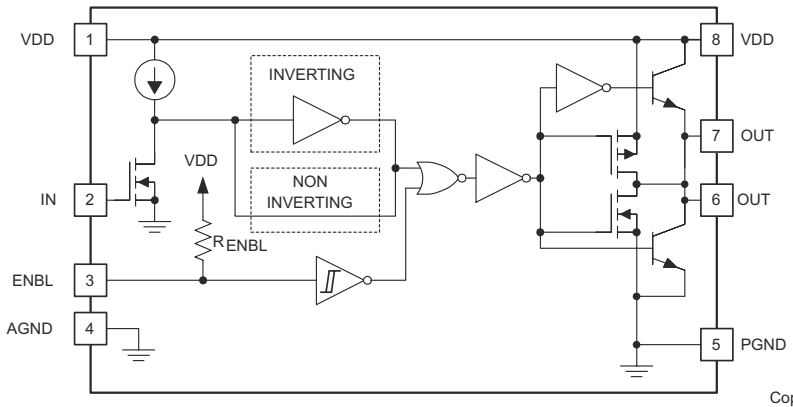
UCC2732x-Q1 ファミリの高速ドライバは、業界標準のピン配置で 9A のピーク駆動電流を供給します。これらのドライバは、高い dV/dt 遷移のために極端なミラー電流を必要とするシステム用に、大きな MOSFET を駆動できます。この結果、外部回路の追加が不要になり、複数の部品を置き換えて、スペースの節減、設計の複雑さの緩和、組み立てコストの削減が可能になります。反転 (UCC27321-Q1) と非反転 (UCC27322-Q1) の 2 つの標準ロジック オプションが用意されています。

貫通電流を最小化する設計により、これらのデバイスの出力は、MOSFET のスイッチング遷移中のミラー プラトー領域で最も必要とされる、高いゲート駆動電流を供給できます。バイポーラと MOSFET トランジスタを並列接続した独自のハイブリッド出力段 (TrueDrive) により、低い電源電圧で効率的な電流供給が可能になります。この駆動アーキテクチャにより、UCC2732x -Q1 は業界標準の 6A、9A、および多くの 12A ドライバ アプリケーションで使用できます。ラッチアップおよび ESD 保護回路も搭載されています。最後に、UCC2732x -Q1 にはイネーブル (ENBL) 機能があり、ドライバ アプリケーションの動作をより的確に制御できます。ENBL は、業界標準のピン配置では未使用のままにしてあったピン 3 に実装されています。このピンは、アクティブ ハイ ロジックでは内部で VDD にプルアップされ、標準動作時にはオープンのままにできます。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
UCC27321-Q1、UCC27322-Q1	SOIC (8)	6.00mm×4.90mm
UCC27322-Q1	MSOP-PowerPAD (8)	4.90mm×3.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



INPUT/OUTPUT TABLE

	ENBL	IN	OUT
INVERTING UCC27321-Q1	0	0	0
	0	1	0
	1	0	1
	1	1	0
NON INVERTING UCC27322-Q1	0	0	0
	0	1	0
	1	0	0
	1	1	1

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機能ブロック図

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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4 概要 (続き)

8 ピン SOIC (D) パッケージ製品に加えて、UCC2732x-Q1 は熱的に強化された小型の 8 ピン MSOP-PowerPAD (DGN) パッケージでも供給されます。PowerPAD パッケージは熱抵抗を大幅に低減するため、温度動作範囲が拡張され、長期的な信頼性が向上します。

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5 Related Products

PRODUCT	DESCRIPTION	PACKAGE
UCC2742x-Q1	Dual 4-A low-side drivers with enable	MSOP-8 PowerPAD, SOIC-8, PDIP-8
TPS2811-Q1	Dual 2-A low-side drivers with internal regulator	TSSOP-8, SOIC-8, PDIP-8
TPS2819-Q1	Single 2-A low-side driver with internal regulator	5-pin SOT-23
TPS2829-Q1	Single 2-A low-side driver	5-pin SOT-23

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6 Pin Configuration and Functions

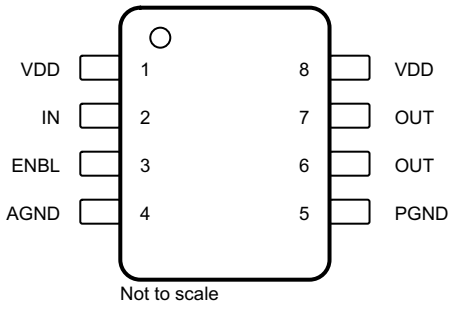


図 6-1. D Package 8-Pin SOIC Top View

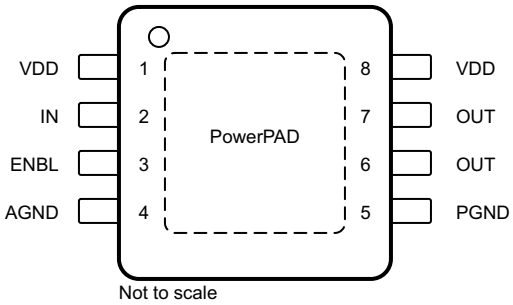


図 6-2. DGN Package 8-Pin MSOP with PowerPAD Top View

表 6-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
AGND	4	GND	The AGND and the PGND must be connected by a single thick trace directly under the device. There must be a low ESR, low ESL capacitor of 0.1 µF between VDD (pin 1) and AGND. The power MOSFETs must be placed on the PGND side of the device while the control circuit must be on the AGND side of the device. The control circuit ground must be common with the AGND while the PGND must be common with the source of the power FETs.
ENBL	3	I	Enable input for the driver with logic-compatible threshold and hysteresis. The driver output can be enabled and disabled with this pin. It is internally pulled up to VDD with a pullup resistor for active-high operation. The output state when the device is disabled is low, regardless of the input state.
IN	2	I	Input signal of the driver, which has logic-compatible threshold and hysteresis. For UCC27321-Q1, IN is inverting, and for UCC37322-Q1, IN is noninverting.
OUT	6, 7	O	Driver outputs that must be connected together externally. The output stage is capable of providing 9-A peak drive current to the gate of a power MOSFET.
PGND	5	GND	Common ground for output stage. This ground must be connected very close to the source of the power MOSFET which the driver is driving. Grounds are separated to minimize ringing effects due to output switching di/dt, which can affect the input threshold. There must be a low ESR, low ESL capacitor of 0.1 µF between VDD (pin 8) and PGND.
VDD	1, 8	PWR	Supply voltage and the power input connections for this device. These pins must be connected together externally.
PowerPAD	Pad	GND	PowerPAD on DGN package only. The PowerPAD thermal pad is not directly connected to any leads of the package. However, it is electrically and thermally connected to the substrate, which is the ground of the device.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
Supply voltage		–0.3	16	V
Output current	OUT		0.6	A
Input voltage	IN, ENBL	–5	6 or V_{DD} + 0.3	V
Power dissipation at T_A = 25°C	D package		650	mW
	DGN package		3	W
Operating junction temperature, T_J		–55	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *セクション 7.3*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND. Currents are positive into and negative out of the specified terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	2000	V
		Charged-device model (CDM), per AEC Q100-011	1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{DD}	Supply voltage	VDD	4.5	15	V

7.4 Thermal Information

THERMAL METRIC(1) (2) (3)		UCC2732x-Q1	UCC27322-Q1	UNIT
		D (SOIC)	DGN (MSOP-PowerPAD)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	113	58.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	61.7	45.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	53.2	34.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	16	1.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	52.7	34	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	11.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) In general, the system designer must attempt to use larger traces on the PCB where possible to spread the heat away from the device more effectively. For information on the PowerPAD package, see *PowerPad™ Thermally Enhanced Package* and *PowerPad™ Made Easy*.
(3) The PowerPAD thermal pad is not directly connected to any leads of the package. However, it is electrically and thermally connected to the substrate, which is the ground of the device.

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7.5 Electrical Characteristics

V_{DD} = 4.5 V to 15 V, T_J = T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{DD}	Static operating current	UCC27321-Q1	IN = Low, ENBL = Low, V_{DD} = 15 V		150	225	µA
					440	650	
			IN = High, ENBL = Low, V_{DD} = 15 V		370	550	
					370	550	
		UCC27322-Q1	IN = Low, ENBL = High, V_{DD} = 15 V		150	225	
					450	650	
			IN = High, ENBL = High, V_{DD} = 15 V		75	125	
					675	1000	
INPUT (IN)							
V_{IH}	Logic 1 input threshold			1.6	2.2	2.5	V
V_{IL}	Logic 0 input threshold			1.1	1.8	2.0	V
	Input current	0 V ≤ V_{IN} ≤ V_{DD}		–10	0	10	µA
OUTPUT (OUT)							
	Peak output current(1)	V_{DD} = 14 V			9		A
R_{OH}	Output resistance high(2)	I_{OUT} = –10 mA			0.6	1.5	Ω
R_{OL}	Output resistance low(2)	I_{OUT} = 10 mA			0.4	1	Ω
ENABLE (ENBL)							
V_{EN_H}	Enable rising threshold voltage	Low-to-high transitions		1.5	2.2	2.7	V
V_{EN_L}	Enable falling threshold voltage	High-to-low transition		1.1	1.65	2	V
	Hysteresis			0.18	0.55	0.9	V
$R_{(ENBL)}$	Enable impedance	V_{DD} = 14 V, ENBL = Low		75	100	145	kΩ
t_{D3}	Propagation delay time	C_{LOAD} = 10 nF (see 図 7-2)			60	95	ns
t_{D4}	Propagation delay time	C_{LOAD} = 10 nF (see 図 7-2)			60	95	ns

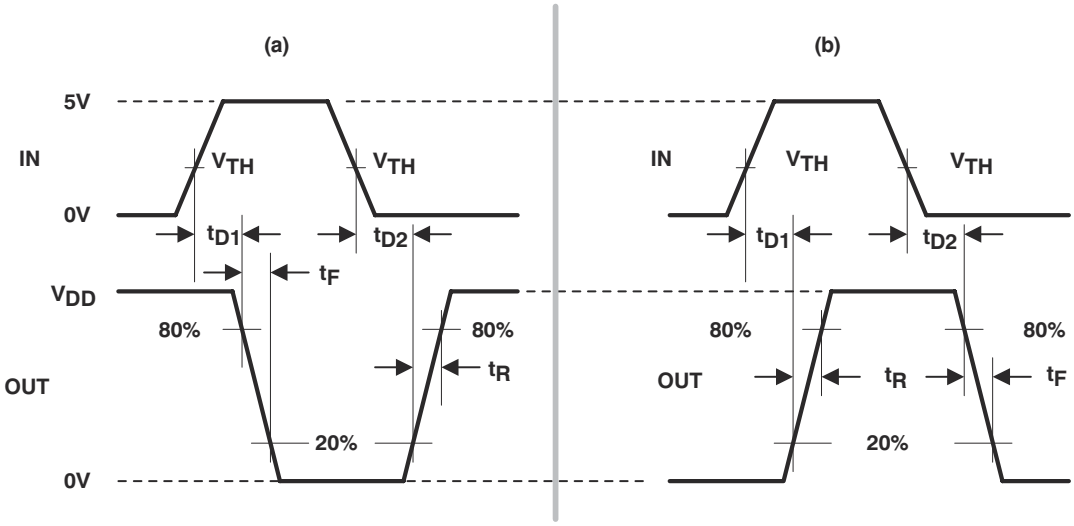
(1) Parameter not tested in production
(2) Output pullup resistance here is a DC measurement that measures resistance of PMOS structure only, not N-channel structure.

7.6 Switching Characteristics

V_{DD} = 4.5 V to 15 V, T_J = T_A = –40°C to 125°C (unless otherwise noted) (see 図 7-1)

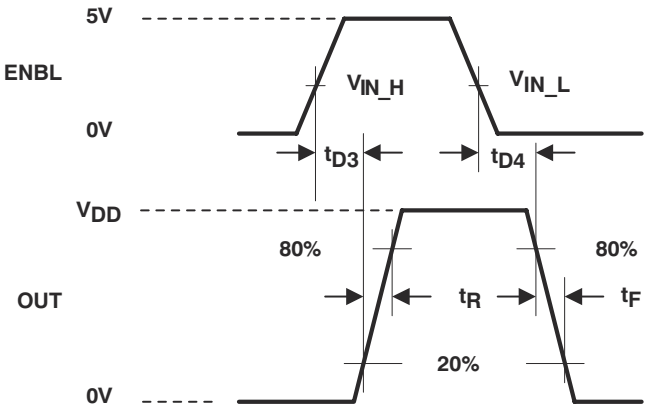
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_R	Rise time (OUT)	C_{LOAD} = 10 nF		20	75	ns
t_F	Fall time (OUT)	C_{LOAD} = 10 nF		20	35	ns
t_{D1}	Delay time, IN rising (IN to OUT)	C_{LOAD} = 10 nF		25	75	ns
t_{D2}	Delay time, IN falling (IN to OUT)	C_{LOAD} = 10 nF		35	75	ns

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The 20% and 80% thresholds depict the dynamics of the bipolar output devices that dominate the power MOSFET transition through the Miller regions of operation.

図 7-1. Switching Waveforms for Inverting Driver (a) and Noninverting Driver (b)



The 20% and 80% thresholds depict the dynamics of the bipolar output devices that dominate the power MOSFET transition through the Miller regions of operation.

図 7-2. Switching Waveforms for Enable to Output

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7.7 Typical Characteristics

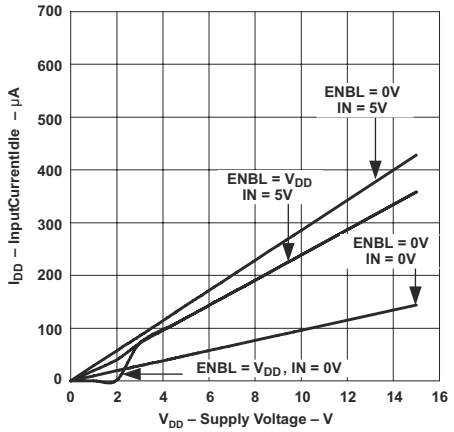


図 7-3. Input Current Idle vs Supply Voltage (UCC27321-Q1)

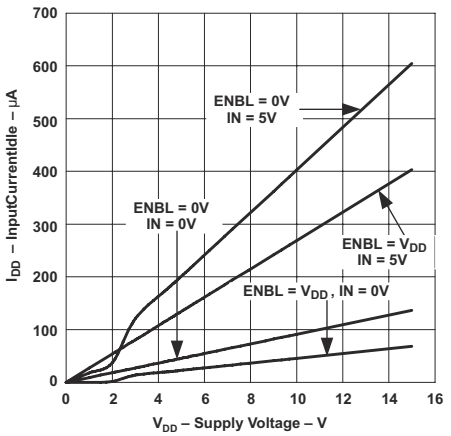


図 7-4. Input Current Idle vs Supply Voltage (UCC27322-Q1)

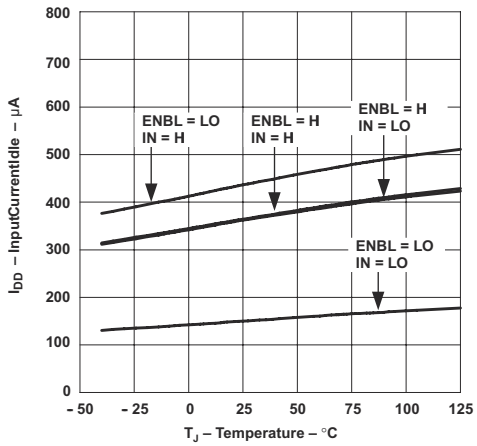


図 7-5. Input Current Idle vs Temperature (UCC27321-Q1)

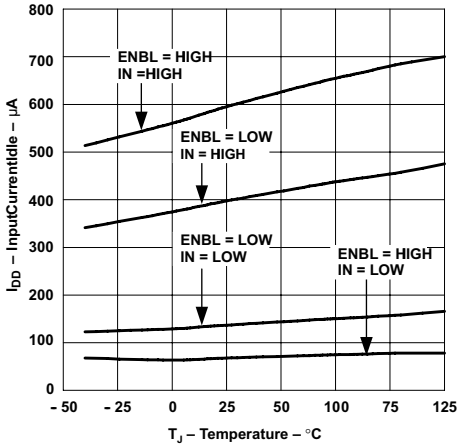


図 7-6. Input Current Idle vs Temperature (UCC27322-Q1)

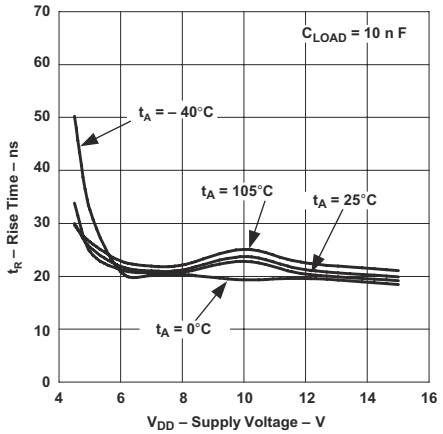


図 7-7. Rise Time vs Supply Voltage

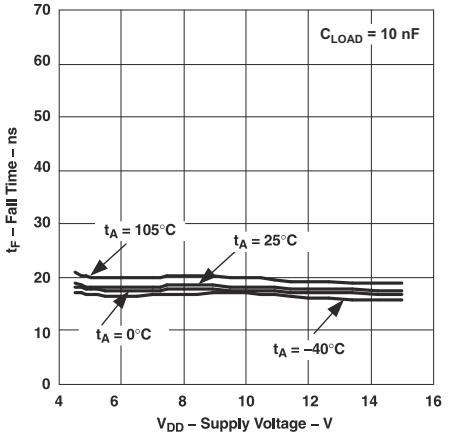


図 7-8. Fall Time vs Supply Voltage

7.7 Typical Characteristics (continued)

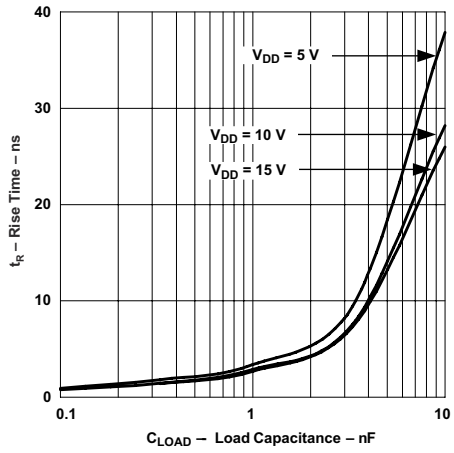


図 7-9. Rise Time vs Load Capacitance

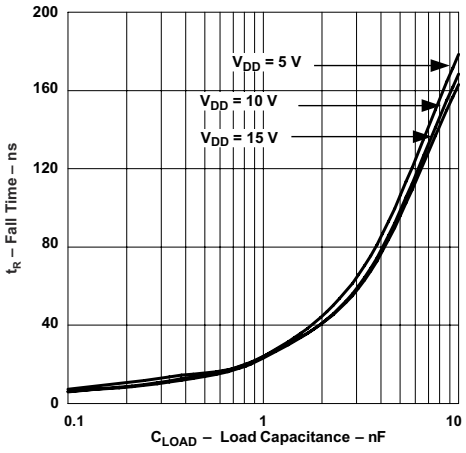


図 7-10. Fall Time vs Output Capacitance

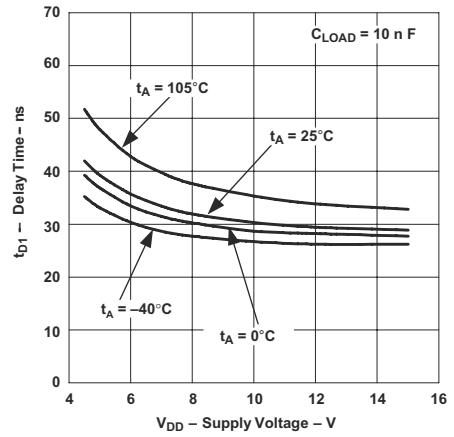


図 7-11. t_{D1} Delay Time vs Supply Voltage

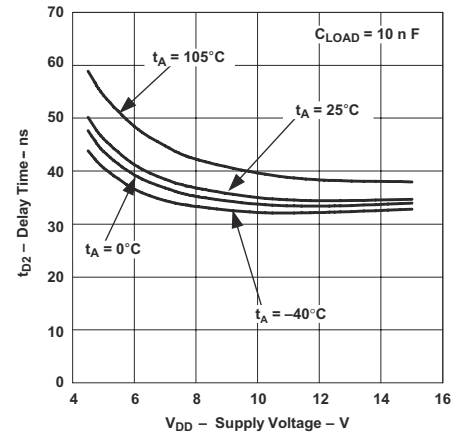


図 7-12. t_{D2} Delay Time vs Supply Voltage

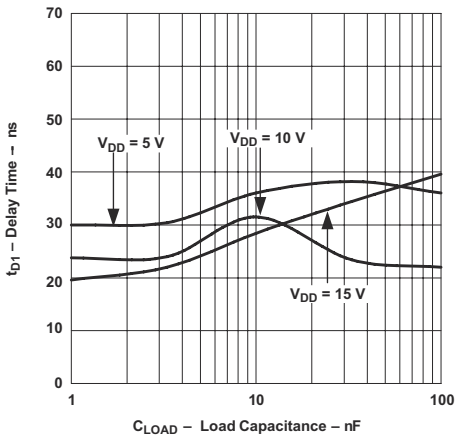


図 7-13. t_{D1} Delay Time vs Load Capacitance

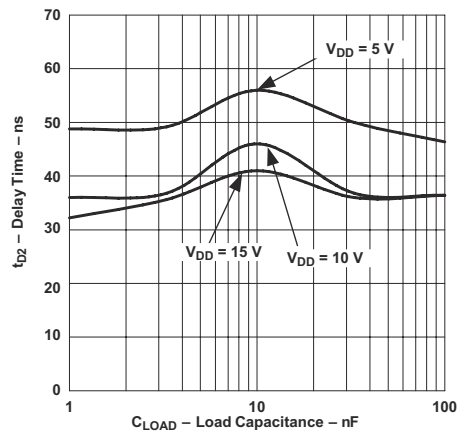


図 7-14. t_{D2} Delay Time vs Load Capacitance

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7.7 Typical Characteristics (continued)

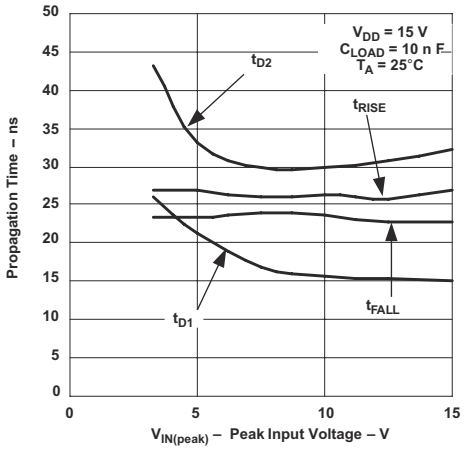


図 7-15. Propagation Times vs Peak Input Voltage

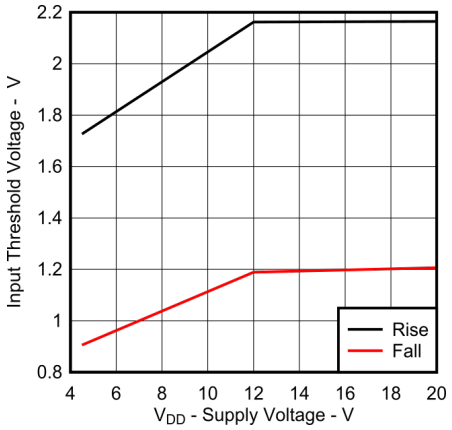


図 7-16. Input Threshold vs Supply Voltage

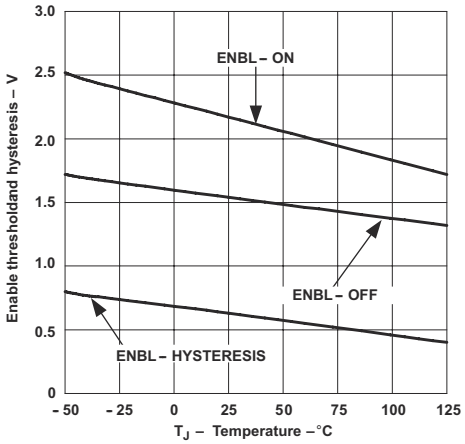


図 7-17. Enable Threshold and Hysteresis vs Temperature

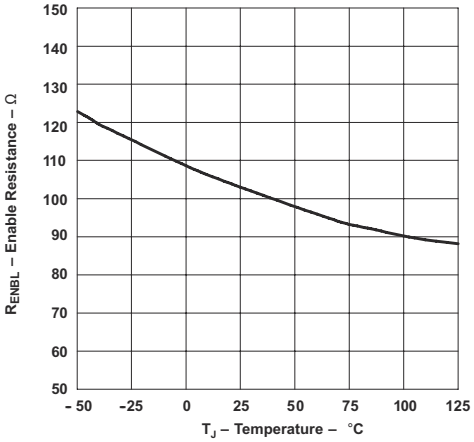


図 7-18. Enable Resistance vs Temperature

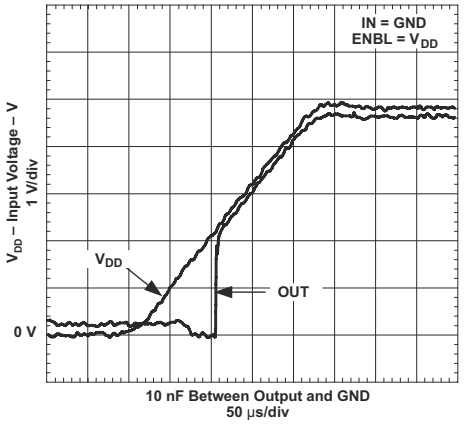


図 7-19. Output Behavior vs V_{DD} (UCC27321-Q1)

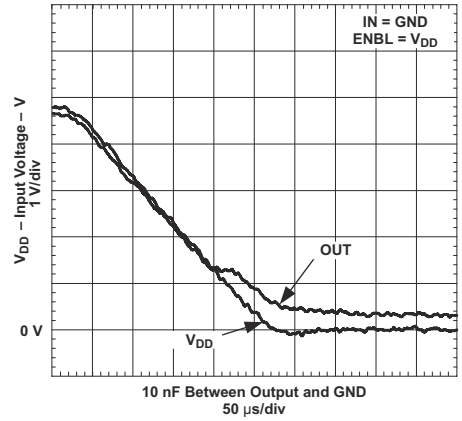


図 7-20. Output Behavior vs V_{DD} (UCC27321-Q1)

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7.7 Typical Characteristics (continued)

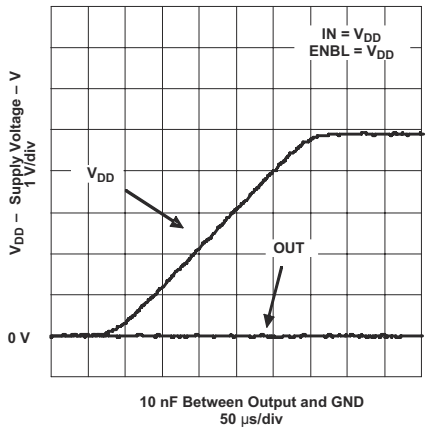


図 7-21. Output Behavior vs V_{DD} (Inverting)

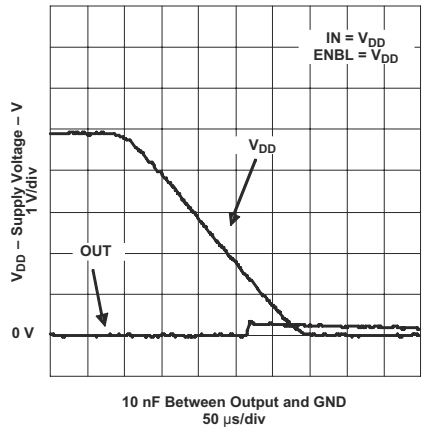


図 7-22. Output Behavior vs V_{DD} (Inverting)

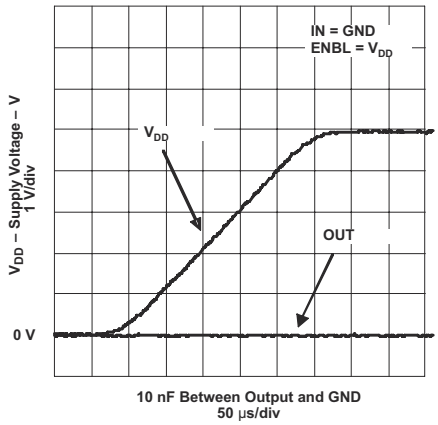


図 7-23. Output Behavior vs V_{DD} (Noninverting)

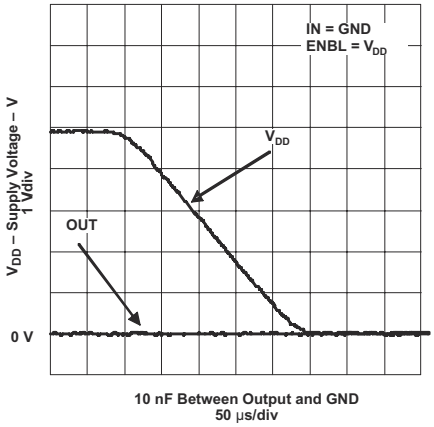


図 7-24. Output Behavior vs V_{DD} (Noninverting)

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8 Detailed Description

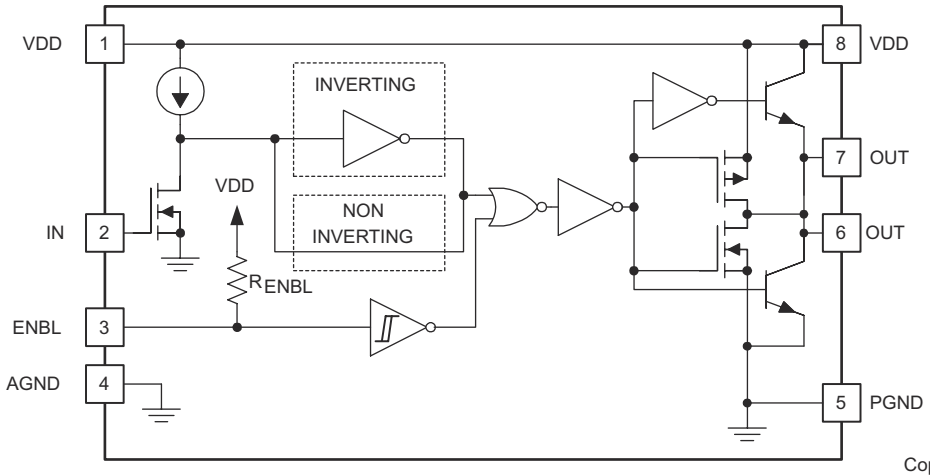
8.1 Overview

The UCC27321-Q1 and UCC27322-Q1 drivers serve as an interface between low-power controllers (discrete controllers, DSPs, MCUs, or microprocessors) and power MOSFETs. High-frequency power supplies often require high-speed, high-current drivers such as the UCC2732x-Q1 family. A leading application provides a high-power buffer stage between the PWM output of the control device and the gates of the primary power MOSFET or IGBT switching devices. In other cases, the device drives the power device gates through a drive transformer. Synchronous rectification supplies also have the need to drive multiple devices simultaneously, which can present an extremely large load to the control circuitry.

The inverting driver (UCC27321-Q1) is useful for generating inverted gate-drive signals from controllers that have outputs of the opposite polarity. For example, this driver can provide a gate signal for ground-referenced, N-channel synchronous rectifier MOSFETs in buck derived converters. This driver can also be used for generating a gate-drive signal for a P-channel MOSFET from a controller that is designed for N-channel applications.

MOSFET gate drivers are generally used when it is not feasible to have the primary PWM regulator device directly drive the switching devices for one or more reasons. The PWM device may not have the brute drive capability required for the intended switching MOSFET, limiting the switching performance in the application. In other cases, there may be a desire to minimize the effect of high-frequency switching noise by placing the high-current driver physically close to the load. Also, newer devices that target the highest operating frequencies may not incorporate onboard gate drivers at all. Their PWM outputs are only intended to drive the high-impedance input to a driver such as the UCC2732x-Q1. Finally, the control device may be under thermal stress due to power dissipation and an external driver can help by moving the heat from the controller to an external package.

8.2 Functional Block Diagram



INPUT/OUTPUT TABLE

	ENBL	IN	OUT
INVERTING UCC27321-Q1	0	0	0
	0	1	0
	1	0	1
	1	1	0
NON INVERTING UCC27322-Q1	0	0	0
	0	1	0
	1	0	0
	1	1	1

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8.3 Feature Description

8.3.1 Input Stage

The IN threshold has a 3.3-V logic sensitivity over the full range of VDD voltage; yet, it is equally compatible with 0-V to V_{DD} signals. The inputs of UCC2732x-Q1 family of drivers are designed to withstand 500-mA reverse current without either damage to the device or logic upset. In addition, the input threshold turnoff of the UCC2732x-Q1 is slightly raised for improved noise immunity. The input stage of each driver must be driven by a signal with a short rise or fall time. This condition is satisfied in typical power-supply applications, where the input signals are provided by a PWM controller or logic gates with fast transition times (<200 ns). The IN input of the driver functions as a digital gate, and is not intended for applications where a slow-changing input voltage is used to generate a switching output when the logic threshold of the input section is reached. While this may not be harmful to the driver, the output of the driver may switch repeatedly at a high frequency.

Users must not attempt to shape the input signals to the driver in an attempt to slow down (or delay) the signal at the output. If limiting the rise or fall times to the power device is desired, then an external resistance can be added between the output of the driver and the load device, which is generally a power MOSFET gate. The external resistor may also help dissipate power from the device package, as discussed in セクション 11.3.

8.3.2 Output Stage

The TrueDrive output stage is capable of supplying ±9-A peak current pulses and swings to both VDD and GND and can encourage even the most stubborn MOSFETs to switch. The pullup and pulldown circuits of the driver are constructed of bipolar and MOSFET transistors in parallel. The peak output current rating is the combined current from the bipolar and MOSFET transistors. The output resistance is the $R_{DS(ON)}$ of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor. Each output stage also provides a very low impedance to overshoot and undershoot due to the body diode of the internal MOSFET. This means that in many cases, external Schottky clamping diodes are not required.

This unique bipolar and MOSFET hybrid output architecture (TrueDrive) allows efficient current sourcing at low supply voltages. The UCC2732x-Q1 family delivers 9 A of gate drive where it is most needed during the MOSFET switching transition—at the Miller plateau region—providing improved efficiency gains.

8.3.3 Source and Sink Capabilities During Miller Plateau

Large power MOSFETs present a large load to the control circuitry. Proper drive is required for efficient, reliable operation. The UCC2732x-Q1 drivers have been optimized to provide maximum drive to a power MOSFET during the Miller plateau region of the switching transition. This interval occurs while the drain voltage is swinging between the voltage levels dictated by the power topology, requiring the charging or discharging of the drain-gate capacitance with current supplied or removed by the driver.

Two circuits are used to test the current capabilities of the UCC2732x-Q1 driver. In each case, external circuitry is added to clamp the output near 5 V while the device is sinking or sourcing current. An input pulse of 250 ns is applied at a frequency of 1 kHz in the proper polarity for the respective test. In each test, there is a transient period when the current peaked up and then settled down to a steady-state value. The noted current measurements are made at a time of 200 ns after the input pulse is applied, after the initial transient.

The circuit in 図 8-1 is used to verify the current-sink capability when the output of the driver is clamped at approximately 5 V, a typical value of gate-source voltage during the Miller plateau region. The UCC2732x-Q1 is found to sink 9 A at V_{DD} = 15 V.

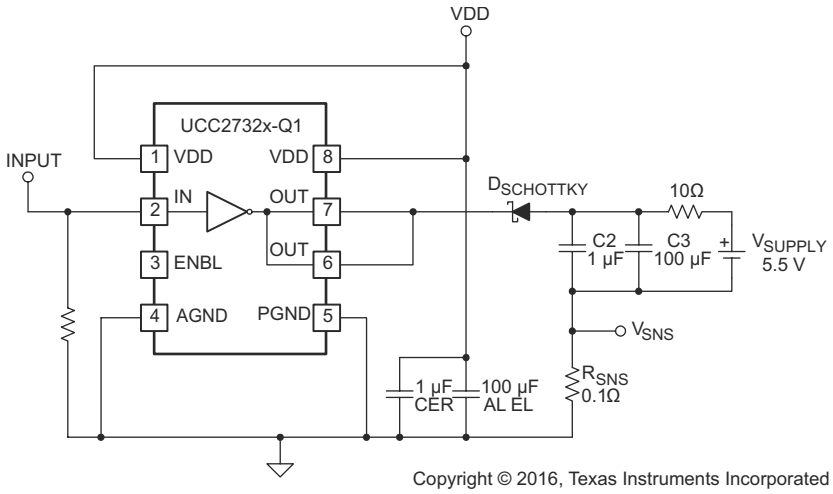


図 8-1. Sink Current Test Circuit

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The circuit in 図 8-2 is used to test the current-source capability with the output clamped to approximately 5 V with a string of Zener diodes. The UCC2732x-Q1 is found to source 9 A at V_{DD} = 15 V.

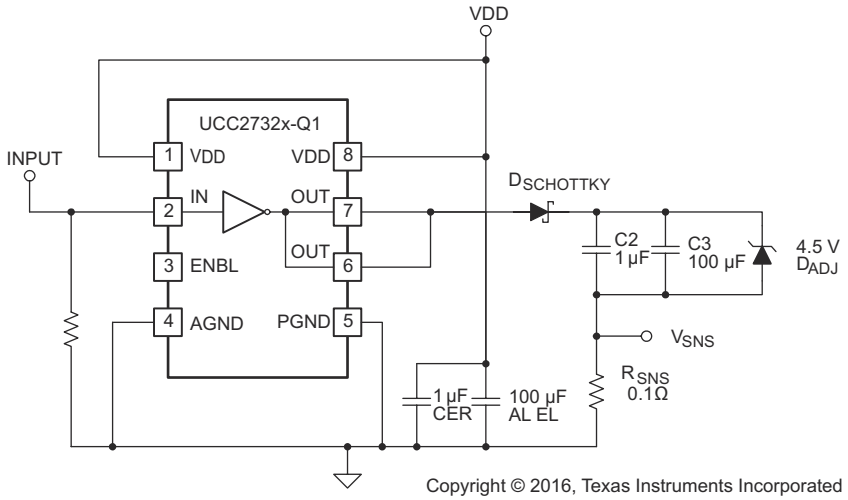


図 8-2. Source Current Test Circuit

The current-sink capability is slightly stronger than the current source capability at lower V_{DD}. This is due to the differences in the structure of the bipolar-MOSFET power output section, where the current source is a P-channel MOSFET and the current sink has an N-channel MOSFET.

In a large majority of applications, it is advantageous that the turnoff capability of a driver is stronger than the turnon capability. This helps to ensure that the MOSFET is held off during common power-supply transients that may turn the device back on.

8.3.4 VDD

Although quiescent VDD current is very low, total supply current is higher, depending on the OUT current and the programmed oscillator frequency. Total VDD current is the sum of quiescent VDD current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Q_g), average OUT current can be calculated from 式 1:

$$I_{OUT} = Q_g \times f \quad (1)$$

where

- f = frequency

For the best high-speed circuit performance, TI recommends two VDD bypass capacitors to prevent noise problems. TI highly recommends the use of surface-mount components. A 0.1-µF ceramic capacitor must be placed closest to the VDD-to-ground connection. In addition, a larger capacitor (such as 1-µF) with relatively low ESR must be connected in parallel, to help deliver the high-current peaks to the load. The parallel combination of capacitors must present a low-impedance characteristic for the expected current levels in the driver application.

8.3.5 Drive Current and Power Requirements

The UCC2732x-Q1 family of drivers is capable of delivering 9 A of current to a MOSFET gate for a period of several hundred nanoseconds. High peak current is required to turn an N-channel device ON quickly. Then, to turn the device OFF, the driver is required to sink a similar amount of current to ground. This repeats at the operating frequency of the power device. An N-channel MOSFET is used in this discussion because it is the most common type of switching device used in high-frequency power-conversion equipment.

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Design And Application Guide For High Speed MOSFET Gate Drive Circuits and *Practical Considerations in High Performance MOSFET, IGBT and MCT Gate Drive Circuits* contain detailed discussions of the drive current required to drive a power MOSFET and other capacitive-input switching devices. Much information is provided in tabular form to give a range of the current required for various devices at various frequencies. The information pertinent to calculating gate-drive current requirements is summarized here. See MOSFET and IGBT drivers for additional documentation.

When a driver is tested with a discrete capacitive load, it is a fairly simple matter to calculate the power that is required from the bias supply. The energy that must be transferred from the bias supply to charge the capacitor is given by 式 2:

$$E = ½CV^2 \quad (2)$$

where

- C = load capacitor
- V = bias voltage feeding the driver

There is an equal amount of energy transferred to ground when the capacitor is discharged. This leads to a power loss given by 式 3:

$$P = 2 \times ½CV^2f \quad (3)$$

where

- f = switching frequency

This power is dissipated in the resistive elements of the circuit. Thus, with no external resistor between the driver and gate, this power is dissipated inside the driver. Half of the total power is dissipated when the capacitor is charged, and the other half is dissipated when the capacitor is discharged. An actual example using the conditions of the previous gate-drive waveform must help clarify this.

With V_{DD} = 12 V, C_{LOAD} = 10 nF, and f = 300 kHz, the power loss can be calculated as in 式 4:

$$P = 10\ nF \times (12\ V)^2 \times (300\ kHz) = 0.432\ W \quad (4)$$

With a 12-V supply, in 式 5 this equates to a current of:

$$I = P / V = 0.432\ W / 12\ V = 0.036\ A \quad (5)$$

The switching load presented by a power MOSFET can be converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge required to swing the drain of the device between the on and off states. Most manufacturers provide specifications that provide the typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Q_g, the power that must be dissipated when charging a capacitor can be determined. This is done by using the equivalence Q_g = CeffV to provide the 式 6 for power:

$$P = C \times V^2 \times f = Q_g \times V \times f \quad (6)$$

式 6 allows a power designer to calculate the bias power required to drive a specific MOSFET gate at a specific bias voltage.

8.3.6 Enable

UCC2732x-Q1 provides an enable input for improved control of the driver operation. This input also incorporates logic-compatible thresholds with hysteresis. The input is internally pulled up to V_{DD} with a 100-kΩ (typical) resistor for active-high operation. When ENBL is high, the device is enabled, and when ENBL is low, the device is disabled. The default state of the ENBL pin is to enable the device, and therefore can be left open for standard

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operation. The output state when the device is disabled is low, regardless of the input state. See the truth table (表 8-1) for operation using enable logic.

The ENBL input is compatible with both logic signals and slow-changing analog signals. It can be directly driven, or a power-up delay can be programmed with a capacitor between ENBL and AGND.

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8.4 Device Functional Modes

The UCC2732x-Q1 device has two functional modes; enabled when ENBL is HIGH and disabled when ENBL is LOW. 表 8-1 lists the logic of this device.

表 8-1. Device Logic and Modes Table

	ENBL	IN	OUT
Inverting UCC27321-Q1	0	0	0
	0	1	0
	1	0	1
	1	1	0
Noninverting UCC27322-Q1	0	0	0
	0	1	0
	1	0	0
	1	1	1

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9 Application and Implementation

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9.1 Application Information

High-current gate driver devices are required in switching power applications for a variety of reasons. To enable fast switching of power devices and reduce associated power losses, a powerful gate driver can be employed between the PWM output of controllers or signal isolation devices and the gates of the power semiconductor devices. Further, gate drivers are indispensable when sometimes it is just not feasible to have the PWM controller directly drive the gates of the switching devices. The situation may be encountered because the PWM signal from a digital controller or signal isolation device is often a 3.3-V or 5-V logic signal which is not capable of effectively turning on a power switch. A level-shifting circuitry is required to boost the logic-level signal to the gate-drive voltage to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on bipolar or MOSFET transistors in totem-pole arrangement, being emitter follower configurations, prove inadequate for this because they lack level-shifting capability and low-drive voltage protection. Gate drivers effectively combine both the level-shifting and buffer drive functions. Gate drivers may also minimize the effect of switching noise by placing the high-current driver physically close to the power switch, drive gate-driver transformers and control floating power device gates, reducing power dissipation and thermal stress in controllers by absorbing gate-charge power losses.

In summary gate drivers are extremely important components in switching power combining benefits of high-performance, low-cost, low component count, board-space reduction, and simplified system design.

9.2 Typical Application

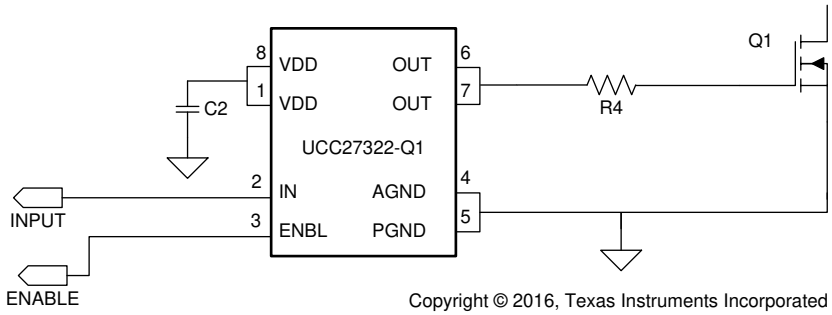


図 9-1. Typical Application Diagram of UCC27322-Q1

9.2.1 Design Requirements

When selecting the proper gate driver device for an end application, some design considerations must be evaluated first to make the most appropriate selection. The following design parameters should be used when selecting the proper gate driver device for an end application: input-to-output configuration, the input threshold type, bias supply voltage levels, peak source and sink currents, availability of independent enable and disable functions, propagation delay, power dissipation, and package type. See the example design parameters and requirements in 表 9-1.

表 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input-to-output configuration	Noninverting
Input threshold type	CMOS
Bias supply voltage levels	12 V
dVDS/dt(1)	20 V/ns
Enable function	Yes
Propagation delay	<50 ns
Power dissipation	<0.45 W
Package type	SOIC (8)

(1) dVDS/dt is a typical requirement for a given design. This value can be used to find the peak source and sink currents required as shown in セクション 9.2.2.4.

9.2.2 Detailed Design Procedure

9.2.2.1 Input-to-Output Configuration

The design must specify which type of input-to-out configuration is used. If turning on the power MOSFET or IGBT when the input signal is in high state is preferred, then a device capable of the noninverting configuration must be selected. If turning off the power MOSFET or IGBT when the input signal is in high state is preferred, then a device capable of the inverting configuration must be chosen. Based on this noninverting requirement of this application, the proper device is the UCC27322-Q1.

9.2.2.2 Input Threshold Type

The type of input voltage threshold determines the type of controller that can be used with the gate driver device. The UCC2732x-Q1 devices feature a TTL and CMOS-compatible input threshold logic, with wide hysteresis. The threshold voltage levels are low voltage and independent of the VDD supply voltage, which allows compatibility with both logic-level input signals from microcontrollers as well as higher-voltage input signals from analog controllers. See セクション 7.5 for the actual input threshold voltage levels and hysteresis specifications for the UCC2732x-Q1 devices.

9.2.2.3 VDD Bias Supply Voltage

The bias supply voltage to be applied to the VDD pins of the device must never exceed the values listed in セクション 7.3. However, different power switches require different voltage levels to be applied at the gate. With a wide operating range from 4.5 V to 15 V, the UCC2732x-Q1 device can be used to drive a variety of power switches, such as Si MOSFETs (V_{GS} = 4.5 V, 10 V, 12 V), IGBTs (V_{GE} = 15 V), and wide-bandgap power semiconductors (such as GaN, certain types of which allow no higher than 6 V to be applied to the gate terminals).

9.2.2.4 Peak Source and Sink Currents

Generally, the switching speed of the power switch during turnon and turnoff must be as fast as possible to minimize switching power losses. The gate driver device must be able to provide the required peak current for achieving the targeted switching speeds for the targeted power MOSFET.

Using the example of a power MOSFET, the system requirement for the switching speed is typically described in terms of the slew rate of the drain-to-source voltage of the power MOSFET (such as dvds/dt). For example, the

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system requirement might state that a SPP20N60C3 power MOSFET must be turned on with a dvds/dt of 20 V/ns or higher under a DC bus voltage of 400 V in a continuous-conduction-mode (CCM) boost PFC-converter application. This type of application is an inductive hard-switching application and reducing switching power loss is critical. This requirement means that the entire drain-to-source voltage swing during power MOSFET turnon event (from 400 V in the OFF state to $V_{DS(ON)}$ in ON state) must be completed in approximately 20 ns or less. When the drain-to-source voltage swing occurs, the Miller charge of the power MOSFET (Q_{gd} for SPP20N60C3 power MOSFET is 33 nC, typically) is supplied by the peak current of gate driver. According to power MOSFET inductive switching mechanism, the gate-to-source voltage of the power MOSFET at this time is the Miller plateau voltage, which is typically a few volts higher than the threshold voltage of the power MOSFET ($V_{GS(th)}$).

To achieve the targeted dvds/dt, the gate driver must be capable of providing the Q_{gd} charge in 20 ns or less. In other words, a peak current of 1.65 A = (33 nC) / (20 ns) or higher must be provided by the gate driver. The UCC2732x-Q1 devices can provide 9-A peak sourcing or sinking current which clearly exceeds the design requirement and has the capability to meet the switching speed required. This 9-A peak sourcing or sinking current provides an extra margin against part-to-part variations in the Q_{gd} parameter of the power MOSFET along with additional flexibility to insert external gate resistors and fine tune the switching speed for efficiency versus EMI optimizations.

In practical designs, the parasitic trace in the gate driver circuit of the PCB has a definitive role to play on the power MOSFET switching speed. The effort of this trace inductance is to limit the di/dt of the output current pulse of the gate driver. To illustrate this effect, consider output current pulse waveform from the gate driver to be approximated to a triangular profile, where the area under the triangle (0.5 × IPEAK × time) would equal the total gate charge of the power MOSFET (Q_g for SPP20N60C3 power MOSFET is 87 nC typically). If the parasitic trace inductance limits the di/dt then a situation may occur in which the full peak current capability of the gate driver is not fully achieved in the time required to deliver the Q_g required for the power MOSFET switching. In other words, the time parameter in the equation would dominate and the IPEAK value of the current pulse would be much less than the true peak current capability of the device, while the required Q_g is still delivered. Because of this, the desired switching speed may not be realized, even when theoretical calculations indicate the gate driver can achieve the targeted witching speed. Thus, placing the gate driver device very close to the power MOSFET and designing a tight gate drive-loop with minimal PCB trace inductance is important to realize the full peak-current capability of the gate driver.

9.2.2.5 Enable and Disable Function

Certain applications demand independent control of the output state of the driver without involving the input signal. A pin which offers enable and disable functions achieves the requirements. For these applications, the UCC2732x-Q1 devices are suitable as they feature an input pin and an Enable pin.

9.2.2.6 Propagation Delay

The acceptable propagation delay from the gate driver is dependent on the switching frequency at which it is used and the acceptable level of pulse distortion to the system. The UCC2732x-Q1 devices feature 25-ns turnon propagation delay and 35-ns turnoff propagation delay (typical), which ensure very little distortion and allow operation at higher frequencies. See セクション 7.5 for the propagation and セクション 7.6 of the UCC2732x-Q1 devices.

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9.2.3 Application Curves

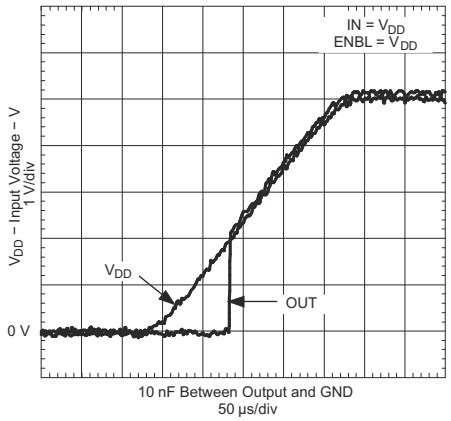


図 9-2. Output Behavior vs V_{DD} (UCC27322-Q1)

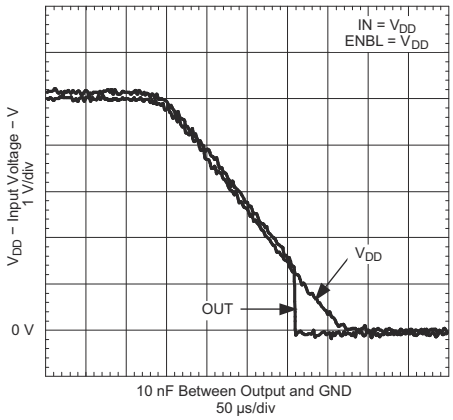


図 9-3. Output Behavior vs V_{DD} (UCC27322-Q1)

10 Power Supply Recommendations

Although quiescent VDD current is very low, total supply current is higher, depending on OUTA and OUTB current and the operating frequency. Total VDD current is the sum of quiescent VDD current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Q_g), average OUT current can be calculated using 式 7.

$$I_{OUT} = Q_g \times f \tag{7}$$

For the best high-speed circuit performance, TI recommends two VDD bypass capacitors to prevent noise problems. TI also highly recommends using surface mount components. A 0.1-µF ceramic capacitor must be placed closest to the VDD to ground connection. In addition, a larger capacitor (such as 1 µF) with relatively low ESR must be connected in parallel to help deliver the high current peaks to the load. The parallel combination of capacitors presents a low impedance characteristic for the expected current levels in the driver application.

11 Layout

11.1 Layout Guidelines

It can be a significant challenge to avoid the overshoot or undershoot and ringing issues that can arise from circuit layout. The low impedance of these drivers and their high di/dt can induce ringing between parasitic inductances and capacitances in the circuit. Take utmost care in the circuit layout.

In general, position the driver physically as close to its load as possible. Place a 1-µF bypass capacitor as close to the output side of the driver as possible, connecting it to pins 1 and 8. Connect a single trace between the two VDD pins (pin 1 and pin 8); connect a single trace between PGND and AGND (pin 5 and pin 4). If a ground plane is used, it may be connected to AGND; do not extend the plane beneath the output side of the package (pins 5 to 8). Connect the load to both OUT pins (pins 7 and 6) with a single trace on the adjacent layer to the component layer; route the return current path for the output on the component side, directly over the output path.

Extreme conditions may require decoupling the input power and ground connections from the output power and ground connections. The UCCx732[1,2] has a feature that allows the user to take these extreme measures, if necessary. There is a small amount of internal impedance of about 15 Ω between the AGND and PGND pins; there is also a small amount of impedance (approximately 30 Ω) between the two VDD pins. To take advantage of this feature, connect a 1-µF bypass capacitor between VDD and PGND (pins 5 and 8) and connect a 0.1-µF bypass capacitor between VDD and AGND (pins 1 and 4). Further decoupling can be achieved by connecting between the two VDD pins with a jumper that passes through a 40-MHz ferrite bead and connects bias power

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only to pin 8 (VDD). Even more decoupling can be achieved by connecting between AGND and PGND with a pair of anti-parallel diodes (anode connected to cathode and cathode connected to anode).

11.2 Layout Example

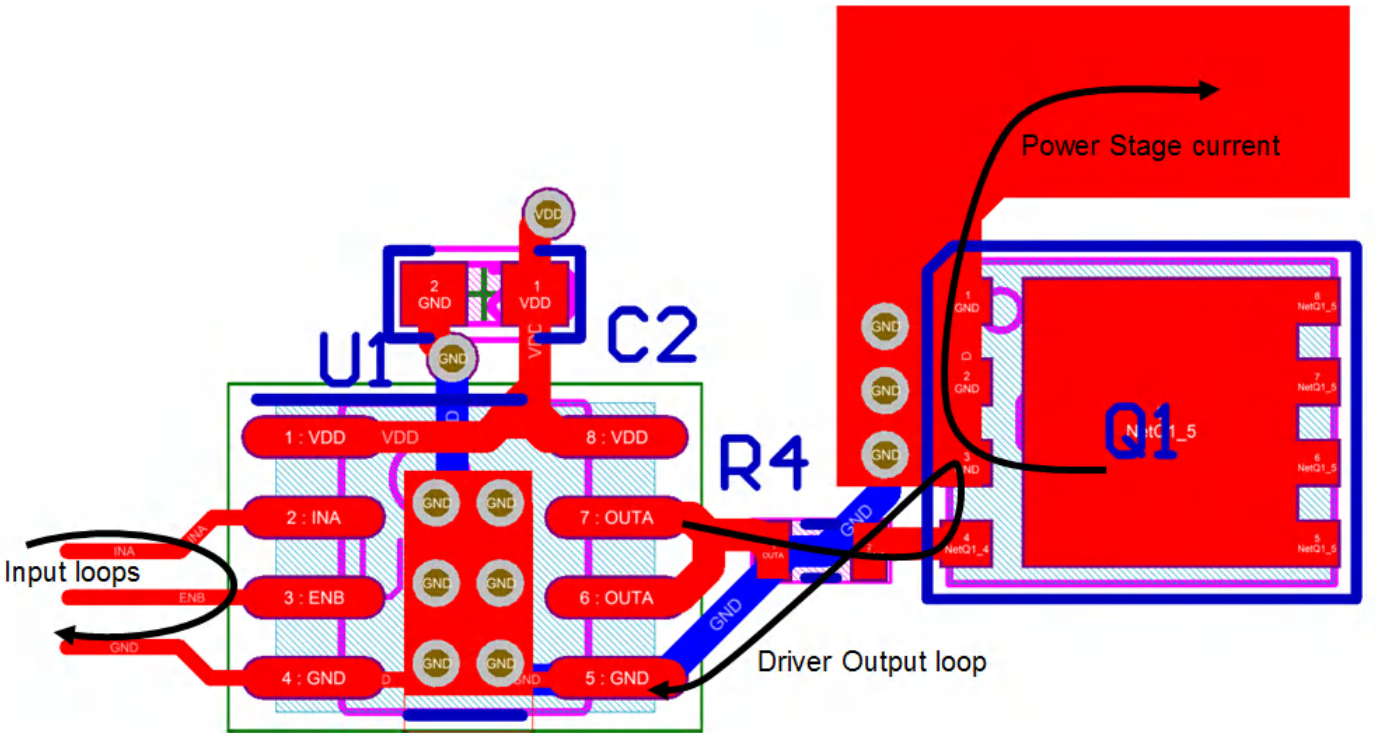


図 11-1. Layout Recommendation

11.3 Thermal Considerations

The useful range of a driver is greatly affected by the drive-power requirements of the load and the thermal characteristics of the package. For a power driver to be useful over a particular temperature range, the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The UCC2732x-Q1 family of drivers is available in two different packages to cover a range of application requirements.

The 8-pin SOIC (D) package has a power rating of approximately 0.5 W at T_A = 70°C. This limit is imposed in conjunction with the power derating factor also given in the table. The power dissipation in our earlier example is 0.432 W with a 10-nF load, 12-V V_{DD}, switched at 300 kHz. Thus, only one load of this size could be driven using the D package. The difficulties with heat removal limit the drive available in the older packages.

The 8-pin MSOP PowerPAD (DGN) significantly relieves this concern by offering an effective means of removing the heat from the semiconductor junction. As illustrated in *PowerPad Thermally Enhanced Package*, the PowerPAD packages offer a lead-frame die pad that is exposed at the base of the package. This pad is soldered to the copper on the PCB directly underneath the package, reducing the θ_{JC} to 4.7°C/W. Data is presented in *PowerPad Thermally Enhanced Package* to show that the power dissipation can be quadrupled in the PowerPAD package when compared to the standard packages. The PCB must be designed with thermal lands and thermal vias to complete the heat removal subsystem, as summarized in *PowerPAD Made Easy*. This allows a significant improvement in heatsink capability over that available in the D package and is shown to more than double the power capability of the D package.

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注

The PowerPAD thermal pad is not directly connected to any leads of the package. However, it is electrically and thermally connected to the substrate, which is the ground of the device.

11.4 Power Dissipation

The UCC2732x-Q1 family of drivers are capable of delivering 9-A of current to a MOSFET gate for a period of several hundred nanoseconds. High peak current is required to turn an N-channel device ON quickly. Then, to turn the device OFF, the driver is required to sink a similar amount of current to ground. This repeats at the operating frequency of the power device. An N-channel MOSFET is used in this discussion because it is the most common type of switching device used in high-frequency power conversion equipment.

Design And Application Guide For High Speed MOSFET Gate Drive Circuits and *Practical Considerations in High Performance MOSFET, IGBT and MCT Gate Drive Circuits* contain detailed discussions of the drive current required to drive a power MOSFET and other capacitive-input switching devices. Much information is provided in tabular form to give a range of the current required for various devices at various frequencies. The information pertinent to calculating gate drive current requirements is summarized here.

When a driver device is tested with a discrete, capacitive load it is a fairly simple matter to calculate the power that is required from the bias supply. The energy that must be transferred from the bias supply to charge the capacitor is given by 式 8.

$$E = \frac{1}{2}CV^2 \tag{8}$$

where

- C is the load capacitor
- V is the bias voltage feeding the driver

There is an equal amount of energy transferred to ground when the capacitor is discharged. This leads to a power loss given by 式 9.

$$P = 2 \times \frac{1}{2}CV^2f \tag{9}$$

where

- f is the switching frequency

This power is dissipated in the resistive elements of the circuit. Thus, with no external resistor between the driver and gate, this power is dissipated inside the driver. Half of the total power is dissipated when the capacitor is charged, and the other half is dissipated when the capacitor is discharged. An example using the conditions of the previous gate-drive waveform helps to clarify this.

With V_{DD} = 12 V, C_{LOAD} = 10 nF, and f = 300 kHz, the power loss can be calculated as shown in 式 11.

$$P = 10\,nF \times (12)^2 \times (300\,kHz) = 0.432\,W \tag{10}$$

With a 12-V supply, this would equate, as shown in 式 11, to a current of:

$$I = \frac{P}{V} = \frac{0.432\,W}{12\,V} = 0.036A \tag{11}$$

The switching load presented by a power MOSFETcan be converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus

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the added charge required to swing the drain of the device between the ON and OFF states. Most manufacturers provide specifications that provide the typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Qg, one can determine the power that must be dissipated when charging a capacitor. This is done by using the equivalence Qg = CeffV to provide 式 12 for power.

$$P = C \times V^2 \times f = Qg \times V \times f \tag{12}$$

式 12 allows a power designer to calculate the bias power required to drive a specific MOSFET gate at a specific bias voltage.

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12 Device and Documentation Support

12.1 Device Support

12.1.1 サード・パーティ製品に関する免責事項

サード・パーティ製品またはサービスに関するテキサス・インスツルメンツの出版物は、単独またはテキサス・インスツルメンツの製品、サービスと一緒に提供される場合に関係なく、サード・パーティ製品またはサービスの適合性に関する是認、サード・パーティ製品またはサービスの是認の表明を意味するものではありません。

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation, see the following:

- Power Supply Seminar SEM-1400 Topic 2: *Design And Application Guide For High Speed MOSFET Gate Drive Circuits* (SLUP133)
- *Practical Considerations in High Performance MOSFET, IGBT and MCT Gate Drive Circuits* (SLUA105)
- MOSFET and IGBT drivers
- *PowerPad Thermally Enhanced Package* (SLMA002)
- *PowerPAD Made Easy* (SLMA004)

12.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

12.4 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

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12.6 静電気放電に関する注意事項



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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

12.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

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13 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (September 2016) to Revision E (November 2023) **Page**

- Changed input threshold voltage values, deleted VOH output high level and VOL output low level, changed output resistance high and output resistance low values in Electrical Characteristics....7
- Changed 図 7-16 9

Changes from Revision C (January 2012) to Revision D (September 2016) **Page**

- 「製品情報」表、「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加。....1
- ドキュメント全体を通して UCC3732x を UCC2732x-Q1 に変更....1
- 「注文情報」表を削除 (データシートの末尾にある POA を参照)....1
- Changed table descriptions for AGND and PGND....5
- Updated values in the *Thermal Information* table to align with JEDEC standards....6
- Changed x-axis values from 1, 10, 100 to 0.1, 1, 10 in Rise Time vs Load Capacitance graph....9
- Deleted note reference [1]....14

Changes from Revision B (January 2011) to Revision C (January 2012) **Page**

- Changed enable impedance maximum from 135 kΩ to 145 kΩ....7

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC27321QDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	Call TI | Nipdau	Level-1-260C-UNLIM	-40 to 125	27321Q
UCC27321QDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27321Q
UCC27322QDGNRQ1	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	EACQ
UCC27322QDGNRQ1.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	EACQ
UCC27322QDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Level-1-260C-UNLIM	-40 to 125	27322Q
UCC27322QDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Level-1-260C-UNLIM	-40 to 125	27322Q

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF UCC27321-Q1, UCC27322-Q1 :

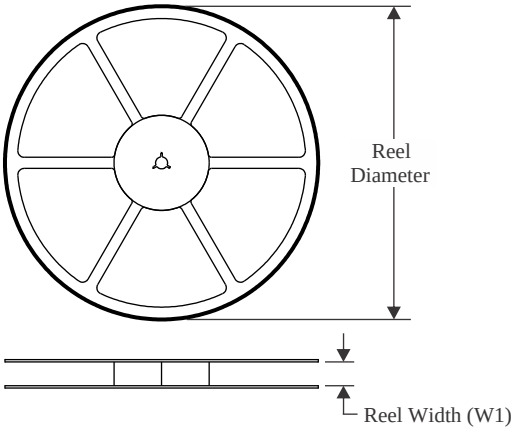
- Catalog : UCC27321, UCC27322
- Enhanced Product : UCC27322-EP

NOTE: Qualified Version Definitions:

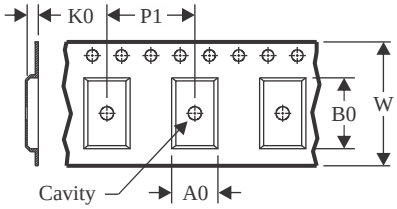
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

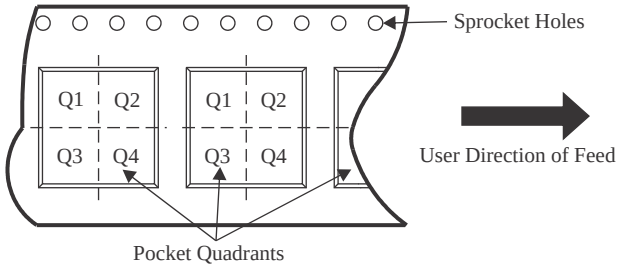


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

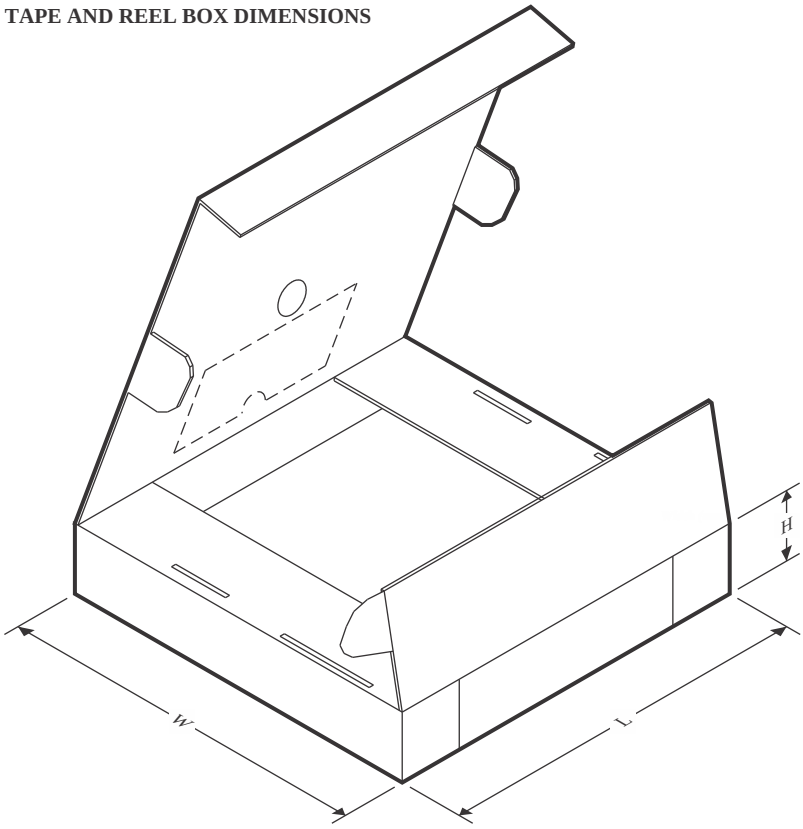
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27321QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC27322QDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC27322QDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC27322QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27321QDRQ1	SOIC	D	8	2500	353.0	353.0	32.0
UCC27322QDGNRQ1	HVSSOP	DGN	8	2500	350.0	350.0	43.0
UCC27322QDGNRQ1	HVSSOP	DGN	8	2500	353.0	353.0	32.0
UCC27322QDRQ1	SOIC	D	8	2500	353.0	353.0	32.0

GENERIC PACKAGE VIEW

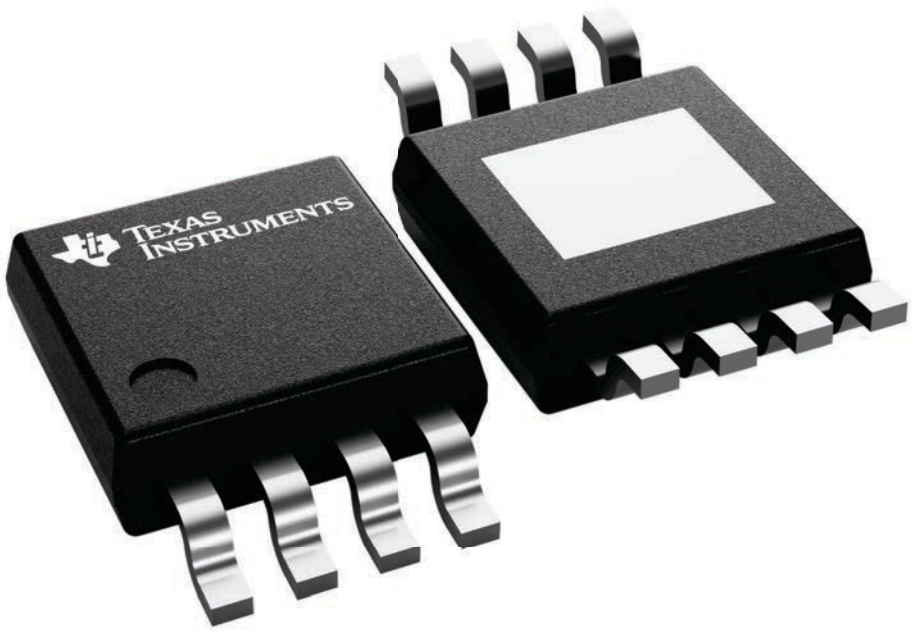
DGN 8

PowerPAD™ HVSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



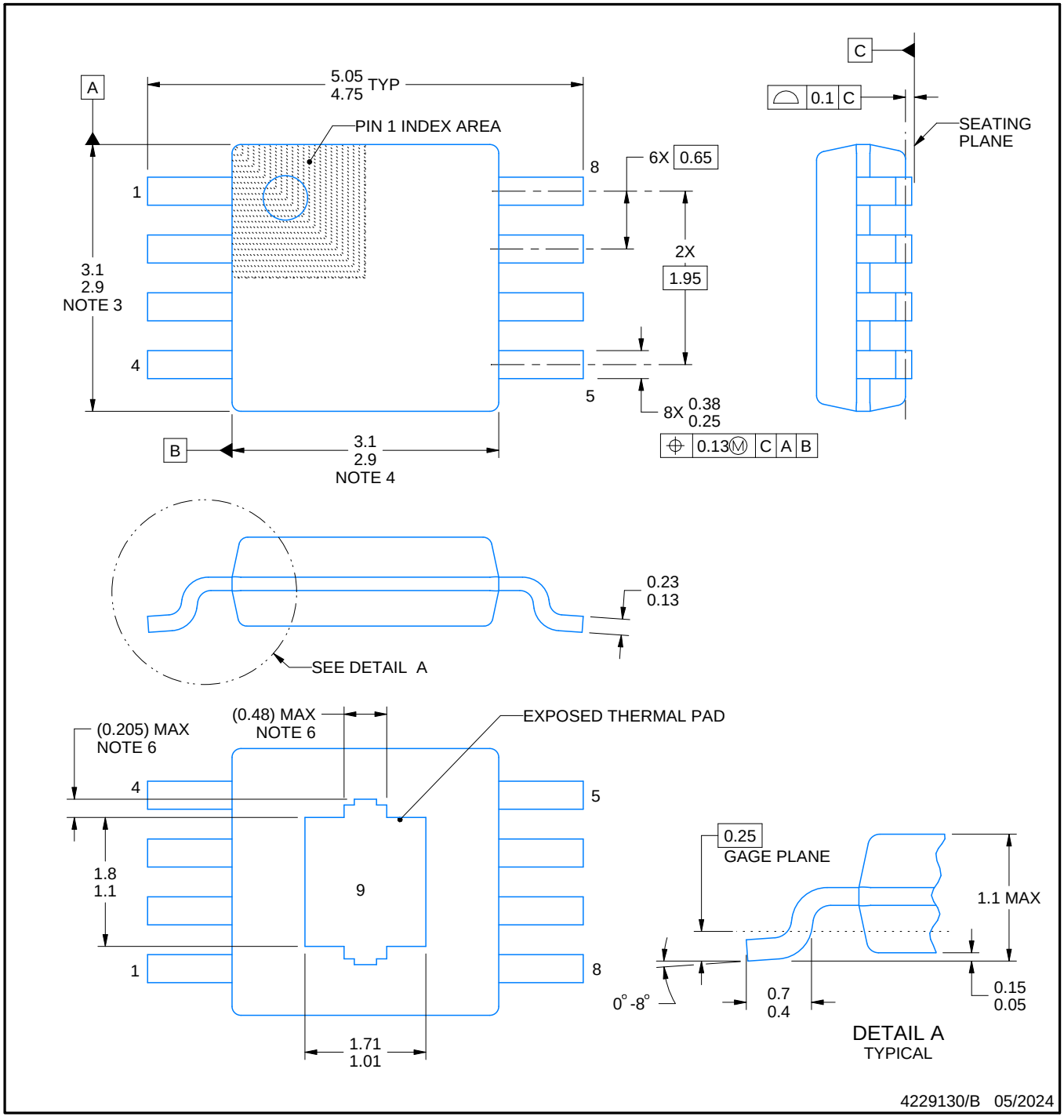
4225482/B

PACKAGE OUTLINE

DGN0008H

PowerPAD™ VSSOP - 1.1 mm max height

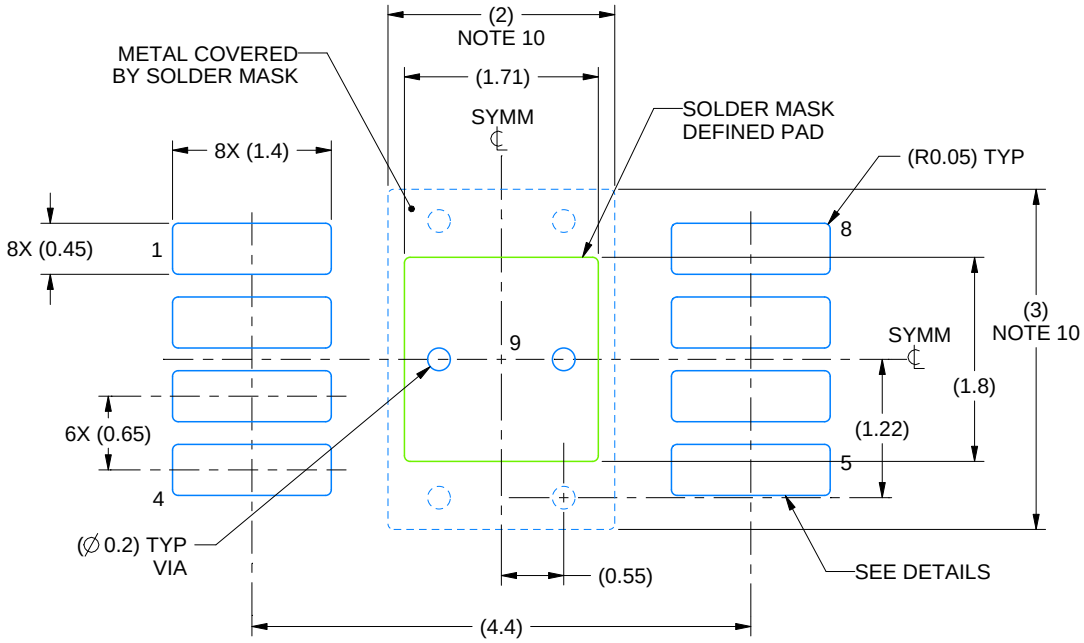
SMALL OUTLINE PACKAGE



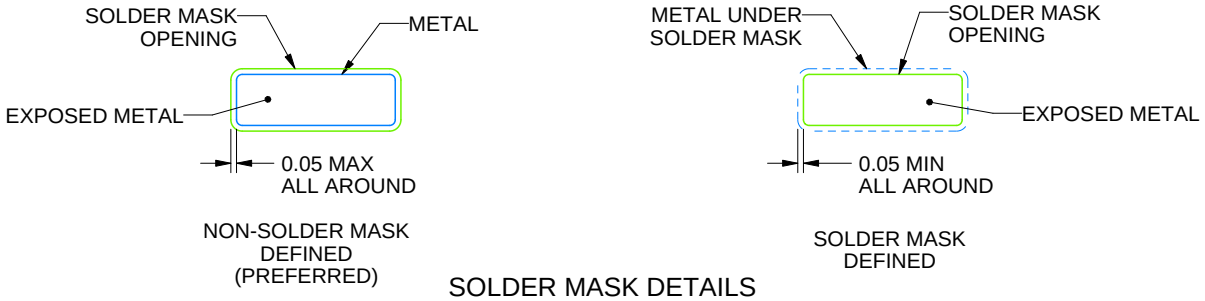
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.
6. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

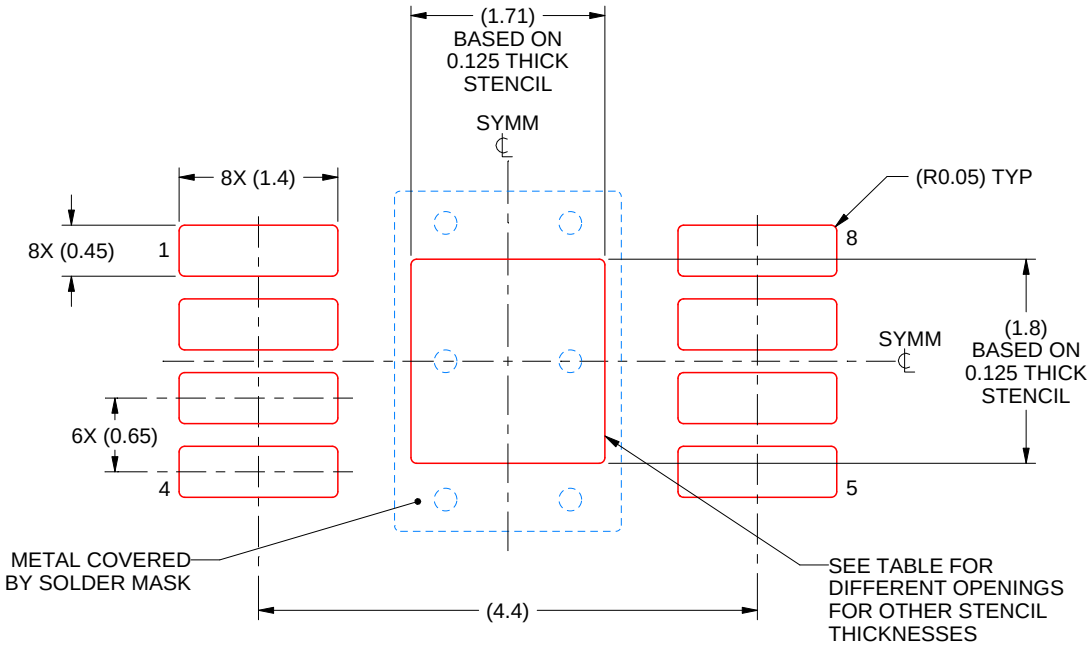


SOLDER MASK DETAILS

4229130/B 05/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
9. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.91 X 2.01
0.125	1.71 X 1.80 (SHOWN)
0.15	1.56 X 1.64
0.175	1.45 X 1.52

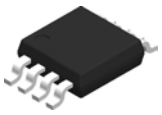
4229130/B 05/2024

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

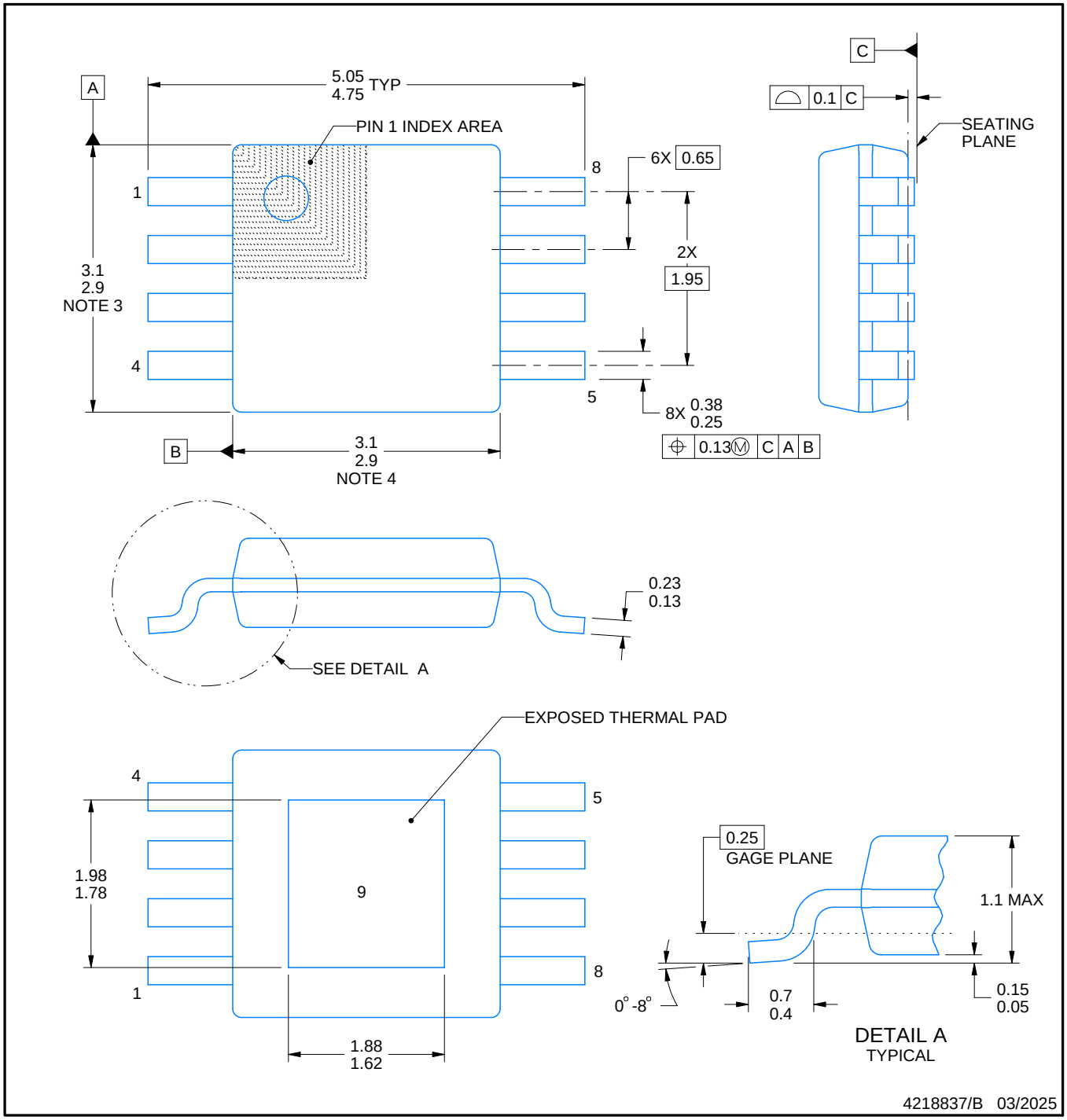
PACKAGE OUTLINE

DGN0008B



HVSSOP - 1.1 mm max height

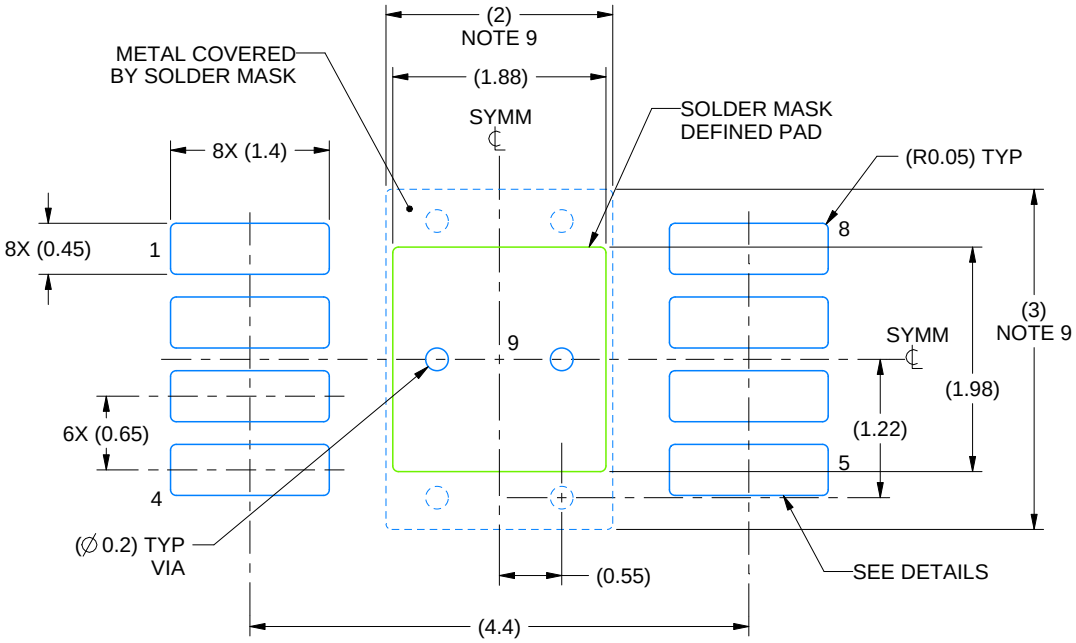
SMALL OUTLINE PACKAGE



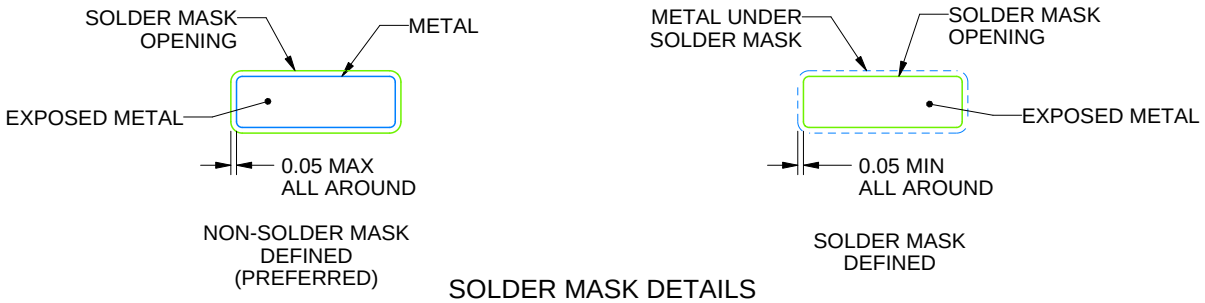
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

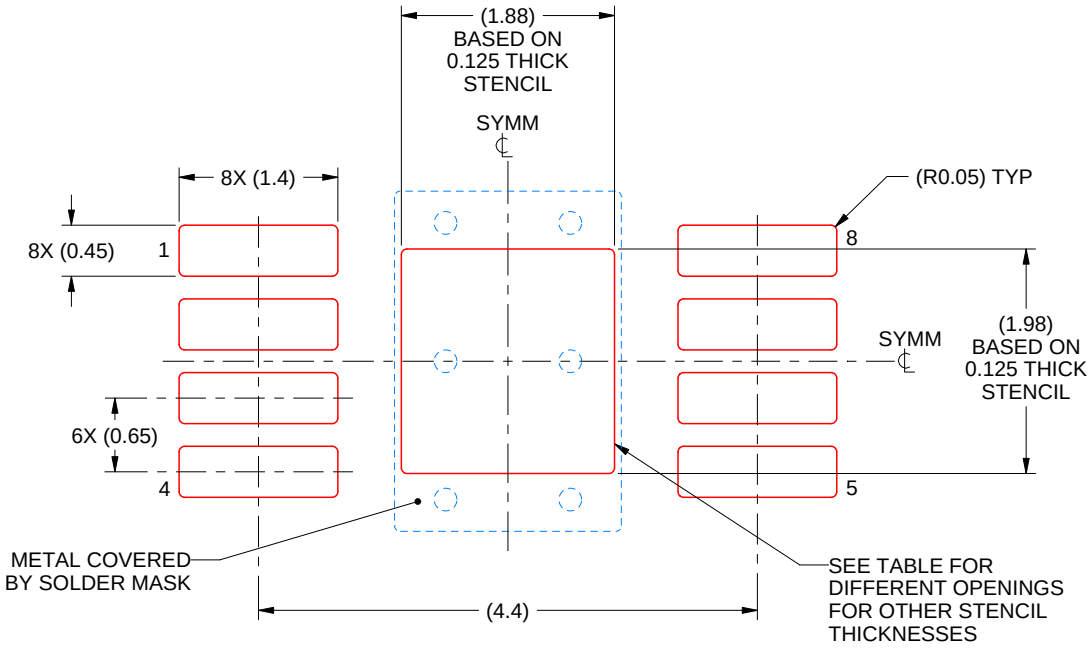


SOLDER MASK DETAILS

4218837/B 03/2025

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



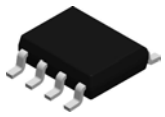
SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.10 X 2.21
0.125	1.88 X 1.98 (SHOWN)
0.15	1.72 X 1.81
0.175	1.59 X 1.67

4218837/B 03/2025

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

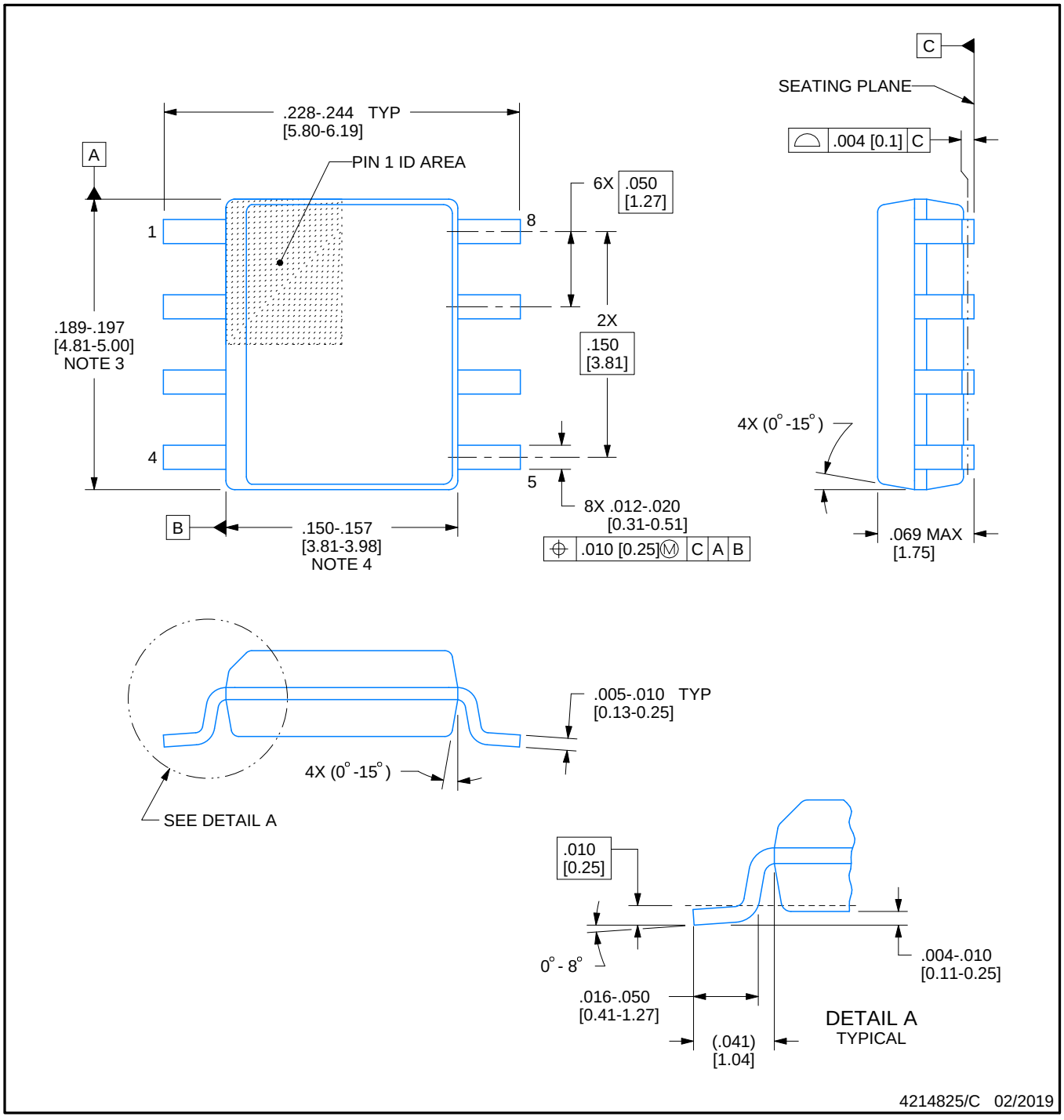


PACKAGE OUTLINE

D0008A

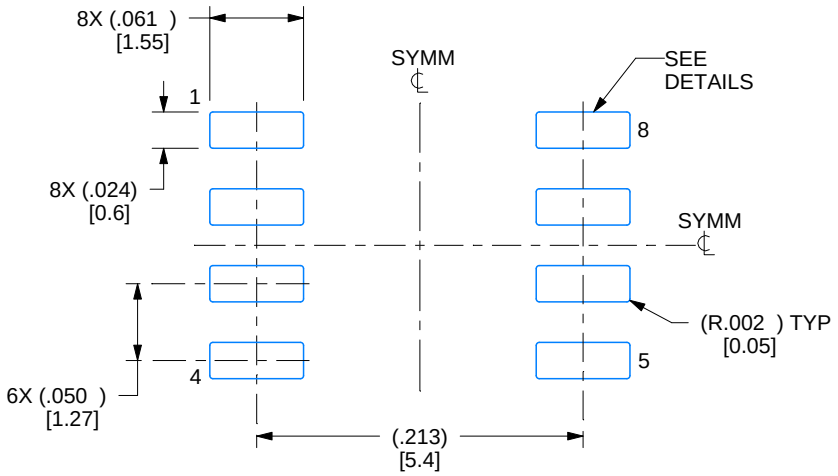
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

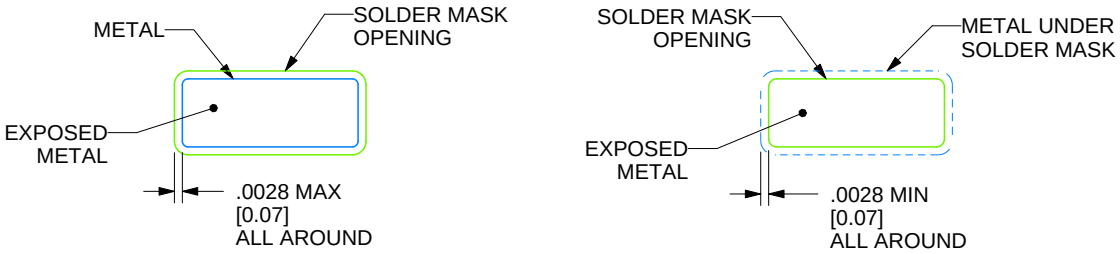


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

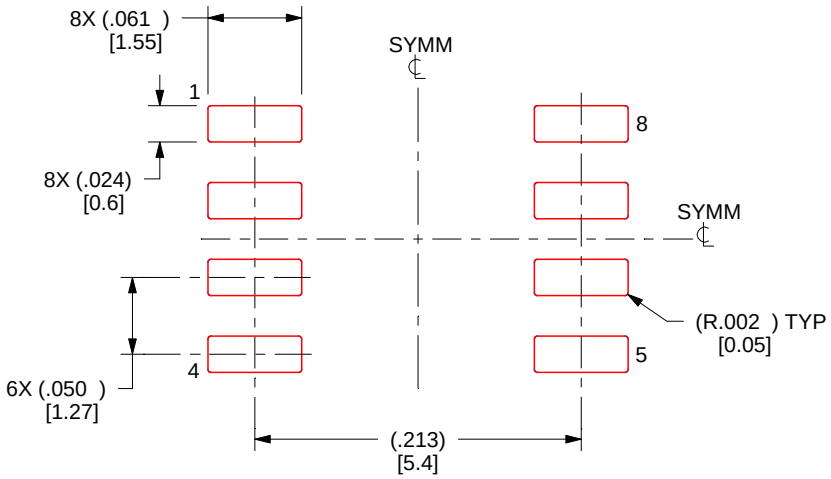
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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