UCC2742x、デュアル、4A、高速ローサイド MOSFET ドライバ、イネーブル付き

1 特長

- 業界標準のピン配置
- ドライバ毎のイネーブル機能
- 高い電流駆動能力:±4A
- 独自のバイポーラおよび CMOS ハイブリッド出力段により、MOSFET のミラー スレッショルドで高電流を供給
- 電源電圧から独立した TTL/CMOS 互換入力
- 標準立ち上がり時間 20ns、標準立ち下がり時間 15ns (1.8nF 負荷時)
- 標準伝播遅延時間:25ns (入力立ち下がり時)、35ns (入力立ち上がり時)
- 電源電圧:4V～15V
- 2 つの出力を並列に使用することで、より高い駆動電流を実現可能
- 熱特性が強化された MSOP PowerPAD™ パッケージで供給
- 定格:-40℃～125℃

2 アプリケーション

- スイッチ・モード電源
- DC/DC コンバータ
- モーター・コントローラ
- ライン・ドライバ
- Class-D スイッチング アンプ

3 概要

UCC2742x ファミリの高速デュアル MOSFET ドライバは、容量性負荷に対して大きなピーク電流を供給できます。3 種類の標準ロジック オプション (反転×2、非反転×2、反転×1 / 非反転×1) を用意しています。熱特性が強化された 8 ピン PowerPAD™ MSOP パッケージ (DGN) によって熱抵抗が大幅に低減され、長期的な信頼性が向上しています。標準の SOIC-8 (D) または PDIP-8 (P) パッケージでも供給されます。

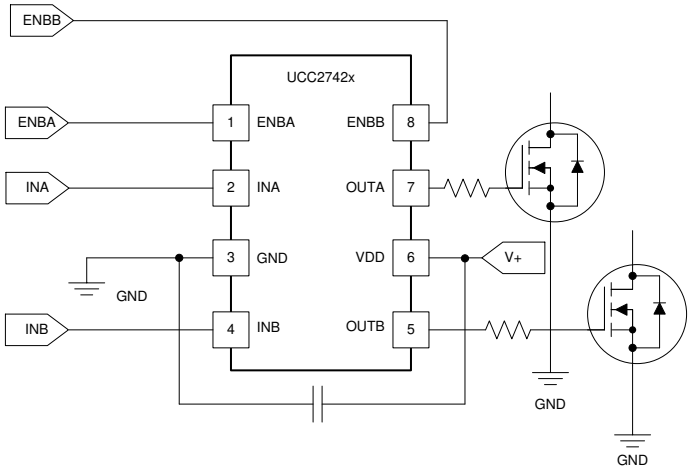
本質的に貫通電流を最小限に抑える設計によって、これらのドライバは、MOSFET のスイッチング遷移中のミラー領域で最も必要とされる 4A の電流を供給します。また、独自のバイポーラおよび MOSFET の並列ハイブリッド出力段により、低い電源電圧でも高効率の電流ソースおよびシンクが可能です。

UCC2742x は、イネーブル (ENB) 機能によって、ドライバ アプリケーションの動作をよりきめ細かく制御できます。ENBA および ENBB は、業界標準ピン配置では未使用だったピン 1 および 8 に実装されています。これらのピンは、アクティブ ハイ ロジックでは内部で V_{DD} にプルアップされ、標準動作時にはオープンにできます。

製品情報(1)

部品番号	パッケージ	本体サイズ (公称)
UCC27423 UCC27424 UCC27425	SOIC (8)	4.90mm × 3.91mm
	MSOP-PowerPAD (8)	3.00mm × 3.00mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。



アプリケーション概略図

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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4 Device Comparison Table

OUTPUT CONFIGURATION	TEMPERATURE RANGE $T_A = T_J$	PACKAGED DEVICES	
		SOIC-8 (D)(1)	MSOP-8 PowerPAD (DGN)(2)
Dual inverting	–40°C to 125°C	UCC27423D	UCC27423DGN
Dual nonInverting	–40°C to 125°C	UCC27424D	UCC27424DGN
One inverting, one noninverting	–40°C to 125°C	UCC27425D	UCC27425DGN

(1) D (SOIC-8) and DGN (PowerPAD-MSOP) packages are available taped and reeled. Add R suffix to device type (e.g. UCC27423DR, UCC27424DGNR) to order quantities of 2,500 devices per reel for D or 1,000 devices per reel for DGN package.
(2) The PowerPAD™ is not directly connected to any leads of the package. However, it is electrically and thermally connected to the substrate which is the ground of the device.

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5 Pin Configuration and Functions

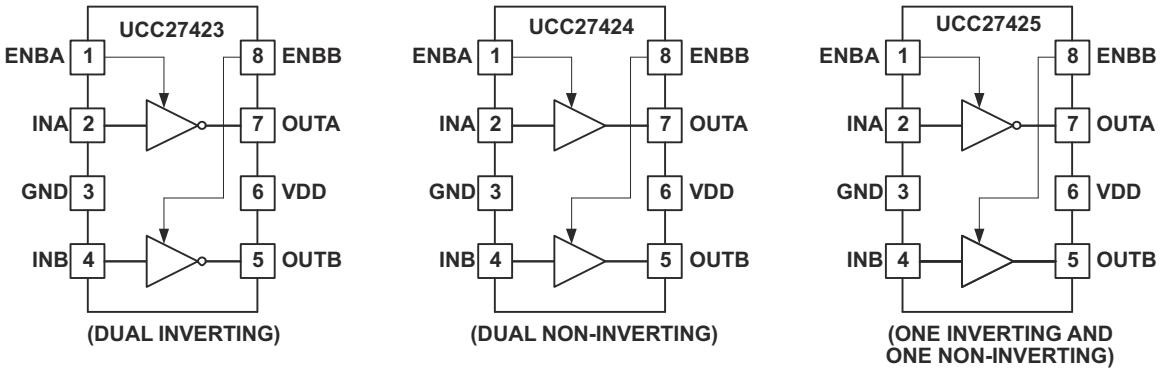

図 5-1. D Package, DGN Package 8-Pin SOIC, 8-PIn MSOP-PowerPAD Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
ENBA	1	I	Enable input for the driver A with logic compatible threshold and hysteresis. The driver output can be enabled and disabled with this pin. It is internally pulled up to V_{DD} with 100 kΩ resistor for active high operation. The output state when the device is disabled will be low regardless of the input state.
ENBB	8	I	Enable input for the driver B with logic compatible threshold and hysteresis. The driver output can be enabled and disabled with this pin. It is internally pulled up to V_{DD} with 100 kΩ resistor for active high operation. The output state when the device is disabled will be low regardless of the input state.(1)
GND	3	—	Common ground: this ground should be connected very closely to the source of the power MOSFET which the driver is driving.
INA	2	I	Input A: input signal of the A driver which has logic compatible threshold and hysteresis. If not used, this input should be tied to either V_{DD} or GND. It should not be left floating.(1)
INB	4	I	Input B. Input signal of the A driver which has logic compatible threshold and hysteresis. If not used, this input should be tied to either V_{DD} or GND. It should not be left floating.
OUTA	7	O	Driver output A. The output stage is capable of providing 4A drive current to the gate of a power MOSFET.
OUTB	5	O	Driver output B. The output stage is capable of providing 4A drive current to the gate of a power MOSFET.
V_{DD}	6	I	Supply. Supply voltage and the power input connection for this device.

(1) Refer to *セクション 7* for more details.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

			MIN	MAX	UNIT
V_{DD}	Supply voltage		–0.3	16	V
I_{OUT_DC}	Output current (OUTA, OUTB) DC			0.2	A
I_{OUT_PULSED}	Pulsed, (0.5 µs)			4.5	A
V_{IN}	Input voltage (INA, INB)		–5	6 or V_{DD} + 0.3 (whichever is larger)	V
	Enable voltage (ENBA, ENBB)		–0.3	6 or V_{DD} + 0.3 (whichever is larger)	V
	Power dissipation at T_A = 25°C	DGN package		3	W
		D package		650	mW
		P package		350	
T_J	Junction operating temperature		–55	150	°C
	Lead temperature (soldering, 10 s)			300	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) When V_{DD} ≤ 6 V, EN rating max value is 6 V; when V_{DD} > 6 V, EN rating max value is V_{DD} + 0.3 V.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	4		15	V
INA and INB	Input voltage	–2		15	V
ENA and ENB	Enable voltage	0		15	V
T_J	Operating junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		UCC2742x			UNIT
		D (SOIC)	DGN (MSOP)	P (PDIP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	107.3	56.6	55.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.2	52.8	45.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	47.3	32.6	32.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.2	1.8	23.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	46.8	32.3	32.5	°C/W

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6.4 Thermal Information (続き)

THERMAL METRIC[1]		UCC2742x			UNIT
		D (SOIC)	DGN (MSOP)	P (PDIP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	5.9	–	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

V_{DD} = 4.5 V to 15 V, T_A = –40°C to 125°C, T_A = T_J, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT (INA, INB)						
V_{IN_H}	Logic 1 input threshold		1.6	2.2	2.5	V
V_{IN_L}	Logic 0 input threshold		0.8	1.2	1.5	V
	Input current	0 V ≤ V_{IN} ≤ V_{DD}	–10	0	10	µA
OUTPUT (OUTA, OUTB)						
	Output current	V_{DD} = 14 V (1)		4		A
R_{OH}	Output resistance high	I_{OUT} = –10 mA(2)		1.2	2.5	Ω
R_{OL}	Output resistance low	I_{OUT} = 10 mA		0.7	1.2	Ω
SWITCHING TIME						
t_r	Rise time (OUTA, OUTB)	C_{LOAD} = 1.8 nF		20	40	ns
t_f	Fall time (OUTA, OUTB)	C_{LOAD} = 1.8 nF		15	40	ns
t_{d1}	Delay, IN rising (IN to OUT)	C_{LOAD} = 1.8 nF		25	40	ns
t_{d2}	Delay, IN falling (IN to OUT)	C_{LOAD} = 1.8 nF		35	50	ns
ENABLE (ENBA, ENBB)						
V_{IN_H}	High-level input voltage	LO to HI transition	1.7	2.4	2.9	V
V_{IN_L}	Low-level input voltage	HI to LO transition	1.1	1.8	2.2	V
	Hysteresis		0.15	0.55	0.90	V
R_{ENB}	Enable impedance	V_{DD} = 14 V, ENB = GND	75	100	140	kΩ
t_{D3}	Propagation delay time (see 図 6-3)	C_{LOAD} = 1.8 nF		30	60	ns
t_{D4}	Propagation delay time (see 図 6-3)	C_{LOAD} = 1.8 nF		100	150	ns
OVERALL						
I_{DD}	UCC27423 Static operating current, V_{DD} = 15 V, ENBA = ENBB = 15 V	INA = 0 V, INB = 0 V		900	1350	µA
		INA = 0 V, INB = HIGH		750	1100	µA
		INA = HIGH, INB = 0 V		750	1100	µA
		INA = HIGH, INB = HIGH		600	900	µA
I_{DD}	UCC27424 Static operating current, V_{DD} = 15 V, ENBA = ENBB = 15 V	INA = 0 V, INB = 0 V		300	450	µA
		INA = 0 V, INB = HIGH		750	1100	µA
		INA = HIGH, INB = 0 V		750	1100	µA
		INA = HIGH, INB = HIGH		1200	1800	µA
I_{DD}	UCC27425 Static operating current, V_{DD} = 15 V, ENBA = ENBB = 15 V	INA = 0 V, INB = 0 V		600	900	µA
		INA = 0 V, INB = HIGH		1050	1600	µA
		INA = HIGH, INB = 0 V		450	700	µA
		INA = HIGH, INB = HIGH		900	1350	µA
I_{DD}	All disabled, V_{DD} = 15 V, ENBA = ENBB = 0 V	INA = 0 V, INB = 0 V		300	450	µA
		INA = 0 V, INB = HIGH		450	700	µA
		INA = HIGH, INB = 0 V		450	700	µA
		INA = HIGH, INB = HIGH		600	900	µA

(1) Parameter not tested in the production
(2) Output pullup resistance in this table is a DC measurement that measures resistance of PMOS structure only (not N-channel structure).

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6.6 Dissipation Ratings

PACKAGE	SUFFIX	POWER RATING (mW) T_A = 70°C(1)	DERATING FACTOR ABOVE 70°C (mW/°C)(1)
SOIC-8	D	344–655(2)	6.25–11.9(2)
PDIP-8	P	500	9
MSOP(3)	DGN	1370	17.1

(1) 125°C operating junction temperature is used for power rating calculations
(2) The range of values indicates the effect of pc-board. These values are intended to give the system designer an indication of the best and worst case conditions. In general, the system designer should attempt to use larger traces on the pc-board where possible in order to spread the heat away form the device more effectively. For information on the PowerPAD™ package, refer to Technical Brief, *PowerPad Thermally Enhanced Package*, Texas Instruments (SLMA002) and Application Brief, *PowerPad Made Easy*, Texas Instruments (SLMA004).
(3) The PowerPAD™ is not directly connected to any leads of this package. However, it is electrically and thermally connected to the substrate which is the ground of the device.

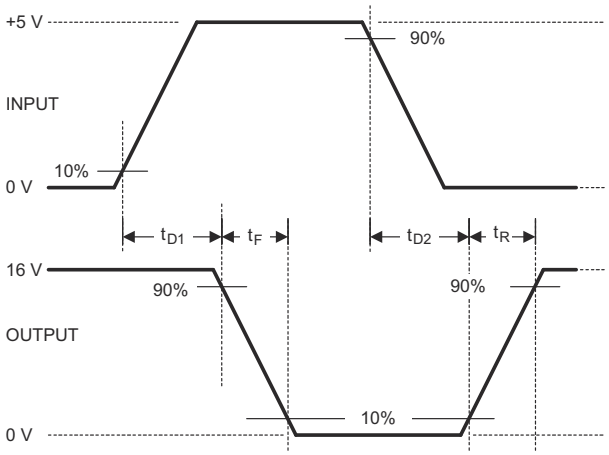


図 6-1. Inverting Driver Switching

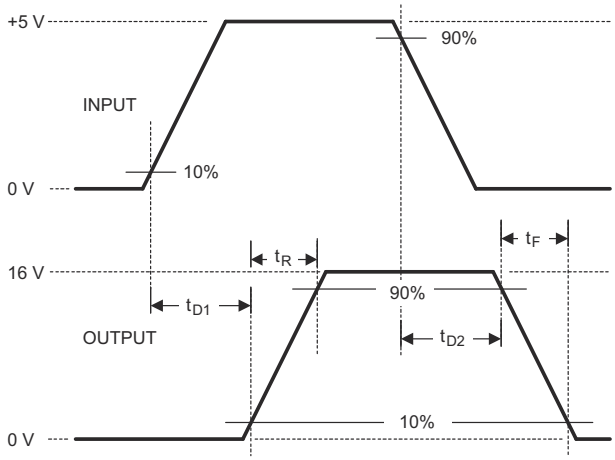
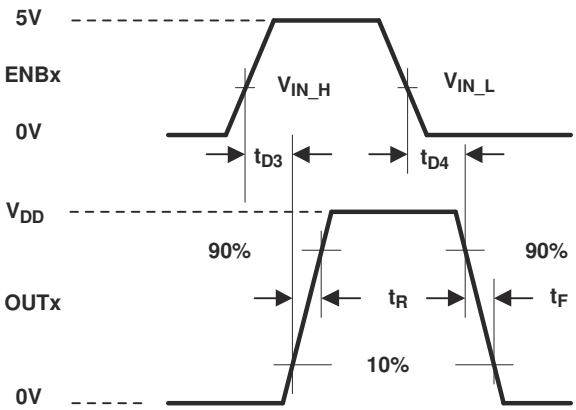


図 6-2. Noninverting Driver Switching



The 10% and 90% thresholds depict the dynamics of the BiPolar output devices that dominate the power MOSFET transition through the Miller regions of operation.

図 6-3. Switching Waveform for Enable to Output

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6.7 Typical Characteristics

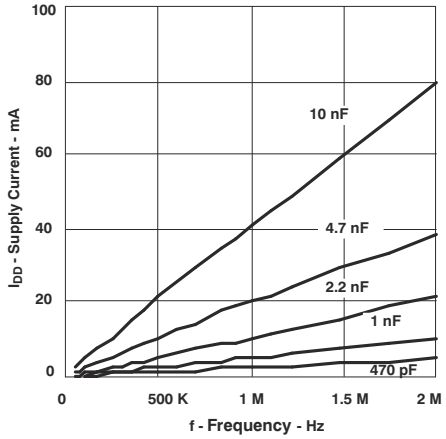

図 6-4. Supply Current vs Frequency (V_{DD} = 4.5 V)

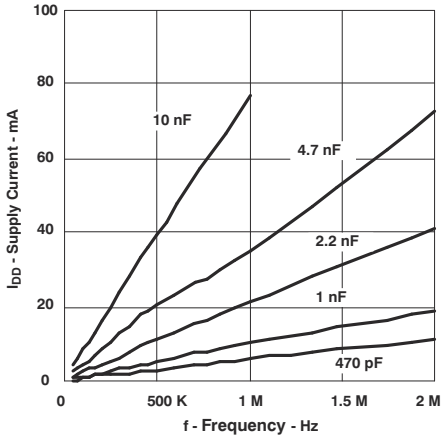

図 6-5. Supply Current vs Frequency (V_{DD} = 8.0 V)

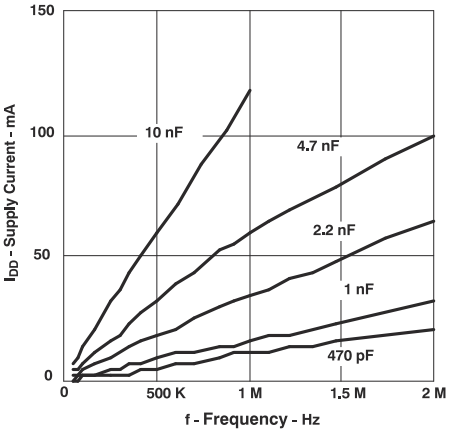

図 6-6. Supply Current vs Frequency (V_{DD} = 12 V)

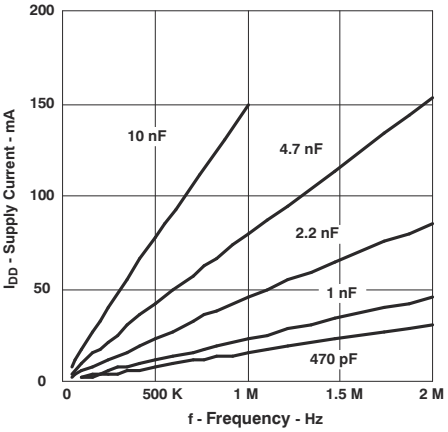

図 6-7. Supply Current vs Frequency (V_{DD} = 15 V)

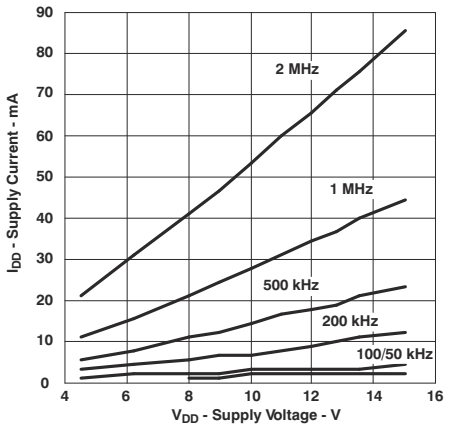

図 6-8. Supply Current vs Supply Voltage (C_{LOAD} = 2.2 nF)

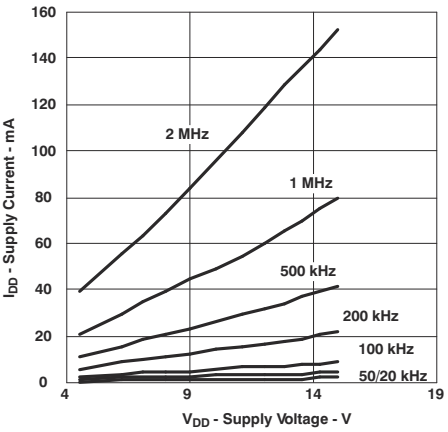

図 6-9. Supply Current vs Supply Voltage (C_{LOAD} = 4.7 nF)

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6.7 Typical Characteristics (continued)

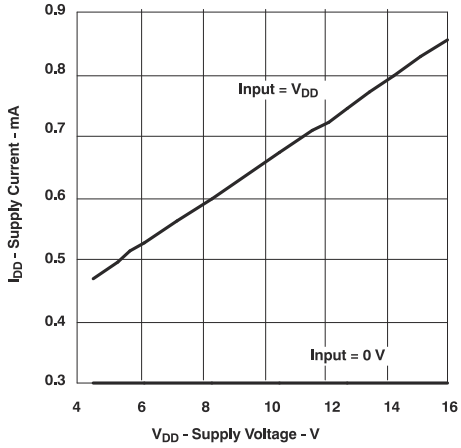

図 6-10. Supply Current vs Supply Voltage (UCC27423)

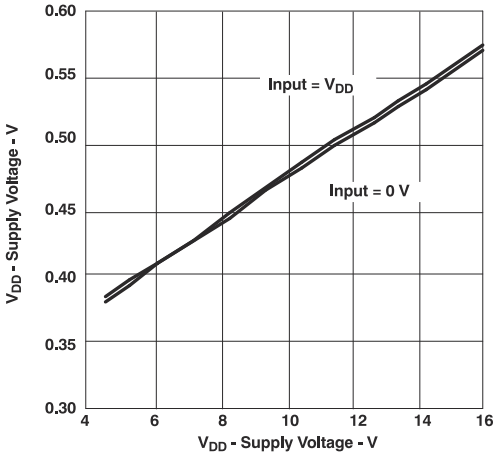

図 6-11. Supply Current vs Supply Voltage (UCC27424)

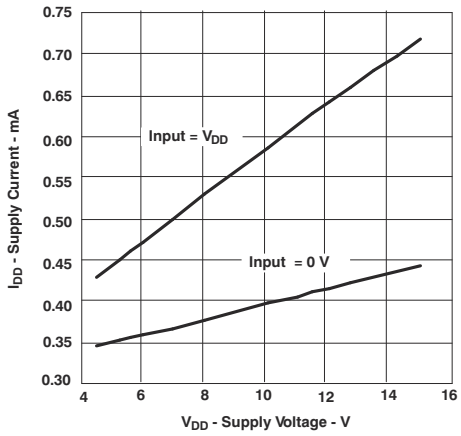

図 6-12. Supply Current vs Supply Voltage (UCC27425)

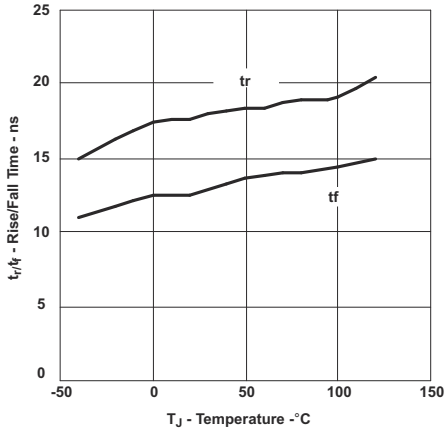

図 6-13. Rise Time and Fall Time vs Temperature (UCC27423)

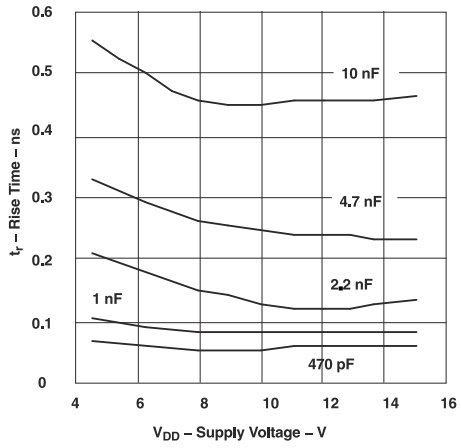

図 6-14. Rise Time vs Supply Voltage

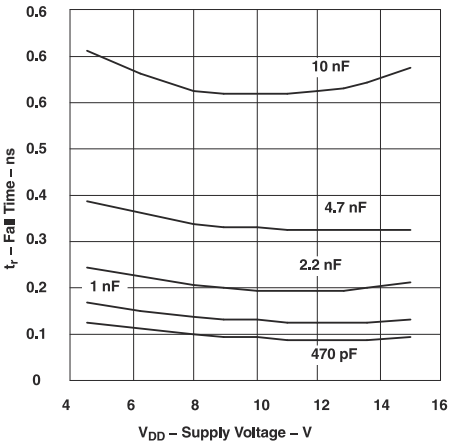

図 6-15. Fall Time vs Supply Voltage

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6.7 Typical Characteristics (continued)

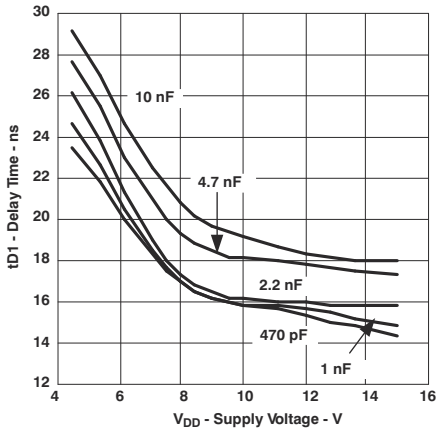

図 6-16. Delay Time (t_{D1}) vs Supply Voltage (UCC27423)

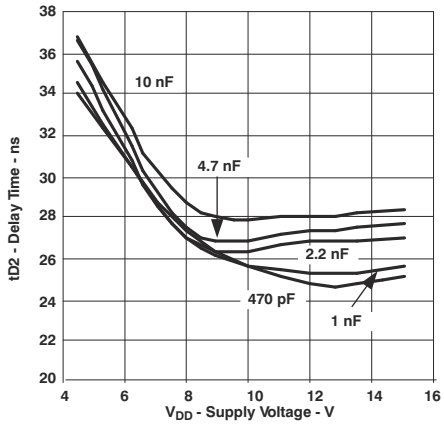

図 6-17. Delay Time (t_{D2}) vs Supply Voltage (UCC27423)

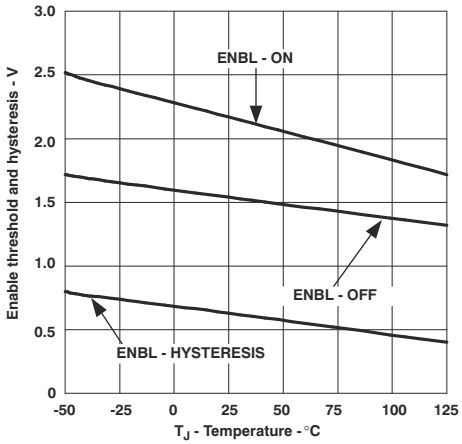

図 6-18. Enable Threshold and Hysteresis vs Temperature

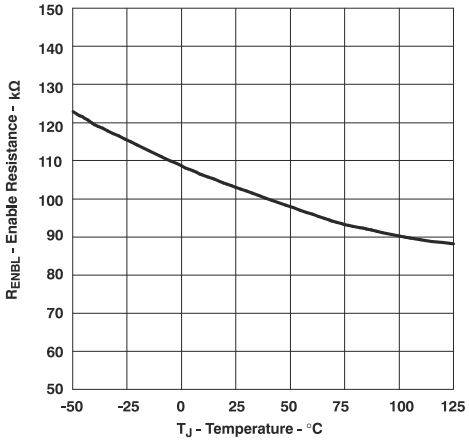

図 6-19. Enable Resistance vs Temperature

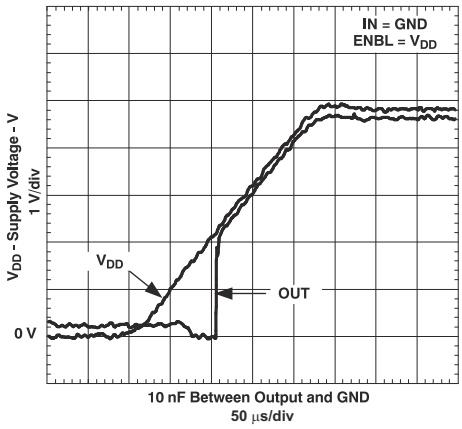

図 6-20. Output Behavior vs Supply Voltage (Inverting)

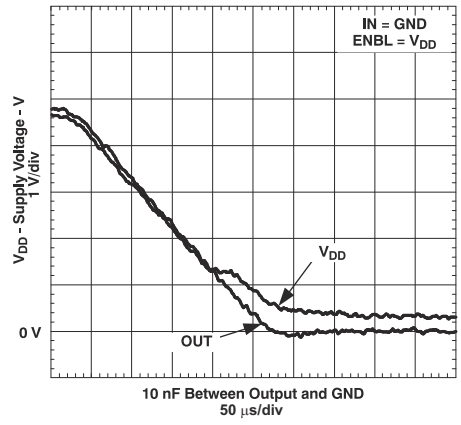

図 6-21. Output Behavior vs Supply Voltage (Inverting)

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6.7 Typical Characteristics (continued)

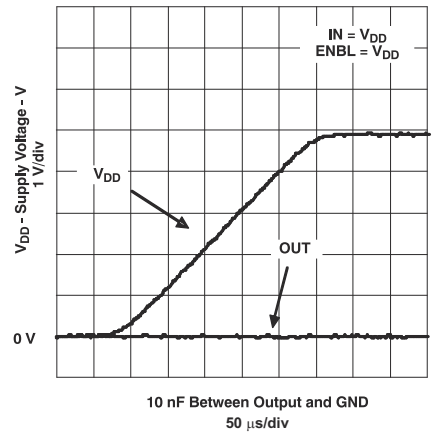

図 6-22. Output Behavior vs V_{DD} (Inverting)

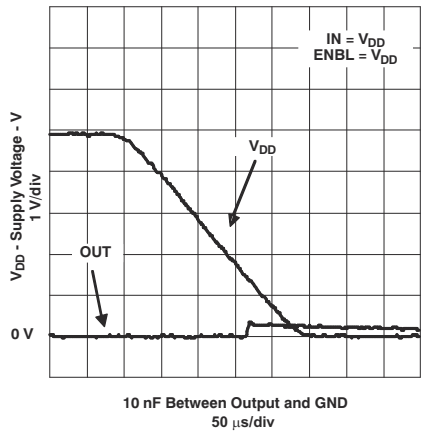

図 6-23. Output Behavior vs V_{DD} (Inverting)

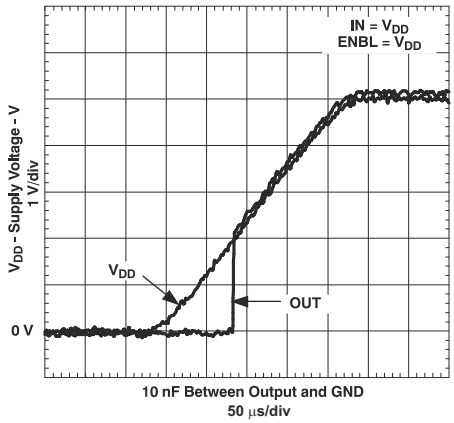

図 6-24. Output Behavior vs V_{DD} (Noninverting)

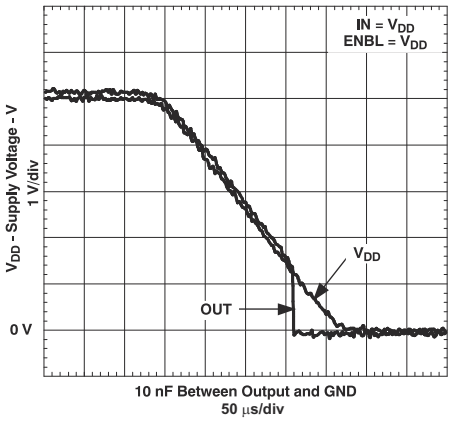

図 6-25. Output Behavior vs V_{DD} (Noninverting)

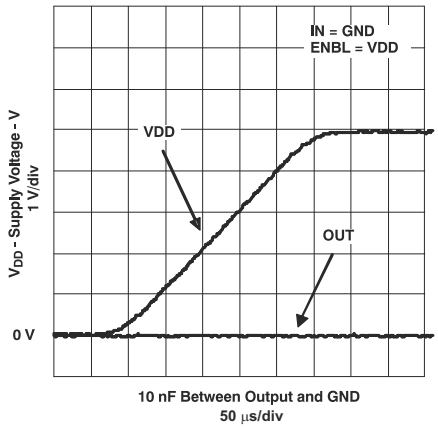

図 6-26. Output Behavior vs V_{DD} (Noninverting)

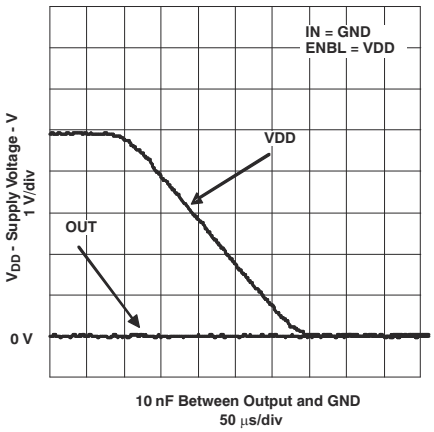

図 6-27. Output Behavior vs V_{DD} (Noninverting)

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6.7 Typical Characteristics (continued)

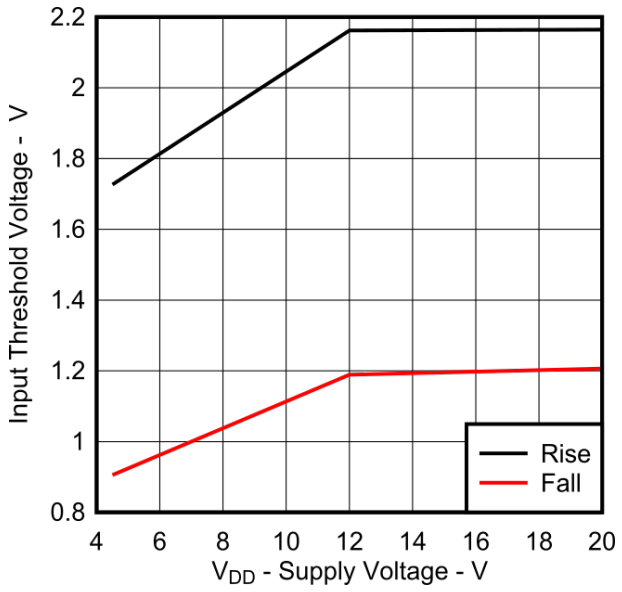


図 6-28. Input Threshold vs Supply Voltage

7 Detailed Description

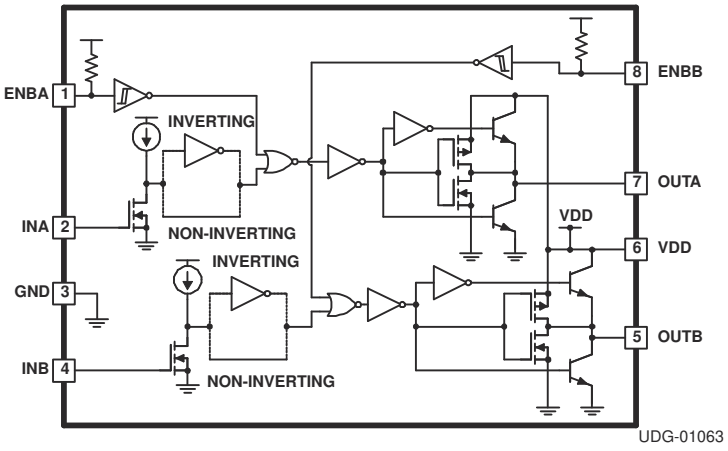
7.1 Overview

The UCC2742x family of high-speed dual MOSFET drivers can deliver large peak currents into capacitive loads. Three standard logic options are offered – dual-inverting, dual-noninverting and one-inverting and one-noninverting driver. The thermally enhanced 8-pin PowerPAD™ MSOP package (DGN) drastically lowers the thermal resistance to improve long-term reliability. It is also offered in the standard SOIC-8 (D) or PDIP-8 (P) packages. Using a design that inherently minimizes shoot-through current, these drivers deliver 4A of current where it is needed most at the Miller plateau region during the MOSFET switching transition. A unique Bipolar and MOSFET hybrid output stage in parallel also allows efficient current sourcing and sinking at low supply voltages. 表 7-1 highlights more details about UCC2742x.

表 7-1. UCC2742x Features and Benefits

FEATURE	BENEFIT
1-ns (typ) delay matching between channels	Ease of paralleling outputs for higher (2 times) current capability, ease of driving parallel-power switches
Expanded V_{DD} operating range of 4 to 15 V	Flexibility in system design
Outputs enabled when enable pins (ENx) in floating condition	Pin-to-pin compatibility with the UCC27324 device from Texas Instruments and industry standard pinout, in designs where Pin 1 and Pin 8 are in floating condition
CMOS/TTL compatible input and enable threshold with wide hysteresis	Enhanced noise immunity, while retaining compatibility with microcontroller logic-level inputs signals (3.3 V, 5 V) optimized for digital power
Ability to handle –5 V_{DC} (max) at input pins (INA/B)	Increased robustness in noisy environments

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Enable

UCC2742x provides dual Enable inputs for improved control of each driver channel operation. The inputs incorporate logic compatible thresholds with hysteresis. They are internally pulled up to V_{DD} with 100kΩ resistor for active high operation. When ENBA and ENBB are driven high, the drivers are enabled and when ENBA and ENBB are low, the drivers are disabled. The default state of the Enable pin is to enable the driver and therefore can be left open for standard operation. However, if the enable pin is left open, it is recommended to terminate any PCB traces to be as short as possible to limit noise. If large noise is present due to non-optimal PCB layout, it is recommended to tie the Enable pin to Vcc or to add a filter capacitor (0.1 µF) to the Enable pin. The output states when the drivers are disabled is low regardless of the input state. See the truth table of 表 7-2 for the operation using enable logic.

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Enable input are compatible with both logic signals and slow changing analog signals. They can be directly driven or a power-up delay can be programmed with a capacitor between ENBA, ENBB and AGND. ENBA and ENBB control input A and input B respectively.

7.3.2 Input Stage

The input thresholds have 3.3 V logic sensitivity over the full range of V_{DD} voltages; it is equally compatible with 0 to V_{DD} signals. The inputs of the UCC2742x driver family are designed to withstand 500-mA reverse current without damaging the IC for logic upset. The input stage of each driver should be driven by a signal with a short rise or fall time. This condition is satisfied in typical power supply applications where the input signals are provided by a PWM controller or logic gates with fast transition times (<200 ns). The input stages to the drivers function as a digital gate, and they are not intended for applications where a slow changing input voltage is used to generate a switching output when the logic threshold of the input section is reached. While this may not be harmful to the driver, the output of the driver may switch repeatedly at a high frequency.

Users should not attempt to shape the input signals to the driver in an attempt to slow down (or delay) the signal at the output. If limited rise or fall times to the power device is desired, an external resistance can be added between the output of the driver and the load device which is generally a power MOSFET gate. The external resistor may also help remove power dissipation from the device package, as discussed in the section on Thermal Considerations.

Importantly, input signal of the two channels, INA and INB, which has logic compatible threshold and hysteresis. If not used, INA and INB must be tied to either V_{DD} or GND; it must not be left floating.

7.3.3 Output Stage

Inverting output s of the UCC27423 and OUTA of the UCC27425 are intended to drive external P-channel MOSFETs. Noninverting outputs of the UCC27424 and OUTB of the UCC27425 are intended to drive external N-Channel MOSFETs. Each output stage is capable of supplying ±4 A peak current pulses and swings to both V_{DD} and GND. The pullup/pulldown circuits of the driver are constructed of bipolar and MOSFET transistors in parallel. The peak output current rating is the combined current from the bipolar and MOSFET transistors. The output resistance is the $R_{DS(on)}$ of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor. Each output stage also provides very low impedance to overshoot and undershoot due to the body diode of the external MOSFET. This means that in many cases, external-Schottky-clamp diodes are not required. The UCC2742x family delivers 4 A of gate drive where it is most needed during the MOSFET switching transition (at the Miller plateau region) providing improved efficiency gains. A unique Bipolar and MOSFET hybrid output stage in parallel also allows efficient current sourcing at low supply voltages.

7.4 Device Functional Modes

With V_{DD} power supply in the range of 4 V to 16 V, the output stage is dependent on the states of the HI and LI pins. 表 7-2 shows the UCC2742x truth table.

表 7-2. Input/Output Logic

		INPUTS (VIN_L, VIN_H)		UCC27423		UCC27424		UCC27425	
ENBA	ENBB	INA	INB	OUTA	OUTB	OUTA	OUTB	OUTA	OUTB
H	H	L	L	H	H	L	L	H	L
H	H	L	H	H	L	L	H	H	H
H	H	H	L	L	H	H	L	L	L
H	H	H	H	L	L	H	H	L	H
L	L	X	X	L	L	L	L	L	L

Importantly, if INA and INB are not used, they must be tied to either V_{DD} or GND; it must not be left floating.

8 Application and Implementation

注

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8.1 Application Information

High frequency power supplies often require high-speed, high-current drivers such as the UCC2742x family. A leading application is the need to provide a high power buffer stage between the PWM output of the control IC and the gates of the primary power MOSFET or IGBT switching devices. In other cases, the driver IC is utilized to drive the power device gates through a drive transformer. Synchronous rectification supplies also have the need to simultaneously drive multiple devices which can present an extremely large load to the control circuitry.

Driver ICs are utilized when it is not feasible to have the primary PWM regulator IC directly drive the switching devices for one or more reasons. The PWM IC may not have the brute drive capability required for the intended switching MOSFET, limiting the switching performance in the application. In other cases there may be a desire to minimize the effect of high frequency switching noise by placing the high current driver physically close to the load. Also, newer ICs that target the highest operating frequencies may not incorporate onboard gate drivers at all. Their PWM outputs are only intended to drive the high impedance input to a driver such as the UCC2742x. Finally, the control IC may be under thermal stress due to power dissipation, and an external driver can help by moving the heat from the controller to an external package.

8.2 Typical Application

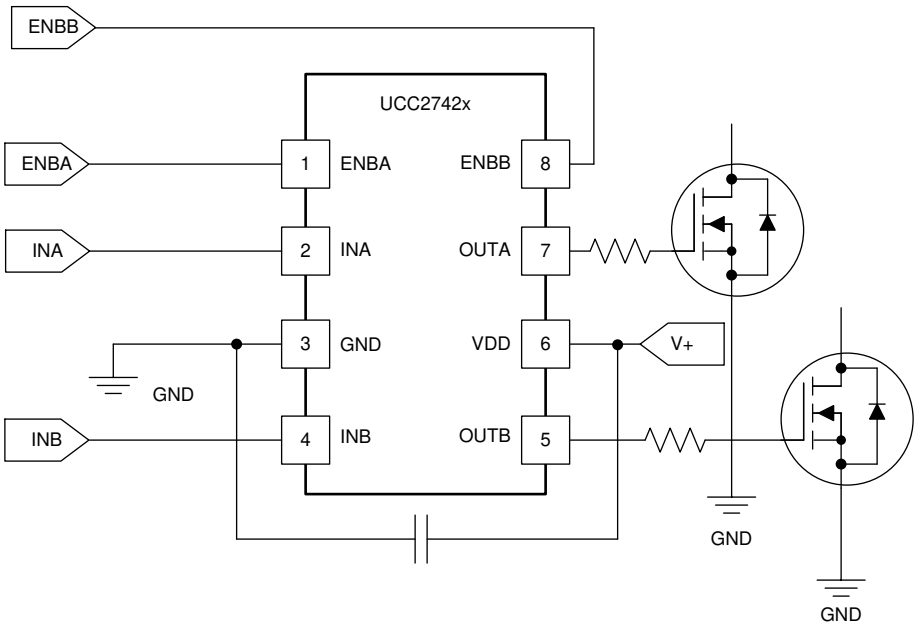

図 8-1. UCC2742x Driving Two Independent MOSFETs

8.2.1 Design Requirements

To select proper device from UCC2742x family, it is recommended to first check the appropriate logic for the outputs. UCC27423 has dual inverting outputs; UCC27424 has dual non-inverting outputs; UCC27425 has an inverting channel A and non-inverting channel B. Moreover, some considerations must be evaluated in order to make the most appropriate selection. Among these considerations are V_{DD}, drive current, and power dissipation.

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8.2.2 Detailed Design Procedure

8.2.2.1 Source and Sink Capabilities During Miller Plateau

Large power MOSFETs present a large load to the control circuitry. Proper drive is required for efficient, reliable operation. The UCC2742x drivers have been optimized to provide maximum drive to a power MOSFET during the Miller plateau region of the switching transition. This interval occurs while the drain voltage is swinging between the voltage levels dictated by the power topology, requiring the charging and discharging of the drain-gate capacitance with current supplied or removed by the driver device.

Two circuits are used to test the current capabilities of the UCC2742x driver. In each case external circuitry is added to clamp the output near 5 V while the IC is sinking or sourcing current. An input pulse of 250 ns is applied at a frequency of 1 kHz in the proper polarity for the respective test. In each test there is a transient period where the current peaked up and then settled down to a steady-state value. The noted current measurements are made at a time of 200 ns after the input pulse is applied, after the initial transient.

The circuit in 図 8-2 is used to verify the current sink capability when the output of the driver is clamped around 5V, a typical value of gate-source voltage during the Miller plateau region. The UCC2742x is found to sink 4.5 A at V_{DD} = 15 V and 4.28 A at V_{DD} = 12 V.

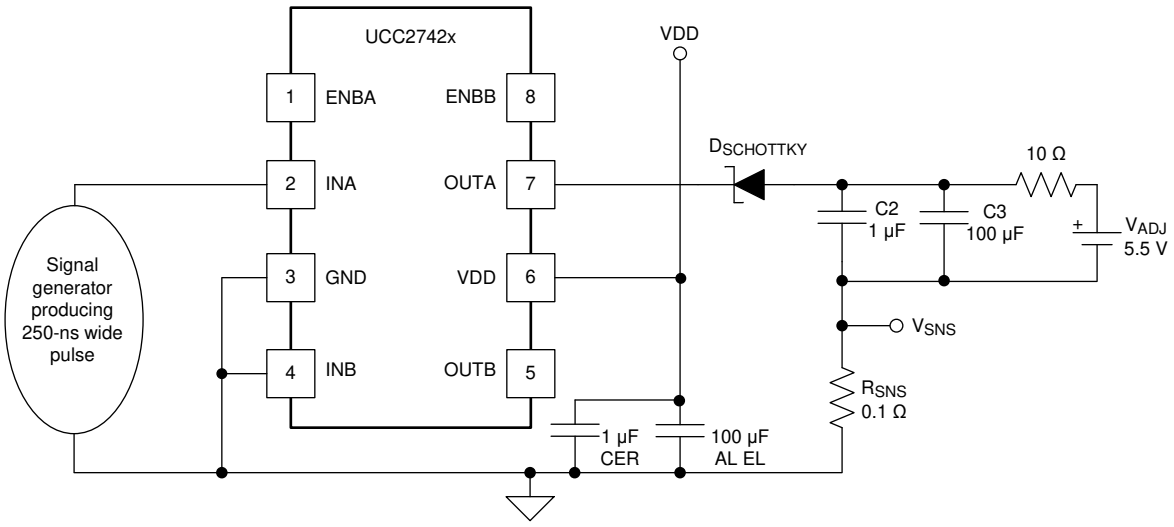

図 8-2. Current Sink Capability Test

The circuit show in 図 8-3 is used to test the current source capability with the output clamped around 5 V with a string of Zener diodes. The UCC2742x is found to source 4.8 A at V_{DD} = 15 V and 3.7 A at V_{DD} = 12 V.

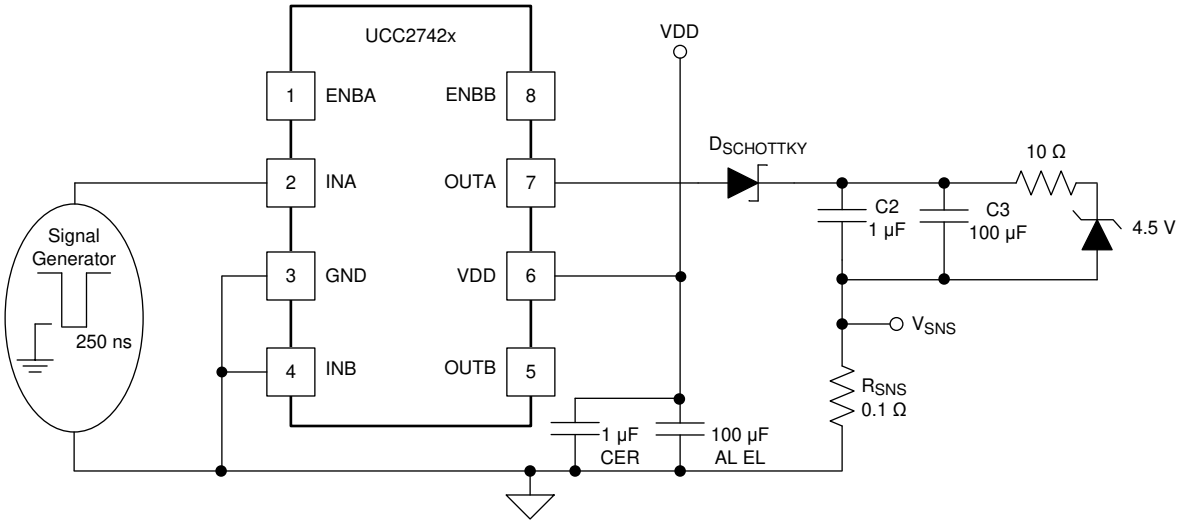

図 8-3. Current Source Capability Test

8.2.2.2 Parallel Outputs

The A and B drivers may be combined into a single driver by connecting the INA and INB inputs together and the OUTA and OUTB outputs together. Then, a single signal can control the paralleled combination as shown in 図 8-4.

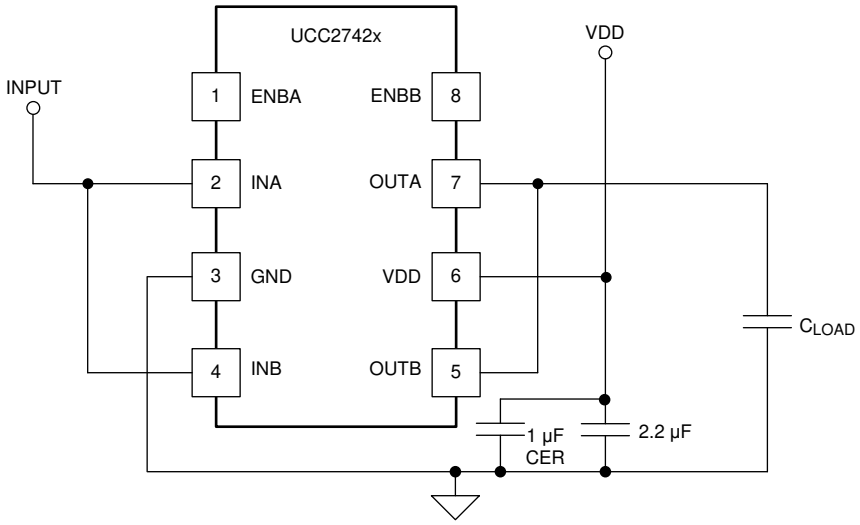

図 8-4. Parallel Operation of UCC27423 and UCC27424

Important consideration about paralleling two channels for UCC27423/4 include the INA and INB should be shorted in PCB layout as close to the device as possible, as well as for OUTA and OUTB, in which condition PCB layout parasitic mismatching between two channels could be minimized. The INA/B slope signal should be fast enough to avoid mismatched V_{IN_H} / V_{IN_L}, t_{d1} / t_{d2} between channel-A and channel-B. It is recommended to have input signal slope faster than 20 V/us.

8.2.2.3 V_{DD}

Although quiescent V_{DD} current is very low, total supply current will be higher, depending on OUTA and OUTB current and the programmed oscillator frequency. Total V_{DD} current is the sum of quiescent V_{DD} current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Q_g), average OUT current can be calculated from 式 1.

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$$I_{OUT} = Q_g \times f \quad (1)$$

where

- f = switching frequency

For the best high-speed circuit performance, two V_{DD} bypass capacitors are recommended to prevent noise problems. The use of surface mount components is highly recommended. A 0.1µF ceramic capacitor should be located closest to the V_{DD} to ground connection. In addition, a larger capacitor (such as 1µF) with relatively low ESR should be connected in parallel, to help deliver the high current peaks to the load. The parallel combination of capacitors should present a low impedance characteristic for the expected current levels in the driver application.

8.2.2.4 Drive Current and Power Requirements

The UCC2742x family of drivers are capable of delivering 4 A of current to a MOSFET gate for a period of several hundred nanoseconds. High peak current is required to turn the device ON quickly. Then, to turn the device OFF, the driver is required to sink a similar amount of current to ground. This repeats at the operating frequency of the power device. A MOSFET is used in this discussion because it is the most common type of switching device used in high frequency power conversion equipment.

References 1 and 2 in *セクション 11.2* discuss the current required to drive a power MOSFET and other capacitive-input switching devices. Reference 2 in *セクション 11.2* includes information on the previous generation of bipolar IC gate drivers.

When a driver IC is tested with a discrete, capacitive load it is a fairly simple matter to calculate the power that is required from the bias supply. The energy that must be transferred from the bias supply to charge the capacitor is given by 式 2.

$$E = \frac{1}{2}CV^2 \quad (2)$$

where

- C = load capacitor, and V = bias voltage (feeding the driver)

There is an equal amount of energy transferred to ground when the capacitor is discharged. This leads to a power loss given by 式 3.

$$P = CV^2 \times f \quad (3)$$

where

- f = switching frequency

This power is dissipated in the resistive elements of the circuit. Thus, with no external resistor between the driver and gate, this power is dissipated inside the driver. Half of the total power is dissipated when the capacitor is charged, and the other half is dissipated when the capacitor is discharged. An actual example using the conditions of the previous gate drive waveform should help clarify this.

With V_{DD} = 12 V, C_{LOAD} = 10 nF, and f = 300 kHz, the power loss can be calculated as 式 4.

$$P = 10\ nF \times (12\ V)^2 \times (300\ kHz) = 0.432\ W \quad (4)$$

With a 12 V supply, this would equate to a current of 式 5.

$$I = \frac{P}{V} = \frac{0.432\ W}{12\ V} = 36\ mA \quad (5)$$

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The actual current measured from the supply was 0.037A, and is very close to the predicted value. But, the I_{DD} current that is due to the IC internal consumption should be considered. With no load the IC current draw is 0.0027 A. Under this condition the output rise and fall times are faster than with a load. This could lead to an almost insignificant, yet measurable current due to cross-conduction in the output stages of the driver. However, these small current differences are buried in the high frequency switching spikes, and are beyond the measurement capabilities of a basic lab setup. The measured current with 10 nF load is reasonably close to that expected.

The switching load presented by a power MOSFET can be converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain of the device between the ON and OFF states. Most manufacturers provide specifications that provide the typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Q_g, one can determine the power that must be dissipated when charging a capacitor. This is done by using the equivalence $Q_g = C_{eff}V$ to provide the power loss in 式 6.

$$P = C \times V^2 \times f = V \times Q_g \times f \tag{6}$$

This equation allows a power designer to calculate the bias power required to drive a specific MOSFET gate at a specific bias voltage.

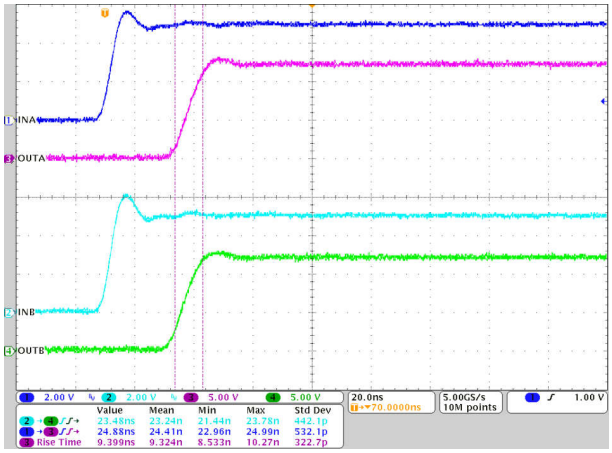
8.2.3 Application Curves

図 8-5 and 図 8-6 shows rising/falling time and turn-on/off propagation delay testing waveform in room temperature for UCC27424, and waveform measurement data (see the bottom part of the waveform). Each channel, INA/INB/OUTA/OUTB, is labeled and displayed on the left hand of the waveforms.

The load capacitance testing condition is 1.8 nF, V_{DD} = 12 V, and f = 300 kHz.

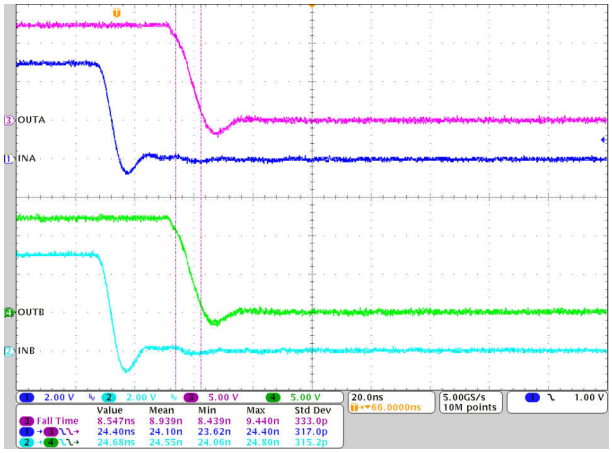
HI and LI share one same input from function generator, therefore, besides the propagation delay and rising/falling time, the difference of the propagation delay between HO and LO gives the propagation delay matching data.

Note the linear rise and fall edges of the switching waveforms. This is due to the constant output current characteristic of the driver as opposed to the resistive output impedance of traditional MOSFET-based gate drivers.



CL = 1.8 nF, V_{DD} = 12 V, f = 300 kHz

図 8-5. Rising Time and Turnon Propagation Delay



CL = 1.8 nF, V_{DD} = 12 V, f = 300 kHz

図 8-6. Falling Time and Turnoff Propagation Delay

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9 Power Supply Recommendations

The recommended bias supply voltage range for UCC2742x is from 4 V to 15 V. The upper end of this range is driven by the 16 V absolute maximum voltage rating of the V_{DD}. It is recommended to keep proper margin to allow for transient voltage spikes.

A local bypass capacitor should be placed between the VDD and GND pins. And this capacitor should be located as close to the device as possible. A low ESR, ceramic surface mount capacitor is recommended. TI recommends using 2 capacitors across VDD and GND: a 100 nF ceramic surface-mount capacitor for high frequency filtering placed very close to VDD and GND pin, and another surface-mount capacitor, 220 nF to 10 µF, for IC bias requirements.

10 Layout

10.1 Layout Guidelines

Optimum performance of gate drivers cannot be achieved without taking due considerations during circuit board layout. The following points are emphasized:

1. Low ESR/ESL capacitors must be connected close to the IC between VDD and GND pins to support high peak currents drawn from VDD during the turn-on of the external MOSFETs.
2. Grounding considerations:
   - The first priority in designing grounding connections is to confine the high peak currents that charge and discharge the MOSFET gates to a minimal physical area. This will decrease the loop inductance and minimize noise issues on the gate terminals of the MOSFETs. The gate driver should be placed as close as possible to the MOSFETs.
   - Star-point grounding is a good way to minimize noise coupling from one current loop to another. The GND of the driver is connected to the other circuit nodes such as source of power MOSFET and ground of PWM controller at one, single point. The connected paths must be as short as possible to reduce inductance.
   - Use a ground plane to provide noise shielding. Fast rise and fall times at OUT may corrupt the input signals during transition. The ground plane must not be a conduction path for any current loop. Instead the ground plane must be connected to the star-point with one single trace to establish the ground potential. In addition to noise shielding, the ground plane can help in power dissipation as well.
3. In noisy environments, tying inputs of an unused channel of the UCC2742x device to VDD or GND using short traces in order to ensure that the output is enabled and to prevent noise from causing malfunction in the output may be necessary.
4. Separate power traces and signal traces, such as output and input signals.

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10.2 Layout Example

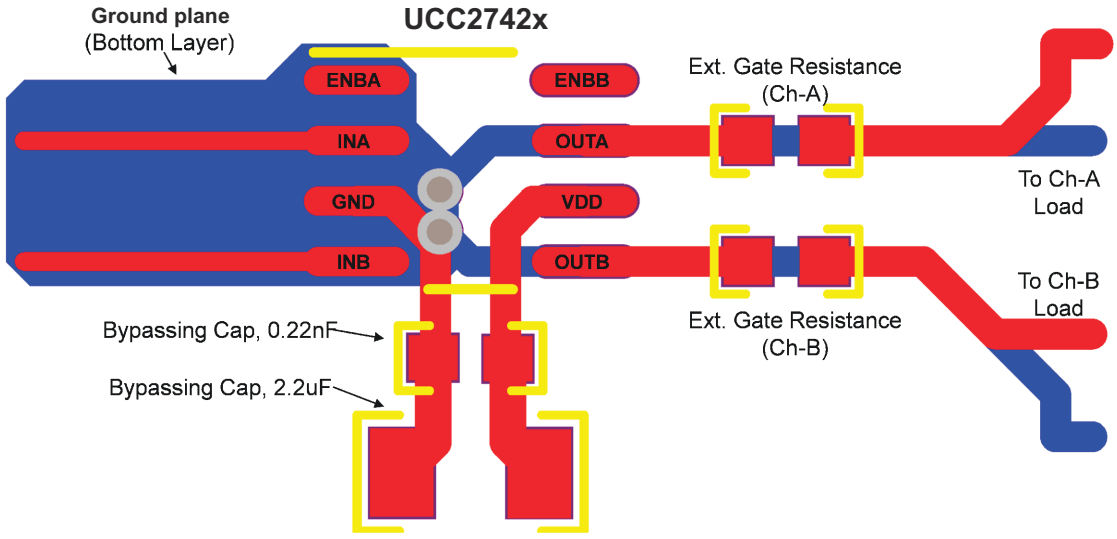

図 10-1. Recommended PCB Layout for UCC2742x

10.3 Thermal Considerations

The useful range of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the IC package. In order for a power driver to be useful over a particular temperature range, the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The UCC2742x family of drivers is available in three different packages to cover a range of application requirements.

As shown in the power dissipation rating table, the SOIC-8 (D) and PDIP-8 (P) packages have a power rating of around 0.5 W with T_A = 70°C. This limit is imposed in conjunction with the power derating factor also given in *セクション 6.6*. Note that the power dissipation in our earlier example is 0.432W with a 10nF load, 12 V_{DD}, switched at 300kHz. Thus, only one load of this size could be driven using the D or P package, even if the two onboard drivers are paralleled. The difficulties with heat removal limit the drive available in the older packages.

The MSOP PowerPAD-8 (DGN) package significantly relieves this concern by offering an effective means of removing the heat from the semiconductor junction. As illustrated in Reference 3 of *セクション 11.2*, the PowerPAD packages offer a leadframe die pad that is exposed at the base of the package. This pad is soldered to the copper on the PC board directly underneath the IC package, reducing the $R_{\theta\ JC(bot)}$ down to 5.9°C/W. Data is presented in Reference 3 of *セクション 11.2* to show that the power dissipation can be quadrupled in the PowerPAD configuration when compared to the standard packages. The PC board must be designed with thermal lands and thermal vias to complete the heat removal subsystem, as summarized in Reference 4 of *セクション 11.2*. This allows a significant improvement in heatsinking over that available in the D or P packages, and is shown to more than double the power capability of the D and P packages. Note that the PowerPAD™ is not directly connected to any leads of the package. However, it is electrically and thermally connected to the substrate which is the ground of the device.

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11 Device and Documentation Support

11.1 Device Support

11.1.1 サード・パーティ製品に関する免責事項

サード・パーティ製品またはサービスに関するテキサス・インスツルメンツの出版物は、単独またはテキサス・インスツルメンツの製品、サービスと一緒に提供される場合に関係なく、サード・パーティ製品またはサービスの適合性に関する是認、サード・パーティ製品またはサービスの是認の表明を意味するものではありません。

11.2 Documentation Support

11.2.1 Related Documentation

- Power Supply Seminar SEM-1400 Topic 2: *Design And Application Guide For High Speed MOSFET Gate Drive Circuits*, by Laszlo Balogh, Texas Instruments (SLUP133).
- Application Note, *Practical Considerations in High Performance MOSFET, IGBT and MCT Gate Drive Circuits*, by Bill Andreycak, Texas Instruments (SLUA105)
- Technical Brief, *PowerPad Thermally Enhanced Package*, Texas Instruments (SLMA002)
- Application Brief, *PowerPAD Made Easy*, Texas Instruments (SLMA004)

11.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

11.4 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

11.5 Trademarks

PowerPAD™ and テキサス・インスツルメンツ E2E™ are trademarks of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

11.6 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

12 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision E (December 2015) to Revision F (November 2023) **Page**

- Changed the ESD ratings value 5
- Changed the input threshold values, remove VOH, VOL in Electrical Characteristics 7
- Updated the position of the waveforms in 図 6-1 8
- Changed Rise Time from ms to ns in 図 6-14 and Fall Time from ms to ns in 図 6-15 9
- Changed 図 6-28 9

Changes from Revision D (May 2013) to Revision E (December 2015) **Page**

- 「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加。 1

Changes from Revision C (July 2011) to Revision D (May 2013) **Page**

- Added *Pin Functions* table note 4
- Added ABSOLUTE MAXIMUM RATINGS note 5
- Added additional ENABLE pin description 14

Changes from Revision B (November 2004) to Revision C (March 2011) **Page**

- 温度定格を変更。 1
- 「オーダー情報」の温度範囲 (3 箇所) 1
- Changed Output current (OUTA, OUTB) DC from 0.3 A to 0.2 A 5
- Changed ELECTRICAL CHARACTERISTICS temperature rating 7
- Changed Low-level output level from 40 mV max to 45 mV max 7

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13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC27423DGN	Obsolete	Production	HVSSOP (DGN) | 8	-	-	Call TI	Call TI	-40 to 105	27423
UCC27423DGNR	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	27423
UCC27423DGNR.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	27423
UCC27423DGNRG4	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	27423
UCC27423DGNRG4.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	27423
UCC27423DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	27423
UCC27423DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	27423
UCC27423P	NRND	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 105	27423
UCC27423P.A	NRND	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 105	27423
UCC27424D	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 105	27424
UCC27424DGNR	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	27424
UCC27424DGNR.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	27424
UCC27424DGNRG4	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	27424
UCC27424DGNRG4.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	27424
UCC27424DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	27424
UCC27424DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	27424
UCC27424DR1G4	NRND	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	27424
UCC27424DR1G4.A	NRND	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	27424
UCC27424P	NRND	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 105	27424
UCC27424P.A	NRND	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 105	27424
UCC27425D	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 105	27425
UCC27425DGN	Obsolete	Production	HVSSOP (DGN) | 8	-	-	Call TI	Call TI	-40 to 105	27425
UCC27425DGNR	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	27425
UCC27425DGNR.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	27425
UCC27425DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	-40 to 105	27425
UCC27425DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	-40 to 105	27425
UCC27425P	NRND	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 105	27425
UCC27425P.A	NRND	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 105	27425
UCC27425PE4	NRND	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 105	27425

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF UCC27423, UCC27424, UCC27425 :

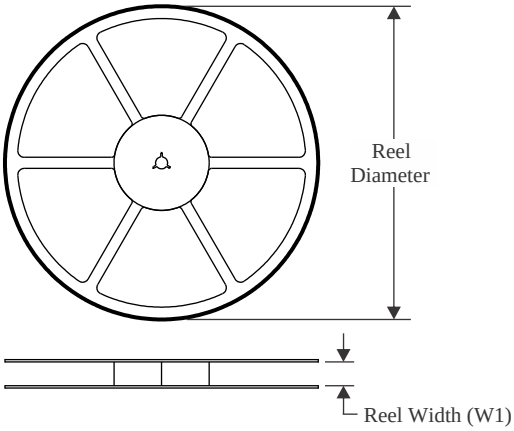
- Automotive : UCC27423-Q1, UCC27424-Q1, UCC27425-Q1
- Enhanced Product : UCC27423-EP, UCC27424-EP

NOTE: Qualified Version Definitions:

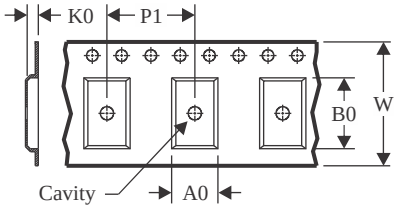
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

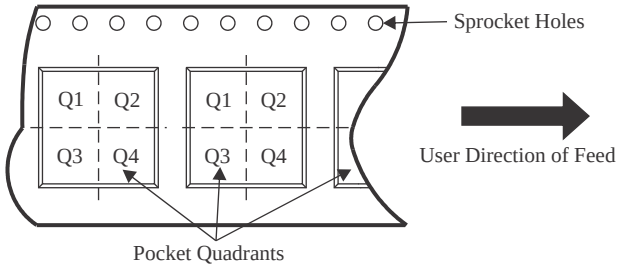


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

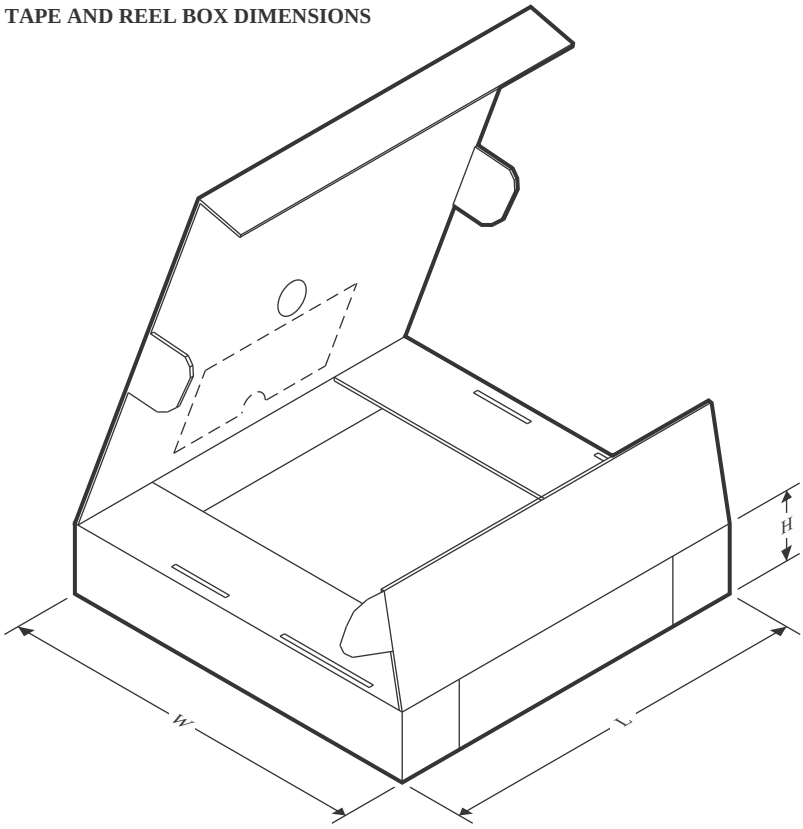
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27423DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC27423DGNRG4	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC27423DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC27423DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC27424DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC27424DGNRG4	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC27424DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC27424DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC27424DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC27424DR1G4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC27425DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC27425DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

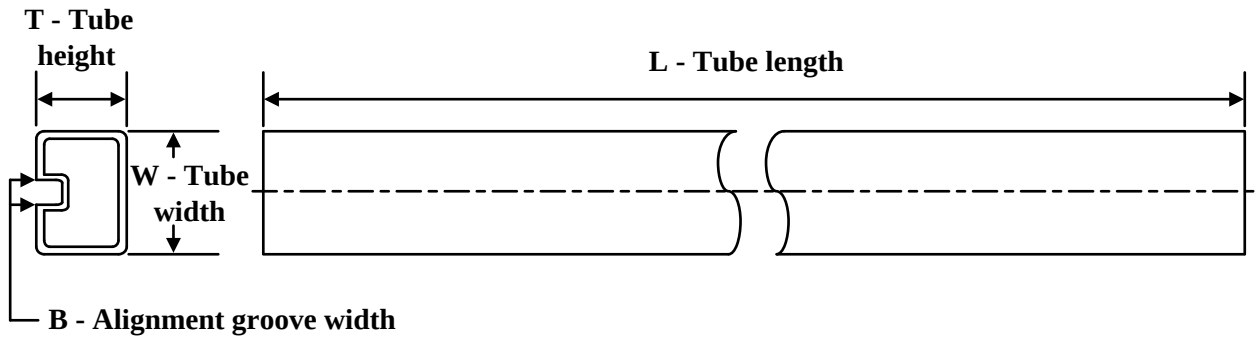
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27423DGNR	HVSSOP	DGN	8	2500	353.0	353.0	32.0
UCC27423DGNRG4	HVSSOP	DGN	8	2500	353.0	353.0	32.0
UCC27423DR	SOIC	D	8	2500	353.0	353.0	32.0
UCC27423DR	SOIC	D	8	2500	353.0	353.0	32.0
UCC27424DGNR	HVSSOP	DGN	8	2500	353.0	353.0	32.0
UCC27424DGNRG4	HVSSOP	DGN	8	2500	353.0	353.0	32.0
UCC27424DR	SOIC	D	8	2500	353.0	353.0	32.0
UCC27424DR	SOIC	D	8	2500	353.0	353.0	32.0
UCC27424DR	SOIC	D	8	2500	353.0	353.0	32.0
UCC27424DR1G4	SOIC	D	8	2500	353.0	353.0	32.0
UCC27425DGNR	HVSSOP	DGN	8	2500	353.0	353.0	32.0
UCC27425DR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UCC27423P	P	PDIP	8	50	506	13.97	11230	4.32
UCC27423P.A	P	PDIP	8	50	506	13.97	11230	4.32
UCC27424P	P	PDIP	8	50	506	13.97	11230	4.32
UCC27424P.A	P	PDIP	8	50	506	13.97	11230	4.32
UCC27425P	P	PDIP	8	50	506	13.97	11230	4.32
UCC27425P.A	P	PDIP	8	50	506	13.97	11230	4.32
UCC27425PE4	P	PDIP	8	50	506	13.97	11230	4.32

GENERIC PACKAGE VIEW

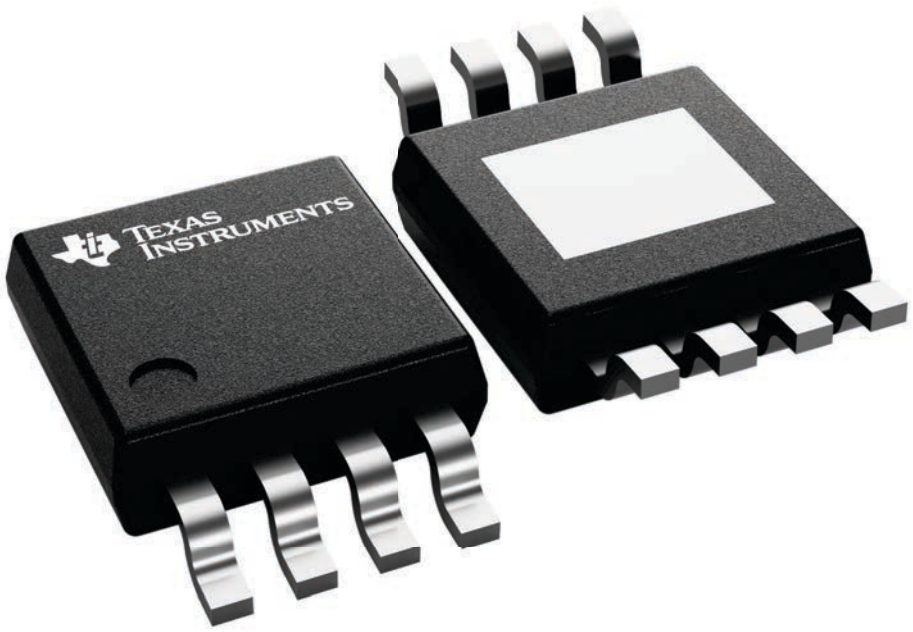
DGN 8

PowerPAD™ HVSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

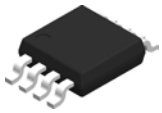
SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



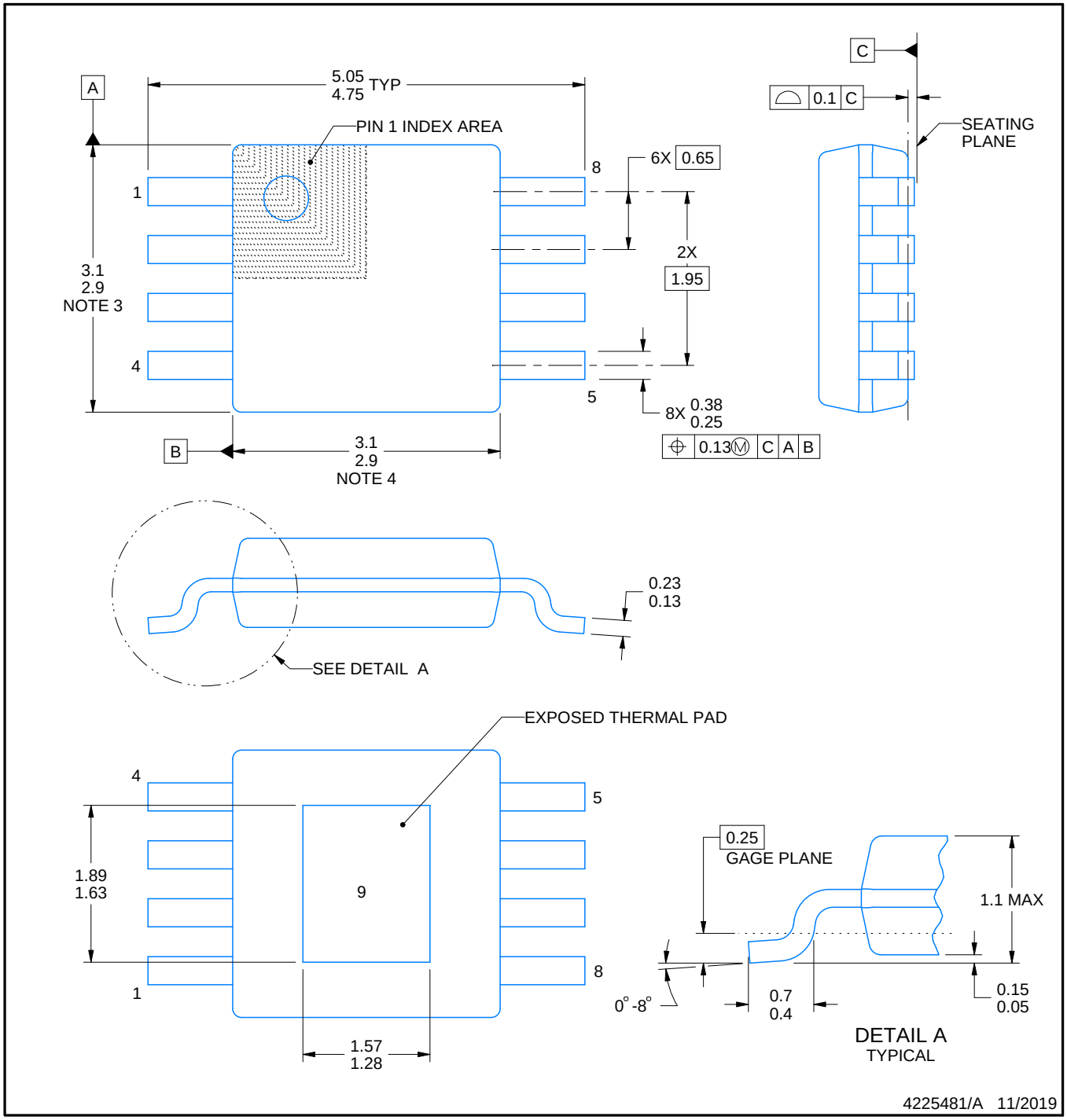
PACKAGE OUTLINE

DGN0008D



PowerPAD™ VSSOP - 1.1 mm max height

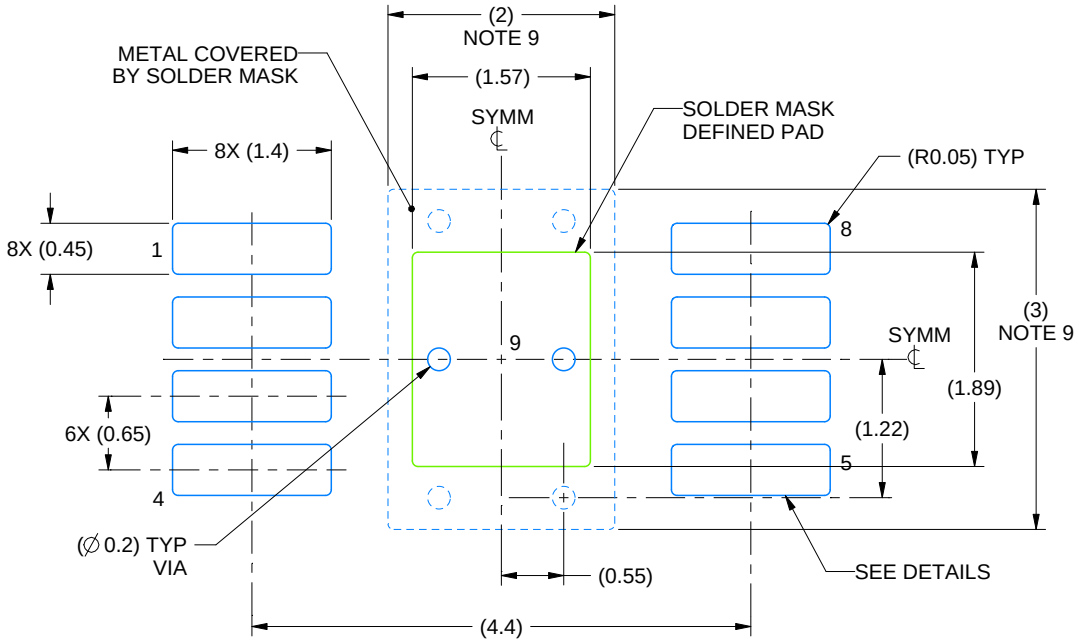
SMALL OUTLINE PACKAGE



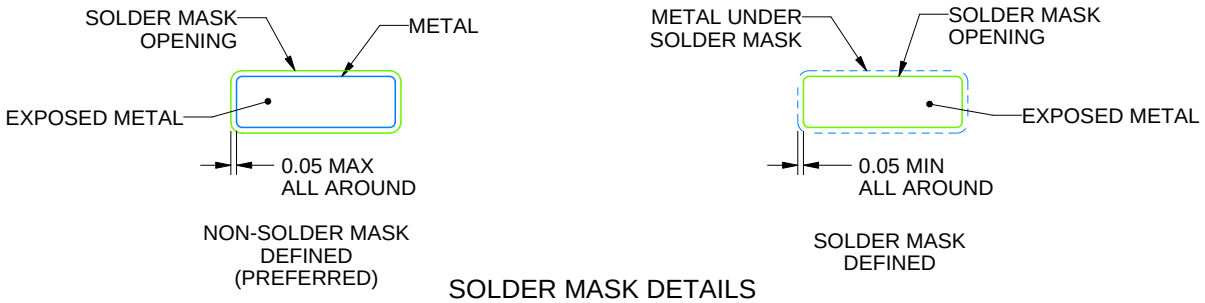
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

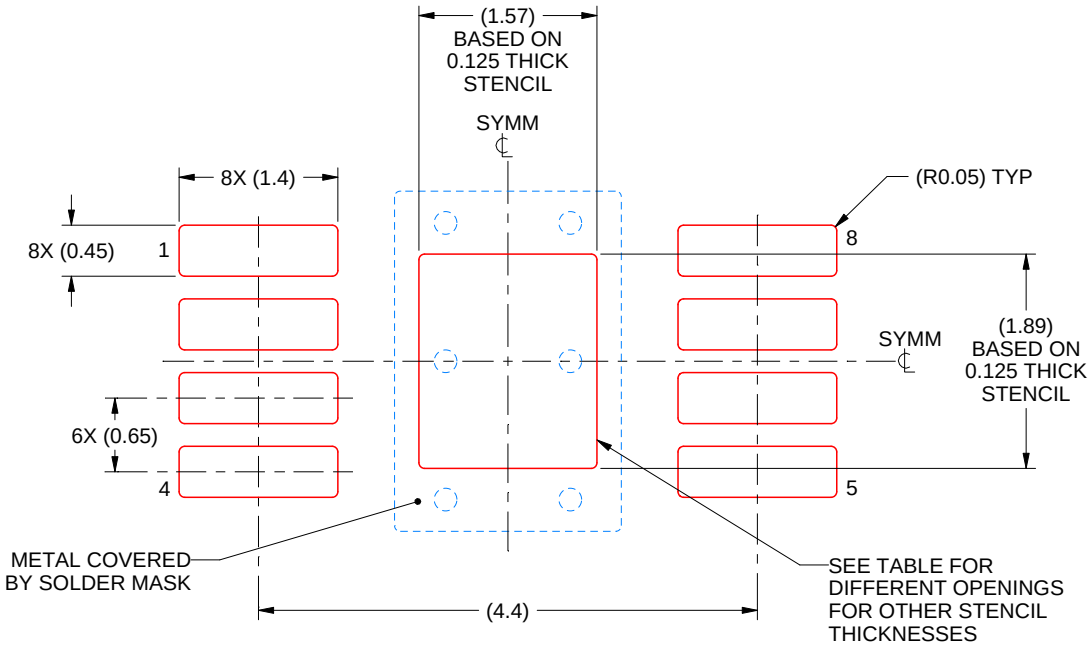


SOLDER MASK DETAILS

4225481/A 11/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

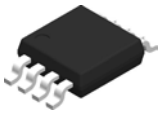
4225481/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

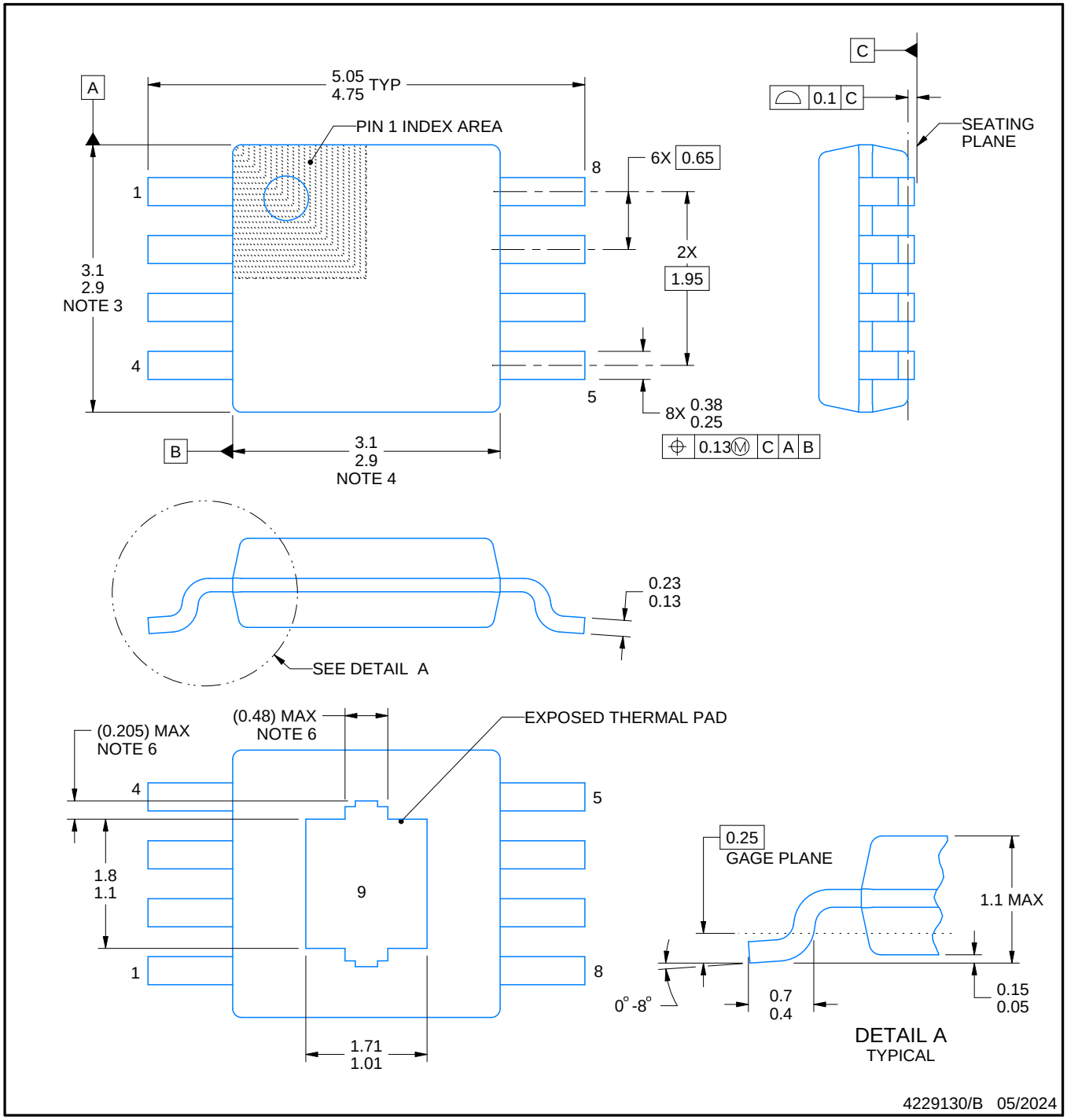
PACKAGE OUTLINE

DGN0008H



PowerPAD™ VSSOP - 1.1 mm max height

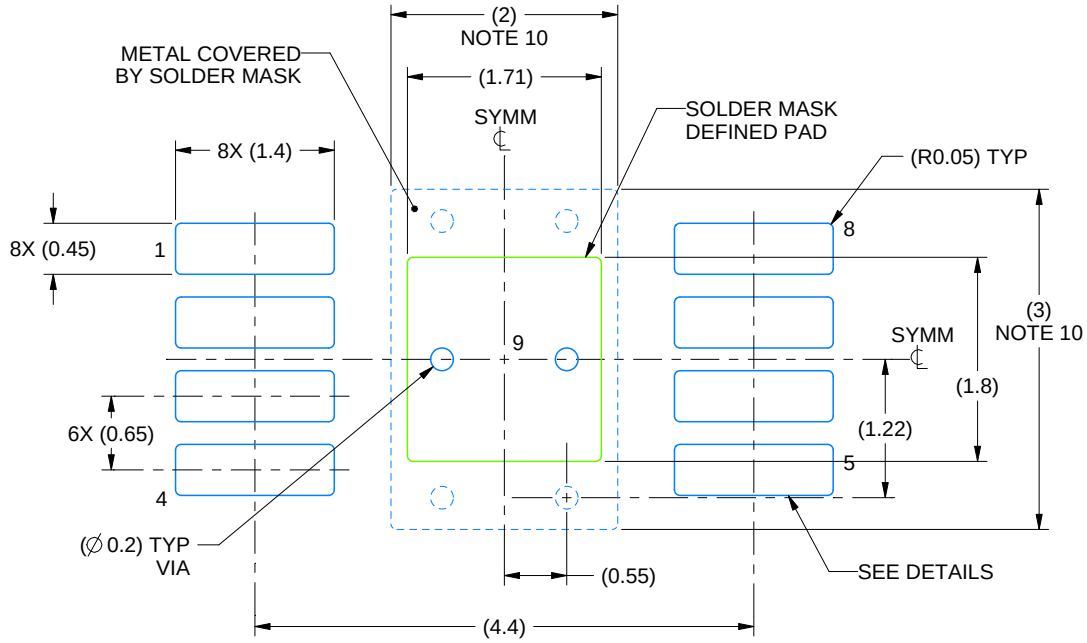
SMALL OUTLINE PACKAGE



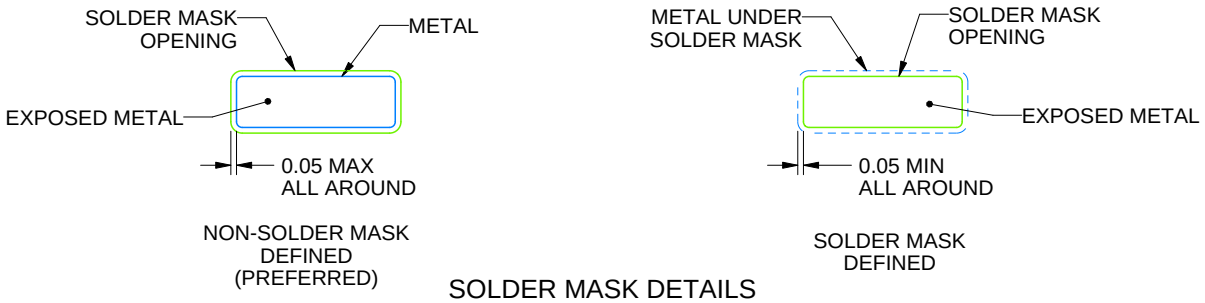
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.
6. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

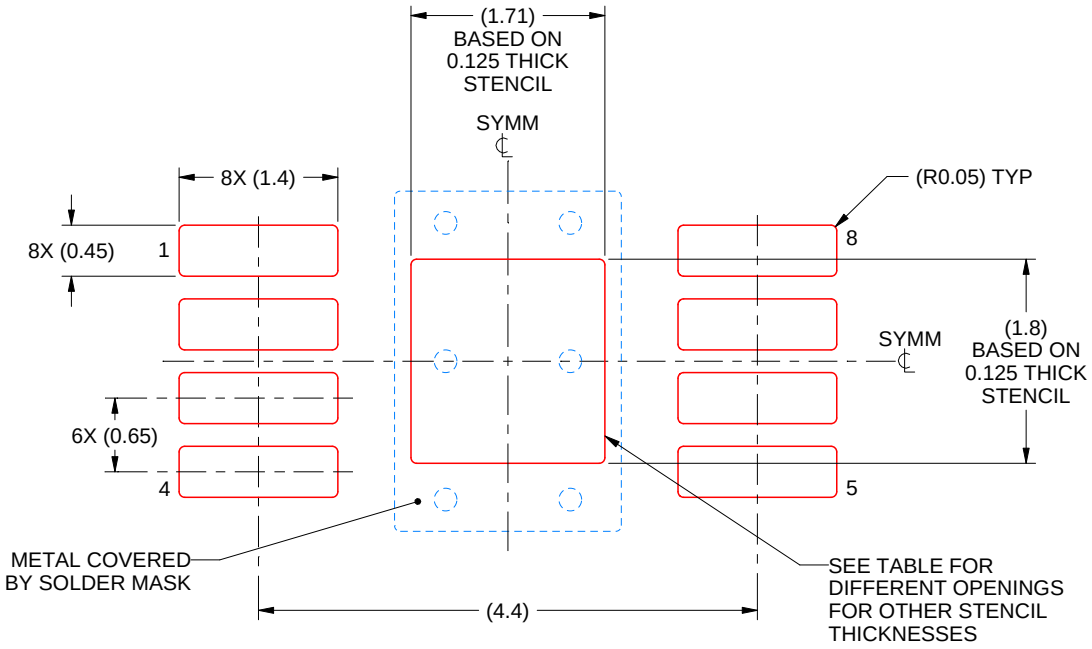


SOLDER MASK DETAILS

4229130/B 05/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
9. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.91 X 2.01
0.125	1.71 X 1.80 (SHOWN)
0.15	1.56 X 1.64
0.175	1.45 X 1.52

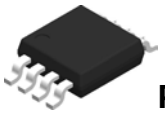
4229130/B 05/2024

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

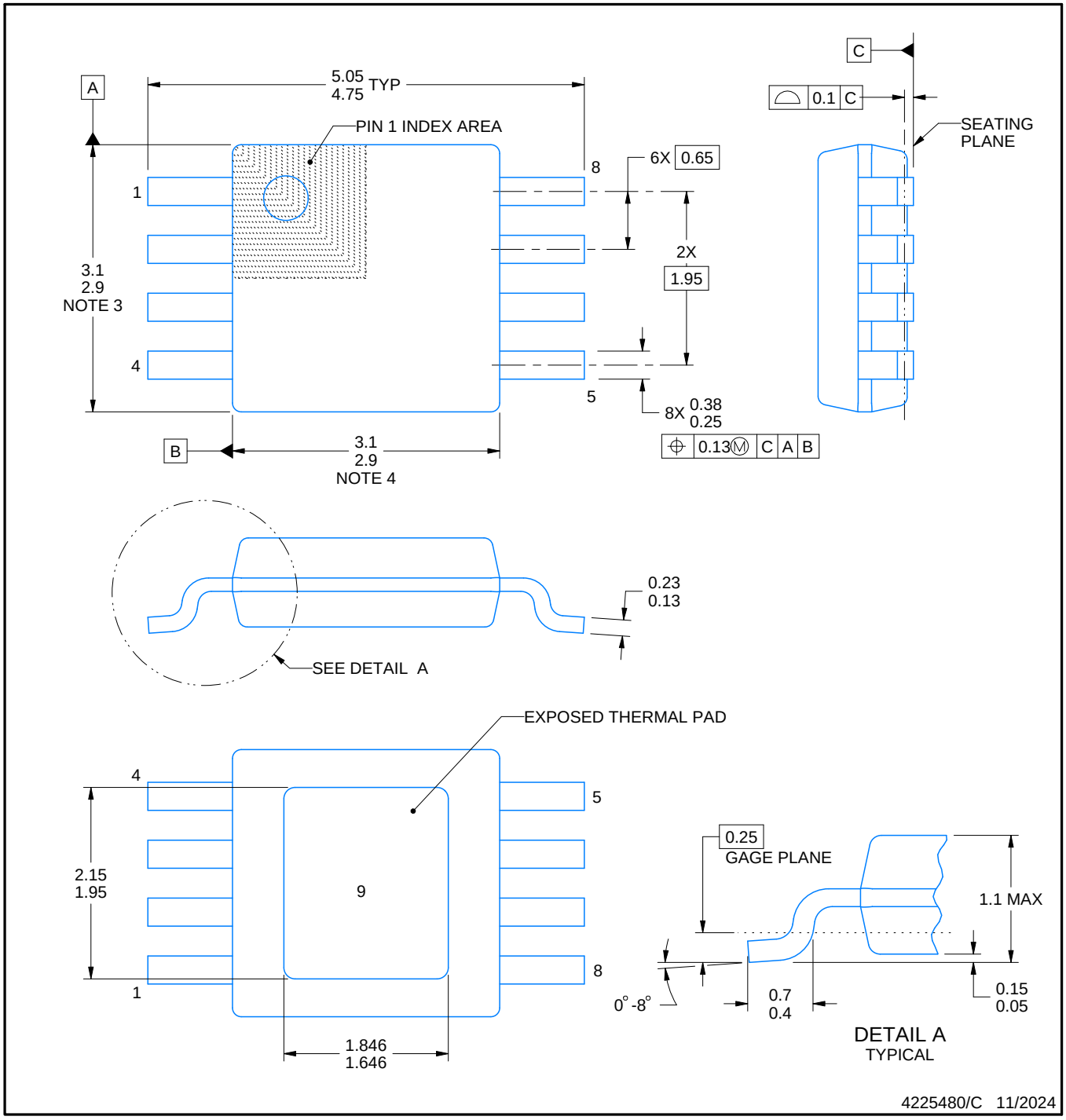
PACKAGE OUTLINE

DGN0008G



PowerPAD™ HVSSOP - 1.1 mm max height

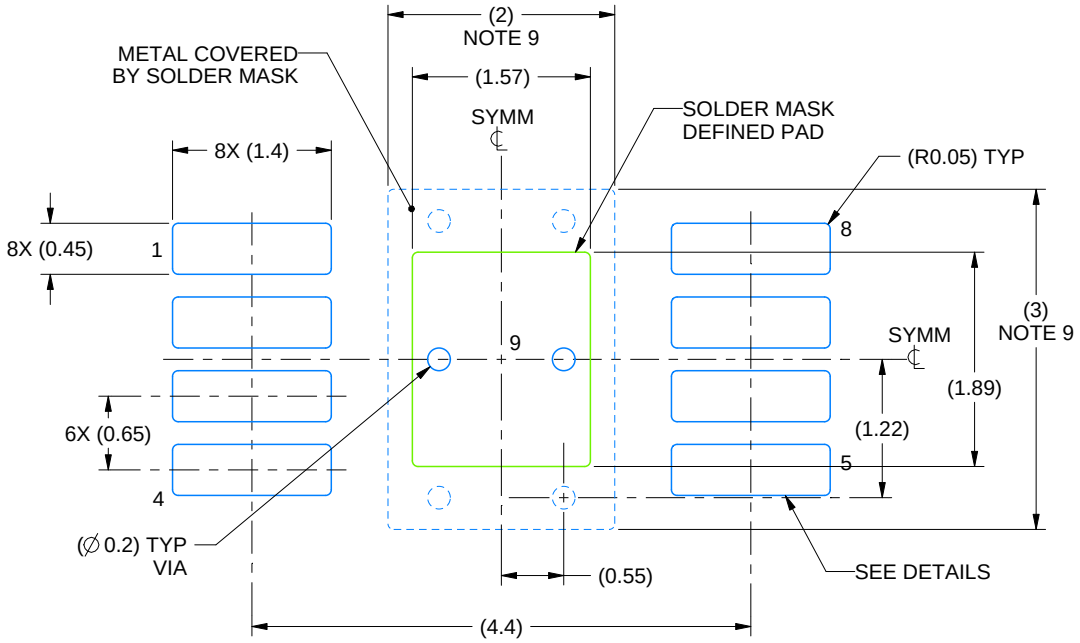
SMALL OUTLINE PACKAGE



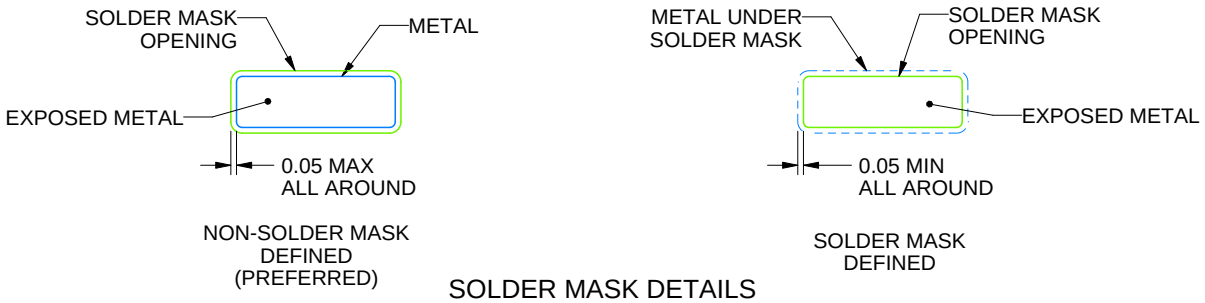
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

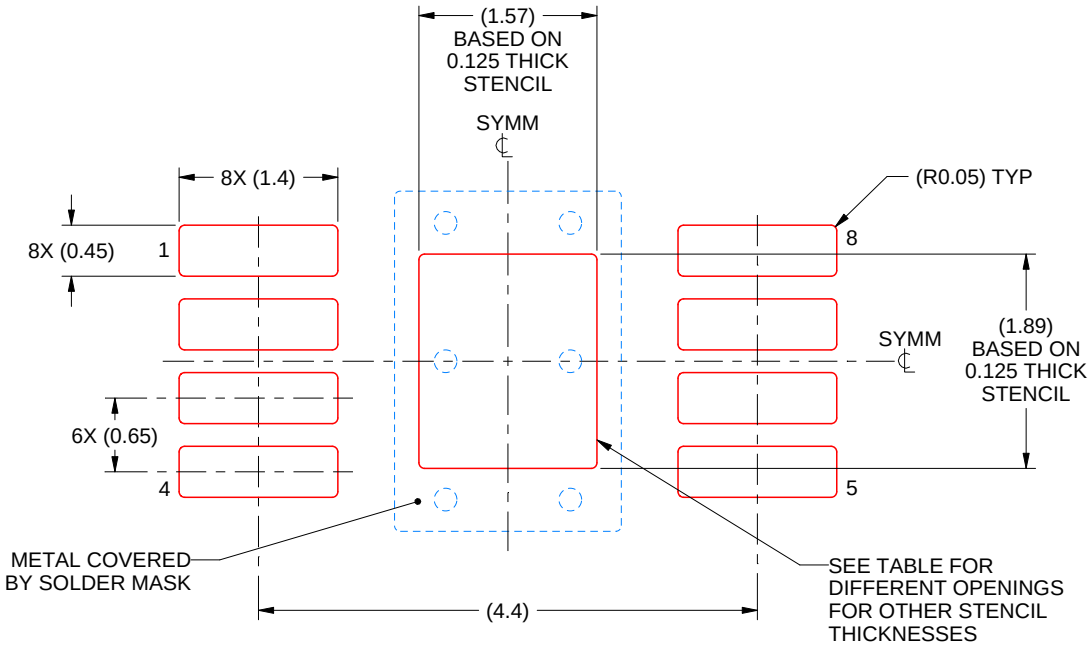


SOLDER MASK DETAILS

4225480/C 11/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



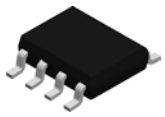
SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225480/C 11/2024

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

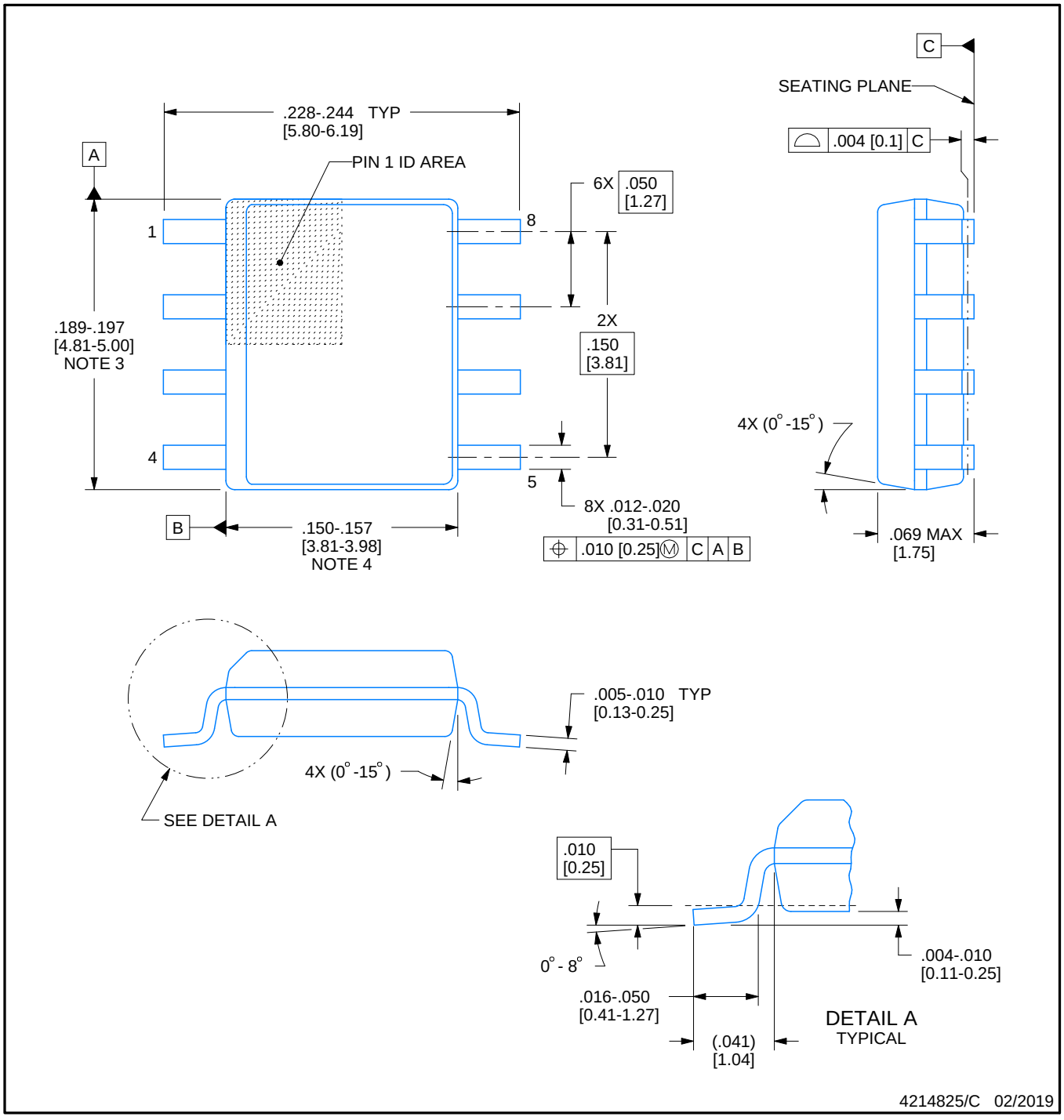


PACKAGE OUTLINE

D0008A

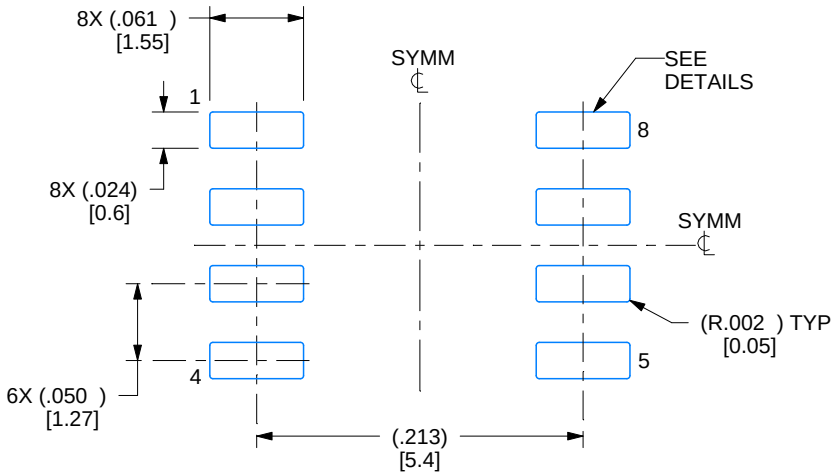
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

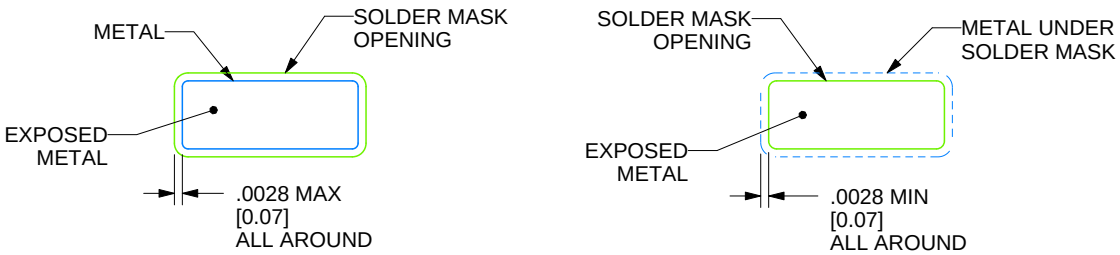


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

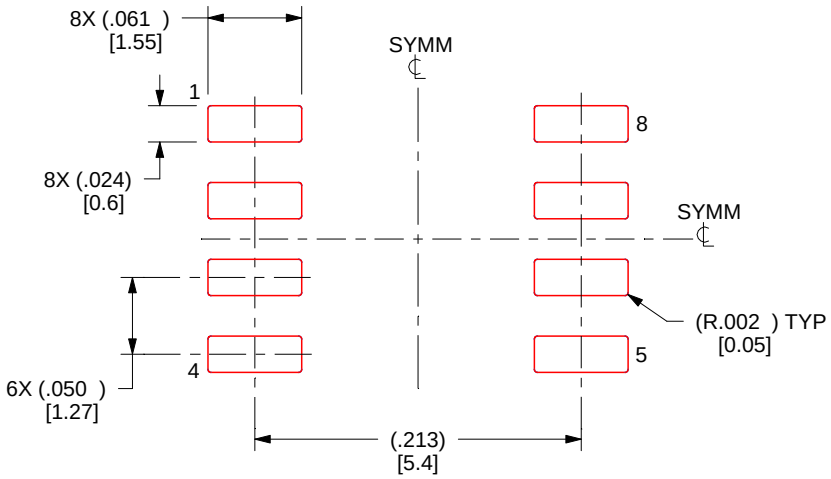
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



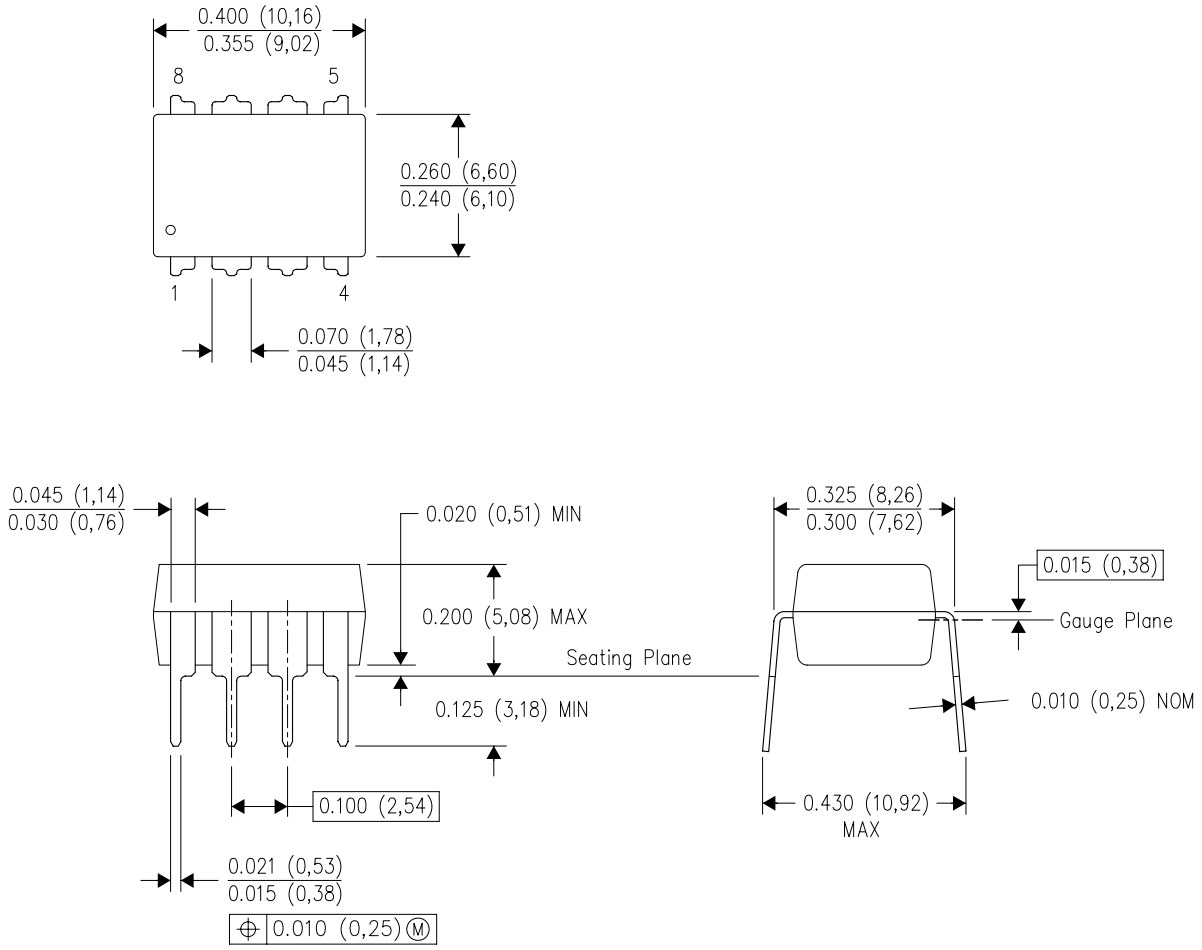
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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