TEXAS INSTRUMENTS
UCC27444-Q1
JAJSNS2A – MAY 2022 – REVISED JULY 2023

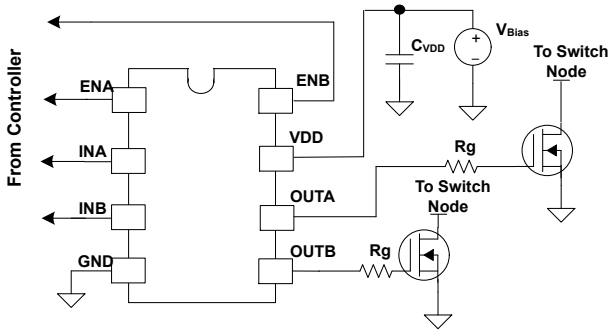
UCC27444-Q1 20V、4A デュアルチャネル、ローサイド・ゲート・ドライバ、-5V 入力機能付き、車載用アプリケーション向け

1 特長

- 車載アプリケーション向けに認定済み
- 以下の結果で AEC-Q100 認定済み:
  - デバイス温度グレード 1:-40℃～+125℃の動作時周囲温度範囲
  - デバイス HBM ESD 分類レベル H2
  - デバイス CDM ESD 分類レベル C6
- 各チャネルの 4A (代表値) ピーク・ソースおよびシンク駆動電流
- -5V まで扱える INA および INB 入力ピン
- 絶対最大 VDD 電圧:20V
- 広い VDD 動作範囲:4.5V～18V
- 2 つの独立したゲート駆動チャネル
- 出力ごとに独立したイネーブル機能
- 高速伝搬遅延時間:18ns (代表値)
- 高速立ち上がり / 立ち下がり時間:11ns/7ns (代表値)
- 2 チャネル間遅延マッチング:1ns (代表値)
- SOIC8 および VSSOP8 PowerPAD™ パッケージ・オプション
- 動作時の接合部温度範囲:-40℃～125℃

2 アプリケーション

- スイッチ・モード電源 (SMPS)
- 力率改善 (PFC) 回路
- DC/DC コンバータ
- AC インバータと VF ドライブ
- マイクロ・インバータ
- DC 高速充電ステーション



アプリケーション概略図

3 概要

UCC27444-Q1 は、MOSFET および GaN パワー・スイッチを効率的に駆動するデュアルチャネル高速ローサイド・ゲート・ドライバです。UCC27444-Q1 は 4A (代表値) のピーク駆動能力を持っています。これにより、パワー・スイッチの立ち上がり / 立ち下がり時間を短縮し、スイッチング損失を低減し、効率を向上させます。本デバイスの高速伝搬遅延 (代表値 18ns) は、システムのデッドタイム最適化、パルス幅利用率、制御ループ応答、過渡性能を改善させることで出力段の効率を向上させます。

UCC27444-Q1 は、INx 入力で -5V を扱えるため、中程度のグランド・バウンスが発生するシステムの堅牢性を向上させることができます。入力をほとんどのコントローラ出力に接続できるため、制御の柔軟性を最大限に高めることができます。独立したイネーブル信号を使うと、メイン制御ロジックとは無関係に電力段を制御できます。システム障害が発生した場合、イネーブル・ローにすることで、ゲート・ドライバを迅速にシャットオフできます。多くの高周波スイッチング電源では、電源デバイスのゲートにノイズを生じさせます。このノイズがゲート・ドライバの出力ピンに注入され、ドライバを誤動作させる可能性があります。本デバイスは、過渡逆電流と逆電圧への対応能力があるため、電源デバイスやパルス変圧器のゲートのノイズが許容され、ドライバの誤動作を防止できます。

UCC27444-Q1 は、低電圧動作とパワーオン・リセット (POR) 機能も搭載しており、システムの堅牢性が向上します。パワー・デバイスの動作に十分なバイアス電圧がない場合は、強力な内部プルダウン MOSFET によってゲート・ドライバの出力が LOW に保持されます。

製品情報

部品番号(1)	パッケージ	本体サイズ (公称)
UCC27444-Q1	SOIC (8)	4.90mm × 3.91mm
	VSSOP (8)	3.00mm × 3.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (May 2022) to Revision A (July 2023)	Page
• ステータスを「事前情報」から「量産データ」に変更	1

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5 Pin Configuration and Functions

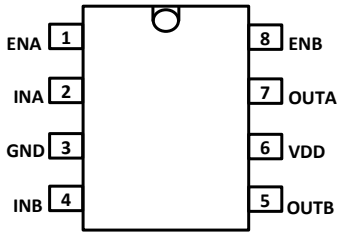


図 5-1. D Package 8-Pin SOIC Top View

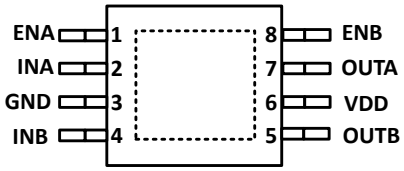


図 5-2. DGN Package 8-Pin VSSOP Top View

表 5-1. Pin Functions

PIN			TYPE(1)	DESCRIPTION
NAME	DGN	D		
ENA	1	1	I	Enable input for Channel A. Biasing ENA, LOW will disable Channel A output regardless of the state of INA. Pulling ENA, HIGH enables the Channel A output. If ENA is left floating, Channel A is enabled by default due to an internal pullup resistor. It is recommended to connect this pin to VDD if unused.
ENB	8	8	I	Enable input for Channel B. Biasing ENB, LOW disables Channel B output regardless of the state of INB. Pulling ENB, HIGH enables the Channel B output. If ENB is left floating, Channel B is enabled by default due to an internal pullup resistor. It is recommended to connect this pin to VDD if unused.
GND	3	3	—	Ground: All signals are referenced to this pin.
INA	2	2	I	Input to Channel A. INA is the non-inverting input of the UCC27444-Q1 device. Connect this pin to GND if unused.
INB	4	4	I	Input to Channel B. INB is the non-inverting input of the UCC27444-Q1 device. Connect this pin to GND if unused.
OUTA	7	7	O	Channel A Output
OUTB	5	5	O	Channel B Output
VDD	6	6	I	Bias supply input. Bypass this pin with two ceramic capacitors, generally ≥ 1 µF and 0.1 µF, which are referenced to GND pin of this device.
	Thermal Pad	—	—	Connect to GND through large copper plane. This pad is not a low-impedance path to GND.

(1) I = Input; O = Output

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2) (3)

		MIN	MAX	UNIT
Supply voltage, VDD		–0.3	20	V
Output Voltage, OUTA, OUTB	DC	–0.3	VDD +0.3	V
	100ns Pulse	–2	VDD +0.3	V
Input Voltage INA, INB,		–5	VDD+0.3	V
Input Voltage ENA, ENB		-0.3	VDD+0.3	V
Operating junction temperature, T_J		–40	150	°C
Lead temperature	Soldering, 10 sec.		300	°C
	Reflow		260	
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages are with respect to GND unless otherwise noted. Currents are positive into, negative out of the specified terminal. See セクション 6.4 of the datasheet for thermal limitations and considerations of packages.
(3) These devices are sensitive to electrostatic discharge; follow proper device handling procedures.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1) HBM ESD classification level H2	±2000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD classification level C6	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range. All voltages are with reference to GND (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage, VDD	4.5	12	18	V
Input voltage, INA, INB	–2		VDD	V
Output Voltage, OUTA, OUTB	0		VDD	V
Operating junction temperature, T_J	–40		125	°C

6.4 Thermal Information

THERMAL METRIC		UCC27444-Q1		UNIT
		DGN	D	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	57.3	131.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	82.0	73.4	
$R_{\theta JB}$	Junction-to-board thermal resistance	30.5	74.6	
ψ_{JT}	Junction-to-top characterization parameter	5.0	25.6	
ψ_{JB}	Junction-to-board characterization parameter	30.4	73.8	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	13.1	n/a	

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6.5 Electrical Characteristics

Unless otherwise noted, VDD = 4.5 V to 18 V, $T_A = T_J$ = –40°C to 125°C, 1-µF capacitor from VDD to GND, no load on the output. Typical condition specifications are at 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BIAS CURRENTS						
I_{VDD}	VDD static supply current	V_{INx} = 3.3 V, ENx = VDD		150	380	uA
I_{VDD}	VDD static supply current	V_{INx} = 0 V, ENx = VDD		107	180	uA
I_{VDDO}	VDD operating current	C_{LOAD} = 1.8 nF, f_{SW} = 1000 kHz, ENx = VDD, V_{INx} = 0 V – 3.3 V PWM		39	45	mA
I_{DIS}	VDD disable current	V_{INx} = 3.3 V, ENx = 0 V		450	570	uA
POWER ON RESET (POR)						
V_{VDD_ON}	VDD POR rising threshold		2.1	3.0	4.0	V
V_{VDD_OFF}	VDD POR falling threshold		1.8	2.7	3.5	V
V_{VDD_HYS}	VDD POR hysteresis			0.3		V
INPUT (INA, INB)						
V_{INx_H}	Input signal high threshold	Output High, ENx = HIGH	1.6	2.2	2.5	V
V_{INx_L}	Input signal low threshold	Output Low, ENx = HIGH	0.8	1.2	1.5	V
V_{INx_HYS}	Input signal hysteresis			1		V
ENABLE (ENA, ENB)						
V_{ENx_H}	Enable signal high threshold	Output High, INx = HIGH	1.7	2.3	2.7	V
V_{ENx_L}	Enable signal low threshold	Output Low, INx = HIGH	1.1	1.8	2.2	V
V_{ENx_HYS}	Enable signal hysteresis			0.7		V
R_{ENx}	EN pin pullup resistance	ENx = 0 V		100		kΩ
OUTPUTS (OUTA, OUTB)						
I_{SRC} (1)	Peak output source current	VDD = 14 V, C_{VDD} = 10 µF, C_L = 0.1 µF, f = 1 kHz		4		A
I_{SNK} (1)	Peak output sink current	VDD = 14 V, C_{VDD} = 10 µF, C_L = 0.1 µF, f = 1 kHz		–4		A
R_{OH} (2)	Pullup resistance	I_{OUT} = –10 mA See セクション 7.3.4.		1.2	2.5	Ω
R_{OL}	Pulldown resistance	I_{OUT} = 10 mA		0.7	1.2	Ω

(1) Parameter not tested in production.
(2) Output pullup resistance in this table is a DC measurement that measures resistance of PMOS structure only (not N-channel structure).

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6.6 Switching Characteristics

Unless otherwise noted, VDD = V_{EN} = 4.5 V to 18 V, T_A = T_J = –40°C to 125°C, 1-µF capacitor from VDD to GND, no load on the output. Typical condition specifications are at 25°C (1).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{Rx}	Rise time	C_{LOAD} = 1.8 nF, 10% to 90%, Vin = 0 V – 5 V		11	25	ns
t_{Fx}	Fall time	C_{LOAD} = 1.8 nF, 90% to 10%, Vin = 0 V – 5V		7	23	ns
t_{D1x}	Turn-on propagation delay	C_{LOAD} = 1.8 nF, V_{INx_H} of the input rise to 10% of output rise, Vin = 0 V –5 V, Fsw = 500 kHz, 50% duty cycle		18	33	ns
t_{D2x}	Turn-off propagation delay	C_{LOAD} = 1.8 nF, V_{INx_L} of the input fall to 90% of output fall, Vin = 0 V – 5 V, VDD= 5V -18V, Fsw = 500 kHz, 50% duty cycle		30	50	ns
t_{D3x}	Enable propagation delay	C_{LOAD} = 1.8 nF, V_{ENx_H} of the enable rise to 10% of output rise, Vin = 0 V – 5 V, Fsw = 500 kHz, 50% duty cycle		19	31	ns
t_{D4x}	Disable propagation delay	C_{LOAD} = 1.8 nF, V_{ENx_L} of the enable fall to 90% of output fall, Vin = 0 V – 5 V, Fsw = 500 kHz, 50% duty cycle		24	52	ns
t_M	Delay matching between two channels	C_{LOAD} = 1.8 nF, Vin = 0 V – 5 V, Fsw = 500 kHz, 50% duty cycle, INA = INB, $\lvert t_{RA} - t_{RB} \rvert$, $\lvert t_{FA} - t_{FB} \rvert$		1	5	ns
t_{PWmin}	Minimum input pulse width	C_L = 1.8 nF, Vin = 0 V – 5 V, Fsw = 500 kHz, Vo > 1.5 V		8	22	ns

(1) Switching parameters are not tested in production.

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6.7 Timing Diagrams

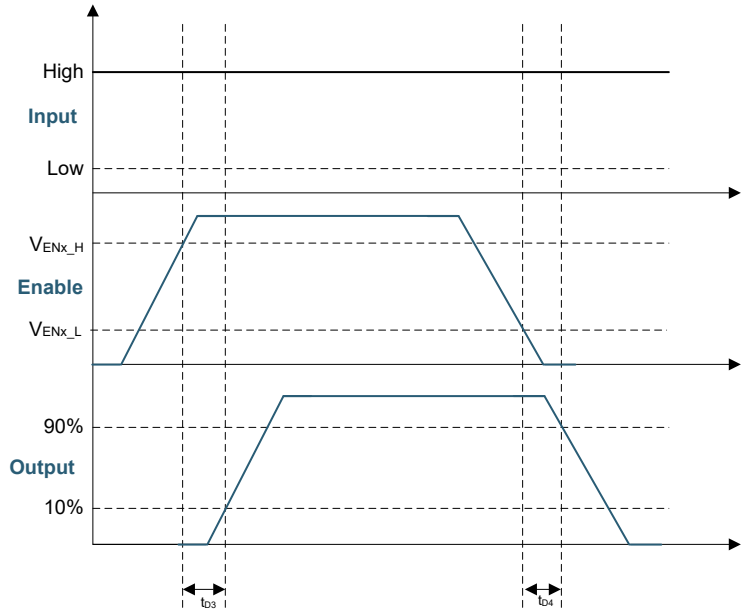


図 6-1. Enable Function

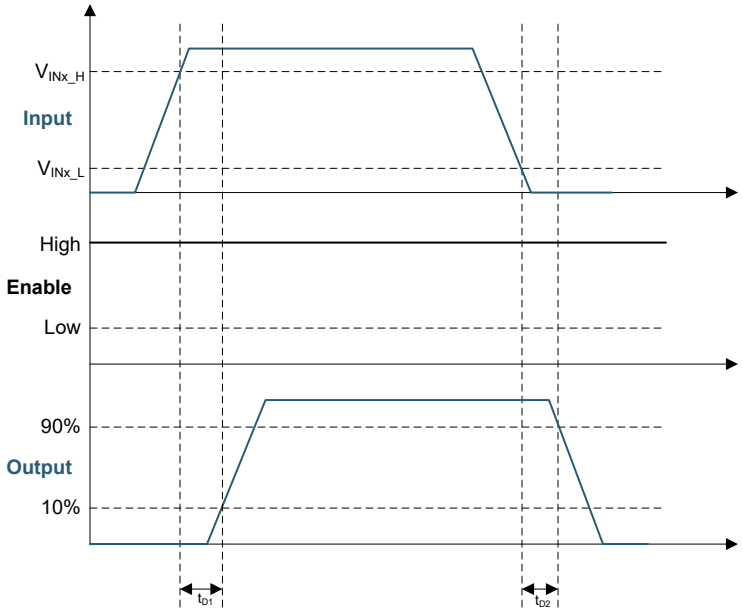


図 6-2. Input-Output Operation

6.8 Typical Characteristics

Unless otherwise specified, VDD = 12 V, INx = 3.3 V, ENx = 3.3 V, T_J = 25°C, no load

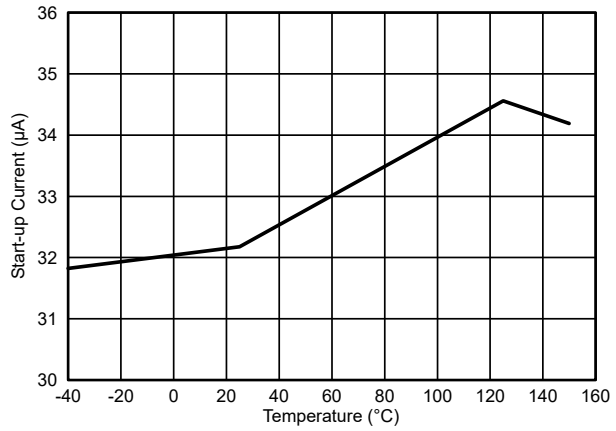


図 6-3. Start-Up and Quiescent Current

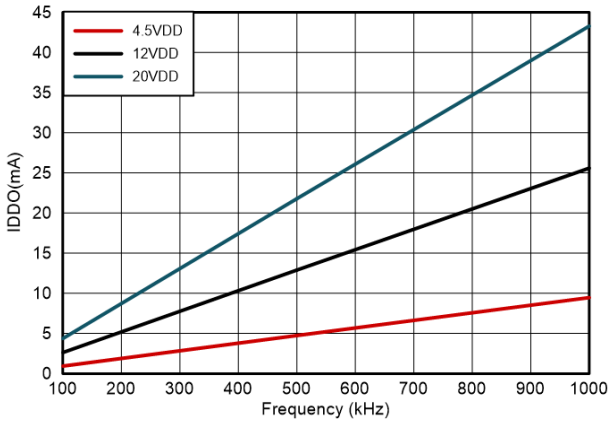


図 6-4. Operating Supply Current (both outputs switching)

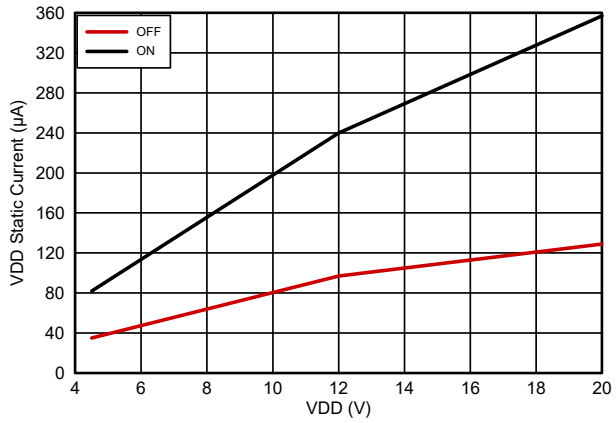


図 6-5. Static Supply Current (outputs in DC on or off condition)

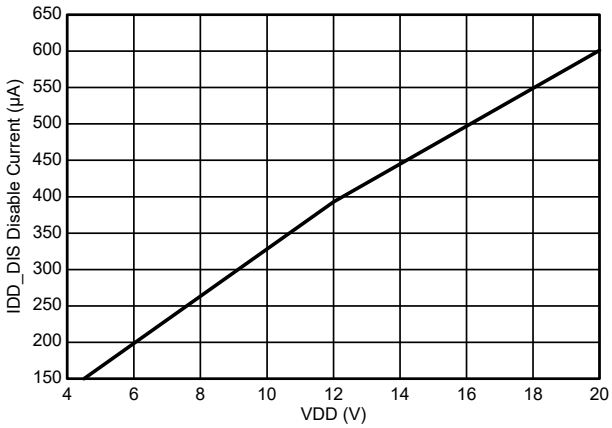


図 6-6. Disable Current (EN = 0 V)

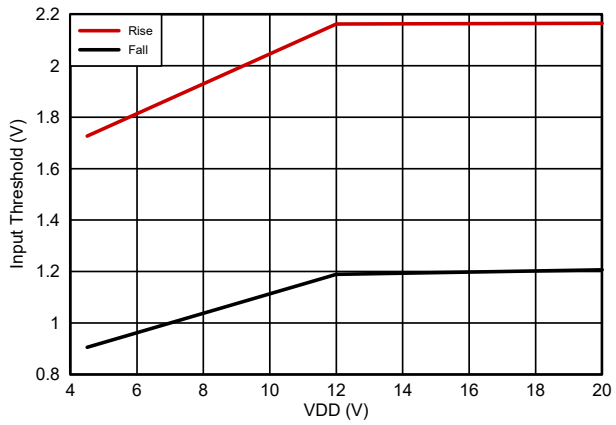


図 6-7. Input Thresholds

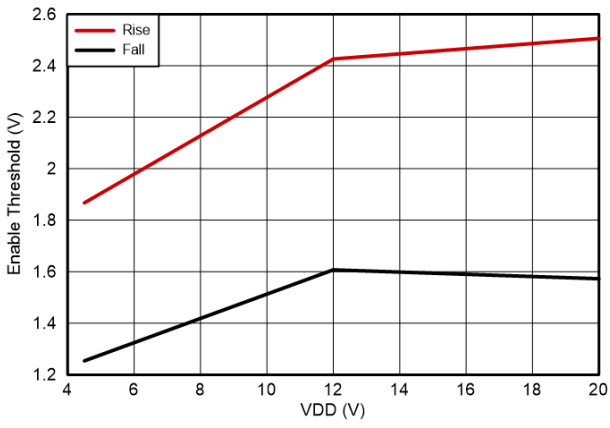


図 6-8. Enable Threshold

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6.8 Typical Characteristics (continued)

Unless otherwise specified, VDD = 12 V, INx = 3.3 V, ENx = 3.3 V, T_J = 25°C, no load

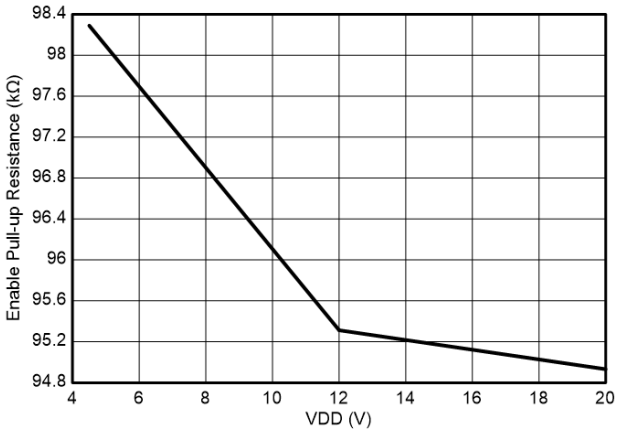


図 6-9. Enable Pullup Resistance

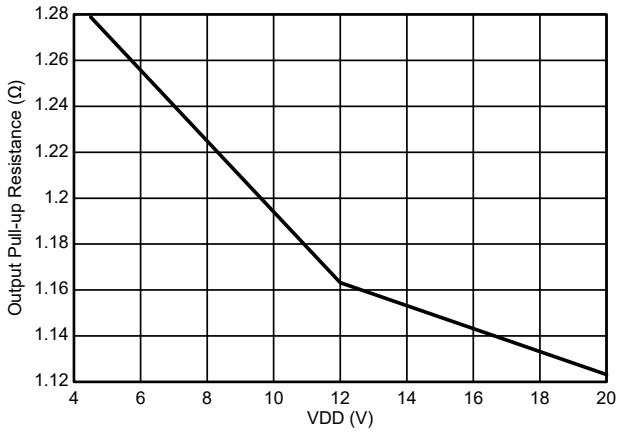


図 6-10. Output Pullup Resistance

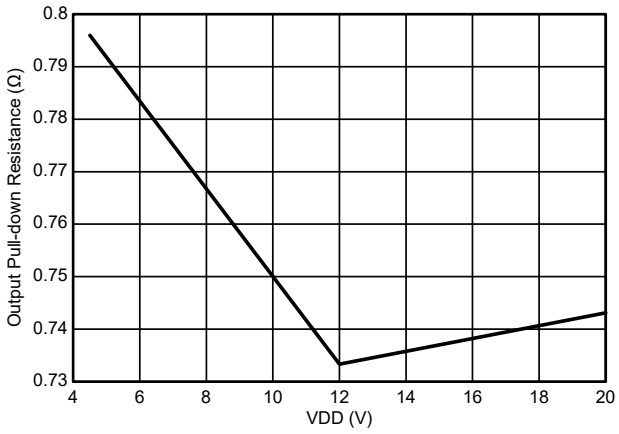
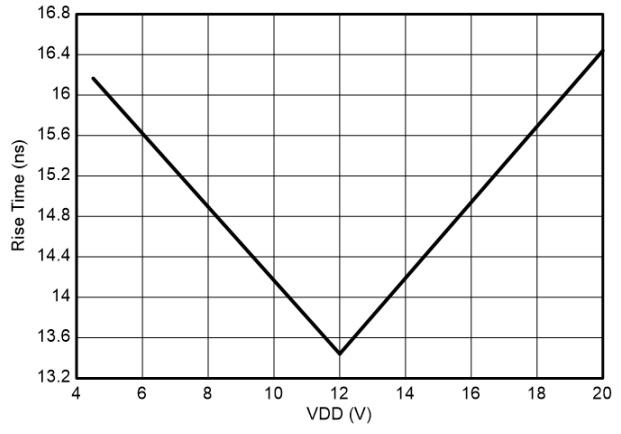
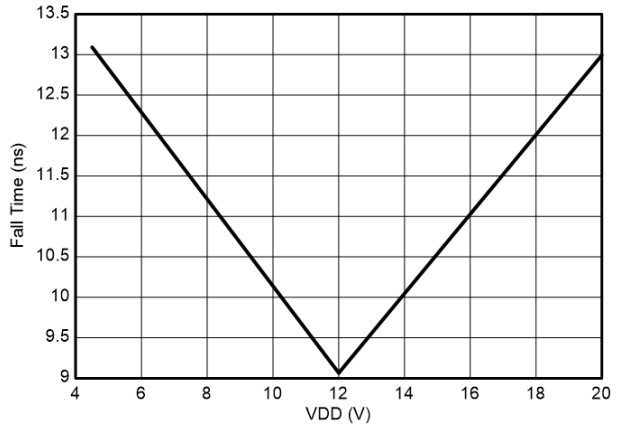


図 6-11. Output Pulldown Resistance



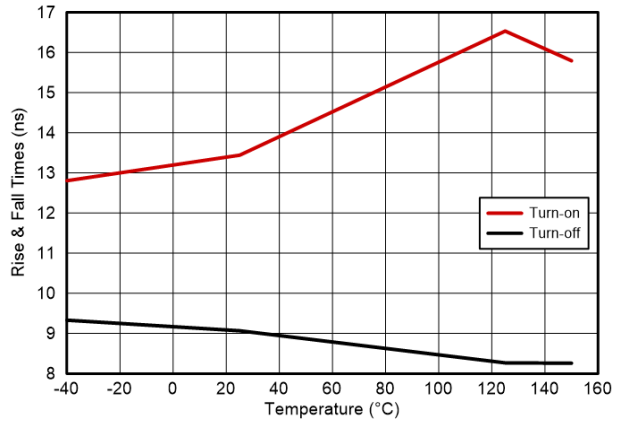
C_{LOAD} = 1.8 nF

図 6-12. Output Rise Time vs VDD



C_{LOAD} = 1.8 nF

図 6-13. Output Fall Time vs VDD

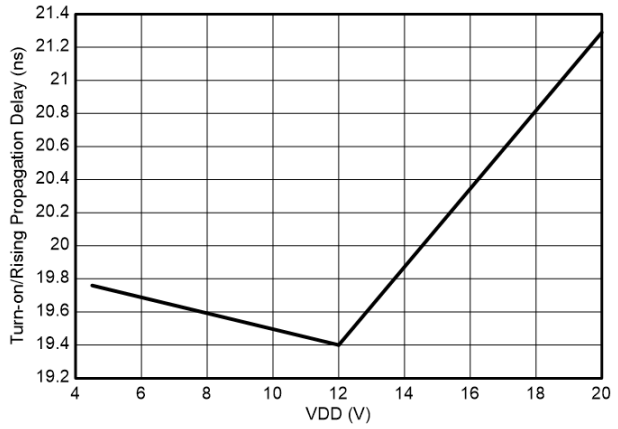


C_{LOAD} = 1.8 nF

図 6-14. Output Rise and Fall Time vs Temperature

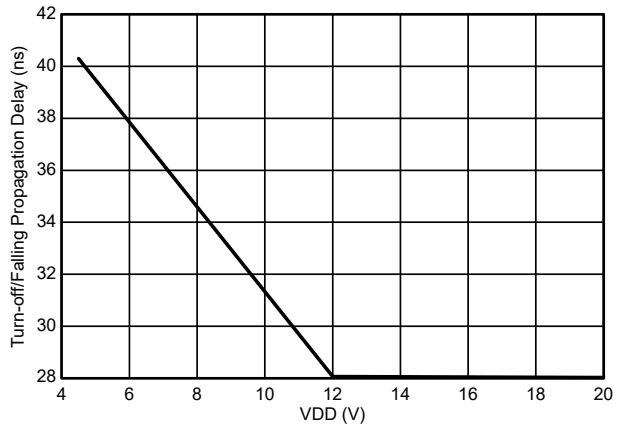
6.8 Typical Characteristics (continued)

Unless otherwise specified, VDD = 12 V, INx = 3.3 V, ENx = 3.3 V, T_J = 25°C, no load



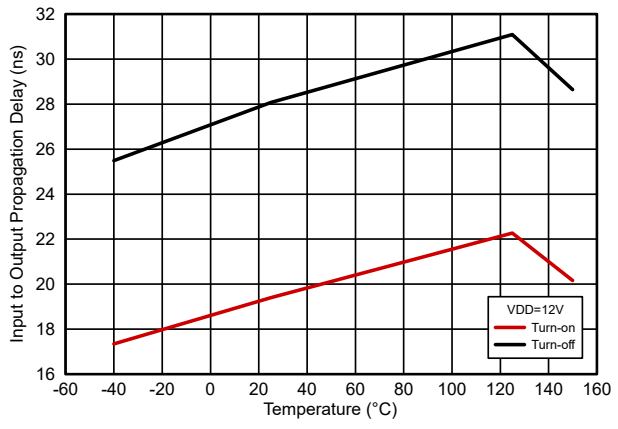
C_{LOAD} = 1.8 nF

図 6-15. Input to Output Rising (turn-on) Propagation Delay vs VDD



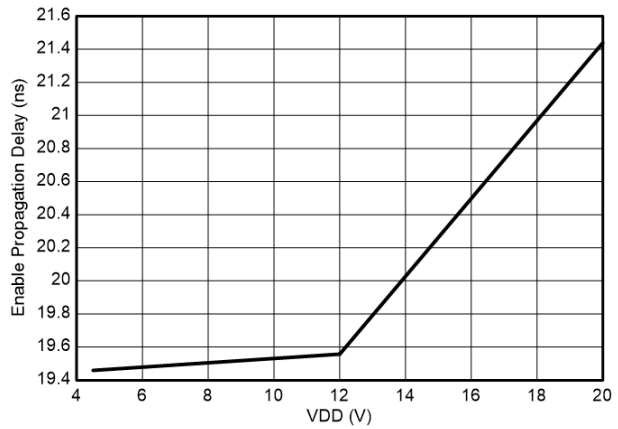
C_{LOAD} = 1.8 nF

図 6-16. Input to Output Falling (turn-off) Propagation Delay vs VDD



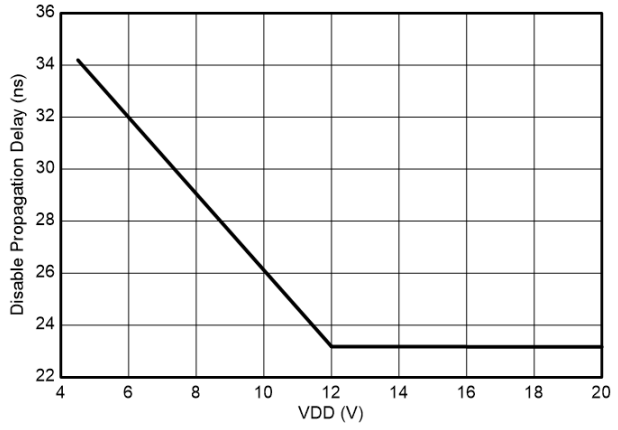
C_{LOAD} = 1.8 nF

図 6-17. Input Propagation Delay vs Temperature



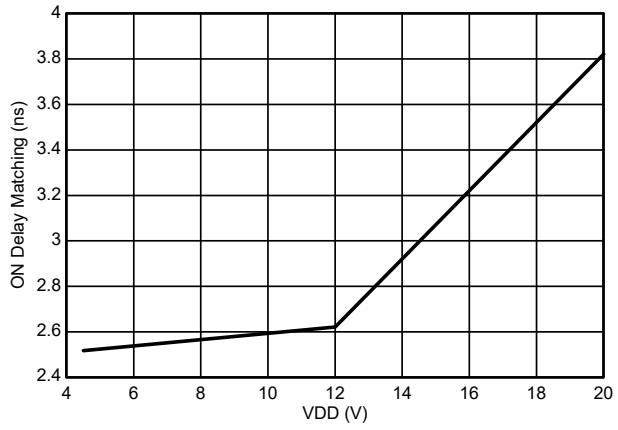
C_{LOAD} = 1.8 nF

図 6-18. Enable to Output Rising Propagation Delay



C_{LOAD} = 1.8 nF

図 6-19. Enable to Output Falling Propagation Delay



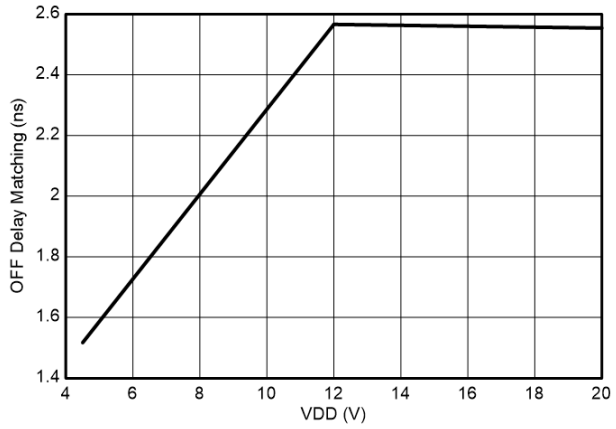
C_{LOAD} = 1.8 nF

図 6-20. Turn-On/Rising Delay Matching

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6.8 Typical Characteristics (continued)

Unless otherwise specified, VDD = 12 V, INx = 3.3 V, ENx = 3.3 V, T_J = 25°C, no load



C_{LOAD} = 1.8 nF

図 6-21. Turn-Off and Falling Delay Matching

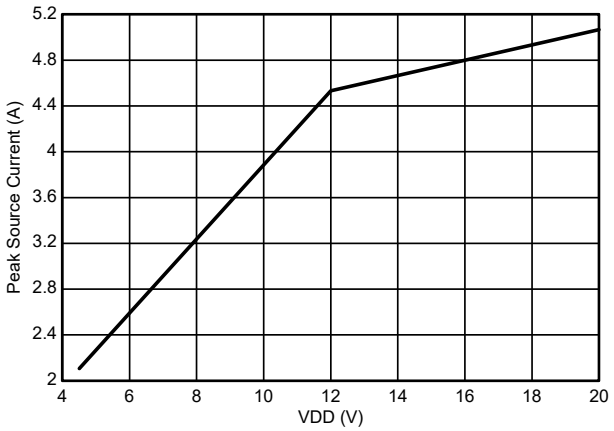


図 6-22. Peak Source Current vs VDD

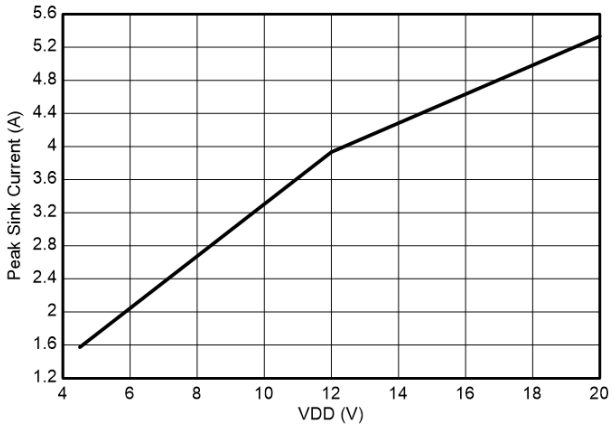


図 6-23. Peak Sink Current vs VDD

7 Detailed Description

7.1 Overview

The UCC27444-Q1 device is the dual-channel, low-side, high-speed, gate driver devices featuring 4-A source and sink current capability, fast switching characteristics, and a host of other features. UCC27444-Q1 Features and Benefits details the advantages of the gate driver's features, which combine to ensure efficient, robust, and reliable operation in high-frequency switching power circuits. The robust inputs of UCC27444-Q1 can handle –5 V, ensuring reliable operation in noisy environments. The driver has good transient handling capability on its output due to its reverse current handling, as well as rail-to-rail output drive, and a small propagation delay (typically 18 ns). With this built-in robustness, the UCC27444-Q1 device can also be directly connected to a gate drive transformer.

The input threshold of UCC27444-Q1 is compatible with TTL low-voltage logic, which is fixed and independent of VDD supply voltage. The driver can also work with CMOS-based controllers as long as the threshold requirement is met.

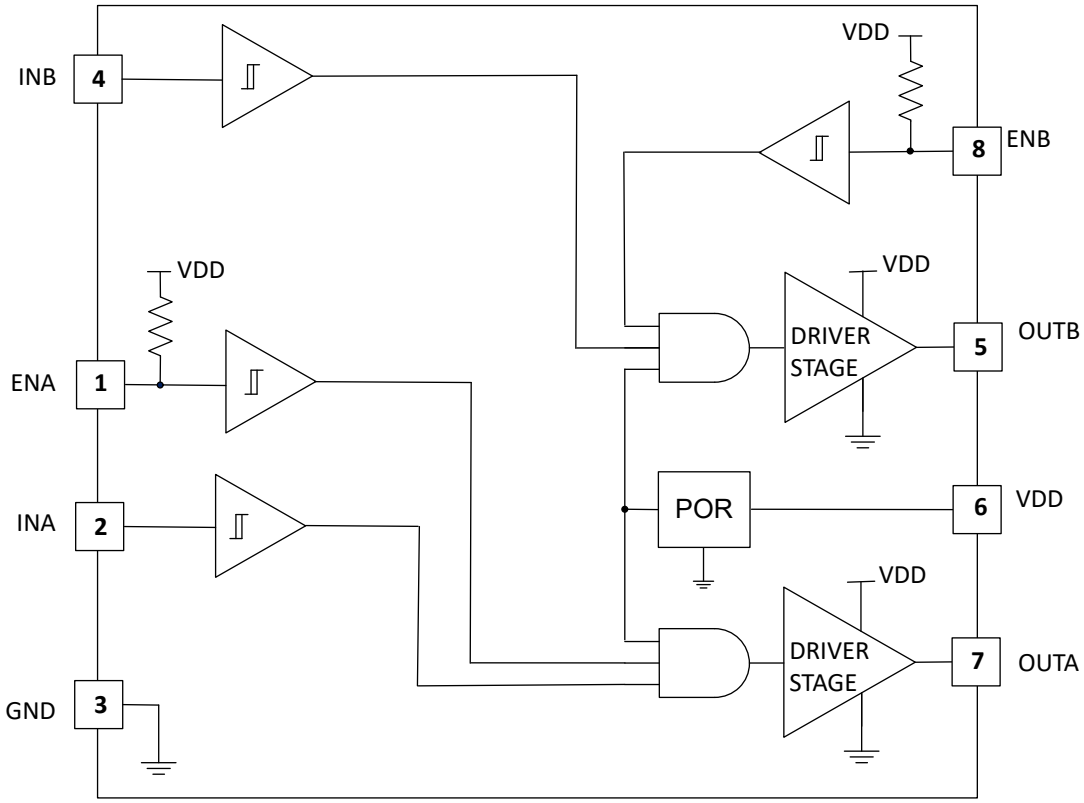
Each channel has an enable pin, ENx, with a fixed TTL compatible threshold. The ENx pins are internally pulled up. Pulling ENx low disables the corresponding channel, while leaving ENx open provides normal operation. The ENx pins can be used as an additional input with the same performance as the INx pins.

表 7-1. UCC27444-Q1 Features and Benefits

FEATURE	BENEFIT
–5-V IN capability	Enhanced signal reliability and device robustness in noisy environments that experience ground bounce on the gate driver
18-ns (typical) propagation delay	Extremely fast control to power device response times.
1-ns (typical) delay matching between channels	Ease of optimizing timing of power device switching such as selecting dead time.
VDD POR protection	Outputs are held low in power on reset conditions, which ensures predictable, glitch-free operation at power-up and power-down.
Outputs are enabled when enable pins (ENx) are in floating condition.	Pin-to-pin compatibility with legacy devices from Texas Instruments in designs where Pin 1 and Pin 8 are "No Connect" pins

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7.2 Functional Block Diagram



Typical ENx pullup resistance is 100 kΩ.

7.3 Feature Description

7.3.1 Operating Supply Current

The UCC27444-Q1 device features low quiescent I_{DD} currents. The typical operating supply current in fully-on state (under static and switching conditions) are summarized in the Electrical Characteristics table. The total supply current is the sum of the quiescent I_{DD} current, the average I_{OUT} current because of switching, and any current related to pullup resistors on the enable pins. Knowing the operating switching frequency (f_{SW}) and the MOSFET gate charge (Q_G) at the drive voltage being used, the average I_{OUT} current can be calculated as product of Q_G and f_{SW}.

The Typical Characteristics provides a complete characterization of the I_{DD} current as a function of switching frequency at different V_{DD} bias voltages. The linear variation and close correlation with the theoretical value of the average I_{OUT} indicate a negligible shoot-through inside the gate driver device, displaying its high-speed characteristics.

7.3.2 Input Stage

The input pins of the UCC27444-Q1 gate driver device are based on a TTL compatible input threshold logic. With a high threshold of 2.2 V and a low threshold of 1.2 V, the logic level thresholds are conveniently driven with PWM control signals derived from 3.3-V and 5-V digital power controller devices.

The UCC27444-Q1 device high resistance driver inputs reduces leakage currents in the input pins. The driver input signals are expected to be in a defined high or low state to control the driver outputs. If a controller is used which may have undefined or tri-state conditions on the driver control signals, it is recommended to have an external pull down resistance from the INx pins to ground.

The input pins can handle wide range of slew rate. In most power supply applications, the gate driver is either driven by the output of a digital controller or logic gates. Therefore, in most applications the input signal slew rate is fast and is no concern for the UCC27444-Q1 family of devices. If limiting the rise or fall times to the power

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device is the primary goal, then an external gate resistor is highly recommended between the output of the driver and the gate of the switching power device. This external resistor has the additional benefit of reducing part of the gate-charge related power dissipation in the gate driver device package and transferring it into the external resistor itself. In short, some of the power gets dissipated in the gate resistor rather than inside of the gate driver. Additionally, the input pins of UCC27444-Q1 are capable of handling –5 V. This improves the system robustness in noisy (electrical) applications. This also enables the driver to directly connect to the output of a gate drive transformer without the use of rectifying diodes, which saves board space and BOM cost.

7.3.3 Enable Function

The enable function is an extremely beneficial feature in gate driver devices, especially for certain applications such as synchronous rectification where the driver outputs are disabled in light-load conditions to prevent negative current circulation and to improve light-load efficiency.

The UCC27444-Q1 device is equipped with independent enable pins (ENx) for exclusive control of each driver channel operation. The enable pins are based on a non-inverting configuration (active-high operation). Thus, when ENx pins are driven high, the drivers are enabled and when ENx pins are driven low, the driver outputs are disabled. Similar to the input pins, the enable pins are also based on a TTL compatible threshold logic that is independent of the supply voltage and are effectively controlled using logic signals from 3.3-V or 5-V controllers. The ENx pins are internally pulled up to VDD using pullup resistors, as a result of which the outputs of the device are enabled in the default state. Hence even if the ENx pins are left floating the driver output is enabled. Essentially, this floating allows the UCC27444-Q1 device to be pin-to-pin compatible with TI's previous generation of drivers (UCC27324, UCC27424, UCC27524), where Pin 1 and Pin 8 are either ENx or N/C pins.

7.3.4 Output Stage

The UCC27444-Q1 device output stage features a P-Channel architecture on the pullup structure, which delivers the highest peak source current when it is most needed, during the Miller plateau region of the power switch turn-on transition (when the power switch drain or collector voltage experiences dV/dt). This pull up achitecture closely emulates the behavior of the popular industry driver devices UCC2732x and UCC2742x. One characteristic of this pullup driver stage architecture is relatively consistent driver output rise and fall times over a wide VDD range.

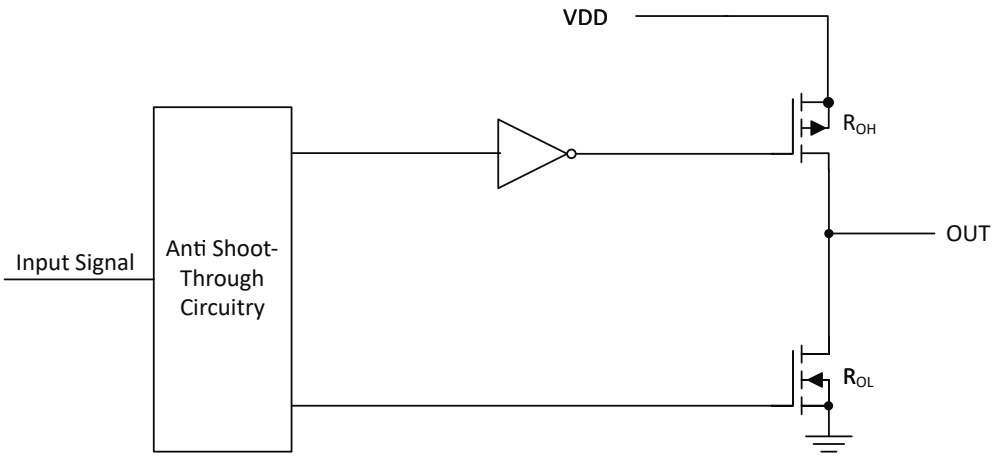


図 7-1. UCC27444-Q1 Gate Driver Output Structure

The R_{OH} parameter is a DC measurement and it is representative of the on-resistance of the P-Channel device on the pull-up stage of the device.

The pull-down structure in the UCC27444-Q1 device is simply comprised of a N-Channel MOSFET. The R_{OL} parameter, which is also a DC measurement, is representative of the impedance of the pulldown stage in the device.

Each output stage in the UCC27444-Q1 device is capable of supplying 4-A peak source and 4-A peak sink current pulses. The output voltage swings between VDD and GND providing rail-to-rail operation, thanks to the

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MOS-output stage which delivers very low dropout. The presence of the MOSFET-body diodes also offers low impedance to transient overshoots and undershoots. The outputs of these drivers are designed to withstand 4 A of peak reverse current transients without damage to the device.

The UCC27444-Q1 device is particularly suited for dual-polarity, symmetrical drive-gate transformer applications where the primary winding of transformer driven by OUTA and OUTB, with inputs INA and INB being driven complementary to each other. This is possible because of the extremely low dropout offered by the MOS output stage of these devices, both during high (V_{OH}) and low (V_{OL}) states along with the low impedance of the driver output stage. All of these allow alleviate concerns regarding transformer demagnetization and flux imbalance. The low propagation delays also ensure proper reset for high-frequency applications.

For applications that have zero voltage switching during power MOSFET turn-on or turn-off interval, the driver supplies high-peak current for fast switching even though the miller plateau is not present. This situation often occurs in synchronous rectifier applications because the body diode is generally conducting before power MOSFET is switched on.

7.3.5 Low Propagation Delays and Tightly Matched Outputs

The UCC27444-Q1 driver device features a low, 18-ns (typical) propagation delay between input and output which offers fast respone time from the control signals to the power devices. Additionally, the driver devices also feature extremely accurate, 1-ns (typical) matched internal propagation delays between the two channels, which is beneficial for applications that require dual gate drives with critical timing. For example, in a PFC application, a pair of paralleled MOSFETs can be driven independently using each output channel, with the inputs of both channels driven by a common control signal from the PFC controller. In this case, the 1-ns delay matching ensures that the paralleled MOSFETs are driven in a simultaneous fashion, minimizing turn-on and turn-off delay differences.

7.4 Device Functional Modes

表 7-2. Device Logic Table

ENA	ENB	INA	INB	UCC27444-Q1	
				OUTA	OUTB
H	H	L	L	L	L
			H	L	H
		H	L	H	L
			H	H	H
L	L	Any	Any	L	L
H Or Float	H Or Float	Float	Float	X	X
Float	Float	L	L	L	L
			H	L	H
		H	L	H	L
			H	H	H

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

High-current gate driver devices are required in switching power applications for a variety of reasons. In order to achieve fast switching of power devices and reduce associated switching-power losses, a powerful gate driver device is employed between the PWM output of control devices and the gates of the power semiconductor devices. Further, gate driver devices are indispensable when it is not feasible for the PWM controller device to directly drive the gates of the switching devices. With the advent of digital power, this situation is often encountered because the PWM signal from the digital controller is often a 3.3-V logic signal which is not capable of effectively turning ON a power switch. A level-shifting circuitry is required to boost the 3.3-V signal to the gate-drive voltage (such as 12 V) in order to fully turn ON the power device and minimize conduction losses. Traditional buffer-drive circuits based on NPN/PNP bipolar transistors in a totem-pole arrangement, as emitter-follower configurations, prove inadequate with digital power because the traditional buffer-drive circuits lack level-shifting capability. Gate driver devices effectively combine both the level-shifting and buffer-drive functions. Gate driver devices also find other needs ,such as minimizing the effect of high frequency switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power device gates, reducing power dissipation and thermal stress in controller devices by moving gate-charge power losses into the controller.

Finally, emerging wide band-gap power device technologies, such as GaN switches, which are capable of supporting very high switching frequency operation, are driving special requirements in terms of gate-drive capability. These requirements include a low operating voltage range (5 V to 6 V), low propagation delays, good delay matching, and availability in compact, low inductance packages with good thermal capability. In summary, gate driver devices are an extremely important component in switching power combining benefits of high performance, low cost, low component count, board space reduction, and simplified system design.

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8.2 Typical Application

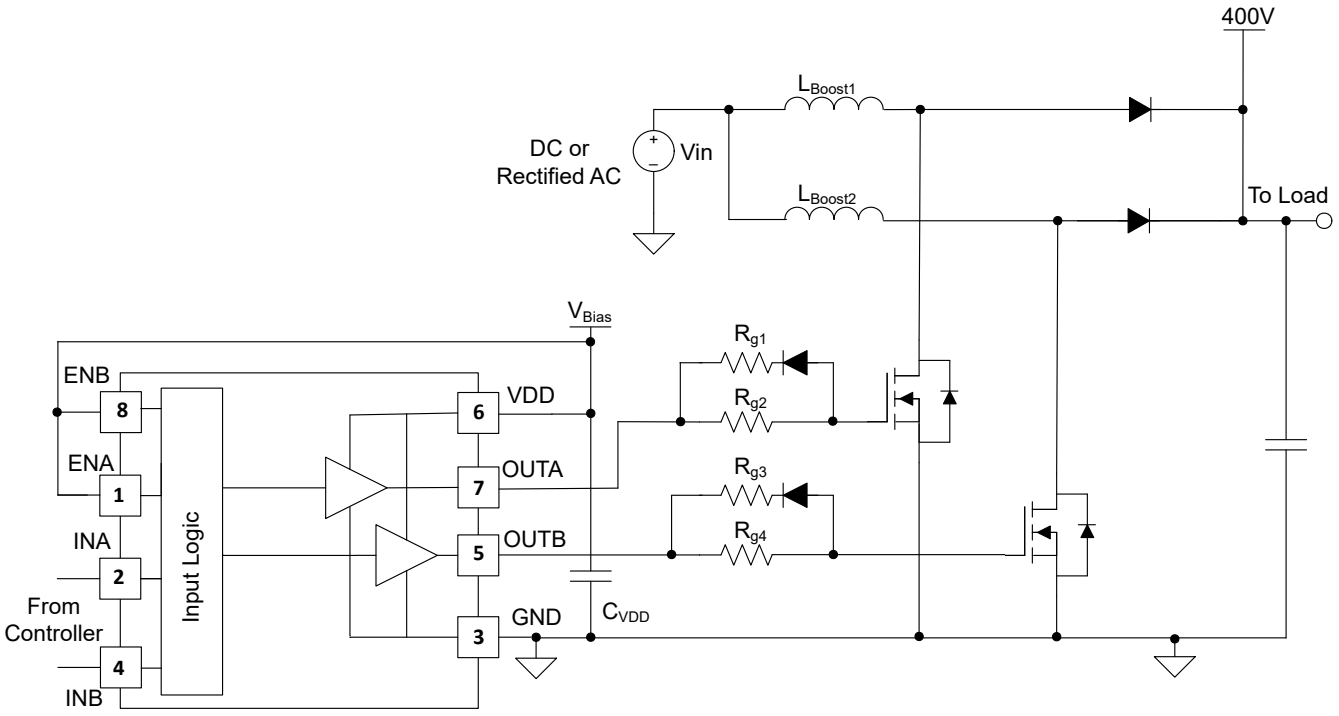


図 8-1. UCC27444-Q1 Typical Application Diagram

8.2.1 Design Requirements

When selecting and designing-in the gate driver device for an end application, some functional aspects must be considered and evaluated first, in order to make the most appropriate selection. Among these considerations are bias voltage, POR, drive current, and power dissipation.

8.2.2 Detailed Design Procedure

8.2.2.1 VDD and Power On Reset

The UCC27444-Q1 device has an internal power on reset (POR) protection feature on the VDD pin supply circuit blocks. When VDD is rising and the level is still below POR threshold, this circuit holds the output low, regardless of the status of the inputs. The POR is typically 3 V with 300-mV typical hysteresis. This hysteresis prevents chatter when VDD supply voltages have noise, specifically at the lower end of the VDD operating range. POR hysteresis is also important to avoid any false tripping due to the bias noise generated because of fast switching transitions, where large peak currents are drawn from the bias supply bypass capacitors. The driver capability to operate at wide bias voltage range, along with good switching characteristics, is especially important in driving emerging power semiconductor devices, such as advanced low gate charge fast MOSFETs, and GaN FETs.

At power-up, the UCC27444-Q1 driver device output remains low until the VDD voltage reaches the POR rising threshold, irrespective of the state of any other input pins such as INx and ENx. After the POR rising threshold, the magnitude of the OUT signal rises with V_{DD} until steady-state V_{DD} is reached.

For the best high-speed circuit performance and to prevent noise problems because the device draws current from the VDD pin to bias all internal circuits, use two VDD bypass capacitors. Also, use surface mount, low ESR capacitors. A 0.1-µF ceramic capacitor should be located less than 1 mm from the VDD to GND pins of the gate-driver device. In addition, a larger capacitor (≥1 µF) must be connected in parallel (also as close to the driver IC as possible) to help deliver the high-current peaks required by the load. The parallel combination of capacitors presents a low impedance characteristic for the expected current levels and switching frequencies in the application.

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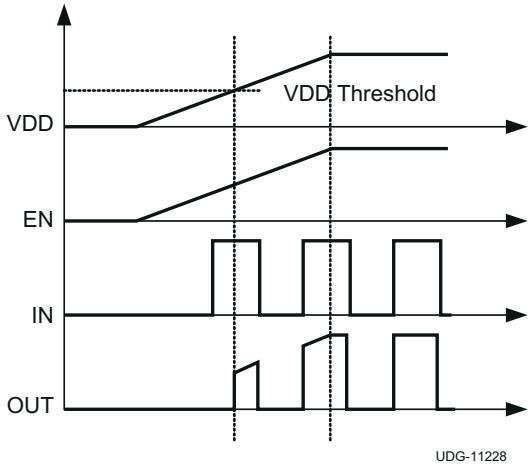


図 8-2. Power-Up Sequence

8.2.2.2 Drive Current and Power Dissipation

The UCC27444-Q1 driver is capable of delivering 4 A of peak current to a switching power device gate (MOSFET, GaN FET) for a period of several-hundred nanoseconds at VDD = 12 V. High peak current is required to turn ON the device quickly. Then, to turn the device OFF, the driver is required to sink a similar amount of current to ground, which repeats at the operating switching frequency of the power device. The power dissipated in the gate driver device package depends on the following factors:

- Gate charge of the power MOSFET (usually a function of the drive voltage V_{GS}, which is very close to input bias supply voltage V_{DD} due to low V_{OH} drop-out).
- Switching frequency
- External gate resistors

Because UCC27444-Q1 features low-quiescent currents and internal logic to eliminate any shoot-through in the output driver stage, their effect on the power dissipation within the gate driver is very small compared to the losses due to switching of the power device.

When a driver device is tested with a discrete capacitive load, calculating the power that is required from the bias supply is fairly simple. The following equation provides an example of the energy that must transfer from the bias supply to charge the capacitor.

$$E_G = \frac{1}{2} C_{LOAD} V_{DD}^2 \tag{1}$$

where

- C_{LOAD} is the load capacitor.
- V_{DD} is the bias voltage of the driver.

There is an equal amount of energy dissipated when the capacitor is discharged. This leads to a total power loss, as shown in the following equation example.

$$P_G = C_{LOAD} V_{DD}^2 f_{SW} \tag{2}$$

where

- f_{SW} is the switching frequency.

With V_{DD} = 12 V, C_{LOAD} = 10 nF and f_{SW} = 300 kHz, the switching power loss is calculated as follows:

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$$P_G = 10\,nF \times 12\,V^2 \times 300\,kHz = 0.432\,W \quad (3)$$

The switching load presented by a power MOSFET is converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Most manufacturers provide specifications that provide the typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Q_g, the power that must dissipate when charging a capacitor is determined, which by using the equivalence $Q_g = C_{LOAD}V_{DD}$ is shown in the following equation.

$$P_G = C_{LOAD}V_{DD}{}^2 f_{SW} = Q_g V_{DD} f_{SW} \quad (4)$$

Assuming that the UCC27444-Q1device is driving power MOSFET with 60 nC of gate charge (Q_g = 60 nC at V_{DD} = 12 V) on each output, the gate charge related power loss is calculated using the equation below.

$$P_G = 2 \times 60\,nC \times 12\,V \times 300\,kHz = 0.432\,W \quad (5)$$

This power P_G is dissipated in the resistive elements of the circuit when the MOSFET turns on or turns off. Half of the total power is dissipated when the load capacitor is charged during turn-on, and the other half is dissipated when the load capacitor is discharged during turn-off. When no external gate resistor is employed between the driver and MOSFET/IGBT, this power is completely dissipated inside the driver package. With the use of external gate resistors, the power dissipation is shared between the internal resistance of driver and external gate resistor in accordance to the ratio of the resistances (more power dissipated in the higher resistance component). Based on this simplified analysis, the driver power dissipation during switching is calculated as follows:

$$P_{SW} = 0.5 \times Q_G \times VDD \times f_{SW} \times \left(\frac{R_{OFF}}{R_{OFF} + R_{GATE}} + \frac{R_{ON}}{R_{ON} + R_{GATE}} \right) \quad (6)$$

where

- $R_{OFF} = R_{OL}$
- R_{ON} (effective resistance of pull-up structure)

The above equation is necessary when the external gate resistor is large enough to reduce the peak current of the driver. In addition to the above gate-charge related power dissipation, dissipation in the driver is related to the power associated with the quiescent bias current consumed by the device to bias all internal circuits such as input stage (with pullup and pulldown resistors), enable, and POR sections. As shown in the electrical characteristics table, the maximum quiescent current is less than 0.6 mA. The power loss due to DC current consumption of the driver internal circuit can be calculated as below.

$$P_Q = I_{DD}V_{DD} \quad (7)$$

Assuming total internal current consumption to be 0.6 mA (maximum) at bias voltage of 12 V, the DC power loss in the driver is:

$$P_Q = 0.6\,mA \times 12\,V = 7.2\,mW \quad (8)$$

This power loss is insignificant compared to gate charge related power dissipation calculated earlier.

With a 12-V supply, the bias current is estimated as follows, with an additional 0.6-mA overhead for the quiescent consumption:

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$$I_{DD} \sim \frac{P_G}{V_{DD}} = \frac{0.432\ W}{12\ V} = 0.036\ A \quad (9)$$

If the gate driver is used with inductive load, then special attention should be paid to the ringing on each pin of the gate driver device. The ringing should not exceed the recommended operating rating of the pin.

8.2.3 Application Curves

The figures below show the typical switching characteristics of the UCC27444-Q1 device used in high-voltage boost converter application. In this application, the UCC27444-Q1 is driving the IGBT switch that has a gate charge of
110nC.

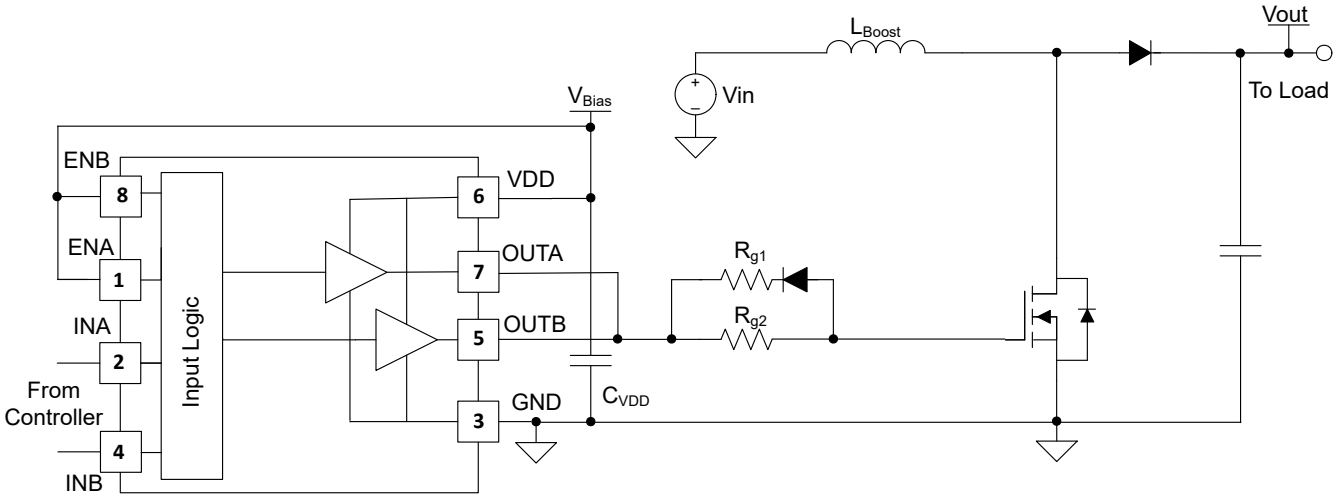
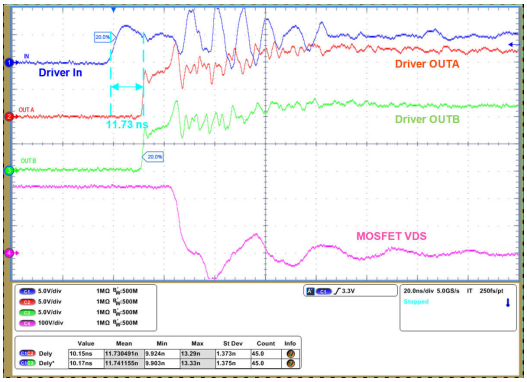
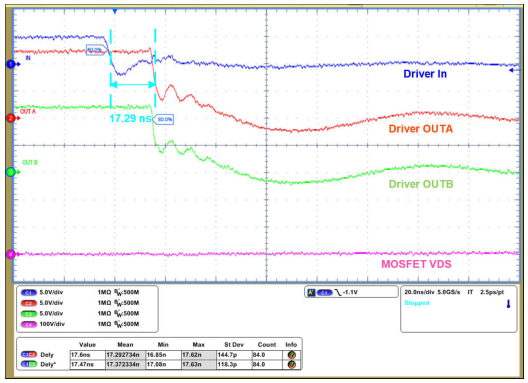


図 8-3. UCC27444-Q1 Used to Drive IGBT in the Boost Converter



Vin = 210 V, Vout= 235 V, Iout=1.1 A, Fsw=125 kHz, driver supply voltage=12 V, gate resistor= 0 Ω

図 8-4. Turn-On Propagation Delay Waveform



Vin = 210 V, Vout= 235 V, Iout=1.1A, Fsw=125 kHz, driver supply voltage=12 V, gate resistor= 0 Ω

図 8-5. Turn-Off Propagation Delay Waveform

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9 Power Supply Recommendations

The bias supply voltage range for the UCC27444-Q1 device is rated to operate is from 4.5 V to 18 V. The lower end of this range is governed by the internal power-on-reset (POR) protection feature on the V_{DD} pin supply circuit blocks. If the driver is in a POR condition when the V_{DD} pin voltage is below the VDD POR turn-on (rising) threshold, the POR protection feature holds the output low, regardless of the status of the inputs. The upper end of this range is driven by the 20-V absolute maximum voltage rating of the VDD pin of the device (which is a stress rating). It is necessary to have sufficient margin from the absolute maximum rating of the device to realize full operating life of the device. Therefore, the upper limit of recommended voltage of the VDD pin is 18 V.

The POR protection feature also has a hysteresis function. This means, when the VDD pin bias voltage exceeds the rising threshold voltage, the device begins to operate normally. If the VDD bias voltage drops below the rising threshold while on, the device continues to deliver normal functionality unless the voltage drop exceeds the hysteresis specification of the falling threshold. Therefore, while operating at or near the 4.5-V, design engineer should ensure that the voltage ripple on the auxiliary power supply output is smaller than the hysteresis specification of the device. Otherwise, the device output may turn-off. During system shutdown, the device operation continues until the VDD pin voltage has dropped below the VDD turn-off (falling) threshold, which must be accounted for while evaluating system shutdown timing or sequencing requirements. At system startup, the device does not begin operation until the VDD pin voltage has exceeded VDD turn-on (rising) threshold.

The quiescent current consumed by the internal circuit blocks of the device is supplied through the VDD pin. Although this fact is well known, recognizing that the charge for source current pulses delivered by the OUTA/B pin is also supplied through the same VDD pin capacitor, is important. As a result, every time a current is sourced out of the output pins, a corresponding current pulse is delivered into the device through the VDD pin. Thus, ensure that the local bypass capacitors are provided between the VDD and GND pins and locate them as close to the device pins as possible for the purpose of decoupling. A low ESR, ceramic surface mount capacitor is required. TI recommends having two capacitors: a 0.1-µF ceramic surface-mount capacitor placed less than 1 mm from the VDD pin of the device and another larger ceramic capacitor (≥1 µF) must be connected in parallel.

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10 Layout

10.1 Layout Guidelines

Proper PCB layout is extremely important in a high-current fast-switching circuit to provide appropriate device operation and design robustness. The UCC27444-Q1 gate driver incorporates small propagation delays and powerful output stages capable of delivering large current peaks with very fast rise and fall times at the gate of power MOSFET to facilitate very quick voltage transitions. Very high di/dt causes unacceptable ringing if the trace lengths and impedances are not well controlled. The following circuit layout guidelines are recommended when designing with these high-speed drivers.

- Place the driver IC as close as possible to the power device in order to minimize the length of high-current traces between the driver IC output pins and the gate of the switching power device.
- Place the VDD bypass capacitors between VDD and GND as close as possible to the driver IC with minimal trace length to improve the noise filtering. These capacitors support high peak current being drawn from VDD pin, during turn-on of power MOSFET. The use of low inductance surface-mounted-device (SMD) components such as 50V rated X7R chip capacitors are highly recommended.
- The turn-on and turn-off current loop paths (driver device, power MOSFET and VDD bypass capacitor) must be minimized as much as possible in order to keep the stray inductance to a minimum. High dI/dt is established in these loops at two instances, namely during turn-on and turn-off transients, which induces significant voltage transients on the output pin of the driver device and Gate of the power MOSFET.
- Wherever possible, parallel the source and return traces to take advantage of flux cancellation.
- Separate power traces and signal traces, such as output and input signals.
- To minimize switch node transients and ringing, adding some gate resistance and/or snubbers on the power devices may be necessary. These measures may also reduce EMI.
- Star-point grounding is a good way to minimize noise coupling from one current loop to another. The GND of the driver is connected to the other circuit nodes such as source of power MOSFET and ground of PWM controller at one, single point. The connected paths must be as short as possible to reduce inductance and be as wide as possible to reduce resistance.
- Use a ground plane to provide noise shielding. Fast rise and fall times at OUT pin of the driver IC may corrupt the input signals of the driver IC. The ground plane must not be a conduction path for any high current (power stage) loop. Instead the ground plane must be connected to the star-point with one single trace to establish the ground potential. In addition to noise shielding, the ground plane can help in power dissipation as well
- External gate resistor and parallel diode-resistor combination may come in handy when replacing any gate driver IC with UCC27444-Q1 device in existing or new designs, specifically if they do not have the same drive strength.

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10.2 Layout Example

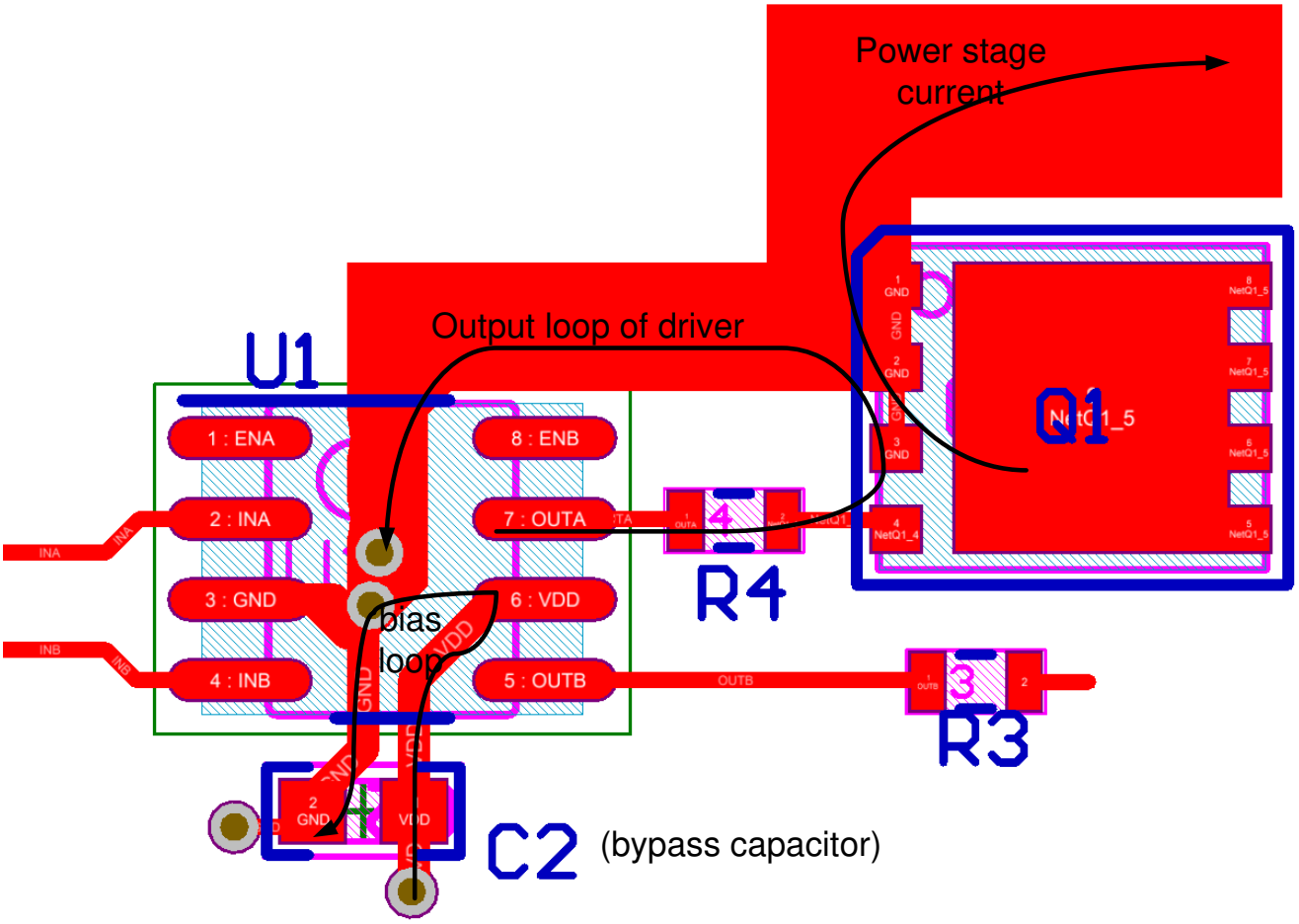


図 10-1. UCC27444-Q1 Layout Example

10.3 Thermal Considerations

The useful range of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the device package. In order for a gate driver device to be useful over a particular temperature range, the package must allow for the efficient removal of the heat produced, while keeping the junction temperature within the specified limit. For detailed information regarding the thermal information table, please refer to the *Semiconductor and IC Package Thermal Metrics Application Note* (SPRA953).

Among the different package options available for the UCC27444-Q1 device, power dissipation capability of the DGN package is of particular mention. The VSSOP-8 (DGN) package offers thermal pad for removing the heat from the semiconductor junction through the bottom of the package. This pad is soldered to the copper on the printed circuit board directly underneath the device package, reducing the thermal resistance to a very low value. This allows a significant improvement in heat-sinking over the D package. The printed circuit board must be designed with thermal lands and thermal vias to complete the heat removal subsystem. Note that the exposed pads in the VSSOP-8 package are not directly connected to any leads of the package, however,PowerPAD is thermally connected to the substrate of the device. TI recommends to externally connect the exposed pads to GND pin of the driver IC in PCB layout.

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11 Device and Documentation Support

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11.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC27444QDGNRQ1	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	444Q
UCC27444QDGNRQ1.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	444Q
UCC27444QDRQ1	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27444Q
UCC27444QDRQ1.A	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27444Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF UCC27444-Q1 :

- Catalog : UCC27444

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

GENERIC PACKAGE VIEW

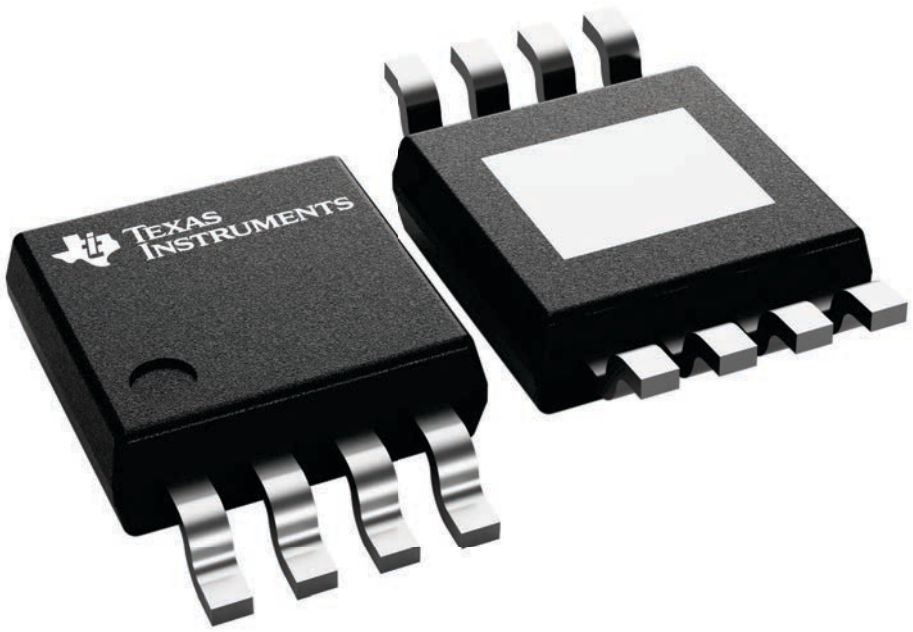
DGN 8

PowerPAD™ HVSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



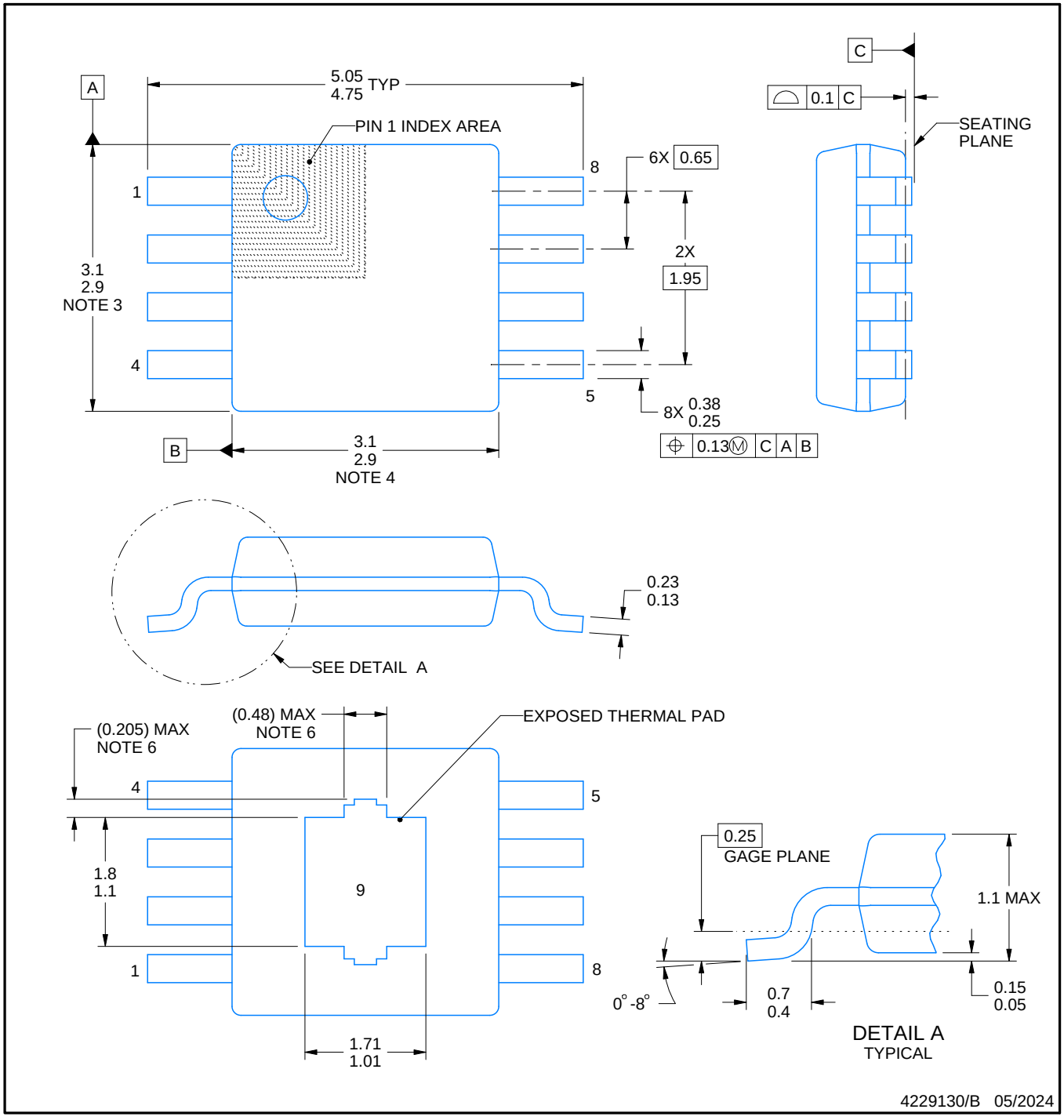
4225482/B

PACKAGE OUTLINE

DGN0008H

PowerPAD™ VSSOP - 1.1 mm max height

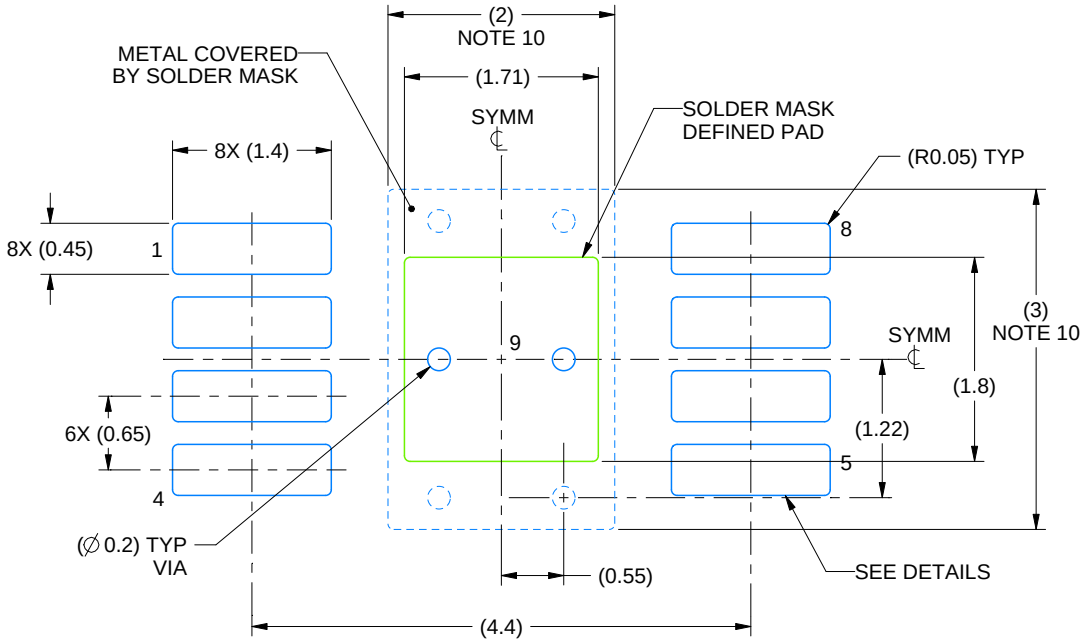
SMALL OUTLINE PACKAGE



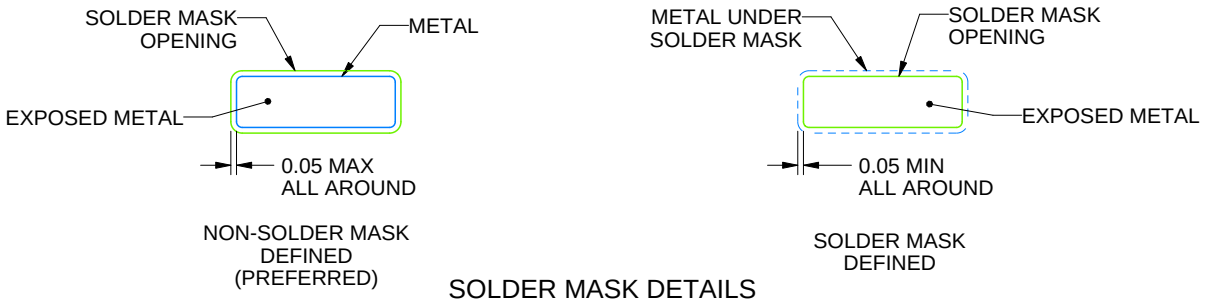
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.
6. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

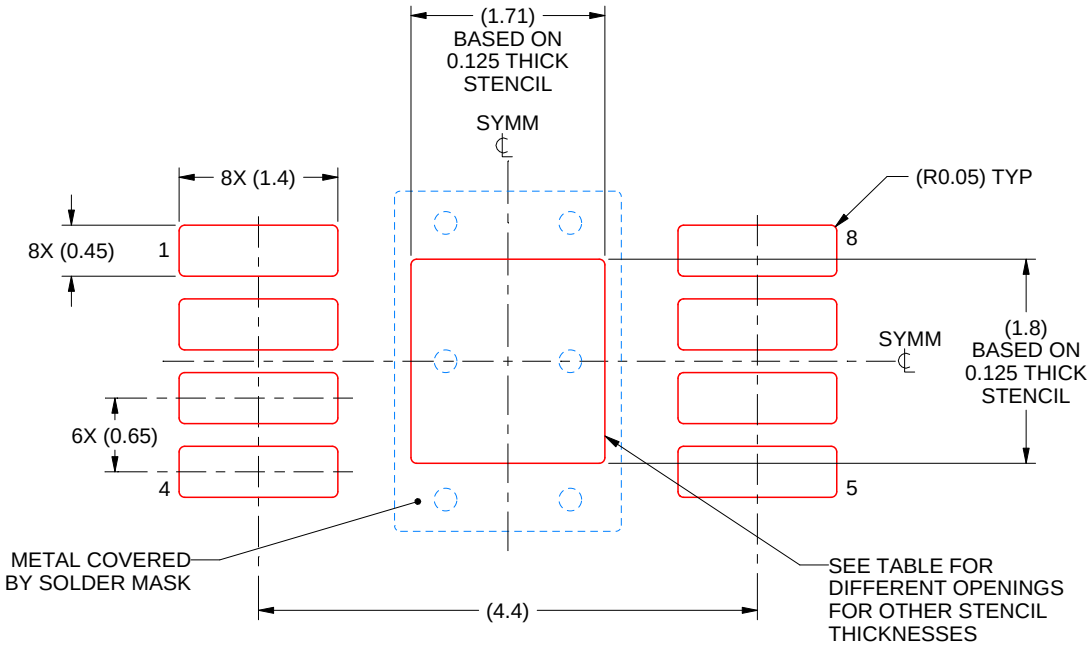


SOLDER MASK DETAILS

4229130/B 05/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
9. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.



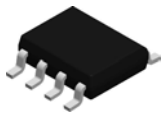
SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.91 X 2.01
0.125	1.71 X 1.80 (SHOWN)
0.15	1.56 X 1.64
0.175	1.45 X 1.52

4229130/B 05/2024

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

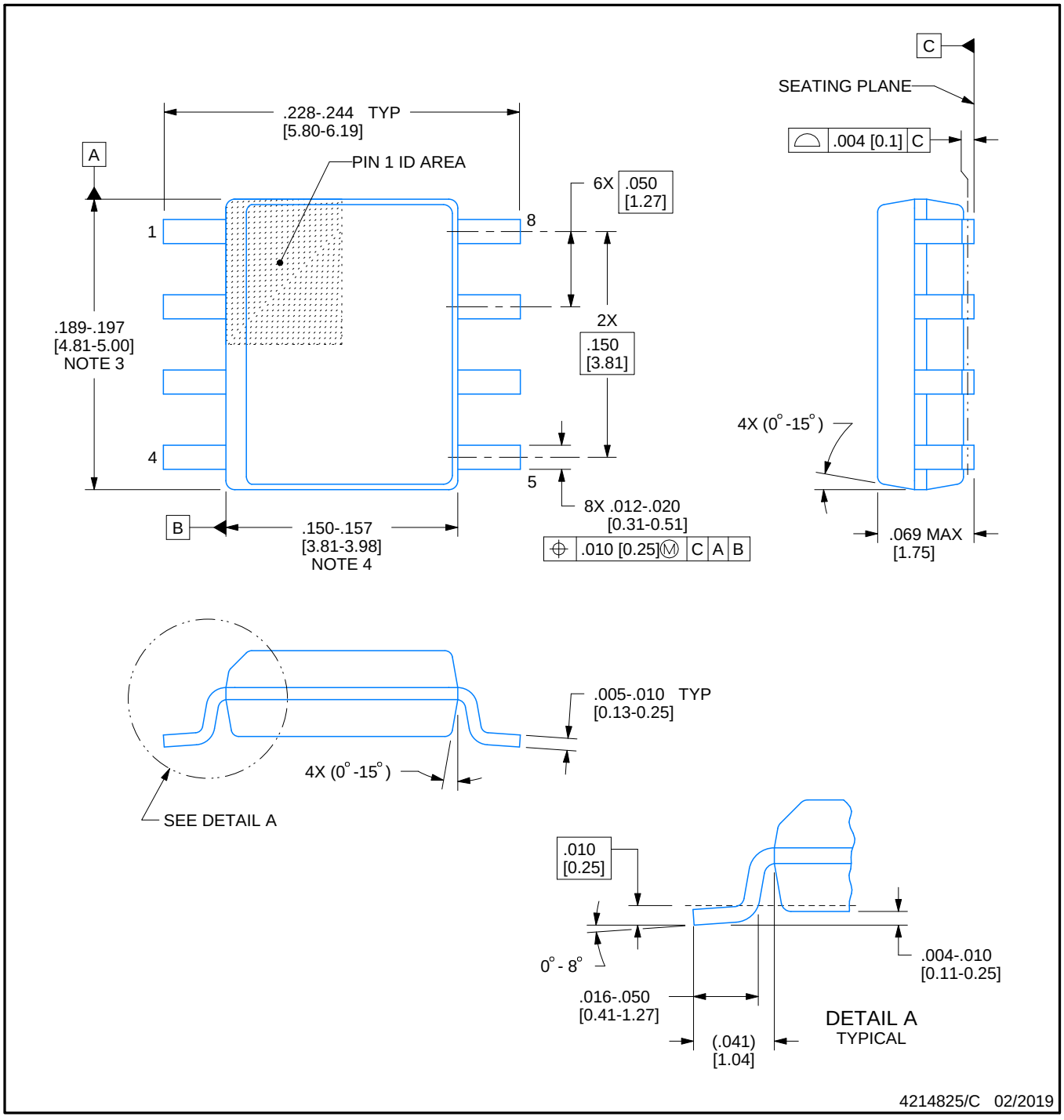


PACKAGE OUTLINE

D0008A

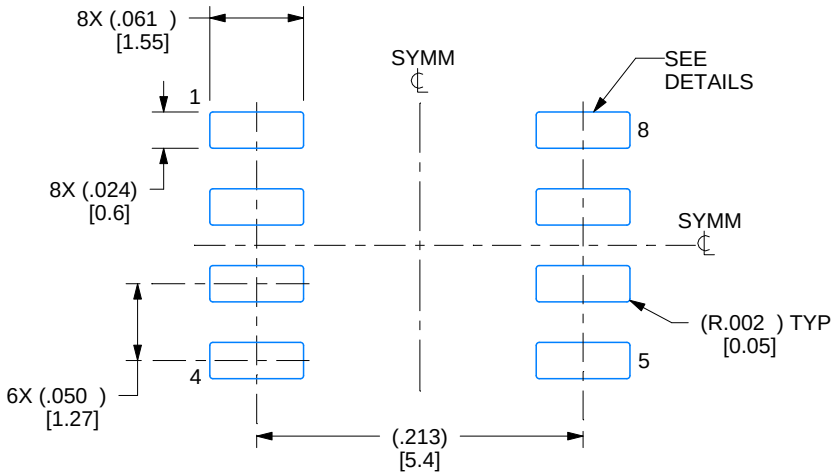
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

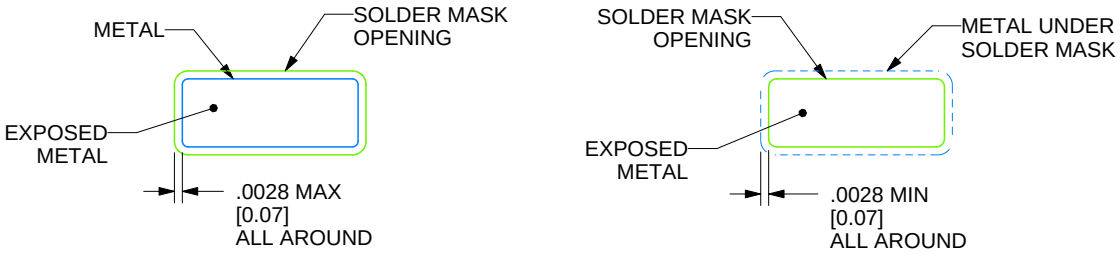


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

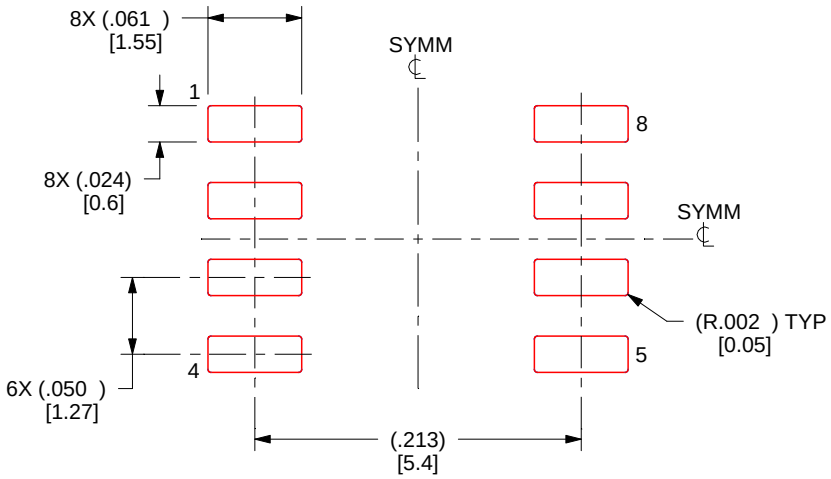
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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