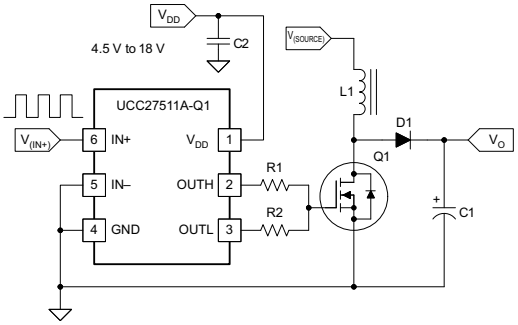
UCC27511A-Q1 4A ピーク ソースおよび 8A ピーク シンクの シングル チャネル、高速ローサイド ゲート ドライバ

1 特長

- 車載アプリケーション用に認定済み
- 下記内容で AEC-Q100 認定済み:
  - デバイス温度グレード 1:-40℃～125℃の動作時周囲温度範囲
  - デバイス HBM ESD 分類レベル 2
  - デバイス CDM ESD 分類レベル C4B
- NPN/PNP ディスクリート ソリューションの代替として最適な低コストのゲートドライバ デバイス
- 4A ピーク ソースおよび 8A ピーク シンク非対称駆動
- 大きなシンク電流によってミラー ターンオンに対する耐性を強化
- UCC27511A-Q1 内での分割出力構成 (ターンオン / ターンオフの速度を簡単に、別々に調整可能)
- 短い伝搬遅延 (標準値 13ns)
- 高速立ち上がり / 立ち下がり時間 (標準値 8ns / 7ns)
- 4.5V～18V の単一電源電圧範囲
- V_{DD} UVLO 時に出力を LOW に保持(電源オンおよび電源オフ時にグリッチのない動作を保証)
- TTL および CMOS 互換の入力ロジック スレッショルド (電源電圧に無関係)
- ヒステリシス付きのロジック スレッショルド による優れたノイズ耐性
- デュアル入力の設計(反転(IN-ピン)または非反転(IN+ピン)のドライバ構成を選択)
  - 使用しない入力ピンはイネーブルおよびディスエーブル機能に使用可能
- 入力ピンのフローティング時は出力を LOW に保持
- 入力ピンの絶対最大電圧レベルが V_{DD} ピンのバイアス電源電圧に制限されない
- 入力ピンは GND ピンより -5V (DC) 低い電圧に耐性
- 動作温度範囲:–40°C～140°C
- 6 ピン DBV (SOT-23) パッケージ オプション



非反転入力のアプリケーション図

2 アプリケーション

- スイッチ モード電源
- DC/DC コンバータ
- デジタル電源コントローラ用コンパニオン ゲートドライバ デバイス
- 太陽光発電、モータ制御、UPS
- GaN など、最新のバンドギャップの広いパワー デバイスのゲート駆動

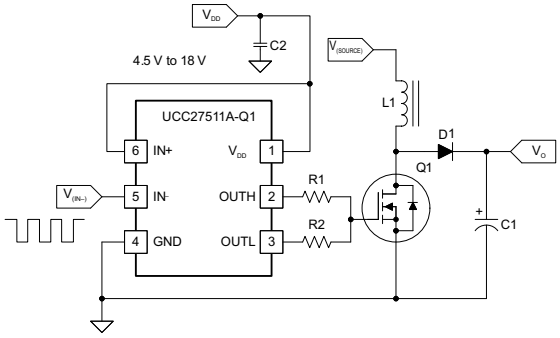
3 概要

UCC27511A-Q1 デバイスは小型のゲート ドライバで、NPN または PNP ディスクリートドライバ (バッファ回路) ソリューションの優れた代替品です。UCC27511A-Q1 車載グレード デバイスはシングル チャネル、ローサイド、高速ゲート ドライバで、MOSFET、IGBT、および最新の GaN などバンドギャップが広いパワー デバイス用の定格を備えています。UCC27511A-Q1 デバイスは立ち上がり、立ち下がり、伝播遅延の時間が短いため、高速なアプリケーションに適しています。本デバイスは、4A ピーク ソースおよび 8A ピーク シンク電流の非対称駆動能力を備えており、寄生ミラー ターンオン効果に対する耐性を強化しています。出力の分離構成により、2 つの抵抗を使用するだけで立ち上がりと立ち下がりの時間を簡単に、別々に調整でき、外付けのダイオードは必要ありません。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
UCC27511A-Q1	DBV (SOT-23 6)	2.90mm × 1.60mm

(1) 供給されているすべてのパッケージについては、セクション 12 を参照してください。



反転入力のアプリケーション図

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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4 Pin Configuration and Functions

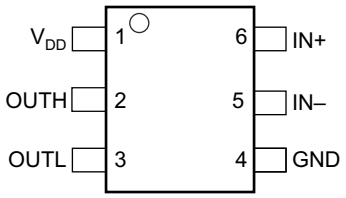


図 4-1. DBV Package 6-Pin SOT-23 Top View

表 4-1. Pin Functions

PIN		I/O	FUNCTION
NO.	NAME		
1	VDD	I	Bias supply input.
2	OUTH	O	Sourcing current output of driver. Connet a resistor between the OUTH pin and the gate of the power-switching device to adjust turnon speed.
3	OUTL	O	Sinking current output of driver. Connect a resistor between the OUTL pin and the gate of the power-switching device to adjust turnoff speed.
4	GND	—	Ground. All signals referenced to this pin.
5	IN–	I	Inverting input. When the driver is used in non-inverting configuration, connect the IN– pin to GND in order to enable output. The OUTx pin is held low if the IN– pin is unbiased or floating.
6	IN+	I	Non-inverting input. When the driver is used in inverting configuration, connect the IN+ pin to V_{DD} in order to enable output. The OUTx pin is held low if the IN+ pin is unbiased or floating.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2) (3)

			MIN	MAX	UNIT
Supply voltage	V_{DD}		–0.3	20	V
Input voltage	IN+, IN– (4)		–6	20	
Output voltage	OUTH		–0.3	V_{DD} + 0.3	
	OUTL	DC	–0.3	20	
		Repetitive pulse less than 200 ns (5)	–2	20	
Output continuous current (OUTH source current and OUTL sink current)	I_{O_DC} (source)			0.3	A
	I_{O_DC} (sink)			0.6	
Output pulsed current (0.5 µs) (OUTH source current and OUTL sink current)	I_{O_pulsed}(source)			4	
	I_{O_pulsed}(sink)			8	
Operating virtual junction temperature range, T_J			–40	150	°C
Lead temperature	Soldering, 10 sec.			300	
	Reflow			260	

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND unless otherwise noted. Currents are positive into and negative out of the specified terminal. See the セクション 7.2.2.7 for thermal limitations and considerations of packages.
(3) These devices are sensitive to electrostatic discharge; follow proper device handling procedures.
(4) Maximum voltage on input pins is not restricted by the voltage on the V_{DD} pin.
(5) Values are verified by characterization on bench.

5.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	–4000	4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins	–1000	1000	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	4.5	12	18	V
V_I	Input voltage, IN+ and IN–	–5		18	V
T_A	Operating junction temperature range	–40		140	°C

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5.4 Thermal Information

THERMAL METRIC[1]		DBV	UNIT
		6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	217.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	97.6	
$R_{\theta JB}$	Junction-to-board thermal resistance	72.2	
ψ_{JT}	Junction-to-top characterization parameter	8.6	
ψ_{JB}	Junction-to-board characterization parameter	71.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics Application Rport*.

5.5 Electrical Characteristics

V_{DD} = 12 V, T_A = T_J = –40°C to 140°C, 1-µF capacitor from V_{DD} to GND. Currents are positive into, negative out of the specified terminal.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
BIAS CURRENTS							
$I_{(START)}$	Startup current	V_{DD} = 3.4 V	IN+ = V_{DD}, IN– = GND	40	100	160	µA
			IN+ = IN– = GND or IN+ = IN– = V_{DD}	25	75	145	
			IN+ = GND, IN– = V_{DD}	20	60	115	
UNDERVOLTAGE LOCKOUT (UVLO)							
$V_{(ON)}$	Supply start threshold	T_A = 25°C		3.91	4.2	4.5	V
		T_A = –40°C to 140°C		3.7	4.2	4.65	
$V_{(OFF)}$	Minimum operating voltage after supply start			3.45	3.9	4.35	
$V_{DD(hys)}$	Supply voltage hysteresis			0.2	0.3	0.5	
INPUTS (IN+, IN–)							
$V_{IH(IN)}$	Input signal high threshold	Output high for IN+ pin, Output low for IN– pin			2.2	2.4	V
$V_{IL(IN)}$	Input signal low threshold	Output low for IN+ pin, Output high for IN– pin		1.0	1.2		
$V_{hys(IN)}$	Input signal hysteresis				1		
SOURCE AND SINK CURRENT							
$I_{P(SRC)}$	Source peak current[1]	$C_{(LOAD)}$ = 0.22 µF, f_S = 1 kHz			–4		A
$I_{P(SNK)}$	Sink peak current[1]	$C_{(LOAD)}$ = 0.22 µF, f_S = 1 kHz			8		A
OUTPUTS (OUTH, OUTL, OUT)							
V_{OH}	High output voltage	V_{DD} = 12 V, $I_{(OUTH)}$ = –10 mA			50	90	mV
		V_{DD} = 4.5 V, $I_{(OUTH)}$ = –10 mA			60	130	
V_{OL}	Low output voltage	V_{DD} = 12, $I_{(OUTL)}$ = 10 mA			5	6.5	
		V_{DD} = 4.5 V, $I_{(OUTL)}$ = 10 mA			5.5	10	

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5.5 Electrical Characteristics (続き)

V_{DD} = 12 V, T_A = T_J = –40°C to 140°C, 1-µF capacitor from V_{DD} to GND. Currents are positive into, negative out of the specified terminal.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{O(H)}$	Output pullup resistance(2)	V_{DD} = 12 V $I_{(OUTH)}$ = –10 mA		5	7.5	Ω
		VDD = 4.5 V $I_{(OUTH)}$ = –10 mA		5	11	
$R_{O(L)}$	Output pulldown resistance	V_{DD} = 12 V $I_{(OUTL)}$ = 10 mA		0.375	0.65	
		V_{DD} = 4.5 V $I_{(OUTL)}$ = 10 mA		0.45	0.75	

(1) Ensured by Design.
(2) $R_{O(H)}$ represents the on-resistance of P-channel MOSFET in pullup structure of the output stage of the UCC27511A-Q1 device.

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5.6 Switching Characteristics

V_{DD} = 12 V, T_A = T_J = –40°C to 140°C, 1-µF capacitor from V_{DD} to GND. Currents are positive into, negative out of the specified terminal. See 図 5-1, 図 5-2, 図 5-3, and 図 5-4

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time(1)	V_{DD} = 12 V $C_{(LOAD)}$ = 1.8 nF, connected to OUTH and OUTL pins tied together		8	12	ns
		V_{DD} = 4.5 V $C_{(LOAD)}$ = 1.8 nF		16	22	
t_f	Fall time(1)	V_{DD} = 12 V $C_{(LOAD)}$ = 1.8 nF, connected to OUTH and OUTL pins tied together		7	11	ns
		V_{DD} = 4.5 V $C_{(LOAD)}$ = 1.8 nF		7	11	
$t_{d(1)}$	IN+ to output propagation delay(1)	V_{DD} = 12 V 5-V input pulse $C_{(LOAD)}$ = 1.8 nF, connected to OUTH and OUTL pins tied together	4	13	23	ns
		V_{DD} = 4.5 V 5-V input pulse $C_{(LOAD)}$ = 1.8 nF, connected to OUTH and OUTL pins tied together	4	15	26	
$t_{d(2)}$	IN– to output propagation delay(1)	V_{DD} = 12 V $C_{(LOAD)}$ = 1.8 nF, connected to OUTH and OUTL pins tied together	4	13	23	ns
		V_{DD} = 4.5 V $C_{(LOAD)}$ = 1.8 nF, connected to OUTH and OUTL pins tied together	4	19	30	

(1) See timing diagrams in 図 5-1, 図 5-2, 図 5-3, and 図 5-4.

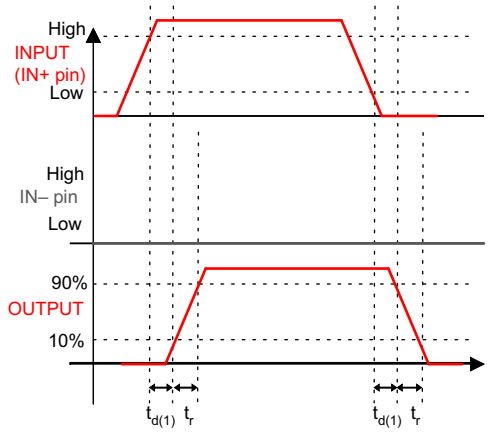


図 5-1. Non-Inverting Configuration (PWM Input to IN+ pin (IN– Pin Tied to GND), Output Represents OUTH and OUTL Pins Tied Together in the UCC27511A-Q1)

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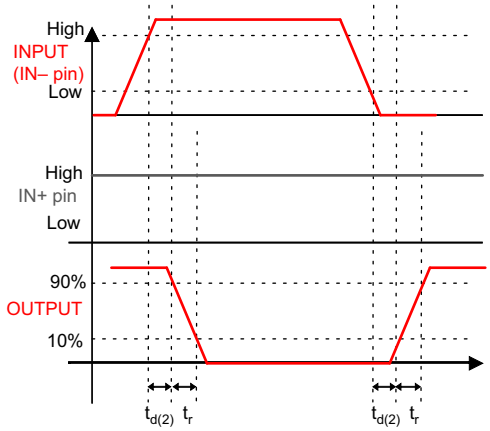


図 5-2. Inverting Configuration (PWM Input to IN– Pin (IN+ Pin Tied to V_{DD}), Output Represents OUTH and OUTL Pins Tied Together in the UCC27511A-Q1)

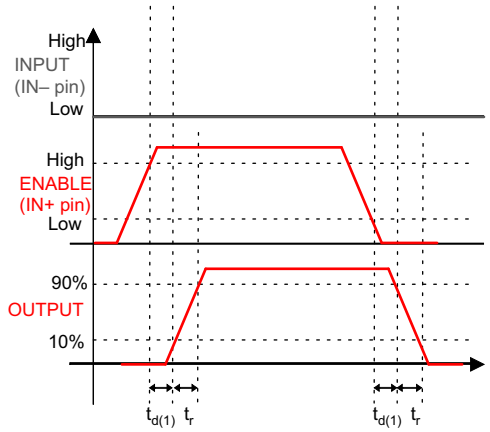


図 5-3. Enable And Disable Function Using IN+ Pin (Enable and Disable Signal Applied to IN+ Pin, PWM Input to IN– Pin, Output Represents OUTH and OUTL Pins Tied Together in the UCC27511A-Q1)

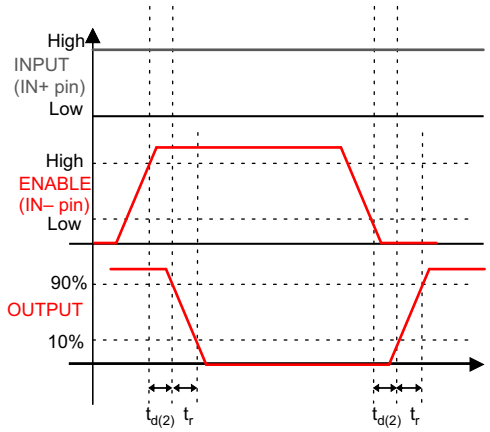
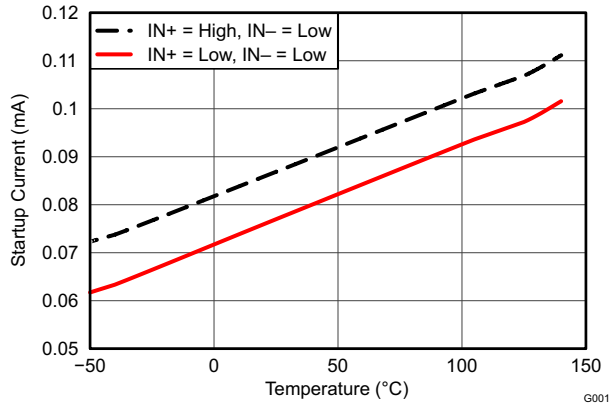


図 5-4. Enable and Disable Function Using IN– Pin (Enable and Disable Signal Applied to IN– Pin, PWM Input to IN+ Pin, Output Represents OUTH and OUTL Pins Tied Together in the UCC27511A-Q1)

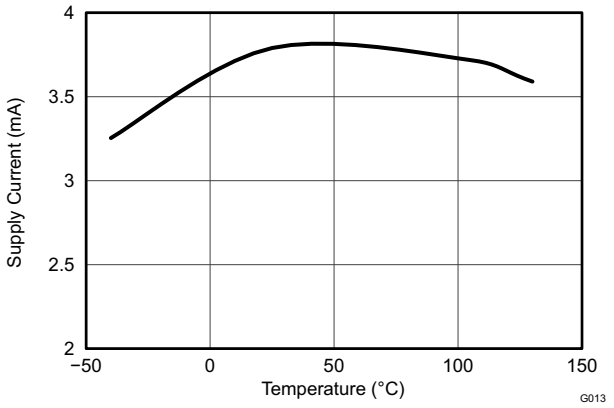
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5.7 Typical Characteristics



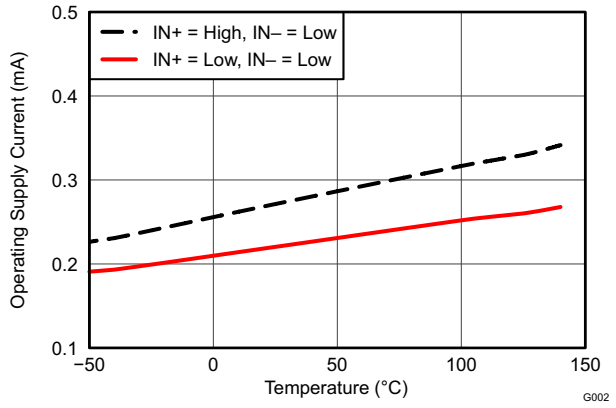
V_{DD} = 3.4 V

図 5-5. Startup Current vs Temperature



V_{DD} = 12 V $C_{(LOAD)}$ = 500 pF f_S = 500 kHz

図 5-6. Operating Supply Current vs Temperature (Output Switching)



V_{DD} = 12 V

図 5-7. Supply Current vs Temperature (Output in DC On or Off Condition)

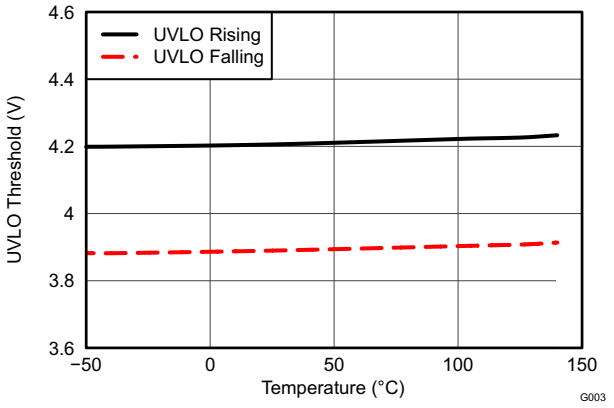
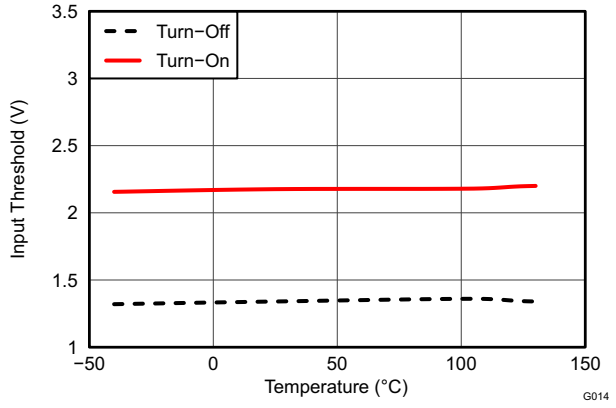
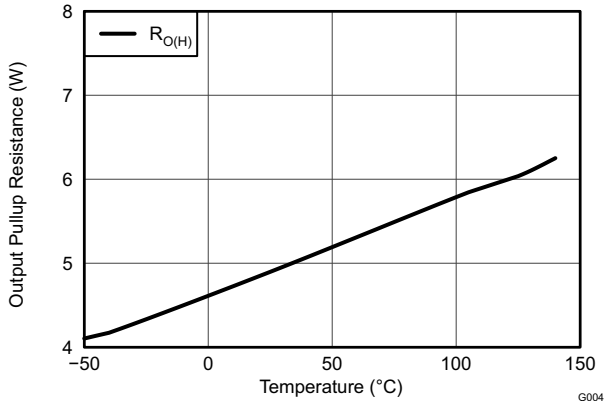


図 5-8. UVLO Threshold Voltage vs Temperature



V_{DD} = 12 V $C_{(LOAD)}$ = 1.8 nF

図 5-9. Input Threshold vs Temperature

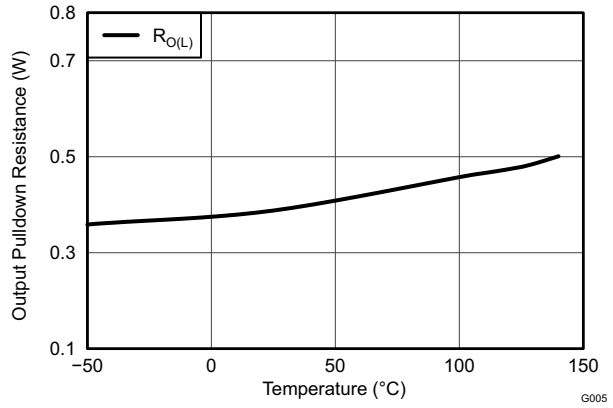


V_{DD} = 12 V I_O = 10 mA

図 5-10. Output Pullup Resistance vs Temperature

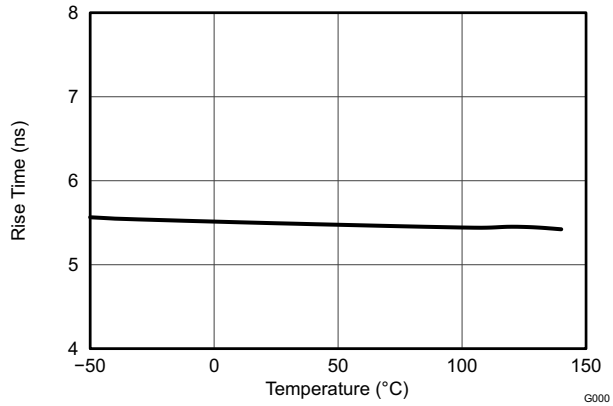
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5.7 Typical Characteristics (continued)



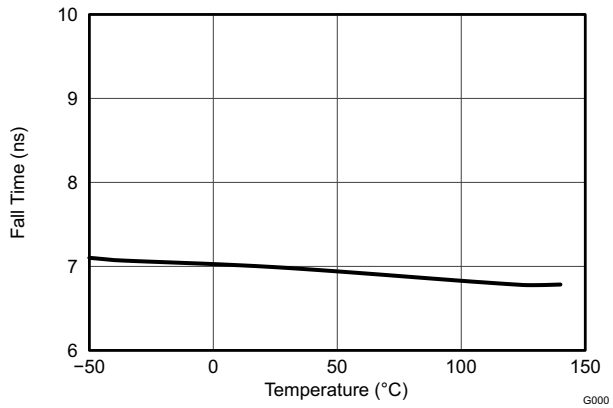
V_{DD} = 12 V I_O = 10 mA

図 5-11. Output Pull-Down Resistance vs Temperature



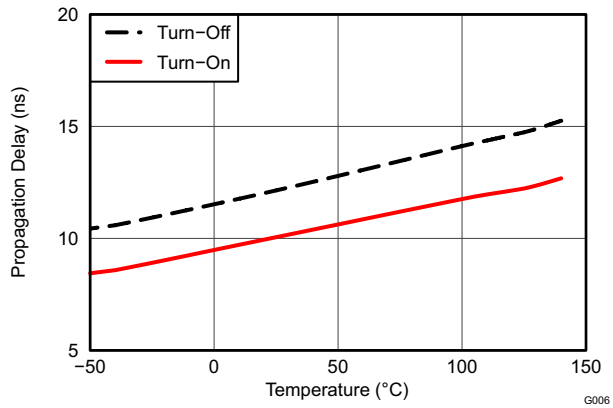
V_{DD} = 12 V $C_{(LOAD)}$ = 1.8 nF

図 5-12. Rise Time vs Temperature



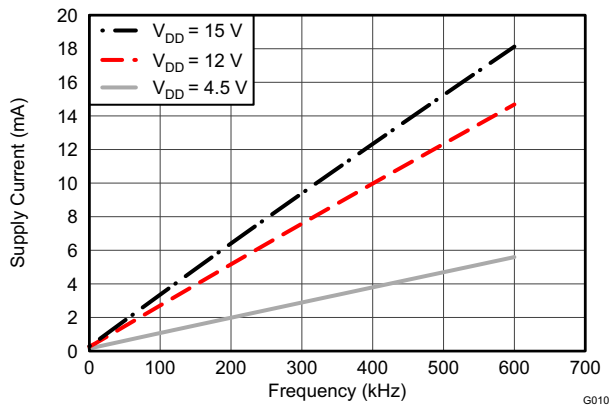
V_{DD} = 12 V $C_{(LOAD)}$ = 1.8 nF

図 5-13. Fall Time vs Temperature



V_{DD} = 12 V

図 5-14. Input to Output Propagation Delay vs Temperature



$C_{(LOAD)}$ = 1.8 nF

図 5-15. Operating Supply Current vs Frequency

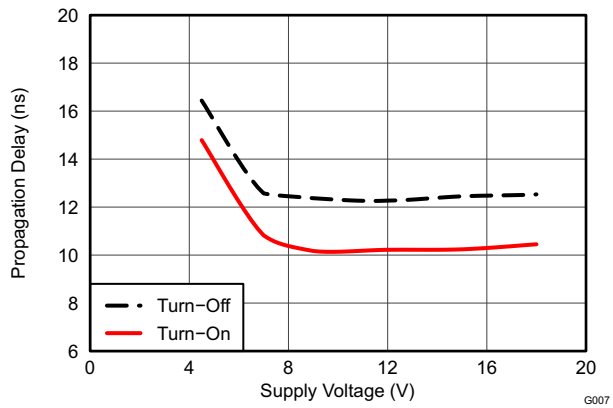


図 5-16. Propagation Delays vs Supply Voltage

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5.7 Typical Characteristics (continued)

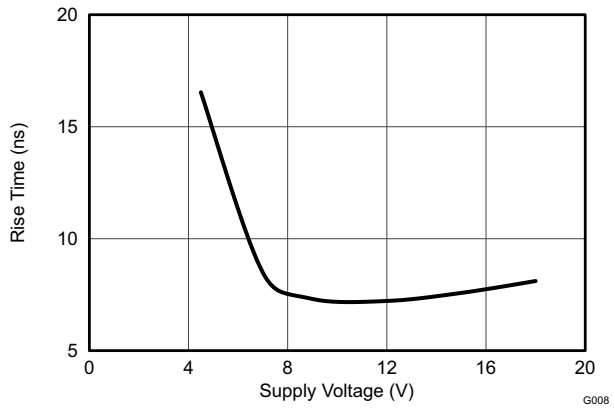


図 5-17. Rise Time vs Supply Voltage

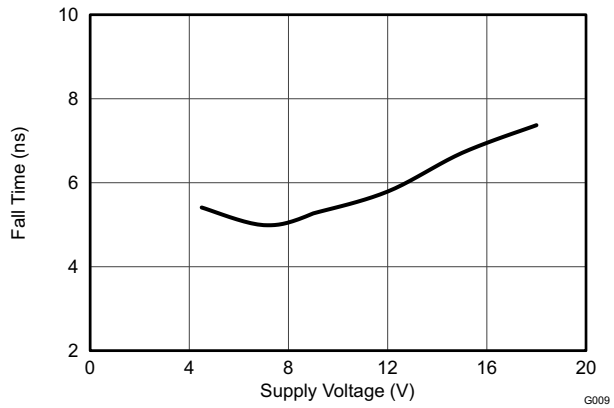


図 5-18. Fall Time vs Supply Voltage

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6 Detailed Description

6.1 Overview

The UCC27511A-Q1 single-channel high-speed low-side gate-driver device is capable of effectively driving MOSFET and IGBT power switches. Using a design that inherently minimizes shoot-through current, the UCC27511A-Q1 device is capable of sourcing and sinking high peak-current pulses into capacitive loads offering rail-to-rail drive capability and extremely small propagation delay of 13 ns (typical).

The UCC27511A-Q1 device provides 4-A source, 8-A sink (asymmetrical drive) peak-drive current capability. Strong sink capability in asymmetrical drive boosts immunity against parasitic, Miller turnon effect. The UCC27511A-Q1 device also features a unique split output configuration where the gate-drive current is sourced through the OUTH pin and sunk through the OUTL pin. This unique pin arrangement allows the user to apply independent turnon and turnoff resistors to the OUTH and OUTL pins (respectively) and easily control the switching slew rates.

Alternatively the OUTH and OUTL pins can be tied together, which results in a typical gate driver output configuration where the source and sink currents are delivered from the same pin. In case of UCC27511A-Q1 device, the state of the device's output is simply determined by the combined states of the OUTH and OUTL pins when tied together. Output high implies that OUTH pin is pulled close to V_{DD} pin bias voltage while OUTL pin is in high-impedance state. Similarly output low implies that OUTL pin is pulled close to the GND pin while OUTH pin is in high-impedance state. OUTH pulled to VDD, while OUTL pulled to GND pin simultaneously is not a valid state for the device.

The UCC27511A-Q1 device is designed to operate over a wide V_{DD} range of 4.5 to 18 V and wide temperature range of –40°C to 140°C. Internal undervoltage lockout (UVLO) circuitry on the V_{DD} pin holds the output low outside V_{DD} operating range. The capability to operate at low voltage levels, such as below 5 V, along with best-in-class switching characteristics, is especially suited for driving emerging wide band-gap power-switching devices such as GaN power-semiconductor devices.

The UCC27511A-Q1 device features a dual-input design which offers flexibility of implementing both inverting (IN– pin) and non-inverting (IN+ pin) configuration with the same device. Either the IN+ or IN– pin can be used to control the state of the driver output. The unused input pin can be used for enable and disable functions. For system robustness, internal pullup and pulldown resistors on the input pins ensure that outputs are held low when the input pins are in floating condition. Therefore the unused input pin is not left floating and must be properly biased to ensure that driver output is in enabled for normal operation.

The input pin threshold of the UCC27511A-Q1 device is based on TTL and CMOS-compatible low-voltage logic which is fixed and independent of the V_{DD} supply voltage. Wide hysteresis between the high and low thresholds offers excellent noise immunity.

表 6-1. UCC27511A-Q1 Device Summary

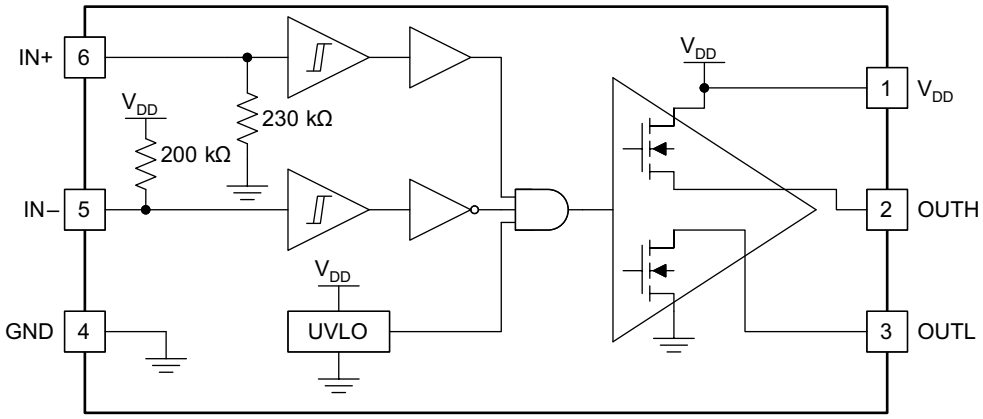
PART NUMBER	PACKAGE	PEAK CURRENT (SOURCE, SINK)	INPUT THRESHOLD LOGIC
UCC27511A-Q1DBV	SOT-23, 6 pin	4-A, 8-A (Asymmetrical Drive)	CMOS/TTL-Compatible (low voltage, independent of V_{DD} bias voltage)

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表 6-2. UCC27511A-Q1 Features and Benefits

FEATURE	BENEFIT
High source and sink current capability 4 A and 8 A (Asymmetrical) – UCC27511A-Q1 device	High current capability offers flexibility in employing UCC2751x family of devices to drive a variety of power switching devices at varying speeds
best-in-class 13-ns (typ) propagation delay	Extremely low pulse-transmission distortion
Expanded V_{DD} Operating range of 4.5 V to 18 V	Flexibility in system design Low V_{DD} operation ensures compatibility with emerging wide band-gap power devices such as GaN
Expanded operating temperature range of –40°C to 140°C (See the セクション 5.5 table)	
V_{DD} UVLO Protection	Outputs are held low in UVLO condition, which ensures predictable glitch-free operation at power up and power down
Outputs held low when input pins (INx) in floating condition	Enables the device to pass abnormal-condition system tests and delivers robust operation
Input pin voltage thresholds are independent of V_{DD}. Input pins can withstand voltages greater than V_{DD}.	System simplification, especially related to auxiliary bias supply architecture
Split output structure in the UCC27511A-Q1 device (OUTH, OUTL)	Allows independent optimization of turnon and turnoff speeds
Strong sink current (8 A) and low pulldown impedance (0.375 Ω) in the UCC27511A-Q1 device	High immunity to C x dV/dt Miller turnon events
CMOS/TTL compatible input-threshold logic with wide hysteresis in the UCC27511A-Q1 device	Enhanced noise immunity, while retaining compatibility with microcontroller logic-level input signals (3.3 V, 5 V) optimized for digital power

6.2 Functional Block Diagram



6.3 Feature Description

In the following sections, the term *output*, or *OUT* refers to the combined state that results when the OUTH pin is tied directly to the OUTL pin. As stated earlier, *output high*, or *OUT high* refers to the state when the OUTH pin is pulled close to V_{DD} pin bias voltage while the OUTL pin is in high-impedance state. Similarly *output low* or *OUT low* implies that the OUTL pin is pulled close to the GND pin while the OUTH pin is in high-impedance state.

6.3.1 V_{DD} and Undervoltage Lockout

The UCC27511A-Q1 device has and internal undervoltage-lockout (UVLO) protection feature on the V_{DD} pin supply circuit blocks. Whenever the driver is in UVLO condition (for example when the V_{DD} voltage is less than $V_{(ON)}$ during power up and when the V_{DD} voltage is less than $V_{(OFF)}$ during power down), this circuit holds all outputs low, regardless of the status of the inputs. The UVLO is typically 4.2 V with 300-mV typical hysteresis. This hysteresis prevents chatter when low V_{DD} supply voltages have noise from the power supply and also when there are droops in the V_{DD} bias voltage when the system commences switching and a sudden increase in I_{DD} occurs. The capability to operate at low voltage levels such as below 5 V, along with best-in-class switching characteristics, is especially suited for driving emerging GaN wide band-gap power-semiconductor devices.

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For example, at power up, the UCC27511A-Q1 driver output remains LOW until the V_{DD} voltage reaches the UVLO threshold. The magnitude of the OUT signal rises with V_{DD} until steady-state V_{DD} is reached. In the non-inverting operation (PWM signal applied to IN+ pin) shown in 図 6-1, the output remains LOW until the UVLO threshold is reached, and then the output is IN–phase with the input. In the inverting operation (PWM signal applied to IN– pin) shown in 図 6-2 the output remains low until the UVLO threshold is reached, and then the output is out-phase with the input. In both cases, the unused input pin must be properly biased to enable the output. Note that in these devices the output turns to high state only if the IN+ pin is high and the IN– pin is low after the UVLO threshold is reached.

Because the driver draws current from the V_{DD} pin to bias all internal circuits, for the best high-speed circuit performance, two V_{DD}-bypass capacitors are recommended to prevent noise problems. The use of surface-mount components is highly recommended. A 0.1-µF ceramic capacitor should be located as close as possible to the V_{DD} to GND pins of the gate driver. In addition, to help deliver the high-current peaks required by the load, a larger capacitor (such as one with a value of 1 µF) with relatively low ESR should be connected in parallel and close proximity. The parallel combination of capacitors should present a low impedance characteristic for the expected current levels and switching frequencies in the application.

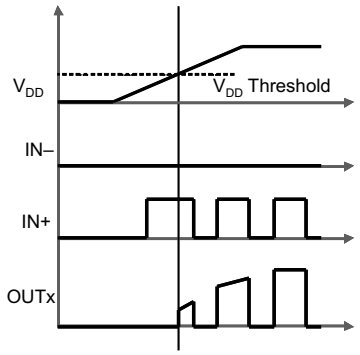


図 6-1. Power-Up (Non-Inverting Drive)

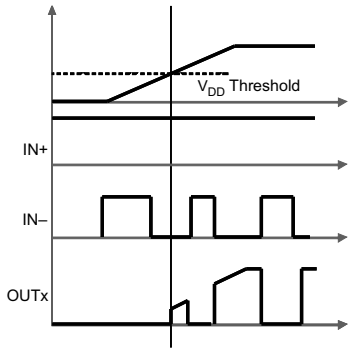


図 6-2. Power-Up (Inverting Drive)

6.3.2 Operating Supply Current

The UCC27511A-Q1 device features very low quiescent I_{DD} currents. The typical operating-supply current in undervoltage-lockout (UVLO) state and fully-on state (under static and switching conditions) are summarized in 図 5-5, 図 5-6 and 図 5-7. The I_{DD} current when the device is fully on and outputs are in a static state (DC high or DC low, refer 図 5-7) represents lowest quiescent I_{DD} current when all the internal logic circuits of the device are fully operational. The total supply current is the sum of the quiescent I_{DD} current, the average I_O current because of switching, and finally any current related to pullup resistors on the unused input pin. For example, when the inverting input pin is pulled low additional current is drawn from the V_{DD} supply through the pullup resistors (see セクション 6.2). Knowing the operating frequency (f_S) and the MOSFET gate (Q_G) charge at the drive voltage being used, the average I_O current can be calculated as product of Q_G and f_S.

A complete characterization of the I_{DD} current as a function of switching frequency at different V_{DD} bias voltages under 1.8-nF switching load is provided in 図 5-15. The strikingly linear variation and close correlation with the theoretical value of the average I_O indicates negligible shoot-through inside the gate-driver device attesting to the high-speed characteristics.

6.3.3 Input Stage

The input pins of the UCC27511A-Q1 device is based on a TTL and CMOS compatible input-threshold logic that is independent of the V_{DD} supply voltage. With a typically high threshold of 2.2 V and a typically low threshold of 1.2 V, the logic-level thresholds can be conveniently driven with PWM control signals derived from 3.3-V and 5-V digital-power controllers. Wider hysteresis (1 V typical) offers enhanced noise immunity compared to traditional TTL-logic implementations, where the hysteresis is typically less than 0.5 V. This device also feature tight control of the input-pin threshold-voltage levels which eases system design considerations and ensures stable operation

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across temperature. The very-low input capacitance on these pins reduces loading and increases switching speed.

Whenever any of the input pins are in a floating condition, the output of the respective channel is held in the low state. This function is achieved using V_{DD}-pullup resistors on all the inverting inputs (IN– pin) or GND-pulldown resistors on all the non-inverting input pins (IN+ pin), (see セクション 6.2).

The device also features a dual-input configuration with two input pins available to control the state of the output. The user has the flexibility to drive the device using either a non-inverting input pin (IN+) or an inverting input pin (IN–). The state of the output pin is dependent on the bias on both the IN+ and IN– pins. For additional clarification, refer to the I/O-logic truth table (表 6-3) and the typical application diagrams, (図 6-4 and 図 6-5).

When an input pin is selected for PWM drive, the other input pin (the *unused* input pin) must be properly biased in order to enable the output. As previously stated, the *unused* input pin cannot remain in a floating condition because whenever any input pin is left in a floating condition the output is disabled. Alternatively, the *unused* input pin can effectively be used to implement an enable or disable function. The following explains this function:

- In order to drive the device in a non-inverting configuration, apply the PWM-control input signal to IN+ pin. In this case, the *unused* input pin, IN–, must be biased low (such as tied to GND) in order to enable the output.
  - Alternately, the IN– pin is used to implement the enable or disable function using an external logic signal. OUT is disabled when IN– is biased high and OUT is enabled when IN– is biased low.
- In order to drive the device in an inverting configuration, apply the PWM-control input signal to IN– pin. In this case, the *unused* input pin, IN+, must be biased high (such as tied to V_{DD}) in order to enable the output.
  - Alternately, the IN+ pin is used to implement the enable or disable function using an external logic signal. OUT is disabled when IN+ is biased low and OUT is enabled when IN+ is biased high.
- Finally, note that the output pin can be driven into a high state **only** when the IN+ pin is biased high and the IN– input is biased low.

The input stage of the driver is preferably driven by a signal with a short rise or fall time. Use caution whenever the driver is used with slowly varying input signals, especially in situations where the device is located in a mechanical socket or PCB layout that is not optimal:

- High dI/dt current from the driver output coupled with board layout parasitics can cause ground bounce. The differential voltage between input pins and GND is modified and triggers an unintended change of output state because of fast 13-ns propagation delay which can ultimately result in high-frequency oscillations that increase power dissipation and pose a risk of damage to the device.
- A 1-V input-threshold hysteresis boosts noise immunity compared to most other industry standard drivers.
- In the worst case, when a slow input signal is used and PCB layout is not optimal, adding a small capacitor (1 nF) between the input pin and GND pin very close to the driver device may be necessary which helps to convert the differential mode noise with respect to the input-logic circuitry into common-mode noise and avoid unintended change of output state.

If limiting the rise or fall times to the power device is the primary goal, then an external resistance is highly recommended between the output of the driver and the power device instead of adding delays on the input signal. This external resistor has the additional benefit of reducing part of the gate-charge related power dissipation in the gate-driver device package and transferring the power dissipation into the external resistor.

6.3.4 Enable Function

As mentioned earlier, an enable and disable function is easily implemented in UCC27511A-Q1 device using the *unused* input pin. When the IN+ pin is pulled down to GND or the IN– pin is pulled down to V_{DD}, the output is disabled. Thus the IN+ pin can be used like an enable pin that is based on active-high logic, while the IN– pin can be used like an enable pin that is based on active-low logic.

6.3.5 Output Stage

図 6-3 shows the output stage of the UCC27511A-Q1 device. The UCC27511A-Q1 device features a unique architecture on the output stage which delivers the highest peak-source current when the peak source current is

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most needed during the Miller plateau region of the power switch turnon transition (when the power-switch drain or collector voltage experiences dV/dt). The device output stage features a hybrid pullup structure using a parallel arrangement of N-channel and P-channel MOSFET devices. By turning on the N-channel MOSFET during a narrow instant when the output changes state from low to high, the gate-driver device is able to deliver a brief boost in the peak-sourcing current enabling fast turnon.

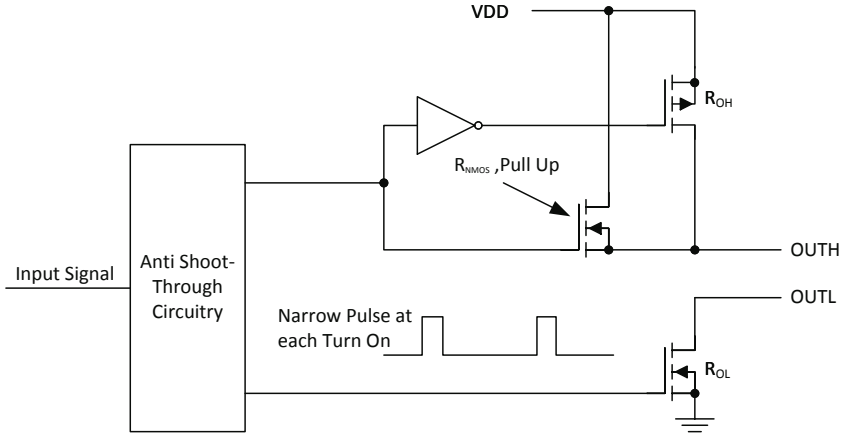


図 6-3. UCC27511A-Q1 Gate Driver Output Structure

The $R_{O(H)}$ parameter (see the セクション 5.5 table) is a DC measurement and is representative of the on-resistance of the P-channel device only, because the N-Channel device is turned on only during output change of state from low to high. Thus the effective resistance of the hybrid pullup stage is much lower than what is represented by $R_{O(H)}$ parameter. The pulldown structure is composed of a N-channel MOSFET only. The $R_{O(L)}$ parameter (see the セクション 5.5 table), which is also a DC measurement, is representative of true impedance of the pulldown stage in the device. In the UCC27511A-Q1 device, the effective resistance of the hybrid pullup structure is approximately 2.7 × $R_{O(L)}$.

The UCC27511A-Q1 device features a unique split output configuration where the gate-drive current is sourced through the OUTH pin and sunk through the OUTL pin. This unique pin arrangement allows users to apply independent turnon and turnoff resistors to the OUTH and OUTL pins respectively and easily control the turnon and turnoff switching dV/dt. This pin arrangement, along with the low pulldown impedance of the output driver stage, is especially useful in applications where a high C × dV/dt Miller turnon immunity is needed (such as with GaN power switches, SR MOSFETs and other applications) and the OUTL pin can be directly tied to the gate of the power device.

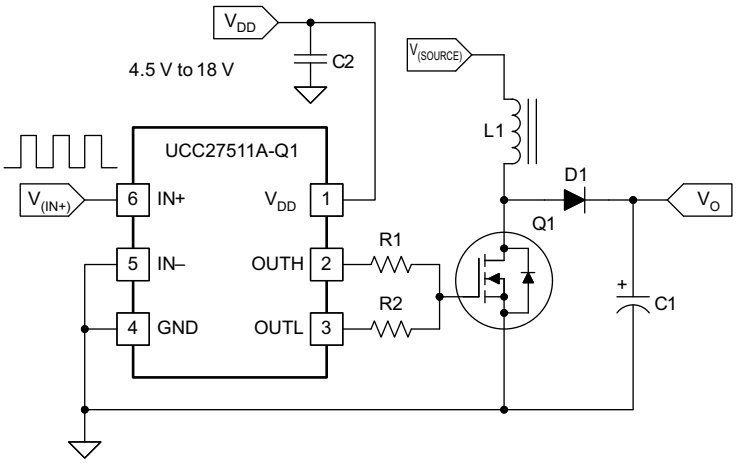


図 6-4. Using Non-Inverting Input (IN– Is Grounded To Enable Output)

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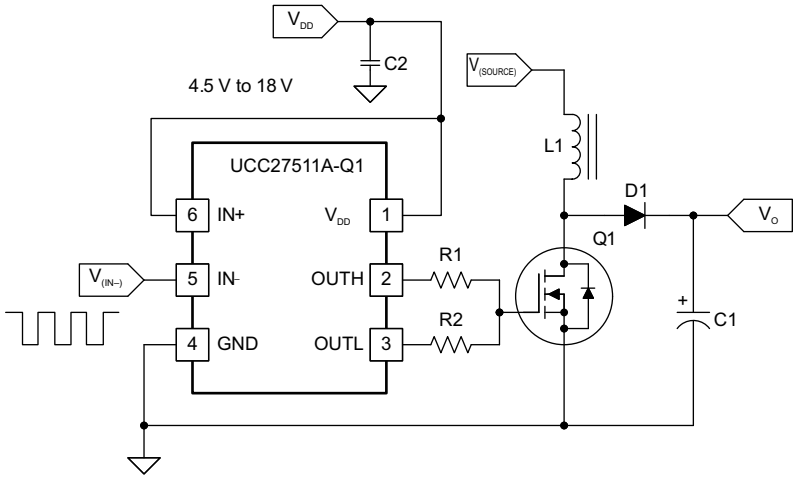


図 6-5. Using Inverting Input (IN+ Is Tied To V_{DD} Enable Output)

The UCC27511A-Q1 device is capable of delivering 4-A source, 8-A sink (asymmetrical drive) at V_{DD} equal to 12 V. Strong sink capability in asymmetrical drive results in a very-low pulldown impedance in the driver output stage which boosts immunity against parasitic, Miller turnon (C × dV/dt turnon) effect, especially where the low gate-charge MOSFETs or emerging wide band-gap GaN-power switches are used.

An example of a situation where the Miller turnon effect is a concern is synchronous rectification (SR). In an SR application, the dV/dt occurs on the MOSFET drain when the MOSFET is already held in off state by the gate driver. The current discharging the $C_{(GD)}$ Miller capacitance during this dV/dt is shunted by the pulldown stage of the driver. If the pulldown impedance is not low enough then a voltage spike can result in the V_{GS} of the MOSFET, which can result in spurious turnon. This phenomenon is shown in 図 6-6. The UCC27511A-Q1 device offers a best-in-class, 0.375-Ω (typ) pulldown impedance boosting immunity against Miller turnon.

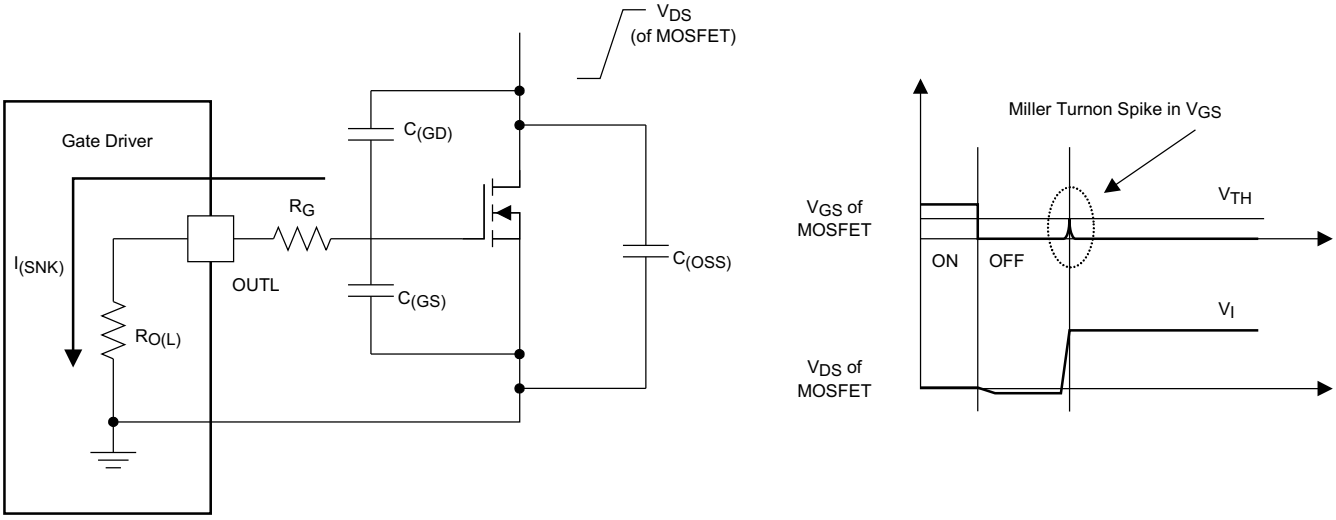


図 6-6. Very-Low Pulldown Impedance in UCC27511A-Q1, 4-A and 8-A Asymmetrical Drive (Output Stage Mitigates Miller Turnon Effect)

The driver-output voltage swings between the V_{DD} and GND pins which provides rail-to-rail operation as a result of the MOS-output stage which delivers very-low dropout. The presence of the MOSFET-body diodes also offers low impedance to switching overshoots and undershoots. In many cases, external Schottky diode clamps are eliminated. The outputs of these drivers are designed to withstand 500-mA reverse current without either damage to the device or logic malfunction.

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6.3.6 Low Propagation Delays

The UCC27511A-Q1 driver device features best-in-class input-to-output propagation delay of 13 ns (typical) at V_{DD} equal to 12 V, which promises the lowest level of pulse transmission distortion available from industry-standard gate-driver devices for high-frequency switching applications. As shown in 図 5-14, very little variation in propagation delay occurs with temperature and supply voltage, offering typically less than 20-ns propagation delays across the entire range of application conditions.

6.4 Device Functional Modes

The device operates in normal mode and UVLO mode. See セクション 6.3.1 for information on UVLO operation mode. In the normal mode the output state is dependent on states of the IN+ and IN– pins. 表 6-3 lists the output states for different input pin combinations.

表 6-3. Device Logic Table

IN+ PIN	IN– PIN	OUTH PIN	OUTL PIN	OUT (OUTH AND OUTL PINS TIED TOGETHER IN THE UCC27511A-Q1)
L	L	High impedance	L	L
L	H	High impedance	L	L
H	L	H	High impedance	H
H	H	High impedance	L	L
x(1)	Any	High impedance	L	L
Any	x(1)	High impedance	L	L

(1) x = Floating Condition

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7 Application and Implementation

注

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7.1 Application Information

High-current gate-driver devices are required in switching-power applications for a variety of reasons. In order to effect fast switching of power devices and reduce associated switching power losses, a powerful gate driver employs between the PWM output of controllers and the gates of the power-semiconductor devices. Further, gate drivers are indispensable when having the PWM controller directly drive the gates of the switching devices is impossible. With the advent of digital power, this situation will be encountered often encountered because the PWM signal from the digital controller is often a 3.3-V logic signal which is not capable of effectively turning on a power switch.

A level-shifting circuitry is needed to boost the 3.3-V signal to the gate-drive voltage (such as 12 V) in order to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN and PNP bipolar transistors in totem-pole arrangement, being emitter follower configurations, prove inadequate with digital power because these circuits lack level-shifting capability. Gate drivers effectively combine both the level-shifting and buffer-drive functions. Gate drivers also satisfy other needs such as minimizing the effect of high-frequency switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power-device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses into the controller.

Finally, emerging wide bandgap power device technologies, such as GaN based switches, which are capable of supporting very high switching frequency operation, are driving very special requirements in terms of gate drive capability. These requirements include operation at low V_{DD} voltages (5 V or lower), low propagation delays and availability in compact, low-inductance packages with good thermal capability. In summary gate-driver devices are extremely important components in switching power combining benefits of high-performance low-cost component count and board-space reduction and simplified system design.

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7.2 Typical Application

図 7-1 shows the typical application of UCC27511A-Q1 device when used as a gate driver for the power MOSFET in a boost-converter application (for example, AC-DC power factor correction in AC-DC chargers for electric vehicles). In this application the UCC27511A-Q1 device is used in the non-inverting input configuration.

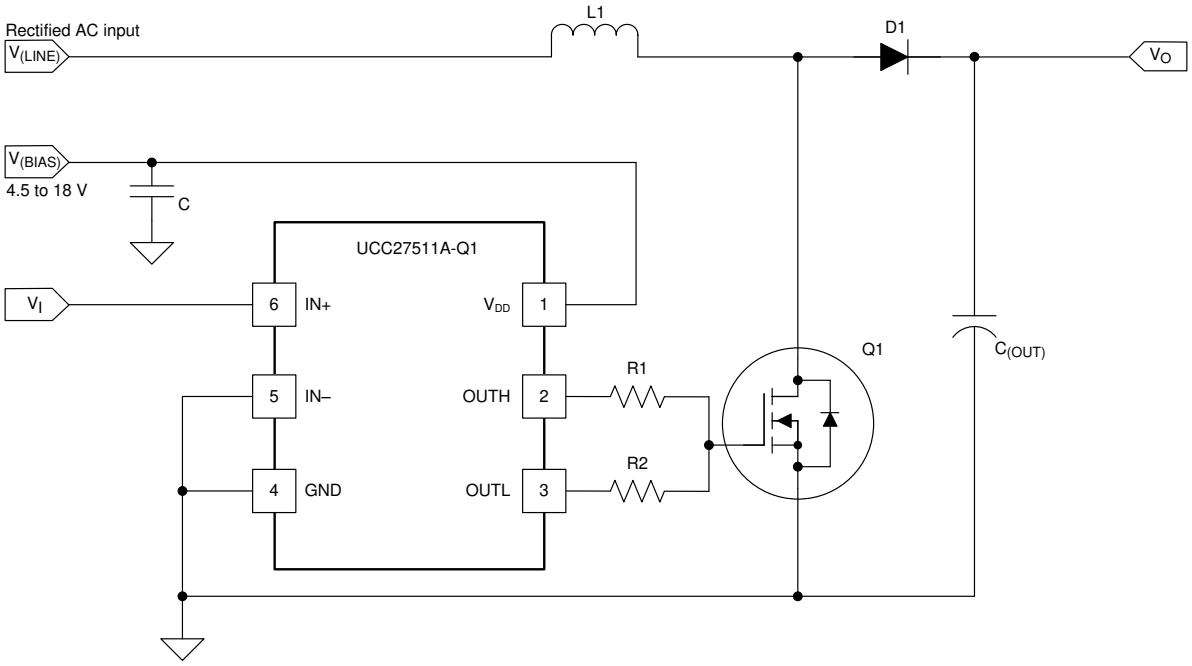


図 7-1. Typical Application in PFC Power Stage

7.2.1 Design Requirements

When selecting the proper gate driver device for an end application, some design considerations must be evaluated first in order to make the most appropriate selection. Among these considerations are input-to-output configuration, the input threshold type, bias supply voltage levels, peak source and sink currents, availability of independent enable and disable functions, propagation delay, power dissipation, and package type.

7.2.2 Detailed Design Procedure

7.2.2.1 Input-to-Output Logic

The design should specify which type of input-to-output configuration should be used. If turning on the power MOSFET or IGBT when the input signal is in high state is preferred, then the non-inverting configuration must be selected. If turning off the power MOSFET or IGBT when the input signal is in high state is preferred, the inverting configuration must be chosen. The UCC27511A-Q1 device can be configured in either an inverting or non-inverting input-to-output configuration using the IN– or IN+ pins respectively. To configure the device for use in inverting mode, tie the IN+ pin to V_{DD} and apply the input signal to the IN– pin. For the non-inverting configuration, tie the IN– pin to GND and apply the input signal to the IN+ pin.

7.2.2.2 Input Threshold Type

The type of Input voltage threshold determines the type of controller that can be used with the gate driver device. The UCC27511A-Q1 device features a TTL and CMOS-compatible input threshold logic, with wide hysteresis. The threshold voltage levels are low voltage and independent of the V_{DD} supply voltage, which allows compatibility with both logic-level input signals from microcontrollers as well as higher-voltage input signals from analog controllers. See the セクション 5.5 table for the actual input threshold voltage levels and hysteresis specifications for the UCC27511A-Q1 device.

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7.2.2.3 V_{DD} Bias Supply Voltage

The bias supply voltage to be applied to the V_{DD} pin of the device should never exceed the values listed in the セクション 5.3 table. However, different power switches demand different voltage levels to be applied at the gate terminals for effective turnon and turnoff. With certain power switches, a positive gate voltage may be required for turnon and a negative gate voltage may be required for turnoff, in which case the V_{DD} bias supply equals the voltage differential. With a wide operating range from 4.5 V to 18 V, the UCC27511A-Q1 device can be used to drive a variety of power switches, such as Si MOSFETs (for example, V_{GS} = 4.5 V, 10 V, 12 V), IGBTs (V_{GE} = 15 V, 18 V), and wide-bandgap power semiconductors (such as GaN, certain types of which allow no higher than 6 V to be applied to the gate terminals).

7.2.2.4 Peak Source and Sink Currents

Generally, switching the speed of the power switch during turnon and turnoff should be as fast as possible in order to minimize switching power losses. The gate driver device must be able to provide the required peak current for achieving the targeted switching speeds for the targeted power MOSFET.

Using the example of a power MOSFET, the system requirement for the switching speed is typically described in terms of the slew rate of the drain-to-source voltage of the power MOSFET (such as dV_{DS}/dt). For example, the system requirement might state that a SPP20N60C3 power MOSFET must be turned-on with a dV_{DS}/dt of 20 V/ns or higher under a DC bus voltage of 400 V in a continuous-conduction-mode (CCM) boost PFC-converter application. This type of application is an inductive hard-switching application and reducing switching power losses is critical. This requirement means that the entire drain-to-source voltage swing during power MOSFET turn-on event (from 400 V in the OFF state to $V_{DS(on)}$ in on state) must be completed in approximately 20 ns or less. When the drain-to-source voltage swing occurs, the Miller charge of the power MOSFET (Q_{GD} parameter in SPP20N60C3 power MOSFET data sheet = 33 nC typical) is supplied by the peak current of gate driver. According to power MOSFET inductive switching mechanism, the gate-to-source voltage of the power MOSFET at this time is the Miller plateau voltage, which is typically a few volts higher than the threshold voltage of the power MOSFET, $V_{GS(TH)}$.

In order to achieve the targeted dV_{DS}/dt, the gate driver must be capable of providing the Q_{GD} charge in 20 ns or less. In other words a peak current of 1.65 A (= 33 nC / 20 ns) or higher must be provided by the gate driver. The UCC27511A-Q1 gate driver is capable of providing 4-A peak sourcing current which clearly exceeds the design requirement and has the capability to meet the switching speed needed. The 2.4x overdrive capability provides an extra margin against part-to-part variations in the Q_{GD} parameter of the power MOSFET along with additional flexibility to insert external gate resistors and fine tune the switching speed for efficiency versus EMI optimizations.

However, in practical designs the parasitic trace inductance in the gate drive circuit of the PCB will have a definitive role to play on the power MOSFET switching speed. The effect of this trace inductance is to limit the dI/dt of the output current pulse of the gate driver. In order to illustrate this, consider output current pulse waveform from the gate driver to be approximated to a triangular profile, where the area under the triangle (½ × I_{PEAK} × time) would equal the total gate charge of the power MOSFET (Q_G parameter in SPP20N60C3 power MOSFET datasheet = 87 nC typical). If the parasitic trace inductance limits the dI/dt then a situation may occur in which the full peak current capability of the gate driver is not fully achieved in the time required to deliver the QG required for the power MOSFET switching. In other words the time parameter in the equation would dominate and the I_{PEAK} value of the current pulse would be much less than the true peak current capability of the device, while the required QG is still delivered. Because of this, the desired switching speed may not be realized, even when theoretical calculations indicate the gate driver is capable of achieving the targeted switching speed. Thus, placing the gate driver device very close to the power MOSFET and designing a tight gate drive-loop with minimal PCB trace inductance is important to realize the full peak-current capability of the gate driver.

7.2.2.5 Enable and Disable Function

Certain applications demand independent control of the output state of the driver without involving the input signal. A pin which offers an enable and disable function achieves this requirement. The UCC27511A-Q1 device offers 2 input pins, IN+ and IN–, both of which control the state of the output as listed in 表 6-3. Based on

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whether an inverting or non-inverting input signal is provided to the driver, the appropriate input pin can be selected as the primary input for controlling the gate driver. The other *unused* input pin can be conveniently used for the enable and disable functionality. If the design does not require an enable function, the unused input pin can be tied to either the V_{DD} pin (in case IN+ is the unused pin), or GND (in case IN– is unused pin) in order to ensure it does not affect the output status.

7.2.2.6 Propagation Delay

The acceptable propagation delay from the gate driver is dependent on the switching frequency at which it is used and the acceptable level of pulse distortion to the system. The UCC27511A-Q1 device features industry best-in-class 13-ns (typical) propagation delays which ensures very little pulse distortion and allows operation at very high-frequencies. See the セクション 5.6 table for the propagation and switching characteristics of the UCC27511A-Q1 device.

7.2.2.7 Thermal Information

The useful range of a driver is greatly affected by the drive-power requirements of the load and the thermal characteristics of the package. In order for a gate driver to be useful over a particular temperature range the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The thermal metrics for the driver package is listed in the セクション 5.4 table. For detailed information regarding the セクション 5.4 table, refer to the Application Note from Texas Instruments entitled *IC Package Thermal Metrics*.

The UCC27511A-Q1 device is offered in a SOT-23, 6-pin package (DBV). セクション 5.4 lists the thermal performance metrics related to SOT-23 package. The ψ_{JT} and ψ_{JB} metrics are used when estimating the die temperature during actual application measurements.

Heat removal occurs primarily through the leads of the device and the PCB traces connected to the leads.

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7.2.2.8 Power Dissipation

Power dissipation of the gate driver has two portions as shown in 式 1.

$$P_D = P_{D(DC)} + P_{D(SW)} \quad (1)$$

where

- P_D is the power dissipation
- $P_{D(DC)}$ is the DC portion of the power dissipation
- $P_{D(SW)}$ is the power dissipated in the gate-driver package during switching

Use 式 2 to calculate the DC portion of the power dissipation.

$$P_{P(DC)} = I_Q \times V_{DD} \quad (2)$$

where

- I_Q is the quiescent current for the driver

The quiescent current is the current consumed by the device to bias all internal circuits such as input stage, reference voltage, logic circuits, protections, and also any current associated with switching of internal devices when the driver output changes state (such as charging and discharging of parasitic capacitances, parasitic shoot-through, and others). The UCC27511A-Q1 device features very low quiescent currents (less than 1 mA, see 図 5-7) and contains internal logic to eliminate any shoot-through in the output driver stage. Thus the effect of the $P_{D(DC)}$ on the total power dissipation within the gate driver can be assumed to be negligible.

The power dissipated in the gate-driver package during switching ($P_{D(SW)}$) depends on the following factors:

- The gate charge required of the power device (usually a function of the drive voltage V_G, which is very close to input bias supply voltage V_{DD} because of low $V_{O(H)}$ drop-out).
- The switching frequency (f_S)
- Use of external gate resistors ($R_{(GATE)}$)

When a driver device is tested with a discrete, capacitive load calculating the power that is required from the bias supply is fairly simple. The energy to charge the capacitor is given by 式 3.

$$E_G = \frac{1}{2} C_{(LOAD)} \times V_{DD}^2 \quad (3)$$

Where

- $C_{(LOAD)}$ is load capacitor
- V_{DD} is bias voltage feeding the driver
- E_G is the energy stored in the capacitor when it is charged to V_{DD}

An equal amount of energy dissipates when the capacitor is charged which leads to a total power loss given by 式 4.

$$P_{tot} = C_{(LOAD)} \times V_{DD}^2 \times f_S \quad (4)$$

where

- P_{tot} is the total power loss
- f_S is the switching frequency

The switching load presented by a power MOSFET or IGBT is converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches

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between the ON and OFF states. Most manufacturers provide specifications of typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge, Q_G, determine the power that must be dissipated when charging a capacitor (calculated using 式 5, to provide 式 6).

$$Q_G = C_{(LOAD)} \times V_{DD} \tag{5}$$

$$P_{tot} = C_{(LOAD)} \times V_{DD}^2 \times f_S = Q_G \times V_{DD} \times f_S \tag{6}$$

This power, P_{tot}, is dissipated in the resistive elements of the circuit when the MOSFET or IGBT is being turned on or off. Half of the total power is dissipated when the load capacitor is charged during turnon, and the other half is dissipated when the load capacitor is discharged during turnoff. When no external gate resistor is employed between the driver and MOSFET or IGBT, this power is completely dissipated inside the driver package. With the use of external gate-drive resistors, the power dissipation is shared between the internal resistance of driver and external gate resistor in accordance to the ratio of the resistance (more power dissipated in the higher resistance component). Based on this simplified analysis, the driver power dissipation during switching is calculated in 式 7.

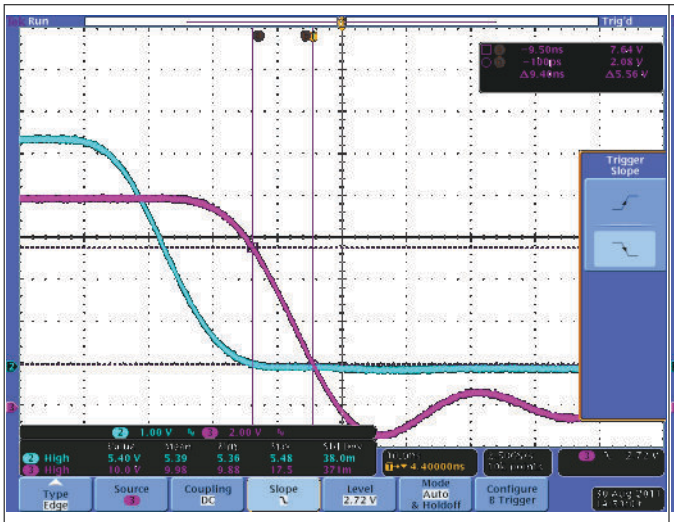
$$P_{D(SW)} = 0.5 \times Q_G \times V_{DD} \times f_S \times \left(\frac{R_{(OFF)}}{R_{(OFF)} + R_{(GATE)}} + \frac{R_{(ON)}}{R_{(ON)} + R_{(GATE)}} \right) \tag{7}$$

where

- $R_{(OFF)} = R_{O(L)}$
- $R_{(ON)}$ (effective resistance of pullup structure) = 2.7 × $R_{O(L)}$

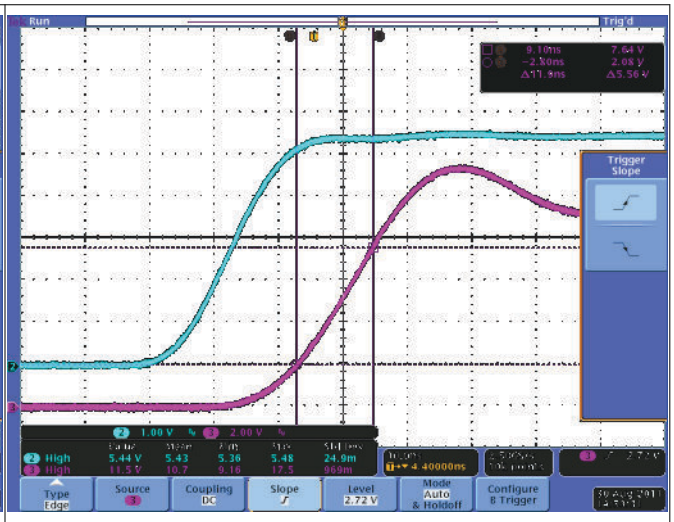
7.2.3 Application Curves

図 7-2 and 図 7-3 show the typical switching characteristics of the UCC27511A-Q1 device.



V_{DD} = 10 V $C_{(LOAD)}$ = 1 nF

図 7-2. Typical Turnon Waveform



V_{DD} = 10 V $C_{(LOAD)}$ = 1 nF

図 7-3. Typical Turnoff Waveform

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8 Power Supply Recommendations

The bias supply voltage range for which the UCC27511A-Q1 device is rated to operate is from 4.5 V to 18 V. The lower end of this range is governed by the internal undervoltage-lockout (UVLO) protection feature on the V_{DD} pin supply circuit blocks. Whenever the driver is in UVLO condition when the V_{DD} pin voltage is below the $V_{(ON)}$ supply start threshold, this feature holds the output low, regardless of the status of the inputs. The upper end of this range is driven by the 20-V absolute maximum voltage rating of the V_{DD} pin of the device (which is a stress rating). Keeping a 2-V margin to allow for transient voltage spikes, the maximum recommended voltage for the V_{DD} pin is 18 V.

The UVLO protection feature also involves a hysteresis function. This means that when the V_{DD} pin bias voltage has exceeded the threshold voltage and device begins to operate, and if the voltage drops, then the device continues to deliver normal functionality unless the voltage drop exceeds the hysteresis specification $V_{DD(hys)}$. Therefore, ensuring that, while operating at or near the 4.5V range, the voltage ripple on the auxiliary power supply output is smaller than the hysteresis specification of the device is important to avoid triggering device shutdown.

During system shutdown, the device operation continues until the V_{DD} pin voltage has dropped below the $V_{(OFF)}$ threshold which must be accounted for while evaluating system shutdown timing design requirements. Likewise, at system startup, the device does not begin operation until the V_{DD} pin voltage has exceeded above the $V_{(ON)}$ threshold.

The quiescent current consumed by the internal circuit blocks of the device is supplied through the V_{DD} pin. Although this fact is well known, recognizing that the charge for source current pulses delivered by the OUTH pin is also supplied through the same V_{DD} pin is important. As a result, every time a current is sourced out of the output pins (OUTH), a corresponding current pulse is delivered into the device through the V_{DD} pin. Thus ensuring that local bypass capacitors are provided between the V_{DD} and GND pins and located as close to the device as possible for the purpose of decoupling is important. A low ESR, ceramic surface mount capacitor is a must. TI recommends to have 2 capacitors; a 100-nF ceramic surface-mount capacitor which can be nudged very close to the pins of the device and another surface-mount capacitor of few microfarads added in parallel.

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9 Layout

9.1 Layout Guidelines

Proper PCB layout is extremely important in a high-current fast-switching circuit to provide appropriate device operation and design robustness. The UCC27511A-Q1 gate driver incorporates short-propagation delays and powerful output stages capable of delivering large current peaks with very fast rise and fall times at the gate of power switch to facilitate voltage transitions very quickly. At higher V_{DD} voltages, the peak-current capability is even higher (4-A/8-A peak current is at V_{DD} equal to 12 V). Very high di/dt causes unacceptable ringing if the trace lengths and impedances are not well controlled. The following circuit-layout guidelines are strongly recommended when designing with these high-speed drivers.

- Place the driver device as close as possible to power device in order to minimize the length of high-current traces between the output pins and the gate of the power device.
- Place the V_{DD}-bypass capacitors between the V_{DD} pin and GND as close as possible to the driver with minimal trace length to improve the noise filtering. These capacitors support high-peak current being drawn from V_{DD} during turnon of power MOSFET. The use of low inductance surface-mount components such as chip resistors and chip capacitors is highly recommended.
- The turnon and turnoff current-loop paths (driver device, power MOSFET, and V_{DD} bypass capacitor) should be minimized as much as possible in order to keep the stray inductance to a minimum. High dI/dt is established in these loops at two instances – during turnon and turnoff transients, which will induce significant voltage transients on the output pin of the driver device and gate of the power switch.
- Wherever possible, parallel the source and return traces, taking advantage of flux cancellation.
- Separate power traces and signal traces, such as the output and input signals.
- Minimize noise coupling from one current loop to another with star-point grounding or other techniques. The GND of the driver should be connected to the other circuit nodes such as source of power switch, ground of PWM controller, and others at one single point. The connected paths should be as short as possible to reduce inductance and be as wide as possible to reduce resistance.
- Use a ground plane to provide noise shielding. Fast rise and fall times at OUT may corrupt the input signals during transition. The ground plane must not be a conduction path for any current loop. Instead the ground plane must be connected to the star-point with one single trace to establish the ground potential. In addition to noise shielding, the ground plane can help in power dissipation as well.
- In noisy environments, tying the unused Input pin of UCC27511A-Q1 device to the V_{DD} (in case of IN+) pin or GND (in case of IN–) using short traces in order to ensure that the output is enabled and to prevent noise from causing malfunction in the output may be necessary.

9.2 Layout Example

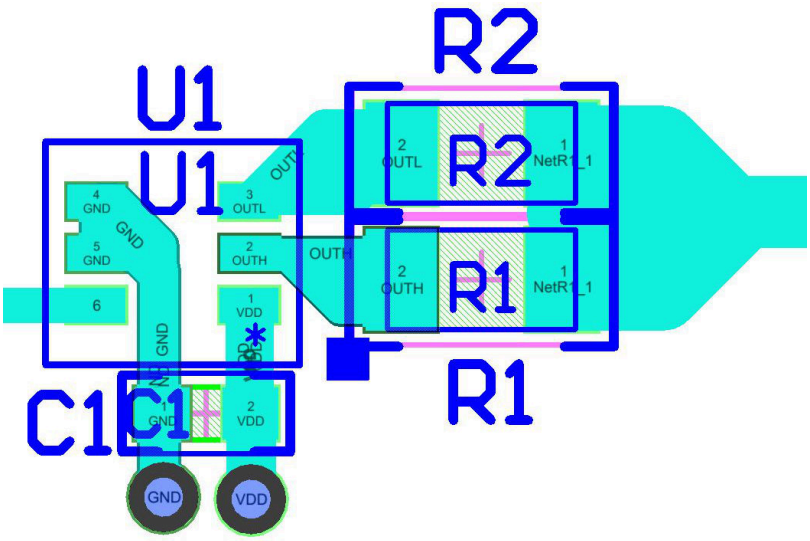


図 9-1. UCC27511A-Q1 Layout Example

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10 Device and Documentation Support

10.1 Device Support

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11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (September 2014) to Revision B (January 2024)	Page
• 「特長」の立ち上がり時間を 9ns から 8ns に変更	1

Changes from Revision * (August 2014) to Revision A (September 2014)	Page
• 製品ステータスを「製品プレビュー」から「量産」に変更	1
• Changed ESD HBM Values From: MIN rev= -2000 V, MAX = 2000 V To: MIN = -4000 V, MAX = 4000 V	4

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC27511AQDBVRQ1	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	EAKQ
UCC27511AQDBVRQ1.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	EAKQ
UCC27511AQDBVRQ1.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	EAKQ

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(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

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(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF UCC27511A-Q1 :

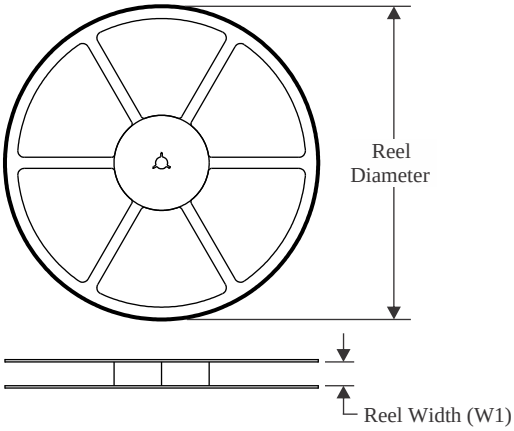
- Catalog : UCC27511A

NOTE: Qualified Version Definitions:

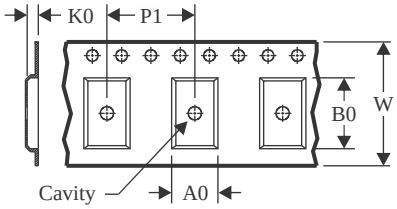
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

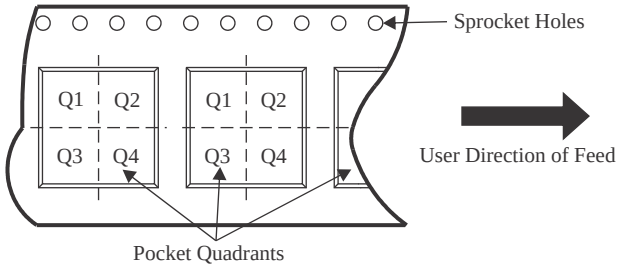


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

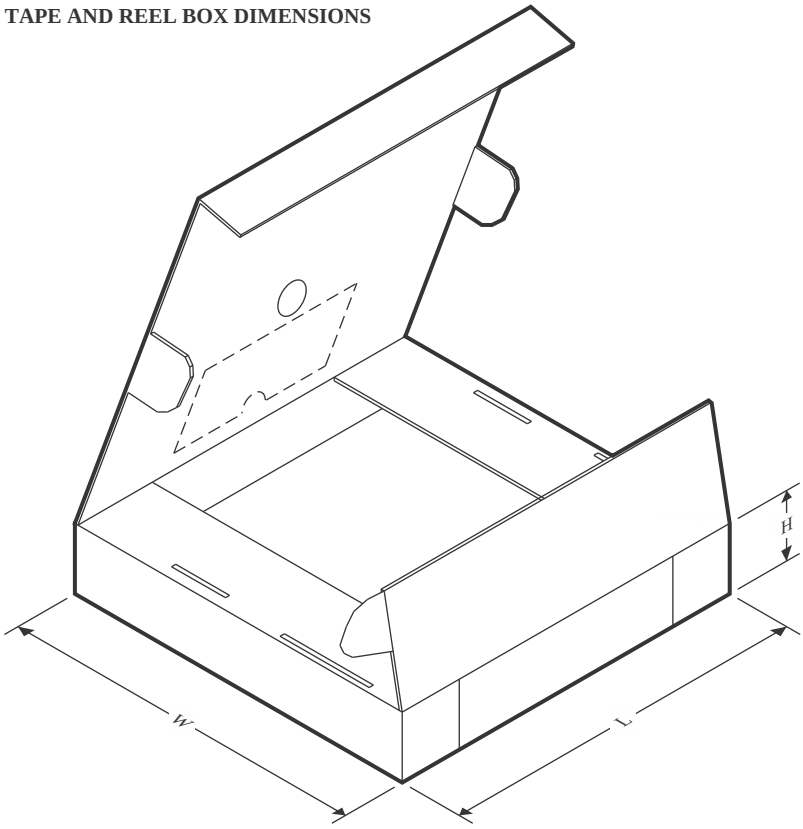
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27511AQDBVRQ1	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

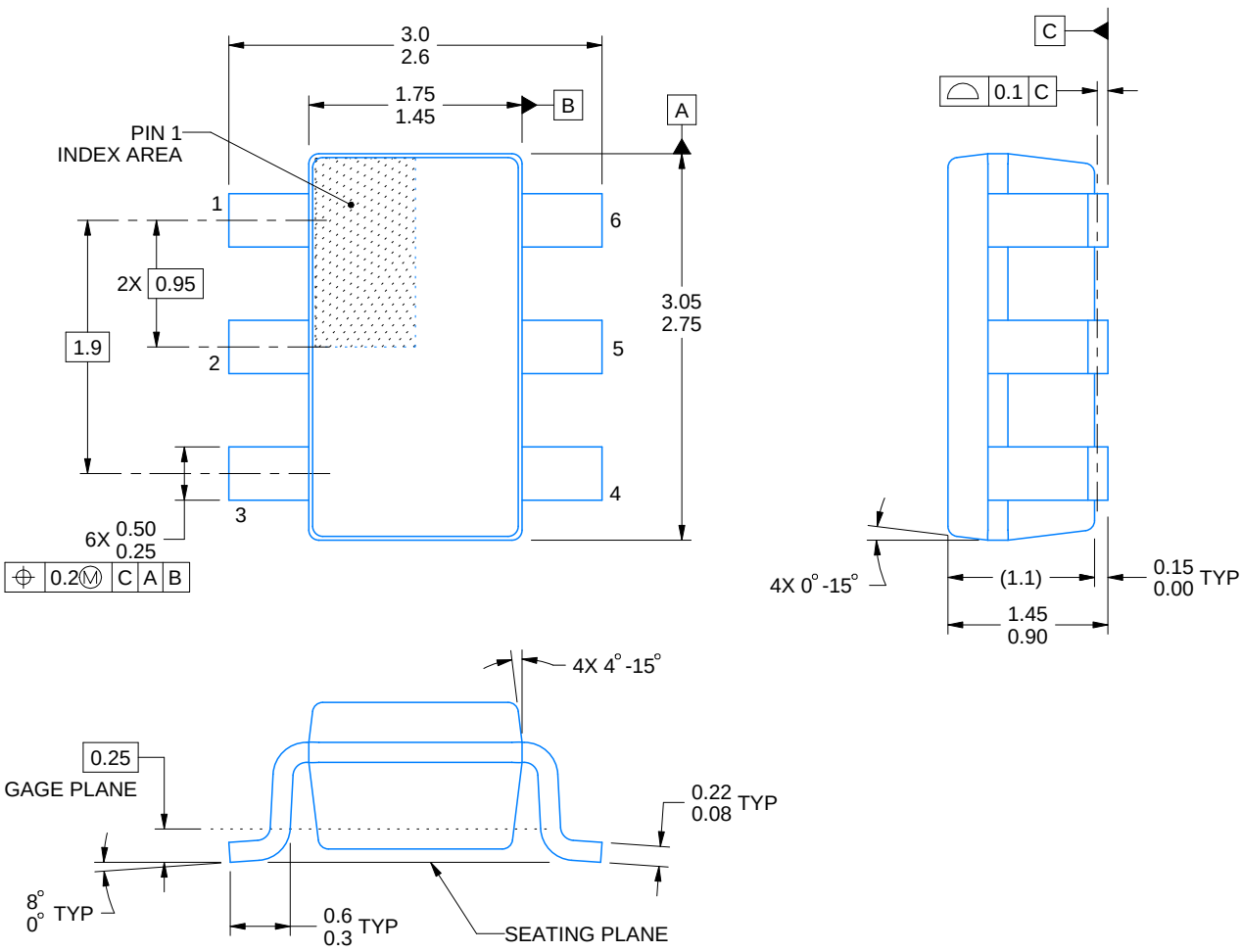
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27511AQDBVRQ1	SOT-23	DBV	6	3000	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

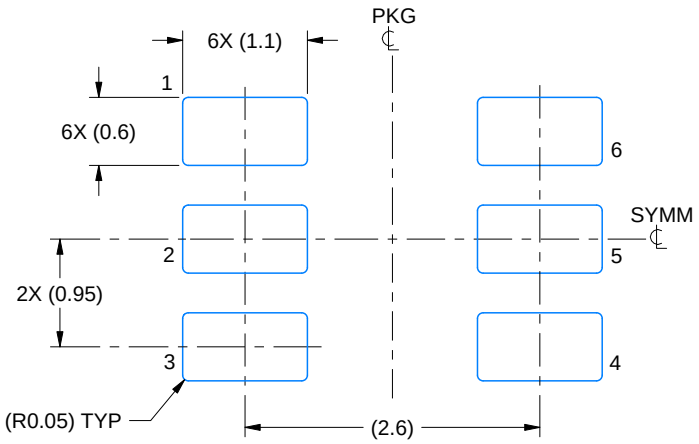
SMALL OUTLINE TRANSISTOR



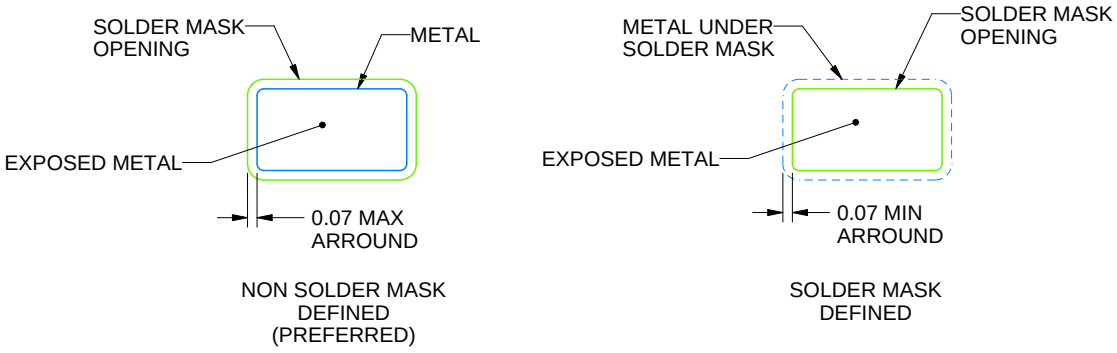
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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

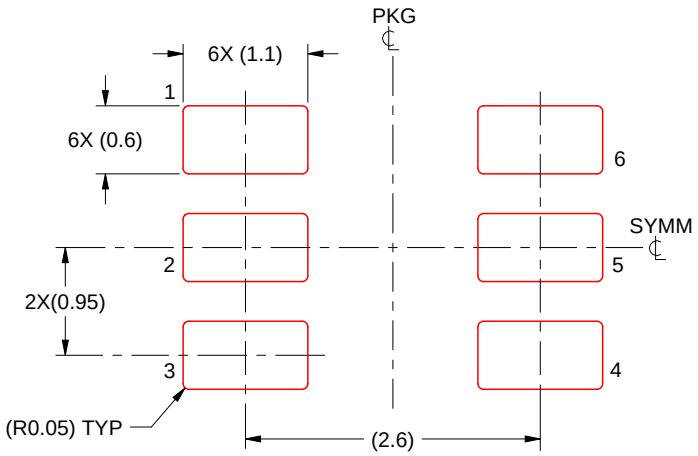


SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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