TEXAS INSTRUMENTS
UCC27611
JAJSC56F – DECEMBER 2012 – REVISED MARCH 2018

UCC27611 5V、4A～6A、ローサイドGaNドライバ

1 特長

- エンハンスメント・モードの窒化ガリウムFET（eGANFET）
- シングル電源VDD電圧範囲：4V～18V
- 駆動電圧VREFを5Vに制御
- 駆動ピーク電流：4Aソース、6Aシンク
- プルアップおよびプルダウン抵抗：1Ωおよび0.35Ω（高スルーレートでのdV/dt耐性を最大化）
- 分割出力構成（各FETのターンオンおよびターンオフ時間を最適化可能）
- 高速伝搬遅延（標準14ns）
- 高速立ち上がり/立ち下がり時間（標準9ns/5ns）
- TTLおよびCMOS互換入力（電源電圧から独立し、デジタルおよびアナログ・コントローラへのインターフェイスが容易）
- デュアル入力設計によって駆動の柔軟性を向上（反転および非反転構成）
- 入力のフローティング時は出力をLowに保持
- VDD低電圧誤動作防止（UVLO）
- eGANFETのフットプリントに対して最適化されたピン配置により、レイアウトが容易
- 露出したサーマル/グランド・パッドを備えた2.00mm×2.00mmのSON-6パッケージ（寄生インダクタンスの最小化によってゲートのリンギングを低減）
- 動作温度範囲：–40°C～140°C

2 アプリケーション

- スイッチ・モード電源
- DC/DCコンバータ
- 同期整流
- ソーラー・インバータ、モーター制御、UPS
- エンベロープ・トラッキング電源

3 概要

UCC27611は、5V駆動用に最適化されたシングル・チャネルの高速ゲート・ドライバであり、特にエンハンスメント・モードのGaN FET用に設計されています。駆動電圧VREFは、内部のリニア・レギュレータによって精密に5Vに制御されます。UCC27611は、4Aソースおよび6Aシンクの非対称レール・ツー・レール・ピーク電流駆動能力を備えています。分割出力構成となっているため、FETに応じてターンオン時間とターンオフ時間を個別に最適化できます。寄生インダクタンスを最小限に抑えたパッケージとピン配置により、立ち上がりおよび立ち下がり時間が短縮され、リンギングが抑制されます。また、伝播遅延が短く、公差や変動も最小限であるため、高い周波数で高効率の動作が可能です。1Ωと0.35Ωの抵抗により、高スルーレートのdV/dtによる急激なスイッチングにも高い耐性を持ちます。

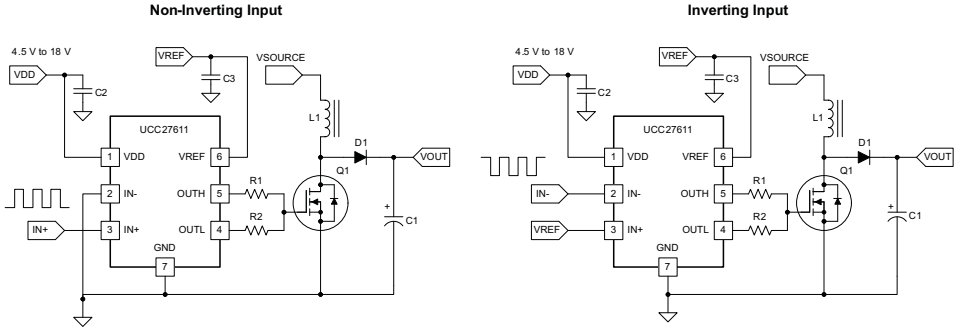
VDD入力信号のスレッショルドから独立していることで、TTLおよびCMOS低電圧ロジックとの互換性が確保されています。安全性の理由により、入力ピンがフローティング状態のときには、内部の入力プルアップ/プルダウン抵抗によって出力がLowに保持されます。VREFピンの内部回路には、低電圧誤動作防止機能が搭載され、VREF電源電圧が動作範囲内になるまで出力がLowに保持されます。UCC27611は、露出したサーマル/グランド・パッドを備えた小型の2.00mm×2.00mm SON-6パッケージ（DRV）で供給され、パッケージの電力処理能力を高めています。UCC27611は、-40°C～140°Cの幅広い温度範囲で動作します。

製品情報(1)

型番	パッケージ	本体サイズ（公称）
UCC27611	SON (6)	2.00mm×2.00mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

代表的なアプリケーションの図



英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.comで閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision E (February 2018) to Revision F — **Page**

- Changed *Power Up (Noninverting Drive)* graphic ... 9
- Changed *Power Up (Inverting Drive)* graphic ... 9

Revision D (October 2017) to Revision E — **Page**

- タイトル Changed ... 1

Revision C (December 2015) to Revision D — **Page**

- タイトル Changed ... 1

Revision B (May 2013) to Revision C — **Page**

- 「*ESD定格*」の表、「*機能説明*」、「*デバイスの機能モード*」、「*アプリケーションと実装*」、「*電源に関する推奨事項*」、「*レイアウト*」、「*デバイスとドキュメントのサポート*」、「*メカニカル、パッケージ、および注文情報*」を追加 ... 1

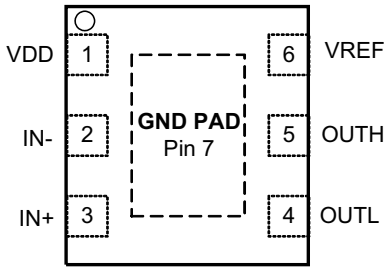
Revision A (December 2012) to Revision B — **Page**

- Added *Electrical Characteristics* Inputs (IN+, IN–) section values ... 5

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5 Pin Configuration and Functions

DRV Package
6-Pin SON With Exposed Thermal Pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	VDD	I	Bias supply input. Connect a ceramic capacitor minimum from this pin to the GND pin as close as possible to the device with the shortest trace lengths possible.
2	IN–	I	Inverting input. Pull IN+ to VDD to enable output, when using the driver device in Inverting configuration.
3	IN+	I	Noninverting input. Pull IN– to GND to enable output, when using the driver device in noninverting configuration.
4	OUTL	O	6-A sink current output of driver.
5	OUTH	O	4-A source current output of driver.
6	VREF	O	Drive voltage, output of internal linear regulator. Connect a ceramic capacitor minimum from this pin to the GND pin as close as possible to the device with the shortest trace lengths possible.
7	GND PAD	—	Ground. All signals are referenced to this node.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD}	Supply voltage	–0.3	20	V
	OUTH	–0.3	VREF + 0.3	V
	OUTL	–0.3	VREF + 0.3	V
	VREF		6	V
	IN+, IN–	–0.3	20	V
I_{out_DC}	Continuous source current of OUTH/sink current of OUTL	0.3	0.6	A
I_{out_pulsed}	Continuous source current of OUTH/sink current of OUTL (0.5 µs),	4	6	A
	Lead temperature, soldering, 10 sec.		300	°C
	Lead temperature, reflow		260	°C
T_J	Operating virtual junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	Supply voltage	4	12	18	V
IN	Input voltage	0		18	V
	IN+, IN– resistance			100	kΩ
T_J	Operating junction temperature	–40		140	°C

6.4 Thermal Information

THERMAL METRIC (1)		UCC27611 DRV (SON) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	80.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	11.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	50.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	18.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

VDD = 12 V, $T_A = T_J$ = –40 °C to 140 °C, 2-µF capacitor from VDD to GND and from VREF to GND. Currents are positive into, negative out of the specified terminal. OUTH and OUTL are tied together. (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BIAS CURRENT						
$I_{DD(off)}$	Start-up current	VDD = 3, IN+ = VDD, IN– = GND		100	180	µA
		IN+ = GND, IN– = VDD		75	160	
UNDER VOLTAGE LOCKOUT (UVLO)						
$V_{DD(on)}$	Supply start threshold		3.55	3.8	4.15	V
$V_{DD(off)}$	Minimum operating voltage after supply start		3.3	3.55	3.9	V
V_{DD_H}	Supply voltage hysteresis			0.25		V
INPUTS (IN+, IN–)						
V_{IN_L}	Input signal low threshold	Output high for IN– pin, Output Low for IN+ pin	0.9	1.1	1.3	V
V_{IN_H}	Input signal high threshold	Output high for IN+ pin, Output low for IN– pin	1.85	2.05	2.25	V
V_{IN_HYS}	Input signal hysteresis		0.7	0.95	1.2	V
V_{REF}						
V_{REF}	VREF regulator output		4.75	5	5.15	V
V_{REF_line}	VREF line regulation	VDD from 6 V to 18 V			0.05	V
V_{REF_load}	VREF load regulation	I_R from 0 mA to 50 mA			0.075	V
I_{SCC}	Short circuit current		–90	–75	–60	mA
OUTPUTS (OUTH/OUTL AND OUT)						
$I_{SRC/SNK}$	Source peak current (OUTH) / sink peak current (OUTL) (2)	C_{LOAD} = 0.22 µF, F_{SW} = 1 kHz, (2)		–4/+6		A
V_{OH}	OUTH high voltage	I_{OUTH} = –10 mA	VDD –0.05			V
V_{OL}	OUTL low voltage	I_{OUTL} = 10 mA			0.02	V
R_{OH}	OUTH pullup resistance	T_A = 25 °C, I_{OUT} = –25 mA to –50 mA		1		Ω
		T_A = –40 °C to 140 °C, I_{OUT} = –50 mA			2	
R_{OL}	OUTH pulldown resistance	T_A = 25 °C, I_{OUT} = 25 mA to 50 mA		0.35		Ω
		TA = –40°C to 140°C, IOUT = 50 mA			1.5	

(1) Device operational with output switching.
(2) Ensured by design, not tested in production.

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_R	Rise time (1)	C_{LOAD} = 1 nF		5		ns
t_F	Fall time (1)	C_{LOAD} = 1 nF		5		ns
t_{D1}	Turnon propagation delay (1)	C_{LOAD} = 1 nF, IN = 0 V to 5 V		14	25	ns
t_{D2}	Turnoff propagation delay (1)	C_{LOAD} = 1 nF, IN = 5 V to 0 V		14	25	ns

(1) See Figure 1 and Figure 2 timing diagrams.

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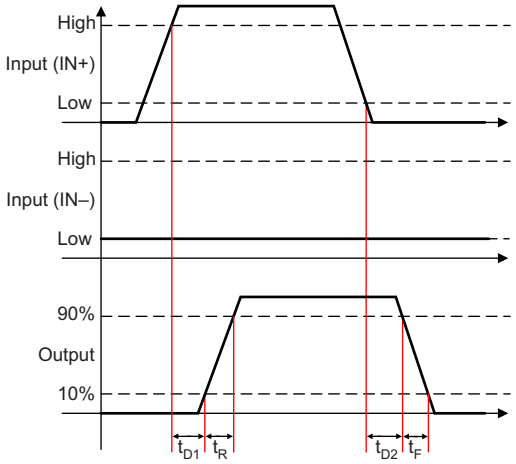


Figure 1. Noninverting Configuration (OUTH and OUTL Are Tied Together)

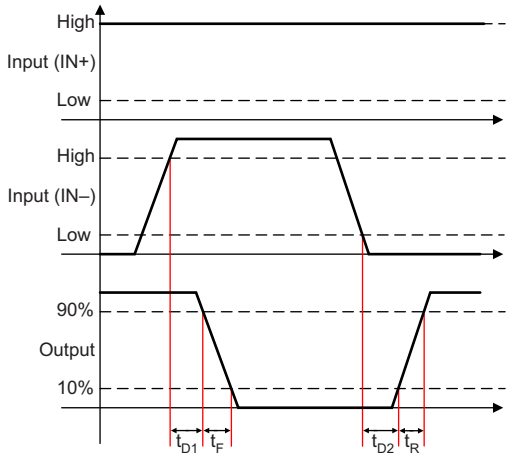


Figure 2. Inverting Configuration (OUTH and OUTL Are Tied Together)

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6.7 Typical Characteristics

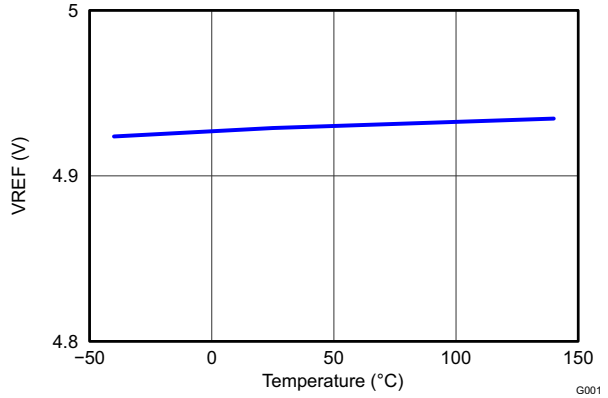


Figure 3. Reference Voltage vs Temperature

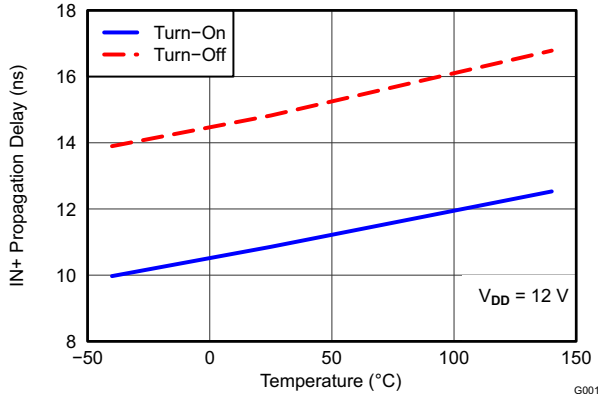


Figure 4. IN+ Propagation Delay

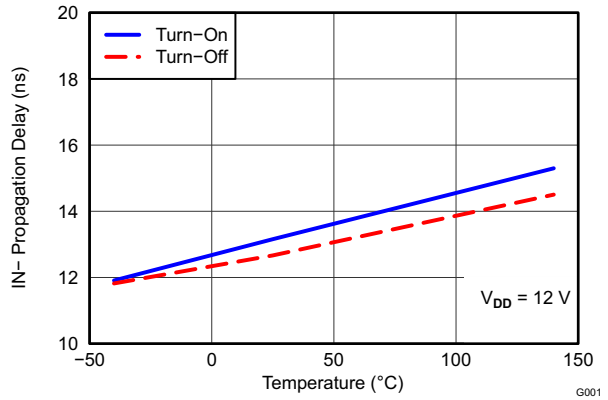


Figure 5. IN– Propagation Delay

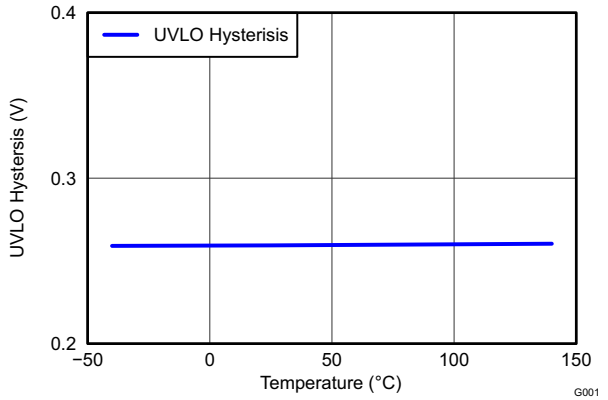


Figure 6. UVLO Hysteresis

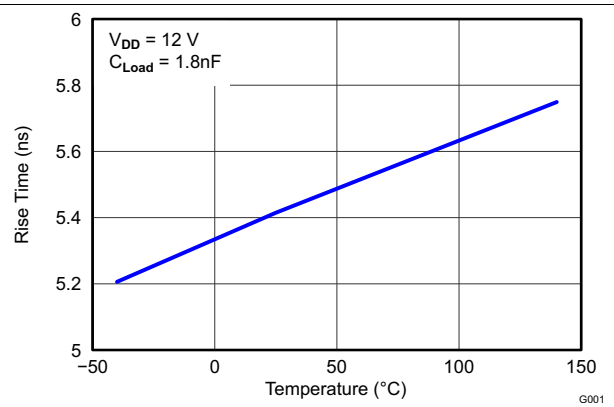


Figure 7. Rise Time

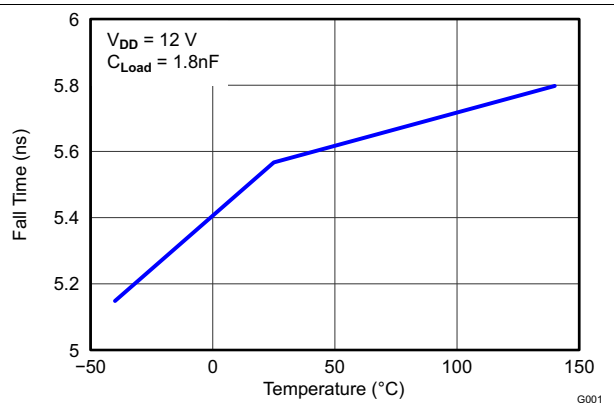


Figure 8. Fall Time

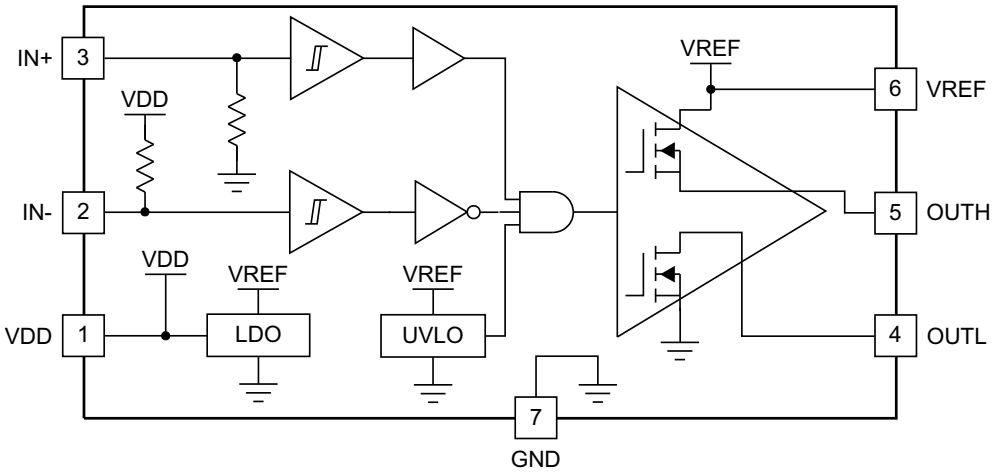
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7 Detailed Description

7.1 Overview

The UCC27611 is a single-channel, high-speed, gate driver capable of effectively driving MOSFET power switches (specifically addressing enhancement mode GaN FETs) by up to 4-A source and 6-A sink peak current. Strong sink capability in asymmetrical drive boosts immunity against parasitic Miller turnon effect. The drive voltage VREF is precisely regulated by internal linear regulator to 5 V, which is optimized for driving enhancement mode GaN FET. The input threshold of UCC27611 is based on TTL and CMOS compatible low-voltage logic, which is fixed and independent of VDD supply voltage. The 0.95-V typical hysteresis offers excellent noise immunity. For safety reason, when the input pins are in a floating condition, the internal input pullup and pulldown resistors hold the output LOW. The device also features a split-output configuration, where the gate-drive current is sourced through the OUTH pin and sunk through the OUTL pin. This pin arrangement allows the user to apply independent turnon and turnoff resistors to the OUTH and OUTL pins, respectively, and easily control the switching slew rates. The driver has rail-to-rail drive capability and extremely small propagation delay, with minimized tolerances and variations. Package and pinout with minimum parasitic inductances reduce the rise and fall time, and limit the ringing allows efficient operation at high frequencies.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 VDD and Undervoltage Lockout

The UCC27611 device has internal Under Voltage LockOut (UVLO) protection feature on the VDD pin supply circuit blocks. Whenever the driver is in UVLO condition (that is when VDD voltage less than $V_{DD(on)}$ during power up, and when VDD voltage is less than $V_{DD(off)}$ during power down), this circuit holds all outputs LOW, regardless of the status of the inputs. The UVLO is typically 3.8 V, with 250-mV typical hysteresis. This hysteresis helps prevent chatter when low VDD supply voltages have noise from the power supply, and also when there are droops in the VDD bias voltage when the system commences switching and there is a sudden increase in I_{DD}. The capability to operate at low-voltage levels such as below 5 V, along with best-in-class switching characteristics, is especially suited for driving emerging GaN wide bandgap power semiconductor devices.

For example, at power up, the UCC27611 driver output remains LOW until the VDD voltage reaches the UVLO threshold. The magnitude of the OUT signal rises with VDD, until steady-state VDD is reached. In the noninverting operation (PWM signal applied to IN+ pin), see Figure 9, the output remains LOW until the UVLO threshold is reached, and then the output is in-phase with the input. In the inverting operation (PWM signal applied to IN– pin), see Figure 10, the output remains LOW until the UVLO threshold is reached, and then the output is out-phase with the input. In both cases, the unused input pin must be properly biased to enable the output.

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Feature Description (continued)

NOTE

The output turns to high state only if IN+ pin is high and IN– pin is low after the UVLO threshold is reached.

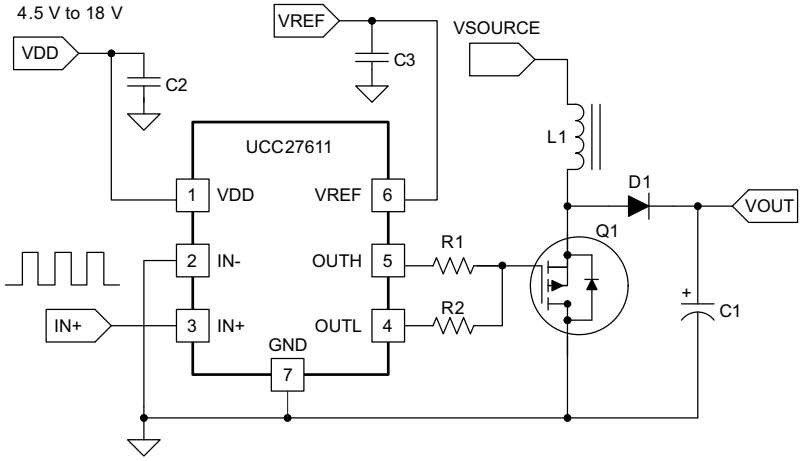


Figure 9. Power Up (Noninverting Drive)

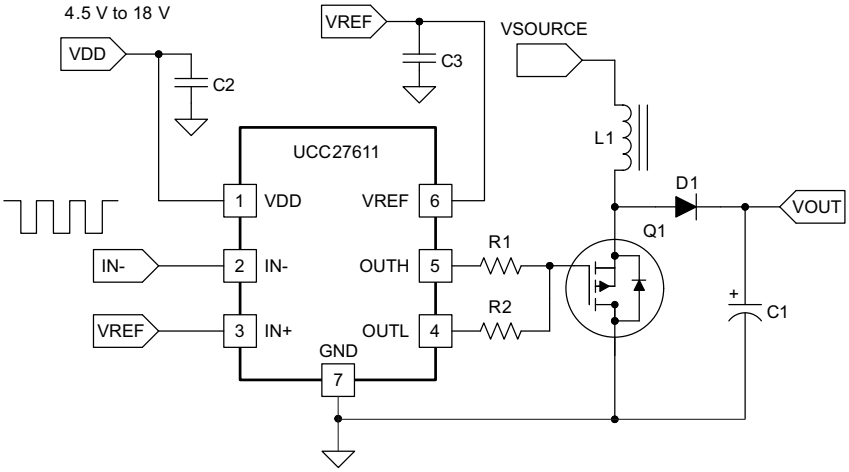


Figure 10. Power Up (Inverting Drive)

7.3.2 Operating Supply Current

The UCC27611 device features very low quiescent I_{DD} current. The total supply current is the sum of the quiescent IDD current, the average I_{OUT} current due to switching, and finally any current related to pullup resistors on the unused input pin. For example, when the inverting input pin is pulled low, additional current is drawn from VDD supply through the pullup resistors (see *Functional Block Diagram*). Knowing the operating frequency (f_{SW}) and the MOSFET gate (Q_G) charge at the drive voltage being used, the average I_{OUT} current can be calculated as product of Q_G and f_{SW}.

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Feature Description (continued)

7.3.3 Input Stage

The input pins of the UCC27611 device is based on a TTL and CMOS compatible input threshold logic that is independent of the VDD supply voltage. With typical high threshold = 2.05 V and typical low threshold = 1.1 V, the logic level thresholds can be conveniently driven with PWM control signals derived from 3.3-V and 5-V digital power controllers. Wider hysteresis (typical 1 V) offers enhanced noise immunity compared to traditional TTL logic implementations, where the hysteresis is typically less than 0.5 V. These devices also feature tight control of the input pin threshold voltage levels, which eases system design considerations, and ensures stable operation across temperature. The very low input capacitance on these pins reduces loading, and increases switching speed.

The device features an important safety function wherein, whenever any of the input pins are in a floating condition, the output of the respective channel is held in the low state. This is achieved using VDD pullup resistors on all the inverting inputs (IN– pin), or GND pulldown resistors on all the noninverting input pins (IN+ pin)(see *Functional Block Diagram*).

The device also features a dual input configuration, with two input pins available to control the state of the output. The user has the flexibility to drive the device using either a noninverting input pin (IN+), or an inverting input pin (IN–). The state of the output pin is dependent on the bias of both the IN+ and IN– pins. See Table 1 input and output logic truth table, and the Figure 12 for additional clarification.

7.3.4 Enable Function

An enable and disable function can be easily implemented in the UCC27611 device using the unused input pin. When IN+ is pulled down to GND, or IN– is pulled down to VDD, the output is disabled. Thus, IN+ pin can be used like an enable pin that is based on active high logic, while IN– can be used like an enable pin that is based on active low logic.

7.3.5 Output Stage

The output stage of the UCC27611 device is illustrated in Figure 11. OUTH and OUTL are externally connected and pinned out as OUTH and OUTL pins. The UCC27611 device features a unique architecture on the output stage, which delivers the highest peak source current when it is most needed during the Miller plateau region of the power switch turnon transition (when the power switch drain and collector voltage experiences dV and dt). The device output stage features a hybrid pullup structure using a parallel arrangement of N-channel and P-channel MOSFET devices. By turning on the N-channel MOSFET, during a narrow instant when the output changes state from low to high, the gate-driver device is able to deliver a brief boost in the peak-sourcing current, enabling fast turnon.

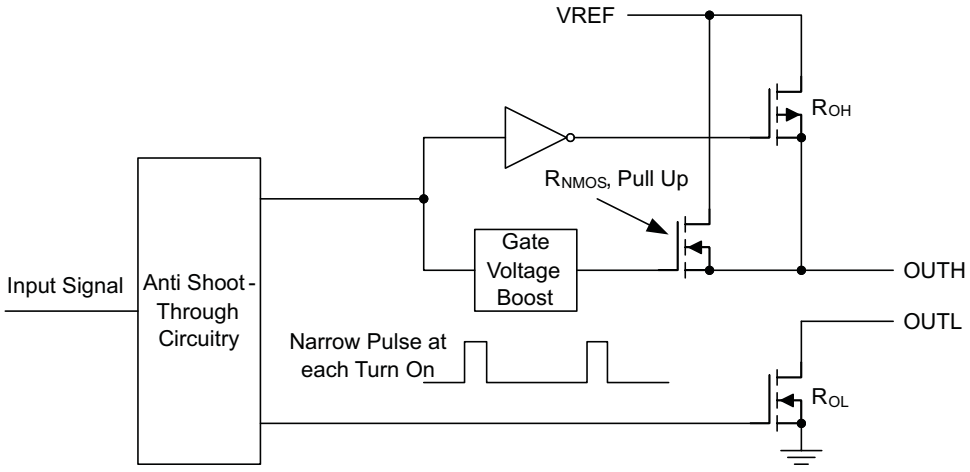


Figure 11. UCC27611 Device Gate Driver Output Structure

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Feature Description (continued)

The R_{OH} parameter (see *Electrical Characteristics*) is a DC measurement, and it is representative of the on-resistance of the P-channel device only, because the N-channel device is turned on only during output change of state from low to high. Thus, the effective resistance of the hybrid pullup stage is much lower than what is represented by R_{OH} parameter. The pulldown structure is composed of a N-channel MOSFET only. The R_{OL} parameter (see *Electrical Characteristics*), which is also a DC measurement, is representative of true impedance of the pulldown stage in the device.

The driver output voltage swings between VDD and GND, providing rail-to-rail operation thanks to the MOS output stage that delivers very low dropout. The presence of the MOSFET body diodes also offers low impedance to switching overshoots and undershoots. This means that in many cases, external Schottky diode clamps may be eliminated. The outputs of these drivers are designed to withstand 500-mA reverse current without either damage to the device, or logic malfunction.

7.3.6 Low Propagation Delays

The UCC27611 driver device feature best-in-class input-to-output propagation delay of 14 ns (typical) at VDD = 12 V. This promises the lowest level of pulse transmission distortion available from industry standard gate-driver devices for high-frequency switching applications. There is very little variation of the propagation delay with temperature and supply voltage as well, offering typically less than 20-ns propagation delays across the entire range of application conditions.

7.4 Device Functional Modes

Table 1 shows the input and output logic.

Table 1. Truth Table

IN+ PIN	IN– PIN	OUTH PIN	OUTL PIN	OUT (OUTH and OUTL pins tied together)
L	L	High-impedance	L	L
L	H	High-impedance	L	L
H	L	H	High-impedance	H
H	H	High-impedance	L	L

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers must validate and test their design implementation to confirm system functionality.

8.1 Application Information

High-current gate-driver devices are required in switching power applications for a variety of reasons. To effect the fast switching of power devices, and reduce associated switching-power losses, a powerful gate-driver device employs between the PWM output of control devices and the gates of the power semiconductor devices. Further, gate-driver devices are indispensable when it is not feasible for the PWM controller device to directly drive the gates of the switching devices. With the advent of digital power, this situation is often encountered because the PWM signal from the digital controller is often a 3.3-V logic signal that is not capable of effectively turning on a power switch. A level-shifting circuitry is required to boost the 3.3-V signal to the gate-drive voltage to fully turn-on the power device and minimize conduction losses. Traditional buffer-drive circuits based on NPN/PNP bipolar transistors in a totem-pole arrangement, as emitter-follower configurations, prove inadequate with digital power because the traditional buffer-drive circuits lack level-shifting capability. Gate-driver devices effectively combine both the level-shifting and buffer-drive functions. Gate-driver devices also find other needs such as minimizing the effect of high-frequency switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power-device gates, reducing power dissipation and thermal stress in controller devices by moving gate-charge power losses into the controller.

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8.2 Typical Application

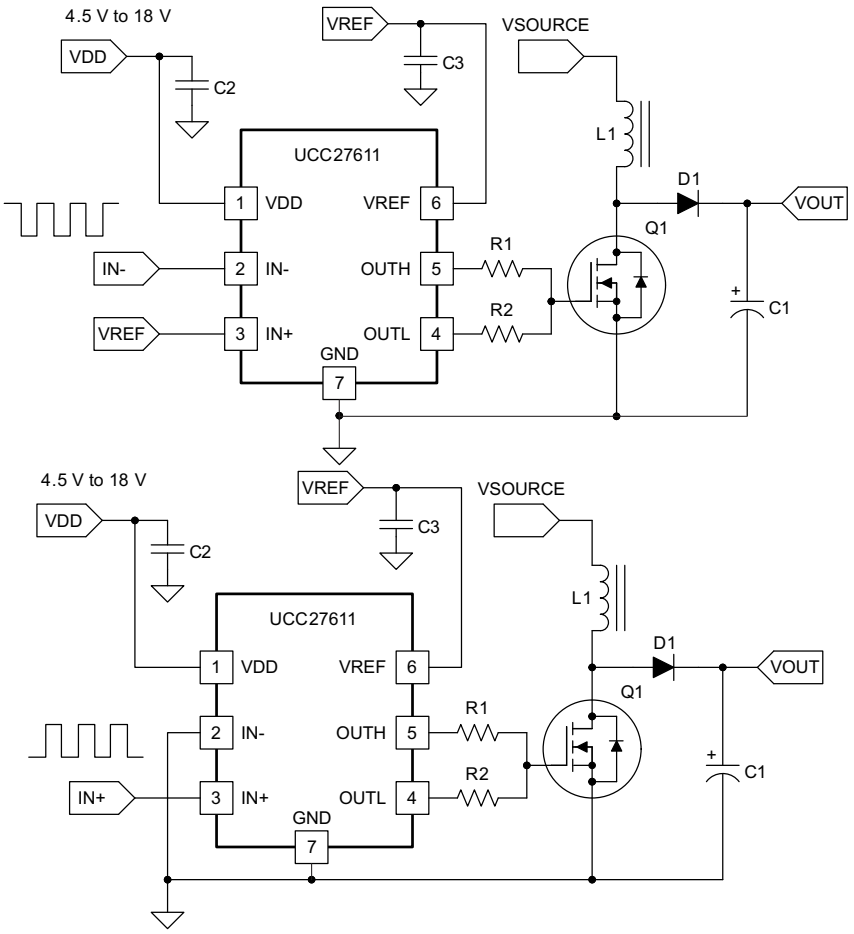


Figure 12. UCC27611 Driving Enhancement Mode GaN FET in Boost Configuration

8.2.1 Design Requirements

The requirements of gate-driver for driving enhancement mode GaN FET are listed as below:

- The headroom between the recommended gate-drive voltage and the absolute maximum rating of GaN transistor is generally marginal. It is critical to drive the GaN FET by an accurate gate-drive supply voltage
- The turnon threshold of the GaN transistor is generally much lower than that of silicon MOSFETs, the risk of Miller turnon and shoot-through becomes a concern for the higher-voltage devices. Low pulldown impedance is necessary to boost the immunity of Miller turnon
- With enhancement mode GaN transistors, the need for minimizing pulldown impedance means that addition pulldown gate resistor and antiparallel diode connection is not recommended. Split the gate pullup and pulldown connections and allow the insertion of external pullup resistance for EMI and voltage-overshoot control is needed
- At high switching speeds, the impact of the gate-drive interconnection impedance becomes important, low-inductance packages with good thermal capability is required for gate driver

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Typical Application (continued)

8.2.2 Detailed Design Procedure

8.2.2.1 Gate Drive Supply Voltage

The drive voltage for GaN FETs must be tightly regulated, that's why a linear regulator is integrated in UCC27611 to providing well-regulated 5-V voltage (VREF). Depending on layout and noise generated by the power stage, the parasitic inductance in conjunction with the Miller capacitance of the FET can cause excessive ringing on the gate drive waveform resulting in peaks higher that the regulated VREF drive voltage. With enough energy present, the potential exists to charge the VREF decoupling capacitor higher than the 6-V maximum allowed on a Gallium Nitride transistor. To prevent this from happening, the driver must be close to its own FET to avoid excessive ringing during fast switching transitions, and external gate resistor R_{GH} connected to OUTH pin of driver must be used to limit the turnon speed.

8.2.2.2 Input Configuration

The UCC27611 offers both inverting (IN–) and noninverting (IN+) inputs to satisfy requirements for inverting and noninverting gate drive in a single device type. The design must specify what type of input-to-output configuration must be used. If turning on the power MOSFET when the input signal is in high state is preferred, then a device capable of the noninverting configuration must be selected. If turning off the power MOSFET when the input signal is in high state is preferred, then a device capable of the inverting configuration must be chosen. Once an input pin has been chosen for PWM drive, the other input pin (the unused input pin) must be properly biased to enable the output. The unused input pin cannot remain in a floating condition, because whenever any input pin is left in a floating condition, the output is disabled for safety purposes. Alternatively, the unused input pin can effectively be used to implement an enable and disable function, as explained below.

- To drive the device in a noninverting configuration, apply the PWM control input signal to IN+ pin. In this case, the unused input pin, IN–, must be biased low (tied to GND) to enable the output. Alternately, the IN– pin can be used to implement the enable and disable function using an external logic signal. OUT is disabled when IN– is biased high and OUT is enabled when IN– is biased low
- To drive the device in an inverting configuration, apply the PWM control input signal to IN– pin. In this case, the unused input pin, IN+, must be biased high (For example, tied to VDD) to enable the output. Alternately, the IN+ pin can be used to implement the enable and disable function using an external logic signal. OUT is disabled when IN+ is biased low and OUT is enabled when IN+ is biased high

NOTE

The output pin can be driven into a high state only when IN+ pin is biased high and IN– input is biased low. See *Device Functional Modes* for information on device functionality.

The input stage of the driver must preferably be driven by a signal with a short rise or fall time. Take care whenever the driver is used with slowly varying input signals, especially in situations where the device is located in a mechanical socket, or PCB layout is not optimal. High dI/dt current from the driver output coupled with board layout parasitic can cause ground bounce. Because the device features just one GND pin, which may be referenced to the power ground, this may modify the differential voltage between input pins and GND and trigger an unintended change of output state. Because of fast 13-ns propagation delay, this can ultimately result in high-frequency oscillations, which increase power dissipation and pose risk of damage. In the worst case, when a slow input signal is used and PCB layout is not optimal, it may be necessary to add a small capacitor between input pin and ground very close to the driver device. This helps to convert the differential mode noise with respect to the input logic circuitry into common mode noise and avoid unintended change of output state.

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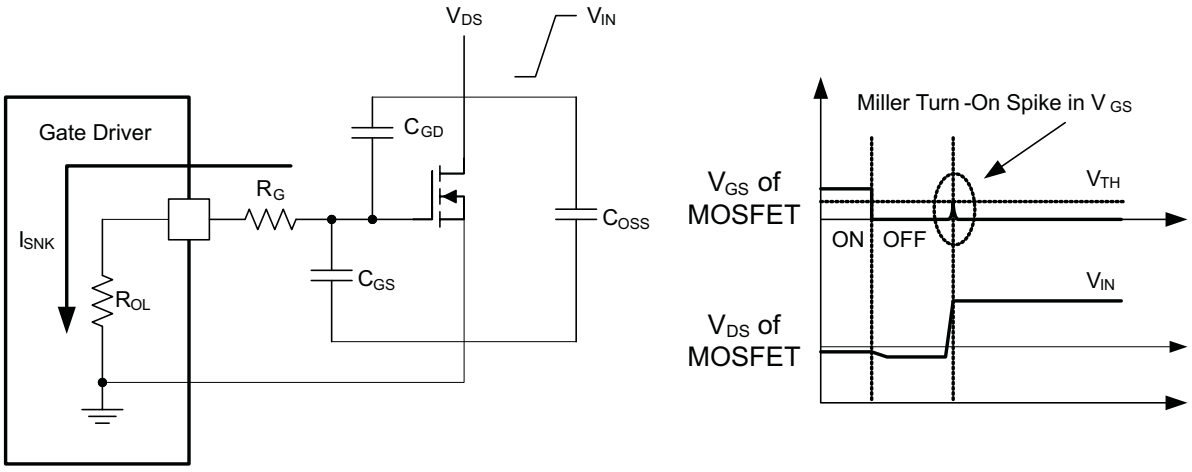
Typical Application (continued)

8.2.2.3 Output Configuration

Generally, the switching speed of the power switch during turnon and turnoff must be as fast as possible to minimize switching power losses. The gate driver device must be able to provide the required peak current for achieving the targeted switching speeds for the targeted power MOSFET. In practical designs, the parasitic trace inductance in the gate drive circuit of the PCB has a definitive role to play on the power MOSFET switching speed. The effect of this trace inductance is to limit the dI/dt of the output current pulse of the gate driver. Because of this, the desired switching speed may not be realized, even when theoretical calculations indicate the gate driver can achieve the targeted switching speed. Thus, placing the gate driver device very close to the power MOSFET and designing a tight gate drive-loop with minimal PCB trace inductance is important to realize the full peak-current capability of the gate driver.

The UCC27611 is capable of delivering 4-A source, 6-A sink (asymmetrical drive) at VDD = 12 V. Strong sink capability in asymmetrical drive results in a very low pulldown impedance in the driver output stage which boosts immunity against parasitic, Miller turnon (C × dV/dt turnon) effect, especially where low gate-charge MOSFETs or emerging wide band-gap GaN power switches are used.

An example of a situation where Miller turnon is a concern is synchronous rectification (SR). In SR application, the dV/dt occurs on MOSFET drain when the MOSFET is already held in OFF state by the gate driver. The current discharging the C_{GD} Miller capacitance during this dV/dt is shunted by the pulldown stage of the driver. If the pulldown impedance is not low enough, then a voltage spike can result in the V_{GS} of the MOSFET, which can result in spurious turnon. This phenomenon is illustrated in Figure 13. UCC27611 offers a best-in-class, 0.35-Ω (typ) pulldown impedance boosting immunity against Miller turnon.



Output stage mitigates Miller turnon effect.

Figure 13. Low-Pulldown Impedance in UCC27611, 4-A and 6-A Asymmetrical Drive

If limiting the rise or fall times to the power device to reduce EMI is necessary, then an external resistance is highly recommended between the output of the driver and the power device. This external resistor has the additional benefit of reducing part of the gate charge related power dissipation in the gate driver device package and transferring it into the external resistor itself. The split outputs of the UCC27611 offer flexibility to adjust the turnon and turnoff speed independently by adding additional impedance in either the turnon path (OUTH) and/or turnoff path (OUTL).

8.2.2.4 Power Dissipation

Power dissipation of the gate driver has two portions as shown in Equation 1:

$$P_{DISS} = P_{DC} + P_{SW} \quad (1)$$

Typical Application (continued)

The DC portion of the power dissipation is $P_{DC} = I_Q \times V_{DD}$ where I_Q is the quiescent current for the driver. The quiescent current is the current consumed by the device to bias all internal circuits such as input stage, reference voltage, logic circuits, protections, and so forth and also any current associated with switching of internal devices when the driver output changes state (such as charging and discharging of parasitic capacitances, parasitic shoot-through and so forth). The UCC27611 device features very low quiescent currents (see *Electrical Characteristics*) and contains internal logic to eliminate any shoot-through in the output driver stage. Thus, the effect of the P_{DC} on the total power dissipation within the gate driver can be safely assumed to be negligible.

The power dissipated in the gate-driver package during switching (P_{SW}) depends on the following factors:

- Gate charge required of the power device (usually a function of the drive voltage V_G, which is very close to input bias supply voltage V_{REF} due to low V_{OH} dropout)
- Switching frequency
- Use of external gate resistors

When a driver device is tested with a discrete, capacitive load it is a fairly simple matter to calculate the power that is required from the bias supply. The energy that must be transferred from the bias supply to charge the capacitor is given by Equation 2:

$$E_G = \frac{1}{2} \times C_{LOAD} \times V_{REF}^2 \tag{2}$$

where

- C_{LOAD} is load capacitor of driver.

There is an equal amount of energy dissipated when the capacitor is charged. This leads to a total power loss given by Equation 3.

$$P_G = C_{LOAD} \times V_{REF}^2 \times f_{SW} \tag{3}$$

where

- f_{SW} is the switching frequency.

The switching load presented by a power MOSFET and IGBT can be converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Most manufacturers provide specifications of typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Q_G, one can determine the power that must be dissipated when charging a capacitor. This is done by using the equation, $Q_G = C_{LOAD} \times V_{REF}$, to provide Equation 4 for power:

$$P_G = C_{LOAD} \times V_{REF}^2 \times f_{SW} = Q_G \times V_{REF} \times f_{SW} \tag{4}$$

This power P_G is dissipated in the resistive elements of the circuit when the MOSFET or IGBT is being turned on or off. Half of the total power is dissipated when the load capacitor is charged during turnon, and the other half is dissipated when the load capacitor is discharged during turnoff. When no external gate resistor is employed between the driver and MOSFET and IGBT, this power is completely dissipated inside the driver package. With the use of external gate-drive resistors, the power dissipation is shared between the internal resistance of driver and external gate resistor in accordance to the ratio of the resistances (more power dissipated in the higher resistance component). Based on this simplified analysis, the driver power dissipation during switching is calculated as Equation 5:

$$P_{SW} = Q_G \times V_{REF} \times f_{SW} \left(\frac{R_{ON}}{R_{ON} + R_{GH}} + \frac{R_{OFF}}{R_{OFF} + R_{GL}} \right) \tag{5}$$

where

- $R_{OFF} = R_{OL}$ and $R_{ON} = 2.7 \times R_{OL}$ (effective resistance of pullup structure).
- R_{GH} and R_{GL} is external gate resistors connect to the OUTH and OUTL pins respective.

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Typical Application (continued)

8.2.2.5 Thermal Considerations

The useful range of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the package. In order for a gate driver to be useful over a particular temperature range, the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The thermal metrics for the driver package is summarized in the *Thermal Information* of the datasheet. The θ_{JA} metric must be used for comparison of power dissipation between different packages. The ψ_{JT} and ψ_{JB} metrics must be used when estimating the die temperature during actual application measurements. For detailed information regarding the thermal information table, please see the Application Note from Texas Instruments entitled, *Semiconductor and IC Package Thermal Metrics IC Package Thermal Metrics* (SPRA953).

The UCC27611 device includes a 6-pin DRV package with exposed thermal pad. The exposed thermal pad in DRV package provides designers with an ability to create an excellent heat removal sub-system from the vicinity of the device, thus helping to maintain a lower junction temperature. This pad must be soldered to the copper on the printed circuit board directly underneath the device package. Then a printed circuit-board designed with thermal lands and thermal vias completes a very efficient heat removal subsystem. In such a design, the heat is extracted from the semiconductor junction through the thermal pad, which is then efficiently conducted away from the location of the device on the PCB through the thermal network. This helps to maintain a lower board temperature near the vicinity of the device leading to an overall lower device junction temperature.

8.2.3 Application Curves

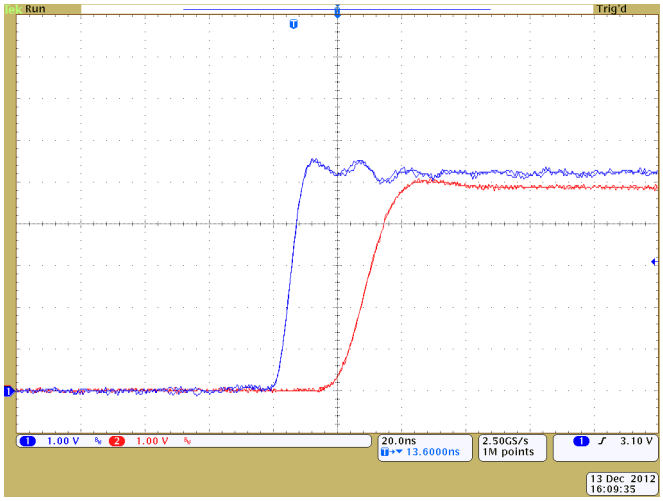


Figure 14. Output Rising
(Ch1 = IN+, Ch2 = OUTPUT)

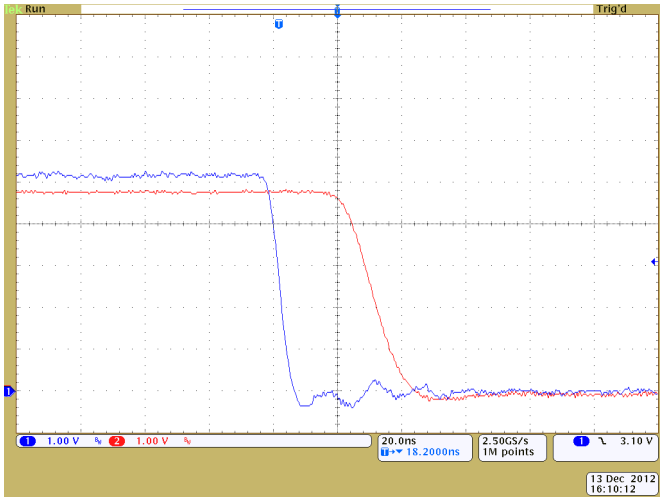


Figure 15. Output Falling
(Ch1 = IN+, Ch2 = OUTPUT)

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9 Power Supply Recommendations

The bias supply voltage range for which the device is rated to operate is from 4 V to 18 V. The lower end of this range is governed by the internal under voltage-lockout (UVLO) protection feature on the VDD pin supply circuit blocks. Whenever the driver is in UVLO condition when the VDD pin voltage is below the $V_{DD(on)}$ supply start threshold, this feature holds the output low, regardless of the status of the inputs. The upper end of this range is driven by the 20-V absolute maximum voltage rating of the VDD pin of the device (which is a stress rating). Keeping a 2-V margin to allow for transient voltage spikes, the maximum recommended voltage for the VDD pin is 18V.

The UVLO protection feature also involves a hysteresis function. This means that when the VDD pin bias voltage has exceeded the threshold voltage and device begins to operate, and if the voltage drops, then the device continues to deliver normal functionality unless the voltage drop exceeds the hysteresis specification $V_{DD(off)}$. Therefore, ensuring that, while operating at or near the 4-V range, the voltage ripple on the auxiliary power supply output is smaller than the hysteresis specification of the device is important to avoid triggering device shutdown.

During system shutdown, the device operation continues until the VDD pin voltage has dropped below the threshold $V_{DD(off)}$ which must be accounted for while evaluating system shutdown timing design requirements. Likewise, at system startup, the device does not begin operation until the VDD pin voltage has exceeded above the $V_{DD(on)}$ threshold.

Because the driver draws current from the VDD pin to bias all internal circuits, for the best high-speed circuit performance, two VDD bypass capacitors are recommended to prevent noise problems. The use of surface mount components is highly recommended. A 0.1-μF ceramic capacitor must be located as close as possible to the VDD to GND pins of the gate driver. In addition, a larger capacitor (such as 1-μF) with relatively low ESR must be connected in parallel and close proximity to help deliver the high-current peaks required by the load. The parallel combination of capacitors must present a low impedance characteristic for the expected current levels and switching frequencies in the application.

The UCC27611 integrate a LDO to provide well-regulated voltage (VREF) to driving GaN FET. The charge for source current pulses delivered by the OUTH pin is supplied through the VREF pin. As a result, every time a current is sourced out of the OUTH pin a corresponding current pulse is delivered into the device through the VREF pin. Thus ensuring that a local bypass capacitor is provided between the VREF and GND pins and located as close to the device as possible for the purpose of decoupling is important. A low ESR, ceramic surface mount capacitor is necessary.

The UCC27611 device is a high-performance driver capable of fast rise and fall times at high-peak currents. Careful PCB layout to reduce parasitic inductances is critical to achieve maximum performance. When a less-than-optimal layout is unavoidable, then TI recommends adding a low capacitance schottky diode to prevent the energy ringing back from the gate and charging up the decoupling capacitor on VREF (see Figure 16).

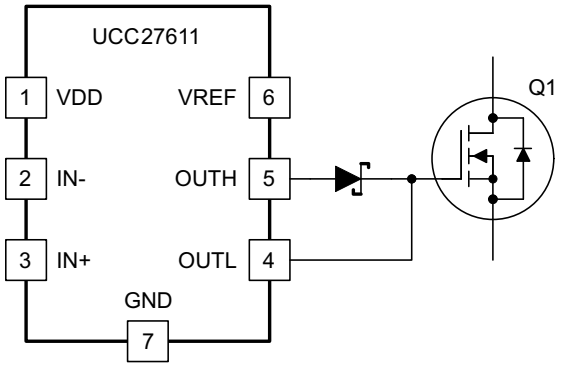


Figure 16. Low-Capacitance Schottky Diode to Prevent From Overcharging

The alternate method would be to add a loading resistor to VREF to bleed off the charge. This method eliminates the additional voltage drop from the diode, but reduces the current available for additional circuits or gate drive if too small a value of resistor is used.

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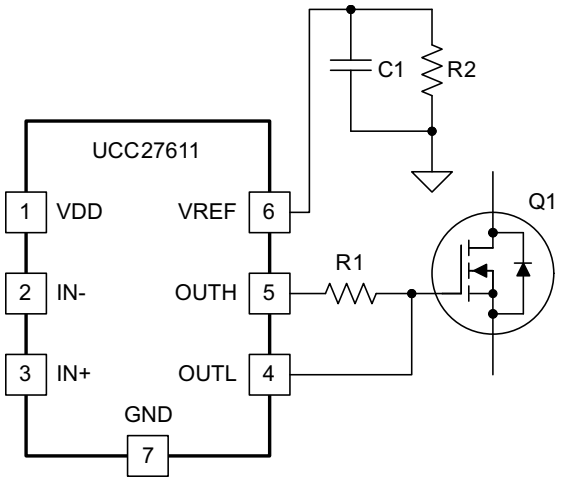


Figure 17. Load Resistor at VREF to Bleed Off the Charge

10 Layout

10.1 Layout Guidelines

Proper PCB layout is extremely important in a high-current, fast-switching circuit to provide appropriate device operation and design robustness. The UCC27611 device gate driver incorporates short-propagation delays and powerful output stages capable of delivering large current peaks with very fast rise and fall times at the gate of power switch to facilitate voltage transitions very quickly. Very high di and dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled. The following circuit layout guidelines are strongly recommended when designing with these high-speed drivers.

- Locate the driver device as close as possible to power device to minimize the length of high-current traces between the output pins and the gate of the power device.
- Locate the VDD and VREF bypass capacitors between VDD, VREF and GND as close as possible to the driver with minimal trace length to improve the noise filtering. These capacitors support high-peak current being drawn from VDD during turnon of power MOSFET. The use of low inductance SMD components such as chip resistors and chip capacitors is highly recommended.
- The turnon and turnoff current loop paths (driver device, power MOSFET and VDD, VREF bypass capacitors) must be minimized as much as possible to keep the stray inductance to a minimum. High dI and dt is established in these loops at two instances – during turnon and turnoff transients, which induces significant voltage transients on the output pin of the driver device and gate of the power switch.
- Wherever possible parallel the source and return traces, taking advantage of flux cancellation.
- Separate power traces and signal traces, such as output and input signals.
- Star-point grounding is a good way to minimize noise coupling from one current loop to another. The GND of the driver must be connected to the other circuit nodes such as source of power switch, ground of PWM controller and so forth at one, single point. The connected paths must be as short as possible to reduce inductance and be as wide as possible to reduce resistance.
- Use a ground plane to provide noise shielding. Fast rise and fall times at OUT may corrupt the input signals during transition. The ground plane must not be a conduction path for any current loop. Instead the ground plane must be connected to the star-point with one single trace to establish the ground potential. In addition to noise shielding, the ground plane can help in power dissipation as well.
- In noisy environments, it may be necessary to tie the unused Input pin of UCC27611 device to VDD or VREF (in case of IN+) or GND (in case of IN–) using short traces to ensure that the output is enabled and to prevent noise from causing malfunction in the output.

10.2 Layout Example

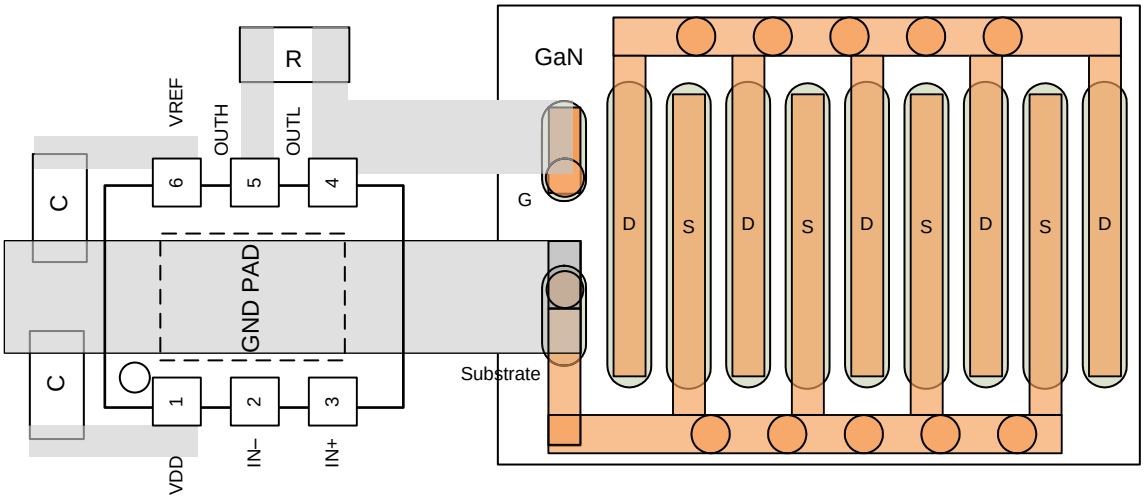


Figure 18. PCB Layout Recommendation

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11 デバイスおよびドキュメントのサポート

11.1 ドキュメントのサポート

11.1.1 関連資料

関連資料については、以下を参照してください。

- *『半導体とICパッケージの熱指標』*(SPRA953)
- *『UCC27611OLEVM-203の使用法』*(SLUUA64)

11.2 ドキュメントの更新通知を受け取る方法

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11.3 コミュニティ・リソース

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11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC27611DRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 140	7611
UCC27611DRVR.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 140	7611
UCC27611DRVT	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 140	7611
UCC27611DRVT.A	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 140	7611
UCC27611DRVTG4	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 140	7611
UCC27611DRVTG4.A	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 140	7611

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

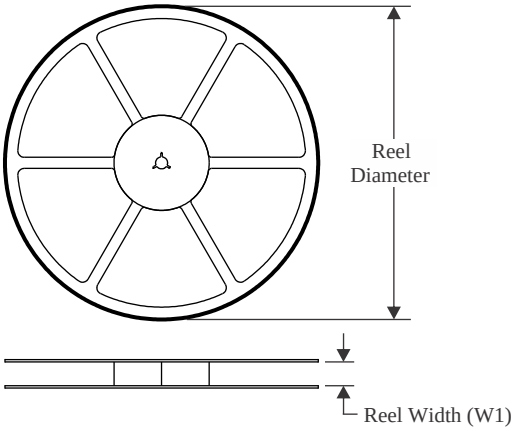
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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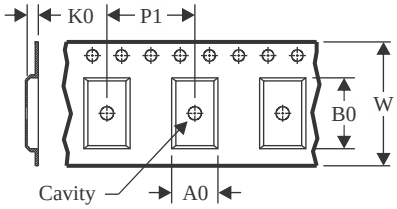
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

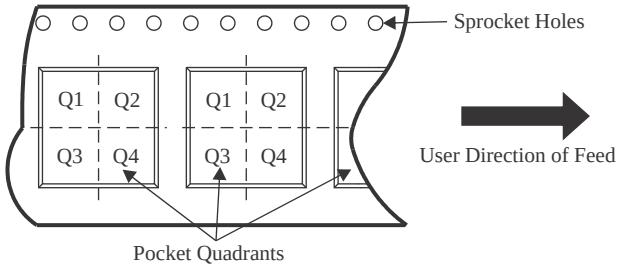


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

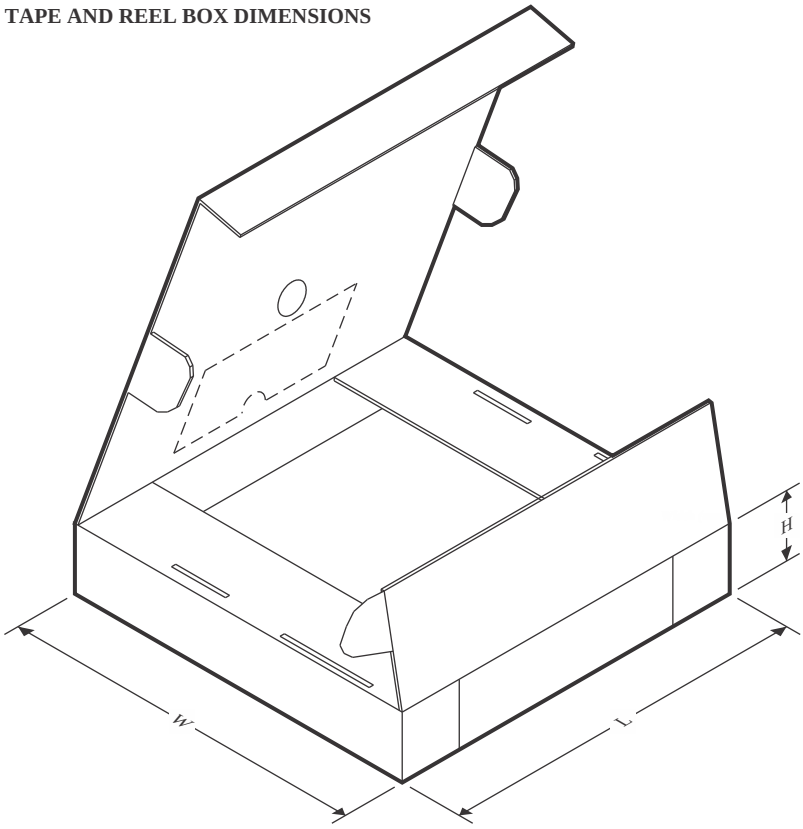
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27611DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
UCC27611DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
UCC27611DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
UCC27611DRVTG4	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

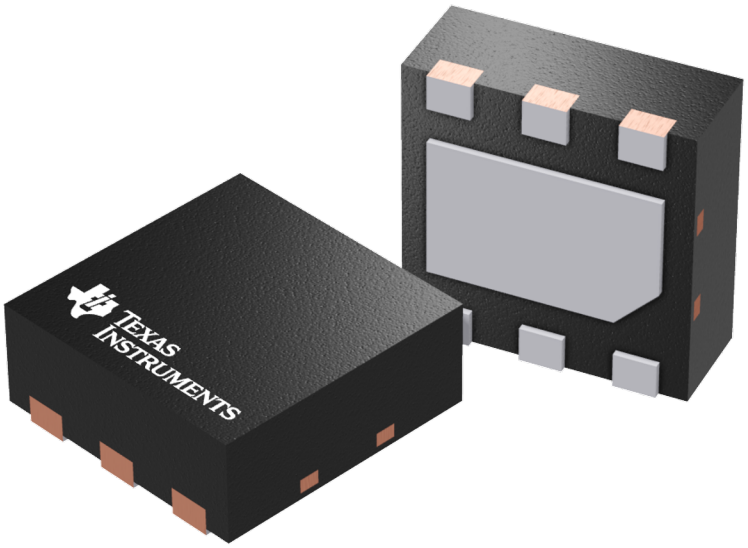


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27611DRVR	WSON	DRV	6	3000	182.0	182.0	20.0
UCC27611DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
UCC27611DRVT	WSON	DRV	6	250	182.0	182.0	20.0
UCC27611DRVTG4	WSON	DRV	6	250	182.0	182.0	20.0

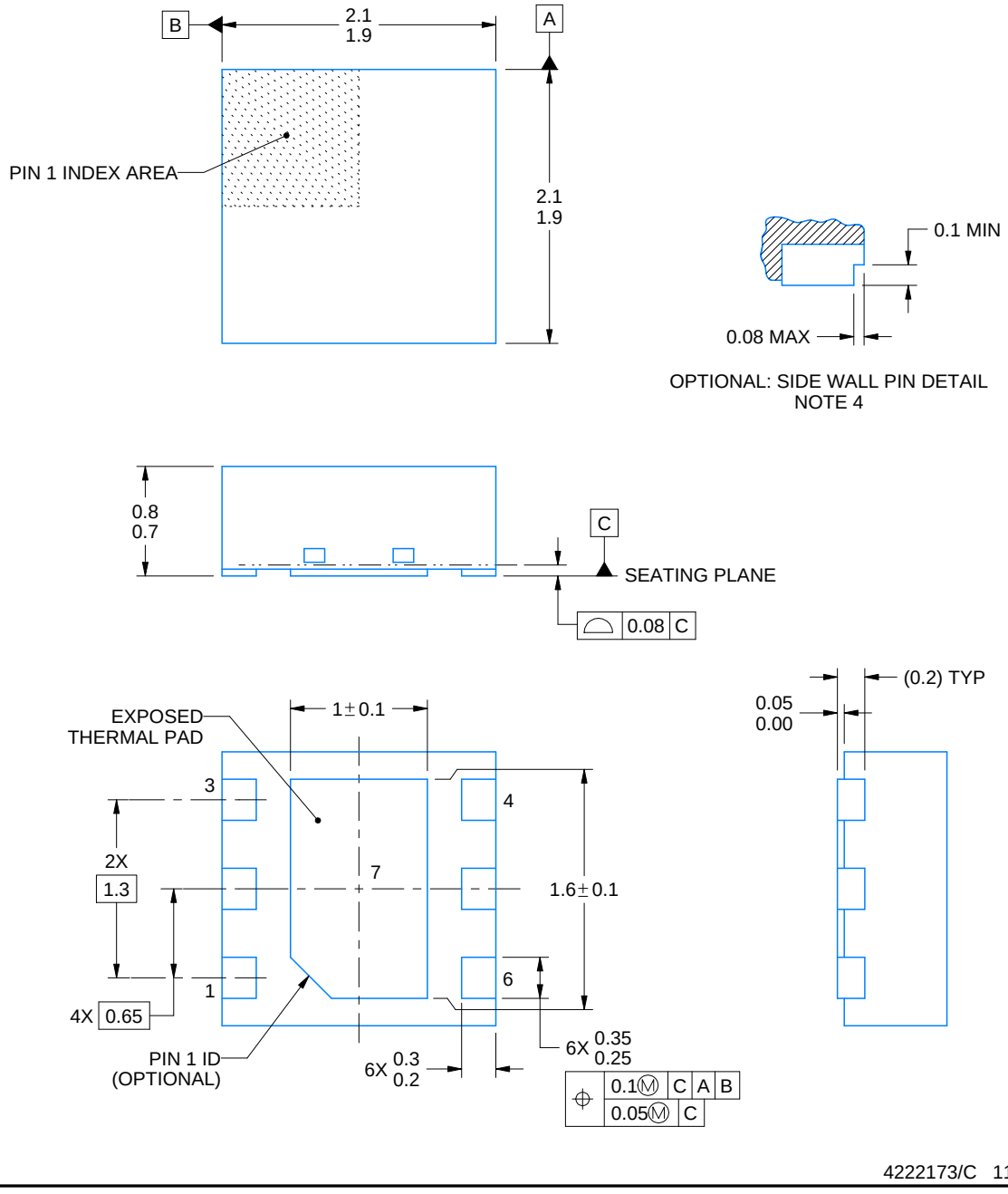
DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



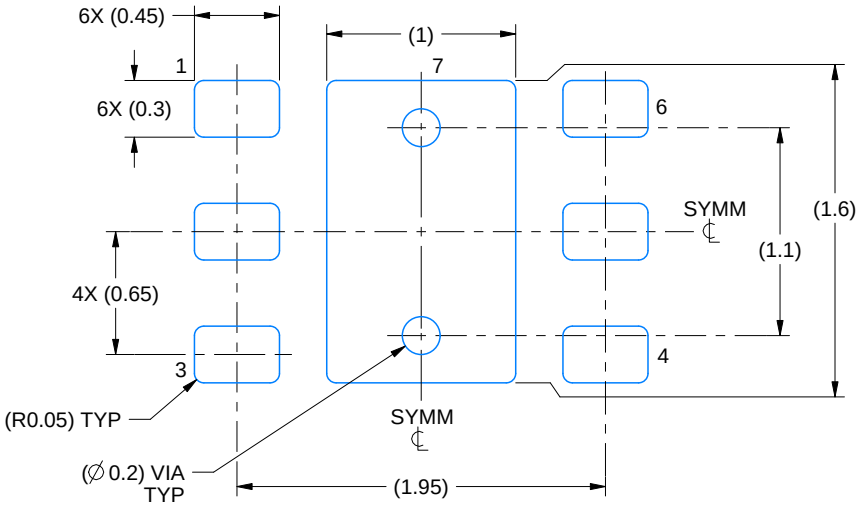
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PLASTIC SMALL OUTLINE - NO LEAD

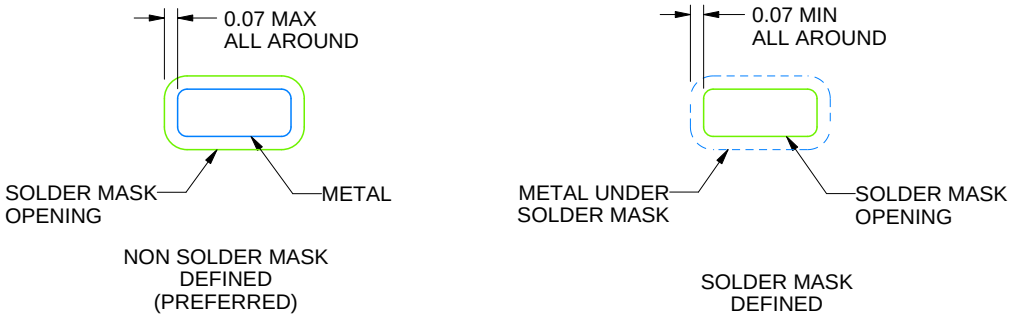


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Minimum 0.1 mm solder wetting on pin side wall. Available for wettable flank version only.



LAND PATTERN EXAMPLE
SCALE:25X

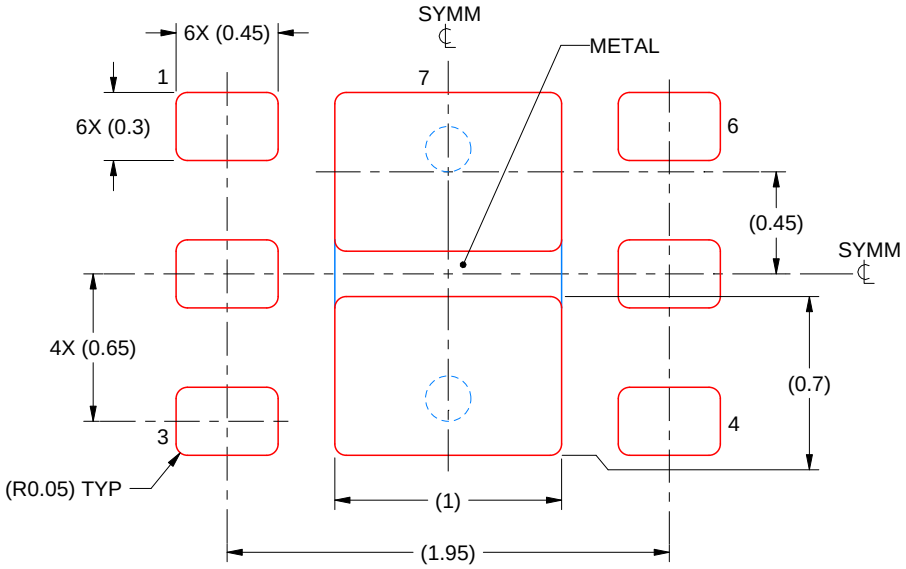


SOLDER MASK DETAILS

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NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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