TEXAS INSTRUMENTS
UCC28740
JAJSF22D – JULY 2013 – REVISED MARCH 2018

UCC28740 オプトカプラ帰還を使用する定電圧、定電流のフライバック・コントローラ

1 特長

- 無負荷時の電力10mW未満
- CVのオプトカプラ帰還、およびCCの1次側レギュレーション(PSR)
- ラインおよび負荷範囲の全体にわたって±1%の電圧レギュレーションと±5%の電流レギュレーションを実現
- 700Vのスタートアップ・スイッチ
- 100kHzの最大スイッチング周波数により電力密度の高い充電器を設計可能
- 共振リング・バレー・スイッチング動作により全体効率を最大化
- EMI準拠を容易にする周波数ディザリング
- クランプされたMOSFETゲート駆動出力
- 過電圧、低ライン、過電流からの保護機能
- SOIC-7パッケージ
- WEBENCH® Power Designerにより、UCC28740を使用するカスタム設計を作成

2 アプリケーション

- USB準拠の消費者向け電子機器用アダプタおよび充電器
  - スマートフォン
  - タブレット・コンピュータ
  - カメラ
- TVおよびデスクトップPC用のスタンバイ電源
- 白物家電

3 概要

UCC28740絶縁フライバック電源コントローラは、光カプラを使用して定電圧(CV)を供給し、大きな負荷のステップに対する過渡応答を改善しています。定電流(CC)レギュレーションは、1次側レギュレーション(PSR)技法により達成されます。このデバイスは、オプトカプラによる帰還と補助フライバック巻線からの情報を処理することにより、出力電圧および電流を正確に高性能で制御します。

内部の700Vスタートアップ・スイッチ、動的に制御される動作状態、および適切に調整された変調プロファイルにより、スタートアップ時間や出力過渡応答を犠牲にすることなく、非常に低いスタンバイ時消費電力を実現します。

UCC28740では、制御アルゴリズムによって、適用される規格を満たすまたは上回る動作効率を実現できます。駆動出力は、MOSFET電力スイッチに接続されます。バレー・スイッチングによる不連続導通モード(DCM)動作でスイッチング損失が低減されます。スイッチング周波数の変調(FM)および1次電流のピーク振幅の変調(AM)により、負荷およびライン範囲の全体にわたって高い変換効率を保持します。

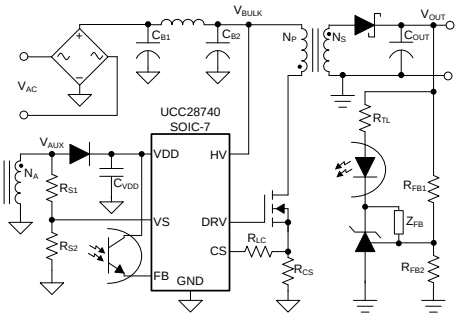
コントローラの最大スイッチング周波数は100kHzで、変圧器内でピーク1次側電流の制御が常に維持されます。1次および2次部品のストレスを抑制する保護機能も備えています。最小スイッチング周波数は170Hzで、無負荷時の電力が10mW未満に抑えられます。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
UCC28740	SOIC (7)	4.90mm×3.91mm

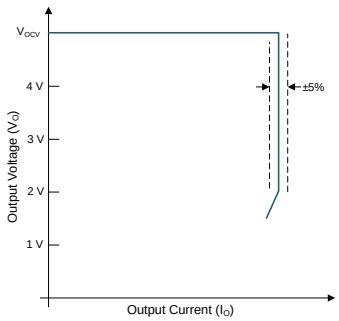
(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

アプリケーション概略図



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代表的なV-I図



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision C (July 2017) から **Revision D** に変更 **Page**

- Changed Pin 7 to Pin 8 to match the mechanical drawing. ... 3
- Changed Layout Example's pin 7 to pin 8 to match the mechanical drawing. ... 29

Revision B (December 2014) から **Revision C** に変更 **Page**

- Moved the timing parameters from the *Electrical Characteristics* table to the *Switching Characteristics* table ... 6
- Deleted *quasi* from *quasi-resonant* in the *Transformer Turns Ratio, Inductance, Primary-Peak Current* section ... 21
- 追加「*開発サポート*」セクション、「*ドキュメントのサポート*」セクション、「*ドキュメントの更新通知を受け取る方法*」セクション、「*コミュニティ・リソース*」セクション ... 30

Revision A (July 2013) から **Revision B** に変更 **Page**

- 「*ESD定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクション 追加 ... 1

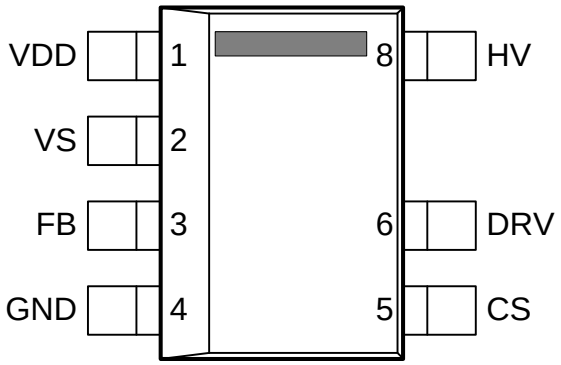
2013年7月 発行のものから更新 **Page**

- マーケティング・ステータスを「製品プレビュー」から「量産データ」に変更 ... 1

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5 Pin Configuration and Functions

D Package
7-Pin SOIC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CS	5	I	The current-sense (CS) input connects to a ground-referenced current-sense resistor in series with the power switch. The resulting voltage monitors and controls the peak primary current. A series resistor is added to this pin to compensate for peak switch-current levels as the AC-mains input varies.
DRV	6	O	Drive (DRV) is an output that drives the gate of an external high-voltage MOSFET switching transistor.
FB	3	I	The feedback (FB) input receives a current signal from the optocoupler output transistor. An internal current mirror divides the feedback current by 2.5 and applies it to an internal pullup resistor to generate a control voltage, V_{CL}. The voltage at this resistor directly drives the control law function, which determines the switching frequency and the peak amplitude of the switching current .
GND	4	—	The ground (GND) pin is both the reference pin for the controller, and the low-side return for the drive output. Special care must be taken to return all AC-decoupling capacitors as close as possible to this pin and avoid any common trace length with analog signal-return paths.
HV	8	I	The high-voltage (HV) pin may connect directly, or through a series resistor, to the rectified bulk voltage and provides a charge to the VDD capacitor for the startup of the power supply.
VDD	1	I	VDD is the bias-supply input pin to the controller. A carefully placed bypass capacitor to GND is required on this pin.
VS	2	I	Voltage sense (VS) is an input used to provide demagnetization timing feedback to the controller to limit frequency, to control constant-current operation, and to provide output-overvoltage detection. VS is also used for AC-mains input-voltage detection for peak primary-current compensation. This pin connects to a voltage divider between an auxiliary winding and GND. The value of the upper resistor of this divider programs the AC-mains run and stop thresholds, and factors into line compensation at the CS pin.

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6 Specifications

6.1 Absolute Maximum Ratings

See (1) and (2).

		MIN	MAX	UNIT
V_{HV}	Start-up pin voltage, HV		700	V
V_{VDD}	Bias supply voltage, VDD		38	V
I_{DRV}	Continuous gate-current sink		50	mA
I_{DRV}	Continuous gate-current source		Self-limiting	mA
I_{FB}	Peak current, VS		1	mA
I_{VS}	Peak current, FB		−1.2	mA
V_{DRV}	Gate-drive voltage at DRV	–0.5	Self-limiting	V
	Voltage, CS	–0.5	5	V
	Voltage, FB	–0.5	7	V
	Voltage, VS	–0.75	7	V
T_J	Operating junction temperature	–55	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal. These ratings apply over the operating ambient temperature ranges unless otherwise noted.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{VDD}	Bias-supply operating voltage	9	35	V
C_{VDD}	VDD bypass capacitor	0.047		µF
I_{FB}	Feedback current, continuous		50	µA
I_{VS}	VS pin current, out of pin		1	mA
T_J	Operating junction temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC (1)		UCC28740 D (SOIC) 7 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	141.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	73.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	89	°C/W
ψ_{JT}	Junction-to-top characterization parameter	23.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	88.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

over operating free-air temperature range, V_{VDD} = 25 V, HV = open, V_{FB} = 0 V, V_{VS} = 4 V, T_A = –40°C to +125°C, T_J = T_A (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HIGH-VOLTAGE START UP						
I_{HV}	Start-up current out of VDD	V_{HV} = 100 V, V_{VDD} = 0 V, start state	100	250	500	µA
$I_{HVLKG25}$	Leakage current at HV	V_{HV} = 400 V, run state, T_J = 25°C		0.01	0.5	µA
BIAS SUPPLY INPUT						
I_{RUN}	Supply current, run	I_{DRV} = 0, run state		2	2.65	mA
I_{WAIT}	Supply current, wait	I_{DRV} = 0, wait state		95	125	µA
I_{START}	Supply current, start	I_{DRV} = 0, V_{VDD} = 18 V, start state, I_{HV} = 0		18	30	µA
I_{FAULT}	Supply current, fault	I_{DRV} = 0, fault state		95	130	µA
UNDERVOLTAGE LOCKOUT						
$V_{VDD(on)}$	VDD turnon threshold	V_{VDD} low to high	19	21	23	V
$V_{VDD(off)}$	VDD turnoff threshold	V_{VDD} high to low	7.35	7.75	8.15	V
VS INPUT						
V_{VSNC}	Negative clamp level	I_{VSLS} = –300 µA, volts below ground	190	250	325	mV
I_{VSB}	Input bias current	V_{VS} = 4 V	–0.25	0	0.25	µA
FB INPUT						
I_{FBMAX}	Full-range input current	f_{SW} = $f_{SW(min)}$	16	23	30	µA
V_{FBMAX}	Input voltage at full range	I_{FB} = 25 µA, T_J = 25°C	0.75	0.88	1	V
R_{FB}	FB-input resistance, linearized	ΔI_{FB} = 20 µA, centered at I_{FB} = 15 µA, T_J = 25°C	10	14	18	kΩ
CS INPUT						
$V_{CST(max)}$	Maximum CS threshold voltage	I_{FB} = 0 µA(1)	738	773	810	mV
$V_{CST(min)}$	Minimum CS threshold voltage	I_{FB} = 35 µA(1)	170	194	215	mV
K_{AM}	AM-control ratio	$V_{CST(max)}$ / $V_{CST(min)}$	3.6	4	4.45	V/V
V_{CCR}	Constant-current regulation factor		318	330	343	mV
K_{LC}	Line-compensation current ratio	I_{VSLS} = –300 µA, I_{VSLS} / current out of CS pin	24	25	28.6	A/A
t_{CSLEB}	Leading-edge blanking time	DRV output duration, V_{CS} = 1 V	180	230	280	ns
DRIVERS						
I_{DRS}	DRV source current	V_{DRV} = 8 V, V_{VDD} = 9 V	20	25		mA
R_{DRVLS}	DRV low-side drive resistance	I_{DRV} = 10 mA		6	12	Ω
V_{DRCL}	DRV clamp voltage	V_{VDD} = 35 V		14	16	V
R_{DRVSS}	DRV pulldown in start-state		150	190	230	kΩ
PROTECTION						
V_{OVP}	Overvoltage threshold	At VS input, T_J = 25°C(2)	4.52	4.6	4.71	V
V_{OCP}	Overcurrent threshold	At CS input	1.4	1.5	1.6	V
$I_{VSL(run)}$	VS line-sense run current	Current out of VS pin increasing	190	225	275	µA
$I_{VSL(stop)}$	VS line-sense stop current	Current out of VS pin decreasing	70	80	100	µA
K_{VSL}	VS line sense ratio	$I_{VSL(run)}$ / $I_{VSL(stop)}$	2.45	2.8	3.05	A/A
$T_{J(stop)}$	Thermal-shutdown temperature	Internal junction temperature		165		°C

(1) This device automatically varies the control frequency and current sense thresholds to improve EMI performance. These threshold voltages and frequency limits represent average levels.
(2) The overvoltage threshold level at VS decreases with increasing temperature by 0.8 mV/°C. This compensation is included to reduce the power-supply output overvoltage detection variance over temperature.

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6.6 Switching Characteristics

over operating free-air temperature range, V_{VDD} = 25 V, HV = open, V_{FB} = 0 V, V_{VS} = 4 V, T_A = –40°C to +125°C, $T_J = T_A$ (unless otherwise noted)

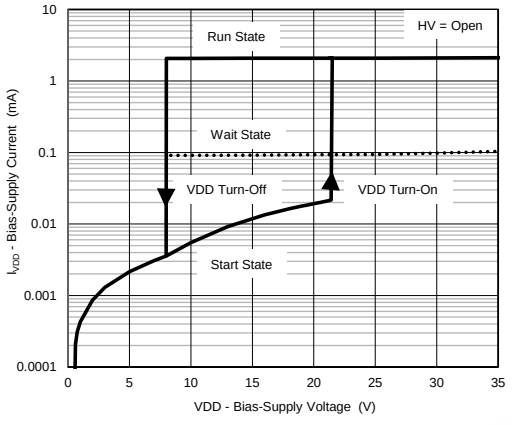
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{SW(max)}$	Maximum switching frequency	I_{FB} = 0 µA(1)	91	100	106	kHz
$f_{SW(min)}$	Minimum switching frequency	I_{FB} = 35 µA(1)	140	170	210	Hz
t_{ZTO}	Zero-crossing timeout delay		1.8	2.1	2.55	µs

(1) This device automatically varies the control frequency and current sense thresholds to improve EMI performance. These threshold voltages and frequency limits represent average levels.

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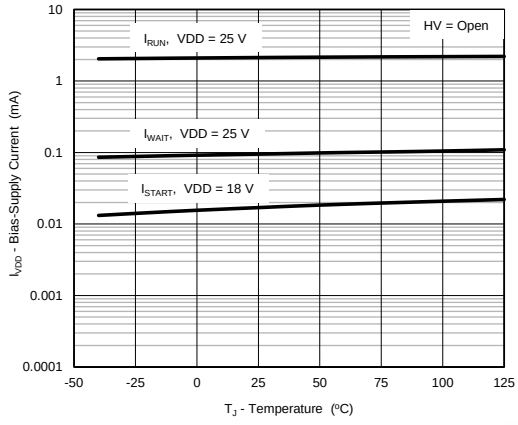
6.7 Typical Characteristics

V_{VDD} = 25 V, T_J = 25°C, unless otherwise noted.



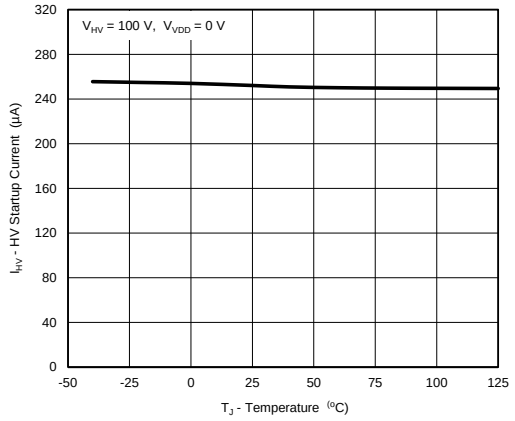
HV = Open

Figure 1. Bias-Supply Current vs. Bias-Supply Voltage



HV = Open

Figure 2. Bias-Supply Current vs. Temperature



V_{HV} = 100 V, V_{VDD} = 0 V

Figure 3. HV Startup Current vs. Temperature

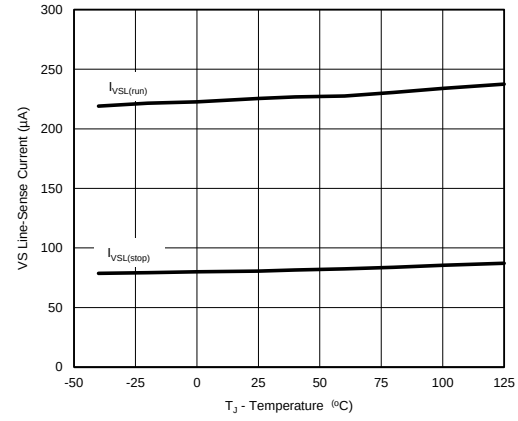


Figure 4. VS Line-Sense Currents vs. Temperature

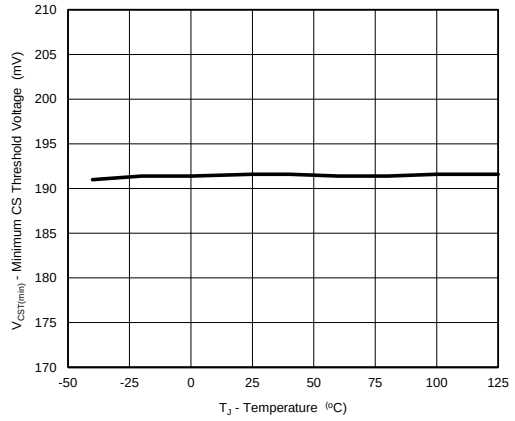


Figure 5. Minimum CS Threshold vs. Temperature

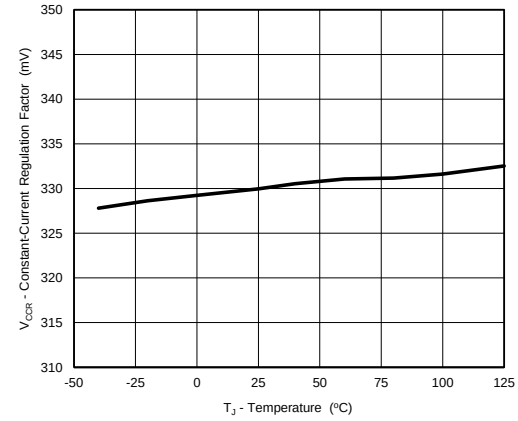


Figure 6. Constant-Current Regulation Factor vs. Temperature

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Typical Characteristics (continued)

V_{VDD} = 25 V, T_J = 25°C, unless otherwise noted.

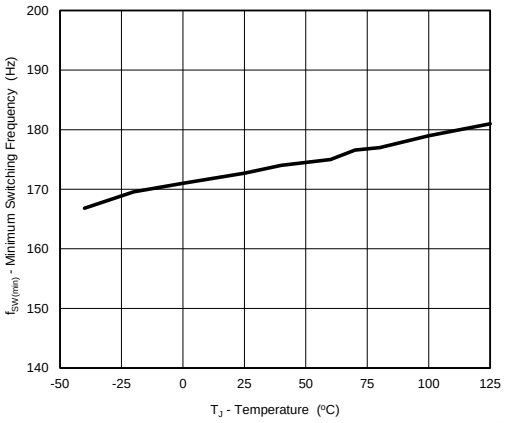
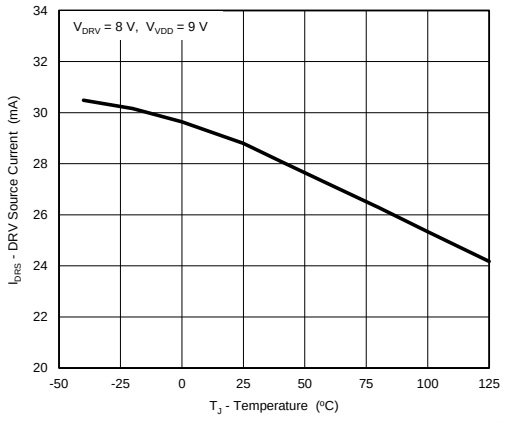


Figure 7. Minimum Switching Frequency vs. Temperature



V_{DRV} = 8 V, V_{VDD} = 9 V

Figure 8. DRV Source Current vs. Temperature

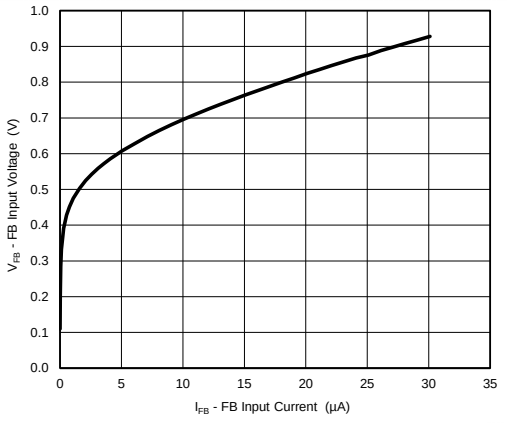


Figure 9. FB Input Voltage vs. FB Input Current

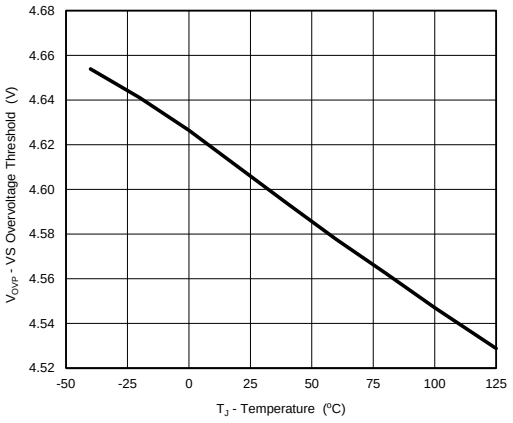


Figure 10. VS Overvoltage Threshold vs. Temperature

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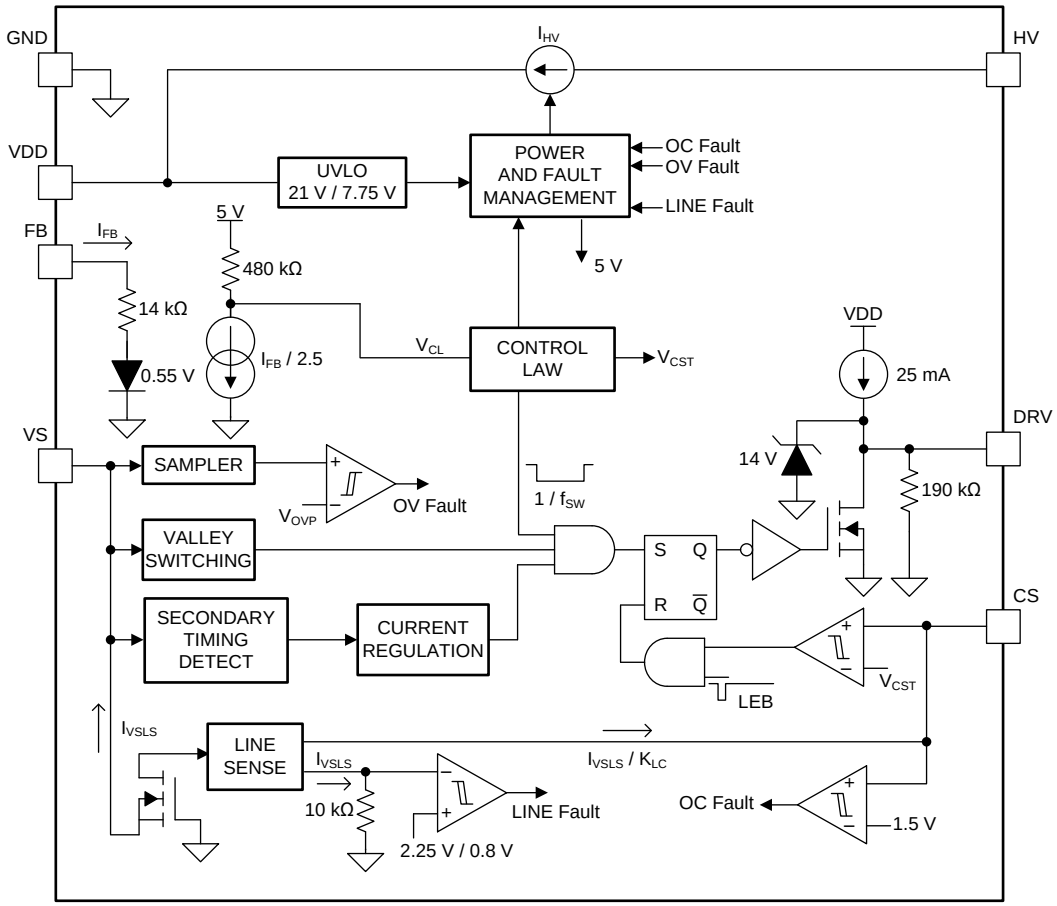
7 Detailed Description

7.1 Overview

The UCC28740 is a flyback power-supply controller which provides high-performance voltage regulation using an optically coupled feedback signal from a secondary-side voltage regulator. The device provides accurate constant-current regulation using primary-side feedback. The controller operates in discontinuous-conduction mode (DCM) with valley-switching to minimize switching losses. The control law scheme combines frequency with primary peak-current amplitude modulation to provide high conversion efficiency across the load range. The control law provides a wide dynamic operating range of output power which allows the power-supply designer to easily achieve less than 30-mW standby power dissipation using a standard shunt-regulator and optocoupler. For a target of less than 10-mW standby power, careful loss-management design with a low-power regulator and high-CTR optocoupler is required.

During low-power operating conditions, the power-management features of the controller reduce the device-operating current at switching frequencies below 32 kHz. At and above this frequency, the UCC28740 includes features in the modulator to reduce the EMI peak energy of the fundamental switching frequency and harmonics. A complete low-cost and low component-count charger-solution is realized using a straight-forward design process.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Detailed Pin Description

VDD (Device Bias Voltage Supply) The VDD pin connects to a bypass capacitor-to-ground. The turnon UVLO threshold is 21 V and turnoff UVLO threshold is 7.75 V with an available operating range up to 35 V on VDD. The typical USB-charging specification requires the output current to operate in constant-current mode from 5 V down to at least 2 V which is achieved easily with a nominal V_{VDD} of approximately 25 V. The additional VDD headroom up to 35 V allows for V_{VDD} to rise due to the leakage energy delivered to the VDD capacitor during high-load conditions.

GND (Ground) UCC28740 has a single ground reference external to the device for the gate-drive current and analog signal reference. Place the VDD-bypass capacitor close to GND and VDD with short traces to minimize noise on the VS, FB, and CS signal pins.

HV (High-Voltage Startup) The HV pin connects directly to the bulk capacitor to provide a startup current to the VDD capacitor. The typical startup current is approximately 250 µA which provides fast charging of the VDD capacitor. The internal HV startup device is active until V_{VDD} exceeds the turnon UVLO threshold of 21 V at which time the HV startup device turns off. In the off state the HV leakage current is very low to minimize standby losses of the controller. When V_{VDD} falls below the 7.75 V UVLO turnoff threshold the HV startup device turns on.

VS (Voltage Sense) The VS pin connects to a resistor-divider from the auxiliary winding to ground. The auxiliary voltage waveform is sampled at the end of the transformer secondary-current demagnetization time to provide accurate control of the output current when in constant-current mode. The waveform on the VS pin determines the timing information to achieve valley-switching, and the timing to control the duty-cycle of the transformer secondary current. Avoid placing a filter capacitor on this input which interferes with accurate sensing of this waveform.
During the MOSFET on-time, this pin also senses VS current generated through R_{S1} by the reflected bulk-capacitor voltage to provide for AC-input run and stop thresholds, and to compensate the current-sense threshold across the AC-input range. For the AC-input run/stop function, the run threshold on VS is 225 µA and the stop threshold is 80 µA.
At the end of off-time demagnetization, the reflected output voltage is sampled at this pin to provide output overvoltage protection. The values for the auxiliary voltage-divider upper-resistor, R_{S1}, and lower-resistor, R_{S2}, are determined by Equation 1 and Equation 2.

$$R_{S1} = \frac{V_{IN(run)} \times \sqrt{2}}{N_{PA} \times I_{VSL(run)}} \quad (1)$$

where

- N_{PA} is the transformer primary-to-auxiliary turns-ratio,
- $V_{IN(run)}$ is the AC RMS voltage to enable turnon of the controller (run), (in case of DC input, leave out the $\sqrt{2}$ term in the equation),
- $I_{VSL(run)}$ is the run-threshold for the current pulled out of the VS pin during the switch on-time (see *Electrical Characteristics*).

$$R_{S2} = \frac{R_{S1} \times V_{OVP}}{N_{AS} \times (V_{OV} - V_F) - V_{OVP}} \quad (2)$$

where

- V_{OV} is the maximum allowable peak voltage at the converter output,
- V_F is the output-rectifier forward drop at near-zero current,
- N_{AS} is the transformer auxiliary-to-secondary turns-ratio,
- R_{S1} is the VS divider high-side resistance,
- V_{OVP} is the overvoltage detection threshold at the VS input (see *Electrical Characteristics*).

FB (Feedback) The FB pin connects to the emitter of an analog-optocoupler output transistor which usually has the collector connected to VDD. The current supplied to FB by the optocoupler is reduced internally by a factor of 2.5 and the resulting current is applied to an internal 480-kΩ resistor to generate the control law voltage (V_{CL}). This V_{CL} directly determines the converter switching frequency and peak primary current required for regulation per the control-law for any given line and load condition.

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Feature Description (continued)

DRV (Gate Drive) The DRV pin connects to the MOSFET gate pin, usually through a series resistor. The gate driver provides a gate-drive signal limited to 14 V. The turnon characteristic of the driver is a 25-mA current source which limits the turnon dv/dt of the MOSFET drain and reduces the leading-edge current spike while still providing a gate-drive current to overcome the Miller plateau. The gate-drive turnoff current is determined by the R_{DSON} of the low-side driver along with any external gate-drive resistance. Adding external gate resistance reduces the MOSFET drain turn-off dv/dt, if necessary.

CS (Current Sense) The current-sense pin connects through a series resistor (R_{LC}) to the current-sense resistor (R_{CS}). The maximum current-sense threshold ($V_{CST(max)}$) is 0.773 V for $I_{PP(max)}$, and the minimum current-sense threshold ($V_{CST(min)}$) is 0.194 V for $I_{PP(min)}$. R_{LC} provides the feed-forward line compensation to eliminate changes in I_{PP} with input voltage due to the propagation delay of the internal comparator and MOSFET turnoff time. An internal leading-edge blanking time of 235 ns eliminates sensitivity to the MOSFET turnon current spike. Placing a bypass capacitor on the CS pin is unnecessary. The target output current in constant-current (CC) regulation determines the value of R_{CS}. The values of R_{CS} and R_{LC} are calculated using Equation 3 and Equation 4. The term V_{CCR} is the product of the demagnetization constant, 0.425, and $V_{CST(max)}$. $V_{CCR}$is held to a tighter accuracy than either of its constituent terms. The term η_{XFMR} accounts for the energy stored in the transformer but not delivered to the secondary. This term includes transformer resistance and core loss, bias power, and primary-to-secondary leakage ratio.

Example:

With a transformer core and winding loss of 5%, primary-to-secondary leakage inductance of 3.5%, and bias power to output power ratio of 0.5%, the η_{XFMR} value at full power is approximately: 1 - 0.05 - 0.035 - 0.005 = 0.91.

$$R_{CS} = \frac{V_{CCR} \times N_{PS}}{2I_{OCC}} \times \sqrt{\eta_{XFMR}} \quad (3)$$

where

- V_{CCR} is a constant-current regulation factor (see *Electrical Characteristics*),
- N_{PS} is the transformer primary-to-secondary turns-ratio (a ratio of 13 to 15 is typical for 5-V output),
- I_{OCC} is the target output current in constant-current regulation,
- η_{XFMR} is the transformer efficiency at full power.

$$R_{LC} = \frac{K_{LC} \times R_{S1} \times R_{CS} \times t_D \times N_{PA}}{L_P} \quad (4)$$

where

- R_{S1} is the VS pin high-side resistor value,
- R_{CS} is the current-sense resistor value,
- t_D is the total current-sense delay consisting of MOSFET turnoff delay, plus approximately 50 ns internal delay,
- N_{PA} is the transformer primary-to-auxiliary turns-ratio,
- L_P is the transformer primary inductance,
- K_{LC} is a current-scaling constant for line compensation (see *Electrical Characteristics*).

7.3.2 Valley-Switching and Valley-Skipping

The UCC28740 uses valley-switching to reduce switching losses in the MOSFET, to reduce induced-EMI, and to minimize the turnon current spike at the current-sense resistor. The controller operates in valley-switching in all load conditions unless the V_{DS} ringing diminishes to the point where valleys are no longer detectable.

As shown in Figure 11, the UCC28740 operates in a valley-skipping mode (also known as valley-hopping) in most load conditions to maintain an accurate voltage or current regulation point and still switch on the lowest available V_{DS} voltage.

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Feature Description (continued)

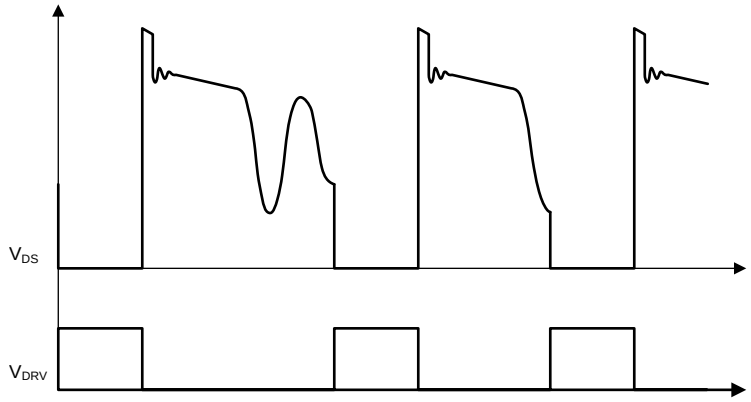


Figure 11. Valley-Skipping Mode

Valley-skipping modulates each switching cycle into discrete period durations. During FM operation, the switching cycles are periods when energy is delivered to the output in fixed packets, where the power-per-cycle varies discretely with the switching period. During operating conditions when the switching period is relatively short, such as at high-load and low-line, the average power delivered per cycle varies significantly based on the number of valleys skipped between cycles. As a consequence, valley-skipping adds additional ripple voltage to the output with a frequency and amplitude dependent upon the loop-response of the shunt-regulator. For a load with an average power level between that of cycles with fewer valleys skipped and cycles with more valleys skipped, the voltage-control loop modulates the FB current according to the loop-bandwidth and toggles between longer and shorter switching periods to match the required average output power.

7.3.3 Startup Operation

An internal high-voltage startup switch, connected to the bulk-capacitor voltage (V_{BULK}) through the HV pin, charges the VDD capacitor. This startup switch functions similarly to a current source providing typically 250 µA to charge the VDD capacitor. When V_{VDD} reaches the 21-V UVLO turnon threshold the controller is enabled, the converter starts switching, and the startup switch turns off.

Often at initial turnon, the output capacitor is in a fully discharged state. The first three switching-cycle current peaks are limited to $I_{PP(min)}$ to monitor for any initial input or output faults with limited power delivery. After these three cycles, if the sampled voltage at VS is less than 1.33 V, the controller operates in a special startup mode. In this mode, the primary current peak amplitude of each switching cycle is limited to approximately 0.63 × $I_{PP(max)}$ and D_{MAGCC} increases from 0.425 to 0.735. These modifications to $I_{PP(max)}$ and D_{MAGCC} during startup allows high-frequency charge-up of the output capacitor to avoid audible noise while the demagnetization voltage is low. Once the sampled VS voltage exceeds 1.38 V, D_{MAGCC} is restored to 0.425 and the primary current peak resumes as $I_{PP(max)}$. While the output capacitor charges, the converter operates in CC mode to maintain a constant output current until the output voltage enters regulation. Thereafter, the controller responds to the condition dictated by the control law. The time to reach output regulation consists of the time the VDD capacitor charges to 21 V plus the time the output capacitor charges.

7.3.4 Fault Protection

The UCC28740 provides extensive fault protection. The protection functions include:

- Output overvoltage
- Input undervoltage
- Internal overtemperature
- Primary overcurrent fault
- CS-pin fault
- VS-pin fault

A UVLO reset and restart sequence applies to all fault-protection events.

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Feature Description (continued)

The output-overvoltage function is determined by the voltage feedback on the VS pin. If the voltage sample of VS exceeds 4.6 V, the device stops switching and the internal current consumption becomes I_{FAULT} which discharges the VDD capacitor to the UVLO-turnoff threshold. After that, the device returns to the start state and a startup sequence ensues.

The UCC28740 always operates with cycle-by-cycle primary peak current control. The normal operating voltage range of the CS pin is 0.773 V to 0.194 V. An additional protection, not filtered by leading-edge blanking, occurs if the CS pin voltage reaches 1.5 V, which results in a UVLO reset and restart sequence.

Current into the VS pin during the MOSFET on-time determines the line-input run and stop thresholds. While the VS pin clamps close to GND during the MOSFET on-time, the current through R_{S1} is monitored to determine a sample of V_{BULK}. A wide separation of the run and stop thresholds allows for clean startup and shutdown of the power supply with the line voltage. The run-current threshold is 225 µA and the stop-current threshold is 80 µA.

The internal overtemperature-protection threshold is 165°C. If the junction temperature reaches this threshold the device initiates a UVLO-reset cycle. If the temperature is still high at the end of the UVLO cycle, the protection cycle repeats.

Protection is included in the event of component failures on the VS pin. If complete loss of feedback information on the VS pin occurs, the controller stops switching and restarts.

7.4 Device Functional Modes

7.4.1 Secondary-Side Optically Coupled Constant-Voltage (CV) Regulation

Figure 12 shows a simplified flyback convertor with the main output-regulation blocks of the device shown, along with typical implementation of secondary-side-derived regulation. The power-train operation is the same as any DCM-flyback circuit. A feedback current is optically coupled to the controller from a shunt-regulator sensing the output voltage.

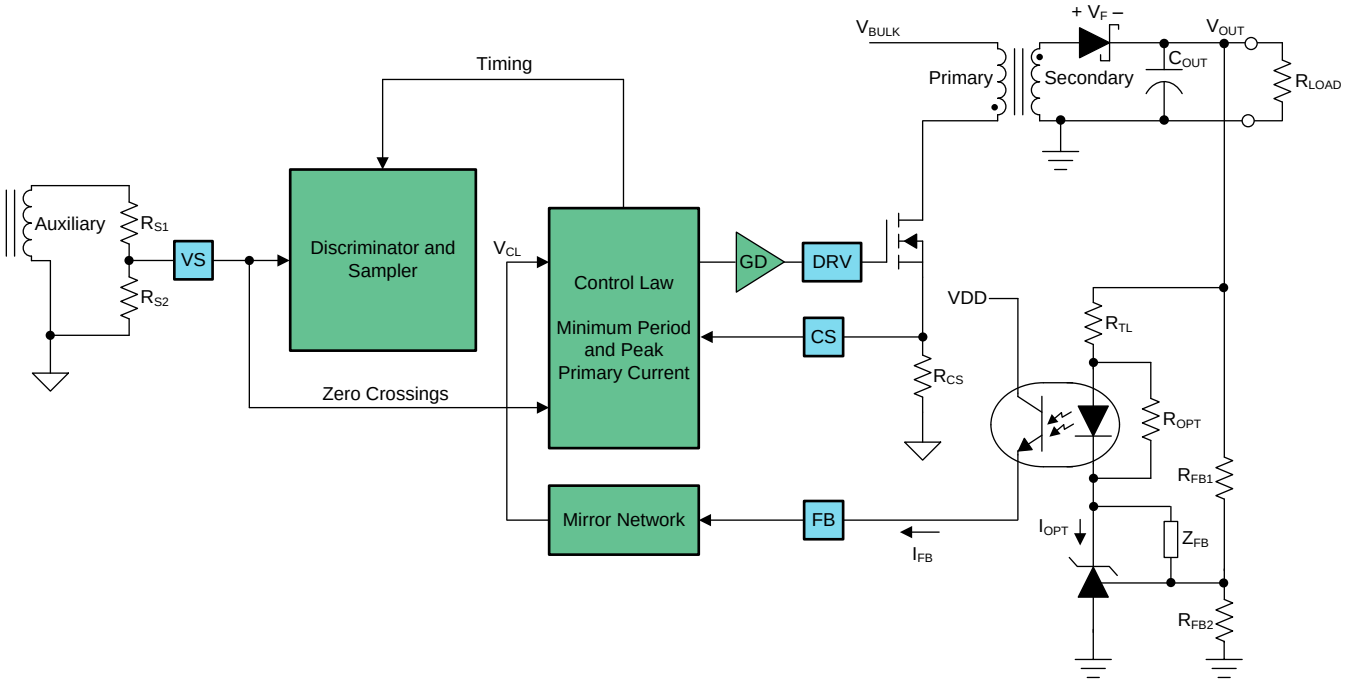


Figure 12. Simplified Flyback Convertor (With the Main Voltage Regulation Blocks)

Device Functional Modes (continued)

In this configuration, a secondary-side shunt-regulator, such as the TL431, generates a current through the input photo-diode of an optocoupler. The photo-transistor delivers a proportional current that is dependent on the current-transfer ratio (CTR) of the optocoupler to the FB input of the UCC28740 controller. This FB current then converts into the V_{CL} by the input-mirror network, detailed in the device block diagram (see *Functional Block Diagram*). Output-voltage variations convert to FB-current variations. The FB-current variations modify the V_{CL} which dictates the appropriate I_{PP} and f_{SW} necessary to maintain CV regulation. At the same time, the VS input senses the auxiliary winding voltage during the transfer of transformer energy to the secondary output to monitor for an output overvoltage condition. When f_{SW} reaches the target maximum frequency, chosen between 32 kHz and 100 kHz, CC operation is entered and further increases in V_{CL} have no effect.

Figure 13 shows that as the secondary current decreases to zero, a clearly defined down slope reflects the decreasing rectifier V_F combined with stray resistance voltage-drop ($I_S R_S$). To achieve an accurate representation of the secondary output voltage on the auxiliary winding, the discriminator reliably blocks the leakage-inductance reset and ringing while continuously sampling the auxiliary voltage during the down slope after the ringing diminishes. The discriminator then captures the voltage signal at the moment that the secondary-winding current reaches zero. The internal overvoltage threshold on VS is 4.6 V. Temperature compensation of –0.8 mV/°C on the overvoltage threshold offsets the change in the output-rectifier forward voltage with temperature. The resistor divider is selected as outlined in the VS pin description (see *Detailed Pin Description*).

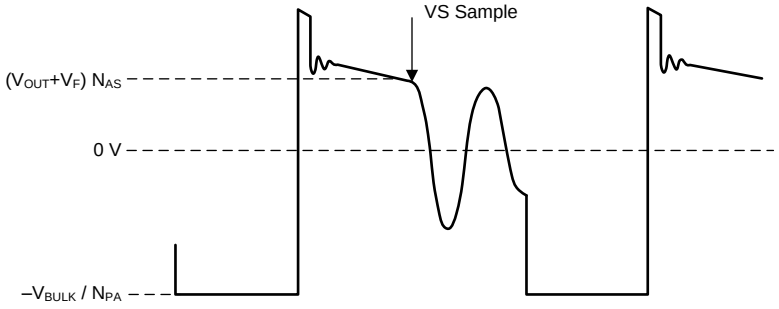


Figure 13. Auxiliary-Winding Voltage

The UCC28740 VS-signal sampler includes signal-discrimination methods to ensure an accurate sample of the output voltage from the auxiliary winding. Controlling some details of the auxiliary-winding signal to ensure reliable operation is necessary; specifically, the reset time of the leakage inductance and the duration of any subsequent leakage-inductance ringing. See Figure 14 for a detailed illustration of waveform criteria to ensure a reliable sample on the VS pin.

The first detail to examine is the duration of the leakage-inductance reset pedestal, t_{LK_RESET}, in Figure 14. Because t_{LK_RESET} mimics the waveform of the secondary-current decay, followed by a sharp downslope, t_{LK_RESET} is internally blanked for a duration which scales with the peak primary current. Keeping the leakage-reset time to less than 600 ns for $I_{PP(min)}$, and less than 2.2 µs for $I_{PP(max)}$ is important.

The second detail is the amplitude of ringing on the V_{AUX} waveform following t_{LK_RESET}. The peak-to-peak voltage variation at the VS pin must be less than 100 mVp-p for at least 200 ns before the end of the demagnetization time (t_{DM}). A concern with excessive ringing usually occurs during light or no-load conditions, when t_{DM} is at the minimum. The tolerable ripple on VS is scaled up to the auxiliary-winding voltage by R_{S1} and R_{S2}, and is equal to 100 mV × (R_{S1} + R_{S2}) / R_{S2} .

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Device Functional Modes (continued)

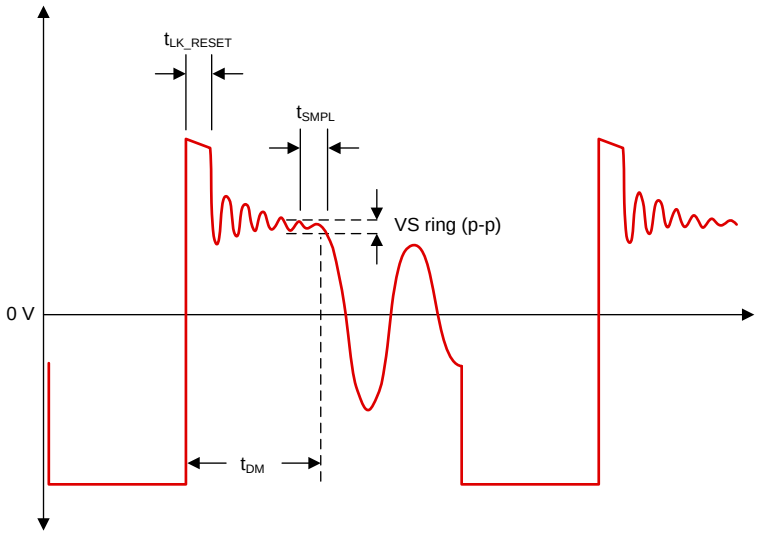


Figure 14. Auxiliary-Winding Waveform Details

During voltage regulation, the controller operates in frequency-modulation mode and amplitude-modulation mode, as shown in Figure 15. The internal operating-frequency limits of the device are 100 kHz and $f_{SW(min)}$. The maximum operating frequency of the converter at full-load is generally chosen to be slightly lower than 100 kHz to allow for tolerances, or significantly lower due to switching-loss considerations. The maximum operating frequency and primary peak current chosen determine the transformer primary inductance of the converter. The shunt-regulator bias power, output preload resistor (if any), and low-power conversion efficiency determine the minimum-operating frequency of the converter. Voltage-loop stability compensation is applied at the shunt-regulator which drives the opto-coupled feedback signal. The tolerances chosen for the shunt-regulator reference and the sense resistors determines the regulation accuracy.

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Device Functional Modes (continued)

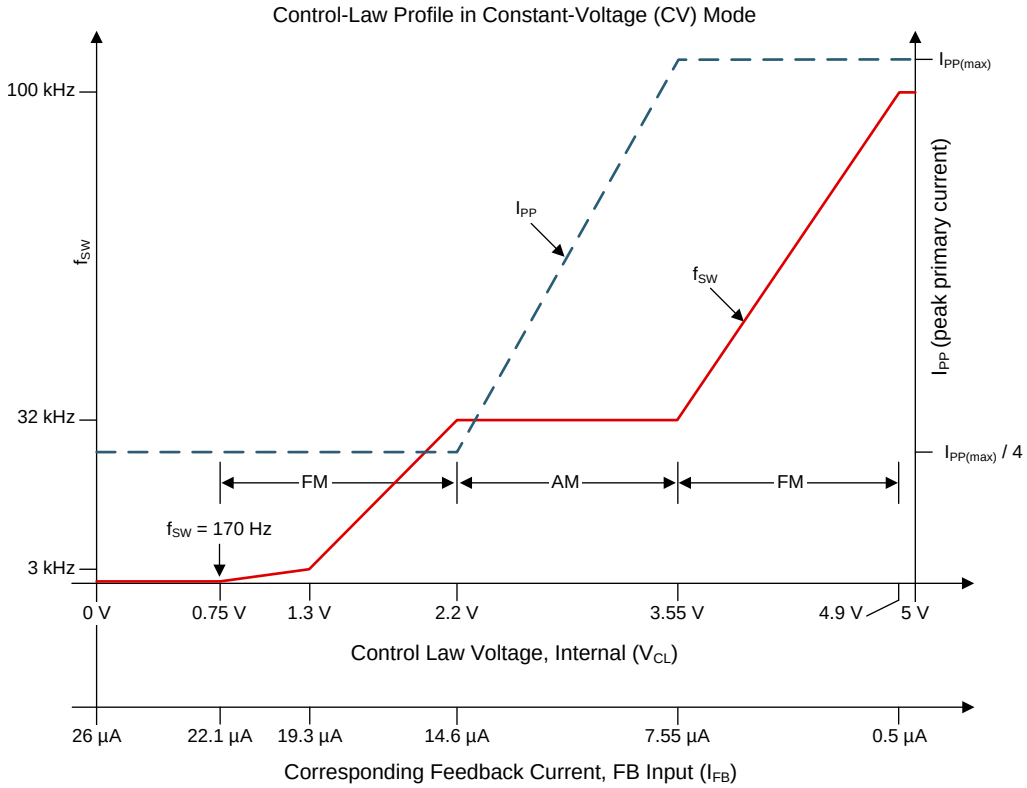


Figure 15. Frequency and Amplitude Modulation Modes (During CV Regulation)

The level of feedback current (I_{FB}) into the FB pin determines the internal V_{CL} which determines the operating point of the controller while in CV mode. When I_{FB} rises above 22 µA, no further decrease in f_{SW} occurs. When the output-load current increases to the point where maximum f_{SW} is reached, control transfers to CC mode. All current, voltage, frequency, breakpoints, and curve-segment linearity depicted in Figure 15 are nominal. Figure 15 indicates the general operation of the controller while in CV mode, although minor variations may occur from part to part. An internal frequency-dithering mechanism is enabled when I_{FB} is less than 14.6 µA to help reduce conducted EMI (including during CC-mode operation), and is disabled otherwise.

7.4.2 Primary-Side Constant-Current (CC) Regulation

When the load current of the converter increases to the predetermined constant-current limit, operation enters CC mode. In CC mode, output voltage regulation is lost and the shunt-regulator drives the current and voltage at FB to minimum. During CC mode, timing information at the VS pin and current information at the CS pin allow accurate regulation of the average current of the secondary winding. The CV-regulation control law dictates that as load increases approaches CC regulation the primary peak current will be at $I_{PP(max)}$. The primary peak current, turns-ratio, demagnetization time t_{DM}, and switching period t_{SW} determine the secondary average output current (see Figure 16). Ignoring leakage-inductance effects, the average output current is given by Equation 5. When the demagnetization duty-cycle reaches the CC-regulation reference, D_{MAGCC}, in the current-control block, the controller operates in frequency modulation (FM) mode to control the output current for any output voltage at or below the voltage-regulation target as long as the auxiliary winding keeps V_{VDD} above the UVLO turnoff threshold. As the output voltage falls, t_{DM} increases. The controller acts to increase t_{SW} to maintain the ratio of t_{DM} to switching period (t_{DM} / t_{SW}) at a maximum of 0.425 (D_{MAGCC}), thereby maintaining a constant average output current.

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Device Functional Modes (continued)

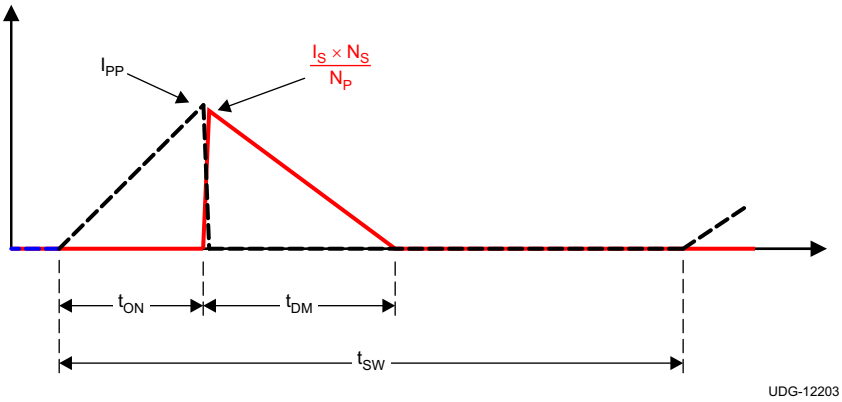


Figure 16. Transformer-Current Relationship

$$I_{OUT} = \frac{I_{PP}}{2} \times \frac{N_P}{N_S} \times \frac{t_{DM}}{t_{SW}} \quad (5)$$

Fast, accurate, opto-coupled CV control combined with line-compensated PSR CC control results in high-performance voltage and current regulation which minimizes voltage deviations due to heavy load and unload steps, as illustrated by the V-I curve in Figure 17.

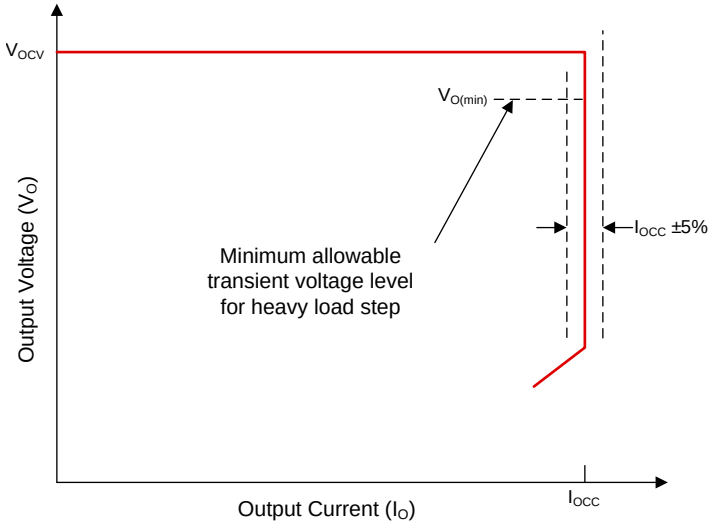


Figure 17. Typical Target Output V-I Characteristic

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

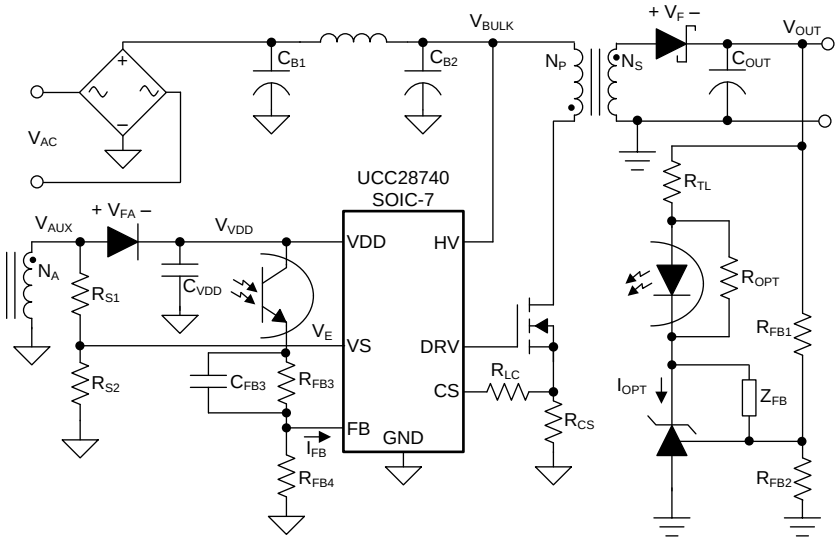
8.1 Application Information

The UCC28740 is a flyback controller that provides constant-voltage (CV) mode control and constant current (CC) mode control for precise output regulation. While in CV operating range, the controller uses an opto-coupler for tight voltage regulation and improved transient response to large load steps. Accurate regulation while in CC mode is provided by primary side control. The UCC28740 uses frequency modulation, peak primary current modulation, valley switching and valley hopping in its control algorithm in order to maximize efficiency over the entire operating range.

8.2 Typical Application

The UCC28740 is well suited for use in isolated off-line systems requiring high efficiency and fault protection features such as USB compliant adapters and chargers for consumer electronics such a smart phones, tablet computers, and cameras. A 10-W application for a USB charger is shown in Figure 18.

This procedure outlines the steps to design a constant-voltage, constant-current flyback converter using the UCC28740 controller. See Figure 18 for component names and network locations. The design procedure equations use terms that are defined below.



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Figure 18. Design Procedure Application Example

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Typical Application (continued)

8.2.1 Design Requirements

Table 1. Design Parameters

PARAMETER	NOTES AND CONDITIONS	MIN	NOM	MAX	UNIT
INPUT CHARACTERISTICS					
Input Voltage, V_{IN}		85	115/230	265	V_{RMS}
Maximum Input Current	$V_{IN} = V_{INmin}$, $I_{OUT} = I_{OUTmax}$		0.265		A_{RMS}
Line Frequency		47	60/50	63	Hz
No Load Input Power Consumption	$V_{INmin} \le V_{IN} \le V_{INmax}$, $I_{OUT} = 0$ A			20	mW
OUTPUT CHARACTERISTICS					
Output Voltage, V_{OUT}	$V_{INmin} \le V_{IN} \le V_{INmax}$, 0 A $\le I_{OUT} \le I_{OUTmax}$	4.95	5	5.05	V
Output Load Current, CV Mode, I_{OUTmax}	$V_{INmin} \le V_{IN} \le V_{INmax}$	1.995	2.1	2.205	A
Output Voltage Regulation	Line Regulation: $V_{INmin} \le V_{IN} \le V_{INmax}$, $I_{OUT} \le I_{OUTmax}$		0.1%		
	Load Regulation: 0 A $\le I_{OUT} \le I_{OUTmax}$		0.1%		
Output Voltage Ripple	$V_{INmin} \le V_{IN} \le V_{INmax}$, 0 A $\le I_{OUT} \le I_{OUTmax}$			150	mVpp
Output Overcurrent, I_{CCC}	$V_{INmin} \le V_{IN} \le V_{INmax}$			2.5	A
Minimum Output Voltage, CC Mode	$V_{INmin} \le V_{IN} \le V_{INmax}$, $I_{OUT} = I_{OCC}$		1.78	2	V
Brown-out Protection	$I_{OUT} = I_{OUTmax}$		68		V_{RMS}
Transient Response Undershoot	$I_{OUT} = I_{OUTmax}$ to 0-A load transient	4.3			V
Transient Response Time	$I_{OUT} = I_{OUTmax}$ to 0-A load transient			20	ms
SYSTEMS CHARACTERISTICS					
Switching Frequency, f_{SW}		1.2		71	kHz
Average Efficiency	25%, 50%, 75%, 100% load average at nominal input voltages		81%		
Operating Temperature			25		°C

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the UCC28740 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

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8.2.2.2 Standby Power Estimate and No-Load Switching Frequency

Assuming minimal no-load standby power is a critical design requirement, determine the estimated no-load power loss based on an accounting of all no-load operating and leakage currents at their respective voltages. Close attention to detail is necessary to account for all of the sources of leakage, however, in many cases, prototype measurement is the only means to obtain a realistic estimation of total primary and secondary leakage currents. At present, converter standby power is certified by compliance-agency authorities based on steady-state room-temperature operation at the highest nominal input voltage rating (typically 230 Vrms).

Equation 6 estimates the standby power loss from the sum of all leakage currents of the primary-side components of the converter. These leakage currents are measured in aggregate by disconnecting the HV input of the controller from the bulk-voltage rail to prevent operating currents from interfering with the leakage measurement.

$$P_{PRI_SB} = V_{BULK} \times \sum_{k=1}^{n_P} I_{PRI_LK_K} \tag{6}$$

Equation 7 estimates the standby power loss from the sum of all leakage and operating currents of the secondary-side components on the output of the converter. Leakage currents result from reverse voltage applied across the output rectifier and capacitors, while the operating current includes currents required by the shunt-regulator, optocoupler, and associated components.

$$P_{SEC_SB} = V_{OCV} \times \sum_{k=1}^{n_S} I_{SEC_K} \tag{7}$$

Equation 8 estimates the standby power loss from the sum of all leakage and operating currents of the auxiliary-side components on the controller of the converter. Leakage currents of the auxiliary diode and capacitor are usually negligible. The operating current includes the wait-state current, I_{WAIT}, of the UCC28740 controller, plus the optocoupler-output current for the FB network in the steady-state no-load condition. The VDD voltage in the no-load condition V_{VDDNL} are the lowest practicable value to minimize loss.

$$P_{AUX_SB} = V_{VDDNL} \times \sum_{k=1}^{n_a} I_{AUX_K} \tag{8}$$

Note that P_{PRI_SB} is the only loss that is not dependent on transformer conversion efficiency. P_{SEC_SB} and P_{AUX_SB} are processed through the transformer and incur additional losses as a consequence. Typically, the transformer no-load conversion efficiency η_{SWNL} lies in the range of 0.50 to 0.70. Total standby input power (no-load condition) is estimated by Equation 9.

$$P_{SB} = P_{PRI_SB} + \frac{1}{\eta_{SWNL}}\left(P_{SEC_SB} + P_{AUX_SB}\right) \tag{9}$$

Although the UCC28740 is capable of operating at the minimum switching frequency of 170 Hz, a typical converter is likely to require a higher frequency to sustain operation at no-load. An accurate estimate of the no-load switching frequency f_{SWNL} entails a thorough accounting of all switching-related energy losses within the converter including parasitic elements of the power-train components. In general, f_{SWNL} is likely to lie within the range of 400 Hz to 800 Hz. A more detailed treatment of standby power and no-load frequency is beyond the scope of this data sheet.

8.2.2.3 Input Bulk Capacitance and Minimum Bulk Voltage

Determine the minimum voltage on the input bulk capacitance, C_{B1} and C_{B2} total, in order to determine the maximum Np-to-Ns turns-ratio of the transformer. The input power of the converter based on target full-load efficiency, the minimum input RMS voltage, and the minimum AC input frequency determine the input capacitance requirement.

Maximum input power is determined based on I_{OCC}, V_{OCV}, V_{CBC} (if used), and the full-load conversion-efficiency target.

$$P_{IN} = \frac{\left(V_{OCV} + V_{CBC}\right) \times I_{OCC}}{\eta} \tag{10}$$

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Equation 11 provides an accurate solution for the total input capacitance based on a target minimum bulk-capacitor voltage. Alternatively, to target a given input capacitance value, iterate the minimum capacitor voltage to achieve the target capacitance value.

$$C_{BULK} = \frac{2P_{IN} \times \left(0.25 + \frac{1}{2\pi} \times \arcsin\left(\frac{V_{BULK(min)}}{\sqrt{2} \times V_{IN(min)}} \right) \right)}{\left(2V_{IN(min)}^{2} - V_{BULK(min)}^{2} \right) \times f_{LINE}} \quad (11)$$

8.2.2.4 Transformer Turns-Ratio, Inductance, Primary Peak Current

The target maximum switching frequency at full-load, the minimum input-capacitor bulk voltage, and the estimated DCM resonant time determine the maximum primary-to-secondary turns-ratio of the transformer.

Initially determine the maximum-available total duty-cycle of the on-time and secondary conduction time based on the target switching frequency, f_{MAX}, and DCM resonant time. For DCM resonant frequency, assume 500 kHz if an estimate from previous designs is not available. At the transition-mode operation limit of DCM, the interval required from the end of secondary current conduction to the first valley of the V_{DS} voltage is ½ of the DCM resonant period (t_R), or 1 µs assuming 500 kHz resonant frequency. The maximum allowable MOSFET on-time D_{MAX} is determined using Equation 12.

$$D_{MAX} = 1 - D_{MAGCC} - \left(\frac{t_R}{2} \times f_{MAX} \right) \quad (12)$$

When D_{MAX} is known, the maximum primary-to-secondary turns-ratio is determined with Equation 13. D_{MAGCC} is defined as the secondary-diode conduction duty-cycle during CC operation and is fixed internally by the UCC28740 at 0.425. The total voltage on the secondary winding must be determined, which is the sum of V_{OCV}, V_F, and V_{OCBC}. For the 5-V USB-charger applications, a turns ratio range of 13 to 15 is typically used.

$$N_{PS(max)} = \frac{D_{MAX} \times V_{BULK(min)}}{D_{MAGCC} \times \left(V_{OCV} + V_F + V_{OCBC} \right)} \quad (13)$$

A higher turns-ratio generally improves efficiency, but may limit operation at low input voltage. Transformer design iterations are generally necessary to evaluate system-level performance trade-offs. When the optimum turns-ratio N_{PS} is determined from a detailed transformer design, use this ratio for the following parameters.

The UCC28740 constant-current regulation is achieved by maintaining D_{MAGCC} at the maximum primary peak current setting. The product of D_{MAGCC} and $V_{CST(max)}$ defines a CC-regulating voltage factor V_{CCR} which is used with N_{PS} to determine the current-sense resistor value necessary to achieve the regulated CC target, I_{OCC} (see Equation 14).

Because a small portion of the energy stored in the transformer does not transfer to the output, a transformer-efficiency term is included in the R_{CS} equation. This efficiency number includes the core and winding losses, the leakage-inductance ratio, and a bias-power to maximum-output-power ratio. An overall-transformer efficiency of 0.91 is a good estimate based on 3.5% leakage inductance, 5% core & winding loss, and 0.5% bias power, for example. Adjust these estimates as appropriate based on each specific application.

$$R_{CS} = \frac{V_{CCR} \times N_{PS}}{2I_{OCC}} \times \sqrt{\eta_{XFMR}} \quad (14)$$

The primary transformer inductance is calculated using the standard energy storage equation for flyback transformers. Primary current, maximum switching frequency, output voltage and current targets, and transformer power losses are included in Equation 16.

First, determine the transformer primary peak current using Equation 15. Peak primary current is the maximum current-sense threshold divided by the current-sense resistance.

$$I_{PP(max)} = \frac{V_{CST(max)}}{R_{CS}} \quad (15)$$

$$L_P = \frac{2\left(V_{OCV} + V_F + V_{OCBC} \right) \times I_{OCC}}{\eta_{XFMR} \times I_{PP(max)}^{2} \times f_{MAX}} \quad (16)$$

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N_{AS} is determined by the lowest target operating output voltage while in constant-current regulation and by the VDD UVLO turnoff threshold of the UCC28740. Additional energy is supplied to VDD from the transformer leakage-inductance which allows a lower turns ratio to be used in many designs.

$$N_{AS} = \frac{V_{VDD(off)} + V_{FA}}{V_{OCC} + V_F} \quad (17)$$

8.2.2.5 Transformer Parameter Verification

Because the selected transformer turns-ratio affects the MOSFET V_{DS} and the secondary and auxiliary rectifier reverse voltages, a review of these voltages is important. In addition, internal timing constraints of the UCC28740 require a minimum on time of the MOSFET (t_{ON}) and a minimum demagnetization time (t_{DM}) of the transformer in the high-line minimum-load condition. The selection of f_{MAX}, L_P, and R_{CS} affects the minimum t_{ON} and t_{DM}.

Equation 18 and Equation 19 determine the reverse voltage stresses on the secondary and auxiliary rectifiers. Stray inductance can impress additional voltage spikes upon these stresses and snubbers may be necessary.

$$V_{REVS} = \frac{V_{IN(max)} \times \sqrt{2}}{N_{PS}} \times V_{OV} \quad (18)$$

$$V_{REVA} = \frac{V_{IN(max)} \times \sqrt{2}}{N_{PA}} \times V_{VDD} \quad (19)$$

For the MOSFET V_{DS} peak voltage stress, an estimated leakage inductance voltage spike (V_{LK}) is included.

$$V_{DSPK} = \left(V_{IN(max)} \times \sqrt{2}\right) + \left(V_{OCV} + V_F + V_{OCBC}\right) \times N_{PS} + V_{LK} \quad (20)$$

Equation 21 determines if $t_{ON(min)}$ exceeds the minimum t_{ON} target of 280 ns (maximum t_{CSLEB}). Equation 22 verifies that $t_{DM(min)}$ exceeds the minimum t_{DM} target of 1.2 µs.

$$t_{ON(min)} = \frac{L_P}{V_{IN(max)} \times \sqrt{2}} \times \frac{I_{PP(max)}}{K_{AM}} \quad (21)$$

$$t_{DM(min)} = \frac{t_{ON(min)} \times V_{IN(max)} \times \sqrt{2}}{N_{PS} \times \left(V_{OCV} + V_F\right)} \quad (22)$$

8.2.2.6 VS Resistor Divider, Line Compensation

The VS divider resistors determine the output overvoltage detection point of the flyback converter. The high-side divider resistor (R_{S1}) determines the input-line voltage at which the controller enables continuous DRV operation. R_{S1} is determined based on transformer primary-to-auxiliary turns-ratio and desired input voltage operating threshold.

$$R_{S1} = \frac{V_{IN(run)} \times \sqrt{2}}{N_{PA} \times I_{VSL(run)}} \quad (23)$$

The low-side VS pin resistor is then selected based on the desired overvoltage limit, V_{OV}.

$$R_{S2} = \frac{R_{S1} \times V_{OVP}}{N_{AS} \times \left(V_{OV} - V_F\right) - V_{OVP}} \quad (24)$$

The UCC28740 maintains tight constant-current regulation over varying input line by using the line-compensation feature. The line-compensation resistor (R_{LC}) value is determined by current flowing in R_{S1} and the total internal gate-drive and external MOSFET turnoff delay. Assume an internal delay of 50 ns in the UCC28740.

$$R_{LC} = \frac{K_{LC} \times R_{S1} \times R_{CS} \times t_D \times N_{PA}}{L_P} \quad (25)$$

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8.2.2.7 Output Capacitance

The output capacitance value is often determined by the transient-response requirement from the no-load condition. For example, in typical low-power USB-charger applications, there is a requirement to maintain a minimum transient V_O of 4.1 V with a load-step I_{TRAN} from 0 mA to 500 mA. Yet new higher-performance applications require smaller transient voltage droop $V_{O\Delta}$ with I_{TRAN} of much greater amplitude (such as from no-load to full-load), which drives the need for high-speed opto-coupled voltage feedback.

$$C_{OUT} \geq \frac{I_{TRAN} \times t_{RESP}}{V_{O\Delta}}$$

where

- t_{RESP} is the time delay from the moment I_{TRAN} is applied to the moment when I_{FB} falls below 1 µA (26)

Additional considerations for the selection of appropriate output capacitors include ripple-current, ESR, and ESL ratings necessary to meet reliability and ripple-voltage requirements. Detailed design criteria for these considerations are beyond the scope of this datasheet.

8.2.2.8 VDD Capacitance, C_{VDD}

The capacitance on VDD must supply the primary-side operating current used during startup and between low-frequency switching pulses. The largest result of three independent calculations denoted in Equation 27, Equation 28, and Equation 29 determines the value of C_{VDD}.

At startup, when $V_{VDD(on)}$ is reached, C_{VDD} alone supplies the device operating current and MOSFET gate current until the output of the converter reaches the target minimum-operating voltage in CC regulation, V_{OCC}. Now the auxiliary winding sustains VDD for the UCC28740 above UVLO. The total output current available to the load and to charge the output capacitors is the CC-regulation target, I_{OCC}. Equation 27 assumes that *all* of the output current of the converter is available to charge the output capacitance until V_{OCC} is achieved. For typical applications, Equation 27 includes an estimated $q_G f_{SW(max)}$ of average gate-drive current and a 1-V margin added to V_{VDD}.

$$C_{VDD} \geq \frac{\left(I_{RUN} + q_G f_{SW(max)}\right) \times \frac{C_{OUT} \times V_{OCC}}{I_{OCC}}}{V_{DD(on)} - \left(V_{VDD(off)} + 1\,V\right)} \quad (27)$$

During a worst-case un-load transient event from full-load to no-load, C_{OUT} overcharges above the normal regulation level for a duration of t_{OV}, until the output shunt-regulator loading is able to drain V_{OUT} back to regulation. During t_{OV}, the voltage feedback loop and optocoupler are saturated, driving maximum I_{FB} and temporarily switching at $f_{SW(min)}$. The auxiliary bias current expended during this situation exceeds that normally required during the steady-state no-load condition. Equation 28 calculates the value of C_{VDD} (with a safety factor of 2) required to ride through the t_{OV} duration until steady-state no-load operation is achieved.

$$C_{VDD} \geq \frac{2 \times I_{AUXNL(max)} \times t_{OV}}{V_{VDDFL} - \left(V_{VDD(off)} + 1\,V\right)} \quad (28)$$

Finally, in the steady-state no-load operating condition, total no-load auxiliary-bias current, I_{AUXNL} is provided by the converter switching at a no-load frequency, f_{SWNL}, which is generally higher than $f_{SW(min)}$. C_{VDD} is calculated to maintain a target VDD ripple voltage lower than ΔV_{VDD}, using Equation 29.

$$C_{VDD} \geq \frac{I_{AUXNL} \times \frac{1}{f_{SWNL}}}{\Delta V_{VDD}} \quad (29)$$

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8.2.2.9 Feedback Network Biasing

Achieving very low standby power while maintaining high-performance load-step transient response requires careful design of the feedback network. Optically coupled secondary-side regulation is used to provide the rapid response needed when a heavy load step occurs during the no-load condition. One of the most commonly used devices to drive the optocoupler is the TL431 shunt-regulator, due to its simplicity, regulation performance, and low cost. This device requires a minimum bias current of 1 mA to maintain regulation accuracy. Together with the UCC28740 primary-side controller, careful biasing will ensure less than 30 mW of standby power loss at room temperature. Where a more stringent standby loss limit of less than 10 mW is required, the TLV431 device is recommended due to its minimum 80-µA bias capability.

Facilitating these low standby-power targets is the approximate 23-µA range of the FB input for full to no-load voltage regulation. The control-law profile graph (see Figure 15) shows that for FB-input current greater than 22 µA, no further reduction in switching frequency is possible. Therefore, minimum power is converted at $f_{SW(min)}$. However, the typical minimum steady-state operating frequency tends to be in the range of several-hundred Hertz, and consequently the maximum steady-state FB current at no-load will be less than I_{FBMAX}. Even so, prudent design practice dictates that I_{FBMAX} should be used for conservative steady-state biasing calculations. At this current level, V_{FBMAX} can be expected at the FB input.

Referring to the Design Procedure Application Example in Figure 18, the main purpose of R_{FB4} is to speed up the turnoff time of the optocoupler in the case of a heavy load-step transient condition. The value of R_{FB4} is determined empirically due to the variable nature of the specific optocoupler chosen for the design, but tends to fall within the range of 10 kΩ to 100 kΩ. A tradeoff must be made between a lower value for faster transient response and a higher value for lower standby power. R_{FB4} also serves to set a minimum bias current for the optocoupler and to drain dark current.

It is important to understand the distinction between *steady-state* no-load bias currents and voltages which affect standby power, and the varying extremes of these same currents and voltages which affect regulation during transient conditions. Design targets for minimum standby loss and maximum transient response often result in conflicting requirements for component values. Trade-offs, such as for R_{FB4} as discussed previously, must be made.

During standby operation, the total auxiliary current (used in Equation 8) is the sum of I_{WAIT} into the IC and the no-load optocoupler-output current I_{CENL}. This optocoupler current is given by Equation 30.

$$I_{CENL} = I_{FBMAX} + \frac{V_{FBMAX}}{R_{FB4}} \tag{30}$$

For fast response, the optocoupler-output transistor is biased to minimize the variation of V_{CE} between full-load and no-load operation. Connecting the emitter directly to the FB input of the UCC28740 is possible, however, an unload-step response may unavoidably drive the optocoupler into saturation which will overload the FB input with full VDD applied. A series-resistor R_{FB3} is necessary to limit the current into FB and to avoid excess draining of C_{VDD} during this type of transient situation. The value of R_{FB3} is chosen to limit the excess I_{FB} and R_{FB4} current to an acceptable level when the optocoupler is saturated. Like R_{FB4}, the R_{FB3} value is also chosen empirically during prototype evaluation to optimize performance based on the conditions present during that situation. A starting value may be estimated using Equation 31.

$$R_{FB3} = \frac{V_{VDDNL} - 1\,V}{I_{CENL}} \tag{31}$$

Note that R_{FB3} is estimated based on the expected no-load VDD voltage, but full-load VDD voltage will be higher resulting in initially higher I_{CE} current during the unload-step transient condition. Because R_{FB3} is interposed between V_E and the FB input, the optocoupler transistor V_{CE} varies considerably more as I_{CE} varies and transient response time is reduced. Capacitor C_{FB3} across R_{FB3} helps to improve the transient response again. The value of C_{FB3} is estimated initially by equating the $R_{FB3}C_{FB3}$ time constant to 1 ms, and later is adjusted higher or lower for optimal performance during prototype evaluation.

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The optocoupler transistor-output current I_{CE} is proportional to the optocoupler diode input current by its current transfer ratio, CTR. Although many optocouplers are rated with nominal CTR between 50% and 600%, or are ranked into narrower ranges, the actual CTR obtained at the low currents used with the UCC28740 falls around 5% to 15%. At full-load regulation, when I_{FB} is near zero, V_{FB} is still approximately 0.4 V and this sets a minimum steady-state current for I_{CE} through R_{FB4}. After choosing an optocoupler, the designer must characterize its CTR over the range of low output currents expected in this application, because optocoupler data sheets rarely include such information. The actual CTR obtained is required to determine the diode input current range at the secondary-side shunt-regulator.

Referring again to Figure 18, the shunt-regulator (typically a TL431) current must be at least 1 mA even when almost no optocoupler diode current flows. Since even a near-zero diode current establishes a forward voltage, R_{OPT} is selected to provide the minimum 1-mA regulator bias current. The optocoupler input diode must be characterized by the designer to obtain the actual forward voltage versus forward current at the low currents expected. At the full-load condition of the converter, I_{FB} is around 0.5 µA, I_{CE} may be around (0.4 V / R_{FB4}), and CTR at this level is about 10%, so the diode current typically falls in the range of 25 µA to 100 µA. Typical opto-diode forward voltage at this level is about 0.97 V which is applied across R_{OPT}. If R_{OPT} is set equal to 1 kΩ, this provides 970 µA plus the diode current for I_{OPT}.

As output load decreases, the voltage across the shunt-regulator also decreases to increase the current through the optocoupler diode. This increases the diode forward voltage across R_{OPT}. CTR at no-load (when I_{CE} is higher) is generally a few percent higher than CTR at full-load (when I_{CE} is lower). At steady-state no-load condition, the shunt-regulator current is maximized and can be estimated by Equation 30 and Equation 32. I_{OPTNL}, plus the sum of the leakage currents of all the components on the output of the converter, constitute the total current required for use in Equation 7 to estimate secondary-side standby loss.

$$I_{OPTNL} = \frac{I_{CENL}}{CTR_{NL}} + \frac{V_{OPTNL}}{R_{OPT}} \tag{32}$$

The shunt-regulator voltage can decrease to a minimum, saturated level of about 2 V. To prevent excessive diode current, a series resistor, R_{TL}, is added to limit I_{OPT} to the maximum value necessary for regulation. Equation 33 provides an estimated initial value for R_{TL}, which may be adjusted for optimal limiting later during the prototype evaluation process.

$$R_{TL} = \frac{V_{OUTNL} - V_{OPTNL} - 2\ V}{I_{OPTNL}} \tag{33}$$

The output-voltage sense-network resistors R_{FB1} and R_{FB2} are calculated in the usual manner based on the shunt-regulator reference voltage and input bias current. Having characterized the optocoupler at low currents and determined the initial values of R_{FB1}, R_{FB2}, R_{FB3}, R_{FB4}, C_{FB3}, R_{OPT} and R_{TL} using the above procedure, the DC-bias states of the feedback network can be established for steady-state full-load and no-load conditions. Adjustments of these initial values may be necessary to accommodate variations of the UCC28740, optocoupler, and shunt-regulator parameters for optimal overall performance.

The shunt-regulator compensation network, Z_{FB}, is determined using well-established design techniques for control-loop stability. Typically, a type-II compensation network is used. The compensation design procedure is beyond the scope of this datasheet.

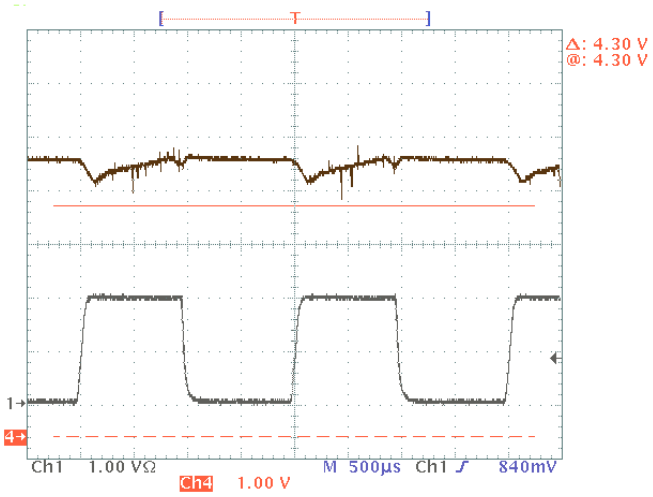
8.2.3 Application Curves

The transient response shown in Figure 19 was taken with a 115 VAC, 60 Hz input voltage and a load transition from 0 A to full load. Channel 1 is the load current on a scale of 1 A per division, channel 4 is the otutput voltage on a scale of 1 V per division. The cursor shows the minimum acceptable voltage limit, 4.30 V, under transient conditions. Also note that the output waveform was taken with the probe on TP5 with the ground referenced to TP4 but not using the tip and barrel technique accounting for the high frequency noise seen on the waveform.

The typical switching waveform can be seen in Figure 20. Channel 1 shows the VS pin at 2 V per division and channel 2 shows the MOSFET drain to source voltage at 100 V per division. The scan was taken at 1.8-A load, 115-VAC, 60-Hz input voltage. At this operating point, the switching frequency is dithering between 58.8 kHz and 52.6 kHz due to valley skipping.

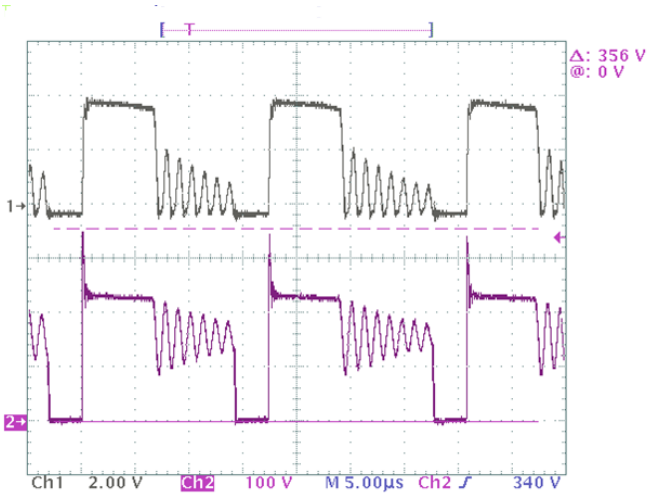
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The UCC28740 controller employs a unique control mechanism to help with EMI compliance. As shown in Figure 21, the DRV pin, shown as channel 3, drives the gate of the MOSFET with a sequence of pulses in which there will be two longer pulses, two medium pulses, and two shorter pulses at any operating point starting with the amplitude modulation mode. The EMI dithering is not enabled at light load. Figure x shows the result of these varying pulse widths on the CS signal, shown on channel 4. The longer pulses result in a peak current threshold of 808 mV, the medium length pulses are shown measured at 780 mV, and the shorter pulses measure a threshold voltage of 752 mV. This dithering adds to the frequency jitter caused by valley skipping and results in a spread spectrum for better EMI compliance.



115 VAC, 60 Hz 0 A to 2 A
CH 1 = Load Current, 1 A/DIV
CH 4 = VOUT, cursor shows minimum limit

Figure 19. Transient Response



CH 1 = VS CH 2 = V_{DS}
I_{OUT} = 1.8 A V_{IN} = 115 VAC, 60 Hz

Figure 20. Switching Waveform

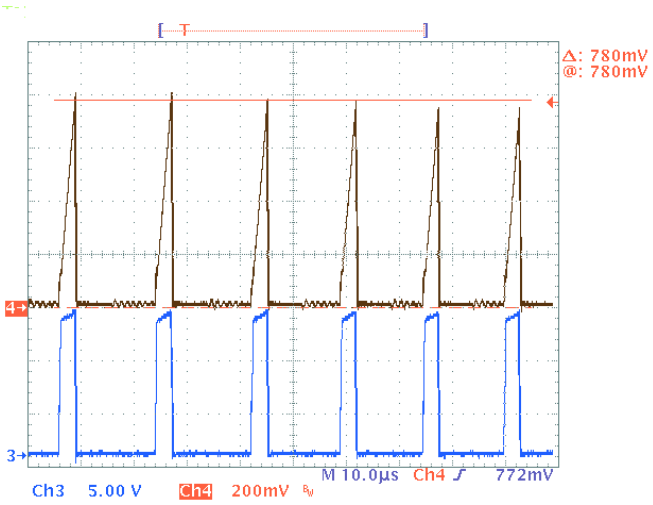


Figure 21. EMI Dithering

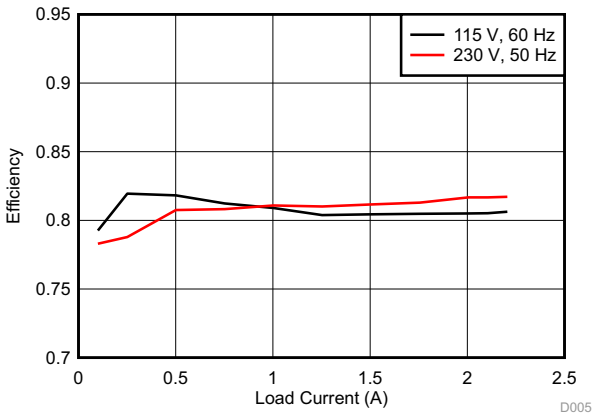


Figure 22. Efficiency

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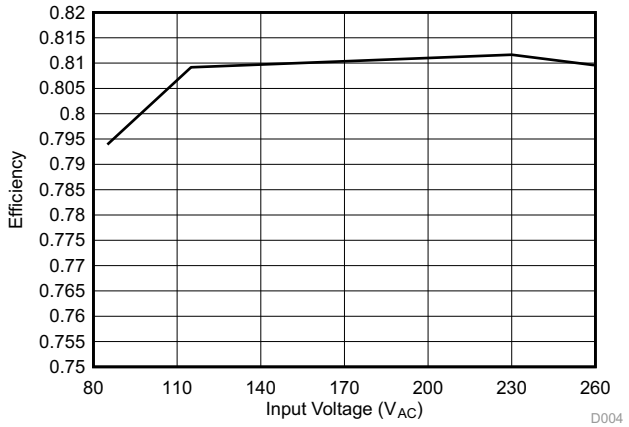


Figure 23. Average Efficiency

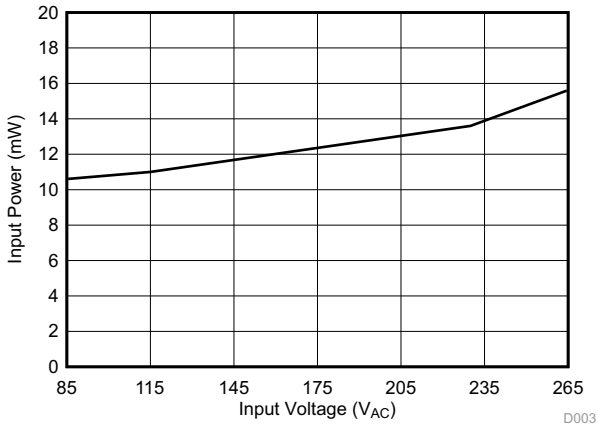


Figure 24. No Load Power Consumption

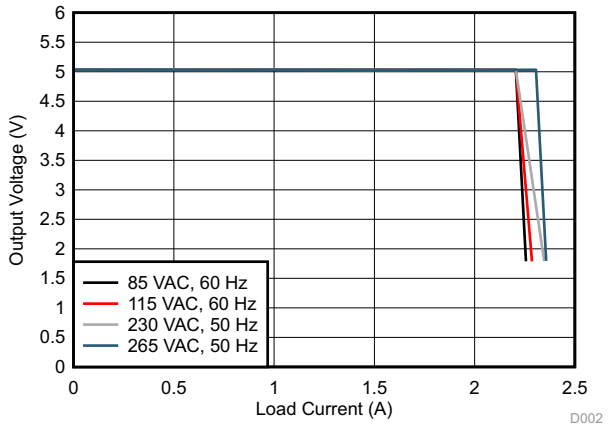


Figure 25. V_{OUT} vs. I_{OUT}

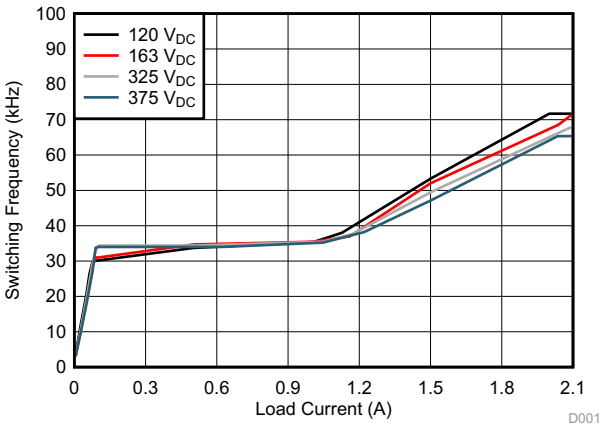
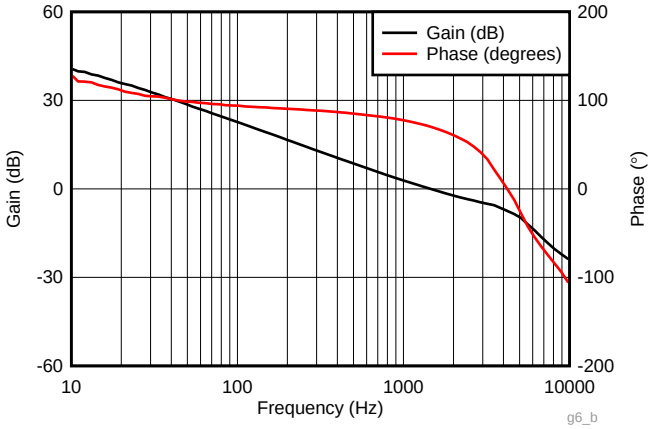


Figure 26. Control Law



V_{IN} = 115 VAC I_{OUT} = 2 A

Figure 27. Bode Plot

9 Power Supply Recommendations

The UCC28740 is designed to be used with a Universal AC input, from 85 VAC to 265 VAC, at 47 Hz to 63 Hz. Other input line conditions can be used provided the HV pin can be set up to provide 500 µA to charge the VDD capacitor for start-up through the internal startup switch. Once the VDD reaches the 21-V UVLO turnon threshold, the VDD rail should be kept within the limits of the Bias Supply Input section of the *Electrical Characteristics* table. To avoid the possibility that the device might stop switching, VDD must not be allowed to fall below the UVLO $V_{VDD(off)}$ range.

10 Layout

10.1 Layout Guidelines

In general, try to keep all high current loops as short as possible. Keep all high current/high frequency traces away from other traces in the design. If necessary, high frequency/high current traces should be perpendicular to signal traces, not parallel to them. Shielding signal traces with ground traces can help reduce noise pick up. Always consider appropriate clearances between the high-voltage connections and any low-voltage nets.

10.1.1 VDD Pin

The VDD pin must be decoupled to GND with good quality, low ESR, low ESL ceramic bypass capacitors with short traces to the VDD and GND pins. The value of the required capacitance on VDD is determined as shown in the *Application and Implementation* section.

10.1.2 VS Pin

The trace between the resistor divider and the VS pin should be as short as possible to reduce/eliminate possible EMI coupling. The lower resistor of the resistor divider network connected to the VS pin should be returned to GND with short traces. Avoid adding any external capacitance to the VS pin so that there is no delay of signal; added capacitance would interfere with the accurate sensing of the timing information used to achieve valley switching and also control the duty cycle of the transformer secondary current.

10.1.3 FB Pin

The PCB tracks from the opto-coupler to the FB pin should have minimal loop area. If possible, it is recommended to provide screening for the FB trace with ground planes. A resistor to GND from the FB pin is recommended to speed up the turnoff time of the opto-coupler during a heavy load step transient. This resistor should be placed as close as possible to FB and GND with short traces, the value of this resistor, RFB4, is detailed in the *Application and Implementation* section.

10.1.4 GND Pin

The GND pin is the power and signal ground connection for the controller. As with all PWM controllers, the effectiveness of the filter capacitors on the signal pins depends upon the integrity of the ground return. Place all decoupling and filter capacitors as close as possible to the device pins with short traces. The IC ground and power ground should meet at the bulk capacitor's return. Try to ensure that high frequency/high current from the power stage does not go through the signal ground.

10.1.5 CS Pin

A small filter capacitor may be placed on CS to GND, with short traces, to filter any ringing that may be present at light load conditions when driving MOSFETs with large gate capacitance. This capacitor may not be required in all designs; however, it is wise to put a place holder for it in your designs. The current sense resistor should be returned to the ground terminal of the input bulk capacitor to minimize the loop area containing the input capacitor, the transformer, the MOSFET, and the current sense resistor.

10.1.6 DRV Pin

The track connected to DRV carries high dv/dt signals. Minimize noise pickup by routing the trace to this pin as far away as possible from tracks connected to the device signal inputs, FB and VS. There is no requirement for a Gate to Source resistor with this device.

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Layout Guidelines (continued)

10.1.7 HV Pin

Sufficient PCB trace spacing must be given between the high-voltage connections and any low-voltage nets. The HV pin may be connected directly, or through series resistance, to the rectified high voltage input rail.

10.2 Layout Example

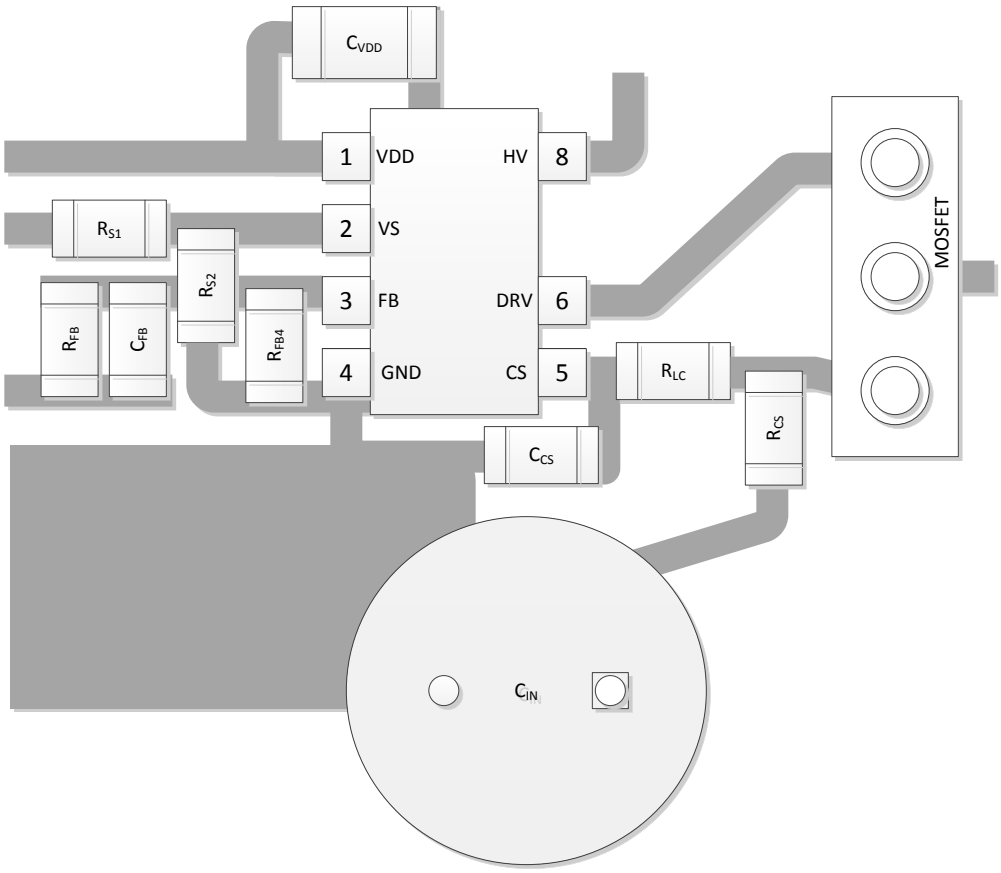


Figure 28. Layout Example Schematic

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 開発サポート

デザイン・ツールについては、UCC28740デザイン・カリキュレータを参照してください。

11.1.1.1 WEBENCH®ツールによるカスタム設計

ここをクリックすると、WEBENCH® Power Designerにより、UCC28740デバイスを使用するカスタム設計を作成できます。

1. 最初に、入力電圧(V_{IN})、出力電圧(V_{OUT})、出力電流(I_{OUT})の要件を入力します。
2. オプティマイザのダイヤルを使用して、効率、占有面積、コストなどの主要なパラメータについて設計を最適化します。
3. 生成された設計を、テキサス・インスツルメンツが提供する他のソリューションと比較します。

WEBENCH Power Designerでは、カスタマイズされた回路図と部品リストを、リアルタイムの価格と部品の在庫情報と併せて参照できます。

ほとんどの場合、次の操作を実行可能です。

- 電気的なシミュレーションを実行し、重要な波形と回路の性能を確認する。
- 熱シミュレーションを実行し、基板の熱特性を把握する。
- カスタマイズされた回路図やレイアウトを、一般的なCADフォーマットでエクスポートする。
- 設計のレポートをPDFで印刷し、同僚と設計を共有する。

WEBENCHツールの詳細は、www.ti.com/WEBENCHでご覧になれます。

11.1.2 デバイスの項目表記

11.1.2.1 容量項(ファラッド単位)

C_{BULK} C_{B1}とC_{B2}の合計入力容量

C_{VDD} VDDピンに必要な最小容量

C_{OUT} 必要な最小出力容量

11.1.2.2 デューティ・サイクル項

D_{MAGCC} 2次側ダイオードのCCモードでの導通デューティ・サイクル制限、0.425

D_{MAX} MOSFETオン時間のデューティ・サイクル

11.1.2.3 周波数項(ヘルツ単位)

f_{LINE} 入力ラインの最小周波数

f_{MAX} コンバータの目標全負荷最大スイッチング周波数

f_{MIN} コンバータの定常状態の最小スイッチング周波数

$f_{SW(min)}$ 可能な最小スイッチング周波数(「*Electrical Characteristics*」を参照)

11.1.2.4 電流項(アンペア単位)

I_{OCC} コンバータの出力定電流目標

$I_{PP(max)}$ 変圧器の最大1次側ピーク電流

I_{START} スタートアップ・バイアス電源電流(「*Electrical Characteristics*」を参照)

I_{TRAN} 必要な正の負荷ステップ電流

$I_{VSL(run)}$ VSピンの実行電流(「*Electrical Characteristics*」を参照)

11.1.2.5 電流および電圧のスケーリング項

K_{AM} ピーク1次側電流の最大値と最小値の比率(「*Electrical Characteristics*」を参照)

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デバイス・サポート (continued)

K_{LC} ライン補償の電流スケーリング定数(「*Electrical Characteristics*」を参照)

11.1.2.6 変圧器の項

L_P 変圧器の1次側インダクタンス

N_{AS} 変圧器の補助と2次側の巻線比

N_{PA} 変圧器の1次側と補助の巻線比

N_{PS} 変圧器の1次側と2次側の巻線比

11.1.2.7 電力項(ワット単位)

P_{IN} コンバータの最大入力電力

P_{OUT} コンバータの全負荷出力電力

P_{SB} スタンバイ時の合計電力

11.1.2.8 抵抗項(オーム単位)

R_{CS} 1次側ピーク電流プログラミング抵抗

R_{ESR} 出力コンデンサの合計ESR

R_{PL} コンバータの出力のプリロード抵抗

R_{S1} ハイサイドVSピン検出抵抗

R_{S2} ローサイドVSピン検出抵抗

11.1.2.9 タイミング項(秒単位)

t_D MOSFETのターンオフ遅延を含む合計電流検出遅延時間、MOSFET遅延に50nsを加算

$t_{DM(min)}$ 2次側整流器の最小導通時間

$t_{ON(min)}$ MOSFETの最小オン時間

t_R DCMデッドタイム中の共振周波数

t_{RESP} 必要な最大負荷ステップに対する、電圧レギュレーション制御ループの最大応答時間

11.1.2.10 電圧項(ボルト単位)

V_{BLK} スタンバイ時電力測定用の最大バルク・コンデンサ電圧

$V_{BULK(min)}$ 最大電力時のC_{B1}およびC_{B2}の最小のバレー電圧

V_{CCR} 定電流レギュレーション係数(「*Electrical Characteristics*」を参照)

$V_{CST(max)}$ CSピンの最大電流検出スレッショルド(「*Electrical Characteristics*」を参照)

$V_{CST(min)}$ CSピンの最小電流検出スレッショルド(「*Electrical Characteristics*」を参照)

$V_{VDD(off)}$ UVLOターンオフ電圧(「*Electrical Characteristics*」を参照)

$V_{VDD(on)}$ UVLOターンオン電圧(「*Electrical Characteristics*」を参照)

V_{DSPK} ハイ・ラインでのMOSFETのドレイン-ソース間ピーク電圧

V_F 電流が0に近いときの、2次側整流器の順方向電圧降下

V_{FA} 補助整流器の順方向電圧降下

V_{LK} リーク・インダクタンス・エネルギーのリセット電圧の推定値

$V_{O\Delta}$ CVモードの負荷ステップ過渡時に許容される出力電圧降下

V_{OCBC} V_{OCV}に追加される目標ケーブル補償電圧(シャント・レギュレータに適用される外部の調整回路から供給)。

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デバイス・サポート (continued)

使用しない場合は0Vに設定

V_{OCC} 定電流レギュレーション時の、コンバータの最低出力電圧目標

V_{OCV} コンバータのレギュレーション出力電圧

V_{OV} 許容される最大のピーク出力電圧

V_{OVP} VS入力での過電圧検出レベル(「*Electrical Characteristics*」を参照)

V_{REVA} 補助整流器でのピーク逆電圧

V_{REVS} 2次側整流器でのピーク逆電圧

V_{RIPPLE} 全負荷時の出力ピーク・ツー・ピーク・リップル電圧

11.1.2.11 AC電圧項(V_{RMS}単位)

$V_{IN(max)}$ コンバータの最大入力電圧

$V_{IN(min)}$ コンバータの最小入力電圧

$V_{IN(run)}$ コンバータのスタートアップ(実行)入力電圧

11.1.2.12 効率項

η 最大出力電力での、コンバータの総効率

η_{SB} 無負荷時のコンバータの推定効率、スタートアップ抵抗およびバイアス損失を除く。5V USB充電器アプリケーションの場合、適切な初期推定値は60%～65%

η_{XFMR} 変圧器の1次側から2次側への電力伝達効率

11.2 ドキュメントのサポート

11.2.1 関連資料

関連資料については、以下を参照してください。

- *『12W、入力電圧範囲が非常に広い電源』*
- *『36W、ユニバーサル入力、90%超の効率、デュアル出力のサーバーPSU用補助電源のリファレンス・デザイン』*
- *『高精度の電圧、電流、電力制限付き60W、24V、高効率の産業用電源』*
- *『スナバでの標準のリカバリ・ダイオードまたは超高速ダイオードの選択』*
- *『低消費電力AC/DCコンバータの制御における課題』*
- *『90～265V AC入力、統合型30Wセンサレス BLDCモータ・ドライブ後付けのリファレンス・デザイン』*
- *『UCC28740EVM-525 10W定電圧、定電流充電アダプタ・モジュールの使用』*
- *『高精度の電流および電力制限付き100W、24V、高効率、高PFの産業用電源』*

11.3 ドキュメントの更新通知を受け取る方法

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11.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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設計サポート ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることが

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コミュニティ・リソース (continued)

できます。技術サポート用の連絡先情報も参照できます。

11.5 商標

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11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC28740D	Active	Production	SOIC (D) | 7	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	U28740
UCC28740DR	Active	Production	SOIC (D) | 7	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	U28740

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF UCC28740 :

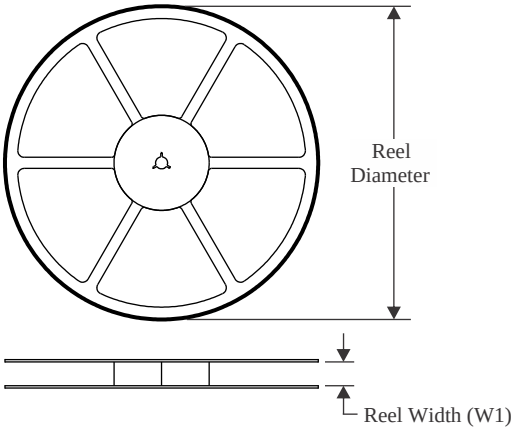
- Automotive : UCC28740-Q1

NOTE: Qualified Version Definitions:

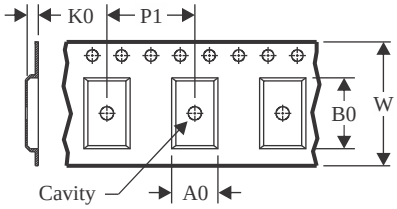
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

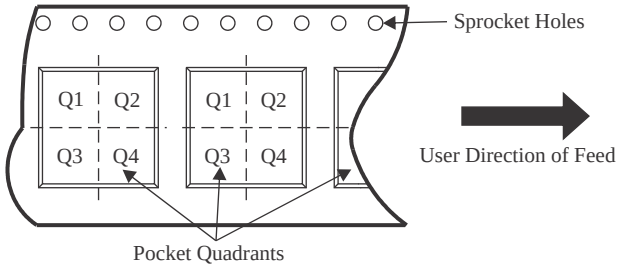


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

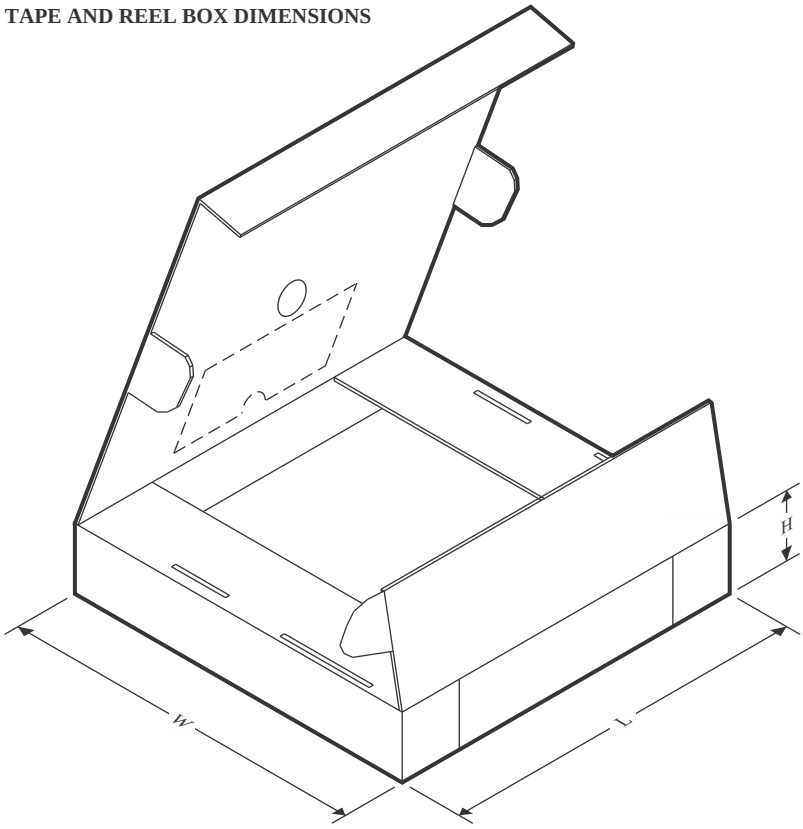
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC28740DR	SOIC	D	7	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

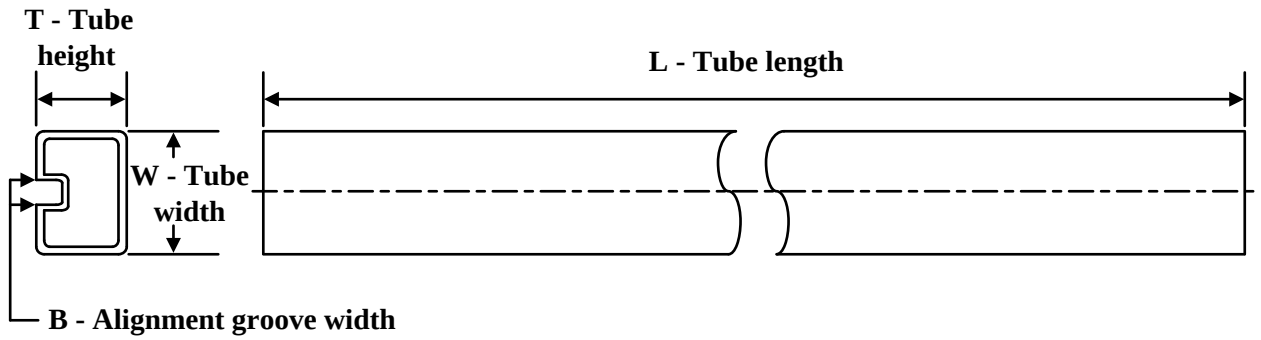
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

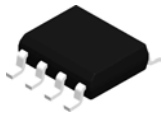
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC28740DR	SOIC	D	7	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UCC28740D	D	SOIC	7	75	506.6	8	3940	4.32

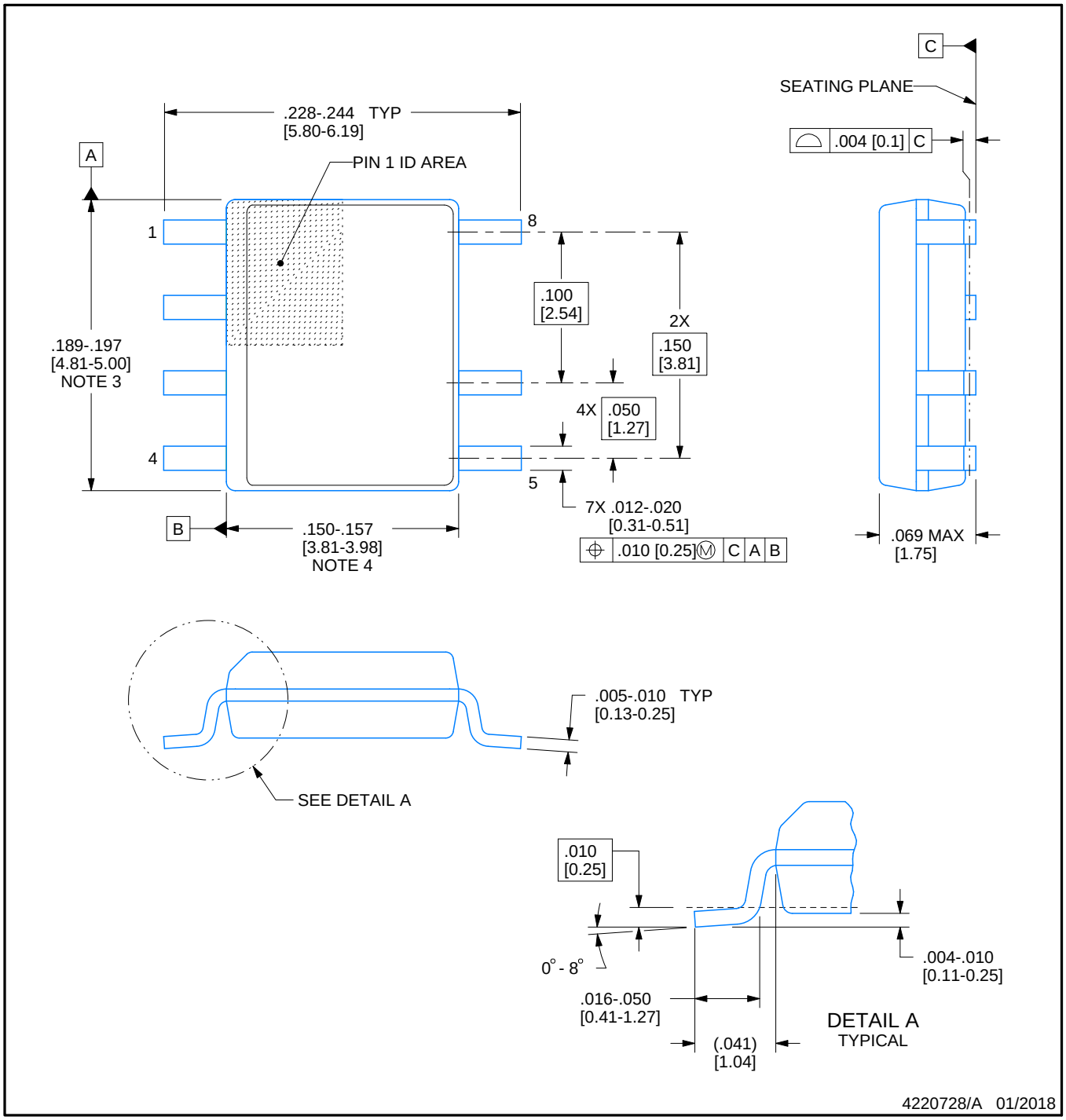


PACKAGE OUTLINE

D0007A

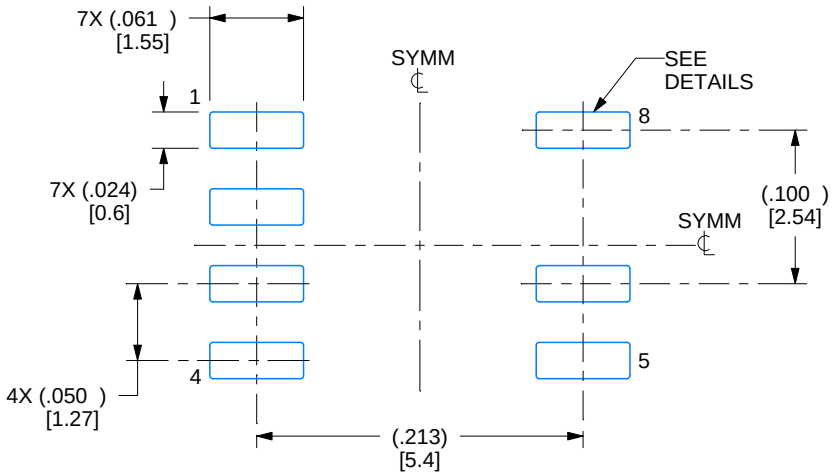
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

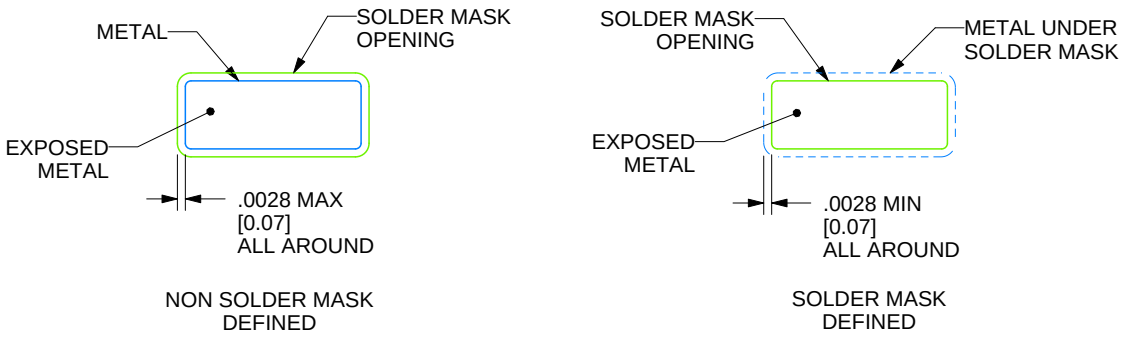


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4220728/A 01/2018

NOTES: (continued)

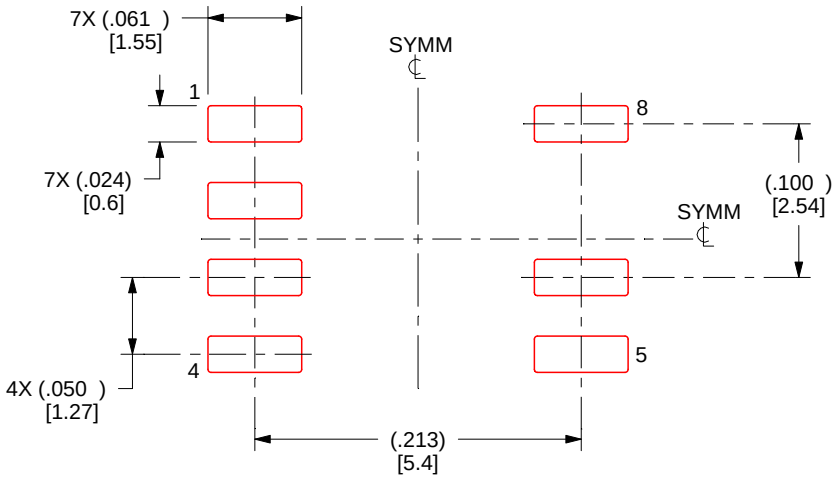
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0007A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4220728/A 01/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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