TEXAS INSTRUMENTS
UCC28740-Q1
JAJSHT2C – AUGUST 2019 – REVISED DECEMBER 2020

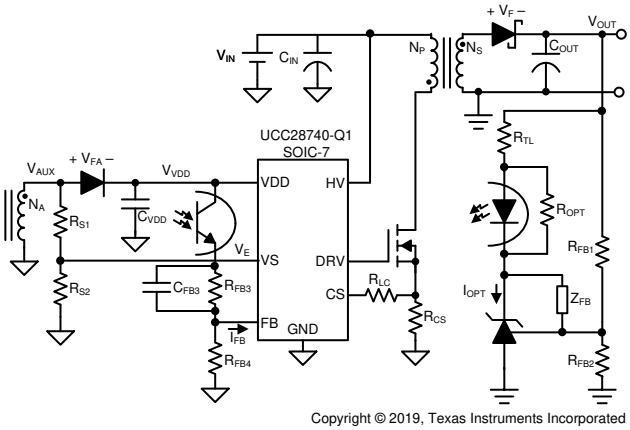
UCC28740-Q1 HV スタートアップおよびフォトカプラ帰還機能を内蔵した超低スタンバイ電力の車載用フライバック・コントローラ

1 特長

- 車載アプリケーション向けに認定済み
- 以下の結果で AEC-Q100 認定済み:
  - デバイス温度グレード 1:-40℃～+125℃
  - デバイス HBM 分類レベル 2:±2kV
  - デバイス CDM 分類レベル C4B:±750V
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 無負荷時の電力 10mW 未満
- ラインおよび負荷範囲全体にわたる ±1% の電圧レギュレーションおよび ±5% の電流レギュレーション
- 700V のスタートアップ・スイッチ
- 100kHz の最大スイッチング周波数により電力密度の高い充電器を設計可能
- 共振リング・バレー・スイッチング動作により、最高の全体効率を実現
- EMI 準拠を容易にする周波数ディザリング
- クランプされた MOSFET 用ゲート駆動出力
- 過電圧、低ライン、過電流からの保護機能
- WEBENCH® Power Designer により、UCC28740-Q1 を使用するカスタム設計を作成

2 アプリケーション

- HV スタートアップおよびフォトカプラ帰還機能を内蔵した超低スタンバイ電力のフライバック
- トラクション・インバータの HV から LV へのバックアップ電源
- HVAC コンプレッサ HV 絶縁電源
- PTC ヒーター HV 絶縁電源



アプリケーション概略図

3 概要

UCC28740-Q1 絶縁型フライバック電源コントローラは、フォトカプラを使用して出力を制御し、大きな負荷ステップに対して高速過渡応答を実現します。

内部の 700V スタートアップ・スイッチ、動的制御される動作状態、および適切に調整された変調プロファイルにより、スタートアップ時間や出力過渡応答を犠牲にすることなく、非常に低いスタンバイ時消費電力を実現します。

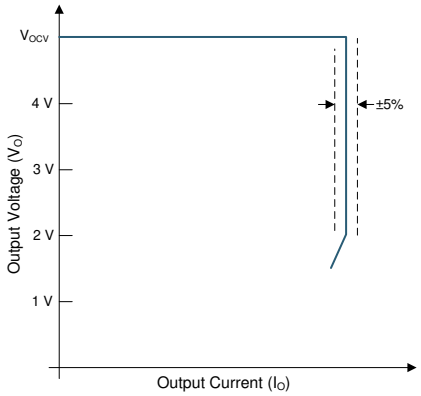
UCC28740-Q1 の制御アルゴリズムにより、適用される規格を満たすか、または上回る動作効率を実現できます。駆動出力は、MOSFET 電力スイッチに接続されます。バレー・スイッチングによる不連続導通モード (DCM) 動作でスイッチング損失が低減されます。スイッチング周波数の変調 (FM) および 1 次電流のピーク振幅の変調 (AM) により、負荷およびライン範囲の全体にわたって高い変換効率を保持します。

コントローラの最大スイッチング周波数は 100kHz で、変圧器内でピーク 1 次側電流の制御が常に維持されます。1 次および 2 次部品のストレスを抑制する保護機能も備えています。最小スイッチング周波数は 170Hz で、無負荷時の電力が 10mW 未満に抑えられます。

製品情報 (1)

部品番号	パッケージ	本体サイズ (公称)
UCC28740-Q1	SOIC (7)	4.90mm x 3.91mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



代表的な V-I 図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (May 2020) to Revision C (December 2020) — **Page**

- 機能安全の情報を追加 1

Changes from Revision A (November 2019) to Revision B (May 2020) — **Page**

- Added to include start-up current IHV at 30V VHV. 5

Changes from Revision * (August 2019) to Revision A (November 2019) — **Page**

- マーケティング・ステータスを「事前情報」から「量産データ」に変更 1

5 Pin Configuration and Functions

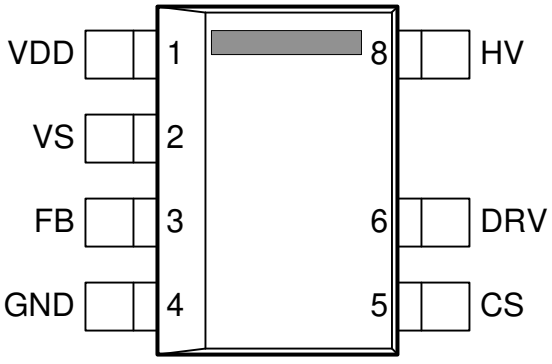


図 5-1. D Package 7-Pin SOIC Top View

5.1 Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CS	5	I	The current-sense (CS) input connects to a ground-referenced current-sense resistor in series with the power switch. The resulting voltage monitors and controls the peak primary current. A series resistor is added to this pin to compensate for peak switch-current levels as the AC-mains input varies.
DRV	6	O	Drive (DRV) is an output that drives the gate of an external high-voltage MOSFET switching transistor.
FB	3	I	The feedback (FB) input receives a current signal from the optocoupler output transistor. An internal current mirror divides the feedback current by 2.5 and applies it to an internal pullup resistor to generate a control voltage, V_{CL}. The voltage at this resistor directly drives the control law function, which determines the switching frequency and the peak amplitude of the switching current .
GND	4	—	The ground (GND) pin is both the reference pin for the controller, and the low-side return for the drive output. Special care must be taken to return all AC-decoupling capacitors as close as possible to this pin and avoid any common trace length with analog signal-return paths.
HV	8	I	The high-voltage (HV) pin may connect directly, or through a series resistor, to the rectified bulk voltage and provides a charge to the VDD capacitor for the startup of the power supply.
VDD	1	I	VDD is the bias-supply input pin to the controller. A carefully placed bypass capacitor to GND is required on this pin.
VS	2	I	Voltage sense (VS) is an input used to provide demagnetization timing feedback to the controller to limit frequency, to control constant-current operation, and to provide output-overvoltage detection. VS is also used for AC-mains input-voltage detection for peak primary-current compensation. This pin connects to a voltage divider between an auxiliary winding and GND. The value of the upper resistor of this divider programs the AC-mains run and stop thresholds, and factors into line compensation at the CS pin.

6 Specifications

6.1 Absolute Maximum Ratings

See (1) and (2).

		MIN	MAX	UNIT
V_{HV}	Start-up pin voltage, HV		700	V
V_{VDD}	Bias supply voltage, VDD		38	V
I_{DRV}	Continuous gate-current sink		50	mA
I_{DRV}	Continuous gate-current source		Self-limiting	mA
I_{FB}	Peak current, VS		1	mA
I_{VS}	Peak current, FB		−1.2	mA
V_{DRV}	Gate-drive voltage at DRV	–0.5	Self-limiting	V
	Voltage, CS	–0.5	5	V
	Voltage, FB	–0.5	7	V
	Voltage, VS	–0.75	7	V
T_J	Operating junction temperature	–55	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal. These ratings apply over the operating ambient temperature ranges unless otherwise noted.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)(1)	±2000	V
		Charged-device model (CDM), per Charged-device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{VDD}	Bias-supply operating voltage	9	35	V
C_{VDD}	VDD bypass capacitor	0.047		µF
I_{FB}	Feedback current, continuous		50	µA
I_{VS}	VS pin current, out of pin		1	mA
T_J	Operating junction temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC[1]		UCC28740-Q1 D (SOIC) 7 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	141.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	73.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	89	°C/W
ψ_{JT}	Junction-to-top characterization parameter	23.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	88.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over operating free-air temperature range, V_{VDD} = 25 V, HV = open, V_{FB} = 0 V, V_{VS} = 4 V, T_A = –40°C to +125°C, T_J = T_A (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HIGH-VOLTAGE START UP						
I_{HV}	Start-up current out of VDD	V_{HV} = 100 V, V_{VDD} = 0 V, start state	100	250	500	µA
		V_{HV} = 30 V, V_{VDD} = $V_{VDD(on)}$ – 0.5 V, start state	130		410	
$I_{HVLKG25}$	Leakage current at HV	V_{HV} = 400 V, run state, T_J = 25°C		0.01	0.5	µA
BIAS SUPPLY INPUT						
I_{RUN}	Supply current, run	I_{DRV} = 0, run state		2	2.65	mA
I_{WAIT}	Supply current, wait	I_{DRV} = 0, wait state		95	125	µA
I_{START}	Supply current, start	I_{DRV} = 0, V_{VDD} = 18 V, start state, I_{HV} = 0		18	30	µA
I_{FAULT}	Supply current, fault	I_{DRV} = 0, fault state		95	130	µA
UNDERVOLTAGE LOCKOUT						
$V_{VDD(on)}$	VDD turnon threshold	V_{VDD} low to high	19	21	23	V
$V_{VDD(off)}$	VDD turnoff threshold	V_{VDD} high to low	7.35	7.75	8.15	V
VS INPUT						
V_{VSNC}	Negative clamp level	I_{VSLS} = –300 µA, volts below ground	190	250	325	mV
I_{VSB}	Input bias current	V_{VS} = 4 V	–0.25	0	0.25	µA
FB INPUT						
I_{FBMAX}	Full-range input current	f_{SW} = $f_{SW(min)}$	16	23	30	µA
V_{FBMAX}	Input voltage at full range	I_{FB} = 25 µA, T_J = 25°C	0.75	0.88	1	V
R_{FB}	FB-input resistance, linearized	ΔI_{FB} = 20 µA, centered at I_{FB} = 15 µA, T_J = 25°C	10	14	18	kΩ
CS INPUT						
$V_{CST(max)}$	Maximum CS threshold voltage	I_{FB} = 0 µA[1]	738	773	810	mV
$V_{CST(min)}$	Minimum CS threshold voltage	I_{FB} = 35 µA[1]	170	194	215	mV
K_{AM}	AM-control ratio	$V_{CST(max)}$ / $V_{CST(min)}$	3.6	4	4.45	V/V
V_{CCR}	Constant-current regulation factor		318	330	343	mV
K_{LC}	Line-compensation current ratio	I_{VSLS} = –300 µA, I_{VSLS} / current out of CS pin	24	25	28.6	A/A
t_{CSLEB}	Leading-edge blanking time	DRV output duration, V_{CS} = 1 V	180	230	280	ns
DRIVERS						
I_{DRS}	DRV source current	V_{DRV} = 8 V, V_{VDD} = 9 V	20	25		mA
R_{DRVLS}	DRV low-side drive resistance	I_{DRV} = 10 mA		6	12	Ω

over operating free-air temperature range, V_{VDD} = 25 V, HV = open, V_{FB} = 0 V, V_{VS} = 4 V, T_A = –40°C to +125°C, T_J = T_A (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DRCL}	DRV clamp voltage	V_{VDD} = 35 V		14	16	V
R_{DRVSS}	DRV pulldown in start-state		150	190	230	kΩ
PROTECTION						
V_{OVP}	Overvoltage threshold	At VS input, T_J = 25°C(2)	4.52	4.6	4.74	V
V_{OCP}	Overcurrent threshold	At CS input	1.4	1.5	1.6	V
$I_{VSL(run)}$	VS line-sense run current	Current out of VS pin increasing	190	225	275	µA
$I_{VSL(stop)}$	VS line-sense stop current	Current out of VS pin decreasing	70	80	100	µA
K_{VSL}	VS line sense ratio	$I_{VSL(run)}$ / $I_{VSL(stop)}$	2.45	2.8	3.05	A/A
$T_{J(stop)}$	Thermal-shutdown temperature	Internal junction temperature		165		°C

(1) This device automatically varies the control frequency and current sense thresholds to improve EMI performance. These threshold voltages and frequency limits represent average levels.
(2) The overvoltage threshold level at VS decreases with increasing temperature by 0.8 mV/°C. This compensation is included to reduce the power-supply output overvoltage detection variance over temperature.

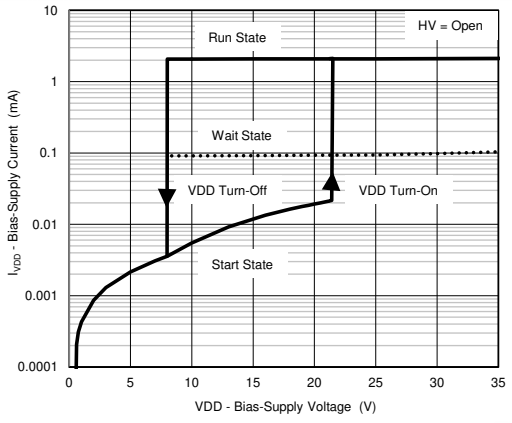
6.6 Switching Characteristics

over operating free-air temperature range, V_{VDD} = 25 V, HV = open, V_{FB} = 0 V, V_{VS} = 4 V, T_A = –40°C to +125°C, T_J = T_A (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{SW(max)}$	Maximum switching frequency	I_{FB} = 0 µA(1)	91	100	108	kHz
$f_{SW(min)}$	Minimum switching frequency	I_{FB} = 35 µA(1)	140	170	210	Hz
t_{ZTO}	Zero-crossing timeout delay		1.8	2.1	2.55	µs

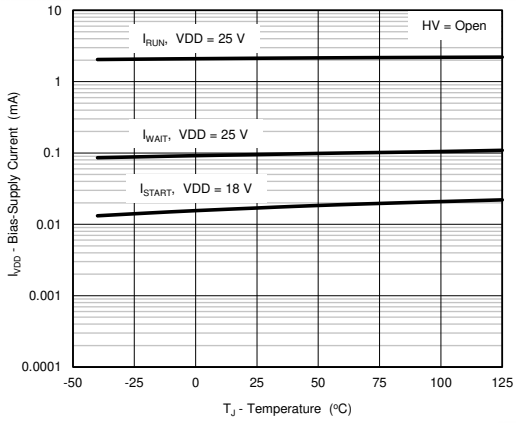
6.7 Typical Characteristics

V_{VDD} = 25 V, T_J = 25°C, unless otherwise noted.



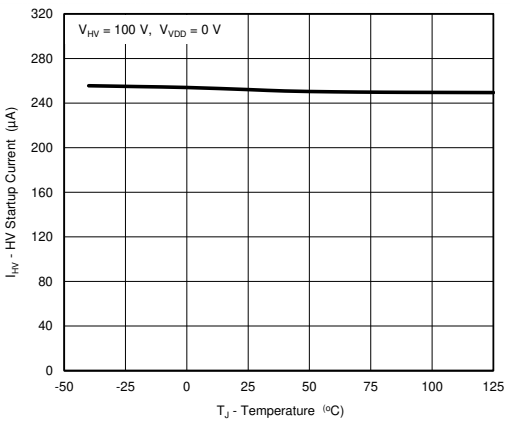
HV = Open

図 6-1. Bias-Supply Current vs. Bias-Supply Voltage



HV = Open

図 6-2. Bias-Supply Current vs. Temperature



V_{HV} = 100 V, V_{VDD} = 0 V

図 6-3. HV Startup Current vs. Temperature

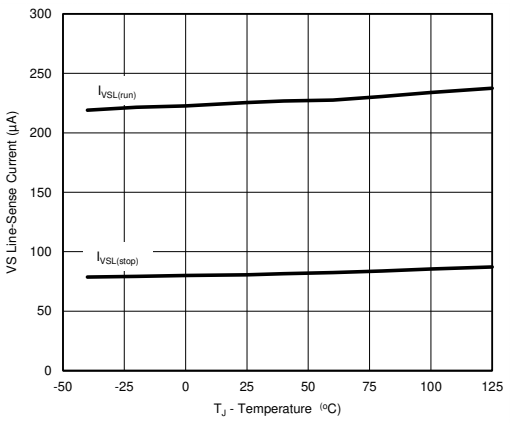


図 6-4. VS Line-Sense Currents vs. Temperature

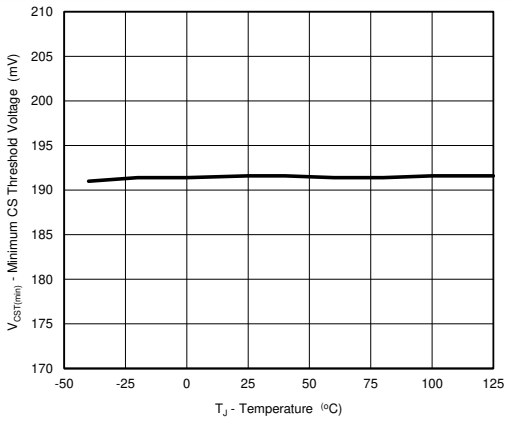


図 6-5. Minimum CS Threshold vs. Temperature

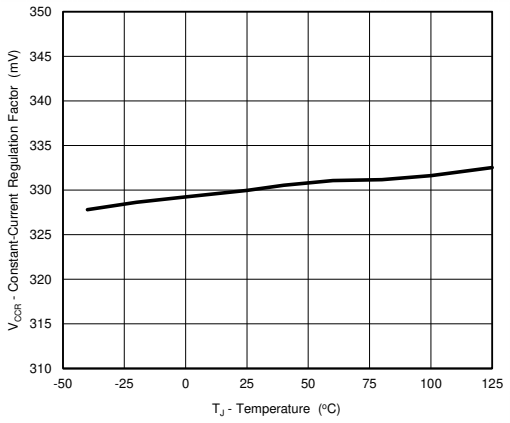


図 6-6. Constant-Current Regulation Factor vs. Temperature

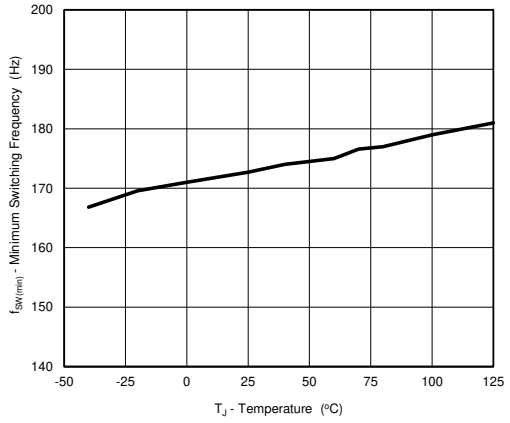
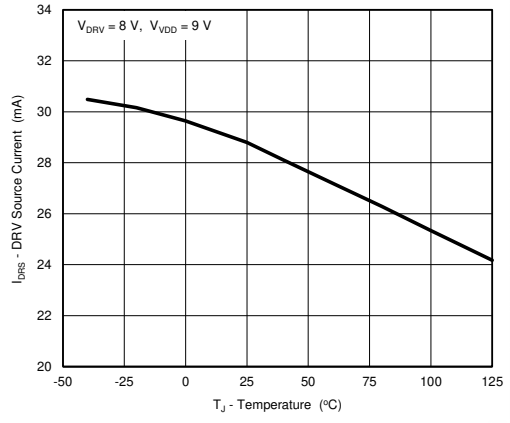


図 6-7. Minimum Switching Frequency vs. Temperature



V_{DRV} = 8 V, V_{VDD} = 9 V

図 6-8. DRV Source Current vs. Temperature

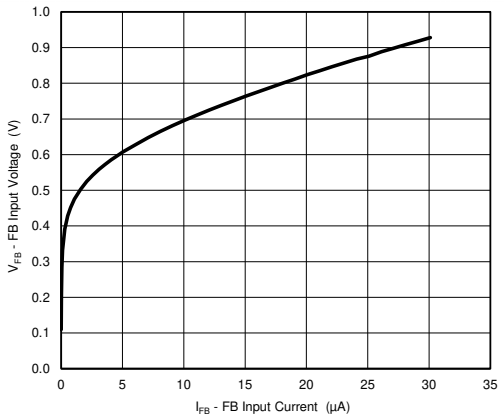


図 6-9. FB Input Voltage vs. FB Input Current

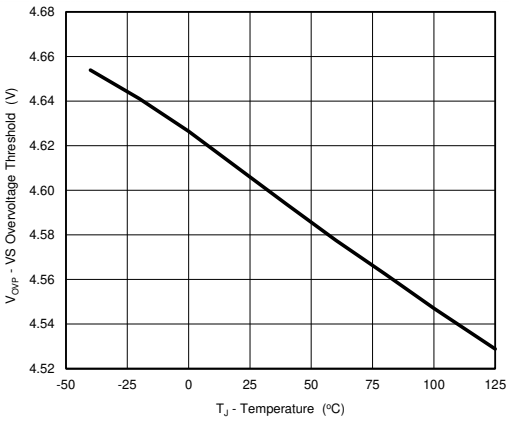


図 6-10. VS Overvoltage Threshold vs. Temperature

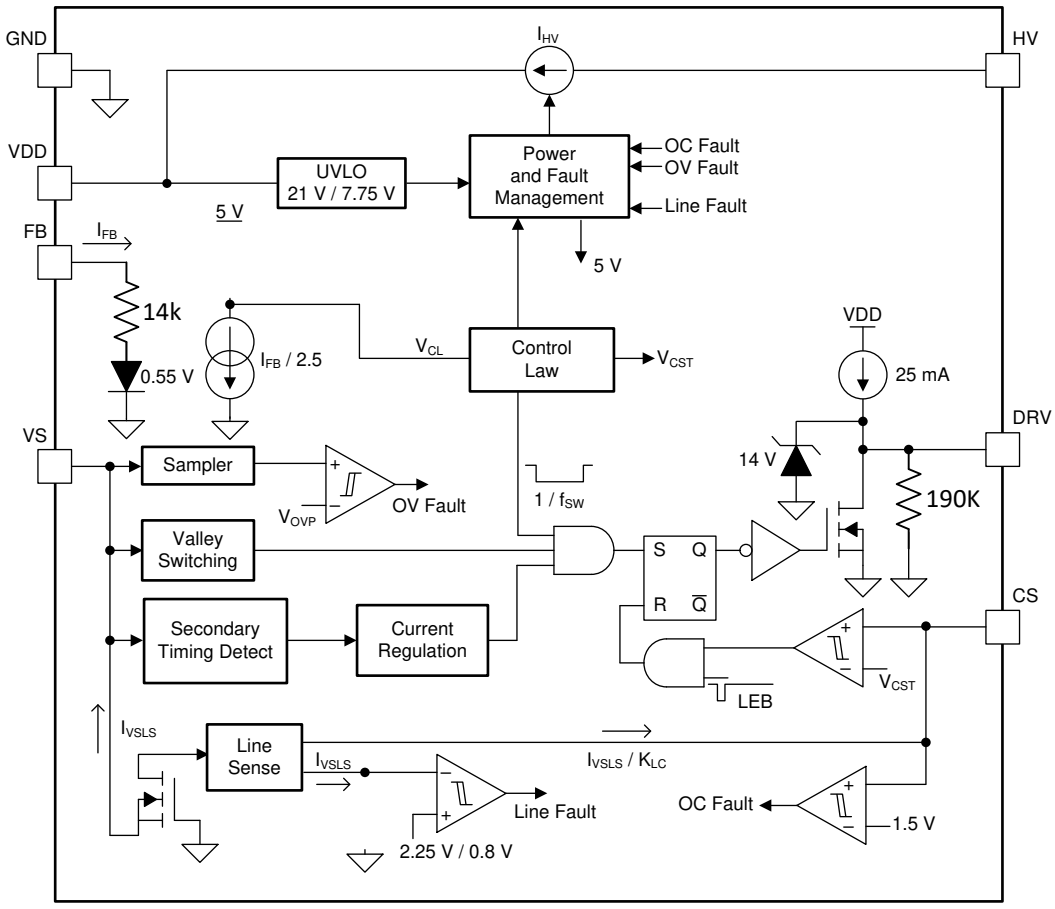
7 Detailed Description

7.1 Overview

The UCC28740-Q1 is a flyback power-supply controller which provides high-performance voltage regulation using an optically coupled feedback signal from a secondary-side voltage regulator. The device provides accurate constant-current regulation using primary-side feedback. The controller operates in discontinuous-conduction mode (DCM) with valley-switching to minimize switching losses. The control law scheme combines frequency with primary peak-current amplitude modulation to provide high conversion efficiency across the load range. The control law provides a wide dynamic operating range of output power which allows the power-supply designer to easily achieve less than 30-mW standby power dissipation using a standard shunt-regulator and optocoupler. For a target of less than 10-mW standby power, careful loss-management design with a low-power regulator and high-CTR optocoupler is required.

During low-power operating conditions, the power-management features of the controller reduce the device-operating current at switching frequencies below 32 kHz. At and above this frequency, the UCC28740-Q1 includes features in the modulator to reduce the EMI peak energy of the fundamental switching frequency and harmonics. A complete low-cost and low component-count charger-solution is realized using a straight-forward design process.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Detailed Pin Description

VDD (Device Bias Voltage Supply) The VDD pin connects to a bypass capacitor-to-ground. The turnon UVLO threshold is 21 V and turnoff UVLO threshold is 7.75 V with an available operating range up to 35 V on VDD. The typical USB-charging specification requires the output current to operate in constant-current mode from 5 V down to at least 2 V which is achieved easily with a nominal V_{VDD} of approximately 25 V. The additional VDD headroom up to 35 V allows for V_{VDD} to rise due to the leakage energy delivered to the VDD capacitor during high-load conditions.

GND (Ground) UCC28740 has a single ground reference external to the device for the gate-drive current and analog signal reference. Place the VDD-bypass capacitor close to GND and VDD with short traces to minimize noise on the VS, FB, and CS signal pins.

HV (High-Voltage Startup) The HV pin connects directly to the bulk capacitor to provide a startup current to the VDD capacitor. The typical startup current is approximately 250 µA which provides fast charging of the VDD capacitor. The internal HV startup device is active until V_{VDD} exceeds the turnon UVLO threshold of 21 V at which time the HV startup device turns off. In the off state the HV leakage current is very low to minimize standby losses of the controller. When V_{VDD} falls below the 7.75 V UVLO turnoff threshold the HV startup device turns on.

VS (Voltage Sense) The VS pin connects to a resistor-divider from the auxiliary winding to ground. The auxiliary voltage waveform is sampled at the end of the transformer secondary-current demagnetization time to provide accurate control of the output current when in constant-current mode. The waveform on the VS pin determines the timing information to achieve valley-switching, and the timing to control the duty-cycle of the transformer secondary current. Avoid placing a filter capacitor on this input which interferes with accurate sensing of this waveform.
During the MOSFET on-time, this pin also senses VS current generated through R_{S1} by the reflected bulk-capacitor voltage to provide for AC-input run and stop thresholds, and to compensate the current-sense threshold across the AC-input range. For the AC-input run/stop function, the run threshold on VS is 225 µA and the stop threshold is 80 µA.
At the end of off-time demagnetization, the reflected output voltage is sampled at this pin to provide output overvoltage protection. The values for the auxiliary voltage-divider upper-resistor, R_{S1}, and lower-resistor, R_{S2}, are determined by 式 1 and 式 2.

$$R_{S1} = \frac{V_{IN(run)} \times \sqrt{2}}{N_{PA} \times I_{VSL(run)}} \quad (1)$$

where

- N_{PA} is the transformer primary-to-auxiliary turns-ratio,
- $V_{IN(run)}$ is the AC RMS voltage to enable turnon of the controller (run), (in case of DC input, leave out the $\sqrt{2}$ term in the equation),
- $I_{VSL(run)}$ is the run-threshold for the current pulled out of the VS pin during the switch on-time (see *セクション 6.5*).

$$R_{S2} = \frac{R_{S1} \times V_{OVP}}{N_{AS} \times (V_{OV} - V_F) - V_{OVP}} \quad (2)$$

where

- V_{OV} is the maximum allowable peak voltage at the converter output,
- V_F is the output-rectifier forward drop at near-zero current,
- N_{AS} is the transformer auxiliary-to-secondary turns-ratio,
- R_{S1} is the VS divider high-side resistance,
- V_{OVP} is the overvoltage detection threshold at the VS input (see *セクション 6.5*).

FB (Feedback) The FB pin connects to the emitter of an analog-optocoupler output transistor which usually has the collector connected to VDD. The current supplied to FB by the optocoupler is reduced internally by a factor of 2.5 and the resulting current is applied to an internal 480-kΩ resistor to generate the control law voltage (V_{CL}). This V_{CL} directly determines the converter switching frequency and peak primary current required for regulation per the control-law for any given line and load condition.

DRV (Gate Drive) The DRV pin connects to the MOSFET gate pin, usually through a series resistor. The gate driver provides a gate-drive signal limited to 14 V. The turnon characteristic of the driver is a 25-mA current source which limits the turnon dv/dt of the MOSFET drain and reduces the leading-edge current spike while still providing a gate-drive current to overcome the Miller plateau. The gate-drive turnoff current is determined by the R_{DSON} of the low-side driver along with any external gate-drive resistance. Adding external gate resistance reduces the MOSFET drain turn-off dv/dt, if necessary.

CS (Current Sense) The current-sense pin connects through a series resistor (R_{LC}) to the current-sense resistor (R_{CS}). The maximum current-sense threshold ($V_{CST(max)}$) is 0.773 V for $I_{PP(max)}$, and the minimum current-sense threshold ($V_{CST(min)}$) is 0.194 V for $I_{PP(min)}$. R_{LC} provides the feed-forward line compensation to eliminate changes in I_{PP} with input voltage due to the propagation delay of the internal comparator and MOSFET turnoff time. An internal leading-edge blanking time of 235 ns eliminates sensitivity to the MOSFET turnon current spike. Placing a bypass capacitor on the CS pin is unnecessary. The target output current in constant-current (CC) regulation determines the value of R_{CS}. The values of R_{CS} and R_{LC} are calculated using 式 3 and 式 4. The term V_{CCR} is the product of the demagnetization constant, 0.425, and $V_{CST(max)}$. $V_{CCR}$is held to a tighter accuracy than either of its constituent terms. The term η_{XFMR} accounts for the energy stored in the transformer but not delivered to the secondary. This term includes transformer resistance and core loss, bias power, and primary-to-secondary leakage ratio.

Example:

With a transformer core and winding loss of 5%, primary-to-secondary leakage inductance of 3.5%, and bias power to output power ratio of 0.5%, the η_{XFMR} value at full power is approximately: 1 - 0.05 - 0.035 - 0.005 = 0.91.

$$R_{CS} = \frac{V_{CCR} \times N_{PS}}{2I_{OCC}} \times \sqrt{\eta_{XFMR}} \quad (3)$$

where

- V_{CCR} is a constant-current regulation factor (see *セクション 6.5*),
- N_{PS} is the transformer primary-to-secondary turns-ratio (a ratio of 13 to 15 is typical for 5-V output),
- I_{OCC} is the target output current in constant-current regulation,
- η_{XFMR} is the transformer efficiency at full power.

$$R_{LC} = \frac{K_{LC} \times R_{S1} \times R_{CS} \times t_D \times N_{PA}}{L_P} \quad (4)$$

where

- R_{S1} is the VS pin high-side resistor value,
- R_{CS} is the current-sense resistor value,
- t_D is the total current-sense delay consisting of MOSFET turnoff delay, plus approximately 50 ns internal delay,
- N_{PA} is the transformer primary-to-auxiliary turns-ratio,
- L_P is the transformer primary inductance,
- K_{LC} is a current-scaling constant for line compensation (see *セクション 6.5*).

7.3.2 Valley-Switching and Valley-Skipping

The UCC28740-Q1 uses valley-switching to reduce switching losses in the MOSFET, to reduce induced-EMI, and to minimize the turnon current spike at the current-sense resistor. The controller operates in valley-switching in all load conditions unless the V_{DS} ringing diminishes to the point where valleys are no longer detectable.

As shown in 図 7-1, the UCC28740-Q1 operates in a valley-skipping mode (also known as valley-hopping) in most load conditions to maintain an accurate voltage or current regulation point and still switch on the lowest available V_{DS} voltage.

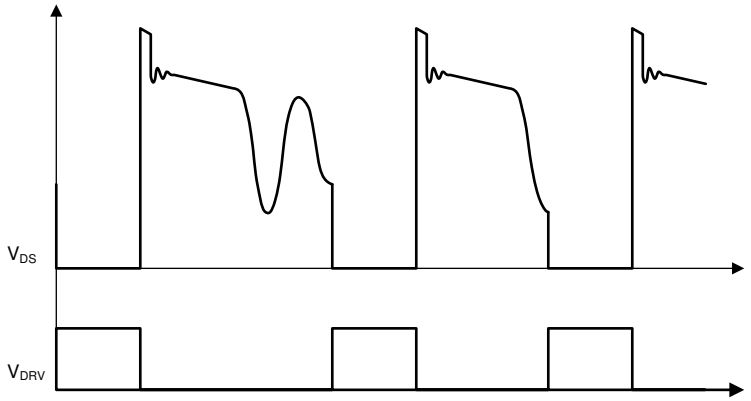


図 7-1. Valley-Skipping Mode

Valley-skipping modulates each switching cycle into discrete period durations. During FM operation, the switching cycles are periods when energy is delivered to the output in fixed packets, where the power-per-cycle varies discretely with the switching period. During operating conditions when the switching period is relatively short, such as at high-load and low-line, the average power delivered per cycle varies significantly based on the number of valleys skipped between cycles. As a consequence, valley-skipping adds additional ripple voltage to the output with a frequency and amplitude dependent upon the loop-response of the shunt-regulator. For a load with an average power level between that of cycles with fewer valleys skipped and cycles with more valleys skipped, the voltage-control loop modulates the FB current according to the loop-bandwidth and toggles between longer and shorter switching periods to match the required average output power.

7.3.3 Startup Operation

An internal high-voltage startup switch, connected to the bulk-capacitor voltage (V_{BULK}) through the HV pin, charges the VDD capacitor. This startup switch functions similarly to a current source providing typically 250 µA to charge the VDD capacitor. When V_{VDD} reaches the 21-V UVLO turnon threshold the controller is enabled, the converter starts switching, and the startup switch turns off.

Often at initial turnon, the output capacitor is in a fully discharged state. The first three switching-cycle current peaks are limited to $I_{PP(min)}$ to monitor for any initial input or output faults with limited power delivery. After these three cycles, if the sampled voltage at VS is less than 1.33 V, the controller operates in a special startup mode. In this mode, the primary current peak amplitude of each switching cycle is limited to approximately 0.63 × $I_{PP(max)}$ and D_{MAGCC} increases from 0.425 to 0.735. These modifications to $I_{PP(max)}$ and D_{MAGCC} during startup allows high-frequency charge-up of the output capacitor to avoid audible noise while the demagnetization voltage is low. Once the sampled VS voltage exceeds 1.38 V, D_{MAGCC} is restored to 0.425 and the primary current peak resumes as $I_{PP(max)}$. While the output capacitor charges, the converter operates in CC mode to maintain a constant output current until the output voltage enters regulation. Thereafter, the controller responds to the condition dictated by the control law. The time to reach output regulation consists of the time the VDD capacitor charges to 21 V plus the time the output capacitor charges.

7.3.4 Fault Protection

The UCC28740-Q1 provides extensive fault protection. The protection functions include:

- Output overvoltage

- Input undervoltage
- Internal overtemperature
- Primary overcurrent fault
- CS-pin fault
- VS-pin fault

A UVLO reset and restart sequence applies to all fault-protection events.

The output-overvoltage function is determined by the voltage feedback on the VS pin. If the voltage sample of VS exceeds 4.6 V, the device stops switching and the internal current consumption becomes I_{FAULT} which discharges the VDD capacitor to the UVLO-turnoff threshold. After that, the device returns to the start state and a startup sequence ensues.

The UCC28740-Q1 always operates with cycle-by-cycle primary peak current control. The normal operating voltage range of the CS pin is 0.773 V to 0.194 V. An additional protection, not filtered by leading-edge blanking, occurs if the CS pin voltage reaches 1.5 V, which results in a UVLO reset and restart sequence.

Current into the VS pin during the MOSFET on-time determines the line-input run and stop thresholds. While the VS pin clamps close to GND during the MOSFET on-time, the current through R_{S1} is monitored to determine a sample of V_{BULK}. A wide separation of the run and stop thresholds allows for clean startup and shutdown of the power supply with the line voltage. The run-current threshold is 225 µA and the stop-current threshold is 80 µA.

The internal overtemperature-protection threshold is 165°C. If the junction temperature reaches this threshold the device initiates a UVLO-reset cycle. If the temperature is still high at the end of the UVLO cycle, the protection cycle repeats.

Protection is included in the event of component failures on the VS pin. If complete loss of feedback information on the VS pin occurs, the controller stops switching and restarts.

7.4 Device Functional Modes

7.4.1 Secondary-Side Optically Coupled Constant-Voltage (CV) Regulation

図 7-2 shows a simplified flyback convertor with the main output-regulation blocks of the device shown, along with typical implementation of secondary-side-derived regulation. The power-train operation is the same as any DCM-flyback circuit. A feedback current is optically coupled to the controller from a shunt-regulator sensing the output voltage.

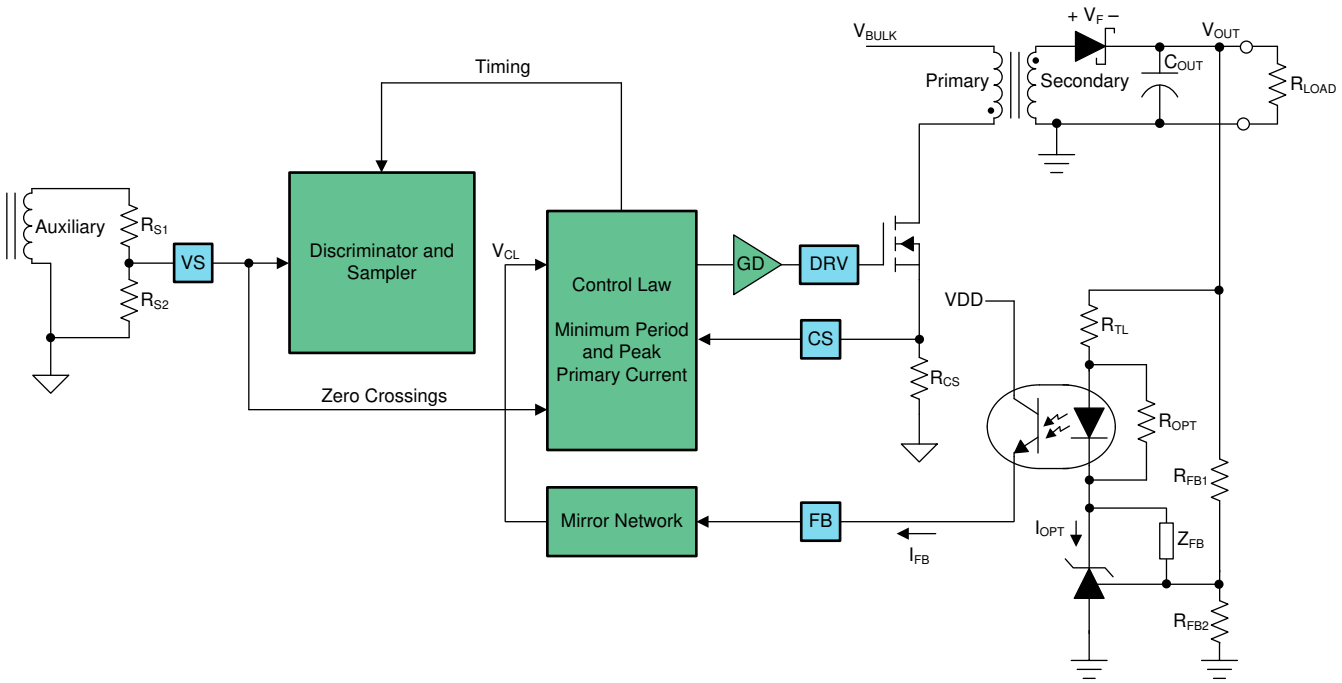


図 7-2. Simplified Flyback Convertor (With the Main Voltage Regulation Blocks)

In this configuration, a secondary-side shunt-regulator, such as the TL431, generates a current through the input photo-diode of an optocoupler. The photo-transistor delivers a proportional current that is dependent on the current-transfer ratio (CTR) of the optocoupler to the FB input of the UCC28740-Q1 controller. This FB current then converts into the V_{CL} by the input-mirror network, detailed in the device block diagram (see *セクション 7.2*). Output-voltage variations convert to FB-current variations. The FB-current variations modify the V_{CL} which dictates the appropriate I_{PP} and f_{SW} necessary to maintain CV regulation. At the same time, the VS input senses the auxiliary winding voltage during the transfer of transformer energy to the secondary output to monitor for an output overvoltage condition. When f_{SW} reaches the target maximum frequency, chosen between 32 kHz and 100 kHz, CC operation is entered and further increases in V_{CL} have no effect.

図 7-3 shows that as the secondary current decreases to zero, a clearly defined down slope reflects the decreasing rectifier V_F combined with stray resistance voltage-drop ($I_S R_S$). To achieve an accurate representation of the secondary output voltage on the auxiliary winding, the discriminator reliably blocks the leakage-inductance reset and ringing while continuously sampling the auxiliary voltage during the down slope after the ringing diminishes. The discriminator then captures the voltage signal at the moment that the secondary-winding current reaches zero. The internal overvoltage threshold on VS is 4.6 V. Temperature compensation of –0.8 mV/°C on the overvoltage threshold offsets the change in the output-rectifier forward voltage with temperature. The resistor divider is selected as outlined in the VS pin description (see *セクション 7.3.1*).

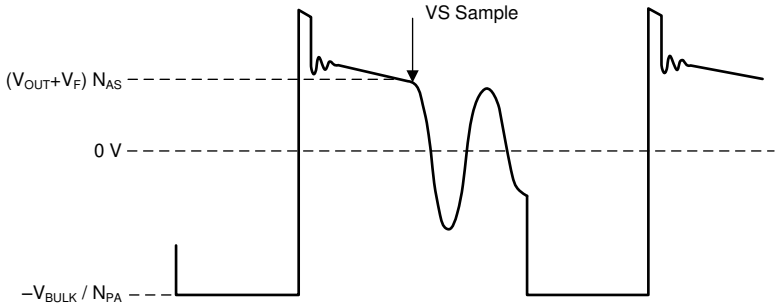


図 7-3. Auxiliary-Winding Voltage

The UCC28740-Q1 VS-signal sampler includes signal-discrimination methods to ensure an accurate sample of the output voltage from the auxiliary winding. Controlling some details of the auxiliary-winding signal to ensure reliable operation is necessary; specifically, the reset time of the leakage inductance and the duration of any subsequent leakage-inductance ringing. See 図 7-4 for a detailed illustration of waveform criteria to ensure a reliable sample on the VS pin.

The first detail to examine is the duration of the leakage-inductance reset pedestal, t_{LK_RESET}, in 図 7-4. Because t_{LK_RESET} mimics the waveform of the secondary-current decay, followed by a sharp downslope, t_{LK_RESET} is internally blanked for a duration which scales with the peak primary current. Keeping the leakage-reset time to less than 600 ns for $I_{PP(min)}$, and less than 2.2 µs for $I_{PP(max)}$ is important.

The second detail is the amplitude of ringing on the V_{AUX} waveform following t_{LK_RESET}. The peak-to-peak voltage variation at the VS pin must be less than 100 mVp-p for at least 200 ns before the end of the demagnetization time (t_{DM}). A concern with excessive ringing usually occurs during light or no-load conditions, when t_{DM} is at the minimum. The tolerable ripple on VS is scaled up to the auxiliary-winding voltage by R_{S1} and R_{S2}, and is equal to 100 mV × (R_{S1} + R_{S2}) / R_{S2} .

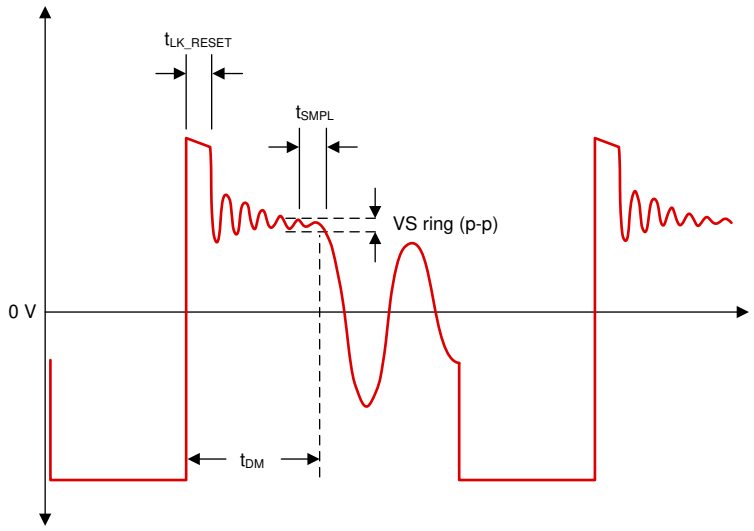


図 7-4. Auxiliary-Winding Waveform Details

During voltage regulation, the controller operates in frequency-modulation mode and amplitude-modulation mode, as shown in 図 7-5. The internal operating-frequency limits of the device are 100 kHz and $f_{SW(min)}$. The maximum operating frequency of the converter at full-load is generally chosen to be slightly lower than 100 kHz to allow for tolerances, or significantly lower due to switching-loss considerations. The maximum operating frequency and primary peak current chosen determine the transformer primary inductance of the converter. The shunt-regulator bias power, output preload resistor (if any), and low-power conversion efficiency determine the minimum-operating frequency of the converter. Voltage-loop stability compensation is applied at the shunt-regulator which drives the opto-coupled feedback signal. The tolerances chosen for the shunt-regulator reference and the sense resistors determines the regulation accuracy.

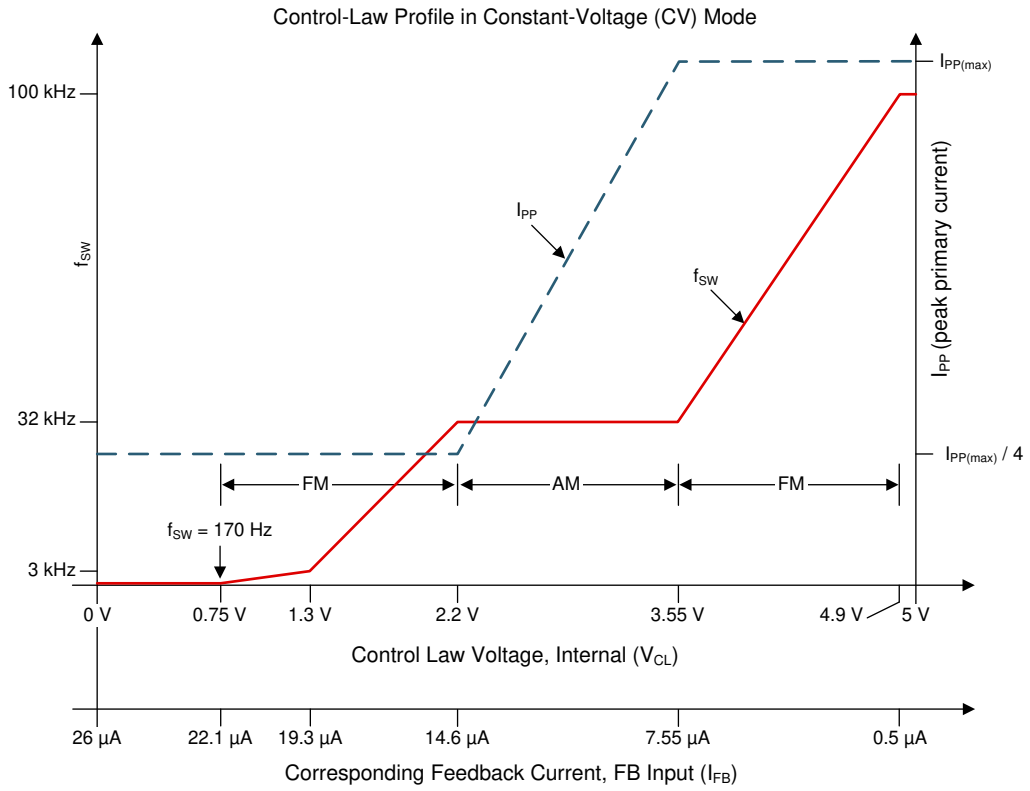


図 7-5. Frequency and Amplitude Modulation Modes (During CV Regulation)

The level of feedback current (I_{FB}) into the FB pin determines the internal V_{CL} which determines the operating point of the controller while in CV mode. When I_{FB} rises above 22 µA, no further decrease in f_{SW} occurs. When the output-load current increases to the point where maximum f_{SW} is reached, control transfers to CC mode. All current, voltage, frequency, breakpoints, and curve-segment linearity depicted in 図 7-5 are nominal. 図 7-5 indicates the general operation of the controller while in CV mode, although minor variations may occur from part to part. An internal frequency-dithering mechanism is enabled when I_{FB} is less than 14.6 µA to help reduce conducted EMI (including during CC-mode operation), and is disabled otherwise.

7.4.2 Primary-Side Constant-Current (CC) Regulation

When the load current of the converter increases to the predetermined constant-current limit, operation enters CC mode. In CC mode, output voltage regulation is lost and the shunt-regulator drives the current and voltage at FB to minimum. During CC mode, timing information at the VS pin and current information at the CS pin allow accurate regulation of the average current of the secondary winding. The CV-regulation control law dictates that as load increases approaches CC regulation the primary peak current will be at $I_{PP(max)}$. The primary peak current, turns-ratio, demagnetization time t_{DM}, and switching period t_{SW} determine the secondary average output current (see 図 7-6). Ignoring leakage-inductance effects, the average output current is given by 式 5. When the demagnetization duty-cycle reaches the CC-regulation reference, D_{MAGCC}, in the current-control block, the controller operates in frequency modulation (FM) mode to control the output current for any output voltage at or below the voltage-regulation target as long as the auxiliary winding keeps V_{VDD} above the UVLO turnoff threshold. As the output voltage falls, t_{DM} increases. The controller acts to increase t_{SW} to maintain the ratio of t_{DM} to switching period (t_{DM} / t_{SW}) at a maximum of 0.425 (D_{MAGCC}), thereby maintaining a constant average output current.

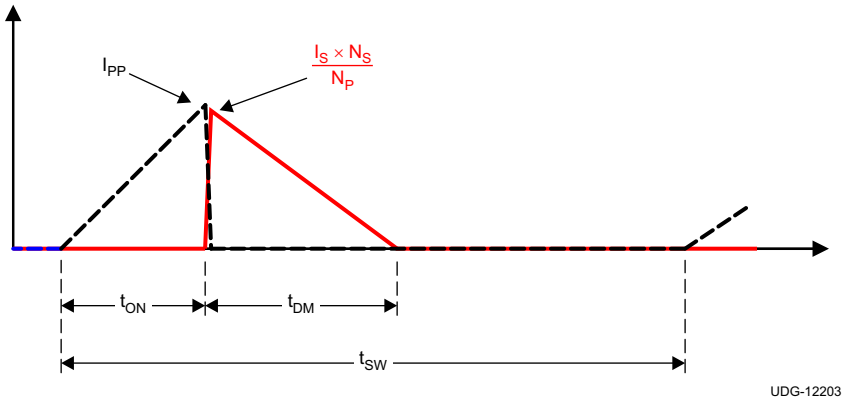


図 7-6. Transformer-Current Relationship

$$I_{OUT} = \frac{I_{PP}}{2} \times \frac{N_P}{N_S} \times \frac{t_{DM}}{t_{SW}} \quad (5)$$

Fast, accurate, opto-coupled CV control combined with line-compensated PSR CC control results in high-performance voltage and current regulation which minimizes voltage deviations due to heavy load and unload steps, as illustrated by the V-I curve in 図 7-7.

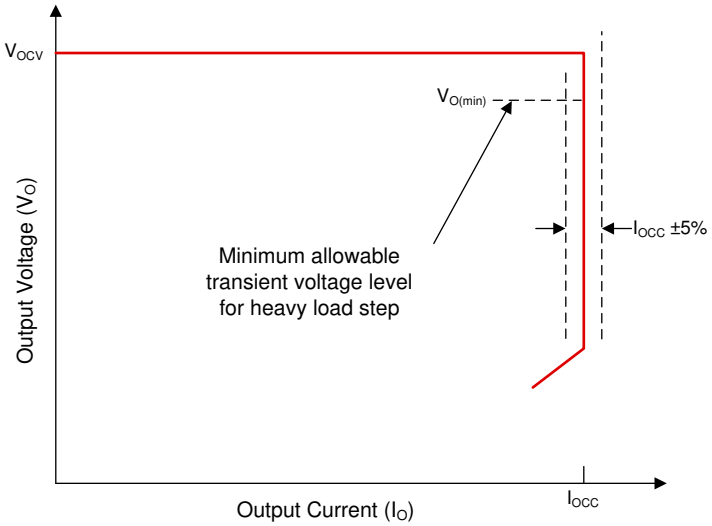


図 7-7. Typical Target Output V-I Characteristic

8 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The UCC28740-Q1 is a flyback controller that provides constant-voltage (CV) mode control and constant current (CC) mode control for precise output regulation. While in CV operating range, the controller uses an opto-coupler for tight voltage regulation and improved transient response to large load steps. Accurate regulation while in CC mode is provided by primary side control. The UCC28740-Q1 uses frequency modulation, peak primary current modulation, valley switching and valley hopping in its control algorithm in order to maximize efficiency over the entire operating range.

8.2 High Voltage Applications

The UCC28740-Q1 offers integrated 700-V start up through the HV pin. However for application where the input (V_{BULK}) is higher than 700-V the HV pin should be biased using a stacked capacitor bank (C_{IN1}, C_{IN2}) illustrated in 図 8-1.

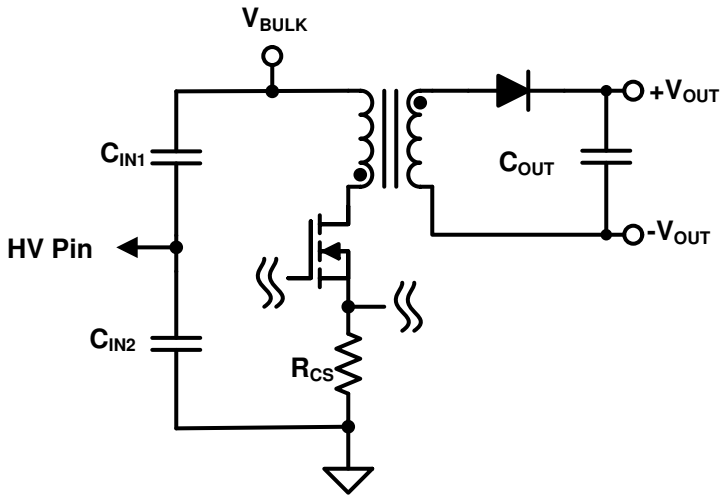


図 8-1. Implementation to Support > 700 V Inputs

8.3 Typical Application

The UCC28740-Q1 is well suited for use in isolated off-line systems requiring high efficiency and fault protection features such as USB compliant adapters and chargers for consumer electronics such a smart phones, tablet computers, and cameras. A 10-W application for a USB charger is shown in 図 8-2.

This procedure outlines the steps to design a constant-voltage, constant-current flyback converter using the UCC28740-Q1 controller. See 図 8-2 for component names and network locations. The design procedure equations use terms that are defined below.

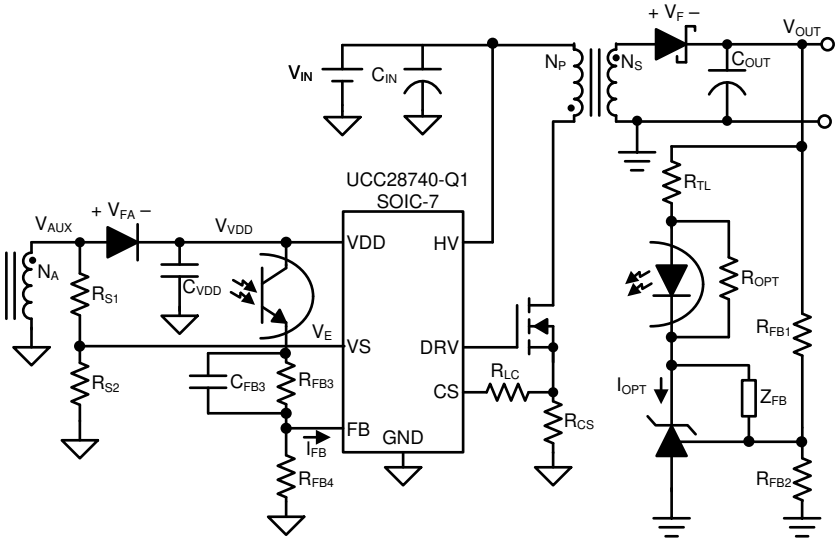


図 8-2. Design Procedure Application Example

8.3.1 Design Requirements

表 8-1. Design Parameters

PARAMETER	NOTES AND CONDITIONS	MIN	NOM	MAX	UNIT
INPUT CHARACTERISTICS					
Input Voltage, V_{IN}		85	115/230	265	V_{RMS}
Maximum Input Current	$V_{IN} = V_{INmin}$, $I_{OUT} = I_{OUTmax}$		0.265		A_{RMS}
Line Frequency		47	60/50	63	Hz
No Load Input Power Consumption	$V_{INmin} \le V_{IN} \le V_{INmax}$, I_{OUT} = 0 A			20	mW
OUTPUT CHARACTERISTICS					
Output Voltage, V_{OUT}	$V_{INmin} \le V_{IN} \le V_{INmax}$, 0 A ≤ $I_{OUT} \le I_{OUTmax}$	4.95	5	5.05	V
Output Load Current, CV Mode, I_{OUTmax}	$V_{INmin} \le V_{IN} \le V_{INmax}$	1.995	2.1	2.205	A
Output Voltage Regulation	Line Regulation: $V_{INmin} \le V_{IN} \le V_{INmax}$, $I_{OUT} \le I_{OUTmax}$		0.1%		
	Load Regulation: 0 A ≤ $I_{OUT} \le I_{OUTmax}$		0.1%		
Output Voltage Ripple	$V_{INmin} \le V_{IN} \le V_{INmax}$, 0 A ≤ $I_{OUT} \le I_{OUTmax}$			150	mVpp
Output Overcurrent, I_{CCC}	$V_{INmin} \le V_{IN} \le V_{INmax}$			2.5	A
Minimum Output Voltage, CC Mode	$V_{INmin} \le V_{IN} \le V_{INmax}$, $I_{OUT} = I_{OCC}$		1.78	2	V
Brown-out Protection	$I_{OUT} = I_{OUTmax}$		68		V_{RMS}
Transient Response Undershoot	$I_{OUT} = I_{OUTmax}$ to 0-A load transient	4.3			V
Transient Response Time	$I_{OUT} = I_{OUTmax}$ to 0-A load transient			20	ms
SYSTEMS CHARACTERISTICS					
Switching Frequency, f_{SW}		1.2		71	kHz
Average Efficiency	25%, 50%, 75%, 100% load average at nominal input voltages		81%		
Operating Temperature			25		°C

8.3.2 Detailed Design Procedure

8.3.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the UCC28740-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.3.2.2 Standby Power Estimate and No-Load Switching Frequency

Assuming minimal no-load standby power is a critical design requirement, determine the estimated no-load power loss based on an accounting of all no-load operating and leakage currents at their respective voltages. Close attention to detail is necessary to account for all of the sources of leakage, however, in many cases,

prototype measurement is the only means to obtain a realistic estimation of total primary and secondary leakage currents. At present, converter standby power is certified by compliance-agency authorities based on steady-state room-temperature operation at the highest nominal input voltage rating (typically 230 Vrms).

式 6 estimates the standby power loss from the sum of all leakage currents of the primary-side components of the converter. These leakage currents are measured in aggregate by disconnecting the HV input of the controller from the bulk-voltage rail to prevent operating currents from interfering with the leakage measurement.

$$P_{PRI\_SB} = V_{BULK} \times \sum_{k=1}^{n_P} I_{PRI\_LK_K} \tag{6}$$

式 7 estimates the standby power loss from the sum of all leakage and operating currents of the secondary-side components on the output of the converter. Leakage currents result from reverse voltage applied across the output rectifier and capacitors, while the operating current includes currents required by the shunt-regulator, optocoupler, and associated components.

$$P_{SEC\_SB} = V_{OCV} \times \sum_{k=1}^{n_S} I_{SEC_K} \tag{7}$$

式 8 estimates the standby power loss from the sum of all leakage and operating currents of the auxiliary-side components on the controller of the converter. Leakage currents of the auxiliary diode and capacitor are usually negligible. The operating current includes the wait-state current, I_{WAIT}, of the UCC28740-Q1 controller, plus the optocoupler-output current for the FB network in the steady-state no-load condition. The VDD voltage in the no-load condition V_{VDDNL} are the lowest practicable value to minimize loss.

$$P_{AUX\_SB} = V_{VDDNL} \times \sum_{k=1}^{n_a} I_{AUX_K} \tag{8}$$

Note that P_{PRI_SB} is the only loss that is not dependent on transformer conversion efficiency. P_{SEC_SB} and P_{AUX_SB} are processed through the transformer and incur additional losses as a consequence. Typically, the transformer no-load conversion efficiency η_{SWNL} lies in the range of 0.50 to 0.70. Total standby input power (no-load condition) is estimated by 式 9.

$$P_{SB} = P_{PRI\_SB} + \frac{1}{\eta_{SWNL}}\left(P_{SEC\_SB} + P_{AUX\_SB}\right) \tag{9}$$

Although the UCC28740-Q1 is capable of operating at the minimum switching frequency of 170 Hz, a typical converter is likely to require a higher frequency to sustain operation at no-load. An accurate estimate of the no-load switching frequency f_{SWNL} entails a thorough accounting of all switching-related energy losses within the converter including parasitic elements of the power-train components. In general, f_{SWNL} is likely to lie within the range of 400 Hz to 800 Hz. A more detailed treatment of standby power and no-load frequency is beyond the scope of this data sheet.

8.3.2.3 Input Bulk Capacitance and Minimum Bulk Voltage

Determine the minimum voltage on the input bulk capacitance, C_{B1} and C_{B2} total, in order to determine the maximum Np-to-Ns turns-ratio of the transformer. The input power of the converter based on target full-load efficiency, the minimum input RMS voltage, and the minimum AC input frequency determine the input capacitance requirement.

Maximum input power is determined based on I_{OCC}, V_{OCV}, V_{CBC} (if used), and the full-load conversion-efficiency target.

$$P_{IN} = \frac{(V_{OCV} + V_{CBC}) \times I_{OCC}}{\eta} \quad (10)$$

式 11 provides an accurate solution for the total input capacitance based on a target minimum bulk-capacitor voltage. Alternatively, to target a given input capacitance value, iterate the minimum capacitor voltage to achieve the target capacitance value.

$$C_{BULK} = \frac{2P_{IN} \times \left(0.25 + \frac{1}{2\pi} \times \arcsin\left(\frac{V_{BULK(min)}}{\sqrt{2} \times V_{IN(min)}}\right)\right)}{\left(2V_{IN(min)}^{2} - V_{BULK(min)}^{2}\right) \times f_{LINE}} \quad (11)$$

8.3.2.4

If using the stacked capacitor bank of CIN1 and CIN2 of figure 18 please size these capacitors with the following equation

$$C_{IN1} = C_{IN2} = C_{BULK} \times 2 \quad (12)$$

8.3.2.5 Transformer Turns-Ratio, Inductance, Primary Peak Current

The target maximum switching frequency at full-load, the minimum input-capacitor bulk voltage, and the estimated DCM resonant time determine the maximum primary-to-secondary turns-ratio of the transformer.

Initially determine the maximum-available total duty-cycle of the on-time and secondary conduction time based on the target switching frequency, f_{MAX}, and DCM resonant time. For DCM resonant frequency, assume 500 kHz if an estimate from previous designs is not available. At the transition-mode operation limit of DCM, the interval required from the end of secondary current conduction to the first valley of the V_{DS} voltage is ½ of the DCM resonant period (t_R), or 1 µs assuming 500 kHz resonant frequency. The maximum allowable MOSFET on-time D_{MAX} is determined using 式 13.

$$D_{MAX} = 1 - D_{MAGCC} - \left(\frac{t_R}{2} \times f_{MAX}\right) \quad (13)$$

When D_{MAX} is known, the maximum primary-to-secondary turns-ratio is determined with 式 14. D_{MAGCC} is defined as the secondary-diode conduction duty-cycle during CC operation and is fixed internally by the UCC28740-Q1 at 0.425. The total voltage on the secondary winding must be determined, which is the sum of V_{OCV}, V_F, and V_{OCBC}. For the 5-V USB-charger applications, a turns ratio range of 13 to 15 is typically used.

$$N_{PS(max)} = \frac{D_{MAX} \times V_{BULK(min)}}{D_{MAGCC} \times (V_{OCV} + V_F + V_{OCBC})} \quad (14)$$

A higher turns-ratio generally improves efficiency, but may limit operation at low input voltage. Transformer design iterations are generally necessary to evaluate system-level performance trade-offs. When the optimum turns-ratio N_{PS} is determined from a detailed transformer design, use this ratio for the following parameters.

The UCC28740-Q1 constant-current regulation is achieved by maintaining D_{MAGCC} at the maximum primary peak current setting. The product of D_{MAGCC} and $V_{CST(max)}$ defines a CC-regulating voltage factor V_{CCR} which is used with N_{PS} to determine the current-sense resistor value necessary to achieve the regulated CC target, I_{OCC} (see 式 15).

Because a small portion of the energy stored in the transformer does not transfer to the output, a transformer-efficiency term is included in the R_{CS} equation. This efficiency number includes the core and winding losses, the leakage-inductance ratio, and a bias-power to maximum-output-power ratio. An overall-transformer efficiency of

0.91 is a good estimate based on 3.5% leakage inductance, 5% core & winding loss, and 0.5% bias power, for example. Adjust these estimates as appropriate based on each specific application.

$$R_{CS} = \frac{V_{CCR} \times N_{PS}}{2I_{OCC}} \times \sqrt{\eta_{XFMR}} \tag{15}$$

The primary transformer inductance is calculated using the standard energy storage equation for flyback transformers. Primary current, maximum switching frequency, output voltage and current targets, and transformer power losses are included in 式 17.

First, determine the transformer primary peak current using 式 16. Peak primary current is the maximum current-sense threshold divided by the current-sense resistance.

$$I_{PP(max)} = \frac{V_{CST(max)}}{R_{CS}} \tag{16}$$

$$L_P = \frac{2\left(V_{OCV} + V_F + V_{OCBC}\right) \times I_{OCC}}{\eta_{XFMR} \times I_{PP(max)}^2 \times f_{MAX}} \tag{17}$$

N_{AS} is determined by the lowest target operating output voltage while in constant-current regulation and by the VDD UVLO turnoff threshold of the UCC28740-Q1. Additional energy is supplied to VDD from the transformer leakage-inductance which allows a lower turns ratio to be used in many designs.

$$N_{AS} = \frac{V_{VDD(off)} + V_{FA}}{V_{OCC} + V_F} \tag{18}$$

8.3.2.6 Transformer Parameter Verification

Because the selected transformer turns-ratio affects the MOSFET V_{DS} and the secondary and auxiliary rectifier reverse voltages, a review of these voltages is important. In addition, internal timing constraints of the UCC28740-Q1 require a minimum on time of the MOSFET (t_{ON}) and a minimum demagnetization time (t_{DM}) of the transformer in the high-line minimum-load condition. The selection of f_{MAX}, L_P, and R_{CS} affects the minimum t_{ON} and t_{DM}.

式 19 and 式 20 determine the reverse voltage stresses on the secondary and auxiliary rectifiers. Stray inductance can impress additional voltage spikes upon these stresses and snubbers may be necessary.

$$V_{REVS} = \frac{V_{IN(max)} \times \sqrt{2}}{N_{PS}} \times V_{OV} \tag{19}$$

$$V_{REVA} = \frac{V_{IN(max)} \times \sqrt{2}}{N_{PA}} \times V_{VDD} \tag{20}$$

For the MOSFET V_{DS} peak voltage stress, an estimated leakage inductance voltage spike (V_{LK}) is included.

$$V_{DSPK} = \left(V_{IN(max)} \times \sqrt{2}\right) + \left(V_{OCV} + V_F + V_{OCBC}\right) \times N_{PS} + V_{LK} \tag{21}$$

式 22 determines if $t_{ON(min)}$ exceeds the minimum t_{ON} target of 280 ns (maximum t_{CSLEB}). 式 23 verifies that $t_{DM(min)}$ exceeds the minimum t_{DM} target of 1.2 µs.

$$t_{ON(min)} = \frac{L_P}{V_{IN(max)} \times \sqrt{2}} \times \frac{I_{PP(max)}}{K_{AM}} \tag{22}$$

$$t_{DM(min)} = \frac{t_{ON(min)} \times V_{IN(max)} \times \sqrt{2}}{N_{PS} \times (V_{OCV} + V_F)} \quad (23)$$

8.3.2.7 VS Resistor Divider, Line Compensation

The VS divider resistors determine the output overvoltage detection point of the flyback converter. The high-side divider resistor (R_{S1}) determines the input-line voltage at which the controller enables continuous DRV operation. R_{S1} is determined based on transformer primary-to-auxiliary turns-ratio and desired input voltage operating threshold.

$$R_{S1} = \frac{V_{IN(run)} \times \sqrt{2}}{N_{PA} \times I_{VSL(run)}} \quad (24)$$

The low-side VS pin resistor is then selected based on the desired overvoltage limit, V_{OV}.

$$R_{S2} = \frac{R_{S1} \times V_{OVP}}{N_{AS} \times (V_{OV} - V_F) - V_{OVP}} \quad (25)$$

The UCC28740-Q1 maintains tight constant-current regulation over varying input line by using the line-compensation feature. The line-compensation resistor (R_{LC}) value is determined by current flowing in R_{S1} and the total internal gate-drive and external MOSFET turnoff delay. Assume an internal delay of 50 ns in the UCC28740-Q1.

$$R_{LC} = \frac{K_{LC} \times R_{S1} \times R_{CS} \times t_D \times N_{PA}}{L_P} \quad (26)$$

8.3.2.8 Output Capacitance

The output capacitance value is often determined by the transient-response requirement from the no-load condition. For example, in typical low-power USB-charger applications, there is a requirement to maintain a minimum transient V_O of 4.1 V with a load-step I_{TRAN} from 0 mA to 500 mA. Yet new higher-performance applications require smaller transient voltage droop $V_{O\Delta}$ with I_{TRAN} of much greater amplitude (such as from no-load to full-load), which drives the need for high-speed opto-coupled voltage feedback.

$$C_{OUT} \geq \frac{I_{TRAN} \times t_{RESP}}{V_{O\Delta}} \quad (27)$$

where

- t_{RESP} is the time delay from the moment I_{TRAN} is applied to the moment when I_{FB} falls below 1 µA

Additional considerations for the selection of appropriate output capacitors include ripple-current, ESR, and ESL ratings necessary to meet reliability and ripple-voltage requirements. Detailed design criteria for these considerations are beyond the scope of this datasheet.

8.3.2.9 VDD Capacitance, C_{VDD}

The capacitance on VDD must supply the primary-side operating current used during startup and between low-frequency switching pulses. The largest result of three independent calculations denoted in 式 28, 式 29, and 式 30 determines the value of C_{VDD}.

At startup, when $V_{VDD(on)}$ is reached, C_{VDD} alone supplies the device operating current and MOSFET gate current until the output of the converter reaches the target minimum-operating voltage in CC regulation, V_{OCC}. Now the auxiliary winding sustains VDD for the UCC28740-Q1 above UVLO. The total output current available to the load and to charge the output capacitors is the CC-regulation target, I_{OCC}. 式 28 assumes that *all* of the output current of the converter is available to charge the output capacitance until V_{OCC} is achieved. For typical

applications, 式 28 includes an estimated $q_G f_{SW(max)}$ of average gate-drive current and a 1-V margin added to V_{VDD}.

$$C_{VDD} \geq \frac{\left(I_{RUN} + q_G f_{SW(max)}\right) \times \frac{C_{OUT} \times V_{OCC}}{I_{OCC}}}{V_{DD(on)} - \left(V_{VDD(off)} + 1\,V\right)} \quad (28)$$

During a worst-case un-load transient event from full-load to no-load, C_{OUT} overcharges above the normal regulation level for a duration of t_{OV}, until the output shunt-regulator loading is able to drain V_{OUT} back to regulation. During t_{OV}, the voltage feedback loop and optocoupler are saturated, driving maximum I_{FB} and temporarily switching at $f_{SW(min)}$. The auxiliary bias current expended during this situation exceeds that normally required during the steady-state no-load condition. 式 29 calculates the value of C_{VDD} (with a safety factor of 2) required to ride through the t_{OV} duration until steady-state no-load operation is achieved.

$$C_{VDD} \geq \frac{2 \times I_{AUXNL(max)} \times t_{OV}}{V_{VDDFL} - \left(V_{VDD(off)} + 1\,V\right)} \quad (29)$$

Finally, in the steady-state no-load operating condition, total no-load auxiliary-bias current, I_{AUXNL} is provided by the converter switching at a no-load frequency, f_{SWNL}, which is generally higher than $f_{SW(min)}$. C_{VDD} is calculated to maintain a target VDD ripple voltage lower than ΔV_{VDD}, using 式 30.

$$C_{VDD} \geq \frac{I_{AUXNL} \times \frac{1}{f_{SWNL}}}{\Delta V_{VDD}} \quad (30)$$

8.3.2.10 Feedback Network Biasing

Achieving very low standby power while maintaining high-performance load-step transient response requires careful design of the feedback network. Optically coupled secondary-side regulation is used to provide the rapid response needed when a heavy load step occurs during the no-load condition. One of the most commonly used devices to drive the optocoupler is the TL431 shunt-regulator, due to its simplicity, regulation performance, and low cost. This device requires a minimum bias current of 1 mA to maintain regulation accuracy. Together with the UCC28740-Q1 primary-side controller, careful biasing will ensure less than 30 mW of standby power loss at room temperature. Where a more stringent standby loss limit of less than 10 mW is required, the TLV431 device is recommended due to its minimum 80-µA bias capability.

Facilitating these low standby-power targets is the approximate 23-µA range of the FB input for full to no-load voltage regulation. The control-law profile graph (see 図 7-5) shows that for FB-input current greater than 22 µA, no further reduction in switching frequency is possible. Therefore, minimum power is converted at $f_{SW(min)}$. However, the typical minimum steady-state operating frequency tends to be in the range of several-hundred Hertz, and consequently the maximum steady-state FB current at no-load will be less than I_{FBMAX}. Even so, prudent design practice dictates that I_{FBMAX} should be used for conservative steady-state biasing calculations. At this current level, V_{FBMAX} can be expected at the FB input.

Referring to the Design Procedure Application Example in 図 8-2, the main purpose of R_{FB4} is to speed up the turnoff time of the optocoupler in the case of a heavy load-step transient condition. The value of R_{FB4} is determined empirically due to the variable nature of the specific optocoupler chosen for the design, but tends to fall within the range of 10 kΩ to 100 kΩ. A tradeoff must be made between a lower value for faster transient response and a higher value for lower standby power. R_{FB4} also serves to set a minimum bias current for the optocoupler and to drain dark current.

It is important to understand the distinction between *steady-state* no-load bias currents and voltages which affect standby power, and the varying extremes of these same currents and voltages which affect regulation during transient conditions. Design targets for minimum standby loss and maximum transient response often result in

conflicting requirements for component values. Trade-offs, such as for R_{FB4} as discussed previously, must be made.

During standby operation, the total auxiliary current (used in 式 8) is the sum of I_{WAIT} into the IC and the no-load optocoupler-output current I_{CENL}. This optocoupler current is given by 式 31.

$$I_{CENL} = I_{FBMAX} + \frac{V_{FBMAX}}{R_{FB4}} \tag{31}$$

For fast response, the optocoupler-output transistor is biased to minimize the variation of V_{CE} between full-load and no-load operation. Connecting the emitter directly to the FB input of the UCC28740-Q1 is possible, however, an unload-step response may unavoidably drive the optocoupler into saturation which will overload the FB input with full VDD applied. A series-resistor R_{FB3} is necessary to limit the current into FB and to avoid excess draining of C_{VDD} during this type of transient situation. The value of R_{FB3} is chosen to limit the excess I_{FB} and R_{FB4} current to an acceptable level when the optocoupler is saturated. Like R_{FB4}, the R_{FB3} value is also chosen empirically during prototype evaluation to optimize performance based on the conditions present during that situation. A starting value may be estimated using 式 32.

$$R_{FB3} = \frac{V_{VDDNL} - 1\ V}{I_{CENL}} \tag{32}$$

Note that R_{FB3} is estimated based on the expected no-load VDD voltage, but full-load VDD voltage will be higher resulting in initially higher I_{CE} current during the unload-step transient condition. Because R_{FB3} is interposed between V_E and the FB input, the optocoupler transistor V_{CE} varies considerably more as I_{CE} varies and transient response time is reduced. Capacitor C_{FB3} across R_{FB3} helps to improve the transient response again. The value of C_{FB3} is estimated initially by equating the $R_{FB3}C_{FB3}$ time constant to 1 ms, and later is adjusted higher or lower for optimal performance during prototype evaluation.

The optocoupler transistor-output current I_{CE} is proportional to the optocoupler diode input current by its current transfer ratio, CTR. Although many optocouplers are rated with nominal CTR between 50% and 600%, or are ranked into narrower ranges, the actual CTR obtained at the low currents used with the UCC28740-Q1 falls around 5% to 15%. At full-load regulation, when I_{FB} is near zero, V_{FB} is still approximately 0.4 V and this sets a minimum steady-state current for I_{CE} through R_{FB4}. After choosing an optocoupler, the designer must characterize its CTR over the range of low output currents expected in this application, because optocoupler data sheets rarely include such information. The actual CTR obtained is required to determine the diode input current range at the secondary-side shunt-regulator.

Referring again to 図 8-2, the shunt-regulator (typically a TL431) current must be at least 1 mA even when almost no optocoupler diode current flows. Since even a near-zero diode current establishes a forward voltage, R_{OPT} is selected to provide the minimum 1-mA regulator bias current. The optocoupler input diode must be characterized by the designer to obtain the actual forward voltage versus forward current at the low currents expected. At the full-load condition of the converter, I_{FB} is around 0.5 µA, I_{CE} may be around (0.4 V / R_{FB4}), and CTR at this level is about 10%, so the diode current typically falls in the range of 25 µA to 100 µA. Typical opto-diode forward voltage at this level is about 0.97 V which is applied across R_{OPT}. If R_{OPT} is set equal to 1 kΩ, this provides 970 µA plus the diode current for I_{OPT}.

As output load decreases, the voltage across the shunt-regulator also decreases to increase the current through the optocoupler diode. This increases the diode forward voltage across R_{OPT}. CTR at no-load (when I_{CE} is higher) is generally a few percent higher than CTR at full-load (when I_{CE} is lower). At steady-state no-load condition, the shunt-regulator current is maximized and can be estimated by 式 31 and 式 33. I_{OPTNL}, plus the sum of the leakage currents of all the components on the output of the converter, constitute the total current required for use in 式 7 to estimate secondary-side standby loss.

$$I_{OPTNL} = \frac{I_{CENL}}{CTR_{NL}} + \frac{V_{OPTNL}}{R_{OPT}} \tag{33}$$

The shunt-regulator voltage can decrease to a minimum, saturated level of about 2 V. To prevent excessive diode current, a series resistor, R_{TL}, is added to limit I_{OPT} to the maximum value necessary for regulation. 式 34 provides an estimated initial value for R_{TL}, which may be adjusted for optimal limiting later during the prototype evaluation process.

$$R_{TL} = \frac{V_{OUTNL} - V_{OPTNL} - 2\ V}{I_{OPTNL}} \tag{34}$$

The output-voltage sense-network resistors R_{FB1} and R_{FB2} are calculated in the usual manner based on the shunt-regulator reference voltage and input bias current. Having characterized the optocoupler at low currents and determined the initial values of R_{FB1}, R_{FB2}, R_{FB3}, R_{FB4}, C_{FB3}, R_{OPT} and R_{TL} using the above procedure, the DC-bias states of the feedback network can be established for steady-state full-load and no-load conditions. Adjustments of these initial values may be necessary to accommodate variations of the UCC28740-Q1, optocoupler, and shunt-regulator parameters for optimal overall performance.

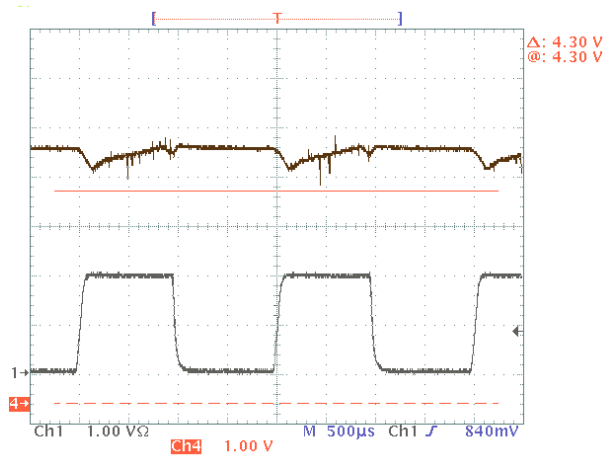
The shunt-regulator compensation network, Z_{FB}, is determined using well-established design techniques for control-loop stability. Typically, a type-II compensation network is used. The compensation design procedure is beyond the scope of this datasheet.

8.3.3 Application Curves

The transient response shown in 図 8-3 was taken with a 115 VAC, 60 Hz input voltage and a load transition from 0 A to full load. Channel 1 is the load current on a scale of 1 A per division, channel 4 is the otutput voltage on a scale of 1 V per division. The cursor shows the minimum acceptable voltage limit, 4.30 V, under transient conditions. Also note that the output waveform was taken with the probe on TP5 with the ground referenced to TP4 but not using the tip and barrel technique accounting for the high frequency noise seen on the waveform.

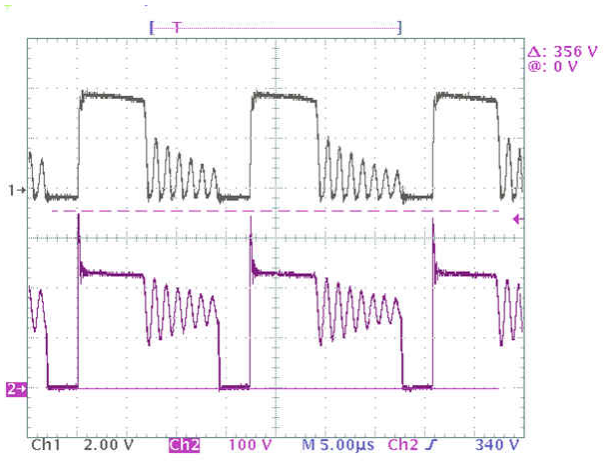
The typical switching waveform can be seen in 図 8-4. Channel 1 shows the VS pin at 2 V per division and channel 2 shows the MOSFET drain to source voltage at 100 V per division. The scan was taken at 1.8-A load, 115-VAC, 60-Hz input voltage. At this operating point, the switching frequency is dithering between 58.8 kHz and 52.6 kHz due to valley skipping.

The UCC28740-Q1 controller employs a unique control mechanism to help with EMI compliance. As shown in 図 8-5, the DRV pin, shown as channel 3, drives the gate of the MOSFET with a sequence of pulses in which there will be two longer pulses, two medium pulses, and two shorter pulses at any operating point starting with the amplitude modulation mode. The EMI dithering is not enabled at light load. Figure x shows the result of these varying pulse widths on the CS signal, shown on channel 4. The longer pulses result in a peak current threshold of 808 mV, the medium length pulses are shown measured at 780 mV, and the shorter pulses measure a threshold voltage of 752 mV. This dithering adds to the frequency jitter caused by valley skipping and results in a spread spectrum for better EMI compliance.



115 VAC, 60 Hz 0 A to 2 A
CH 1 = Load Current, 1 A/DIV
CH 4 = VOUT, cursor shows minimum limit

図 8-3. Transient Response



CH 1 = VS CH 2 = V_{DS}
I_{OUT} = 1.8 A V_{IN} = 115 VAC, 60 Hz

図 8-4. Switching Waveform

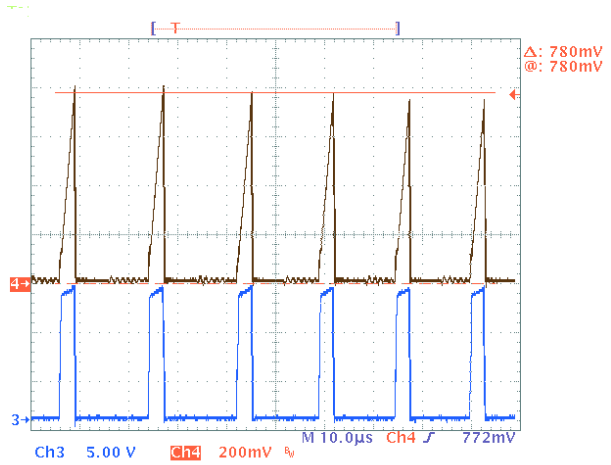


図 8-5. EMI Dithering

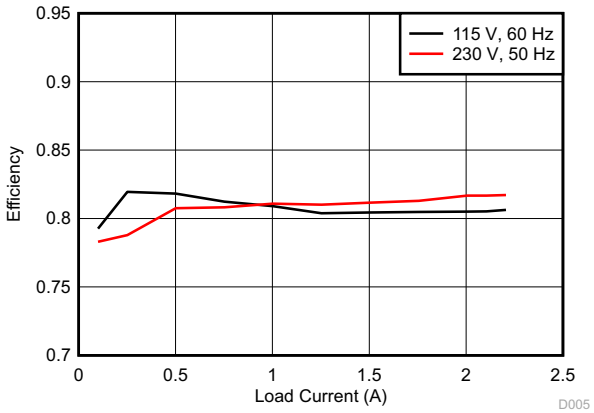


図 8-6. Efficiency

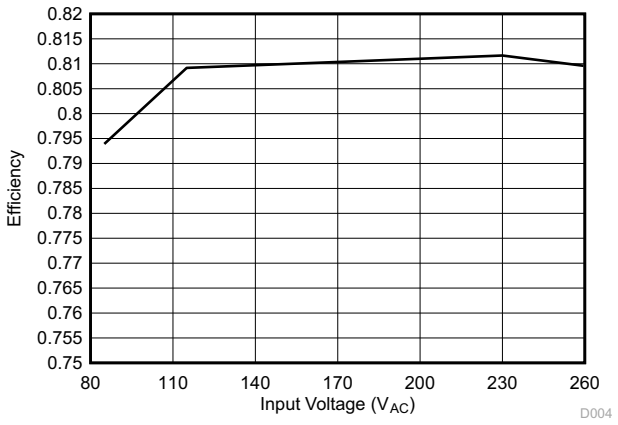


図 8-7. Average Efficiency

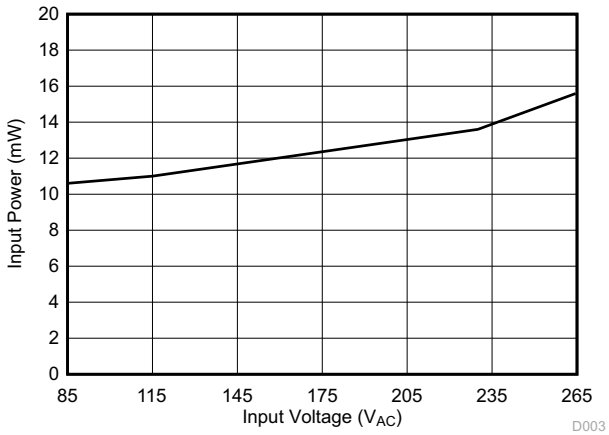


図 8-8. No Load Power Consumption

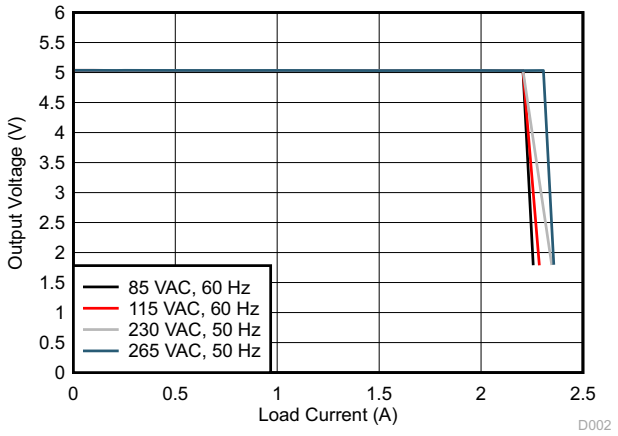


図 8-9. V_{OUT} vs. I_{OUT}

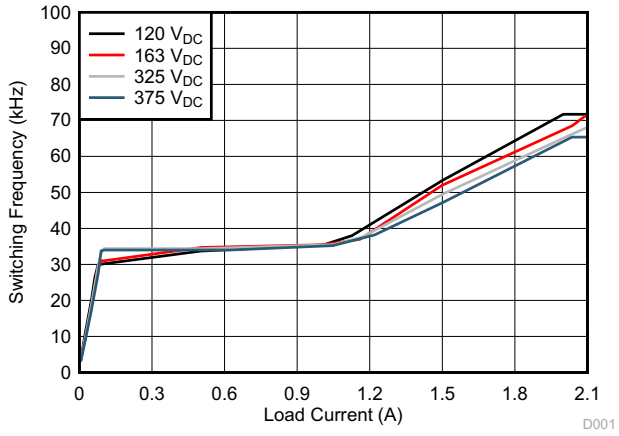
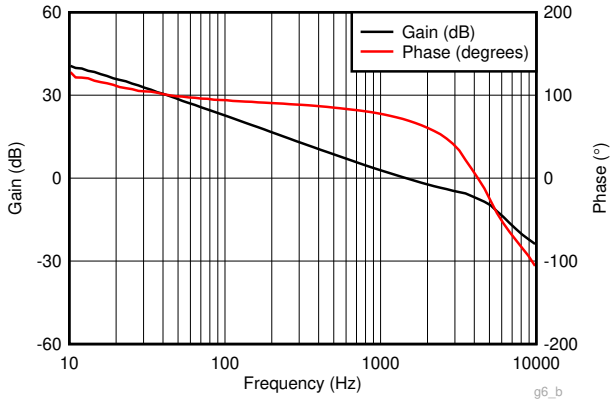


図 8-10. Control Law



V_{IN} = 115 VAC I_{OUT} = 2 A

図 8-11. Bode Plot

9 Power Supply Recommendations

The UCC28740-Q1 is designed to be used with a Universal AC input, from 85 VAC to 265 VAC, at 47 Hz to 63 Hz. Other input line conditions can be used provided the HV pin can be set up to provide 500 µA to charge the VDD capacitor for start-up through the internal startup switch. Once the VDD reaches the 21-V UVLO turnon threshold, the VDD rail should be kept within the limits of the Bias Supply Input section of the セクション *6.5* table. To avoid the possibility that the device might stop switching, VDD must not be allowed to fall below the UVLO $V_{VDD(off)}$ range.

10 Layout

10.1 Layout Guidelines

In general, try to keep all high current loops as short as possible. Keep all high current/high frequency traces away from other traces in the design. If necessary, high frequency/high current traces should be perpendicular to signal traces, not parallel to them. Shielding signal traces with ground traces can help reduce noise pick up. Always consider appropriate clearances between the high-voltage connections and any low-voltage nets.

10.1.1 VDD Pin

The VDD pin must be decoupled to GND with good quality, low ESR, low ESL ceramic bypass capacitors with short traces to the VDD and GND pins. The value of the required capacitance on VDD is determined as shown in the *セクション 8* section.

10.1.2 VS Pin

The trace between the resistor divider and the VS pin should be as short as possible to reduce/eliminate possible EMI coupling. The lower resistor of the resistor divider network connected to the VS pin should be returned to GND with short traces. Avoid adding any external capacitance to the VS pin so that there is no delay of signal; added capacitance would interfere with the accurate sensing of the timing information used to achieve valley switching and also control the duty cycle of the transformer secondary current.

10.1.3 FB Pin

The PCB tracks from the opto-coupler to the FB pin should have minimal loop area. If possible, it is recommended to provide screening for the FB trace with ground planes. A resistor to GND from the FB pin is recommended to speed up the turnoff time of the opto-coupler during a heavy load step transient. This resistor should be placed as close as possible to FB and GND with short traces, the value of this resistor, RFB4, is detailed in the *セクション 8* section.

10.1.4 GND Pin

The GND pin is the power and signal ground connection for the controller. As with all PWM controllers, the effectiveness of the filter capacitors on the signal pins depends upon the integrity of the ground return. Place all decoupling and filter capacitors as close as possible to the device pins with short traces. The IC ground and power ground should meet at the bulk capacitor's return. Try to ensure that high frequency/high current from the power stage does not go through the signal ground.

10.1.5 CS Pin

A small filter capacitor may be placed on CS to GND, with short traces, to filter any ringing that may be present at light load conditions when driving MOSFETs with large gate capacitance. This capacitor may not be required in all designs; however, it is wise to put a place holder for it in your designs. The current sense resistor should be returned to the ground terminal of the input bulk capacitor to minimize the loop area containing the input capacitor, the transformer, the MOSFET, and the current sense resistor.

10.1.6 DRV Pin

The track connected to DRV carries high dv/dt signals. Minimize noise pickup by routing the trace to this pin as far away as possible from tracks connected to the device signal inputs, FB and VS. There is no requirement for a Gate to Source resistor with this device.

10.1.7 HV Pin

Sufficient PCB trace spacing must be given between the high-voltage connections and any low-voltage nets. The HV pin may be connected directly, or through series resistance, to the rectified high voltage input rail.

10.2 Layout Example

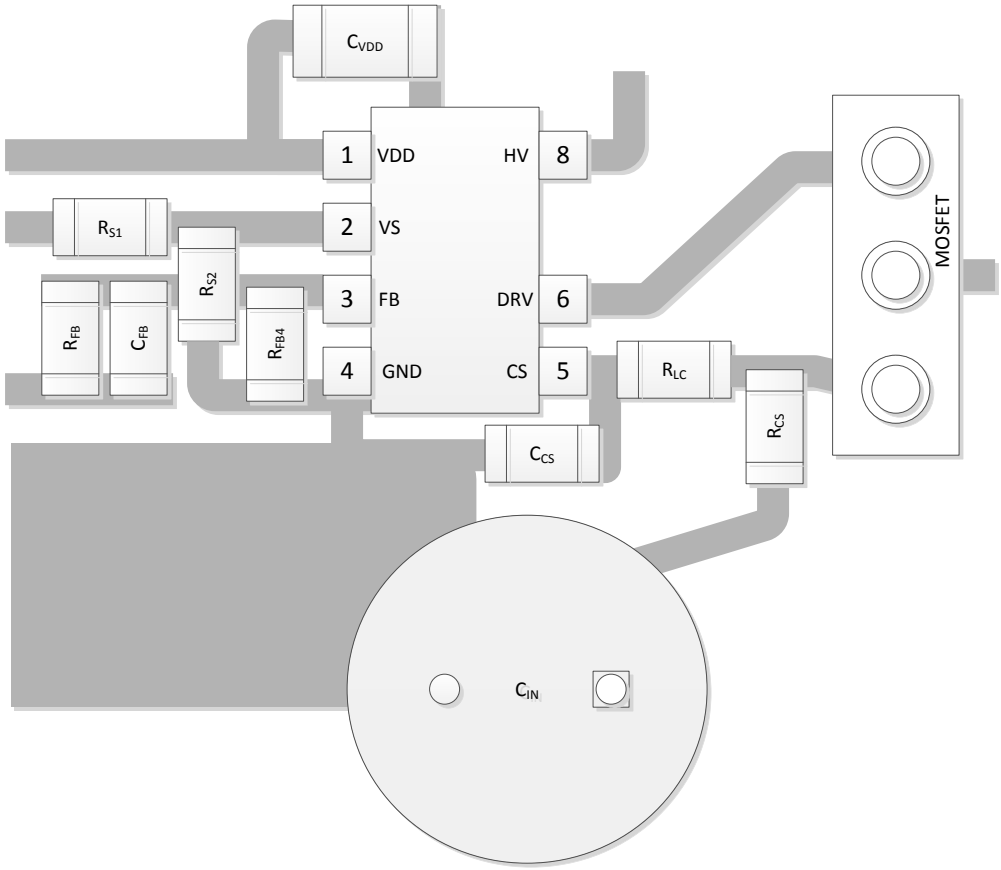


図 10-1. Layout Example Schematic

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

For design tools see the UCC28740 Design Calculator

11.1.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the UCC28740 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

11.1.2 Device Nomenclature

11.1.2.1 Capacitance Terms in Farads

C_{BULK}	The total input capacitance of C_{B1} and C_{B2}.
C_{VDD}	The minimum required capacitance on the VDD pin.
C_{OUT}	The minimum output capacitance required.

11.1.2.2 Duty Cycle Terms

D_{MAGCC}	The secondary diode conduction duty-cycle limit in CC mode, 0.425.
D_{MAX}	MOSFET on-time duty-cycle.

11.1.2.3 Frequency Terms in Hertz

f_{LINE}	The minimum input-line frequency.
f_{MAX}	The target full-load maximum switching frequency of the converter.
f_{MIN}	The steady-state minimum switching frequency of the converter.
$f_{SW(min)}$	The minimum possible switching frequency (see *セクション 6.5*).

11.1.2.4 Current Terms in Amperes

I_{OCC}	The converter output constant-current target.
$I_{PP(max)}$	The maximum transformer primary peak current.
I_{START}	The startup bias-supply current (see *セクション 6.5*).
I_{TRAN}	The required positive load-step current.
$I_{VSL(run)}$	The VS-pin run current (see *セクション 6.5*).

11.1.2.5 Current and Voltage Scaling Terms

K_{AM}	The maximum-to-minimum peak primary current ratio (see *セクション 6.5*).
K_{LC}	The current-scaling constant for line compensation(see *セクション 6.5*).

11.1.2.6 Transformer Terms

L_P The transformer primary inductance.

N_{AS} The transformer auxiliary-to-secondary turns-ratio.

N_{PA} The transformer primary-to-auxiliary turns-ratio.

N_{PS} The transformer primary-to-secondary turns-ratio.

11.1.2.7 Power Terms in Watts

P_{IN} The converter maximum input power.

P_{OUT} The full-load output power of the converter.

P_{SB} The total standby power.

11.1.2.8 Resistance Terms in Ohms

R_{CS} The primary peak-current programming resistance.

R_{ESR} The total ESR of the output capacitor(s).

R_{PL} The preload resistance on the output of the converter.

R_{S1} The high-side VS-pin sense resistance.

R_{S2} The low-side VS-pin sense resistance.

11.1.2.9 Timing Terms in Seconds

t_D The total current-sense delay including MOSFET-turnoff delay; add 50 ns to MOSFET delay.

$t_{DM(min)}$ The minimum secondary rectifier conduction time.

$t_{ON(min)}$ The minimum MOSFET on time.

t_R The resonant frequency during the DCM dead time.

t_{RESP} The maximum response time of the voltage-regulation control-loop to the maximum required load-step.

11.1.2.10 Voltage Terms in Volts

V_{BLK} The highest bulk-capacitor voltage for standby power measurement.

$V_{BULK(min)}$ The minimum valley voltage on C_{B1} and C_{B2} at full power.

V_{CCR} The constant-current regulation factor (see セクション 6.5).

$V_{CST(max)}$ The CS-pin maximum current-sense threshold (see セクション 6.5).

$V_{CST(min)}$ The CS-pin minimum current-sense threshold (see セクション 6.5).

$V_{VDD(off)}$ The UVLO turnoff voltage (see セクション 6.5).

$V_{VDD(on)}$ The UVLO turnon voltage (see セクション 6.5).

V_{DSPK} The MOSFET drain-to-source peak voltage at high line.

V_F The secondary-rectifier forward-voltage drop at near-zero current.

V_{FA} The auxiliary-rectifier forward-voltage drop.

V_{LK} The estimated leakage-inductance energy reset voltage.

$V_{O\Delta}$ The output voltage drop allowed during the load-step transient in CV mode.

V_{OCBC} The target cable-compensation voltage added to V_{OCV} (provided by an external adjustment circuit applied to the shunt-regulator). Set equal to 0 V if not used.

V_{OCC} The converter lowest output voltage target while in constant-current regulation.

V_{OCV} The regulated output voltage of the converter.

V_{OV} The maximum allowable peak output voltage.

V_{OVP} The overvoltage-detection level at the VS input (see セクション 6.5).

V_{REVA} The peak reverse voltage on the auxiliary rectifier.

V_{REVS} The peak reverse voltage on the secondary rectifier.

V_{RIPPLE} The output peak-to-peak ripple voltage at full-load.

11.1.2.11 AC Voltage Terms in V_{RMS}

$V_{IN(max)}$ The maximum input voltage to the converter.

$V_{IN(min)}$ The minimum input voltage to the converter.

$V_{IN(run)}$ The converter startup (run) input voltage.

11.1.2.12 Efficiency Terms

η The converter overall efficiency at full-power output.

η_{SB} The estimated efficiency of the converter at no-load condition, excluding startup resistance or bias losses. For a 5-V USB-charger application, 60% to 65% is a good initial estimate.

η_{XFMR} The transformer primary-to-secondary power-transfer efficiency.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

-
- *12-W Ultra-Wide Input Range Power Supply*
- *36-W, Universal Input, >90% Efficiency, Dual Output, Auxiliary Supply Reference Design for Server PSU*
- *60-W, 24-V, High-Efficiency Industrial Power Supply With Precision Voltage, Current, and Power Limit*
- *Choosing Standard Recovery Diode or Ultra-Fast Diode in Snubber*
- *Control Challenges for Low Power AC/DC Converters*
- *Integrated 30-W Sensorless BLDC Motor Drive Retrofit Reference Design With 90- to 265-V AC Input*
- *Using the UCC28740EVM-525 10 W Constant- Voltage, Constant-Current Charger Adaptor Module*
- *100-W, 24-V, High Efficiency, High PF, Industrial Power Supply With Precision Current and Power Limit*

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

11.5 Trademarks

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Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC28740QDRQ1	Active	Production	SOIC (D) | 7	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	28740Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

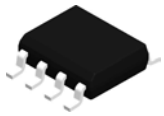
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF UCC28740-Q1 :

- Catalog : UCC28740

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

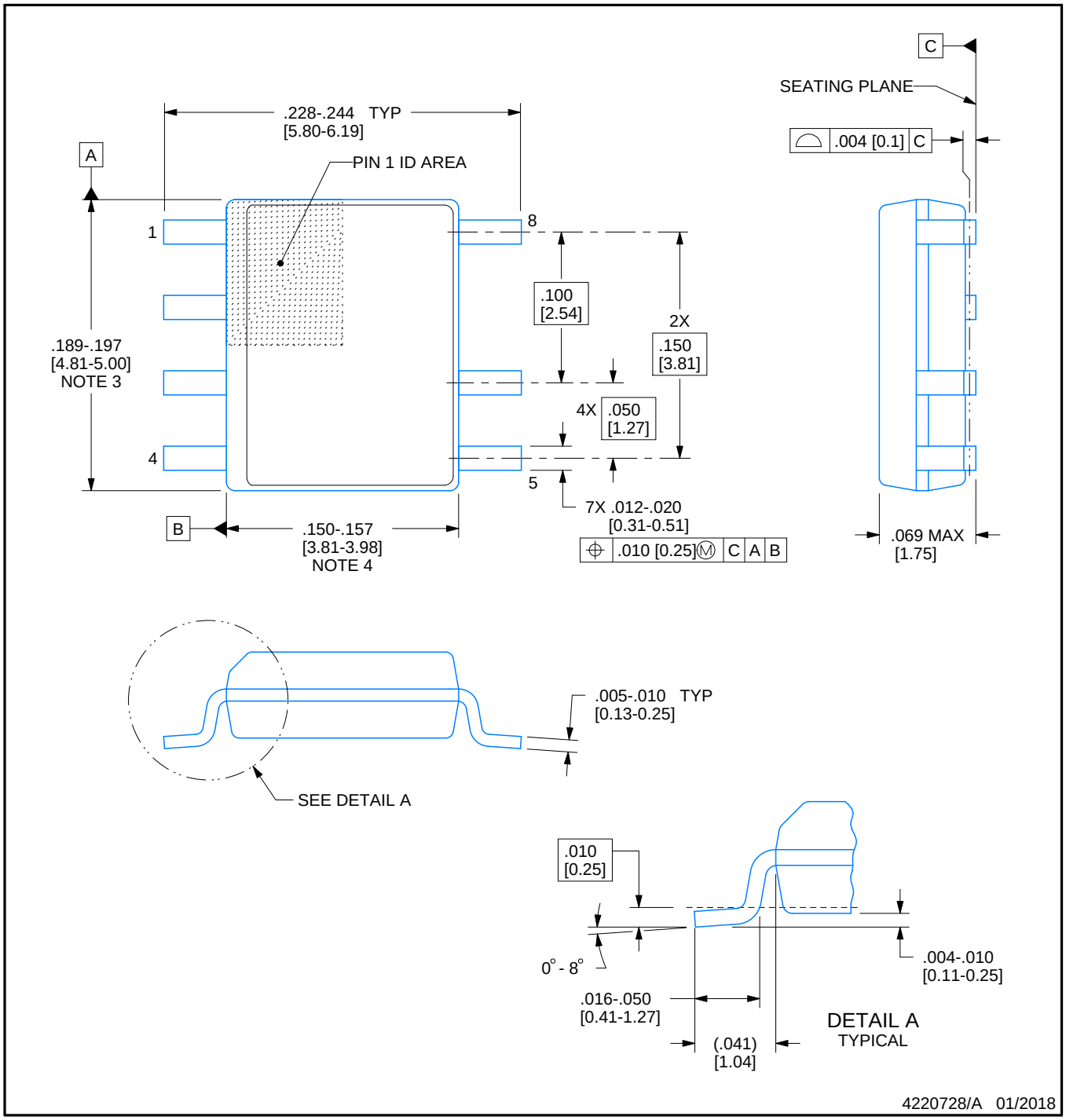


PACKAGE OUTLINE

D0007A

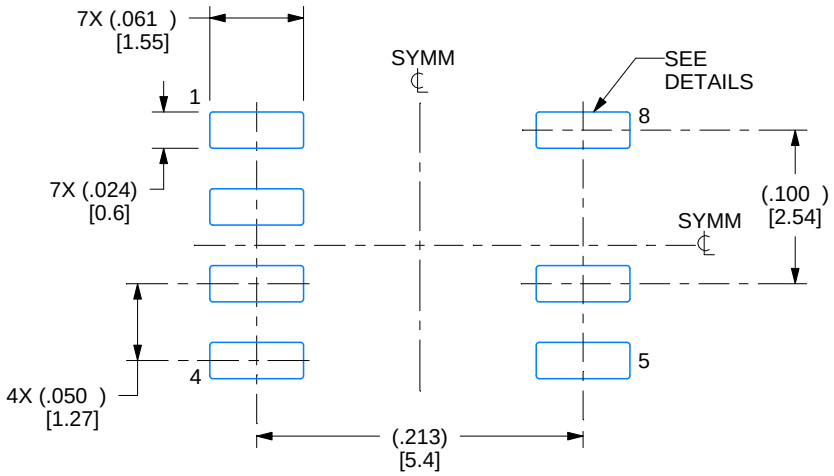
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

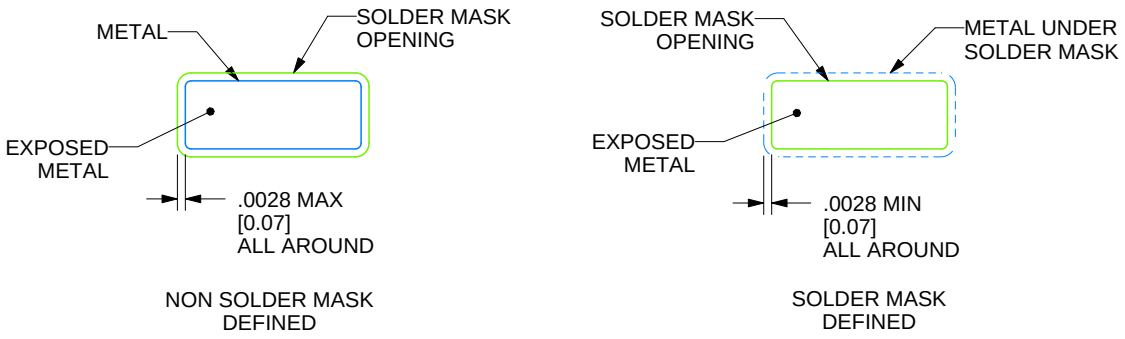


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4220728/A 01/2018

NOTES: (continued)

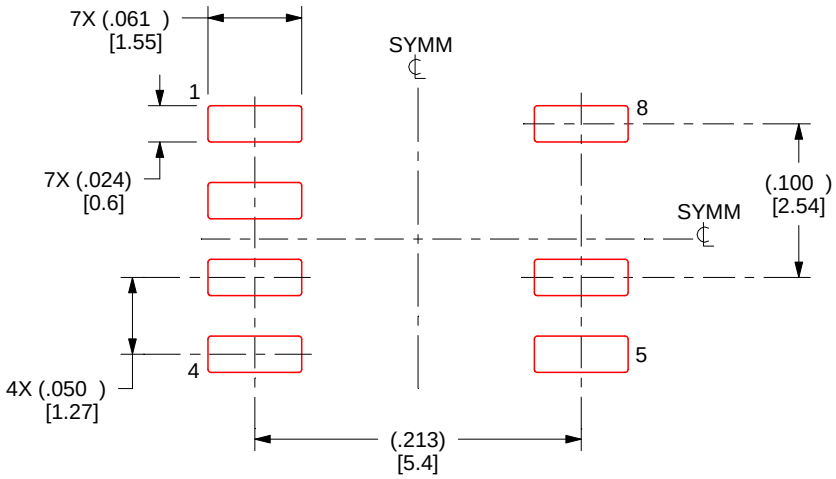
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0007A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4220728/A 01/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月