UCC28750 オフライン アプリケーション向け、2 次側安定化 (SSR) 機能搭載、電流モード フライバック コントローラ

1 特長

- 内部スロープ補償による安定した連続導通モード (CCM) 動作
- 65kHz または 100kHz の固定周波数動作
- フォトカプラによる 2 次側安定化 (SSR) 機能
- 周波数フォールドバックとバースト モードによる軽負荷時の効率の向上
- 周波数ディザリングによる EMI 性能の向上
- ゲート ソース / シンク能力：300mA/500mA
- 4ms の内部ソフト スタート
- 堅牢な保護機能：
  - 過電圧および低電圧誤動作防止
  - 出力過電力保護 (OPP)
  - 出力短絡 (OSC) 保護
  - 出力過電圧 (OVP) 保護
  - サイクル単位のピーク過電流制限
  - FLT ピンでの外部過熱、過電圧保護 (OTP、OVP)、ブラウンアウト検出
  - 内部サーマル シャットダウン

2 アプリケーション

- 絶縁型オフライン AC/DC 電源
- 電化製品
  - バッテリ・パックとチャージャ
  - 小型家電製品
  - 主な家電製品
- グリッド・インフラ
  - 電気メーター
  - ストリング・インバータ
  - マイクロインバータ
- 電力供給
  - 12V 出力、サーバー向け PSU (電源)

3 概要

UCC28750 は、フォトカプラを使用する、高性能、低スタンバイ電力、コスト効率の優れたオフライン フライバック コンバータ アプリケーション向けに最適化された、高集積電流モード、連続導通対応の PWM コントローラです。軽負荷の状況では周波数フォールドバックおよびバースト モードに移行し、軽負荷時の効率を向上させます。UCC28750 で使用されているバースト モード アルゴリズムは、最小実効スイッチング周波数を制御して、軽負荷状況における可聴ノイズを防止します。周波数ディザリングにより EMI 性能が向上します。これは、通常動作、周波数フォールドバック動作、および電力昇圧動作でアクティブになります。

UCC28750 は保護機能を搭載しており、最小限の外付け部品で堅牢なコンバータ設計を実現できます。出力過電力保護 (OPP) とサイクル単位の過電流制限により、負荷段および電力段の部品を電気的ストレスから保護します。過電圧および低電圧誤動作防止 (OVLO および UVLO) により、望ましくない入力状態でのスイッチングを防止します。FLT ピンは、デバイス バリアントに応じて、ライン ブラウンアウトの検出および保護機能、または外部過熱および過電圧保護機能を備えています。FLT ピンは、デバイス バリアントに関係なく、ピンをグランドにプルダウンして外部制御でデバイスをディセーブルにする目的にも使用されます。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
UCC28750	DBV (SOT23-6)	2.9mm×1.6mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。

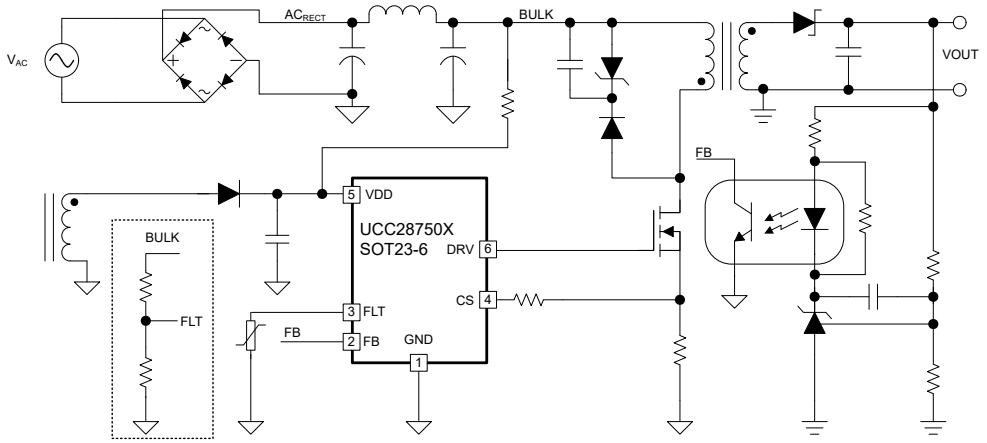

図 3-1. 代表的なアプリケーションの図

このリソースの元の言語は英語です。 翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。 実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

Table of Contents

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4 Device Comparison

Device Comparison

PART NUMBER	SWITCHING FREQUENCY	PROTECTION RESPONSE	FAULT PIN MODE
UCC287501	65kHz	Auto-Restart	Brown Out
UCC287502	65kHz	Auto-Restart	OVP, External NTC
UCC287503	65kHz	Latching	Brown Out
UCC287504	65kHz	Latching	OVP, External NTC
UCC287505	100kHz	Auto-Restart	Brown Out
UCC287506	100kHz	Auto-Restart	OVP, External NTC
UCC287507	100kHz	Latching	Brown Out
UCC287508	100kHz	Latching	OVP, External NTC

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5 Pin Configuration and Functions

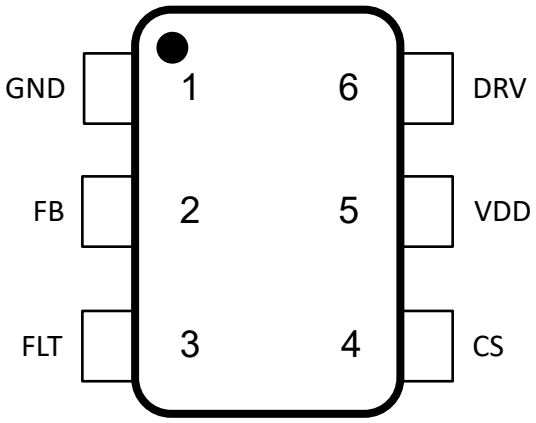

図 5-1. Top-view of DBV package (6 pins)

表 5-1. Pin Descriptions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
GND	1	G	Ground return for the controller. Connect this pin to the primary-side ground of the converter using a low-impedance path.
FB	2	I	Voltage feedback pin with internal DC bias. Typically, connect this pin to the collector of an opto-coupler device to provide isolated voltage feedback from the secondary side of the converter.
FLT	3	I	Fault sensing pin. Implement over-temperature protection by connecting an NTC resistor between this pin and GND. Connecting a resistor or Zener diode from a rectified auxiliary winding voltage can also implement output voltage overvoltage protection. Implement brownout detection by using a resistor divider from the bulk voltage to the FLT pin. Pulling this pin below the disable threshold disables switching operation.
CS	4	I	Current-sense and slope-compensation input pin. Connect this pin to the source lead of the flyback power MOSFET and the external current sensing resistor. An optional series resistor between the CS pin and source of the power MOSFET can be used to adjsut the amplitude of the controller's internal slope compensation.
VDD	5	P	Bias supply pin for the controller. Typically connect this pin the output of an auxiliary bias winding from the flyback transformer, and to a resistor network from the line voltage to provide bias at start-up. Other bias schemes that do not violate the pin ratings of the device are permissible.
DRV	6	O	Low-side gate-driver output optimized to drive low-cost silicon MOSFETs with up to 300 mA peak pull-up and 500 mA peak pull-down capability. A series gate resistor can be used to slow the turn-on and turn-off of the MOSFET to control high-frequency EMI.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
VDD	VDD input voltage range	–0.3	30	V
DRV	DRV output voltage range	–0.3	V_{VDD} + 0.3	V
CS	CS pin voltage	–0.3	5.5	V
FB	FB pin voltage	–0.3	5.5	V
	FB pin source current	Internally limited		mA
FLT	FLT pin voltage range	–0.3	5.5	V
	FLT pin sink current	0	5	mA
T_J	Junction temperature	–40	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
VDD	Operating VDD input voltage	10		26	V
DRV	DRV output voltage range	–0.3		12	V
CS	CS pin voltage	–0.3		0.9	V
FB	FB pin voltage	–0.3		2.6	V
FLT	FLT pin voltage range	–0.3		4	V
GND	GND pin voltage	–0.3		0.3	V
T_J	Junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		UCC28750 PKG DBV (SOT-23) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	231.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	158.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	117.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	94.9	°C/W

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THERMAL METRIC(1)		UCC28750 PKG DBV (SOT-23) 6 PINS	UNIT
Ψ_{JB}	Junction-to-board characterization parameter	116.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

Unless otherwise specified, VDD = 20 V; V_{FB} = 2.3 V; V_{FLT} = 2 V; T_A = 25 °C; C_{DRV} = 1000 pF

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD PIN						
$V_{uvlo(on)}$	VDD undervoltage-lockout turn-on voltage (rising)	-40°C < T_J < 125°C	14.3	15.3	16.3	V
$V_{uvlo(off)}$	VDD undervoltage-lockout turn-off voltage (falling)	-40°C < T_J < 125°C	8	9	10	V
V_{ovlo} (1)	VDD overvoltage-lockout threshold	V_{FB} = 2.3 V	26	28	30	V
V_{por} (1)	Power-on reset level (latch-off fault un-latches, IC reset)			5		V
$I_{VDD(start)}$	Start-up controller bias current	V_{VDD} = 14 V		5	10	µA
$I_{VDD(on)}$	Operating controller bias current	UCC287501/2/3/4 (65 kHz) f_{SW} = 65 kHz C_{DRV} = 1000 pF V_{FB} = 2.3 V		1.8	2.5	mA
		UCC287505/6/7/8 (100 kHz) f_{SW} = 100 kHz C_{DRV} = 1000 pF V_{FB} = 2.3 V		2	2.7	mA
$I_{VDD(wait)}$ (1)	Wait state bias current	FB Pin bias current subracted from value		360		µA
$I_{VDD(fault)}$ (1)	Fault state controller bias current	FB Pin bias current subracted from value		360		µA
$I_{VDD(dis)}$ (1)	Disabled state controller bias current	V_{FLT} = 0 V		250		µA
FB PIN (1)						
R_{FB}	Pull-up resistor			10		kΩ
$V_{FB(offset)}$	Internal offset of V_{FB}			0.8		V
G_{FB}	FB pin to CS pin ratio			2		V/V
$I_{FB(short)}$	FB pin short circuit current			0.5		mA
$V0_{peak}$	Feedback voltage pin threshold to clamp maximum switching frequency			3.0		V
$V1_{norm}$	Feedback voltage threshold to operate at the fixed switching frequency			2.6		V
$V2_{foldback}$	Feedback voltage pin threshold to linearly lower switching frequency			2.0		V
$V3_{burst}$	Feedback voltage pin threshold to enter burst mode			1.2		V
$V4_{stop}$	Feedback voltage pin threshold to stop switching			1.1		V
V_{open}	Feedback voltage open loop			5		V
V_{opp}	Feedback voltage which starts the over-power protection fault timer	Duty cycle > 60-%		2.6		V
DRV PIN (1)						
$I_{source(pk)}$ (1)	Peak driver source current			300		mA

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Unless otherwise specified, VDD = 20 V; V_{FB} = 2.3 V; V_{FLT} = 2 V; T_A = 25 °C; C_{DRV} = 1000 pF

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{sink(pk)}$ (1)	Peak driver sink current			500		mA
R_{OL} (1)	Pull-down resistance (off-state)	VDD = $V_{UVLO(off)}$ + 100 mV, I_{DRV} =1 mA		5		Ω
$V_{DRV(clamp)}$ (1)	DRV voltage clamp	VDD = 20 V		12		V
		VDD = $V_{uvlo(off)}$ + 100 mV	8			V
FLT PIN						
$V_{brownout}$ (1)	Voltage on FLT pin which causes the controller to stop switching when a brownout event is detected			1.4		V
$I_{brownout}$ (1)	Current source which changes the threshold of $V_{brownout}$ after a brown-in event, providing hysteresis			4		µA
$FLT_{hyst(brownout)}$ (1)	Hysteresis on FLT pin for the brownout threshold. The FLT pin must cross $V_{brownout}$ + $FLT_{hyst(brownout)}$ to enable switching operation			50		mV
$V_{FLT(open)}$ (1)	Voltage on FLT pin when nothing is connected	UCC287502/4/6/8		2.3		V
$V_{FLT(ovp)}$	Voltage on FLT pin which causes the controller to stop switching when an overvoltage event occurs		3.8	4.1	4.3	V
$FLT_{hyst(ovp)}$ (1)	Hyteresis on FLT pin for the overvoltage protection threshold			100		mV
$I_{FLT(ovp, clamp)}$ (1)	Current sink that is enabled during the OVP fault			500		µA
$I_{FLT(tsd)}$ (1)	Current source out of the pin into an NTC resistor for external over-temperature fault			100		µA
$V_{FLT(tsd)}$ (1)	Voltage on FLT pin which causes the controller to stop switching when an overtemperature even occurs		0.95	1	1.05	V
$FLT_{hyst(tsd)}$ (1)	Hysteresis on FLT pin for the thermal shutdown theshold			200		mV
$V_{FLT(dis)}$	Voltage on FLT pin which causes the controller to stop switching when the pin is pulled below the threshold		0.45	0.5	0.55	V
$FLT_{hyst(dis)}$ (1)	Hysteresis on FLT pin for the disable theshold			100		mV
$t_{prop(dis)}$ (1)	Propagation from the time when the disable fault occurs to the time when the controller stops switching			1		µs
CS PIN AND INTERNAL SLOPE-COMPENSATION (1)						
$V_{CS(limit)}$	CS peak current limit voltage	V_{FB} > $V0_{Norm}$		900		mV
$V_{CS(min)}$	CS peak current limit voltage	V_{FB} < $V3_{Burst}$		200		mV
$t_{ontime(min)}$	Minimum on time possible, this is a sum of the $t_{prop(ocl)}$ and t_{leb} specifications			310		ns
$t_{prop(ocl)}$	Current limit propagation delay			60		ns
t_{leb}	Leading edge blanking time			250		ns
t_{ss}	Soft-start time			4.3		ms
$I_{ramp(slope)}$	Slope compensation current ramp amplitude	V_{FB} = 2.3 V		100		µA
INTERNAL THERMAL SHUTDOWN (1)						

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Unless otherwise specified, VDD = 20 V; V_{FB} = 2.3 V; V_{FLT} = 2 V; T_A = 25 ℃; C_{DRV} = 1000 pF

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{shut}	Internal die temperature that will stop device operation			160		℃
$T_{shut(hyst)}$	Thermal shutdown hysteresis			20		℃
$T_{shut(rec)}$	Internal die temperature to recover from thermal shutdown			140		℃

(1) Specified by design, not production tested.

6.6 Switching Characteristics

Unless otherwise specified, VDD = 20 V; V_{FB} = 2.3 V; V_{FLT} = 2 V; T_A = 25 ℃; C_{DRV} = 1000 pF

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DRV PIN (1)						
t_{rise}	Drive voltage rise time	VDD > 12 V, 10-90% Rise time C_{LOAD} = 1000 pF		120		ns
t_{fall}	Drive voltage fall time	90-10% Fall time C_{LOAD} = 1000 pF		20		ns
OSCILLATOR AND FREQUENCY FOLDBACK						
f_{sw}	Switching frequency	UCC287501/2/3/4 (65 kHz version) V_{FB} = 3.5 V		130		kHz
		UCC287505/6/7/8 (100 kHz version) V_{FB} = 3.5 V		200		kHz
		$V1_{norm} < V_{FB}$		Frequency Increase		kHz
		UCC287501/2/3/4 -40℃ < T_J < 125℃ $V2_{foldback} < V_{FB} < V1_{norm}$	56	65	73	kHz
		UCC287505/6/7/8 -40℃ < T_J < 125℃ $V2_{foldback} < V_{FB} < V1_{norm}$	87	100	113	kHz
		$V3_{burst} < V_{FB} < V2_{foldback}$		Frequency Foldback		kHz
		$V4_{stop} < V_{FB} < V3_{burst}$		25		kHz
		$V_{FB} < V_{burst}$		Burst Mode Operation		kHz
D_{max}	Max Duty Cycle			80		%
$f_{dither(range)}$	Frequency modulation (EMI dither) range			± 5		%
T_{dither}	Frequency modulation period (EMI dither)	From peak to peak f_{sw}		4.4		ms

(1) Specified by design, not production tested.

6.7 Timing Requirements

Unless otherwise specified, VDD = 20 V; V_{FB} = 2.3 V; V_{FLT} = 2 V; T_A = 25 ℃; C_{DRV} = 1000 pF

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PROTECTIONS(1)						
$VDD_{delay(ovlo)}$	Switching cycles required to trigger over-voltage lockout	V_{VDD} = 29 V V_{FB} = 2.3 V		3		cycles
t_{opp}	Duration that V_{FB} must be at or above the V_{opp} threshold to trigger the fault	V_{FB} = 3 V, Duty cycle > 60 %	80	85	90	ms
$t_{brownout}$	Amount of time the brownout threshold must be active to trigger the brownout fault	V_{FLT} = 1.3 V		44		ms
$FLT_{delay(ovp)}$	Delay from the time the FLT over-voltage fault occurs to when the controller stops switching	V_{FLT} = 4.1 V		3		cycles

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Unless otherwise specified, VDD = 20 V; V_{FB} = 2.3 V; V_{FLT} = 2 V; T_A = 25 °C; C_{DRV} = 1000 pF

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$FLT_{delay(tsd)}$	Delay from the time the FLT thermal shutdown fault occurs to when the controller stops switching	V_{FLT} = 0.9 V		32		cycles
$CS_{oscp(delay)}$	Number of cycles of output short circuit condition to trigger the fault	$V_{CS} \geq V_{CS(limit)}$ during t_{leb}		8		cycles
$T_{shut(delay)}$	Number of switching cycles once internal temperature reaches threshold to trigger fault	T_J > 160 °C		32		cycles

(1) Specified by design, not production tested.

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6.8 Typical Characteristics

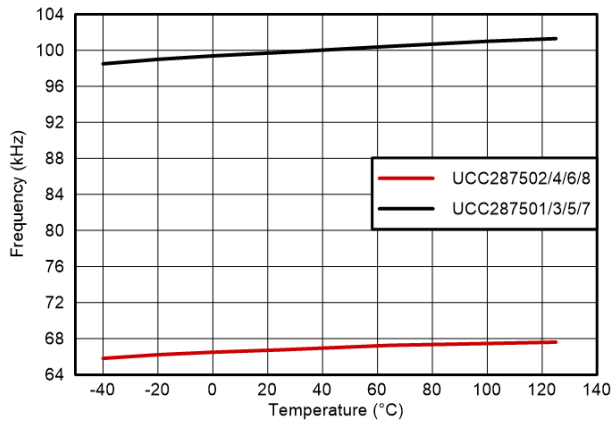

図 6-1. Switching Frequency vs Temperature

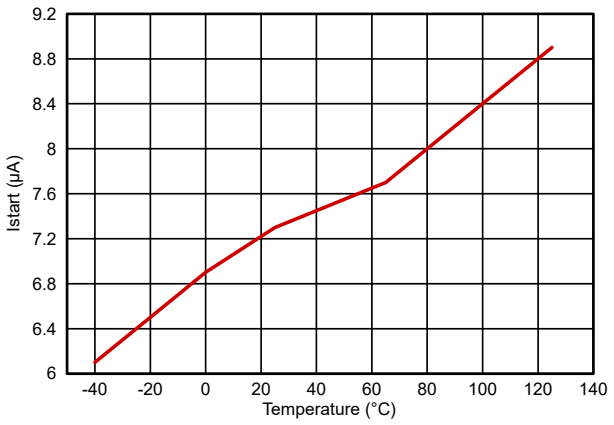

図 6-2. Startup Current vs Temperature

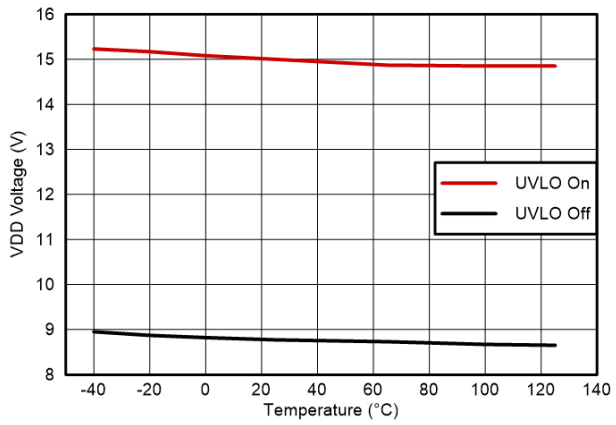

図 6-3. UVLO On/Off vs Temperature

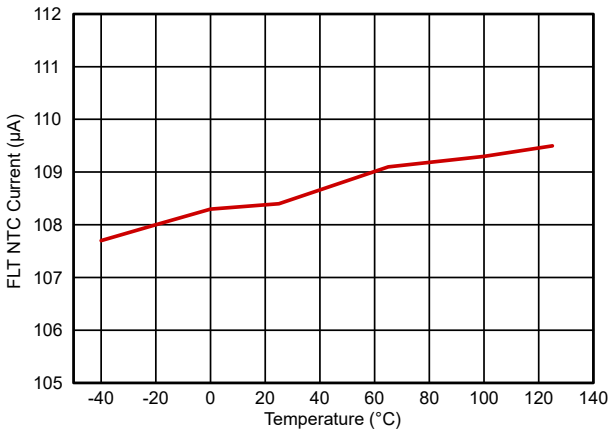

図 6-4. FLT NTC Current vs Temperature

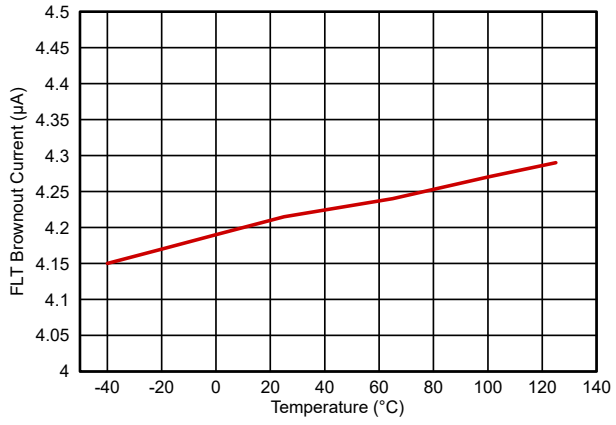

図 6-5. FLT Brownout Current vs Temperature

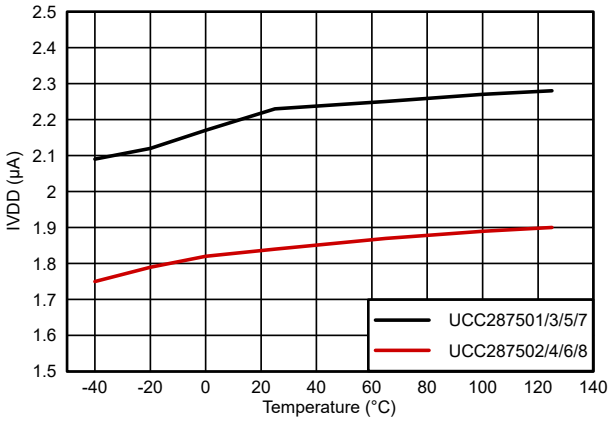

図 6-6. Operating Current vs Temperature

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6.8 Typical Characteristics (continued)

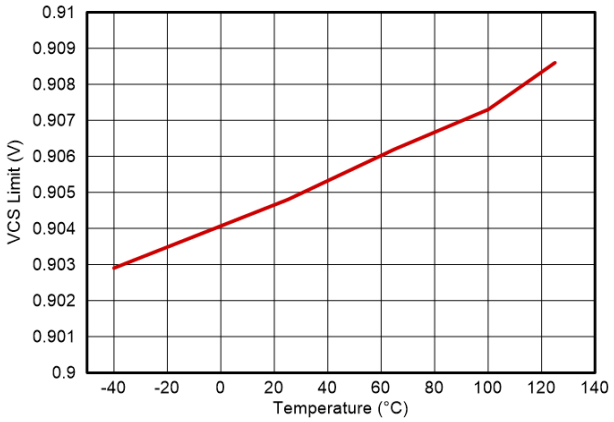

図 6-7. Current Sense Max Limit vs Temperature

7 Detailed Description

7.1 Overview

UCC28750 is a flyback controller which provides high-performance voltage regulation using an optocoupler feedback from the secondary-side. A control law allows a high efficiency across the entire load range, enabling both discontinuous-conduction mode (DCM) and continuous-conduction mode (CCM) designs. Frequency dithering lowers the EMI energy and helps ease with EMI standards compliance. The programmable FLT pin makes the controller adaptable to various protection requirements such as brown in/out, over-voltage, over-temperature, and external disable control.

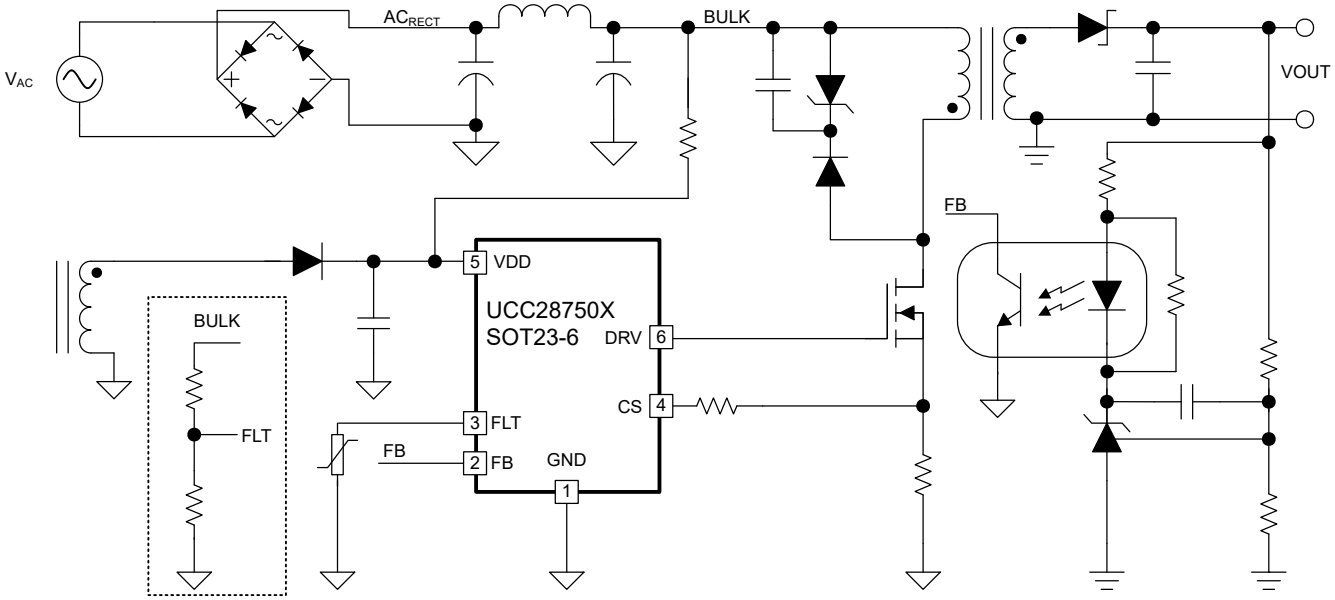

図 7-1. The UCC28750 in a flyback design

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7.2 Functional Block Diagram

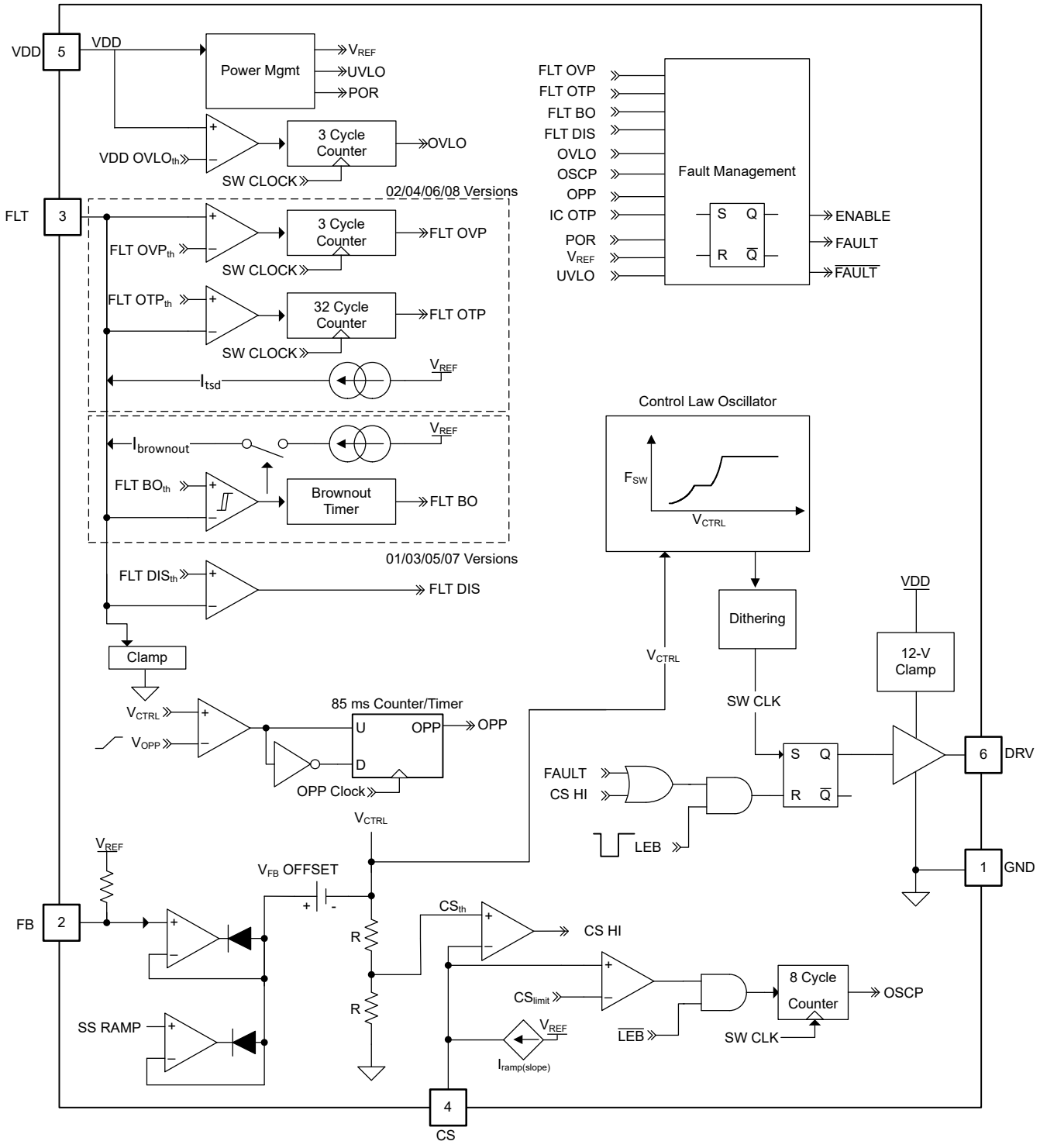

図 7-2. Functional Block Diagram

7.3 Detailed Pin Descriptions

7.3.1 VDD - Input Bias

The VDD pin provides the bias to the controller, powering the internal references, regulators, and the undervoltage lockout (UVLO) circuit. The VDD pin is typically powered through a resistor network connected to the rectified bulk voltage and later an auxiliary winding in an AC/DC flyback application or a separate, active source outside of AC/DC applications. The VDD pin has a wide range of operation from a turn on of 15.3V, $V_{uvlo(on)}$, to a turn off of 9V, $V_{uvlo(off)}$, and a max voltage of 28V, V_{ovlo}. The VDD pin has low startup current, decreasing startup time and lowering the power loss of the trickle charging network used in AC/DC flyback applications.

In addition to the C_{VDD} capacitors shown in figures 図 7-3 and 図 7-4, bypass capacitors can be added for additional filtering at the pin.

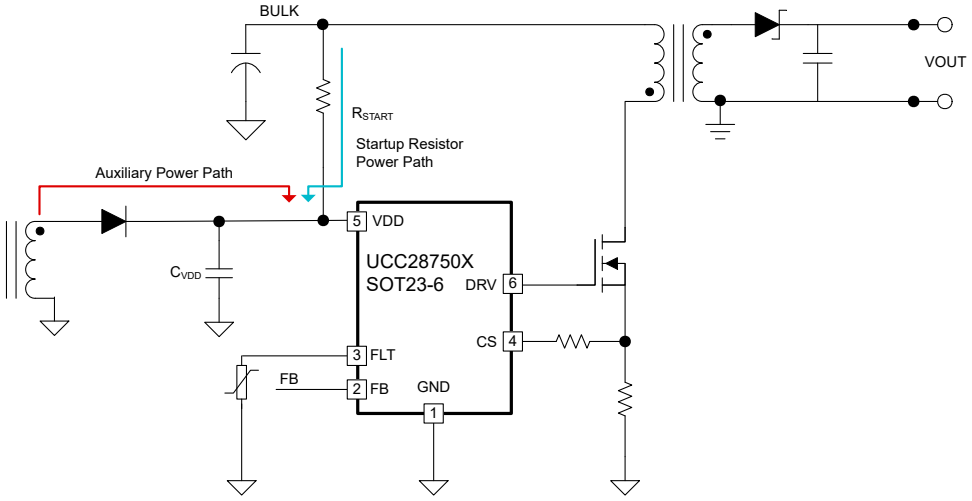

図 7-3. Biasing paths in a flyback application

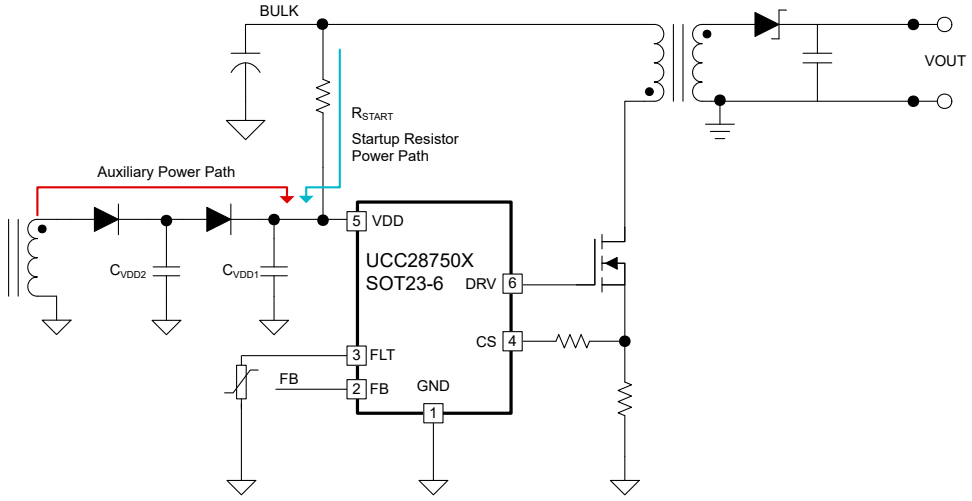

図 7-4. Biasing path using two diodes to split the VDD capacitance

Refer to セクション 8.2.3.5 in the design guide to size the VDD pin capacitance.

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7.3.2 DRV - Gate Drive Out

The DRV pin is the output of the internal gate drive of the UCC28750 controller, and is connected to the gate pin of a MOSFET switching device, typically with a series resistor. The DRV pin drives a MOSFET gate with a sink/source current of 500mA and 300mA, respectively. The DRV signal is powered through VDD, but is clamped to 12V.

7.3.3 CS - Current Sensing

The current sensing pin, CS, is an input pin which translates the primary switching device's current information into a voltage to be compared to the internal control voltage. The CS pin has a range of 200mV, $V_{CS(min)}$, to 900mV, $V_{CS(limit)}$. The generated current sense threshold is the control voltage (V_{CTRL}) divided down by a gain of 2V/V, G_{FB}.

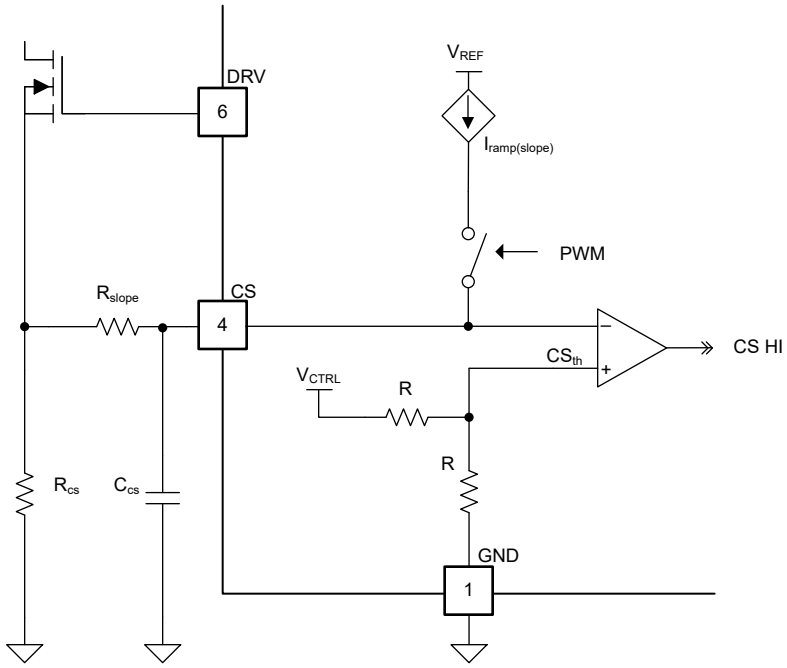

図 7-5. Current Sensing Pin Circuit

An internal slope compensation ramp, $I_{ramp(slope)}$, programmed through an external series resistor R_{slope} enables stable operation in a continuous-conduction-mode (CCM) by removing the unwanted effect of sub-harmonic oscillation when the duty cycle is above 50%.

An internal leading-edge blanking circuit blinds the controller from noise during the turn-on edge of a MOSFET. If additional filtering is required a capacitor from the CS pin to GND can be used. The time constant of the RC filter cannot be similar to the leading edge blanking time of 250ns, as the additional filtering can lead to more power being delivered than designed due to delays in sensing. In addition to delivering more power, heavy filtering on the CS pin does not allow the criteria to be met for the short-circuit protection response. The criteria for a short-circuit pulse is that the CS pin voltage is greater than 900mV, $V_{CS(limit)}$, during the leading edge blanking time.

A small capacitor with a value of 10pF to 50pF is recommended on C_{CS}.

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7.3.4 FB - Feedback

The Feedback (FB) pin connects to the collector of an analog optocoupler output transistor and carries information about the system output state. Internally, the FB node is pulled up to V_{REF} by the R_{FB} resistor. This interaction of the pull up resistor and the output current from the optocoupler output transistor work together to create a control voltage. The current sense threshold reference CS_{th} is created by offsetting the FB pin voltage by 0.8V, $V_{FB(offset)}$, then divided down by a factor of 2V/V, G_{FB}.

The control voltage directly determines the converter switching frequency and peak primary current limit. More detail is provided in the セクション 7.4.2 section of the data sheet.

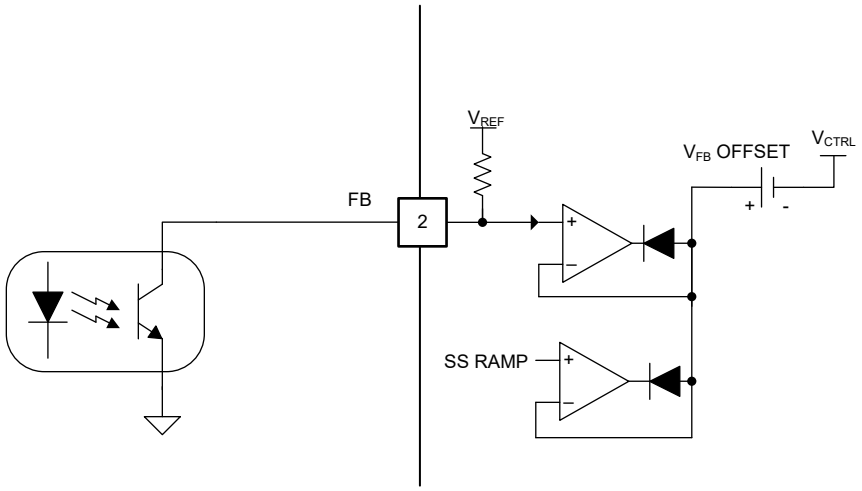

図 7-6. Feedback pin schematic drawing

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7.3.5 FLT - Fault

The FLT pin is a programmable protection pin that shuts down the device in unwanted conditions. The UCC28750 device has two versions of the FLT pin: a programmable brown-in/brown-out detection version, and over-temperature and over-voltage version. All versions of the device can disable the system by pulling the FLT pin below 0.5V, $V_{FLT(dis)}$. There is no delay in exiting the disable state when the FLT pin is raised above the $V_{FLT(dis)}$ threshold.

The brown-in/out fault detection monitors the rectified bulk voltage in a flyback application and stops switching operation when the line voltage drops below a programmed threshold longer than 45ms, $t_{brown-out}$. The brown-out fault resumes switching operation immediately when the FLT pin voltage goes above the brown-out threshold and does not wait for a new VDD fault cycle.

The overvoltage protection fault triggers when the FLT pin rises above $V_{FLT(ovp)}$ for three consecutive switching cycles. Care is required when designing the overvoltage circuit such that the current going into the FLT pin does not exceed 5mA. If the FLT pin voltage drops below 1.0V, $V_{FLT(tsd)}$, for 32 switching cycles then the overtemperature protection response is triggered.

The FLT pin can be left floating, or open, for only the UCC287502/4/6/8 variants. If the pin is left floating in UCC287501/3/5/7 variants that have the brown-out feature the device does not start up as the FLT pin is in a disable state. At startup with the brown-out configuration there is no current sourced from the FLT pin to raise the pin voltage above protection levels.

More information on the operation and programming of the FLT pin is found in section セクション 7.4.4.

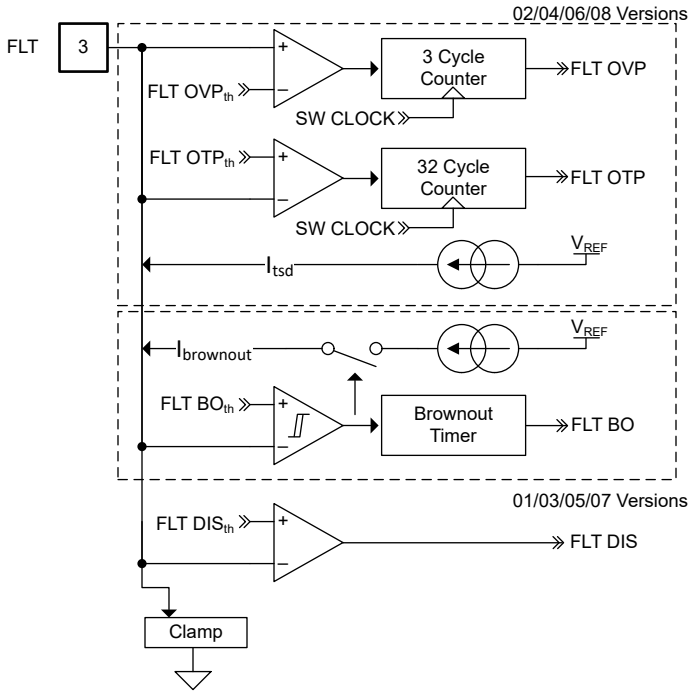

図 7-7. FLT Pin Block Diagram

7.3.6 GND - Ground Return

The GND pin is the external return pin, and provides a reference point for the internal circuitry and the gate drive of the device.

7.4 Feature Description

7.4.1 Soft Start

The UCC28750 includes a soft start feature to lower the peak current during the start-up phase. At the beginning of a normal startup operation the output voltage of the system is zero, and the capacitors at the output are discharged. In this scenario the FB pin is pulled up to the internal V_{REF} value. In a controller without a soft start feature, the controller switches at the highest power mode. The soft-start feature limits the stresses on the system and switching devices by clamping the internal FB voltage during the start-up phase to a stepping ramp. Now, the output voltage can rise in a controlled manner.

The internal soft-start ramp is compared to the FB pin voltage, and as long as the internal ramp is lower than the FB pin voltage, the internal ramp is in control of the power delivery level. As the output voltage increases to the programmed level, the FB pin decreases and takes control instead of the internal soft start ramp. The full ramp time of soft start is fixed internally to 4.3ms, t_{ss}.

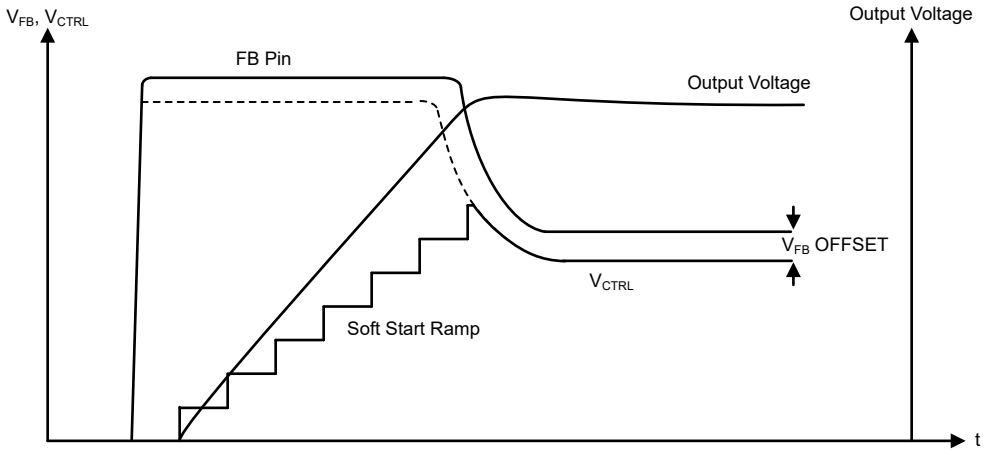

図 7-8. Softstart Ramp on Startup

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7.4.2 Control Law

UCC28750 is a fixed frequency controller under normal operating conditions, but modulates the switching frequency and CS thresholds at higher and lighter loads, providing a momentary boost of power for high loads and increased efficiency at light loads.The frequency control law uses alternating amplitude and frequency modulating regions in conjunction with an amplitude modulated current sense threshold to achieve regulation at varying conditions.

There are five regions of operation, referred to as section A-E in 図 7-9 .

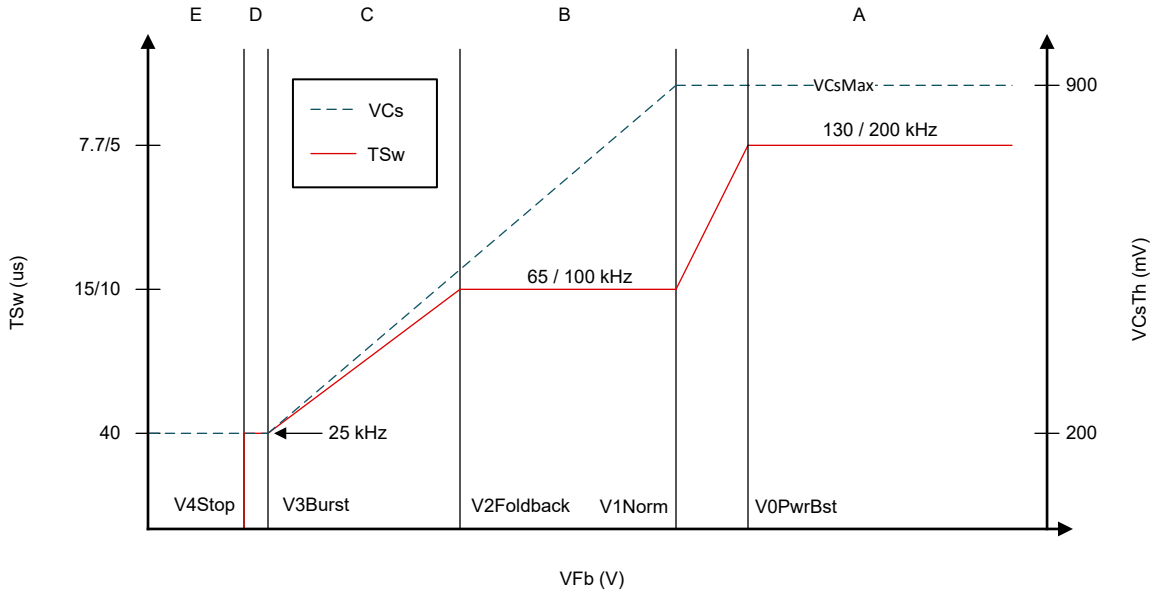

図 7-9. UCC28750 Control Law

1. Region A: This region is the power boost region in which the frequency increased to the maximum of 130/200kHz (based on the device variant) and the current sense threshold is fixed to the $V_{CS(limit)}$ of 900mV.
2. Region B: This is the normal operating region, where the switching frequency is fixed to 65/100kHz, but the current sensing threshold is amplitude modulated to provide the necessary power required by the application load.
3. Region C: This is the frequency foldback region, where the switching frequency and current sensing threshold are being lowered, to accommodate lower power requirements and lower switching losses.
4. Region D, E: These two regions are the burst mode operation of the controller. When the FB voltage is lower than 1.2V,V3Burst, but higher than 1.1V, V4Stop, the controller continues to switch but at the lowest current sensing threshold and frequency. When the FB pin voltage is below V4Stop, the controller stops switching operation. Without switching the FB pin rises as the output voltage drops, and the controller resumes switching operation.

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7.4.3 Frequency Dithering

Frequency dithering, also known as frequency swapping, frequency hopping, frequency jitter, is a concept to modulate the primary switching frequency by a small amount to spread the EMI energy, lowering EMI peaks. UCC28750 modulates the primary switching frequency by superimposing a triangular frequency onto the switching frequency, shifting the switching frequency by 5%, $f_{dither(range)}$, over a period of 240Hz, T_{dither}.

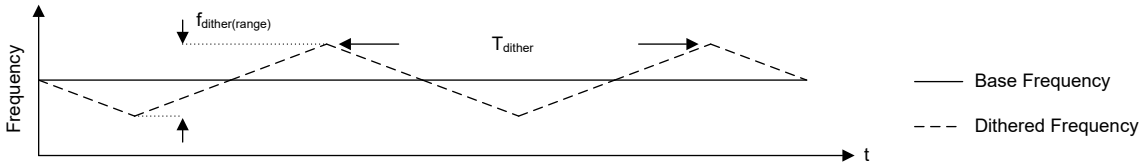

図 7-10. Frequency Dithering of a Fixed Frequency

7.4.4 Fault Protections

UCC28750 includes a set of protection features, both internally fixed and externally programmable. These faults are designed to protect the device and the system application. UCC28750 has latches and auto-restart options for the protection responses. In a latched device when a fault is detected UCC28750 does not resume switching operation, even if all faults are removed, until the VDD pin voltage is brought below 5V, V_{por}, and then up to the turn on threshold of 15.3V, $V_{uvlo(on)}$. In the auto-restart response the device resumes switching operation every startup cycle. The a fault is detected again the controller re-enters the fault state. If all faults are removed prior to a startup cycle then the controller resumes normal operation.

The faults are listen below:

- VDD under and overvoltage lockout
- Internal overtemperature shutdown
- Output overpower protection (OPP) with internal compensation
- Output short circuit protection (OSCP)
- FLT pin protections
  - Input line brown-in/out detection
  - Overvoltage protection
  - External overtemperature protection
  - Controllable disable/shutdown

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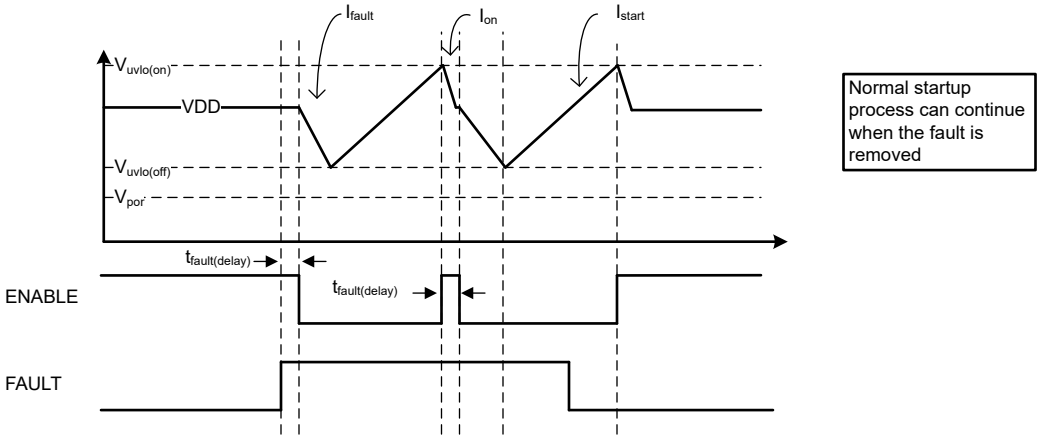

図 7-11. Auto-Restart Fault Diagram

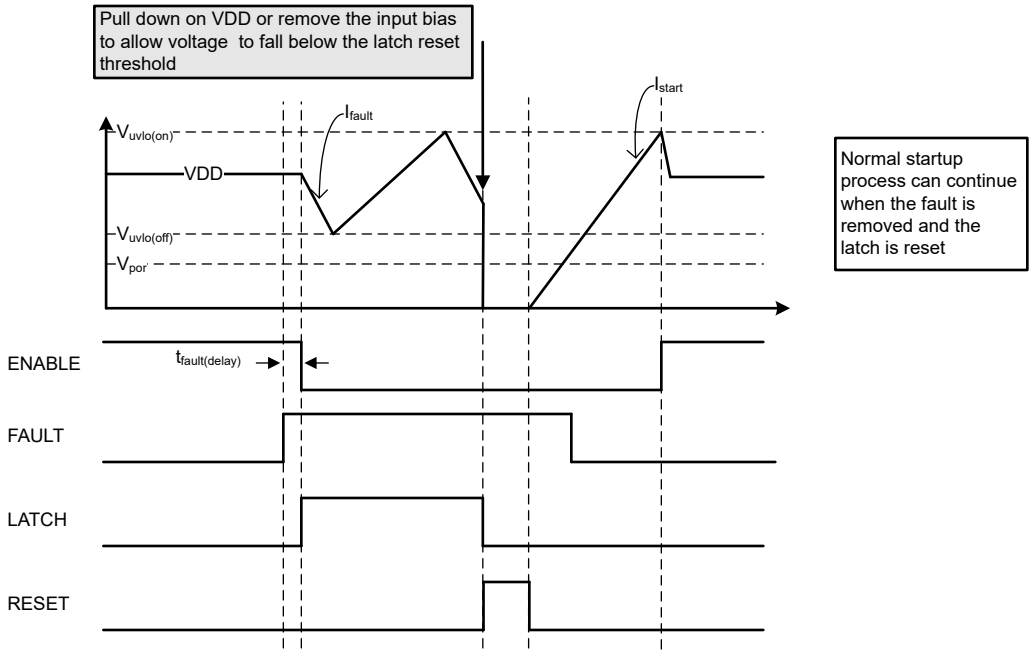

図 7-12. Latch Fault Diagram

7.4.4.1 VDD Overvoltage and Undervoltage Lockout

UCC28750 operates over a wide input voltage range, and has protections to enable safe operation. The device does not start switching operation until the input voltage, VDD, reaches above 15.3V, $V_{uvlo(on)}$, threshold. UCC28750 continues to operate until the input voltage reaches either 9V, $V_{uvlo(off)}$, or 28V, V_{ovlo}. The upper limit to the operation range is defined as the over-voltage lockout threshold. In the UVLO case, the device stops switching immediately. In the OVLO case, the device stops switching operation and triggers a protection response after the input voltage goes above the V_{ovlo} threshold for three consecutive switching cycles.

7.4.4.2 Internal Overtemperature Protection

The device has an internal temperature threshold, which disables the part once the internal die has reached 160℃ and is qualified after 32 switching cycles. The thermal shutdown threshold has a large hysteresis of 20℃. Once the fault clear temperature of 140℃ is reached the part can resume normal switching operation. If the device is a latched version, then the VDD pin voltage needs to be brought below 5V, V_{por}, to have the device resume switching operation.

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7.4.4.3 Output Overpower Protection

The output power-protection is a line-compensated, feedback based protection to limit the output power of the system application. The FB pin voltage is compared to a ramp that is generated based on the switch on-time, the duty cycle, of each switching event. When the FB pin voltage is greater than the ramp at the negative edge of the internal PWM signal, the OPP timer increases. If the FB pin voltage is less than the OPP threshold, the timer decreases. When the timer reaches the OPP time, t_{opp}, of 85ms the fault is engaged and the device stops switching.

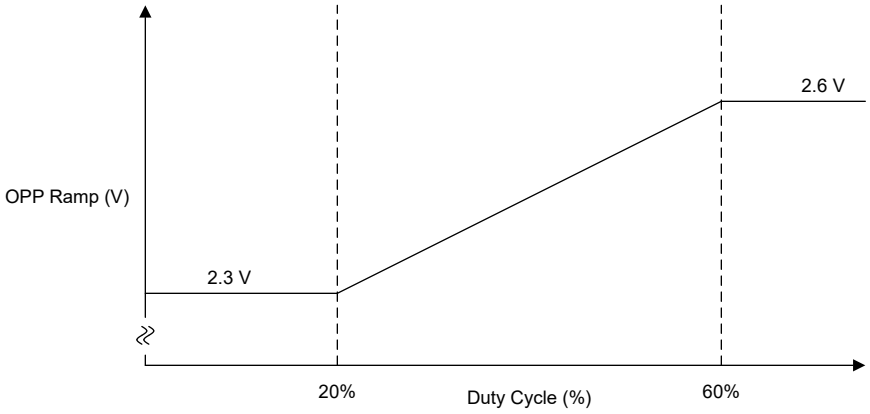

図 7-13. OPP Ramp

In 図 7-14 , the output load in an application is increased which causes the control loop to increase the FB pin voltage. The increase in FB pin voltage indicates the need to deliver more power to maintain regulation. Once the FB pin is above the OPP ramp and OPP is detected, the internal OPP timer starts counting towards the t_{opp} limit of 85ms. Eventually the OPP timer is reached and the protection is engaged and the device stops switching.

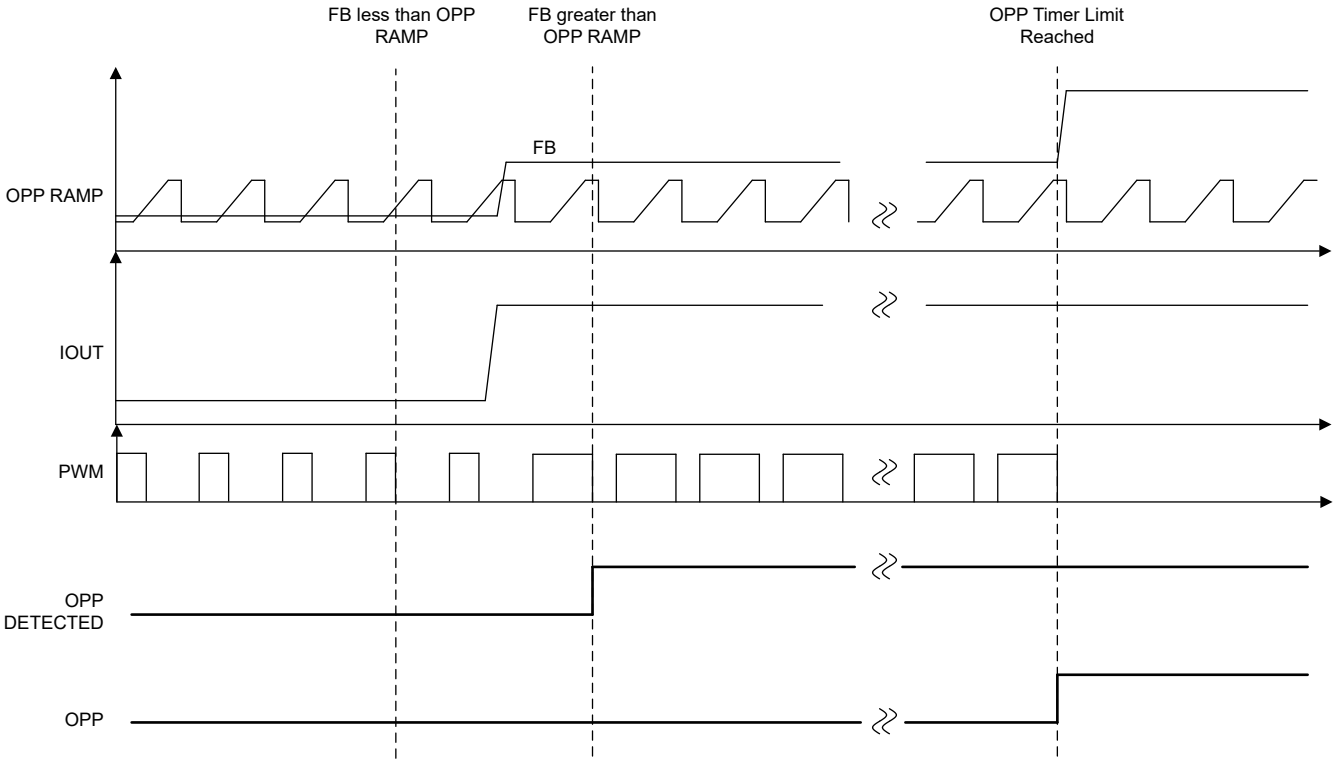

図 7-14. Load Step Causing OPP

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図 7-15 shows how the timer operation works, with a load condition that is not as long as t_{opp} initially, but with repetitive high load pulses the overpower protection can still engage. In an application that requires momentary power boosts, the time of the power boost pulse must be shorter than the time without a power boost to not engage OPP. Otherwise, over time, the internal timer reaches the 85ms limit to engage OPP.

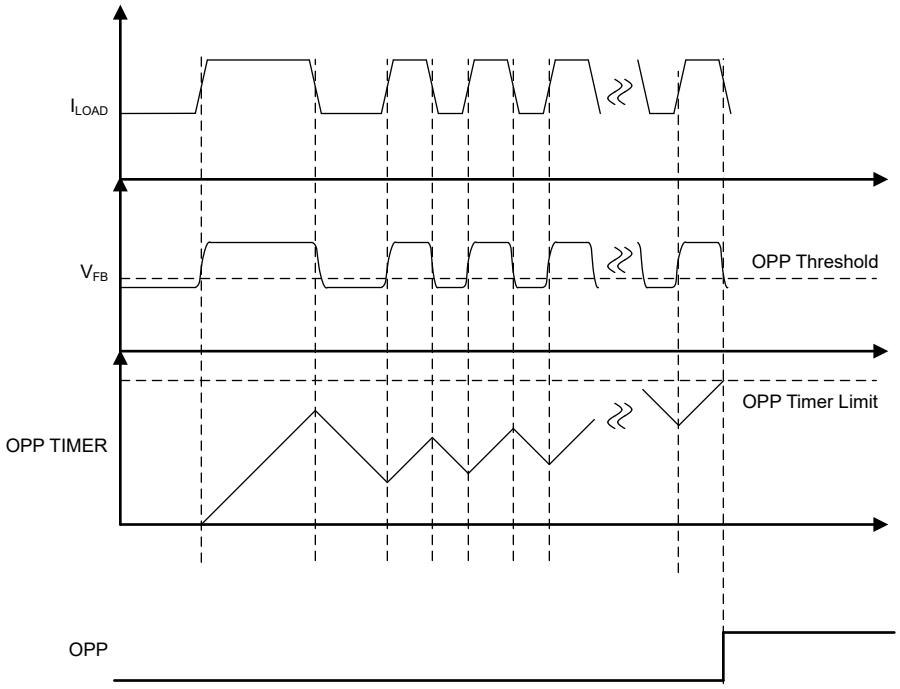

図 7-15. OPP Timer Increasing to the OPP Timer Limit

7.4.4.4 Output Short-Circuit Protection

In the event of an output short circuit, the UCC28750 can protect the system by quickly shutting down. During a short-circuit event, the current sense sees a sharp rise during the switch on-time, and a very shallow negative slope during the off-time of the switching cycle. The UCC28750 is turned on for a minimum amount of time for every switching cycle due to the leading edge blanking (LEB) feature and internal logic delays. If the CS pin is above the maximum CS threshold during the leading edge blanking time for eight cycles, the output short-circuit protection is engaged and the device stops switching operation.

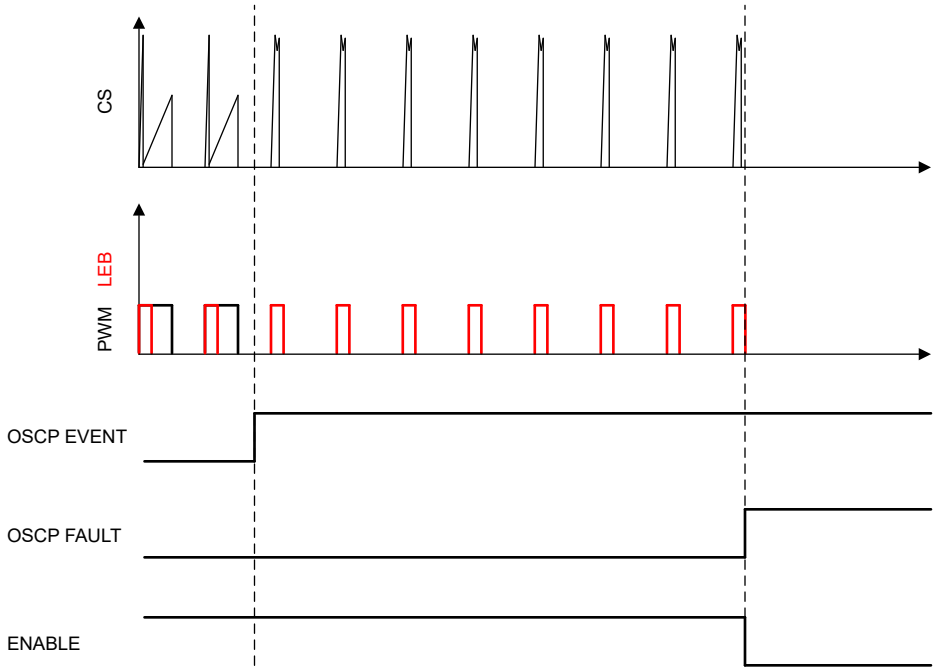

図 7-16. Output Short-Circuit Protection Diagram

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7.4.4.5 FLT Pin Protections

The FLT pin is a programmable fault pin and changes operation basedo on the UCC28750 variant, whether the device is a brown-out or over-temperature/over-voltage version.

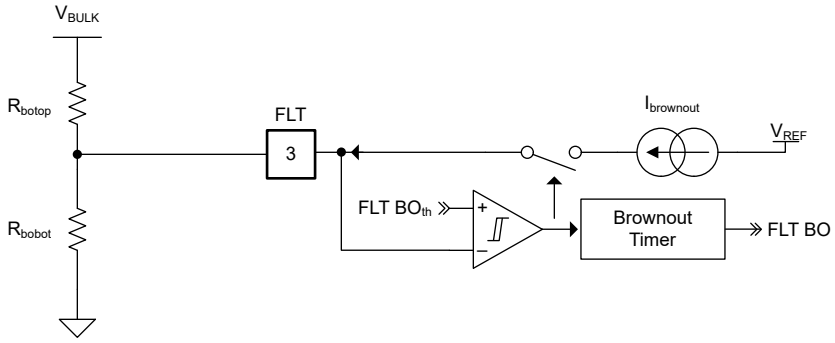

図 7-17. FLT Pin Brown-out Configuration Example

The brown-out variant is a fault method to control the turn-on and turn-off thresholds of the system application. Once the system has crossed the turn-on (also known as brown-in) threshold, the UCC28750 turns on an offset current, typically 4µA, which makes the thresholds programmable. The offset current is turned on only after the bulk voltage passes the brown-in threshold first. The FLT pin voltage must cross the $V_{brown\text{-}out}$ threshold for $t_{brown\text{-}out}$ for the brown-out fault to trigger. The time required to trigger the fault disqualifies any short term false triggering events from incorrectly triggering the brown-out. The FLT pin has a clamp internally that prevents the FLT pin from reaching dangerous levels if the application requires the brownout feature and has a wide input range requirement (such as a 100V,AC to 400V,AC operating range).

The top resistor shown in 図 7-17 must not be a single resistor. Most non-high-voltage rated resistors typically have a voltage rating of around 200V. Therefore, the top resistor in the brownout resistor divider must be formed with several resistors, typically three.

Programming the brown-in and brown-out thresholds is a matter of choosing the desired voltage divider resistor values:

$$V_{bi} = \frac{\left(V_{\text{brownout}} + 50\text{mV}\right) \times \left(R_{\text{botop}} + R_{\text{bobot}}\right)}{R_{\text{bobot}}} \quad (1)$$

$$V_{\text{bo}} = \frac{\left(V_{\text{brownout}}\right) \times \left(R_{\text{botop}} + R_{\text{bobot}}\right) - I_{\text{brownout}} \times R_{\text{bobot}} \times R_{\text{botop}}}{R_{\text{bobot}}} \quad (2)$$

Where:

- V_{bi} is the programmed brown-in input voltage level
- V_{bo} is the resultant brown-out input voltage level
- $V_{brown\text{-}out}$ is the FLT pin's brown-out threshold, 1.4V
- R_{bobot} is the bottom resistor in the voltage divider
- R_{botop} is the top equivalent resistor in the voltage divider
- $I_{brown\text{-}out}$ is the offset current enabled once the input voltage passes the V_{bi} level

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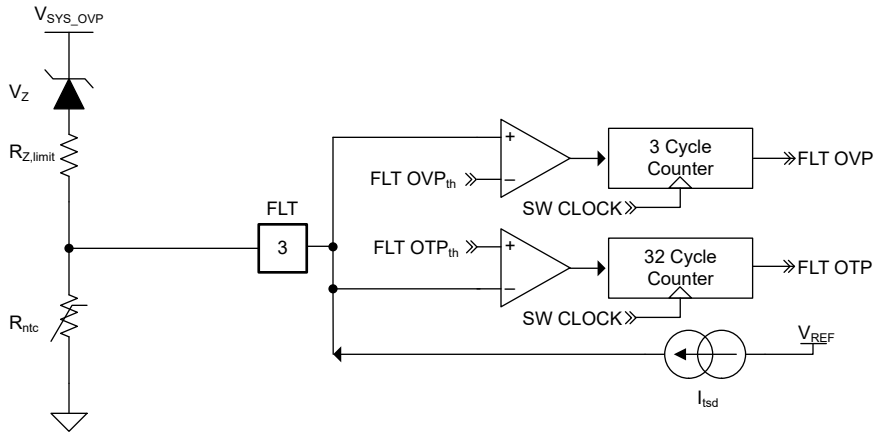

図 7-18. FLT Pin Overvoltage/Overtemperature Configuration Example

The programmable over-voltage and over-temperature features are available in the UCC28750 variants. The overvoltage protection fault is triggered when the FLT pin voltage crosses 4V, $V_{FLT(ovp)}$, for three consecutive switching cycles, similar as the three switching cycles required for OVLO. In 図 7-18, V_{SYS_OVP} is a voltage source that can be used to triggeer the protection outside of the device VDD and system output voltage. If the overvoltage is configured with a Zener diode, then the following restriction applies:

$$V_{SYS\_OVP} > V_Z - V_{FLT(ovp)} \quad (3)$$

Where:

- V_Z is the breakdown voltage of the Zener diode
- V_{SYS_OVP} is a user defined location that is susceptible to over-voltage and is used to turn off the UCC28750

Care must be take that the current going into the FLT pin from the Zener diode's breakdown does not exceed 5mA. Therefore a current limiting resistor is recommended if a Zener diode is use for overvoltage protection on the FLT pin.

A different method can be applied as long as the voltage stays within the FLT pin's voltage rating.

The overtemperature fault is triggered when the FLT pin voltage crosses the 1V, $V_{FLT(tsd)}$, overtemperature threshold for 32 switching cycles, $FLT_{delay(tsd)}$. Finally, the disable threshold of 0.5V ,$V_{FLT(dis)}$, stops switching operation immediately immediately.

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7.4.5 Slope Compensation

The UCC28750 device is a peak-current mode control device which offers high efficiency while overcoming drawbacks from voltage-mode control devices. However, when the application requires switching with a duty cycle greater than 50%, the application can suffer from an instability called sub-harmonic oscillation. 図 7-19 shows what can happen to the switching operation and inductor current of a peak current mode control scheme. The perturbed current, without a compensated ramp, cannot return to a normal steady state operation. By adding a ramp onto the fixed threshold, this phenomenon is resolved.

The slope compensation ramp is programmed through a series resistor on the CS pin, and is shown in more detail in セクション 8.2.3.3.

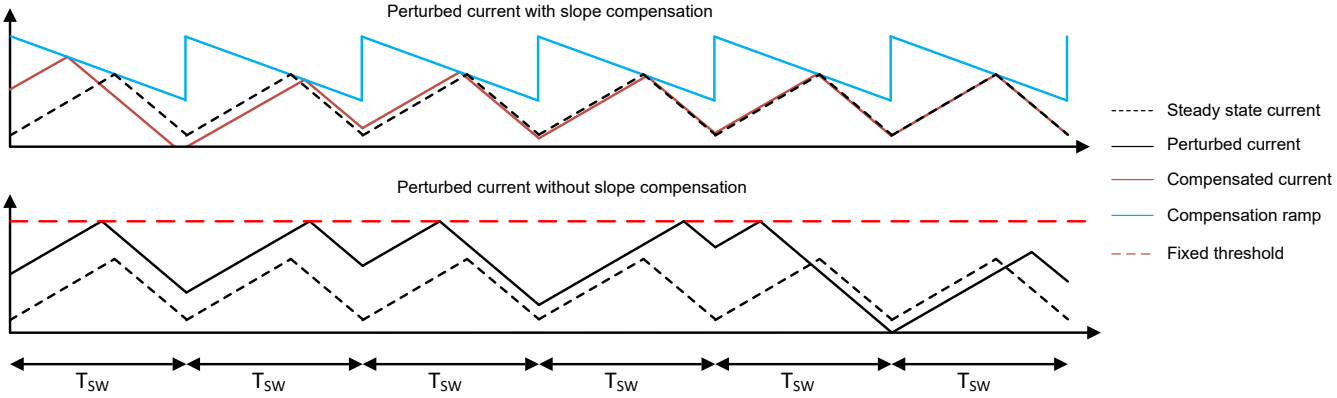

図 7-19. Slope Compensation in a Peak Current Mode Control Scheme

7.5 Device Functional Modes

7.5.1 Off

At an initial startup phase, the device is in the off state while the voltage at the VDD pin is below the $V_{uvlo(on)}$ voltage of 15.3 V. In this state the device's features and circuitry are disabled, and the device's current consumption is only the quiescent current, $I_{VDD(start)}$, of 5 µA. Once the VDD pin voltages crosses the turn on threshold, the device enters in to the startup phase. If a fault occurs, or the system application is shutting down, the device remains on until the VDD pin voltage falls below $V_{uvlo(off)}$.

7.5.2 Startup

When the UCC28750's VDD pin voltage reaches the turn-on threshold, the device enters into the startup state and begins to deliver power to the output. In this state the internal control voltage is clamped to a fixed ramp, enabling a controlled rise in the output voltage while lowering current stresses on the switching devices. After the soft start ramp is finished rising, or the FB pin voltage falls below the soft start ramp, is the startup state finished. All of the fault features are still enabled during this time, and can cause the device to enter into a fault state.

7.5.3 On

Once finished with the startup state, the device enteres the on state. In this state all of the features of the control law are enabled. The control loop of the system application takes over as the main feedback signal for the control voltage. The FB pin voltage determines the switching operation of the device, and decides if the controller operates in the burst mode, frequency foldback, fixed frequency, or power boost modes, as seen in the セクション 7.4.2 section.

7.5.4 Fault

The fault state is entered when the UCC28750 devices recognizes one of the numerous faults available, as seen in セクション 7.4.4. When a fault is triggered, the device stop switching operation, and begins to sink a fault current of 350 µA. This fault current causes the VDD pin voltage to drop to the $V_{uvlo(off)}$ voltage, turning off the device and resetting the fault logic states. Once the device crosses the turn on voltage, $V_{uvlo(on)}$, the startup phase begins and if the fault is removed then normal operation resumes. If the device is a latched variant (UCC287501/3/5/7), then the switching operation cannot resume until the VDD pin voltage is brought below the 5 V, V_{por} , power-on reset threshold. Refer to figures below for expected operation waveforms in a fault state.

To have the correctly VDD cycle as shown in the fault diagrams a restriction on the startup resistors is placed, where R_{START} is the startup resistor network shown in セクション 7.3.1.

$$\frac{V_{\text{bulk,max}}}{I_{\text{fault}}} < R_{\text{start}} \tag{4}$$

7.5.5 Disabled

The disabled state is a low-power state that is entered by bringing the FLT pin voltage below the $V_{flt(dis)}$ threshold of 0.5 V, available in all variants of the UCC28750 device. In this state the device current consumption drops to 250 µA, and switching operation is stopped. The device resumes normal operation, if no other faults are present, once the FLT pin voltage exceeds 0.5 V. A logic level MOSFET can be used with a control signal from another source to bring the FLT pin voltage below the 0.5-V threshold.

Because the device consumes less current in the disabled state, extra care must be taken with the selection of the start up trickle charge resistors if that biasing scheme is used as shown in 図 7-3 and 図 7-4. If the startup resistors are too small and do not meet the criteria of 式 5, the amount of current through the biasing path can be greater than the current that the device consumes. This leads to the VDD pin voltage rising and causing an over stress event on the VDD pin. A Zener diode can be put from VDD to GND as a safety clamp.

$$\frac{V_{\text{bulk,max}}}{I_{\text{dis}}} < R_{\text{start}} \tag{5}$$

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8 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The UCC28750 device is an optimized AC-DC flyback controller that uses secondary side regulation through an optocoupler interface and peak-current mode control to tightly regulate the output voltage. The information from the optocoupler interface determines the voltage at the FB pin, which controls the mode of operation. Under light loads the UCC28750 switches at a lower frequency, entering burst mode if the load is light enough. At higher loads the device switches at the fixed frequency, 65kHz or 100kHz, depending on the UCC28750 variant. The UCC28750 has duty cycle capabilities greater than 50%, and the integrated slope compensation allows the application to make full use of both continuous and discontinuous conduction modes of operation.

8.2 Typical Application

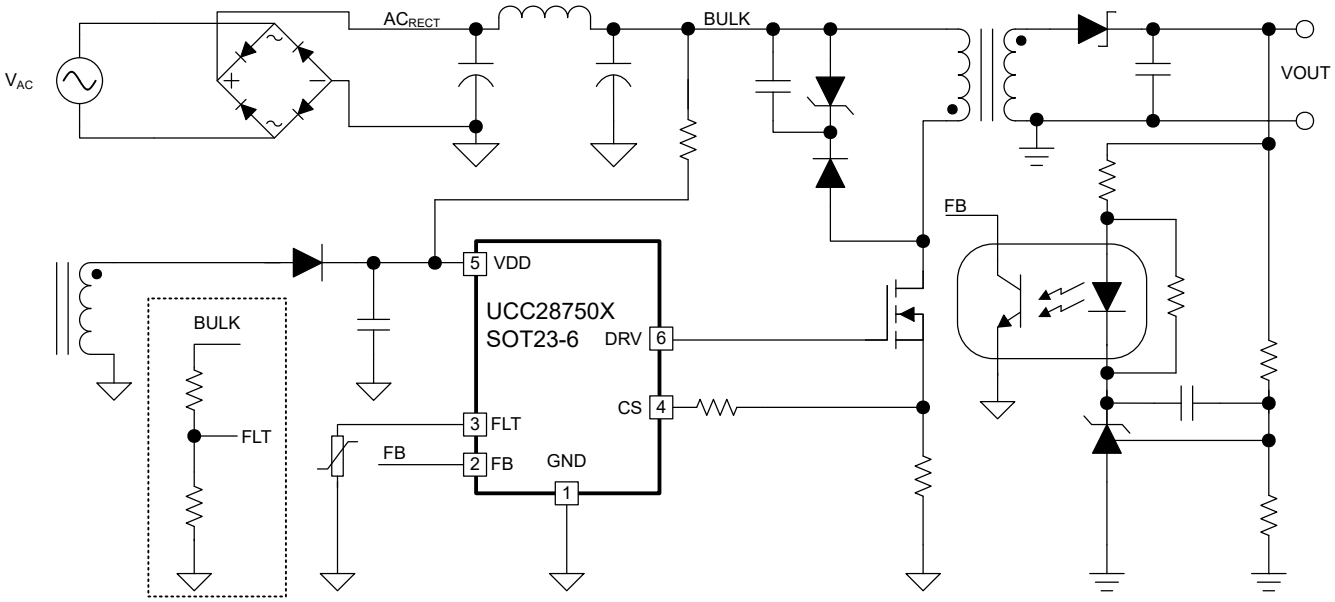

図 8-1. Typical Application Diagram

8.2.1 Application

The typical application of the UCC28750 is an off-line flyback power supply up to 70W. A trickle charge resistor network and an auxiliary winding provide the bias from startup to normal operation to the controller. The auxiliary winding provides information of the ouput voltage, which can be used for over-voltage protection. The FLT pin is programmed to provide over-temperature protection to an expected hotspot on the printed circuit board, such as the transformer.

8.2.2 Design Requirements

表 8-1. Design Parameters

PARAMETER	Conditions	MIN	TYP	MAX	UNIT
Input Requirements					
Input Line Voltage		90	120/240	265	V, AC
Minimum Bulk Voltage			90		V, DC
Input Line Frequency		47	50/60	63	Hz
Output Requirements					
Output Voltage	VIN = Min to max, Iout = No load to Full load		24		V
Output Current	VIN = Min to max	0		2.5	A
Output Voltage Ripple	Steady state		1		%
	Load transient 10% to 90% of maximum current		5		%
System Characteristics					
Switching Frequency	VIN = Min to max, Max output current		65		kHz
	VIN = Min to max, Min output current		25		kHz

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8.2.3 Detailed Design Procedure

8.2.3.1 Input Bulk Capacitance with Minimum Bulk Voltage

The bulk capacitance can consist of a set of one or more capacitors connected in parallel, often with some inductance between them to suppress differential mode noise. Input EMI filter design is outside the scope of this data sheet and is not discussed.

The mimimum bulk voltage valley, $V_{bulk,min}$, is dependent on the total input capacitance value used in the power stage design. The input capacitor is chosen to maintain an acceptable input voltage ripple. The ripple is largest at the minimum input line at the largest output power scenario. Therefore, the input bulk capacitance is based on the a wanted $V_{bulk,min}$ at the max power.

The input power can be estimated by taking the maximum output power and dividing the result by the estimated efficiency.

$$P_{\text{in}} = \frac{V_{\text{out}} \times I_{\text{out,max}}}{\eta} \tag{6}$$

$$C_{\text{bulk}} = \frac{2P_{\text{in}} \times \left(\frac{1}{4} + \frac{1}{2\,\pi} \arcsin\left(\frac{V_{\text{bulk,min}}}{\left(\sqrt{2}\text{VIN}_{\text{min}}\right)}\right)\right)}{\left(\sqrt{2}\text{VIN}_{\text{min}}\right)^2 - \left(V_{\text{bulk,min}}\right)^2} \tag{7}$$

Where

- $V_{bulk,min}$ is the minimum DC bulk voltage
- VIN_{min} is the minimum AC voltage applied to the flyback application

For this design, the result from taking the design requirements and the plugging in those values to 式 6 and 式 7, a recommended minimum of 110µF for the bulk input capacitance.

8.2.3.2 Transformer Turns Ratio and Inductance

The transformer design process starts with selecting a switching frequency and maximum duty cycle. With the UCC287502, the switching frequency is set to 65kHz for the max load operation. The maximum duty cycle can safely be chosen to be above 50% as the UCC28750 is a flexible controller capable of DCM and CCM operation while handling sub-harmonic oscillation with the internal slope compensation feature.

$$D_{\text{max,initial}} = 65\,\% \tag{8}$$

With the maximum duty cycle for the design set, the secondary to primary transformer turns ratio, N_S to N_P, can be chosen by using the boundary mode condition equations to simplify the design process. The turns ratio selection is an iterative process, and the primary switching MOSFET device maximim drain-to-source voltage must be accounted for when designing the transformer.

The turns ratio is initially chosen by using the minimum input voltage and the maximum duty cycle value. This scenario has the highest average current the transformer and switching device must handle, and is why in most of the equations use this worst case for determining the inductance and turns ratio of the transformer. Setting N_P to 1 turn, the secondary turns in the turns ratio is determined with 式 9

$$N_S = \frac{V_o \times \left(1 - D_{\text{max,initial}}\right)}{V_{\text{bulk,min}} \times D_{\text{max,initial}}} \tag{9}$$

The 650V drain-to-source (V_{DS}) rated MOSFET is a popular device used in flyback topologies, especially those with a universal input requirement (80V,AC to 265V,AC). The reflected voltage, the voltage seen by the transformer during the secondary conduction time, must be below the MOSFET V_{DS} rating, with additional margin for the leakage spike. The leakage spike is additional ringing that occurs in flyback designs due to the MOSFET output capacitance and transformer leakage inductance.

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$$V_{\text{margin}} = 0.8 \times V_{\text{DS}} \tag{10}$$

$$V_{\text{reflected}} = V_{\text{bulk,max}} + \frac{N_P}{N_S} \times V_o \tag{11}$$

$$V_{\text{reflected}} < V_{\text{margin}} \tag{12}$$

Combining 式 10, 式 11, 式 12, and solving for the turns ratio results in a constraint for the turns ratio:

$$\frac{N_P}{N_S} < \frac{V_{\text{margin}} - V_{\text{bulk,max}}}{V_o} \tag{13}$$

A turns ratio of 1:6 is chosen for this design concept. The duty cycle can be iterated on and a new maximum duty cycle, D_{max}, can be selected with the new turns ratio, and comes out to be around 65%, which is what the max was initially set to.

$$D_{\text{max}} = \frac{V_o}{\frac{N_S}{N_P} \times V_{\text{bulk,min}} + V_o} \tag{14}$$

With the selected turns ratio, maximum duty cycle, input range, and output power range, the magnetizing inductance value can be calculated using equation 式 15, and comes out to be approximately 480µH. The equation for the inductance is derived by using the boundary mode equations and equating the average input power equal to the average output power, with a factor for the efficiency.

$$L = \frac{V_{\text{bulk,min}}^2 \times D_{\text{max}}^2 \times T_{\text{sw}} \times \eta}{2 \times P_{\text{out,max}} \times K_{\text{ccm}}} \tag{15}$$

Where

- η as the assumed efficiency of the flyback
- T_{sw} as the normal operation switching period
  - In this case 15µs , as the device variant for this application design is a 65kHz variant
- K_{ccm} is factor from 0.1 to 1 that determines the percentage of output max output power at the boundary condition that the flyback enters into the CCM state

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8.2.3.3 Current Sense and Slope Compensation Network

The CS pin consists of a network of current sensing resistors and the slope compensation components. For designs with a maximum duty cycle less than 50%, the slope compensation network is not necessary, and thus the current sensing resistor is a calculation based on just the maximum peak current and the maximum threshold on the CS pin. The current sensing resistors connected from the source of the MOSFET to the ground control the maximum peak current of the power stage. The CS pin maximum threshold is 900mV, and a small margin is used to have a more robust design.

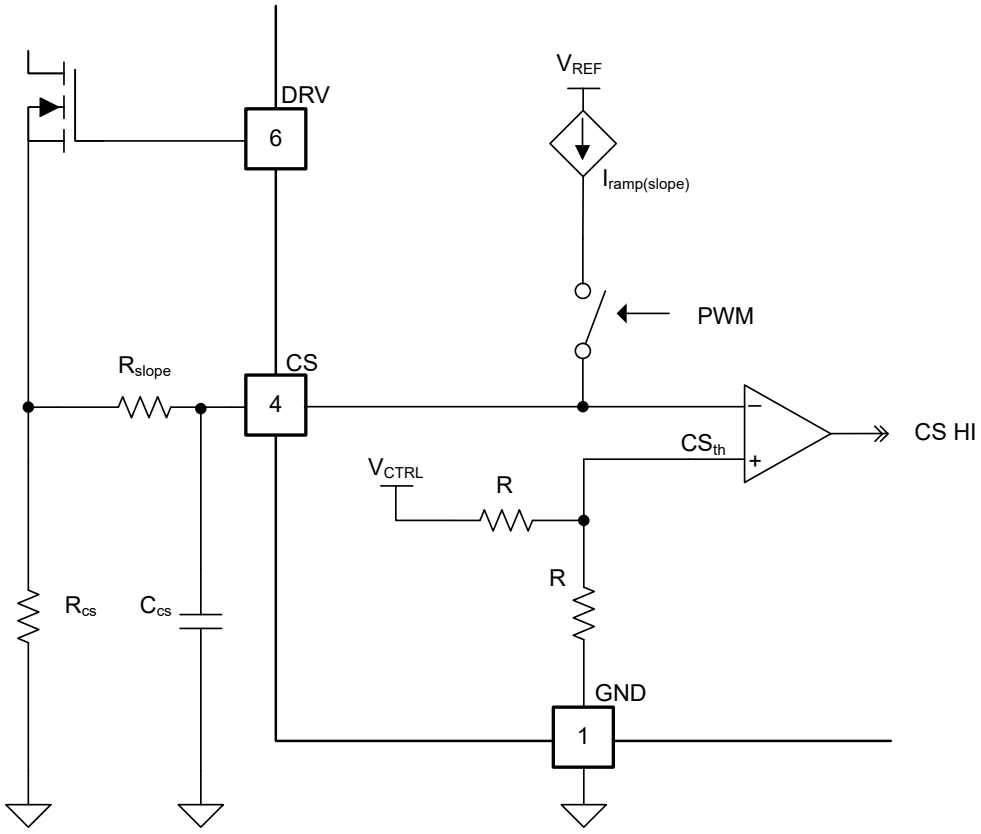

図 8-2. CS Pin Diagram

$$R_{CS} = \frac{0.8 \times V_{CS,max}}{i_{pk}} \quad (16)$$

Because UCC28750 can operate in CCM and DCM, the boundary mode equation for i_{pk} is used as a starting point for selecting the current sense resistor value, with R_{CS} initially selected with a nominal value of 420mΩ.

$$I_{\text{pk}} = \frac{V_{\text{bulk,min}} \times D_{\text{max}} \times T_{\text{sw}}}{L} \tag{17}$$

In a design with the duty cycle greater than 50% slope compensation must be used to avoid sub-harmonic isolation. UCC28750 has an internal ramp that helps remedy this issue. A resistor is added between the CS pin and the current sense resistor which programs the amount value of the ramp. In a peak-current current scheme, adding a ramp that is equal to half of the slope of the flyback transformer during the off-time of the switching device removes instability. The slope, S_{off}, with units Amps per second, and reflected to the primary side, during the off time of the primary switching MOSFET is shown in 式 18.

$$S_{\text{off}} = \frac{V_o \frac{N_P}{N_S}}{L} \tag{18}$$

UCC28750 has a current source that ramps to 100µA at the device's maximum duty cycle of 80%. Therefore the ramp amplitude is a ratio of the max level and the calculated duty cycle of the design. The term i_{slope} has units of Amps per second, just like S_{off}.

$$i_{\text{slope}} = \frac{i_{\text{ramp}}}{D_{\text{max}} \times T_{\text{sw}}} \tag{19}$$

Where i_{ramp} is the 100µA amplitude of the slope compensation current during the fixed frequency (65/100 kHz) region in the control law.

The value of the R_{slope} resistor is half of the S_{off} value divided by the i_{slope}.

$$R_{\text{slope}} = \frac{\frac{1}{2} \times S_{\text{off}}}{i_{\text{slope}}} \tag{20}$$

With a slope compensation resistor in place, the CS pin voltage needs to be re-evaluated to make sure that full power delivery is still possible at the minimum input voltage and highest load. The ramp that is generated from R_{slope} causes the CS pin threshold to be reached earlier than expected, if the R_{CS} stays the same as calculated from 式 16.

$$V_{\text{CS,with slope comp}} = R_{\text{slope}} \times \left(i_{\text{slope}} \times D_{\text{max}} \times T_{\text{sw}}\right) + R_{\text{CS}} \times I_{\text{pk}} \tag{21}$$

$$V_{\text{CS,with slope comp}} < 0.8 \times V_{\text{CS,max}} \tag{22}$$

$V_{CS,with\ slope\ comp}$, the addition of the peak current, represented as a voltage, and the ramp from the slope compensation current source, can go above the threshold set in 式 22. The slope compensation resistor is changed to be lowered, rather than the current sense changing to accommodate the value from 式 20, as adding too much of a ramp can change the control mode from peak-current mode control to effectively voltage mode control.

式 21 is modified to solve for R_{slope} with R_{CS} locked from the initial value of 420mΩ, the new R_{slope} is 1kΩ.

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8.2.3.4 Output Capacitors

The output capacitor value is determined by two factors in a power supply design: steady state ripple voltage and the output transient voltage response. The capacitor values for the transient response are typically specified as a load step from no load to full load of the power supply design.

$$C_{\text{out}} = \frac{I_{\text{step}} \times t_{\text{response}}}{\Delta V_{\text{out}}} \tag{23}$$

Where

- I_{step} is the largest step in load current
- $t_{response}$ is the approximate response time
- ΔV_{out} is the allowable output voltage change

$$t_{\text{response}} = \frac{0.33}{f_c} + T_{\text{sw}} \tag{24}$$

Where

- f_c is the approximate crossover frequency, typically set to one-tenth the switching frequency
- T_{sw} is the switching period expected at the initial load condition before the load step

The ripple voltage in steady state has two major contributors: the change in the output voltage due to the charge and discharge of the output capacitors in every switching cycle, and the step in the output voltage due to the equivalent series resistor of the capacitors. An additional margin is placed on the ESR calculation to account for variance and aging of the

$$\text{ESR} \leq \frac{V_{\text{ripple}}}{i_{\text{pk,max}} \times N_{\text{PS}}} \times 50\,\% \tag{25}$$

$$C_{\text{ripple}} = \frac{I_{\text{out,max}} \times D_{\text{max}}}{V_{\text{ripple}} \times f_{\text{sw}}} \tag{26}$$

Where

- V_{ripple} is the allowable voltage ripple for a design
- N_{PS} is the primary to secondary turns ratio
- $I_{out,max}$ is the maximum output load current
- $i_{pk,\ max}$ is the primary side maximum peak current of the transformer

The final output capacitor value is the larger of the C_{out} and C_{ripple} values. The estimated crossover frequency largely determines the value of capacitance to use. For example, a crossover frequency of 2.5kHz suggests to use 900µF, while a 6.5kHz crossover is much lower capacitance, about 350µF. Use multiple capacitors to lower the equivalent ESR and get the actual capacitance close to the nameplate capacitance. Multiple capacitors increase robustness by accounting for DC derating and temperature rating fluctuations in the capacitance value.

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8.2.3.5 VDD Capacitance, C_{VDD}

The capacitance on VDD needs to supply the device operating current until the output of the converter reaches the target minimum operating voltage. At this time the auxiliary winding can sustain the voltage to the UCC28750. The input VDD capacitance is determind by the on current of the controller and the output voltage rise time of the application. The VDD capacitor must be able to keep the VDD pin voltage above 9V, $V_{uvlo(off)}$, until the output voltage reflected to the auxiliary can take over as the primary bias to the controller.

The soft start feature in UCC28750 does not ramp to full power deliver in the first steps, therefore a conservative 2ms addition is placed into 式 27 to help size the input capacitors.

A split diode and capacitor network can be used in flyback designs to lower the initial startup time, but still have a path for a bulk capacitance on the device's input put, as shown セクション 7.3.1 and reproduced here for ease of use.

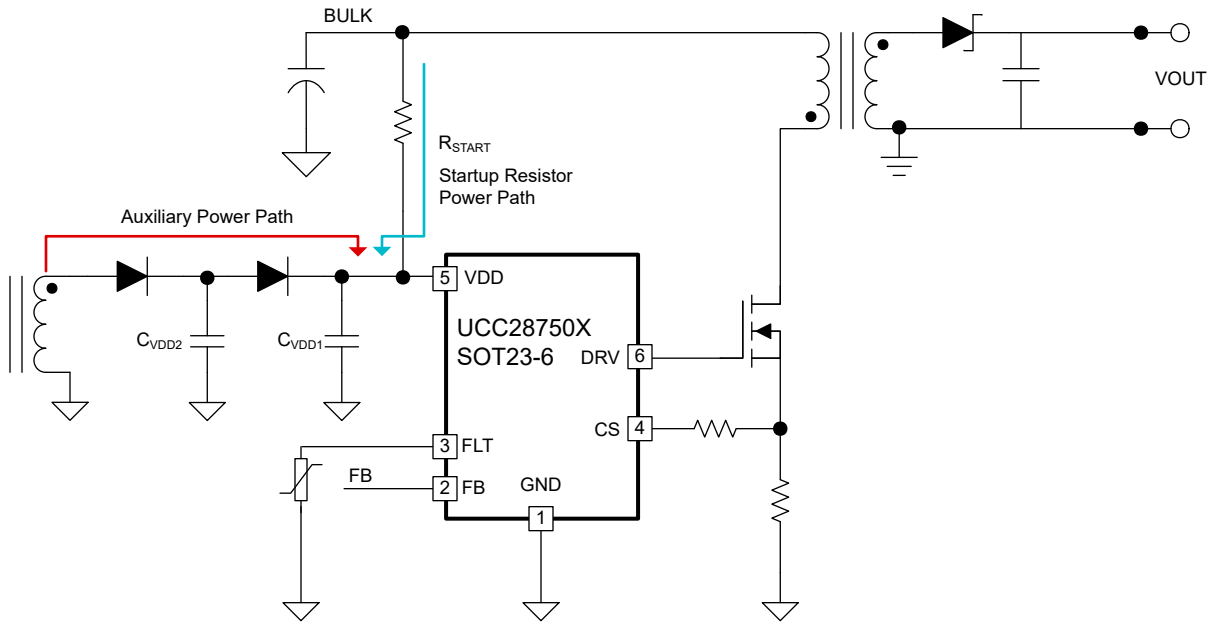

図 8-3. Split Diode Biasing Scheme for Use With Startup Resistors

The first capacitor, C_{VDD1}, is determined by the startup resistor value and the desired turn-on time. The startup resistor values are constrained by power loss and fault requirements as mentioned in セクション 7.5.4.

For a design with a typical one second start time, and a startup resistor network with an sum resistance of 1.2MΩ after adding in additional margin. The resulting C_{VDD1} value is approximatly 6µF. The nearest standard value is 6.8µF.

C_{VDD2} is largely determined by the output voltage rise time and the feedback loop estimates. Those parameters can cause an small overshoot during startup, especially at no load applications. When an overshoot occurs the device can stop switching if the feedback loop pulls down on the FB pin voltage enough to push the control law into the off state ("F" region in 図 7-9).

The output voltage rise time is derived from the assumed power available to charge the capacitor from zero volts to the programmed output voltage. The "2ms" term added in 式 27 is to account for the fact that the device's soft start does not output full power in the first two milliseconds which, if not added to the equation, which can understate the rise time of the output voltage.

$$t_{vo,rise} = \frac{1}{2}\frac{C_{out} \times V_{out}^2}{P_{out,max}} + 2\ ms \quad (27)$$

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Typically, the crossover frequency is initially placed at one-tenth the switching frequency of the power stage. That estimate can be used to determine the initial value of C_{VDD2}. Through experiementation and measurement, the actual crossover frequency can be determined. Using the response time estimate equation from セクション 8.2.3.4, 式 24, the overshoot of the output can be determined by modifying 式 27 for V_{out} and adding the $t_{response}$ estimate into the time term. The overshoot value can then be used to determine the amount of time required for that overshoot to decay back to steady state.

$$V_{\text{out,overshoot}} = \sqrt{\frac{2 \times \left(t_{\text{vo,rise}} - 2\ \text{ms}\ + t_{\text{response}}\right)}{C_{\text{out}}}} - V_{\text{out}} \tag{28}$$

$$t_{\text{decay}} = \frac{C_{\text{out}} \times V_{\text{out,overshoot}}}{I_{\text{load}}} \tag{29}$$

式 29 is dependent on the output load. When the output load is near zero, the decay time becomes long and therefore C_{VDD2} must be large to survive the decay time. Experimentation and testing must be performed to determine if a "dummy load," a resistor put at the output, is required to lower the decay time if the feedback loop causes too large of an overshoot.

The time for the overshoot to reach down to steady state regulation levels uses the fundamental capacitor equation.

$$C_{\text{VDD2}} = \frac{I_{\text{off}} \times t_{\text{decay}}}{V_{\text{UVLO,on}} - \left(V_{\text{UVLO,off}} + 1\ \text{V}\right)} \tag{30}$$

Where

- I_{off} is the UCC28750 off-state current, typically 350µA

With the large range of t_{decay} from the sum of $t_{vo,rise}$ and $t_{response}$ to the worse case of a one second decay time, C_{VDD2} can range from 15µF to 70µF.

8.2.4 Application Performance Plots

The figures below are a result of testing and experimentation of the universal input, 60 W output, UCC28750 Evaluation Module. In the waveforms showcasing the switching node (the drain of the switching device) in セクション 8.2.4.3, Q1 refers to the switching device in a flyback application.

8.2.4.1 Startup

CH1 =V_{BULK} , CH2 = V_{CC}, CH3 = V_{GATE}, CH4 = V_{OUT}

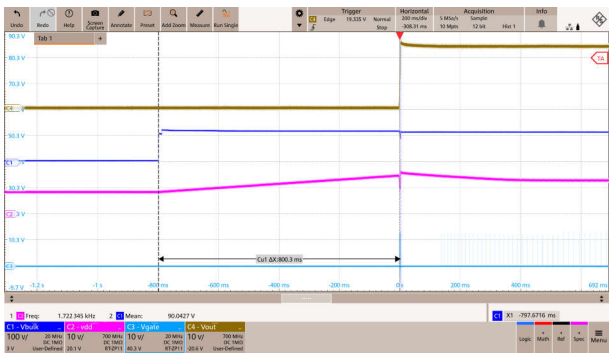

図 8-4. Start-Up Waveforms at 85Vac and No Load

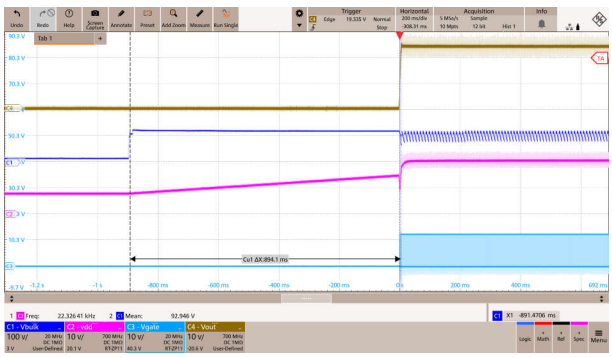

図 8-5. Start-Up Waveforms at 85Vac and Full Load

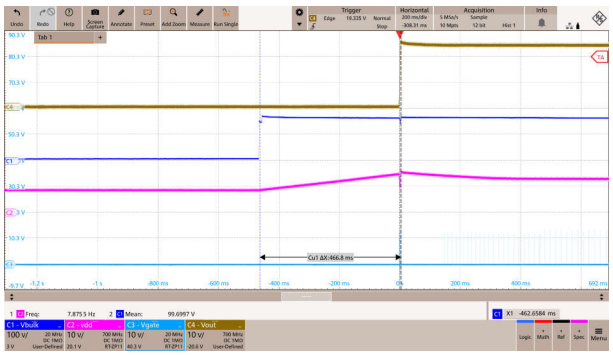

図 8-6. Start-Up Waveforms at 115Vac and No Load

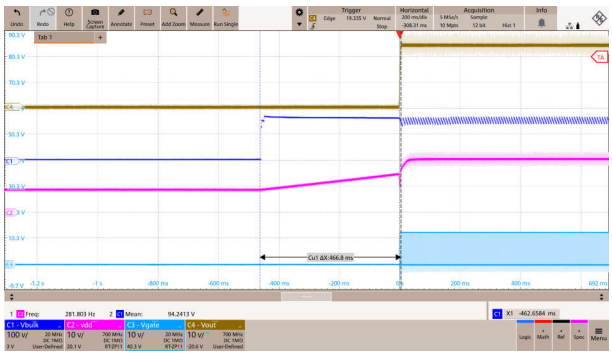

図 8-7. Start-Up Waveforms at 115Vac and Full Load

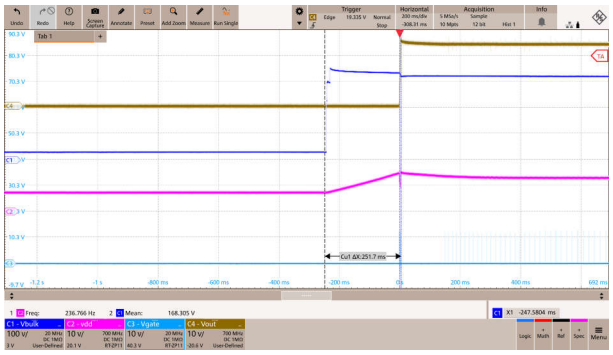

図 8-8. Start-Up Waveforms at 230Vac and No Load

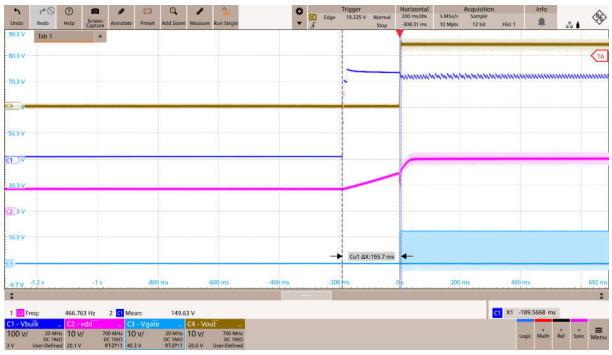

図 8-9. Start-Up Waveforms at 230Vac and Full Load

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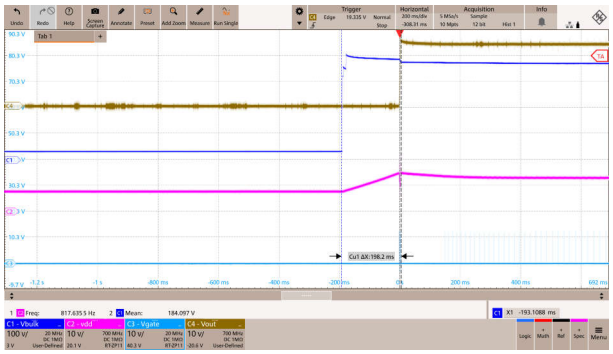

図 8-10. Start-Up Waveforms at 265Vac and No Load

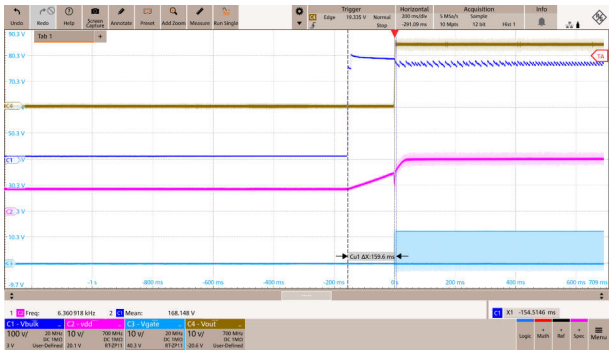

図 8-11. Start-Up Waveforms at 265Vac and Full Load

8.2.4.2 Load Transients

CH1 = V_{OUT}, CH4 = I_{OUT}

Load = 0.100A to 2 .5A, 1kHz, 50% Duty Cycle

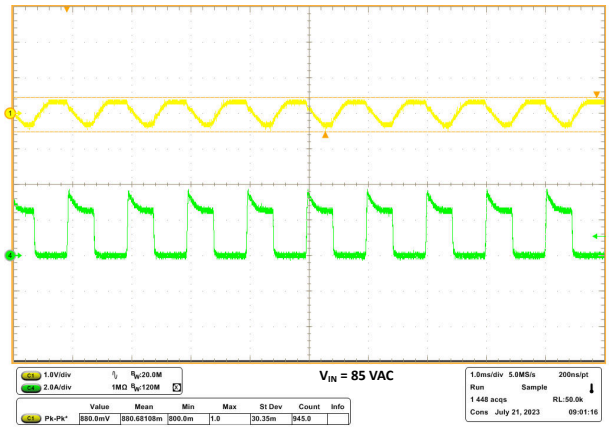

図 8-12. Load Transients at 85Vac

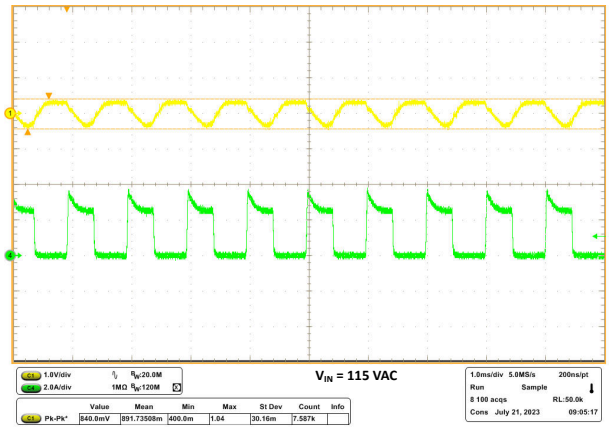

図 8-13. Load Transients at 115Vac

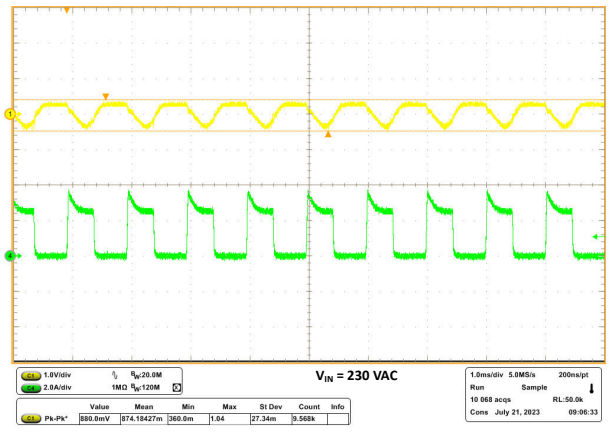

図 8-14. Load Transients at 230Vac

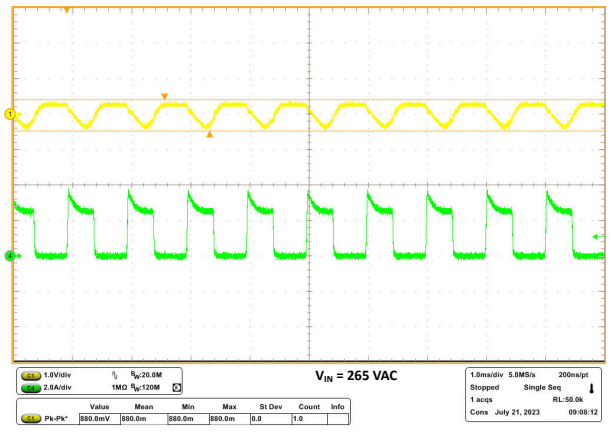

図 8-15. Load Transients at 265Vac

8.2.4.3 Q1 Drain Voltage Evaluation

CH1=V_{Q1d}, CH3 = V_{GATE}, CH4 = V_{OUT}

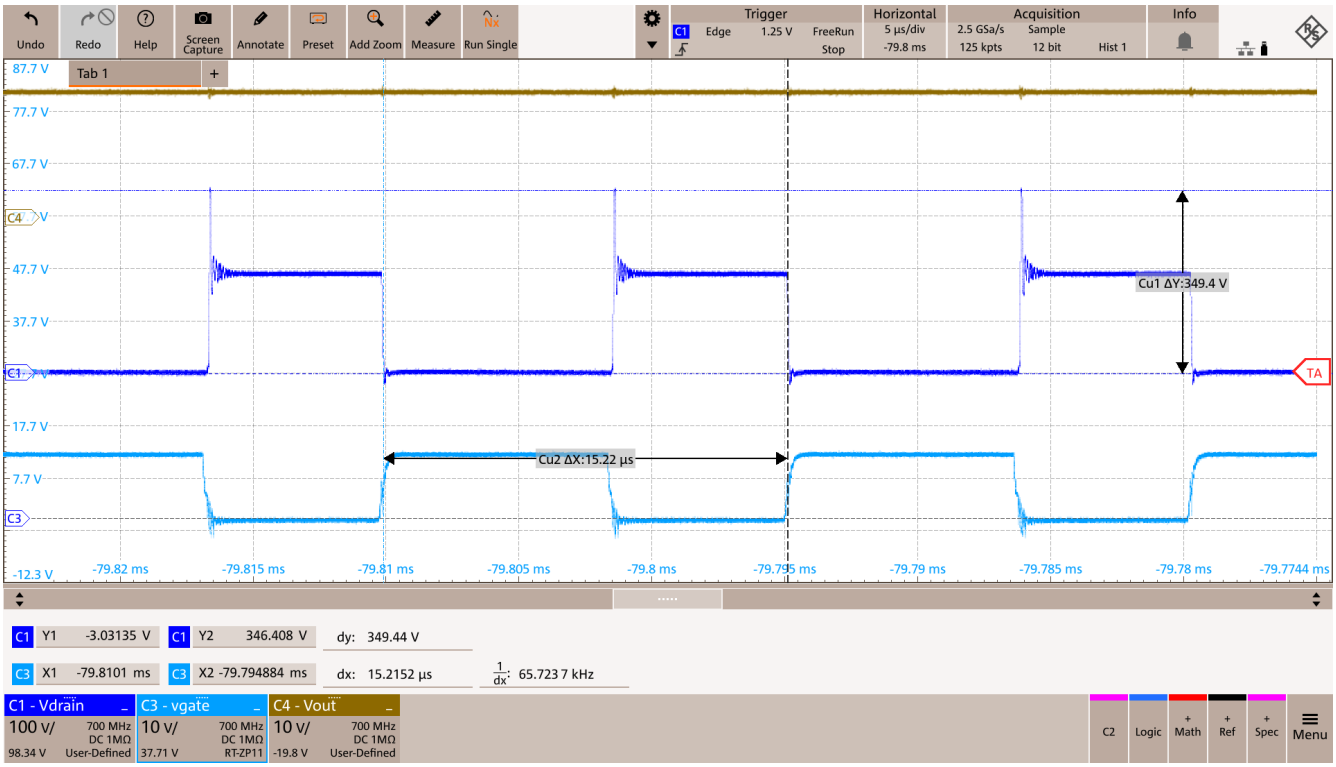

図 8-16. Steady State Waveform at 85Vac

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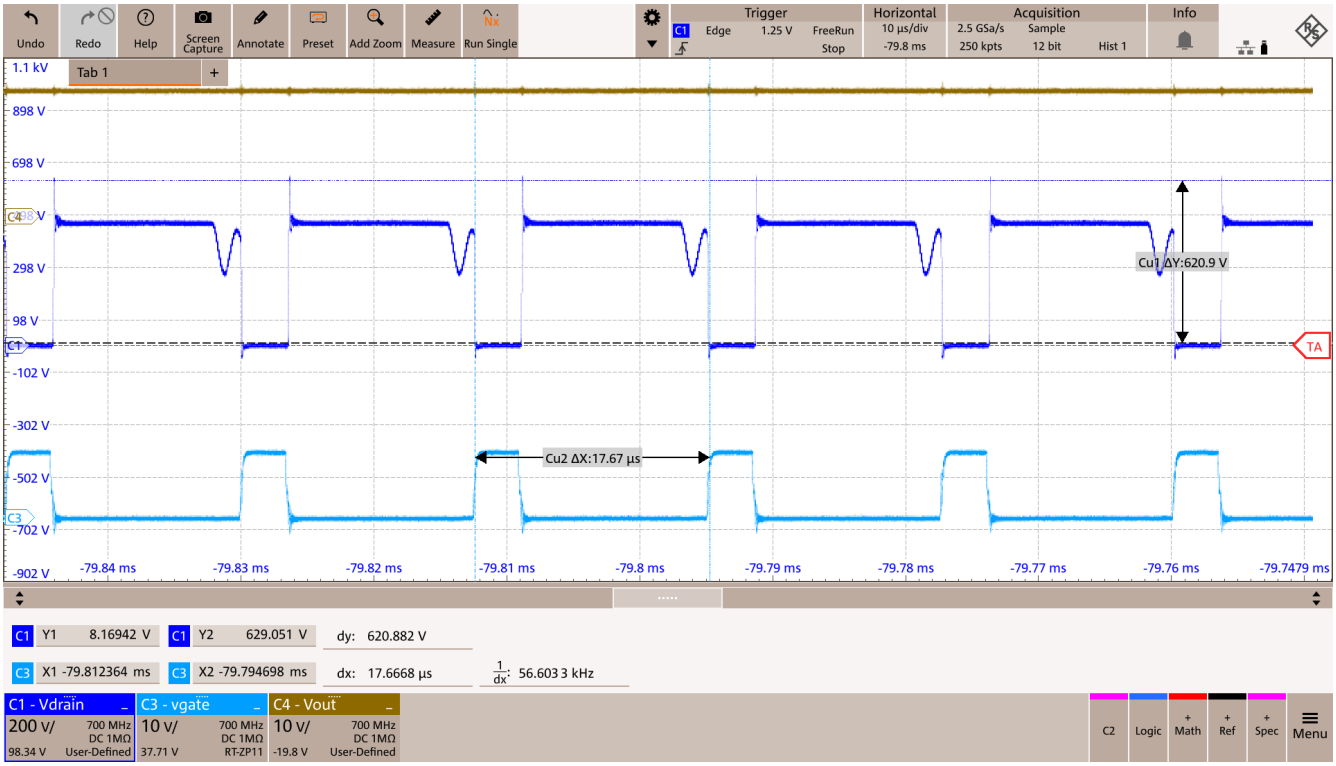

図 8-17. Steady State Waveform at 85Vac

8.2.5 What to Do and What Not to Do

Do

- Use multiple resistors for the high voltage startup resistor network
- Limit the current into the FLT pin, as the pin can only handle 5mA
- Use multiple resistors for the current sensing resistor if designing for higher power designs (such as 60W)
- Use high frequency bypass capacitors close to the transformer in addition to the bulk capacitors
- Place the slope compensation resistor close to the UCC28750 device, not the current sensing resistor
- Use an additional current sensing filter capacitor to aid the leading edge blanking with noise filtering
- Place a resistor in series with the DRV pin to the gate of the MOSFET to tune the turn-on and turn-off rate of the MOSFET
  - To increase turn off speed, use a separate diode and resistor path for the turn-off edge to have a faster turn-off edge and a slower turn-on edge

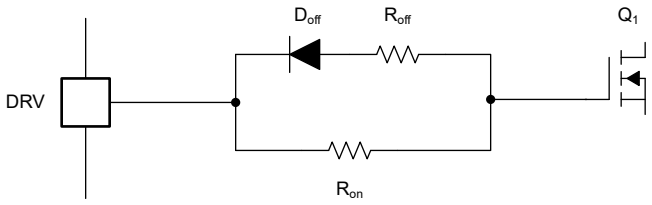

図 8-18. DRV gate drive resistor network setup

Do not

- Use small traces for the power path, use large traces, greater than 40mil (1mm)
  - A trace can carry about 0.5A to 1A per 10mil (0.254mm) trace thickness
- Put high voltage traces next to low voltage traces, use a high voltage spacing rule and set a restriction in layout

- Arbitrarily place grounding points, have a particular power path ground loop and a separate signal ground loop, tied together near the power stage input bulk capacitor

8.3 Power Supply Recommendations

The UCC28750 is intended for AC-to-DC adapters and chargers with universal input voltage range of 85 VRMS to 265VRMS, 47Hz to 63Hz, using flyback topology. The UCC28750 can also be used in other applications and converter topologies with different input voltages. In any case, be sure that all voltages and currents are within the recommended operating conditions and absolute maximum ratings of the device.

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8.4 Layout

8.4.1 Layout Guidelines

To increase the reliability and feasability of the project adhere to the following guidelines on PCB layout with the UCC28750. These guidelines are general rules that can be followed for any power supply topology and are generally topology-agnostic. The main theme in power supply layouts is to keep the power loops and signal loops as small as possible to avoid coupling of strong signals from one to another and to lower losses caused by additional parasitics that arise from poor layout.

In a flyback topology, especially the primary which this guidelines are for, there are several loops to pay attention to and minimize:

- The primary power loop that delivers power to the output
- The snubber loop that absorbs the ringing due to leakage inductances
- The gate drive loop from the device to the gate of the switching device and back to the return
- The auxiliary power loop that rectifies the auxiliary voltage to a steady bias voltage for the UCC28750
- The feedback loop which carries low-current, sensitive information regarding regulation

The startup resistor path is not critical, as once startup is complete the path does not deliver significant power or information. The auxiliary winding takes over as the bias for the UCC28750 instead and is the higher priority power path for the device.

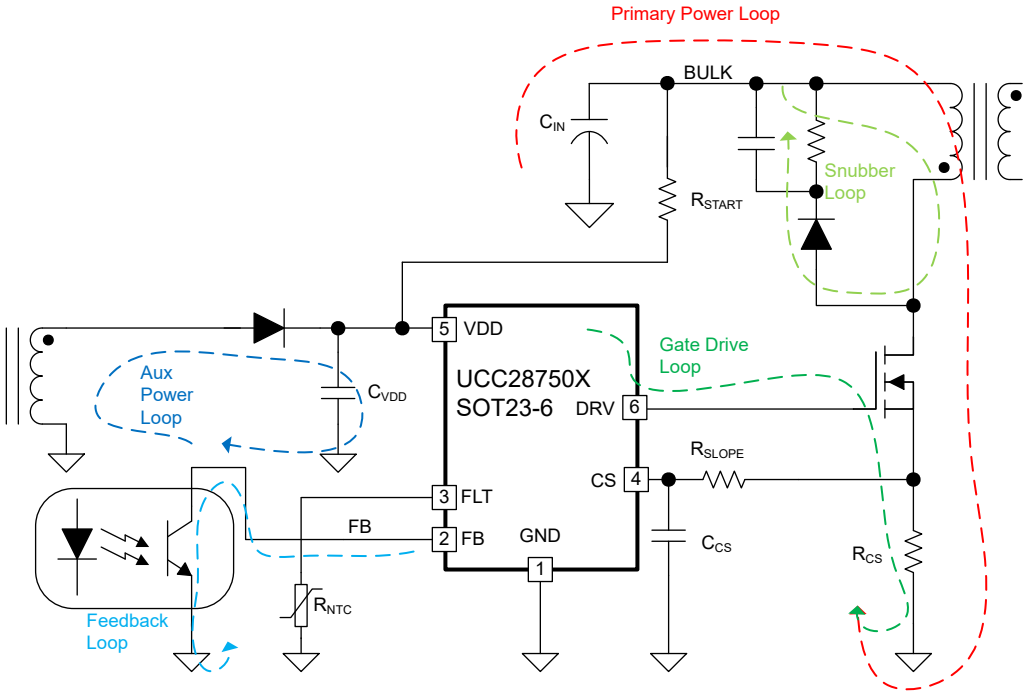

図 8-19. Simplified Primary Side Schematic Layout Guidelines

8.4.2 Layout Example

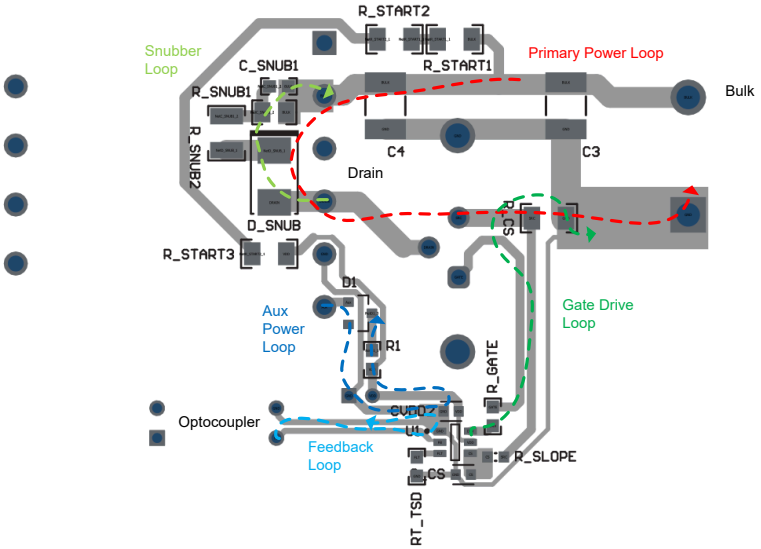

図 8-20. Bottom Layout of the Guidelines Schematic

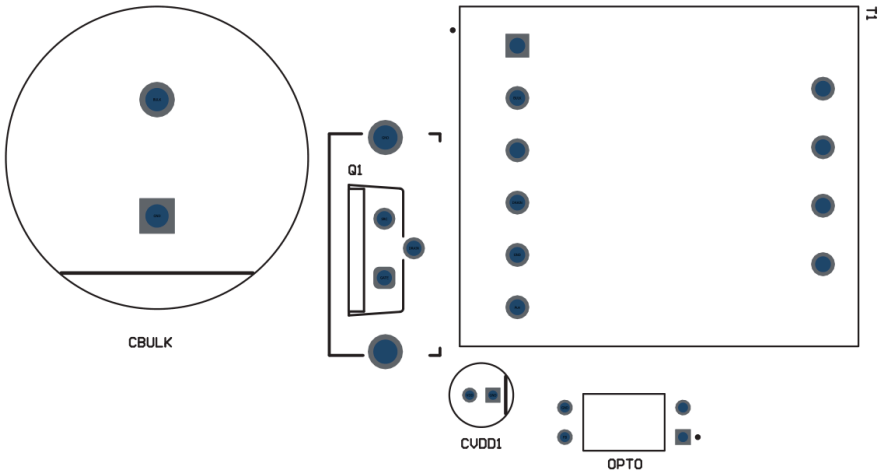

図 8-21. Top Layout of the Guidelines Schematic, No Traces

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9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.3 サポート・リソース

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9.5 静電気放電に関する注意事項

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.6 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
December 2023	*	Initial release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC287501DBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	U501
UCC287501DBVR.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	U501
UCC287502DBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	U502
UCC287502DBVR.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	U502
UCC287503DBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	U503
UCC287503DBVR.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	U503
UCC287504DBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	U504
UCC287504DBVR.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	U504
UCC287505DBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	U505
UCC287505DBVR.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	U505
UCC287506DBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	U506
UCC287506DBVR.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	U506
UCC287507DBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	U507
UCC287507DBVR.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	U507
UCC287508DBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	U508
UCC287508DBVR.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	U508

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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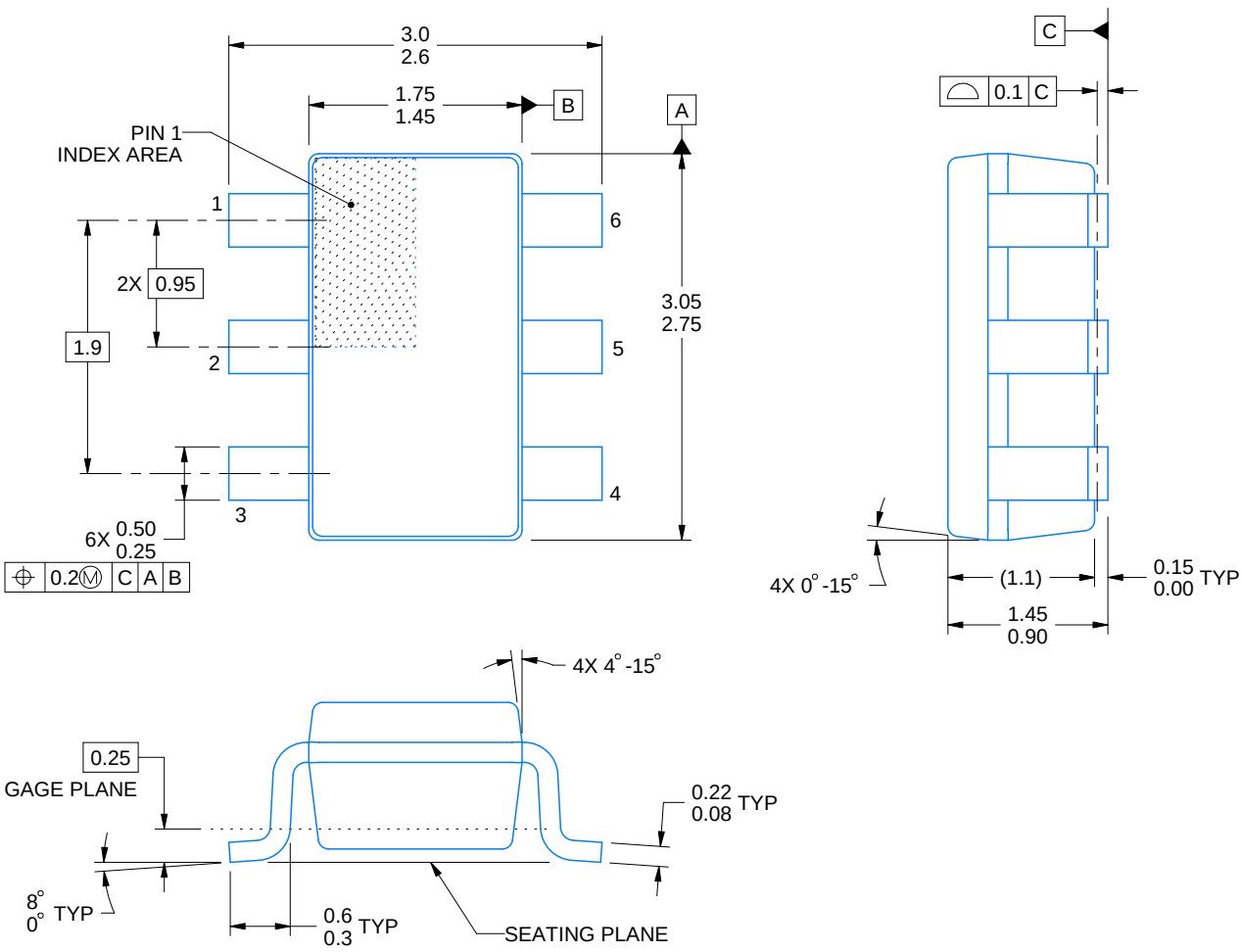
PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

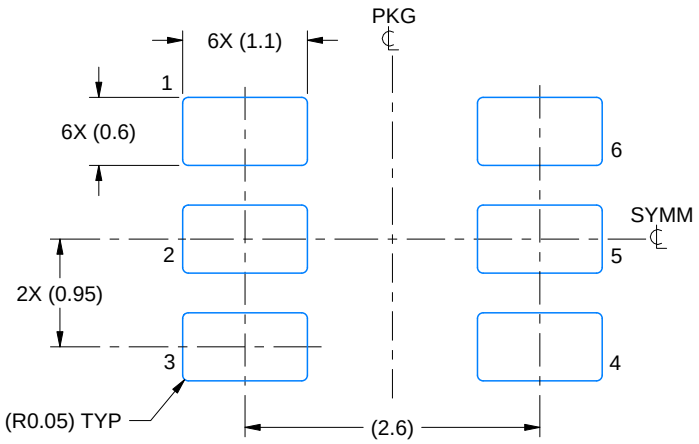
SMALL OUTLINE TRANSISTOR



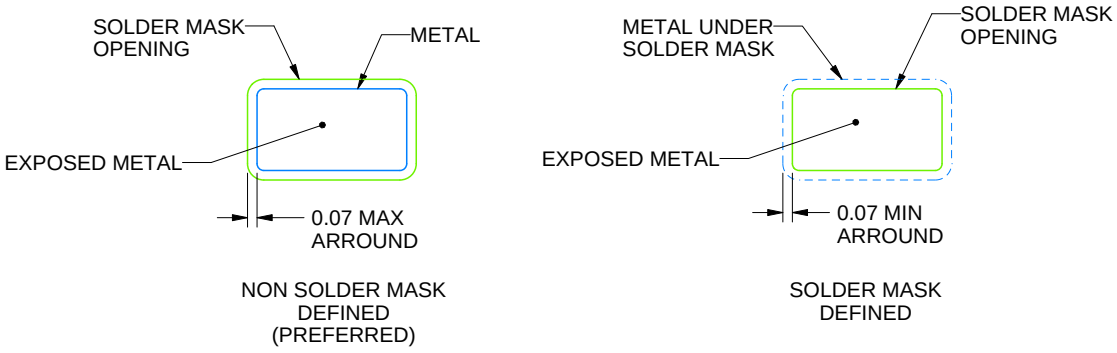
4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

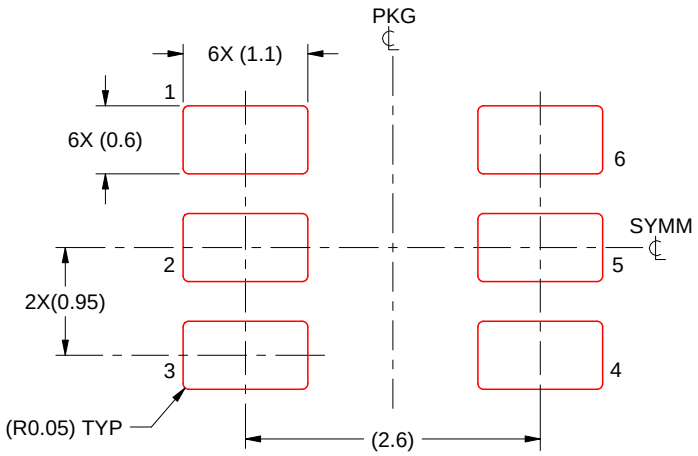


SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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