TEXAS INSTRUMENTS
UCC28780
JAJSE40A – OCTOBER 2017 – REVISED FEBRUARY 2018

UCC28780 高周波数アクティブ・クランプ・フライバック・コントローラ

1 特長

- 適応型制御による、プライマリFETの完全および部分的なゼロ電圧スイッチング(ZVS)
- 外部のSiまたはGaN FETのタイミングをプログラム可能
- 最高1MHzの高いスイッチング周波数
- プログラム可能な適応型バースト制御およびスタンバイ・モードにより、軽負荷時の高効率、低い出力リップル、可聴帯域ノイズの低減を実現
- 直接ライン・センシングなしにブラウンアウトを検出
- 正確にプログラム可能な過電力保護(OPP)によりピーク電力モードをサポート
- フォルト保護機能: 過熱、出力過電圧、出力短絡、過電流、ピン・フォルト
- オプトカプラ・ベースの帰還を持つ直接インターフェイスにより、出力電圧を動的にスケーリング可能
- 内部的なソフトスタート
- NTCサーミスタ・インターフェイスと外部イネーブル

2 アプリケーション

- ノートPC、タブレット、TV、セットトップ・ボックス、プリンタ用の高密度のAC/DCアダプタ
- USB Power Delivery、直接および高速モバイル充電器
- AC/DCまたはDC/AC補助電源

3 概要

UCC28780は高周波数のアクティブ・クランプ・フライバック・コントローラで、DoE Level VIやEU CoC V5 Tier-2などの厳格な効率性の国際規格に準拠する、高密度のAC/DC電源を可能にします。ユーザーが高度な制御規則をプログラム可能なため、シリコン(Si)および窒化ガリウム(GnN)の両方のパワーFETについて、性能を最適化できます。ロジック・レベルのゲート信号およびイネーブル出力により、ドライバとGaN FETを組み合わせたスイッチング・デバイスとの直接動作がさらに強化されます。

高度な自動チューニング技法、適応型デッドタイム最適化、可変スイッチング周波数制御規則により、広い動作範囲にわたってゼロ電圧スイッチング(ZVS)が達成されます。適応型マルチモード制御を使用して、入力と出力の条件に応じて動作を変更することにより、UCC28780は高い効率を実現し、同時に可聴帯域のノイズを低減できます。スイッチング周波数は最高1MHzまで変更でき、過電力保護を正確にプログラム可能なため、広いライン範囲にわたって熱設計用に一貫した電力が得られ、パッシブ部品のサイズをさらに削減でき、高い電力密度が可能になります。

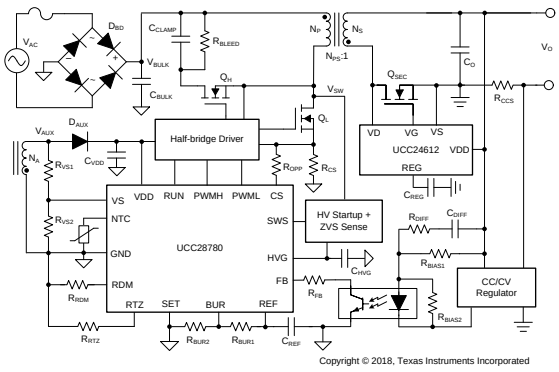
UCC28780は、UCC24612などのVDSセンシング同期整流コントローラとともに動作し、非常に小型で高い変換効率の設計を実現できます。

製品情報(1)

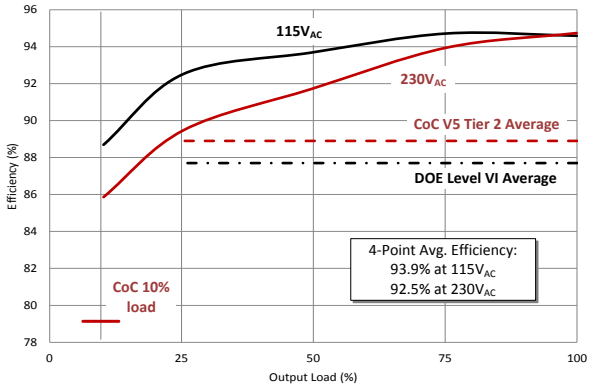
発注型番	パッケージ	本体サイズ(公称)
UCC28780RTE	WQFN-16	3.00mm×3.00mm
UCC28780D	SOIC-16	10.33mm×7.50mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

概略回路図



45W、20VのGaN-ACFアダプタの効率



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4 改訂履歴

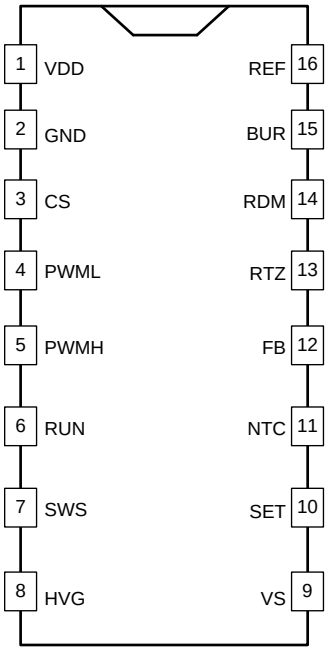
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

日付	改訂内容	注
2018年2月	A	初版

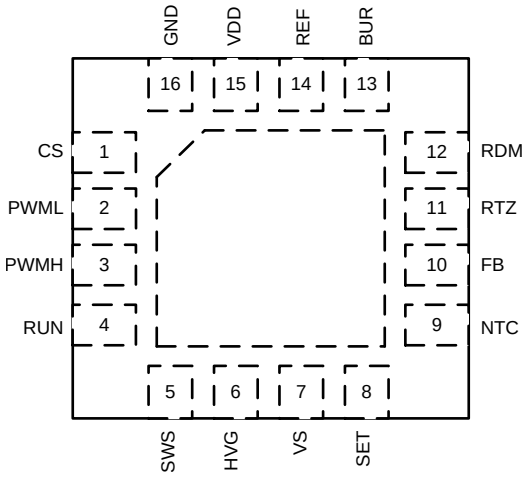
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5 Pin Configuration and Functions

D Package
16-Pin SOIC
Top View



RTE Package
16-Pin WQFN
Top View



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Pin Functions

PIN			TYPE(1)	DESCRIPTION
NAME	SOIC	WQFN		
BUR	15	13	I	This pin is used to program the burst level of the converter at light load. A resistive divider between REF and GND is used to set a voltage at this pin to determine the peak current level when the converter enters the adaptive burst mode. In addition, the Thevenin resistance on BUR pin (equivalent resistance of the divider resistors in parallel) is used to set an offset voltage for smooth mode transition which increases the peak current level when the converter enters the low power mode.
CS	3	1	I	This is the current sense input pin. This pin couples through a line-compensation resistor to a current-sense resistor to sense and control the peak primary current in each switching cycle. A current sourced from this pin, which magnitude is proportional to the converter's input voltage derived from the VS-pin input signal, creates an offset voltage across the line-compensation resistor to program an OPP level at high line.
FB	12	10	I	The feedback current signal to close the converter's regulation loop is coupled to this pin. This pin presents a 4-V output that is designed to have 0-µA to 75-µA current pulled out of the pin corresponding to the converter operating from full-power to zero-power conditions.
GND	2	16	G	Ground reference and return for all controller signals.
HVG	8	6	O	The high-voltage gate pin is used to control the gate of an external depletion-mode MOSFET for start-up and switch-node voltage sensing. A 2.2-nF ceramic bypass capacitor to ground is required.
NTC	11	9	I	This is an interface to an external NTC (negative temperature coefficient) thermistor for remote temperature sensing. Pulling this pin low shuts down PWM action and initiates a fault response.
PWMH	5	3	O	The PWMH pin is a logic-level output signal used to control the gate of the high-side clamp switch through an external gate driver.
PWML	4	2	O	The PWML pin is a logic-level output signal used to control the gate of the low-side primary switch through an external gate driver.
RDM	14	12	I	A resistor to ground on this pin programs a synthesized demagnetization time used to control the on-time of the high-side switch to achieve zero voltage switching on the low-side switch. The controller applies a voltage on this pin that varies with the output voltage derived from the VS pin signal.
REF	16	14	O	5V reference output that requires a 0.1-µF ceramic bypass capacitor to ground. This reference is used to power internal circuits and can supply a limited external load current.
RTZ	13	11	I	A resistor to ground on this pin programs an adaptive transition-to-zero delay from the turn-off edge of the high-side clamp switch to the turn-on edge of the low-side switch.
RUN	6	4	O	This output pin is high when the controller is in a run state. During start-up and wait states this output is low. It can be used to enable and disable the external gate drivers to reduce the static power consumption. There is a preset delay, $t_{D(RUN-PWML)}$, of about 2.2 µs that delays the initiation of PWML switching after this pin has gone high.
SET	10	8	I	This pin is used to configure the controller to be optimized for Gallium Nitride (GaN) power FETs or silicon (Si) power FETs on the primary side. Depending on setting, it will optimize parameters of the ZVS control loop, dead-time adjustment, and protection features. When pulled high to REF pin, it is optimized for Si FETs. When pulled low to GND, it is optimized for GaN FETs .
SWS	7	5	I	This sensing input is used to monitor the switch-node voltage as it nears zero volts in normal operation. During start-up, this pin is connected to the VDD pin internally to allow the high-voltage sensing network to provide start-up current.
VDD	1	15	P	Bias power input to the controller. A hold-up capacitor to ground is required for the bias power supplied from the transformer auxiliary winding to this pin.
VS	9	7	I	This voltage sensing input pin is coupled to the auxiliary winding of the converter's transformer via a resistor divider. The pin and the associated external resistors are used to monitor the output and input voltages of the converter.

(1) I = Input, O = Output, P = Power, G = Ground

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input Voltage	VDD		38	V
	SWS	–6	38	
	VDD-SWS (Run state)	-20	38	
	CS	–0.3	3.6	
	NTC	–0.3	7	
	FB	–0.3	7	
	VS (Continuous)	–0.75	7	
	VS (Transient, 100ns Max.)	–1	7	
	RTZ	–0.3	7	
	BUR	–0.3	7	
	SET	–0.3	7	
	RDM	–0.3	7	
Output Voltage	REF	–0.3	7	V
	HVG	–0.3	25	
	PWML, PWMH, RUN	–0.3	7	
Source Current	REF		5	mA
	HVG		Self-limiting	
	VS (Continuous)		2	
	VS (Transient, 100ns Max.)		2.5	
	FB		1	
	PWML, PWMH, RUN		1	
	RTZ		Self-limiting	
	RDM		Self-limiting	
Sink Current	PWML, PWMH, RUN		1	mA
	SWS		5	mA
Operating junction temperature, T_J		–55	150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{VDD}	Bias-supply operating voltage	12		34	V
C_{VDD}	VDD capacitor	0.3			µF
C_{REF}	REF bypass capacitor	0.1			µF
C_{HVG}	HVG bypass capacitor	2.2			nF
T_J	Operating Junction temperature	-40		125	°C

6.4 Thermal Information of SOIC

THERMAL METRIC(1)		D	UNIT
		SOIC	
		16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	83.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	42.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Thermal Information of WQFN

THERMAL METRIC(1)		RTE + PAD	UNIT
		WQFN	
		16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.6 Electrical Characteristics

Over operating free-air temperature range, V_{VDD} = 15V, R_{RDM} = 115 kΩ, R_{RTZ} = 140 kΩ, V_{BUR}= 1.2 V, V_{SET} = 0 V, R_{NTC} = 50 kΩ, V_{VS} = 4 V, V_{SWS} = 0 V, I_{FB} = 0 μA, I_{HVG} = 25 μA, and -40 ºC < T_J = T_A < 125 ºC (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
BIAS SUPPLY INPUT CURRENT						
$I_{RUN(STOP)}$	Supply current, run	No switching		2.3	3	mA
$I_{RUN(SW)}$	Supply current, run	Switching, I_{VSL} = 0 μA		2.5	3.3	mA
I_{WAIT}	Supply current, wait	I_{FB} = -85 μA		400	550	μA
I_{START}	Supply current, start	V_{VDD} = $V_{VDD(ON)}$ – 100 mV, V_{VS} = 0 V		70	140	μA
I_{FAULT}	Supply current, fault	Fault state		265	350	μA
UNDER-VOLTAGE LOCKOUT (UVLO)						
$V_{VDD(ON)}$	VDD turn-on threshold	V_{VDD} increasing	16.7	17.5	18.2	V
$V_{VDD(OFF)}$	VDD turn-off threshold	V_{VDD} decreasing	9.35	9.8	10.4	V
$V_{VDD(PCT)}$	Offset to power cycle for long output voltage overshoot	Offset above $V_{VDD(OFF)}$, I_{FB} = -85 μA	0.3	1	1.5	V
VS INPUT						
V_{VSNC}	Negative clamp level	I_{VSL} = -1.25 mA, voltage below ground	170	250	325	mV
V_{ZCD}	Zero-crossing detection (ZCD) level	V_{VS} decreasing	10	30	55	mV
t_{ZC}	Zero-crossing timeout delay		1.8	2.2	2.7	μs
$t_{D(ZCD)}$	Propagation delay from ZCD high to PWML high	V_{VS} step from 4 V to -0.1 V		20	45	ns
I_{VSB}	Input bias current	V_{VS} = 4 V	-0.25	0	0.25	μA
CS INPUT						
$V_{CST(MAX)}$	Maximum CS threshold voltage	V_{CS} increasing	765	800	825	mV
$V_{CST(MIN)}$	Minimum CS threshold voltage	V_{CS} decreasing, I_{FB} = -85 μA	123	150	170	mV
t_{CSLEB}	Leading-edge blanking time	V_{SET} = 5 V, V_{CS} = 1 V	175	200	225	ns
		V_{SET} = 0 V, V_{CS} = 1 V	115	130	145	
$t_{D(CS)}$	Propagation delay of CS comparator high to PWML low	V_{CS} step from 0 V to 1 V		15	25	ns
K_{LC}	Line-compensation current ratio	I_{VSL} = -1.25 mA, I_{VSL} / current out of CS pin	22.5	25	27	A/A
RUN, PWML, PWMH						
V_{PWMLH} V_{PWMHH} V_{RUNH}	High level of PWML, PWMH, and RUN pins	$I_{PWML(H)}$ = -1 mA, I_{RUN}= -1 mA	4.4	5		V
V_{PWMLL} V_{PWMHL} V_{RUNL}	Low level of PWML, PWMH, and RUN pins	$I_{PWML(H)}$ = +1 mA, I_{RUN} = +1 mA			0.5	V
t_{RISE}	Turn-on rise time, 10% to 90%(1)	C_{LOAD} = 10 pF			10	ns
t_{FALL}	Turn-off fall time, 90% to 10%(1)	C_{LOAD} = 10 pF			10	ns
$t_{D(RUN-PWML)}$	Delay from RUN high to PWML high		1.8		5.4	μs
$t_{D(VS-PWMH)}$	Dead-time between VS high and PWMH high	V_{SET} = 5 V	44	55	70	ns
$t_{D(PWML-H)}$	Dead-time between PWML low and PWMH high	V_{SET} = 0 V	34	42	51	ns
$t_{ON(MIN)}$	Minimum on-time of PWML in low power mode	V_{SET} = 5 V, I_{FB} = -85 μA, V_{CS} = 1 V	70	90	115	ns
		V_{SET} = 0 V, I_{FB} = -85 μA, V_{CS} = 1 V	48	65	80	ns

(1) Not tested in protection, and limits guaranteed by design.

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Electrical Characteristics (continued)

Over operating free-air temperature range, V_{VDD} = 15V, R_{RDM} = 115 kΩ, R_{RTZ} = 140 kΩ, V_{BUR}= 1.2 V, V_{SET} = 0 V, R_{NTC} = 50 kΩ, V_{VS} = 4 V, V_{SWS} = 0 V, I_{FB} = 0 μA, I_{HVG} = 25 μA, and -40 ºC < T_J = T_A < 125 ºC (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
PROTECTION						
V_{OVP}	Over-voltage threshold	V_{VS} increasing	4.4	4.5	4.6	V
V_{OCP}	Over-current threshold	V_{CS} increasing	0.97	1.2	1.35	
$V_{CST(OPP)}$	Over-power threshold on CS pin	I_{VSL} = 0 μA	574	600	627	mV
		I_{VSL} = -333 μA	492	545	595	
		I_{VSL} = -666 μA	426	460	492	
		I_{VSL} = -1.25 mA	405	425	452	
K_{OPP}	OPP threshold voltage ratio	$V_{CST(OPP)}$ ratio between I_{VSL} = 0 μA and I_{VSL} = -1.25 mA	1.36	1.4	1.44	V/V
t_{OPP}	OPP fault timer	I_{FB} = 0 A	115	160	200	ms
$I_{VSL(RUN)}$	VS line-sense run current	Current out of VS pin increasing	330	365	400	μA
$I_{VSL(STOP)}$	VS line-sense stop current	Current out of VS pin decreasing	275	305	335	
K_{VSL}	VS line-sense ratio	$I_{VSL(STOP)}$ / $I_{VSL(RUN)}$	0.81	0.836	0.85	A/A
t_{BO}	Brown-out detection delay time	I_{VSL} < $I_{VSL(STOP)}$	35	60	75	ms
$R_{RDM(TH)}$	R_{RDM} threshold for CS pin fault		41	50	59	kΩ
t_{CSF1}	Max. PWML on time for detecting CS pin fault	V_{SET} = 5 V	1.6	2	2.3	μs
t_{CSF0}	Max. PWML on time for detecting CS pin fault	R_{RDM} < $R_{RDM(TH)}$ for V_{SET} = 0 V	0.8	1	1.15	μs
t_{FDR}	Fault-reset delay timer	OCP, OPP, OVP, SCP, or CS pin fault	1	1.5	1.9	s
$T_{J(STOP)}$	Thermal shut-down temperature	Internal junction temperature	125			°C
NTC INPUT						
V_{NTCTH}	NTC shut-down voltage	Voltage decreasing	0.9	1.0	1.1	V
R_{NTCTH}	NTC shut-down resistance	R_{NTC} decreasing	8.7	9.5	10.3	kΩ
R_{NTCR}	NTC recovery resistance	R_{NTC} increasing	19.5	21.7	24	kΩ
I_{NTC}	NTC pull-up current, out of pin	R_{NTC} = 12 kΩ	85	105	120	μA
BUR INPUT AND LOW POWER MODE						
$K_{BUR-CST}$	Ratio from V_{BUR} to V_{CST}	V_{CST} between $V_{CST(OPP1)}$ and 0.7 V	3.9	4	4.13	V/V
$f_{BR(UP)}$	Upper threshold of burst rate frequency in adaptive burst mode(1)		29	34	39	kHz
$f_{BR(LR)}$	Lower threshold of burst rate frequency in adaptive burst mode(1)		21	25	29	kHz
f_{LPM}	Burst rate frequency in low power mode		22	25	28	kHz
I_{BUR}	Bias current of V_{BUR} offset in LPM		2.1	2.7	3.4	μA
RTZ INPUT						
$t_{Z(MAX)}$	Maximum programmable dead-time from PWMH low to PWML high	R_{RTZ} = 280 kΩ, I_{VSL} = -1 mA, V_{SET} = 5 V	380	480	565	ns
$t_{Z(MIN)}$	Minimum programmable dead-time from PWMH low to PWML high	R_{RTZ} = 78.4 kΩ, I_{VSL} = -1 mA, V_{SET} = 0 V	66	72	86	ns
t_Z	Dead-time from PWMH low to PWML high	I_{VSL} = -150 μA	144	172	205	ns
		I_{VSL} = -450 μA	123	150	177	ns
		I_{VSL} = -733 μA	110	125	145	ns
K_{TZ}	T_Z compensation ratio	T_Z ratio between I_{VSL} = -200 μA and I_{VSL} = -733 μA	1.26	1.4	1.57	s/s

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Electrical Characteristics (continued)

Over operating free-air temperature range, V_{VDD} = 15V, R_{RDM} = 115 kΩ, R_{RTZ} = 140 kΩ, V_{BUR}= 1.2 V, V_{SET} = 0 V, R_{NTC} = 50 kΩ, V_{VS} = 4 V, V_{SWS} = 0 V, I_{FB} = 0 μA, I_{HVG} = 25 μA, and -40 ºC < T_J = T_A < 125 ºC (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
SWS INPUT						
$V_{TH(SWS)}$	SWS zero voltage threshold	V_{SET} = 5 V	8.8	9	9.6	V
		V_{SET} = 0 V	3.7	4	4.3	V
$t_{D(SWS-PWML)}$	Time between SWS low to PWML high	V_{SWS} step from 5 V to 0 V		12	28	ns
FB INPUT						
$I_{FB(SBP)}$	Maximum control FB current	I_{FB} increasing		75	95	μA
$V_{FB(REG)}$	Regulated FB voltage level		4	4.3	4.65	V
R_{FBI}	FB input resistance		7	8	9.5	kΩ
REF OUTPUT						
V_{REF}	REF voltage level	I_{REF} = 0 A	4.9	5	5.1	V
$I_{S(REF)}$	Short current of REF pin	Short REF pin	8	14	18	mA
$V_{R(LINE)}$	Line regulation of V_{REF}	V_{VDD} = 12 V to 35 V	-5		7	mV
$V_{R(LOAD)}$	Load regulation of V_{REF}	I_{REF} = 0 mA to 1 mA, change in V_{REF}	-10		10	mV
HVG OUTPUT						
V_{HVG}	HVG voltage level	I_{HVG} = +/-200 μA, run state	9.7	10.5	11.4	V
$I_{SE(HVG)}$	HVG max sink current during startup	V_{HVG} = 13 V, start state	55	90	140	μA
$I_{S(HVG)}$	Short current of HVG pin	Short HVG pin	0.4	1	1.6	mA
$V_{HR(LINE)}$	Line regulation of V_{HVG}	V_{VDD} = 12 V to 35 V	-25		25	mV
$V_{HVG(OV)}$	HVG over voltage threshold		13.0	13.8	14.6	V
RDM INPUT						
$t_{DM(MAX)}$	Maximum PWMH pulse width with maximum tuning	V_{SWS} = 12 V	6.08	6.76	7.6	μs
$t_{DM(MIN)}$	Minimum PWMH pulse width with minimum tuning	V_{SWS} = 0 V	3.05	3.4	3.8	μs

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6.7 Typical Characteristics

V_{VDD} = 15V, R_{RDM} = 115 kΩ, R_{RTZ} = 140 kΩ, V_{SET} = 0 V, and $T_J = T_A$ = 25 ºC (unless otherwise noted)

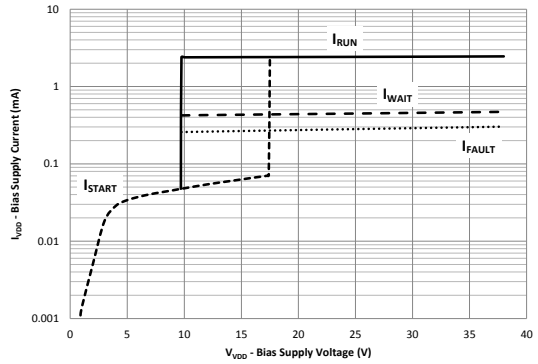


図 1. VDD Bias-Supply Current vs. VDD Bias-Supply Voltage

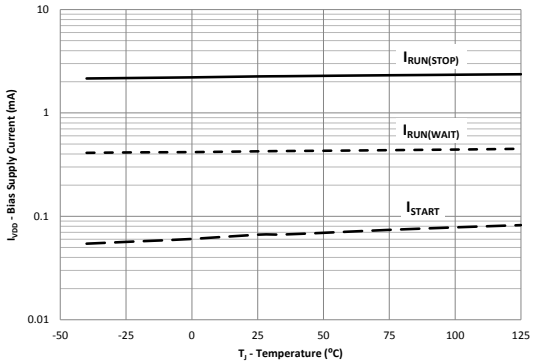


図 2. VDD Bias-Supply Current vs. Junction Temperature

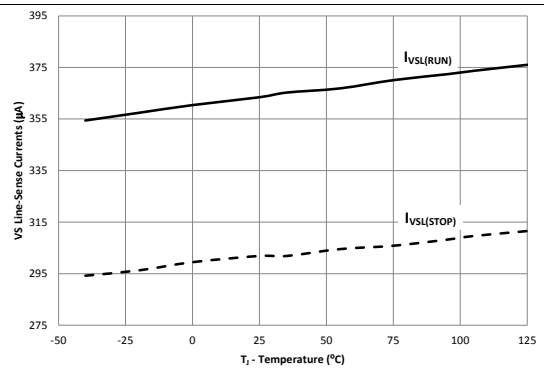


図 3. VS Line-Sense Currents vs. Temperature

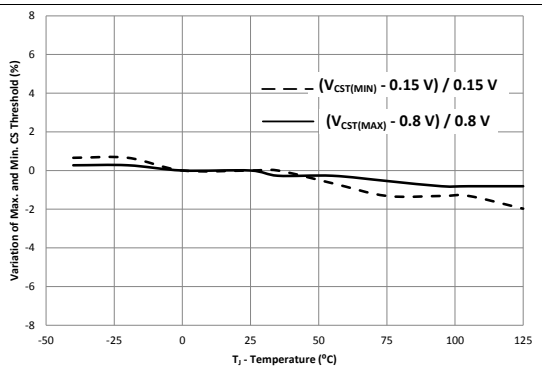


図 4. Percentage Variation of Maximum and Minimum CS Thresholds vs. Temperature

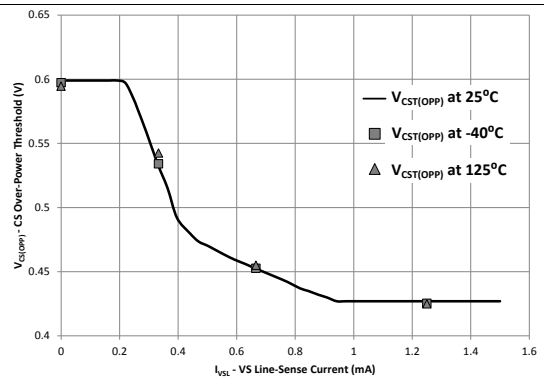


図 5. CS Over-Power Threshold vs. VS Line-Sense Currents

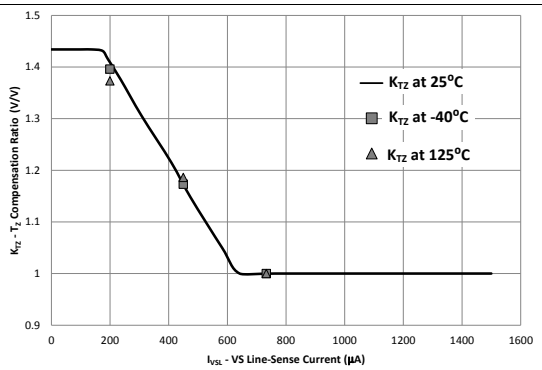


図 6. t_Z Compensation Ratio (K_{TZ}) vs. VS Line-Sense Currents

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Typical Characteristics (continued)

V_{VDD} = 15V, R_{RDM} = 115 kΩ, R_{RTZ} = 140 kΩ, V_{SET} = 0 V, and T_J = T_A = 25 ºC (unless otherwise noted)

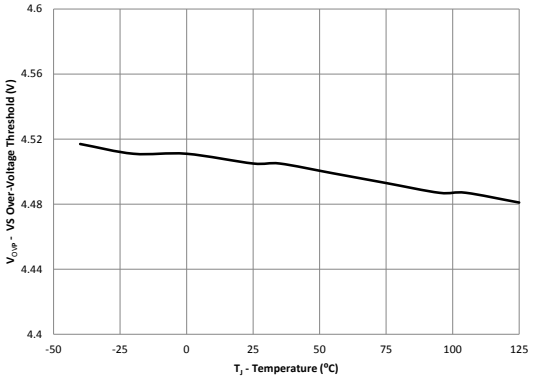


図 7. VS Over-Voltage Threshold vs. Temperature

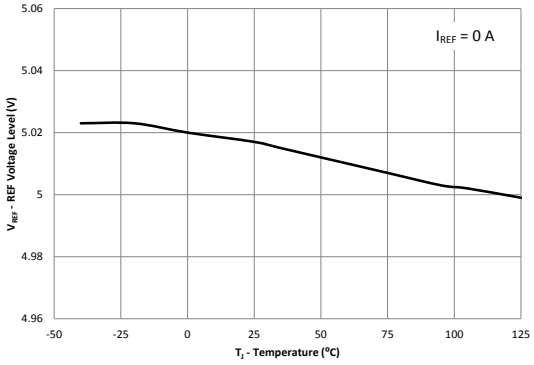


図 8. REF Voltage vs. Temperature

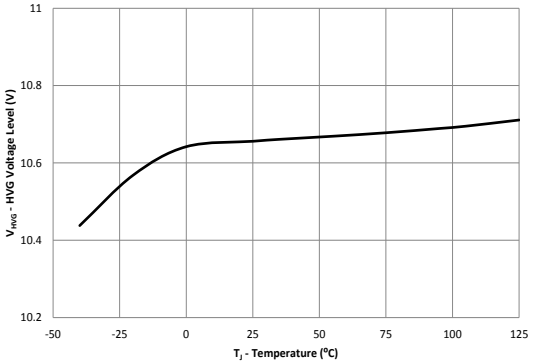


図 9. HVG Voltage vs. Temperature

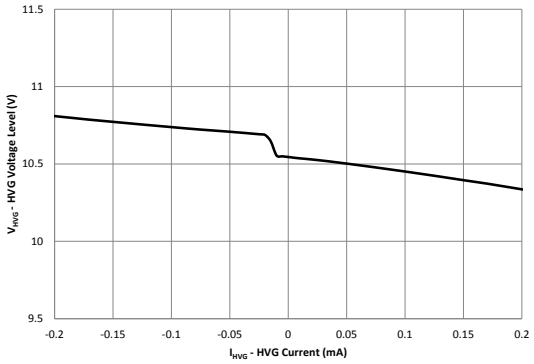


図 10. HVG Voltage vs. HVG Current

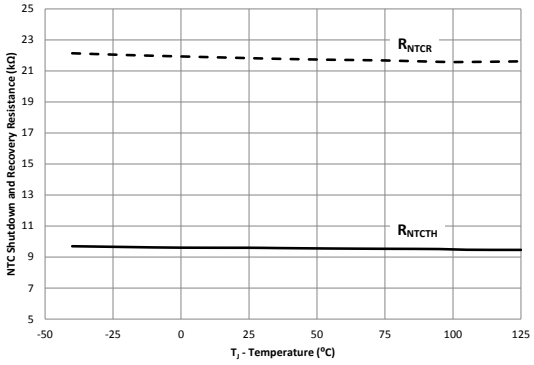


図 11. NTC Thresholds vs. Junction Temperature

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7 Detailed Description

7.1 Overview

The UCC28780 is a transition-mode (TM) active clamp flyback (ACF) controller, equipped with advanced control schemes to enable significant size reduction of passive components for higher power density and higher average efficiency. The control law is optimized for Silicon (Si) and Gallium Nitride (GaN) power FETs in a half-bridge configuration and is capable of driving high-frequency AC/DC converters up to 1 MHz. The zero voltage switching (ZVS) control of the UCC28780 is capable of auto-tuning the on-time of a high-side clamp switch (Q_H) by using a unique lossless ZVS sensing network connected between the switch-node voltage (V_{SW}) and SWS pin. The ACF controller is designed to adaptively achieve targeted full-ZVS or partial-ZVS conditions for the low-side main switch (Q_L) with minimum circulating energy over wide operating conditions. Auto-tuning eliminates the risk of losing ZVS due to component tolerance, input/output voltage changes, and temperature variations, since the Q_H on-time is corrected cycle-by-cycle.

Dead-times between PWML (controls Q_L) and PWMH (controls Q_H) are optimally adjusted to help minimize the circulating energy required for ZVS. Therefore, the overall system efficiency can be significantly improved and more consistent efficiency can be obtained in mass production of the soft-switching topology. The programming features of the RTZ, RDM, BUR, and SET pins provide rich flexibility to optimize the power stage efficiency across a range of output power and operating frequency levels.

The UCC28780 uses four different operating modes to maximize efficiency over wide load and line ranges. Adaptive amplitude modulation (AAM) adjusts the peak primary current at the higher load levels. Adaptive burst mode (ABM) modulates the pulse count of each burst packet in the medium to light load range. Low power mode (LPM) reduces the peak primary current of each two-pulse burst packet in the very light load range. Standby power (SBP) mode minimizes the loss during no load conditions.

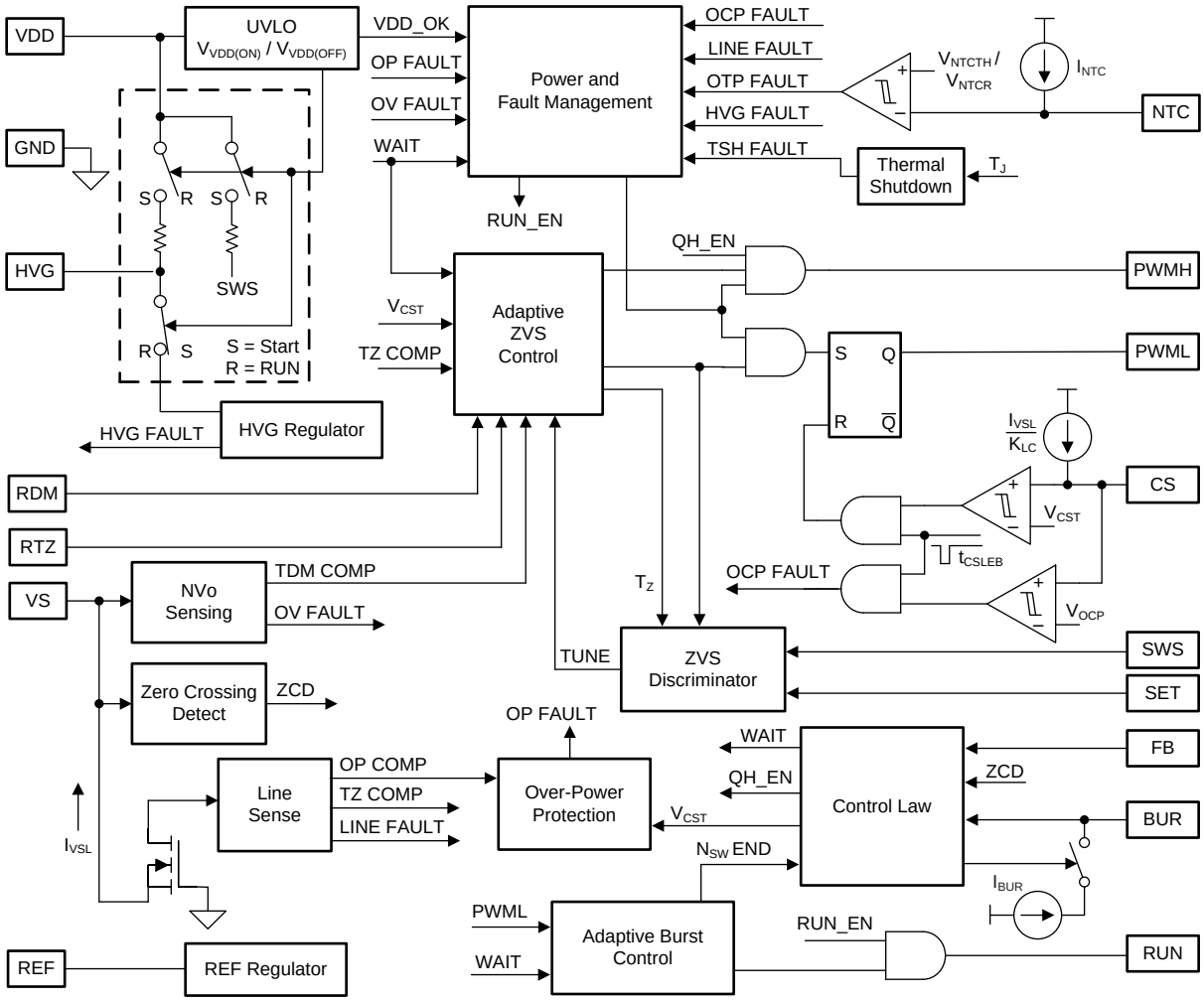
The unique burst mode control of the UCC28780 maximizes the light load efficiency of the ACF power stage, while avoiding the concerns of conventional burst operation - such as output ripple and audible noise. The burst control provides an enable signal through the RUN pin to dynamically manage the static current of the half-bridge driver and also adaptively disables the on-time of Q_H. These functions can be used to manage the quiescent power consumed by the half-bridge driver, further improving the converter's light-load efficiency and reducing its standby power.

Instead of using a conventional high-voltage resistor, the UCC28780 starts up the VDD supply voltage with an external high-voltage depletion-mode MOSFET between the SWS pin and the switch node. Fast startup is achieved with low standby power overhead. Moreover, the HVG pin controls the gate of the depletion-mode FET to also allow this MOSFET to be used in a lossless ZVS sensing. This arrangement avoids additional sensing devices.

The UCC28780 also integrates a robust set of protection features tailored to maximize the reliability. These features include internal soft start, brown in/out, output over-voltage, output over-power, system over-temperature, switch over-current, output short-circuit protection, and pin open/short.

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7.2 Functional Block Diagram



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7.3 Detailed Pin Description

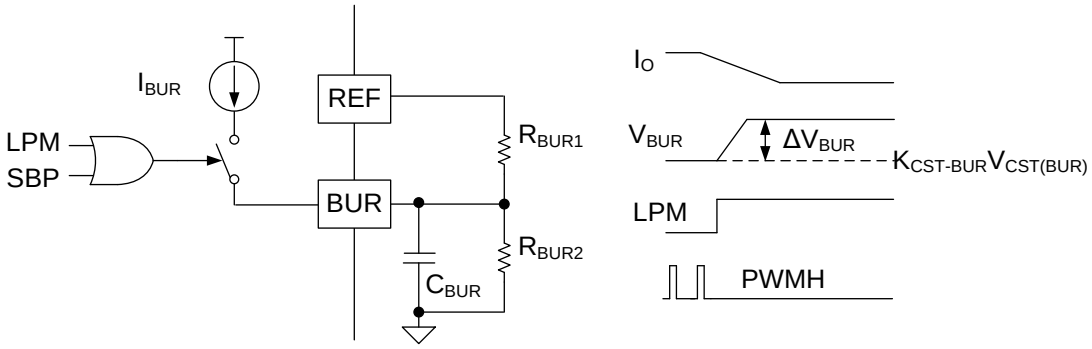
7.3.1 BUR Pin (Programmable Burst Mode)

The voltage at the BUR pin (V_{BUR}) sets a target peak current threshold ($V_{CST(BUR)}$) which programs the onset of adaptive burst mode (ABM) and determines the clamped peak current level of switching cycles in each burst packet. When V_{BUR} is designed higher, ABM will start at heavier output load conditions with higher peak current, so the benefit is the higher light-load efficiency but the side effect is a larger burst output voltage ripple. Therefore, 50% to 60% of output load at high line is the recommended highest load condition entering into ABM ($I_{o(BUR)}$) for both Si and GaN-based ACF designs. The gain between V_{BUR} and $V_{CST(BUR)}$ is a constant gain of $K_{BUR-CST}$, so setting $V_{CST(BUR)}$ just requires properly selecting the resistor divider on the BUR pin formed by R_{BUR1} and R_{BUR2}. V_{BUR} should be set between 0.7 V and 2.4 V. If V_{BUR} is less than 0.7 V, $V_{CST(BUR)}$ holds at 0.7 V / $K_{BUR-CST}$. If V_{BUR} is higher than 2.4 V, $V_{CST(BUR)}$ stays at 2.4 V / $K_{BUR-CST}$.

$$R_{BUR2} = \frac{R_{BUR1} K_{BUR-CST} V_{CST(BUR)}}{V_{REF} - K_{BUR-CST} V_{CST(BUR)}} = \frac{4 \times R_{BUR1} V_{CST(BUR)}}{5V - 4 \times V_{CST(BUR)}} \quad (1)$$

In order to enhance the mode transition between ABM and Low Power Mode (LPM), a programmable offset voltage (ΔV_{BUR}) is generated on top of the V_{BUR} setting in ABM through an internal 2.7-μA current source (I_{BUR}), as shown in 図 12. In ABM mode, V_{BUR} is set through the resistor voltage divider to fulfill the target average efficiency. After transition from ABM to LPM, the current source is enabled in LPM and flows out of the BUR pin, so ΔV_{BUR} can be programmed based on the Thevenin resistance on the BUR pin, which can be expressed as

$$\Delta V_{BUR} = I_{BUR} \times \frac{R_{BUR1} R_{BUR2}}{R_{BUR1} + R_{BUR2}} \quad (2)$$



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図 12. Hysteresis Voltage Generation on BUR Pin

When V_{BUR} becomes higher after transition to LPM, the initial peak magnetizing current in LPM is increased with larger energy per switching cycle in a burst packet, which forces UCC28780 to stay in LPM with a higher feedback current than ABM. If ΔV_{BUR} is designed too small, it is possible that mode toggling between LPM and ABM can occur resulting in audible noise. For that situation, ΔV_{BUR} greater than 100 mV is recommended. To minimize the noise coupling effect on V_{BUR}, a filter capacitor on the BUR pin (C_{BUR}) may be needed. C_{BUR} needs to be properly designed to minimize the delay of generating ΔV_{BUR} in time during mode transition. It is recommended that C_{BUR} should be sized small enough to ensure ΔV_{BUR} settles within 40 μs, corresponding to the burst frequency of 25 kHz in LPM (f_{LPM}). Based on three RC time constants representing 95% of a settled steady state value from a step response, the design guide of C_{BUR} is expressed as

$$C_{BUR} \le 40\mu s \times \frac{R_{BUR1} + R_{BUR2}}{3 R_{BUR1} R_{BUR2}} \quad (3)$$

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Detailed Pin Description (continued)

7.3.2 FB Pin (Feedback Pin)

The FB pin connects to the collector of an optocoupler output transistor through an external current-limiting resistor (R_{FB}). Depending on the operating mode, the controller uses different content of the collector current flowing out of the FB pin (I_{FB}) to regulate the output voltage. For the operating modes based on peak current control, I_{FB} is converted into an internal peak current threshold (V_{CST}) to modulate the amplitude of the current sense signal on the CS pin. For example, when the output voltage (V_O) is lower than the regulation level set by the shunt regulator, the "current level" of I_{FB} moves to lower value, so V_{CST} goes up to deliver more power to the output load.

As the burst control takes over the V_O regulation, where V_{CST} is clamped to $V_{CST(BUR)}$, the "current ripple" of I_{FB} is used to modulate burst off time, as shown in 図 13. Specifically, after a group of pulses stop bursting, the output load current starts to discharge the output capacitor, which makes V_O start to decay. A proper type-III compensation on the secondary side of V_O feedback loop minimizes the phase-delay between I_{FB} current ripple and output voltage ripple. For a detailed design guide on each passive component of the type-III compensator, please refer to Application and Implementation. When the decaying I_{FB} intersects with an internal reference current ($I_{TH(FB)}$), the ripple regulator generates a new set of grouped burst pulses to deliver more power, which makes V_O and I_{FB} ripples move upward.

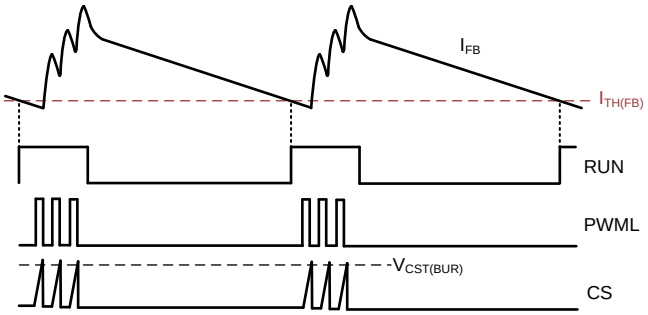


図 13. Concept of Burst Control

The nature of ripple-based control in burst mode requires additional care on the noise level of I_{FB} to improve the consistency of burst off-time between burst cycles. Firstly, a high-quality ceramic-bypass capacitor between FB pin and REF pin (C_{FB}) is required for decoupling I_{FB} noise. A minimum of 100 pF is recommended. There is an internal 8-kΩ resistor (R_{FBI}) connected to the FB pin that in conjunction with an external C_{FB} forms an effective low-pass filter. On the other hand, too strong low-pass filtering with too large C_{FB} can attenuate the I_{FB} ripple creating slope distortion of the intersection point between I_{FB} and $I_{TH(FB)}$, which can cause inconsistent burst off-times, even though V_O stays in regulation and the I_{FB} noise is low. Secondly, since ABM utilizes the falling-edge burst-ripple content of I_{FB} to determine the beginning of every burst packet, the operation is affected if the burst-ripple content of the output voltage is too small due to using a low-ESR output capacitor, or if there is an additional low-frequency ringing on the output ripple due to using a second-order output filter.

Compared with an electrolytic-type of output capacitor, the advantage of ACF using a low-ESR output capacitor such as a polymer capacitor is to minimize the switching-ripple content of the output voltage to meet the ripple specification, but the burst-ripple content is also reduced. Therefore, the switching ripple and noise on I_{FB} may be very close to $I_{TH(FB)}$, which triggers the next burst event prematurely. For a converter using a second-order output filter, a π filter design as example, even though both switching-ripple and burst-ripple contents are further attenuated, additional low-frequency ringing caused by the resonance between the output filter inductor and one of the output filter capacitors is generated, which may trigger the next burst event too early as well. Therefore, applying an active ripple compensation (ARC) technique is recommended to generate a noise-free burst ripple artificially to stabilize the ABM operation of ACF using either a low-ESR output capacitor or a second-order output filter.

図 14 illustrates the implementation of ARC formed by a high-impedance resistor (R_{COMP}) in series with a small-signal enhancement MOSFET (Q_{COMP}) where its gate is controlled by the RUN pin of UCC28780. When RUN pin is in a high state which turns on Q_{COMP}, R_{COMP} connected to FB pin creates a compensation current (I_{COMP}), with a magnitude around V_{FB} / R_{COMP}. When RUN pin changes to a low state which turns off Q_{COMP}, R_{COMP} and the drain-source junction capacitor of Q_{COMP} creates a slow falling edge of I_{COMP}, with a ramp slope dependent on

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Detailed Pin Description (continued)

the RC time constant. Then, the summation of the current from the optocoupler (I_{OPTO}) and I_{COMP} becomes the total feedback current out of FB pin (I_{FB}) to compare with $I_{TH(FB)}$. As the ARC operation in 図 15 explains, the magnitude of I_{COMP} helps to push any switching and noise content of I_{FB} away from $I_{TH(FB)}$, and the slow falling edge of I_{COMP} further pushes the undesirable ripple content away from $I_{TH(FB)}$, especially the low-frequency ringing of the π output filter. The magnitude of I_{COMP} can be adjusted by R_{COMP}, and 1 MΩ to 2 MΩ is the recommended value which injects around 2 μA to 4 μA of compensation ripple current into the loop.

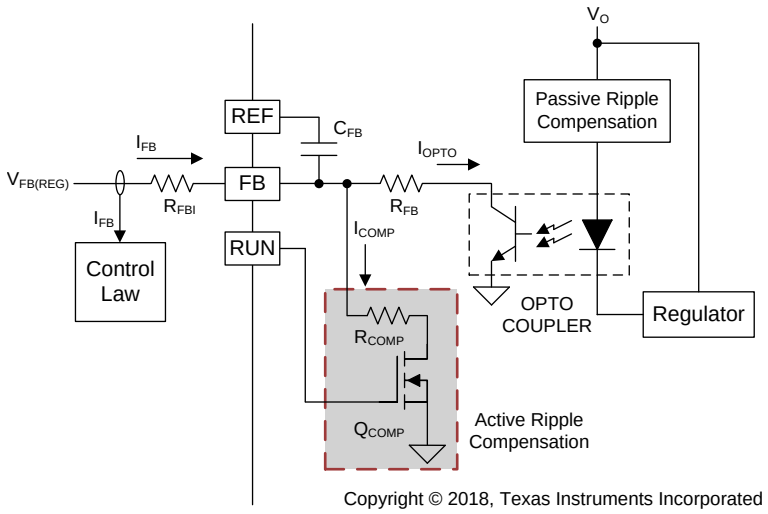


図 14. Implementation of Active Ripple Compensation (ARC)

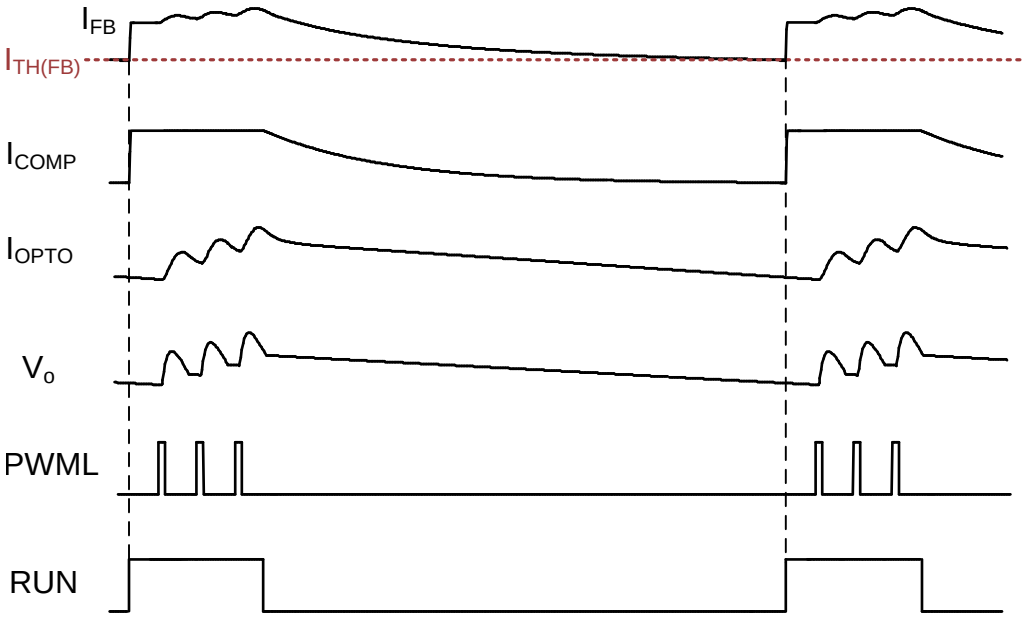


図 15. Concept of Burst Control with ARC

7.3.3 VDD Pin (Device Bias Supply)

The VDD pin is the primary bias for the internal 5-V REF regulator, internal 11-V HVG regulator, other internal references, and the undervoltage lock-out (UVLO) circuit. As shown in Functional Block Diagram, the UVLO circuit connected to the VDD pin controls three power-path switches among VDD, HVG, and SWS pins, in order to allow Q_S to be able to perform both V_{VDD} startup and V_{SW} sensing for ZVS control after startup. During startup, SWS and HVG pins are connected to VDD pin allowing an external depletion-mode MOSFET (Q_S) to charge the

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Detailed Pin Description (continued)

VDD capacitor (C_{VDD}) from the switch-node voltage (V_{SW}). After VDD startup competes, the ZVS discriminator block is enabled, so as switching logics. Then, the transformer starts delivering energy to the output capacitor (C_O) every switching cycle, so both output voltage (V_O) and auxiliary winding voltage (V_{AUX}) increase. As V_{AUX} is high enough, the auxiliary winding will take over to power V_{VDD}. The UVLO circuit provides a turn-on threshold of $V_{VDD(ON)}$ at 17.5 V and turn-off threshold of $V_{VDD(OFF)}$ at 9.8 V. The range can accommodate lower values of VDD capacitor (C_{VDD}) and support shorter power-on delays. 38-V maximum operating level on V_{VDD} alleviates concerns with leakage energy charging of C_{VDD} and gives added flexibility when a varying output voltage must be supported.

As V_{VDD} reaches $V_{VDD(ON)}$, SWS pin is disconnected from the VDD pin, so the C_{VDD} size has to be sufficient to hold V_{VDD} higher than $V_{VDD(OFF)}$ until the positive auxiliary winding voltage is high enough to take over bias power delivery during V_O soft start. Therefore, the calculation of minimum capacitance ($C_{VDD(MIN)}$) needs to consider the discharging effect from the sink current of the UCC28780 during switching in its run state ($I_{RUN(SW)}$), the average operating current of driver (I_{DR}), and the average gate charge current of half-bridge FETs (I_{Qg}) throughout the longest time of V_O soft start ($t_{SS(MAX)}$).

$$C_{VDD(MIN)} = \frac{(I_{RUN(SW)} + I_{DR} + I_{Qg})t_{SS(MAX)}}{V_{VDD(ON)} - V_{VDD(OFF)}} \tag{4}$$

$t_{SS(MAX)}$ estimation should consider the averaged soft-start current ($I_{SEC(SS)}$) on the secondary side of ACF, the constant-current output load ($I_{O(SS)}$) (if any), maximum output capacitance ($C_{O(MAX)}$), and a 1-ms time-out potentially being triggered in the startup sequence.

$$t_{SS(MAX)} = \frac{C_{O(MAX)}V_O}{I_{SEC(SS)} - I_{O(SS)}} + 1ms \tag{5}$$

During V_O soft start, V_{CST} reaches the maximum current threshold on the CS pin ($V_{CST(MAX)}$) , so $I_{SEC(SS)}$ at the minimum voltage of the input bulk capacitor ($V_{BULK(MIN)}$) can be approximated as:

$$I_{SEC(SS)} = \frac{N_{PS}V_{CST(MAX)}}{2R_{CS}} \frac{V_{BULK(MIN)}}{V_{BULK(MIN)} + N_{PS}(V_O + V_F)} \tag{6}$$

where R_{CS} is the current sense resistor, N_{PS} is primary-to-secondary turns ratio, and V_F is the forward voltage drop of the secondary rectifier.

For details of the startup sequencing, one can refer to the Device Functional Modes of this datasheet.

7.3.4 REF Pin (Internal 5-V Bias)

The output of the internal 5-V regulator of the controller is connected to this pin. It requires a high-quality ceramic-bypass capacitor (C_{REF}) to GND for decoupling switching noise and lowering the voltage droop as the controller transitions from wait state to run state. The minimum C_{REF} value is 0.1 μF, and a high quality dielectric material should be used, such as a X7R. The output short current ($I_{S(REF)}$) of the REF regulator is self-limited to approximately 14 mA. 5-V bias is only available after the under-voltage lock-out (UVLO) circuit enables the operation of UCC28780 after V_{VDD} reaches $V_{VDD(ON)}$.

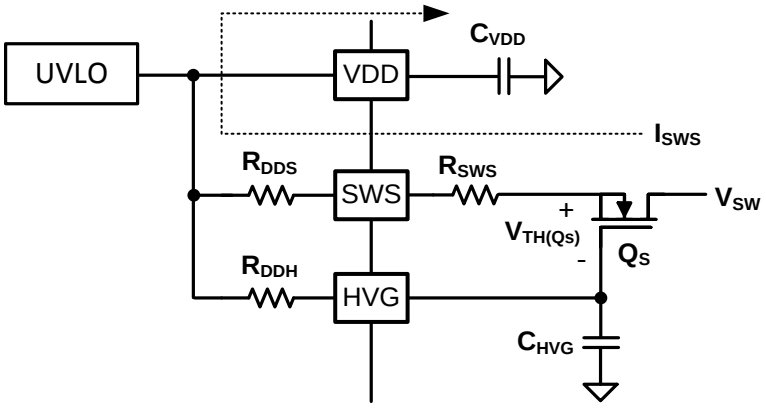
7.3.5 HVG and SWS Pins

The HVG pin provides a controlled voltage to the gate of the depletion-mode MOSFET (Q_S), enabling Q_S to serve both V_{VDD} startup and lossless ZVS sensing from the high-voltage switch node (V_{SW}). During V_{VDD} startup, the UVLO circuit commands two power-path switches connecting SWS and HVG pins to VDD pin with two internal current-limit resistors (R_{DDS} and R_{DDH}) separately, as shown in 図 16. In this configuration, Q_S behaves as a current source to charge the VDD capacitor (C_{VDD}). R_{DDS} is set at 12 kΩ when V_{VDD} is below 1 V to limit the maximum fault current under VDD pin short events. R_{DDS} is reduced to 1 kΩ when V_{VDD} rises above 1 V to allow V_{VDD} to charge faster. The maximum charge current (I_{SWS}) is affected by R_{DDS}, the external series resistance (R_{SWS}) from SWS pin to Q_S, and the threshold voltage of Q_S ($V_{TH(Qs)}$). I_{SWS} can be calculated as

$$I_{SWS} = \frac{V_{TH(Qs)}}{R_{DDS} + R_{SWS}} \tag{7}$$

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Detailed Pin Description (continued)

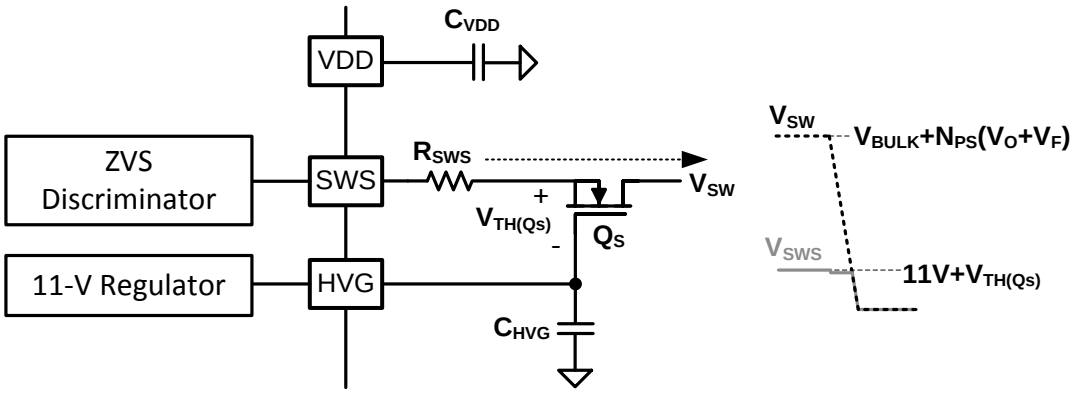


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図 16. Operation of the VDD Startup Circuit

After V_{VDD} reaches $V_{VDD(ON)}$, the two power-path switches open the connections among SWS, HVG, and VDD pins. At this point, a third power-path switch connects an internal 11-V regulator to the HVG pin for configuring Q_S to perform lossless ZVS sensing. As Q_S gate is fixed at 11 V and the drain pin voltage of Q_S becomes higher than the sum of Q_S threshold voltage ($V_{TH(Qs)}$) and the 11-V gate voltage, Q_S turns off and the source pin voltage of Q_S can no longer follow the drain pin voltage change, so this gate control method makes Q_S act as a high-voltage blocking device with the drain pin connected to V_{SW}. When the controller is switching, V_{SW} can be lower than 11 V, so Q_S turns on and forces the source pin voltage to follow V_{SW}, becoming a replica of the V_{SW} waveform at the lower voltage level, as illustrated in 図 17.

The limited window for monitoring the V_{SW} waveform suffices for ZVS control of the UCC28780, since the ZVS tuning threshold ($V_{TH(SWS)}$) is lower than that, which is at 9 V for V_{SET} = 5 V and at 4 V for V_{SET} = 0 V. The 9-V threshold is the auto-tuning target of the internal adaptive ZVS control loop for realizing a partial ZVS condition on the ACF using Si primary switches. On the other hand, performing full ZVS operation is more suitable for the ACF with GaN primary switches. The 4-V threshold can help to better compensate sensing delay between V_{SW} and the SWS pin more than using a 0-V threshold. The internal 11-V regulator requires a high quality ceramic bypass capacitor (C_{HVG}) between the HVG pin and GND for noise filtering and providing compensation to the regulator circuitry. The minimum C_{HVG} value is 2.2 nF and an X7R-type dielectric capacitor is recommended. The controller enters a fault state if the HVG pin is open or shorted to GND during V_{VDD} start-up, or if V_{HVG} overshoot is higher than $V_{HVG(OV)}$ of 13.8 V in run state. The output short current of HVG regulator ($I_{S(HVG)}$) is self-limited to around 1mA.



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図 17. ZVS Sensing by Reusing the VDD Startup Circuit

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Detailed Pin Description (continued)

7.3.6 RTZ Pin (Sets Delay for Transition Time to Zero)

The dead-time between PWMH falling edge and PWML rising edge (t_Z) serves as the wait time for V_{SW} transition from its high level down to the target ZVS point. Since the optimal t_Z varies with V_{BULK}, the internal dead-time optimizer automatically extends t_Z as V_{BULK} is less than the highest voltage of the input bulk capacitor ($V_{BULK(MAX)}$). The circulating energy for ZVS can be further reduced, obtaining higher efficiency at low line versus a fixed dead-time over a wide line voltage range. A resistor on RTZ pin (R_{RTZ}) programs the minimum t_Z ($t_{Z(MIN)}$) at $V_{BULK(MAX)}$, which is the sum of the propagation delay of the high-side driver ($t_{D(DR)}$) and the minimum resonant transition time of V_{SW} falling edge ($t_{LC(MIN)}$).

$$R_{RTZ} = K_{TZ} \times t_{Z(MIN)} = K_{TZ} \times (t_{D(DR)} + t_{LC(MIN)}) \tag{8}$$

where K_{TZ} is equal to 11.2×10^{11} (unit: F^{-1}) for V_{SET} = 0 V, and 5.6×10^{11}(unit: F^{-1}) for V_{SET} = 5 V. As illustrated in 図 18, after PWMH turns off Q_H after $t_{D(DR)}$ delay, the negative magnetizing current (i_{M-}) becomes an initial condition of the resonant tank formed by magnetizing inductance (L_M) and the switch-node capacitance (C_{SW}). C_{SW} is the total capacitive loading on the switch-node, including all junction capacitance (C_{OSS}) of switching devices, stray capacitance of the boot-strap diode, intra-winding capacitance of the transformer, the snubber capacitor, and parasitic capacitance of the PCB traces between switch-node and ground. Unlike a conventional valley-switching flyback converter, the resonance of an active clamp flyback converter at high line does not begin at the peak of the sinusoidal trajectory. The transition time of V_{SW} takes less than half of the resonance period. The following $t_{LC(MIN)}$ expression quantifies the transition time for R_{RTZ} calculation, where an arccosine term represents the initial angle at the resonance beginning. The value of π minus the arccosine term at $V_{BULK(MAX)}$ of 375 V, V_O of 20 V, and N_{PS} of 5 is around 0.585π, which is close to one quarter of the resonance period.

$$t_{LC(MIN)} = [\pi - \cos^{-1}(\frac{N_{PS}(V_O + V_F)}{V_{BULK(MAX)}})] \times \sqrt{L_M C_{SW}} \tag{9}$$

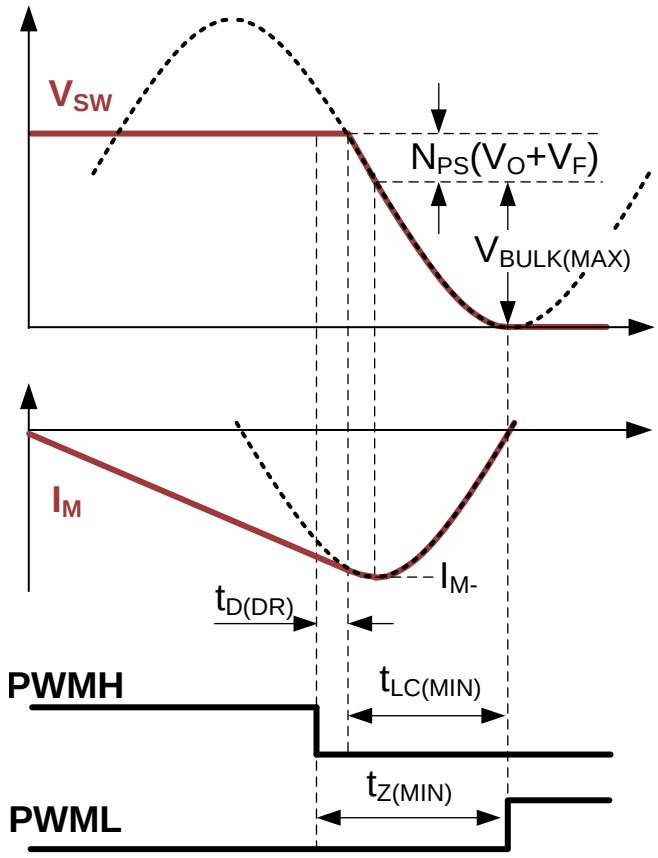


図 18. RTZ Setting for the Falling-edge Transition of V_{SW}

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Detailed Pin Description (continued)

7.3.7 RDM Pin (Sets Synthesized Demagnetization Time for ZVS Tuning)

The R_{RDM} resistor provides the power stage information to the t_{DM} optimizer for auto-tuning the on-time of PWMH to achieve ZVS within a given t_Z discharge time. The following equation calculates the resistance, based on the knowledge of the primary magnetizing inductance (L_M), auxiliary-to-primary turns ratio (N_A/N_P), the values of the resistor divider (R_{VS1} and R_{VS2}) from the auxiliary winding to VS pin, and the current sense resistor (R_{CS}). Among those parameters, L_M contributes the most variation due to its typically wider tolerance. The optimizer is equipped with wide enough on-time tuning range of PWMH to cover tolerance errors. Therefore, just typical values are enough for the calculation.

$$R_{RDM} = \frac{N_A R_{VS2}}{N_P (R_{VS1} + R_{VS2})} \frac{K_{DM} L_M}{R_{CS}} \tag{10}$$

where K_{DM} is equal to 5×10^9 (unit: F^{-1}) for both V_{SET} = 5 V and 0 V.

7.3.8 RUN Pin (Driver Enable Pin)

The RUN pin is a logic-level output signal to enable the gate driver. It generates a 5-V logic output when the driver should be active, and pulls down to less than 0.5 V when the driver should be disabled. During burst mode operation, the RUN pin serves as a power management function to dynamically reduce the static current of the driver, so light-load efficiency can be further improved and standby power can be minimized. In addition, there are two delays between RUN going high to first PWML pulse going high in each burst packet. The first delay is a fixed 2.2-μs delay time, intended to provide an appropriate wake-up time for UCC28780 and the gate driver to transition from a wait state to a run state. The second delay is another 2.2-μs timeout, t_{ZC} in the electrical table, intended to turn on the low-side switch of the first switching cycle per burst packet around the valley point of DCM ringing by waiting for the zero crossing detection (ZCD) on the auxiliary winding voltage (V_{AUX}). Therefore, the minimum total delay time is 2.2 μs typically if ZCD is detected immediately after the first 2.2-μs wake-up time, while the maximum total delay time is 4.4 μs if ZCD is not triggered after the timeout. The total delay time with tolerance over temperature are listed as $t_{D(RUN-PWML)}$ in the electrical table. RUN pin can also be used to control the external active ripple compensation network to enhance the stability of the burst regulation loop.

7.3.9 SET Pin

Due to different capacitance non-linearity between Si and GaN power FETs as well as different propagation delays of their drivers, SET pin is provided to program critical parameters of UCC28780 for the two distinctive power stages. Firstly, this pin sets the zero voltage threshold ($V_{TH(SWS)}$) at the SWS input pin to be two different auto-tuning targets for ZVS control. When SET pin is tied to GND, $V_{TH(SWS)}$ is set at its low level of 4 V for realizing full ZVS, which allows the low-side switch (Q_L) to be turned on when the switch-node voltage drops close to 0 V. When SET pin is tied to REF pin, $V_{TH(SWS)}$ is set at 9 V for implementing partial ZVS, which makes Q_L turn on at around 9V. Secondly, this pin generates different PWML-to-PWMH dead-time ($t_{D(PWML-H)}$) to achieve ZVS on the high-side clamp switch (Q_H). A fixed 40ns for V_{SET} = 0 V and an adaptive adjustment for V_{SET} = 5 V. Thirdly, this setting also selects the current sense leading edge blanking time (t_{CSLEB}) to accommodate different delays of the gate drivers; 130 ns for V_{SET} = 0 V and 200 ns for V_{SET} = 5 V. Fourthly, the minimum PWML on-time ($t_{ON(MIN)}$) in low-power mode and standby-power mode varies based on the driver capability; 65 ns for V_{SET} = 0 V and 90 ns for V_{SET} = 5 V. Finally, the maximum PWML on-time for detecting CS pin fault (t_{CSF}). t_{CSF} for V_{SET} = 5 V (t_{CSF1}) is set at 2 μs. t_{CSF} for V_{SET} = 0 V (t_{CSF0}) depends on R_{RDM}, which is configured to 1 μs under $R_{RDM} < R_{RDM(TH)}$ and to 2 μs under $R_{RDM} \geq R_{RDM(TH)}$.

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7.4 Device Functional Modes

7.4.1 Adaptive ZVS Control with Auto-Tuning

図 19 shows the simplified block diagram explaining the ZVS control of UCC28780. A high-voltage sensing network provides the replica of the switch node voltage waveform (V_{SW}) with a limited "visible" voltage range that the SWS pin can handle. The ZVS discriminator identifies the ZVS condition and determines the adjustment direction for the on-time of PWMH (t_{DM}) by detecting if V_{SW} reaches a predetermined ZVS threshold, $V_{TH(SWS)}$, within t_Z, where t_Z is the targeted zero voltage transition time of V_{SW} controlled by the PWMH-to-PWML dead-time optimizer.

In 図 19, V_{SW} of the current switching cycle in the dashed line has not reached $V_{TH(SWS)}$ after t_Z expires. The ZVS discriminator sends a TUNE signal to increase t_{DM} for the next switching cycle in the solid line, such that the negative magnetizing current (I_{M-}) can be increased to bring V_{SW} down to a lower level in the same t_Z. After a few switching cycles, the t_{DM} optimizer settles and locks into ZVS operation of the low-side switch (Q_L). In steady-state, there is a fine adjustment on t_{DM}, which is the least significant bit (LSB) of the ZVS tuning loop. This small change of t_{DM} in each switching cycle is too small to significantly move the ZVS condition away from the desired operating point. 図 20 demonstrates how fast the ZVS control can lock into ZVS operation. Before the ZVS loop is settled, UCC28780 starts in a valley-switching mode as t_{DM} is not long enough to create sufficient I_{M-}. Within 15 switching cycles, the ZVS tuning loop settles and begins toggling t_{DM} with an LSB.

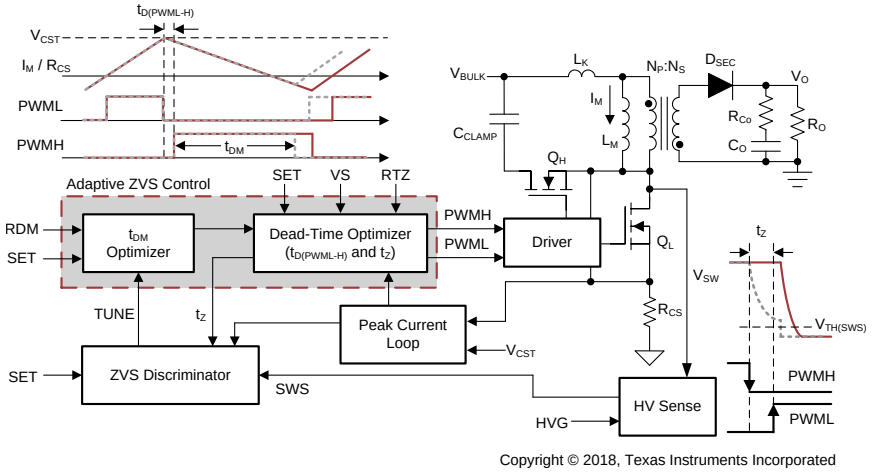


図 19. Block Diagram of Adaptive ZVS Control

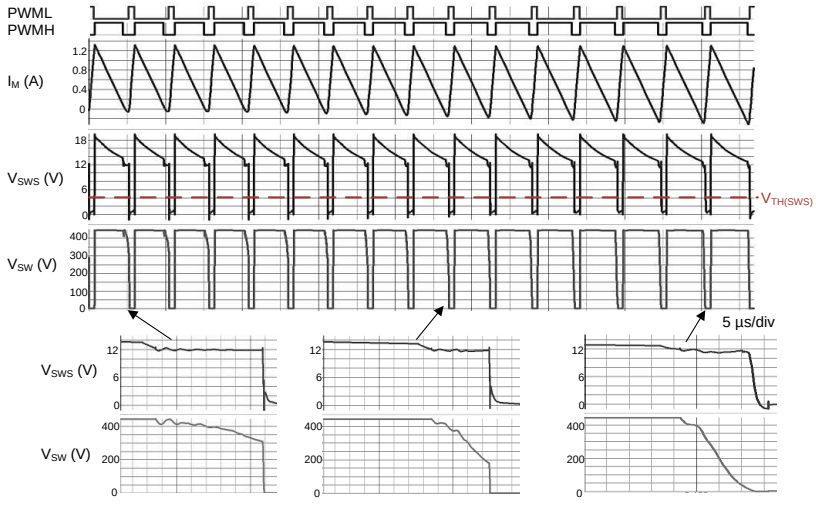


図 20. Auto-Tuning Process of Adaptive ZVS Control

Device Functional Modes (continued)

7.4.2 Dead-Time Optimization

The dead-time optimizer in 図 19 controls the two dead-times: the dead-time between PWMH falling edge and PWML rising edge (t_Z), as well as the dead-time between PWML falling edge and PWMH rising edge ($t_{D(PWML-H)}$).

The adaptive control law for t_Z of UCC28780 utilizes the line feed-forward signal to extend t_Z as V_{BULK} reduces, as shown in 図 21. The VS pin senses V_{BULK} through the auxiliary winding voltage (V_{AUX}) when the low-side switch (Q_L) is on. The auxiliary winding creates a line-sensing current (I_{VSL}) out of the VS pin flowing through the upper resistor of the voltage divider on VS pin (R_{VS1}). Minimum t_Z ($t_{Z(MIN)}$) is set at $V_{BULK(MAX)}$ through the RTZ pin. When I_{VSL} is lower than 666 µA, t_Z linearly increases and the maximum t_Z extension is 140% of $t_{Z(MIN)}$.

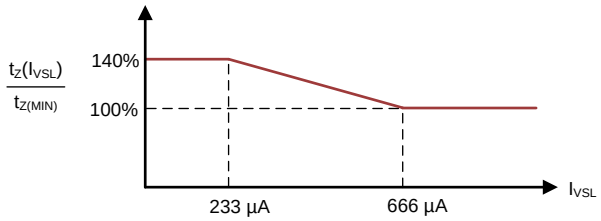


図 21. t_Z Control Optimized for Wide Input Voltage Range

The control law for $t_{D(PWML-H)}$ of UCC28780 is programmable based on the SET pin voltage. When V_{SET} = 0 V, a fixed delay around 40 ns is used to fit a GaN-based ACF with a fast dV/dt on the V_{SW} rising edge. With V_{SET} = 5 V, the dead-time optimization is enabled to intelligently adapt to the effect of nonlinear junction capacitance of Si MOSFETs on the dV/dt of V_{SW} rising edge. The high capacitance region of the C_{OSS} curve for the Si Q_L creates a shallow ramping on V_{SW} after PWML turns off. When C_{OSS} of Si Q_L moves to the low capacitance region with V_{SW} increasing, V_{SW} starts to ramp up very quickly. Since the changing slope varies with different peak magnetizing currents as output load changes, using a fixed dead-time can potentially cause hard-switching on the high-side clamp switch (Q_H) if the dead-time is not long enough. UCC28780 utilizes the zero crossing detect (ZCD) signal on the auxiliary-winding voltage to identify if V_{SW} overcomes the shallow ramping, and generates a 50-ns delay ($t_{D(VS-PWMH)}$) before turning on PWMH. This feature allows cycle-by-cycle dead-time adjustment to avoid hard-switching of Q_H, while providing fast turn-on timing for Q_H to minimize the body-diode conduction time.

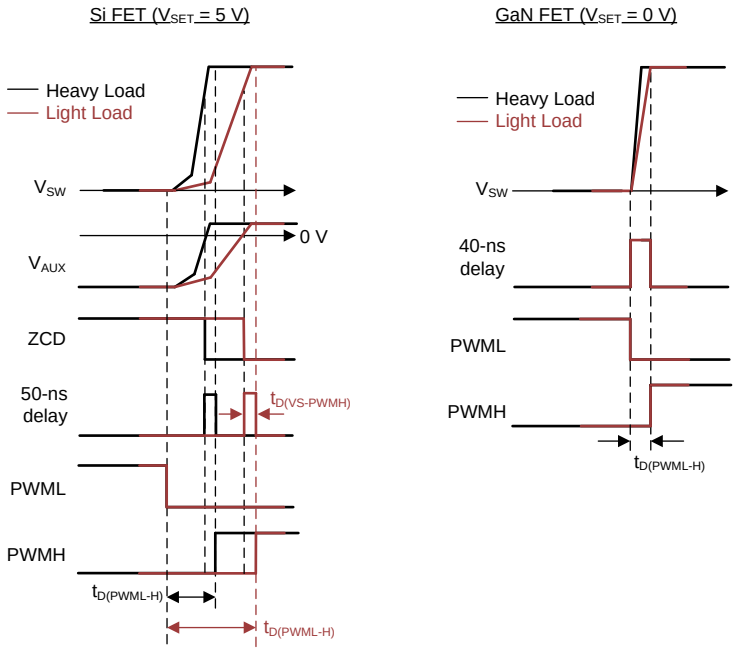


図 22. $t_{D(PWML-H)}$ Control Optimized for GaN and Si FETs

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Device Functional Modes (continued)

7.4.3 Control Law across Entire Load Range

UCC28780 contains four modes of operation summarized in 表 1. Starting from heavier load, the AAM mode forces PWML and PWMH into complementary switching with ZVS tuning enabled. ABM mode generates a group of PWML and PWMH pulses as a burst packet, and adjusts the burst off-time to regulate the output voltage. At the same time, the burst frequency variation is confined above 20kHz by adjusting the number of PWML and PWMH pulses per packet to mitigate audible noise and reduce burst output ripple. In LPM and SBP modes, PWMH and the ZVS tuning loop are disabled, so the converter operates in valley-switching.

表 1. Functional Modes

	MODE	OPERATION	PWMH	ZVS
AAM	Adaptive Amplitude Modulation	ACF operation with PWML and PWMH in complementary switching	Enabled	Yes
ABM	Adaptive Burst Mode	Variable f_{BUR} > 20 kHz, ACF operation in complementary switching	Enabled	Yes
LPM	Low Power Mode	Fix f_{BUR} ≈ 25 kHz, valley-switching	Disabled	No
SBP	StandBy Power	Variable f_{BUR} < 25 kHz, valley-switching	Disabled	No

図 23 addresses the critical parameter changes among the four operating modes, where V_{CST} is the peak current threshold compared with the current-sense voltage from CS pin, f_{SW} is the switching frequency of PWML, f_{BUR} is the burst frequency, and N_{SW} is the pulse number of PWML per burst packet. The following section explains the detailed operation of each mode.

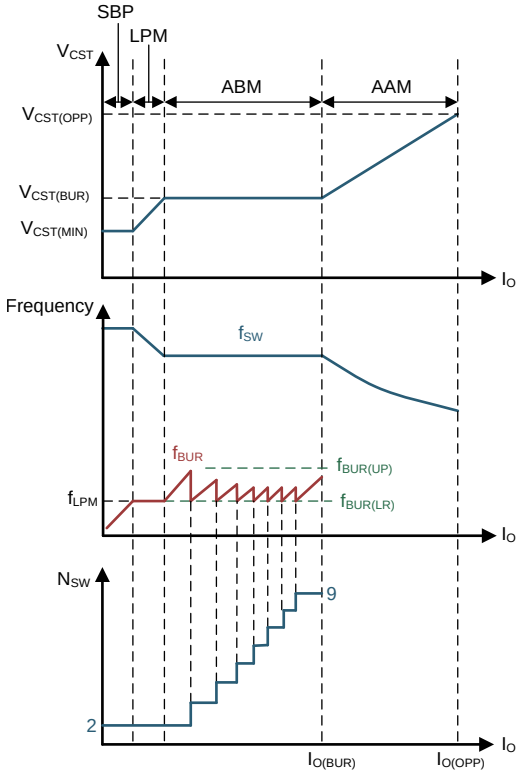


図 23. Control Law Over Entire Load Range

7.4.4 Adaptive Amplitude Modulation (AAM)

The switching pattern in AAM forces PWML and PWMH to alternate in a complementary fashion with dead-time in between, as shown in 図 24. As the load current reduces, the negative magnetizing current (I_{M-}) stays the same, while the positive magnetizing current (I_{M+}) reduces by the internal peak current loop to regulate the output voltage. I_{M+} generates a current-feedback signal (V_{CS}) on CS pin through a current-sense resistor (R_{CS}) in series with Q_L, and a peak current threshold (V_{CST}) in the current loop controls the peak current variation. Due to the nature of transition-mode (TM) operation, lowering the peak current with lighter load conditions results in higher switching frequency. When the load current increases to an over-power condition ($I_{O(OPP)}$) where V_{CST} correspondingly reaches an OPP threshold ($V_{CST(OPP)}$) of the peak current loop, the OPP fault response will be triggered after a 160-ms timeout. The RUN signal stays high in AAM, so the half-bridge driver remains active.

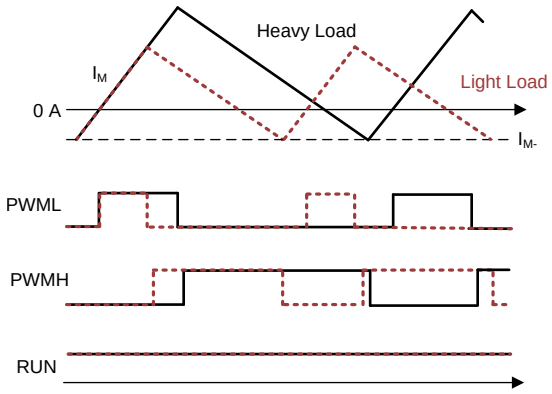


図 24. PWM Pattern in AAM

7.4.5 Adaptive Burst Mode (ABM)

As the load current reduces to $I_{O(BUR)}$ where V_{CS} reaches to $V_{CST(BUR)}$ threshold, ABM starts and V_{CS} is clamped. The peak magnetizing current and the switching frequency (f_{SW}) of each switching cycle are fixed for a given input voltage level. $V_{CST(BUR)}$ is programmed by the BUR pin voltage (V_{BUR}). The PWM pattern of ABM is shown in 図 25. When RUN goes high, a delay time between RUN and PWML ($t_{D(RUN-PWML)}$) is given to allow both the gate driver and the UCC28780 time to wake up from a wait state to a run state. PWML is set as the first pulse to build up the bootstrap voltage of the high-side driver before PWMH starts switching. The first PWML pulse turns on Q_L close to a valley point of the DCM ringing on the switch-node voltage (V_{SW}) by sensing the condition of zero crossing detection (ZCD) on the auxiliary winding voltage (V_{AUX}). The following switching cycles operate in a ZVS condition, since PWMH is enabled. As the number of PWML pulses (N_{SW}) in the burst packet reaches its target value, the RUN pin pulls low after the ZCD of the last switching cycle is detected, and forces the half-bridge driver and UCC28780 into a wait state for the quiescent current reduction of both devices. In this mode, the minimum off-time of the RUN signal is 2.2 µs and the minimum on-time of PWML is limited to the leading-edge blanking time (t_{CSLEB}) of the peak current loop. However, more grouped pulses means more risk of higher output ripple and higher audible noise. The following equation estimates how burst frequency (f_{BUR}) varies with output load and other parameters.

$$f_{BUR} = \frac{I_O}{I_{O(BUR)}} \frac{f_{SW}}{N_{SW}} \tag{11}$$

As $I_O < I_{O(BUR)}$, f_{BUR} can become lower than the audible noise range if N_{SW} is fixed. In ABM, N_{SW} is modulated to ensure f_{BUR} stays above 20 kHz by monitoring f_{BUR} in each burst period. As I_O reduces, f_{BUR} becomes lower and reaches a predetermined low-level frequency threshold ($f_{BUR(LR)}$) of 25 kHz. The ABM loop commands N_{sw} of both PWML and PWMH to be reduced by one pulse to maintain f_{BUR} above $f_{BUR(LR)}$. At the same time, the burst frequency ripple on the output voltage reduces as N_{SW} drops with the load reduction. As I_O increases, f_{BUR} becomes higher and reaches a predetermined high-level frequency threshold ($f_{BUR(UP)}$) of 34 kHz. The ABM loop commands N_{SW} to be increased by one pulse to push f_{BUR} back below $f_{BUR(UP)}$.

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This algorithm maximizes the number of pulses in each burst packet to improve light-load efficiency, while also limiting the burst output ripple and audible noise. As I_O moves below the boundary between AAM and ABM, the maximum N_{SW} is nine and the minimum N_{SW} is two. As I_O is close to the boundary between AAM and ABM, the maximum N_{SW} can be higher than nine, to provide a smoother mode transition. When the load slightly increases in this boundary, more than nine pulses are generated in a burst packet as 図 26 shows. f_{BUR} starts to move lower than 20kHz. The burst pattern with disordered N_{SW} and inconsistent f_{BUR} among the asymmetric burst packets generates a frequency spreading effect to weaken the strength of potential audible noise, when the controller operates in the transition region. It is found that dip varnishing the transformer is a very effective way to mitigate the minor audible noise around the mode transition. ABM operation with lower peak magnetizing current through lower BUR-pin voltage can also help to minimize the potential audible noise. Generally speaking, entering ABM at around 50 to 60% of output load and using a varnished transformer provides good balance between the light-load efficiency and smooth mode transitions with minimal audible noise.

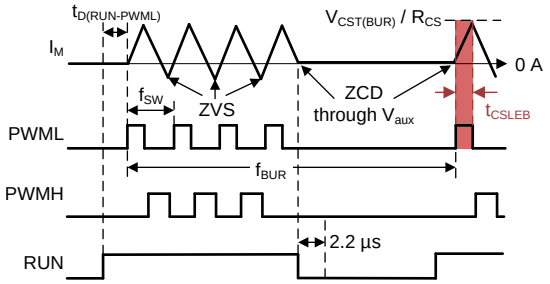


図 25. PWM Pattern in ABM

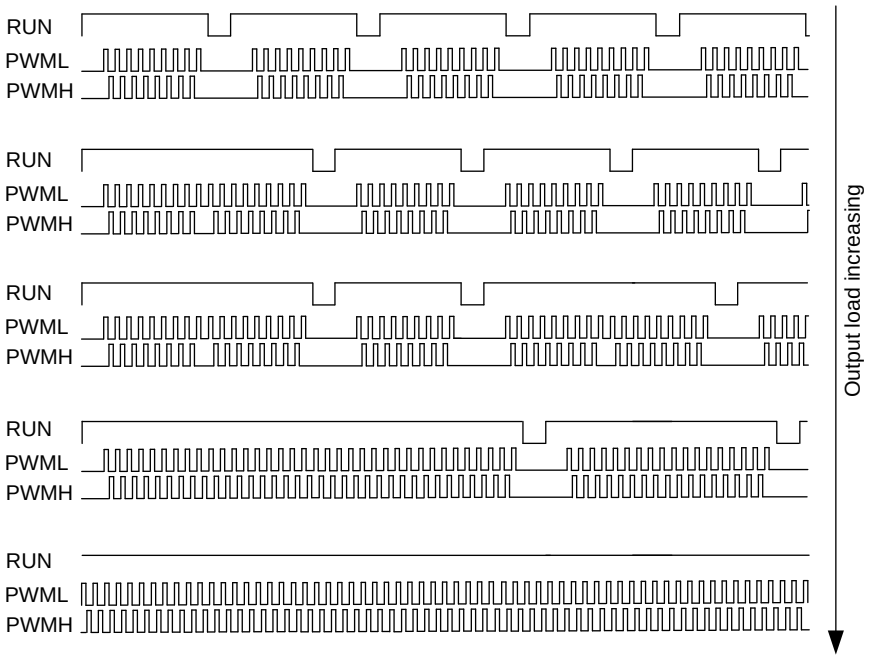


図 26. Mode Transition Behavior between AAM and ABM

7.4.6 Low Power Mode (LPM)

As N_{SW} drops to two in ABM and the condition of f_{BUR} less than $f_{BUR(LR)}$ is qualified under two consecutive burst periods, UCC28780 enters into LPM mode and disables PWMH. The purpose of LPM is to provide a soft peak current transition between $V_{CST(BUR)}$ and $V_{CST(MIN)}$. LPM fixes N_{SW} at two and sets f_{BUR} equal to f_{LPM} of 25 kHz. In LPM mode, V_{CST} is controlled to regulate the output voltage. At the start of each burst packet, after RUN pulls high, $t_{D(RUN-PWML)}$ is used to wake up both the gate driver and UCC28780. With PWMH disabled, the two PWML pulses turn on Q_L close to valley-switching by sensing ZCD. When ZCD is detected again at the end of the second pulse, the RUN pin goes low and the UCC28780 enters its low-power wait state. In LPM mode, the

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minimum on-time of PWML can be further reduced to $t_{ON(MIN)}$, to allow the peak magnetizing current to be reduced beyond the level limited by t_{CSLEB} of the peak current loop. In this condition, operation of the LPM control loop is changed from a current-mode control to a voltage-mode control, so the on-time adjustment of PWML is not limited to t_{CSLEB}. With this feature, before f_{BUR} starts to fall below f_{LPM} and enters the audible frequency range of SBP mode, the peak current is low enough to limit the magnitude of audible excitation.

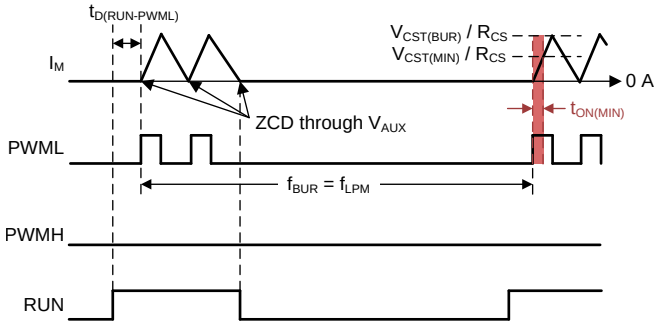


図 27. PWM Pattern in LPM

7.4.7 Standby Power Mode (SBP)

As V_{CST} drops to $V_{CST(MIN)}$, UCC28780 enters into SBP mode and PWMH continues to stay disabled. The purpose of SBP is to lower f_{BUR} in order to minimize standby power. SBP fixes N_{SW} at two and V_{CST} to $V_{CST(MIN)}$, while the burst off-time is adjusted to regulate the output voltage. As f_{BUR} is well below f_{LPM}, the switching-related loss can be minimized. In addition, lowering f_{BUR} forces both the gate driver and UCC28780 to remain in wait states longer to minimize the static power loss. The equivalent static current of the UCC28780 in SBP can be represented as

$$I_{VDD(SBP)} = (I_{RUN} - I_{WAIT})\left(\frac{2}{f_{SW(SBP)}} + t_{D(RUN-PWML)}\right) f_{BUR} + I_{WAIT} \quad (12)$$

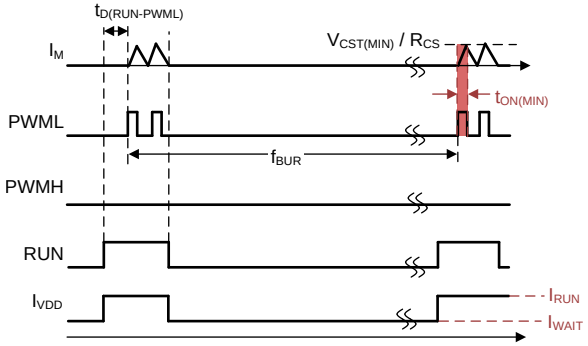


図 28. PWM Pattern in SBP

7.4.8 Startup Sequence

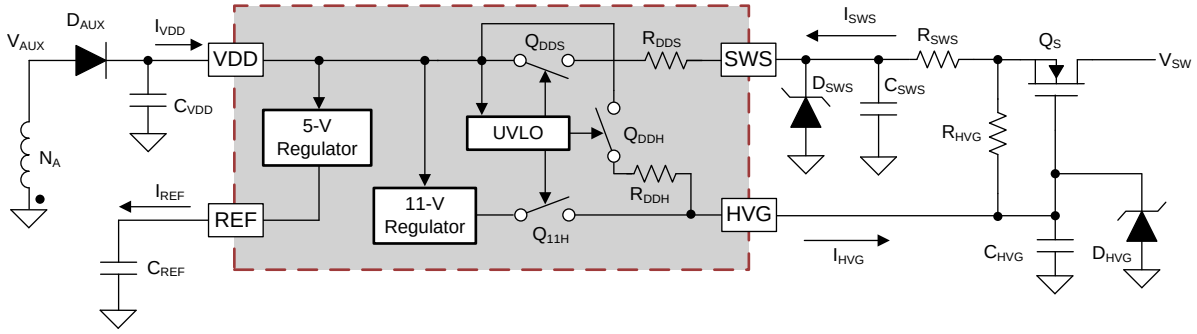
図 29 shows the simplified block diagram related with the VDD startup function of UCC28780, and 図 30 addresses the startup sequence. The detailed description on the startup waveforms is :

1. Time interval A: The UVLO circuit commands the two internal power-path switches (Q_{DDS} and Q_{DDH}) to build connections among SWS, VDD, and HVG pins through two serial current-limiting resistors (R_{DDS} and R_{DDH}). The depletion-mode MOSFET (Q_S) starts sourcing charge current (I_{SWS}) safely from the high-voltage switch-node voltage (V_{SW}) to the VDD capacitor (C_{VDD}). Before V_{VDD} reaches 1 V, I_{SWS} is limited by the high-resistance R_{DDS} of 12 kΩ to prevent potential device damage if C_{VDD} or VDD pin is shorted to ground.
2. Time interval B: After V_{VDD} rises above 1 V, R_{DDS} is reduced to a smaller resistance of 1 kΩ. I_{SWS} is increased to charge C_{VDD} faster. The maximum charge current during VDD startup can be quantified by 式 7.
3. Time interval C: As V_{VDD} reaches $V_{VDD(ON)}$ of 17.5 V, the ULVO circuit turns-off Q_{DDS} to disconnect the source pin of Q_S to C_{VDD}, and turns-off Q_{DDH} to break the gate-to-source connection of Q_S, so Q_S loses its

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current-charge capability. V_{DD} then starts to drop, because the 5-V regulator on REF pin starts to charge up the reference capacitor (C_{REF}) to 5 V, which maximum charge current ($I_{SE(REF)}$) is self-limited at around 14 mA. After V_{REF} is settled, the UVLO circuit turns-on another power-path switch (Q_{11H}), so an internal 11-V regulator is connected to the HVG pin. The voltage on the HVG pin capacitor (C_{HVG}) starts to be discharged by the regulator.

4. Time interval D: During discharging C_{HVG} of the recommended 2.2 nF, the sink current of the 11-V regulator ($I_{SE(HVG)}$) is self-limited at around 90 μA, so it takes longer than 25 μs for settling to 11 V. If V_{HVG} reaches 11 V in less than 10 to 25 μs, the HVG pin open fault is triggered to protect the device. Once V_{HVG} is settled to 11 V without the fault event, RUN pin goes high and UCC28780 enters a run state with $I_{VDD} = I_{RUN}$.
5. Time interval E: There is a 2.2-μs delay from RUN going high to PWML starting to switch in order to wake-up the gate driver and UCC28780.
6. Time interval F: This is the soft-start region of peak magnetizing current. The first purpose is to limit the supply current if the output is short. The second purpose is to push the switching frequency higher than the audible frequency range during repetitive startup situations. At the beginning of V_O soft-start, the peak current is limited by two V_{CST} thresholds. The first V_{CST} startup threshold ($V_{CST(SM1)}$) is clamped at 0.28 V and the following second threshold ($V_{CST(SM2)}$) is 0.6 V. When $V_{CST} = V_{CST(SM1)}$, PWMH is disabled if the VS pin voltage (V_{VS}) < 0.28 V, and the first five PWML pulses are forced to stay at this current level. After V_{VS} exceeds 0.28 V and the first five PWML pulses are generated, the peak current threshold changes from $V_{CST(SM1)}$ to $V_{CST(SM2)}$. In case of the inability to build up V_O with $V_{CST(SM1)}$ at the beginning of the V_O soft-start due to excessively large output capacitor and/or constant-current output load, there is an internal time-out of 1ms to force V_{CST} to switch to $V_{CST(SM2)}$.
7. Time interval G: When V_{VS} rises above 0.6 V, V_{CST} is allowed to reach $V_{CST(MAX)}$ of 0.8 V, so the rising rate of V_O startup becomes faster. When PWML is in a high state, I_{VDD} can be larger than I_{RUN}, because the 5-V regulator provides the line-sensing current pulse (I_{VSL}) on the VS pin to sense V_{BULK} condition.
8. Time interval H: V_O and V_{CST} settle, and the auxiliary winding takes over the VDD supply. There is a switching ripple on C_{HVG} during PWML switching, due to the dV/dt coupling of V_{SW} through the junction capacitance of Q_S. UCC28780 provides an over-voltage protection on HVG pin to avoid the risk of high overshoot under high dV/dt conditions. The over-voltage threshold of HVG pin ($V_{HVG(OV)}$) is 13.8V.



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図 29. Functional Startup Block Diagram

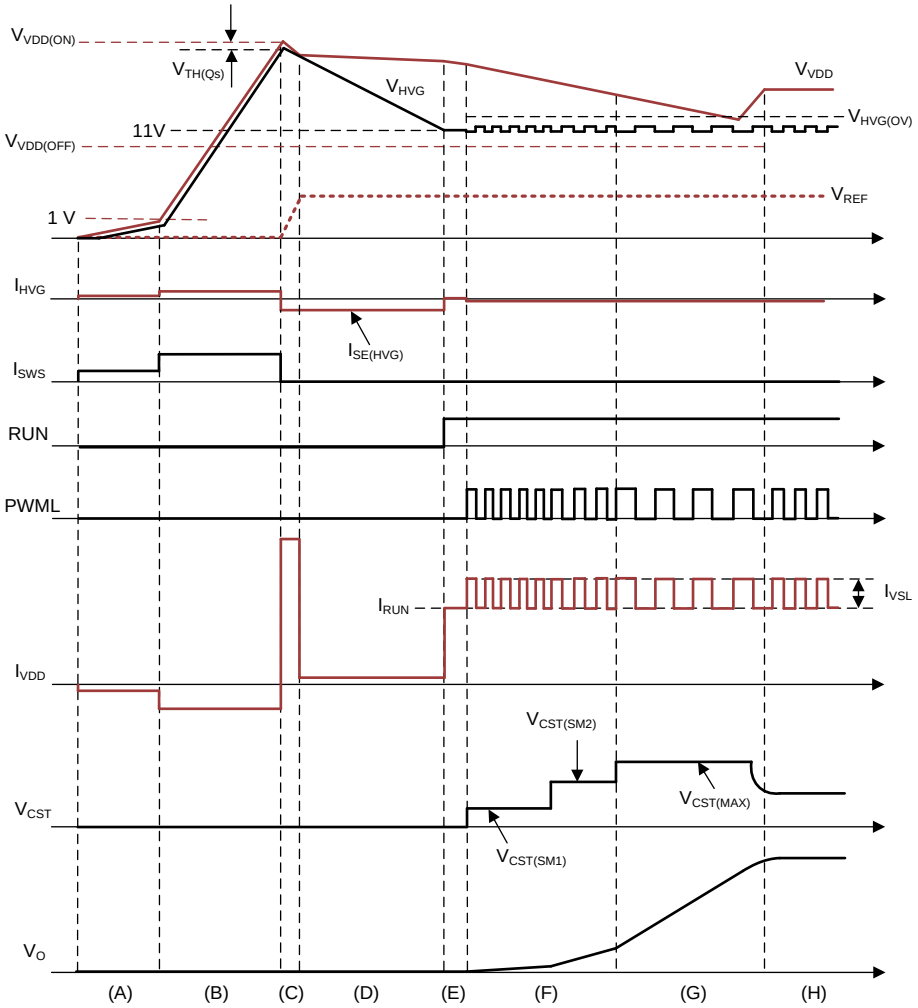


図 30. Startup Timing Waveforms

7.4.9 Survival Mode of VDD

When the output voltage overshoot occurs during step-down load transients, the V_O feedback loop commands the UCC28780 to stop switching quickly through increasing I_{FB}, in order to prevent additional energy from aggravating the overshoot. Since V_{VDD} keeps dropping during this time, the conventional way to prevent a controller from shutting down is to oversize the VDD capacitor so as to hold V_{VDD} above $V_{VDD(OFF)}$. Instead, UCC28780 is equipped with the survival-mode operation to hold V_{VDD} above $V_{VDD(OFF)}$ during the transient event, so the size of VDD capacitor can be significantly reduced and the PCB footprint for the auxiliary power can be minimized. Specifically, there is a ripple comparator to regulate V_{VDD} above a 11-V threshold, which is $V_{VDD(OFF)}$ plus $V_{VDD(PTC)}$ in the electrical table. The ripple regulator is enabled when the V_O feedback loop requests the UCC28780 to stop switching due to V_O overshoot.

The regulator initiates unlimited PWML pulses when V_{VDD} drops lower than 11 V, and stops switching after V_{VDD} rises above 11 V. Since V_{VDD} is lower than the reflected output voltage overshoot, most of the magnetizing energy is delivered to the auxiliary winding and brings V_{VDD} above the 11-V threshold quickly. After V_O moves back to the regulation level, V_O feedback loop forces the UCC28780 to begin switching again by reducing I_{FB}, and the PWML and PWMH pulses are then controlled by the normal operating mode.

To prevent the controller from getting stuck in survival mode continuously or toggling between SBP and survival mode at zero load, some guidelines on the auxiliary power delivery path to VDD can be considered:

1. The normal V_{VDD} level under regulated V_O must be away from the 11-V threshold.
2. VDD capacitor should not be over-sized, but designed just big enough to hold $V_{VDD} > V_{VDD(OFF)}$ under the

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longest V_O soft-start time.

3. The current-limiting resistor (R_{VDD1}) in series with the auxiliary rectifier diode (D_{AUX}) should not be too large, so the delivery path with lower series impedance can help the VDD capacitor charge faster.
4. Ensure good coupling between the auxiliary winding (N_{AUX}) and the secondary winding (N_S) of the transformer.

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7.4.10 System Fault Protections

The UCC28780 provides extensive protections on different system fault scenarios. The protection features are summarized in 表 2.

表 2. System Fault Protection

PROTECTION	SENSING	THRESHOLD	DELAY TO ACTION	ACTION
VDD UVLO	VDD voltage	$V_{VDD(OFF)} \le V_{VDD} \le V_{VDD(ON)}$	None	UVLO reset
Over-power protection (OPP)	CS voltage	$V_{CST(OPP)} \le V_{CST} \le V_{CST(MAX)}$	t_{OPP} (160 ms)	t_{FDR} restart (1.5s)
Peak current limit (PCL)	CS voltage	$V_{CST} \le V_{CST(MAX)}$		
Over-current protection (OCP)	CS voltage	$V_{CS} \ge V_{OCP}$	3 PWML pulses	t_{FDR} restart
Output short-circuit protection (SCP)	CS, VS, and VDD voltages	(1) $V_{VDD} = V_{VDD(OFF)}$ & $V_{CST} \ge V_{CST(OPP)}$; (2) $V_{VDD} = V_{VDD(OFF)}$ & $V_{VS} \le 0.6$ V	$\le t_{OPP}$	t_{FDR} restart
Output over-voltage protection (OVP)	VS voltage	$V_{VS} \ge V_{OVP}$	3 PWML pulses	t_{FDR} restart
Brown-in detection	VS current	$I_{VSL} \le I_{VSL(RUN)}$	4 PWML pulses	UVLO reset
Brown-out detection	VS current	$I_{VSL} \le I_{VSL(STOP)}$	t_{BO} (60ms)	UVLO reset
Over-temperature protection (OTP)	NTC voltage	$R_{NTC} \le R_{NTCTH}$	3 PWML pulses	UVLO reset until $R_{NTC} \ge R_{NTCR}$
Thermal shutdown	Junction temperature	$T_J \ge T_{J(STOP)}$	3 PWML pulses	UVLO reset

7.4.10.1 Brown-In and Brown-Out

The VS pin senses the negative voltage level of the auxiliary winding during the on-time of low-side switch (Q_L) to detect an under-voltage condition of the input AC line. When the bulk voltage (V_{BULK}) is too low, UCC28780 stops switching and no V_O restart attempt is made until the AC input line voltage is back into normal range. As Q_L turns on with PWML, the negative voltage level of auxiliary winding voltage (V_{AUX}) is equal to V_{BULK} divided by primary-to-auxiliary turns ratio (N_{PA}) of the transformer, which is N_P / $N_{A,}$. During this time, the voltage on VS pin is clamped to about 250 mV below GND. As a result, V_{AUX} can create a line-sensing current (I_{VSL}) out of the VS pin flowing through the upper resistor of the voltage divider on VS pin (R_{VS1}). With I_{VSL} proportional to V_{BULK}, it can be used to compare against two under-voltage thresholds, $I_{VSL(RUN)}$ and $I_{VSL(STOP)}$.

The target brown-in AC voltage ($V_{AC(BI)}$) can be programmed by the proper selection of R_{VS1}. For every UVLO cycle of VDD, there are at least four initial test pulses from PWML to check I_{VSL}condition. I_{VSL} of the first test pulse is ignored. If $I_{VSL} \le I_{VSL(RUN)}$ is valid for the rest three consecutive test pulses, the controller stops switching, the RUN pin goes low, and a new UVLO start cycle is initiated after V_{VDD} reaches $V_{VDD(OFF)}$. On the other hand, if $I_{VSL} > I_{VSL(RUN)}$ occurs, V_O soft start sequence is initiated.

$$R_{VS1} = \frac{V_{AC(BI)}\sqrt{2}}{N_{PA} \times I_{VSL(RUN)}} = \frac{N_A}{N_P}\frac{V_{AC(BI)}\sqrt{2}}{365\mu A} \tag{13}$$

The brown-out AC voltage ($V_{AC(BO)}$) is set internally by around 83% of $V_{AC(BI)}$, which provides enough hysteresis to compensate for possible sensing errors through the auxiliary winding. A 60-ms timer (t_{BO}) is used to bypass the effect of line ripple content on the I_{VSL} sensing. Only when the $I_{VSL} \le I_{VSL(STOP)}$ condition lasts longer than 60 ms, i.e. typically three line cycles of 50 Hz, the brown-out fault is triggered. The fault is reset after V_{VDD} reaches $V_{VDD(OFF)}$. 図 31 shows an example of the timing sequence of brown-in and brown-out protections.

$$V_{AC(BO)} = \frac{I_{VSL(STOP)}}{I_{VSL(RUN)}} V_{AC(BI)} = 0.83 \times V_{AC(BI)} \tag{14}$$

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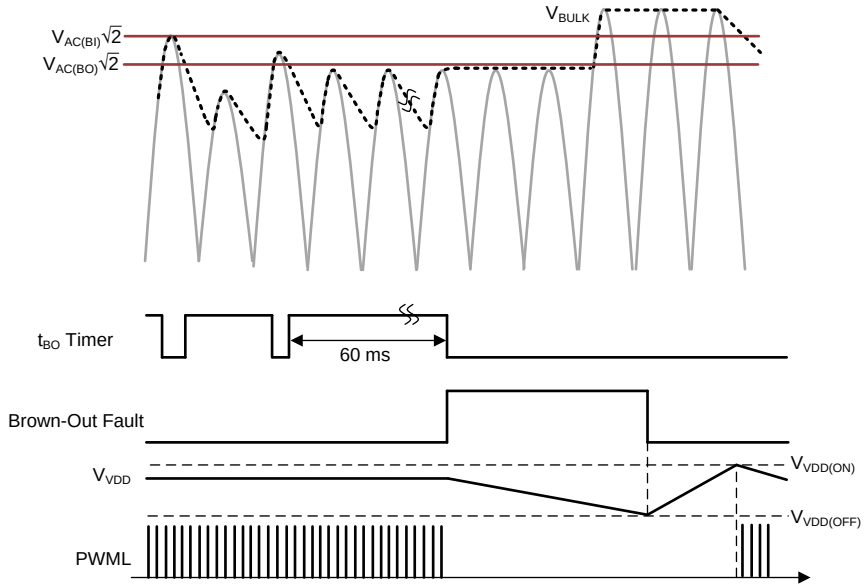


図 31. Timing Diagram of Brown In/Out

7.4.10.2 Output Over-Voltage Protection

VS pin senses the positive voltage level of the auxiliary winding voltage (V_{AUX}) to detect an over-voltage condition of V_O. When an OVP event is triggered, UCC28780 stops switching and there is a 1.5-s fault recovery time (t_{FDR}) before any V_O restart attempt is made. As Q_L turns off, the settled V_{AUX} is equal to (V_O+V_F) x N_{AS}, where N_{AS} is the auxiliary-to-secondary turns ratio of the transformer, N_A / N_S, and V_F is the forward voltage drop of the secondary-side rectifier. The VS pin senses V_{AUX} through a voltage divider formed by R_{VS1} and R_{VS2}. The pin voltage (V_{VS}) is compared with an internal OVP threshold (V_{OVP}). If $V_{VS} \geq V_{OVP}$ condition is qualified for three consecutive PWML pulses, the controller stops switching, brings RUN pin low, and initiates the 1.5-s time delay. During this long delay time, only the UVLO-cycle of V_{VDD} is active, and there are no test pulses of PWML. After the 1.5-s timeout is completed and V_{VDD} reaches the next $V_{VDD(OFF)}$, a normal start sequence begins. The calculation of R_{VS2} is

$$R_{VS2} = \frac{R_{VS1} \times V_{OVP}}{N_{AS} \times (V_{O(OVP)} + V_F) - V_{OVP}} = \frac{R_{VS1} \times 4.5V}{(N_A / N_S)(V_{O(OVP)} + V_F) - 4.5V} \quad (15)$$

The long t_{FDR} timer helps to protect the power stage components from the large current stress during every restart. After OVP is triggered, V_O may be brought down quickly by the output load current. If OVP were reset directly after one UVLO cycle of VDD without the 1.5-s delay, the first PWMH pulse turns on Q_H under the condition of a large voltage difference between the high clamp capacitor voltage (V_{CLAMP}) and the low reflected voltage. A large current can flow through the clamp switch (Q_H) and secondary rectifier. Therefore, the 1.5-s timer of UCC28780 allows V_{CLAMP} to drop to a lower voltage level through a bleeding resistor (R_{BLEED}) in parallel with C_{CLAMP} before the next V_O restart attempt, such that the current stress can be minimized. A large R_{BLEED} can be used with the long time-out to minimize the impact on standby power. For example, to discharge V_{CLAMP} to 10% of its normal level in 1.5 s, only 3 mW of additional standby power is added with R_{BLEED} = 2.8 MΩ and C_{CLAMP} = 220 nF. 図 32 illustrates the timing sequence as V_{CLAMP} is discharged to a residual voltage ($V_{RESIDUAL}$) in 1.5 s. R_{BLEED} also helps to reduce the voltage overcharge on the clamp capacitor in LPM and SBP modes in which PWMH is disabled, so the voltage stress in the passive-clamp operation can be controlled.

During LPM to ABM mode transition, it is possible to falsely trigger OVP if the setting does not have enough design margin. In LPM mode with a disabled PWMH, the leakage energy of the transformer charges V_{CLAMP} higher than the reflected voltage. When the controller enters into ABM and the PWMH is enabled, the active-clamp circuit of ACF needs to take some time to balance the voltage difference, depending on the clamp capacitor value. As a result, V_{AUX} can sense the higher V_{CLAMP} condition during the voltage balancing and the controller may treat this as an OVP event, even though V_O still stays in regulation and does not reach the actual OVP point. It may only happen with a large C_{CLAMP} design, so slightly increasing the OVP setting can resolve the problem.

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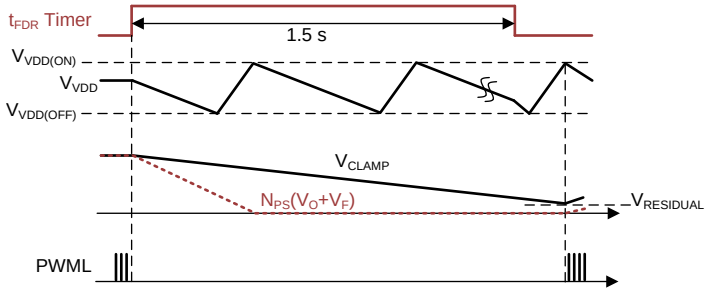


図 32. Timing Diagram of C_{CLAMP} Discharging During 1.5-s Recovery Time

7.4.10.3 Over-Temperature Protection

The UCC28780 uses an external NTC resistor (R_{NTC}) tied to the NTC pin to program a thermal shutdown temperature near the hotspot of the converter. The NTC shutdown threshold (V_{NTCTH}) of 1 V with an internal 105-μA current source flowing through R_{NTC} results in a 9.5-kΩ thermistor shutdown threshold. If the NTC resistance stays lower than 9.5 kΩ for more than three consecutive PWML pulses, an OTP fault event is triggered, and the 1-V threshold is increased to 2.25 V. The NTC resistance has to increase above 21.7 kΩ to reset the OTP fault. This threshold change provides a safe temperature hysteresis to help the hot-spot temperature cool down before the next V_O restart attempt, reducing the thermal stress to the components. This pin can also be used as an electrical shutdown function by shorting this pin with a controlled switch to GND. With the pin shorted to GND, V_{VDD} performs UVLO cycling, and there is at least three consecutive PWML pulses generated to check the state. The NTC pin can be left floating or tied to the REF pin if not used.

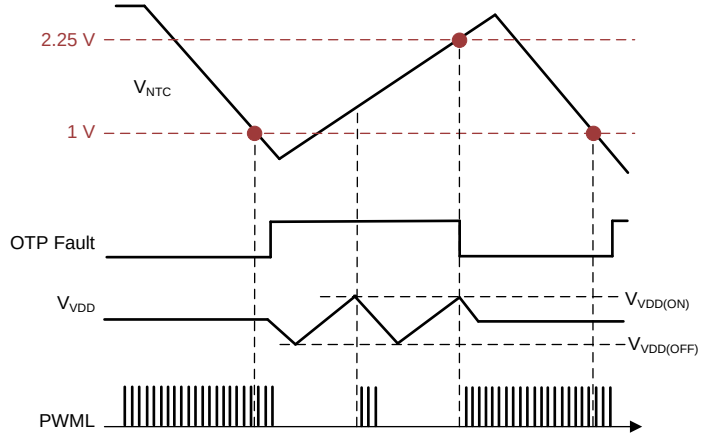


図 33. Timing Diagram of OTP with NTC

7.4.10.4 Programmable Over-Power Protection

The over-power protection (OPP) enables the ACF to operate in an over-power condition for a limited amount of time, so the UCC28780 can support a power stage design with peak power requirements. As shown in 図 34, when V_{CST} is higher than the threshold voltage of the OPP curve ($V_{CST(OPP)}$), a 160-ms timer starts. If V_{CST} remains higher than $V_{CST(OPP)}$ continuously for 160 ms, the long 1.5-s timer starts and the controller stays in fault state without switching. This long recovery time reduces the average current during a sustained over-power event. The system benefits includes the reduction of thermal stress in high density adapters and the protection of its output cable.

The OPP function uses I_{VSL} as a line feed-forward signal to vary $V_{CST(OPP)}$ depending on V_{BULK}, in order to make the OPP trigger point constant over a wide line voltage range. The UCC28780 allows programing of the OPP curve by adding a line-compensation offset voltage on the CS pin through a resistor (R_{OPP}) connected between the CS pin and current-sense resistor (R_{CS}). An internal current source flowing out of CS pin creates the offset voltage on R_{OPP}. This current level is equal to I_{VSL} divided by a constant gain of K_{LC}. As R_{OPP} increases, the OPP trigger point becomes lower at high line, so lower peak magnetizing current is allowed to run continuously.

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The highest threshold of OPP curve ($V_{CST(OPP1)}$) of 0.6 V helps to determine R_{CS} value at $V_{BULK(MIN)}$.

$$R_{CS} = \frac{V_{CST(OPP1)}}{\frac{P_{O(OPP)}}{V_{BULK(MIN)}\eta}\frac{2}{D_{MAX}} - \frac{V_{BULK(MIN)}t_{D(CST)}}{L_M}} \quad (16)$$

where $P_{O(OPP)}$ is the output power that triggers OPP, and $t_{D(CST)}$ is the sum of all delays in the peak current loop which contributes additional peak current overshoot. $t_{D(CST)}$ consists of propagation delay of the low-side driver, current sense filter delay (R_{OPP} x C_{CS}), internal CS comparator delay ($t_{D(CS)}$), and nonlinear capacitance delay of Q_L. After R_{CS} is determined, R_{OPP} can be adjusted to keep a similar OPP point at highest line. Note that setting the OPP trigger point too far away from the full power may introduce more challenge on the thermal design, since the converter runs continuously with more power as long as the corresponding peak current is slightly less than OPP threshold.

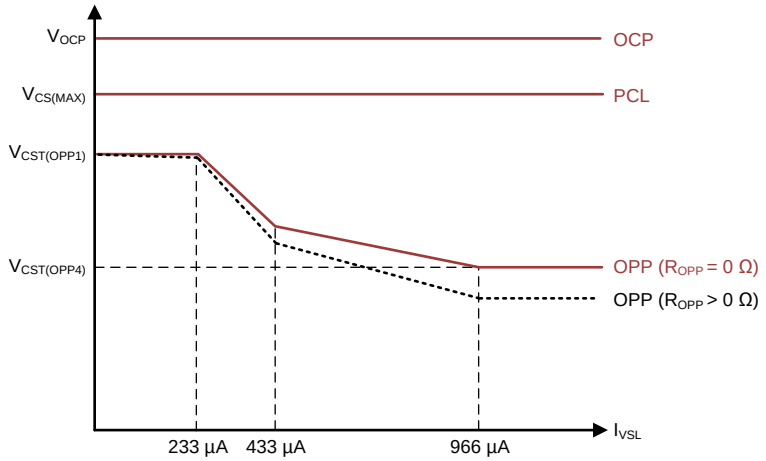


図 34. CS-Pin Related Faults

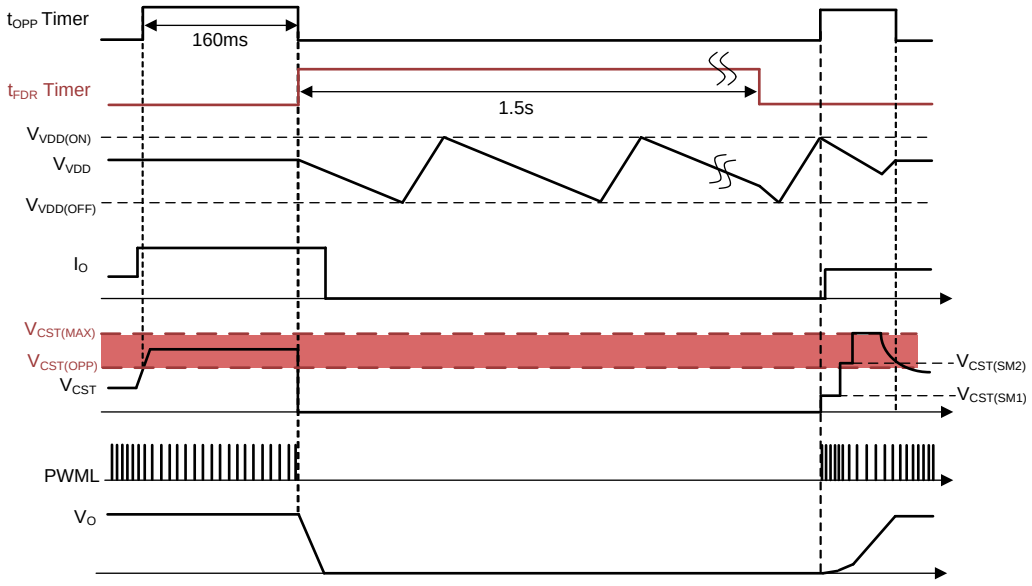


図 35. Timing Diagram of OPP

7.4.10.5 Peak Current Limit

The peak current threshold of the OPP curve is used to initiate the 160-ms timer, while the peak current limit (PCL) determines the highest controllable peak current of the peak current loop, $V_{CST(MAX)}$ = 0.8 V. In other words, this feature provides the highest "short duration" peak power ($P_{O(MAX)}$) that the converter can reach. For example, to supply a highest peak power of 150%, R_{CS} should be chosen to ensure that the peak current at 150% load and $V_{BULK(MIN)}$ must not be above $V_{CST(MAX)}$. Then, the threshold of the OPP power ($P_{O(OPP)}$) can be programmed to around 112% to support 150% peak power design, based on the following equation. Additionally, before V_O reaches steady state during a V_O soft-start, the highest V_{CST} can also reach to $V_{CST(MAX)}$. The transformer must have enough design margin separating its maximum flux density from the saturation limit of the core material under the peak current level in PCL.

$$P_{O(OPP)} = \frac{V_{CST(OPP1)}}{V_{CST(MAX)}} P_{O(MAX)} = \frac{0.6V}{0.8V} P_{O(MAX)} \tag{17}$$

7.4.10.6 Output Short-Circuit Protection

When an output short-circuit is applied, the peak current reaches the PCL limit and triggers the 160-ms OPP fault timer. During this event, the VDD power supply is lost due to the auxiliary winding voltage being close to 0 V. Without additional short-circuit detection, if V_{VDD} reaches $V_{VDD(OFF)}$ before the 160-ms timeout, the 1.5-s recovery time for the OPP fault cannot be triggered but only a UVLO recycle is performed. To remedy this scenario, as V_{VDD} reaches $V_{VDD(OFF)}$, UCC28780 checks two additional parameters to identify the short-circuit event at the output, and initiates the 1.5-s recovery without waiting for 160 ms to expire. Specifically, when V_{VDD} reaches $V_{VDD(OFF)}$, if either V_{CST} is greater than the OPP threshold ($V_{CST(OPP)}$) or the VS-pin voltage is less than 0.6 V, the 1.5-s recovery delay is initiated. With this additional layer of intelligence, the average load current during continued short-circuit event can be greatly reduced, and thus also the thermal stress on the power supply.

7.4.10.7 Over-Current Protection

The UCC28780 operates with cycle-by-cycle primary-peak current control. The normal operating range of the CS pin is 0.15 V to 0.8 V. If the CS-pin voltage exceeds the 1.2-V over-current level, any time after the internal leading edge blanking time (t_{CSLEB}) and before the end of the transformer demagnetization, for three consecutive PWML cycles, the device stop switching, RUN pin goes low, and 1.5-s recovery time is initiated. Similar to OVP, OPP, and SCP, only the UVLO-cycle of VDD is active, there are no test PWML pulses at all. After the 1.5-s time-out is completed and V_{VDD} reaches the next $V_{DD(OFF)}$, a normal start sequence begins.

7.4.10.8 Thermal Shutdown

The internal over-temperature shutdown threshold is higher than 125°C. If the junction temperature of the device reaches this threshold, the device initiates a UVLO reset and re-start fault cycle. If the temperature is still high at the end of the UVLO cycle, the protection cycle repeats. This internal protection is not suitable to substitute for the NTC for the hotspot temperature protection. The NTC thermistor can provide more accurate and remote temperature sensing with less compromise on PCB layout.

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7.4.11 Pin Open/Short Protections

As summarized in 表 3, UCC28780 strengthens the protections of several critical pins under open and short conditions, such as CS, HVG, RDM and RTZ pins.

表 3. Protections for Open and Short of Critical Pins

PROTECTION	SENSING	CONDITION	DELAY TO ACTION	ACTION
CS pin short	PWML on-time at first PWML pulse only	> 2 µs (V_{SET} = 5 V)	none	t_{FDR} restart (1.5 s)
		> 2 µs (V_{SET} = 0 V, $R_{RDM} \geq R_{RDM(TH)}$)		
		> 1 µs (V_{SET} = 0V, $R_{RDM} < R_{RDM(TH)}$)		
CS pin open	CS voltage	$V_{CS} \geq V_{OCP}$	3 PWML pulses	t_{FDR} restart (1.5 s)
HVG pin open	HVG voltage at $UVLO_{ON}$	V_{HVG} drops to 12 V within 10 µs	none	UVLO reset
HVG pin over voltage	HVG voltage	$V_{HVG} \geq V_{HVG(OV)}$	3 PWML pulses	UVLO reset
RDM pin short	RDM current at $UVLO_{ON}$	V_{RDM} = 0 V, self-limited I_{RDM}	none	UVLO reset
RDM pin open	RDM current at $UVLO_{ON}$	RDM = Open	none	UVLO reset
RTZ pin short	RTZ current at $UVLO_{ON}$	V_{RTZ} = 0 V, self-limited I_{RTZ}	none	UVLO reset
RTZ pin open	RTZ current at $UVLO_{ON}$	RTZ = Open	none	UVLO reset

7.4.11.1 Protections on CS pin Fault

UCC28780 identifies a fail-short event on the CS pin by monitoring the on-time pulse width of the first PWML pulse after V_{VDD} startup is completed. As shown in 図 30, the normal first on-time pulse width should be limited by the clamped $V_{CST(SM1)}$ level of 0.28 V and the rising slope of the current-loop feedback signal from the current-sense resistor (R_{CS}) to the CS pin. When the current feedback path is gone due to a CS pin short to GND, the peak magnetizing current increases and potentially can damage the power stage. Therefore, a maximum on-time of the first PWML pulse under V_{SET} = 5 V, t_{CSF1} of 2 µs in the electrical table, is used to limit the first peak-current stress of the silicon-based converter and then will trigger a CS pin short protection which initiates the t_{FDR} recovery of 1.5 s.

Additionally, t_{CSF0} in the electrical table confines the maximum on-time of the first PWML pulse on the GaN-based converter with V_{SET} = 0 V. There are two corresponding values based on two predetermined ranges of the RDM pin setting in order to provide the protection over a wider switching frequency range. Specifically, t_{CSF0} is set at 2 µs with R_{RDM} higher than the $R_{RDM(TH)}$ threshold of 50 kΩ, while t_{CSF0} is reduced to 1 µs under $R_{RDM} < R_{RDM(TH)}$. Since a GaN-based converter is capable of operating at higher switching frequency by lowering the magnetizing inductance (L_M), it is possible that the peak current can increase higher than a lower switching-frequency design under the same $V_{CST(SM1)}$ level and same on-time of PWML. The RDM pin can provide a good indication on the switching frequency range of a GaN power stage, since the lower L_M requires smaller R_{RDM} setting. With a different t_{CSF0} setting, the CS pin fault adapts to a wide switching frequency range.

Unlike a CS pin short protection which senses the first on-time pulse width of PWML only, CS pin open protection monitors the fail-open condition cycle-by-cycle. An internal 4-µA current source out of the CS pin is used to pull the CS pin voltage up to 3.3 V as the CS pin exhibits high impedance during a fail-open condition. When the CS voltage is higher than the 1.2-V threshold of the OCP limit and lasts for three consecutive PWML pulses, the CS pin open protection is triggered which initiates the 1.5-s recovery.

7.4.11.2 Protections on HVG pin Fault

As shown in 図 30, after V_{VDD} reaches $V_{VDD(ON)}$, an internal 11-V regulator on the HVG pin should force V_{HVG} back to the regulation level before PWML starts switching. If the recommended HVG-pin capacitor (C_{HVG}) of 2.2 nF and the connection to the depletion-mode MOSFET (Q_S) are in place, the settling time of V_{HVG} to 11 V is much longer than 10 µs with a limited sink current of the regulator ($I_{SE(HVG)}$) to discharge C_{HVG}.

The first fault scenario is that if C_{HVG} is too small, or the HVG pin is open, the pin is not able to control Q_S correctly for the high-voltage sensing function of ZVS control, so no switching action will be performed. When either two situations happen, V_{HVG} settles to 11 V very quickly instead. Therefore, after a 10-µs delay from the instance of V_{VDD} reaching $V_{VDD(ON)}$, UCC28780 checks if V_{HVG} is below 12 V for the pin-fault detection, and then performs one UVLO cycle of VDD directly without switching as the protection response. The above protection is

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to prevent the controller from generating PWM signals. However, when the HVG pin is open and disconnected from the Q_S gate, the source voltage of Q_S keeps increasing until the TVS on the SWS pin (D_{SWS}) starts to clamp the voltage continuously. To shrink the size of D_{SWS} without incurring too much thermal stress in the small package in this fault condition, it is highly recommended that a small Zener diode (D_{HVG}) between Q_S gate to ground should be used to limit the Q_S source voltage. Same as D_{SWS}, D_{HVG} should be higher than $V_{VDD(ON)}$, so as to prevent interference with normal VDD startup.

The second fault scenario is the over-voltage condition of HVG pin after the converter starts switching. When the switch-node voltage (V_{SW}) rises with a high dV/dt condition, there is a charge current flowing through the junction capacitance of Q_S, and part of the current can charge up C_{HVG}. If the overshoot is too large, the voltage on the SWS pin also increases due to the nature of the depletion-mode MOSFET operation. UCC28780 detects the overshoot event on HVG pin with an over-voltage threshold ($V_{HVG(OV)}$) of 13.8V cycle-by-cycle. When V_{HVG} is higher than $V_{HVG(OV)}$ for three consecutive PWML pulses, the HVG over-voltage protection is triggered which performs one UVLO cycle of VDD.

The third fault scenario is an HVG pin short event at the beginning of VDD startup, and Q_S is not able to charge up the VDD capacitor to $V_{DD(ON)}$, so there is no chance to enable the controller.

7.4.11.3 Protections on RDM and RTZ pin Faults

Since RDM and RTZ pins are the critical programming pins for ZVS control, UCC28780 offers both open and short protections to those pins. After V_{VDD} reaches $V_{VDD(ON)}$, a fixed voltage level is applied to the pin and the corresponding current level flowing out of the pin is sensed to detect the pin fault event. As a result, too small of a current represents the pin-open state, and too large of a current represents the pin-short state where the short current level is self-limited. When the fault event is identified, one UVLO cycle of VDD is triggered as the protection response.

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8 Application and Implementation

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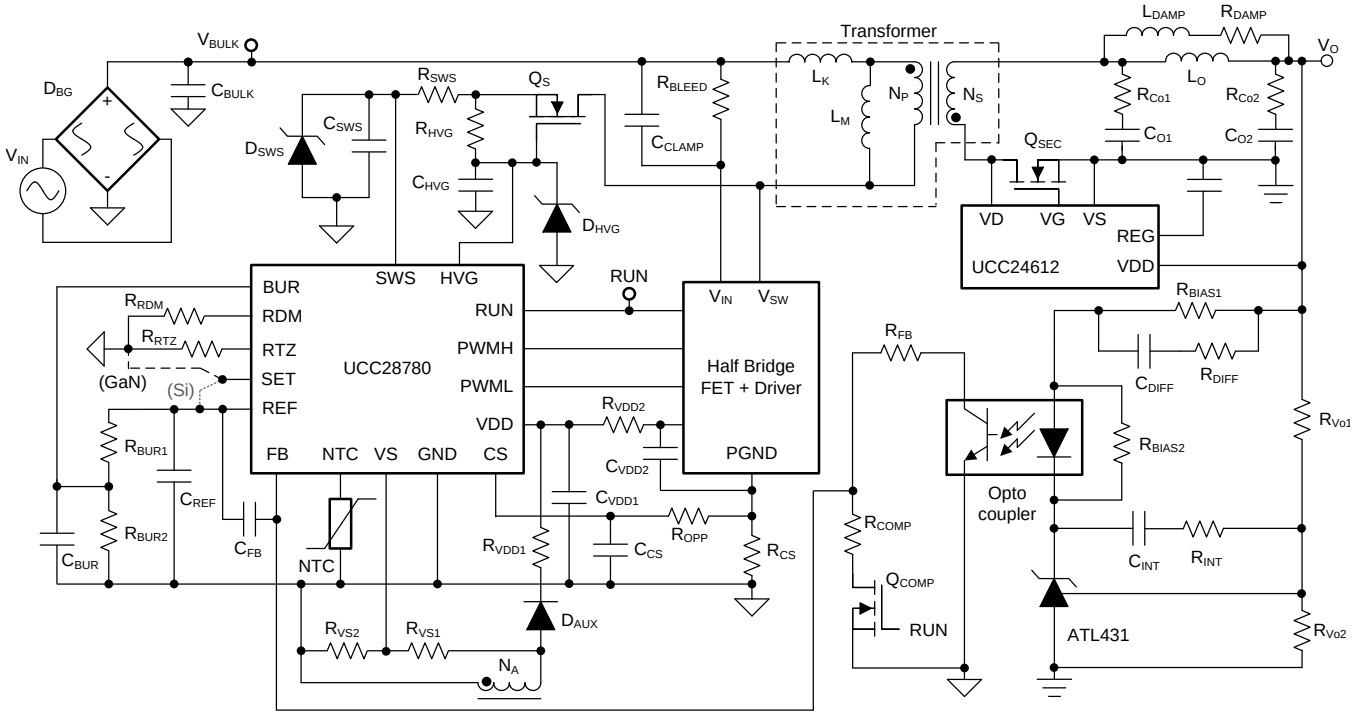
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

A typical application of a high-frequency active-clamp AC-to-DC flyback converter is to enable high-density AC-to-DC power supply design which complies with stringent global efficiency standards. Both Silicon (Si) and Gallium Nitride (GaN) power FETs may be used, with appropriate drivers for each.

8.2 Typical Application Circuit

The following application circuit applies to a GaN-based power stage with SET pin connected to ground, and to a Si-based power stage with SET pin tied to the REF pin.



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図 36. Typical Application Circuit

Typical Application Circuit (continued)

8.2.1 Design Requirements

表 4. UCC28780 Electrical Performance Specifications for GaN FET(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{IN}	Input line voltage (RMS)		90	115 / 230	264	V
f_{LINE}	Input line frequency		47	50 / 60	63	Hz
P_{STBY}	Input power at no-load	V_{IN} = 115 V_{RMS}, I_O = 0 A		41.1		mW
		V_{IN} = 230 V_{RMS}, I_O = 0 A		52.8		mW
$P_{0.25W}$	Input power at 0.25W load	V_{IN} = 115 V_{RMS}, P_O = 250.6 mW		383.8		mW
		V_{IN} = 230 V_{RMS}, P_O = 250.6 mW		435.0		mW
OUTPUT CHARACTERISTICS						
V_O	Output voltage	V_{IN} = 115 V_{RMS}, I_O = 2.25 A		19.853		V
		V_{IN} = 230 V_{RMS}, I_O = 2.25 A		19.852		
		V_{IN} = 115 V_{RMS}, I_O = 0 A		19.943		
		V_{IN} = 230 V_{RMS}, I_O = 0 A		19.948		
$I_{O(FL)}$	Full-load rated output current	V_{IN} = 90 to 264 V_{RMS}		2.25		A
V_{O_pp}	Output ripple voltage	V_{IN} = 115 V / 230 V_{RMS}, I_O = 0 A to 2.25 A		80		mVpp
		V_{IN} = 115 V / 230 V_{RMS}, I_O = 2.25 A		45		
		V_{IN} = 115 V / 230 V_{RMS}, I_O = 0 A		50		
$P_{O(OPP)}$	Over-power protection power limit	V_{IN} = 90 to 264 V_{RMS}		55		W
t_{OPP}	Over-power protection duration	V_{IN} = 90 to 264 V_{RMS}, P_O = $P_{O(OPP)}$		160		ms
ΔV_O	Output voltage deviation during step load transient	I_O step between 0 A to 2.25 A		< 5		%
SYSTEMS CHARACTERISTICS						
η	Full-load efficiency	V_{IN} = 115 V_{RMS}, I_O = 2.25 A		94.59		%
		V_{IN} = 230 V_{RMS}, I_O = 2.25 A		94.74		%
		V_{IN} = 90 V_{RMS}, I_O = 2.25 A		93.98		%
η	4-point average efficiency(2)	V_{IN} = 115 V_{RMS}		93.88		%
		V_{IN} = 230 V_{RMS}		92.47		%
η	Efficiency at 10% load	V_{IN} = 115 V_{RMS}, I_O = 10% of $I_{O(FL)}$		88.69		%
		V_{IN} = 230 V_{RMS}, I_O = 10% of $I_{O(FL)}$		85.86		%
T_{AMB}	Ambient operating temperature range	V_{IN} = 90 to 264 V_{RMS}, I_O = 0 to 2.25 A		25		°C

(1) The performance listed in this table is achieved using secondary-resonance and based on the test results from a single board.
(2) Average efficiency of four load points, I_O = 25%, 50%, 75%, and 100% of $I_{O(FL)}$.

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8.2.2 Detailed Design Procedure

8.2.2.1 Input Bulk Capacitance and Minimum Bulk Voltage

In an offline application, the input bulk capacitor (C_{BULK}) should be sized for the minimum input AC line voltage ($V_{IN(MIN)}$) and minimum voltage of the input bulk capacitor ($V_{BULK(MIN)}$). Due to the transition-mode operation, too low of $V_{BULK(MIN)}$ selection results in higher RMS current at $V_{IN(MIN)}$ and affects the full load efficiency, while too high of $V_{BULK(MIN)}$ enlarges the volume of the bulk capacitor. This equation does not account for the hold-up time requirement over line drop-outs.

$$C_{BULK(MIN)} = \frac{\frac{P_O}{\eta} \times [0.5 + \frac{1}{\pi} \times \arcsin(\frac{V_{BULK(MIN)}}{\sqrt{2} \times V_{IN(MIN)}})]}{(2 \times {V_{IN(MIN)}}^2 - {V_{BULK(MIN)}}^2) \times f_{LINE}} \quad (18)$$

8.2.2.2 Transformer Calculations

8.2.2.2.1 Primary-to-Secondary Turns Ratio (N_{PS})

N_{PS} influences the design tradeoffs on the voltage rating between primary and secondary switches, and the balance between the magnetic core and winding loss of the transformer, which are explained in detail as follows:

1. Maximum N_{PS} ($N_{PS(MAX)}$) is limited by the maximum derated drain-to-source voltage of Q_L ($V_{DS_QL(MAX)}$). In the expression below, ΔV_{CLAMP} is the voltage above the reflected output voltage. It can be either the ripple voltage of C_{CLAMP} in AAM mode, or the voltage over-charge of C_{CLAMP} by the leakage energy as Q_H is disabled in LPM mode. V_O is the output voltage, and V_F is the forward voltage drop of the secondary rectifier.
$$N_{PS(MAX)} = \frac{V_{DS_QL(MAX)} - V_{BULK(MAX)} - \Delta V_{CLAMP}}{V_O + V_F} \quad (19)$$
2. Minimum N_{PS} ($N_{PS(MIN)}$) is limited by the maximum derated drain-to-source voltage of the secondary rectifier ($V_{DS_SR(MAX)}$). In the expression for $N_{PS(MIN)}$, ΔV_{SPIKE} should account for any additional voltage spike higher than $V_{BULK(MAX)}/N_{PS}$ that occurs when Q_H is active and turns-off at non-zero current in AAM mode.
$$N_{PS(MIN)} = \frac{V_{BULK(MAX)}}{V_{DS_SR(MAX)} - V_O - \Delta V_{SPIKE}} \quad (20)$$
3. Since the high-frequency transformer is usually a core-loss limited design instead of a saturation-limited design, the minimum duty cycle (D_{MIN}) at $V_{BULK(MAX)}$ is more important. Lower D_{MIN} increases core loss at $V_{BULK(MAX)}$, so this constraint creates another limitation on $N_{PS(MIN)}$.
$$N_{PS(MIN)} = \frac{D_{MIN} V_{BULK(MAX)}}{(1 - D_{MIN})(V_O + V_F)} \quad (21)$$
4. The winding loss distribution between the primary and secondary side of the transformer is the final consideration. As N_{PS} increases, primary RMS current reduces, while secondary RMS current increases.

8.2.2.2.2 Primary Magnetizing Inductance (L_M)

After N_{PS} is chosen, L_M can be estimated based on minimum switching frequency ($f_{SW(MIN)}$) at $V_{BULK(MIN)}$, maximum duty cycle (D_{MAX}), and output power at nominal full load current ($P_{O(FL)}$). K_{RES} represents the duty cycle loss to wait for the switch-node voltage transition from the reflected output voltage to zero. 5% to 6% of K_{RES} is used as a initial estimated value. The selection of minimum switching frequency ($f_{SW(MIN)}$) has to consider the impact on full-load efficiency and EMI filter design.

$$D_{MAX} = \frac{N_{PS}(V_O + V_F)}{V_{BULK(MIN)} + N_{PS}(V_O + V_F)} \quad (22)$$

$$L_M = \frac{{D_{MAX}}^2 {V_{BULK(MIN)}}^2 \eta}{2 P_{O(FL)}} \times \frac{(1 - K_{RES})}{f_{SW(MIN)}} \quad (23)$$

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8.2.2.2.3 Primary Turns (N_P)

The turn number on the primary side of the transformer (N_P) is determined by two design considerations:

1. The maximum flux density (B_{MAX}) must be kept below the saturation limit (B_{SAT}) of the magnetic core under the highest peak magnetizing current ($I_{M+(MAX)}$) condition, a given cross-section area (A_E) of the core geometry, and highest core temperature. When I_{FB} = 0 A, such as V_O soft-start or step-up load transient, the peak magnetizing current reaches $I_{M+(MAX)}$, since V_{CST} = $V_{CST(MAX)}$ in those conditions. $I_{M+(MAX)}$ can be calculated based on the output power triggering an OPP fault ($P_{O(OPP)}$) with V_{CST} = $V_{CST(OPP1)}$ at $V_{BULK(MIN)}$. After N_P is chosen, N_S can be calculated through N_{PS}.

$$I_{M+(MAX)} = \frac{2P_{O(OPP)}}{D_{MAX}V_{BULK(MIN)}\eta}\frac{V_{CST(MAX)}}{V_{CST(OPP1)}} \tag{24}$$

$$B_{MAX} = \frac{L_M I_{M+(MAX)}}{N_P A_E} < B_{SAT} \tag{25}$$

2. The AC flux density (ΔB) affects the core loss of a transformer. For a transition-mode active clamp flyback, the core loss at high line is usually highest, since the switching frequency is highest and duty cycle is smallest for a given load condition. The following equation is the ΔB calculation including the contribution of negative magnetizing current (I_{M-}), used to put into the Steinmetz equation for more accurate core loss estimation. For $V_{BULK} \geq N_{PS}(V_O+V_F)$, I_{M-} is calculated with V_{BULK} divided by the characteristic impedance of L_M and the lumped time-related switch-node capacitance (C_{SW}). The expression of f_{SW} is derived based on the triangular approximation of the magnetizing current, which also considers I_{M-} effect over wide AC line condition.

$$I_{M-} = -\sqrt{\frac{C_{SW}}{L_M}}V_{BULK} \tag{26}$$

$$I_{IN} = \frac{P_{O(FL)}}{\eta}\frac{1}{V_{BULK}} \tag{27}$$

$$D = \frac{N_{PS}(V_O+V_F)}{V_{BULK}+N_{PS}(V_O+V_F)} \tag{28}$$

$$f_{SW} = \frac{D^2 V_{BULK}}{2L_M I_{IN} - DL_M I_{M-} + DV_{BULK} \times 0.5\pi\sqrt{L_M C_{SW}}} \tag{29}$$

$$I_{M+} = \sqrt{\frac{2P_{O(FL)}}{\eta L_M f_{SW}} + {I_{M-}}^2} \tag{30}$$

$$\Delta B = \frac{L_M(I_{M+}-I_{M-})}{N_P A_E} \tag{31}$$

8.2.2.2.4 Secondary Turns (N_S)

N_S and N_P are adjusted to the nearest suitable integers. With the new N_{PS}, Primary Magnetizing Inductance (L_M) is recalculated to update the parameter change.

$$N_S = \frac{N_P}{N_{PS}} \tag{32}$$

8.2.2.2.5 Turns of Auxiliary Winding (N_A)

Turns of the auxiliary winding (N_A) is an integer value usually chosen to provide a nominal V_{VDD} that satisfies all devices powered from V_{VDD}, such as the gate driver, UCC28780, etc. N_A is determined by the following design considerations:

1. V_{VDD} must be lower than the maximum rating voltage of VDD pin ($V_{VDD(MAX)}$) at maximum output voltage ($V_{O(MAX)}$). $V_{VDD(MAX)}$ is limited by the lowest voltage rating of the devices connected to VDD pin.

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$$N_{A(MAX)} = \frac{V_{VDD(MAX)}}{V_{O(MAX)} + V_F} N_S \quad (33)$$

2. The nominal V_{VDD} should consider the impact on the standby power. Higher V_{VDD} results in the static-loss increase with the total bias current of the devices connected to VDD pin.
3. V_{VDD} should be higher than the 11-V threshold voltage of survival mode, which is the sum of $V_{VDD(OFF)}$ and $V_{VDD(PCT)}$, at the minimum sustained output voltage ($V_{O(MIN)}$). ΔV represents the voltage difference between the nominal V_{VDD} and the survival-mode threshold. A minimum of 3 V is a recommended design margin of ΔV.

$$N_{A(MIN)} = \frac{V_{VDD(OFF)} + V_{VDD(PCT)} + \Delta V}{V_{O(MIN)} + V_F} N_S \quad (34)$$

8.2.2.2.6 Winding and Magnetic Core Materials

Not only by the control of AC flux density (ΔB) with L_M and N_P design, the core loss of the transformer can also be significantly reduced by a proper selection of the magnetic core material. For a converter operating at 200 kHz to 400 kHz of switching frequencies (at full load condition), core materials such as 3F36 from Ferroxcube and N49 from TDK exhibit low core loss density in the frequency range. Litz wires are recommended for both primary and secondary windings, in order to reduce the AC winding loss caused by the proximity effect and the skin effect of the transformer windings.

8.2.2.3 Clamp Capacitor Calculation

There are two resonance approaches for an active clamp flyback (ACF) converter, primary resonance and secondary resonance, which affect the design guide on the clamp capacitor (C_{CLAMP}). Referring to 図 36, if C_{O1} serves as the energy-storage capacitor at the output with larger capacitance and C_{O2} is a high-frequency decoupling capacitor, leakage inductance of transformer (L_K) mainly resonates with C_{CLAMP} during the demagnetization time of the magnetizing inductance (L_M). This configuration is called the primary-resonance ACF converter. On the other hand, if C_{O2} serves as the energy-storage capacitor at the output with larger capacitance and C_{O1} is much smaller than the equivalent capacitance of C_{CLAMP} reflected to the secondary side (C_{CLAMP}/N_{PS}^2), L_K mainly resonates with C_{O1}. This configuration is called the secondary-resonance ACF converter.

For primary-resonance ACF, the design tradeoff between conduction loss and turn-off switching loss of Q_H needs to be considered. Higher C_{CLAMP} results in less RMS current flowing through the transformer windings and switching devices, so the conduction loss can be reduced. However, a higher C_{CLAMP} design results in Q_H turning-off before the clamp current returns to 0 A. The condition of non zero current switching (ZCS) increases the turn-off switching loss of Q_H. This is aggravated if the turn-off speed of Q_H is not fast enough. Therefore, C_{CLAMP} needs to be fine-tuned based on the loss attribution. If the resonance between L_K and C_{CLAMP} is designed to be completed by the time Q_H is turned-off, the clamp current should reach close to 0 A around three quarters of the resonant period. The following equation can be used to design C_{CLAMP} for obtaining ZCS at $V_{BULK(MIN)}$ and full load. This design results in a non-ZCS condition at $V_{BULK(MAX)}$, since the switching frequency at $V_{BULK(MAX)}$ is higher in transition-mode operation. A low-ESR clamp capacitor is recommended to minimize the conduction loss. If a ceramic capacitor is used as the low-ESR capacitor, the DC bias effect on the capacitance reduction also needs to be considered.

$$C_{CLAMP} = \frac{1}{L_K}\left[\frac{L_M I_{M+(FL)}}{1.5\pi N_{PS}(V_O + V_F)}\right]^2 \quad (35)$$

For secondary-resonance ACF, C_{O1} is used to adjust the resonance time with L_K to fulfill the ZCS condition, so a large C_{CLAMP} will not compromise ZCS. Besides, during the on-time of low-side switch (Q_L), the small C_{O1} is partially discharged by the load current at the same time. After Q_L turns off and the resonance begins, the discharged C_{O1} makes the initial resonance voltage lower than the reflected clamp capacitor voltage across C_{CLAMP}, which forces more magnetizing current delivered to output, so the conduction loss is reduced with less RMS current flowing through Q_H and the primary winding.

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8.2.2.4 Bleed-Resistor Calculation

R_{BLEED} is used to discharge the clamp capacitor voltage to a residual voltage ($V_{RESIDUAL}$) during the 1.5-s fault delay recovery time (t_{FDR}). After the converter recovers from the fault mode, lower $V_{RESIDUAL}$ reduces the maximum current stress ($I_{SHORT(MAX)}$) flowing through the switching devices within their respective safe operating areas, even if the output voltage is shorted. $V_{RESIDUAL}$ can be determined by the target $I_{SHORT(MAX)}$ multiplied with the characteristic impedance between the leakage inductance (L_K) and the clamp capacitor (C_{CLAMP}). $I_{SHORT(MAX)}$ is based on the de-rated maximum pulse current of Q_H or the output-rectifier current reflected to the primary side, whichever is lower. This design guide can be applied to both primary and secondary resonance ACF converters. An excessively low value of R_{BLEED} results in over-discharging of C_{CLAMP}, and introduces excess continuous power loss which affects standby power.

$$V_{RESIDUAL} \approx I_{SHORT(MAX)} \sqrt{\frac{L_K}{C_{CLAMP}}} \tag{36}$$

$$R_{BLEED} = \frac{t_{FDR}}{C_{CLAMP} \ln\left[\frac{N_{PS}(V_O + V_F) + \Delta V_{CLAMP}}{V_{RESIDUAL}}\right]} \tag{37}$$

8.2.2.5 Output Filter Calculation

The bulk output capacitor of active clamp flyback (ACF) converters, C_{O1} of the primary-resonance ACF or C_{O2} of the secondary-resonance ACF, is often determined by the transient-response requirement from no load to full load transition. For a target output voltage undershoot (ΔV_O) with the load step-up transient of ΔI_O, the minimum bulk output capacitance ($C_{O(MIN)}$) can be expressed as

$$C_{O(MIN)} = \frac{\Delta I_O t_{RESP}}{\Delta V_O} \tag{38}$$

where t_{RESP} is the time delay from the moment ΔI_O is applied to the moment when I_{FB} falls below 1 μA.

The output filter inductor (L_O) is an essential component for the secondary-resonance ACF, not only to filter the large switching voltage ripple across C_{O1} but also to decouple the effect of C_{O2} on the resonance period. The sum of L_O impedance, ESR of C_{O2} (R_{Co2}), and C_{O2} impedance at minimum switching frequency ($f_{SW(MIN)}$) must be much higher than C_{O1} impedance at the same frequency to force most of switching resonance current to flow through C_{O1}.

$$L_O >> \frac{1}{(2\pi f_{SW(MIN)})^2 C_{O1}} - \frac{1}{(2\pi f_{SW(MIN)})^2 C_{O2}} - \frac{R_{Co2}}{2\pi f_{SW(MIN)}} \tag{39}$$

One benefit of lowering the ESR on C_{O1} (R_{Co1}) is to help to reduce the switching ripple on the output voltage. Another benefit is reducing the conduction loss of C_{O1} for the secondary-resonance ACF converter. However, the issue is that the damping between L_O and C_{O1} is weakened. Without proper damping, the magnitude of low-frequency resonance ripple between L_O and C_{O1} enlarges output ripple, affects the loop stability, and affects the operation of synchronous rectifier (Q_{SEC}). The secondary-resonance ACF converter is the most vulnerable since C_{O1} with low capacitance significantly weakens the damping. To resolve this issue, it is found that a serial damping network formed by L_{DAMP} and R_{DAMP} is a very effective way to minimize the impact. However, too strong of a damping design results in noticeable conduction loss increase and full load efficiency drop. Therefore, it is recommended that L_{DAMP} and R_{DAMP} should be higher than the theoretical strong damping value as the following equations suggest. Even though the damping network is an additional component, the physical size or the footprint is much smaller than L_O, not only because of the small value but also the wide selection of a small-size chip inductor which winding resistance can be a free R_{DAMP}. For the 45W secondary-resonance ACF design with primary GaN FETs and a polymer-type C_{O2}, when a 0.68-μH chip inductor is in parallel with a 1-μH output filter inductor, there is only 0.15% full-load efficiency drop at 90-V AC input, and there is a negligible efficiency difference at 230-V AC input.

$$L_{DAMP} > 0.13 \times L_O \tag{40}$$

$$R_{DAMP} > \sqrt{\frac{L_O}{C_{O1}}} \tag{41}$$

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8.2.2.6 Calculation of ZVS Sensing Network

There are four components in the application circuit to help the depletion MOSFET (Q_S) perform ZVS sensing safely, C_{SWS}, R_{SWS}, D_{SWS}, and R_{HVG}. Design considerations and selection guidelines for the values of these components are given here.

At the rising edge of the switch node, the fast dV/dt coupling through the drain-to-source capacitance of Q_S ($C_{OSS(Qs)}$) generates a charge current flowing into the capacitive loading of the Q_S source pin. The result is a voltage overshoot on both the SWS pin and across the gate-to-source of Q_S ($V_{GS(Qs)}$). The SWS pin, with an absolute maximum voltage of 38 V, can handle higher voltage stress than $V_{GS(Qs)}$. Therefore, a capacitor between the SWS pin and GND (C_{SWS}) should be selected properly to prevent the voltage overshoot from damaging the Q_S gate. Since $C_{OSS(Qs)}$ and C_{SWS} form a voltage divider, the minimum C_{SWS} ($C_{SWS(MIN)}$) can be derived as

$$C_{SWS(MIN)} = \frac{C_{OSS(Qs)} \times [V_{BULK(MAX)} + N_{PS}(V_O + V_F)]}{V_{HVG} + V_{GS_MAX(Qs)}} - C_{Dsws} \quad (42)$$

where $V_{GS_MAX(Qs)}$ is the de-rated maximum gate-to-source voltage of Q_S, V_{HVG} is the steady-state voltage level of 11 V, and C_{Dsws} is the parasitic capacitance of TVS diode (D_{SWS}) on the SWS pin.

Without resistive damping, both the charge current on the rising edge of V_{SW} and the discharge current on the falling edge of V_{SW} are oscillatory with the parasitic inductance within the ZVS sensing network resonating with C_{SWS}. Therefore, a series resistor (R_{SWS}) between SWS pin and source-pin of Q_S is used to dampen the high-frequency ringing, helping to obtain a cleaner sensing signal on the SWS pin and preventing any high-frequency current from interfering with other noise-sensitive signals. R_{SWS} can be expressed as:

$$R_{SWS} > \sqrt{\frac{L_{SWS}}{C_{SWS} + C_{Dz}}} \quad (43)$$

where L_{SWS} is the lumped parasitic inductance including the packaging of Q_S and PCB traces of Q_S and C_{SWS} return path.

Based on the above design guide, even though R_{SWS} and C_{SWS} may be sufficient to manage the voltage overshoot in normal operation, a low-capacitance TVS diode (D_{SWS}) is still highly recommended to serve as a safety backup of the ZVS sensing network. A regular Zener diode is not suitable due to its high capacitance and slow clamping response.

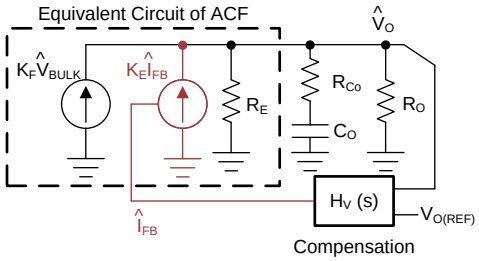
Based on the above equations, a general recommendation is that a 50 V C0G-type ceramic capacitor of 22 pF for C_{SWS}, a chip resistor no higher than 120 Ω for R_{SWS}, and a TVS diode with the clamp voltage between 18 V to 24 V for D_{SWS}. Too large of R_{SWS} or C_{SWS} introduces a sensing delay between V_{SW} and SWS pin, so the ZVS control pulls down V_{SW} earlier than expected before the end of t_Z by unnecessarily extending t_{DM}. The recommended R_{SWS} and C_{SWS} values only introduce a minor 2.6-ns delay, so the ZVS control is not be affected.

Another issue with too large of R_{SWS} is that an additional voltage drop may be created by the charge current through $C_{OSS(Qs)}$ during high dV/dt events of V_{SW}, which becomes another voltage stress onto the gate-to-source voltage of Q_S . For the power stage that can generate very high dV/dt, lowering R_{SWS} and increasing C_{SWS} may be necessary to enhance the protection on Q_S. Alternatively, a back-to-back TVS can be added between the gate and source pins of Q_S to provide a direct clamping to the possible over-voltage stress condition. Furthermore, a high-impedance discharge resistor (R_{HVG}) between the gate and source pins of Q_S helps to discharge the residual voltage on the gate capacitance, and R_{HVG} around 1 MΩ should be enough to serve the purpose. Note that too small R_{HVG} can hurt standby power, since it creates a continuous current flowing through Q_S.

8.2.2.7 Calculation of Compensation Network

UCC28780 integrates two control concepts to benefit high-efficiency operation: peak current-mode control and burst ripple control. The peak current loop in AAM can be analyzed based on the linear control theory, so the compensation target is to obtain enough phase margin and gain margin for the given small-signal characteristic of an active clamp flyback converter. For transition-mode operation, the power stage can be modeled as a voltage-controlled current source charging an output capacitor (C_O) with an equivalent-series resistance (R_{Co}) and the output load (R_O) as shown in 図 37. The first-order plant characteristic and high switching frequency operation in AAM make the peak current loop easier to stabilize than ABM.

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図 37. Small-Signal Model of ACF in AAM Loop

The adaptive burst mode (ABM) is a ripple-based control, so the linear control theory for AAM cannot be applied. The most critical stability criterion of burst control is to make the burst ripple content of I_{FB} to be in-phase with the burst ripple voltage of V_O. In normal operation, the fundamental burst frequency (f_{BUR}) in ABM varies between 20 kHz and 40 kHz. An example of normal burst operation is illustrated in 図 38.

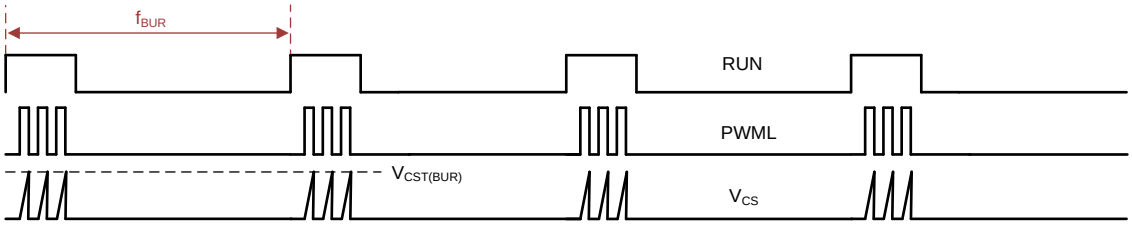


図 38. Expected Burst Pattern Example

Strong phase-delay in the frequency range creates slope distortion around the intersection point between I_{FB} and $I_{TH(FB)}$, so the ripple regulator generates inconsistent burst off-times. As shown in 図 39, the sub-harmonic oscillation at half of f_{BUR} is a typical phenomenon of an unstable ABM loop. Two burst packets are adjacent to each other and the pulse count (N_{SW}) is different by one pulse count.

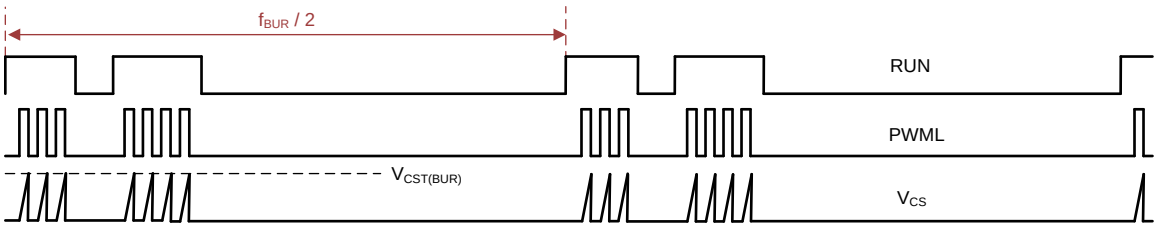
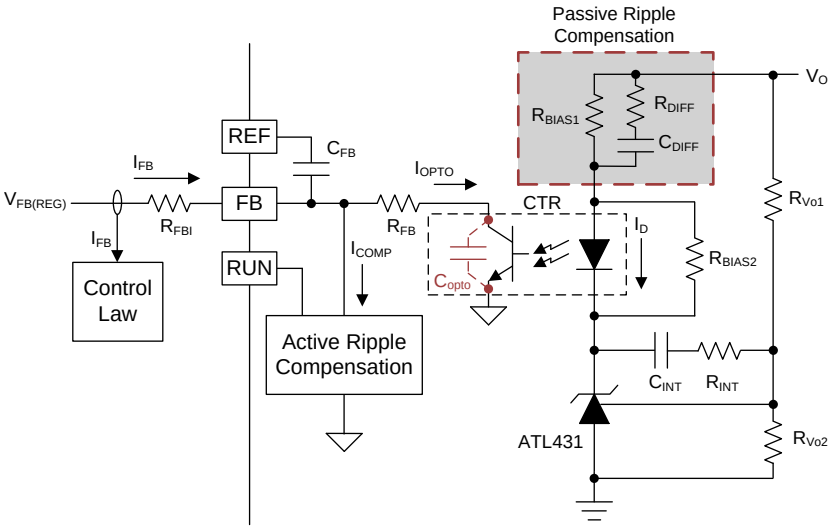


図 39. Typical Behavior of Unstable ABM Loop

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図 40. Compensation Network, $H_V(s)$

In order to minimize the phase-delay of I_{FB}, the transfer function from I_{FB} to V_O guides the pole/zero placement of the secondary-side passive ripple compensation network in 図 40. In the primary-side control circuitry, two poles at ω_{FB} and ω_{OPTO} introduce phase-delay on I_{FB}. ω_{FB} pole is formed by the external filter capacitor C_{FB} and the parallel resistance of the internal R_{FBI} and the external current-limiting resistor (R_{FB}). ω_{OPTO} pole is formed by the parasitic capacitance of the optocoupler output (C_{OPTO}) and the series resistance of R_{FBI} and R_{FB}. For C_{FB} = 100 pF, R_{FBI} = 8 KΩ, and R_{FB} = 20 KΩ, the delay effect of ω_{FB} pole located at 278 kHz is negligible. However, ω_{OPTO} pole is located less than 10 kHz, and introduces large phase delay in the interested f_{BUR} range of ABM, since C_{OPTO} is in a few nF range contributed by the Miller effect of the collector-to-base capacitance of the BJT in the optocoupler output. Therefore, an RC network (R_{DIFF} and C_{DIFF}) in parallel with R_{BIAS1} is used to compensate the phase-delay of the optocoupler, which introduces an extra pole/zero pair located at ω_{P1} and ω_{Z1} respectively. The basic design guide is to place the ω_{Z1} zero close to the ω_{OPTO} pole, and to place ω_{P1} pole away from highest f_{BUR}.

$$\frac{I_{FB}(s)}{V_O(s)} = \frac{CTR}{R_{BIAS1}} \frac{1+(s/\omega_{Z0})}{(s/\omega_{Z0})} \frac{1}{1+(s/\omega_{P1})} \frac{1+(s/\omega_{Z1})}{1+(s/\omega_{OPTO})} \frac{1}{1+(s/\omega_{FB})} \tag{44}$$

$$\omega_{Z0} = \frac{1}{(R_{Vo1} + R_{INT})C_{INT}} \tag{45}$$

$$\omega_{Z1} = \frac{1}{(R_{DIFF} + R_{BIAS1})C_{DIFF}} \tag{46}$$

$$\omega_{P1} = \frac{1}{R_{DIFF}C_{DIFF}} \tag{47}$$

$$\omega_{OPTO} = \frac{1}{(R_{FB} + R_{FBI})C_{OPTO}} \tag{48}$$

$$\omega_{FB} = \frac{1}{(R_{FBI} \,//\, R_{FB})C_{FB}} \tag{49}$$

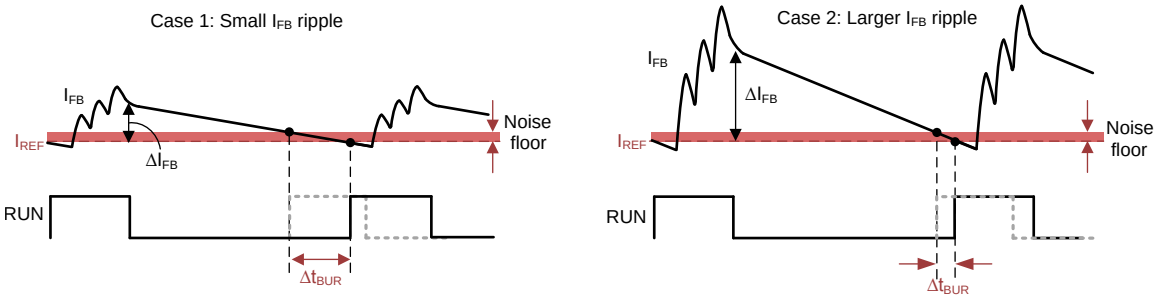


図 41. Effect of Signal-to-Noise Ratio of i_{FB} to ABM Operation

Another guideline of obtaining a more consistent burst off-time is to maintain large enough ripple amplitude of I_{FB} in ABM mode (ΔI_{FB}) for better signal-to-noise ratio. 図 41 shows that when the noise floor alters the intersection point of each burst cycle, larger ΔI_{FB} performs much less burst off-time variation if the noise floor stays the same. ΔI_{FB} around 10 μA is a recommended initial design value. The ripple ratio (K_{RIPPLE}) between ΔI_{FB} and the burst voltage ripple of V_O in ABM ($\Delta V_{O(ABM)}$) is obtained by simplifying the small-signal gain of $I_{FB}(s)/V_O(s)$ transfer function between 20 kHz and 40 kHz.

$$\Delta I_{FB} = K_{RIPPLE} \times \Delta V_{O(ABM)} \approx 10\mu A \tag{50}$$

$$K_{RIPPLE} \equiv \left.\frac{I_{FB}(s)}{V_o(s)}\right|_{20kHz<f<40kHz} \approx \frac{CTR}{R_{BIAS1}}\frac{\omega_{OPTO}}{\omega_{Z1}} = \frac{CTR}{R_{BIAS1}}\frac{(R_{DIFF}+R_{BIAS1})C_{DIFF}}{(R_{FB}+R_{FBI})C_{OPTO}} \tag{51}$$

With the above understanding on burst control, the step-by-step design procedure is:

1. R_{FB} selection needs to consider both the output voltage regulation and compensation challenge on the low-frequency pole at ω_{OPTO}. R_{FB} should be less than the maximum value of 28 kΩ to provide a sufficient feedback current of 95 μA for the output voltage regulation in SBP mode, under the worst-case $V_{FB(REG)}$ and R_{FBI}. R_{FB} = 28 kΩ and C_{OPTO} = 2 nF result in the ω_{OPTO} pole located at 2.8 kHz. Such a low-frequency pole forces the ω_{Z1} zero to be designed around 2.8 kHz to compensate the phase-delay.

$$R_{FB(MAX)} = \frac{V_{FB(REG)} - V_{CE(OPTO)}}{I_{FB(SBP)}} - R_{FBI} \tag{52}$$

2. R_{BIAS1} is determined based on a given current transfer ratio (CTR) of the optocoupler, $\Delta V_{O(ABM)}$, and target 10 μA of ΔI_{FB} as example.

$$R_{BIAS1} = \frac{CTR}{\Delta I_{FB}}\Delta V_{O(ABM)} = \frac{CTR}{10\mu A}\Delta V_{O(ABM)} \tag{53}$$

3. C_{DIFF} is designed to position $\omega_{Z1} \approx \omega_{OPTO}$ and locate ω_{P1} at least two-times higher frequency than 2π x $f_{BUR(UP)}$ as example.

$$C_{DIFF} = \frac{1}{R_{BIAS1}}\frac{\omega_{P1}-\omega_{Z1}}{\omega_{P1}\times\omega_{Z1}} = \frac{1}{R_{BIAS1}}\frac{(4\pi f_{BUR(UP)})-\omega_{OPTO}}{(4\pi f_{BUR(UP)})\times\omega_{OPTO}} \tag{54}$$

4. R_{DIFF} is designed to position ω_{P1} two-times higher than 2π x $f_{BUR(UP)}$, but lower than the switching frequency in ABM (2π x $f_{SW(BUR)}$). Too small of R_{DIFF} moves ω_{P1} higher than 2π x $f_{SW(BUR)}$, so the high differentiation gain on the secondary-side compensator amplifies the switching ripple and increases the noise floor. Therefore, R_{DIFF} should be fine-tuned based on the actual noise level of a given design.

$$R_{DIFF} = \frac{1}{\omega_{P1}C_{DIFF}} = \frac{1}{4\pi f_{BUR(UP)}C_{DIFF}} \tag{55}$$

5. R_{INT} selection is not designed for the small-signal compensation, but to resolve the slow large-signal response of the shunt regulator. Specifically, after a step-down load change from heavy load to no load occurs, the output voltage overshoot and the long settling time forces ATL431 to reduce the cathode voltage continuously by the integrator configuration of ATL431 until the output voltage gets back to normal regulation level. If the load step-up transient happens before the output voltage is settled from the previous load step-down event, the low voltage across ATL431 becomes the initial voltage level for the integrator to move to a

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new steady-state. Since the time for ATL431 moving from lower voltage to a high voltage delays i_{FB} reduction, the controller response from SBP mode to AAM mode is delayed as well, which slows down the energy delivery to the output and results in a large voltage undershoot. To resolve this problem, R_{INT} behaves like a current-limiting resistor for C_{INT}, which slows down the reduction on the cathode voltage of ATL431. R_{INT} needs to be adjusted based on the voltage undershoot requirement under the lowest repetitive rate of load change.

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8.2.3 Application Curves

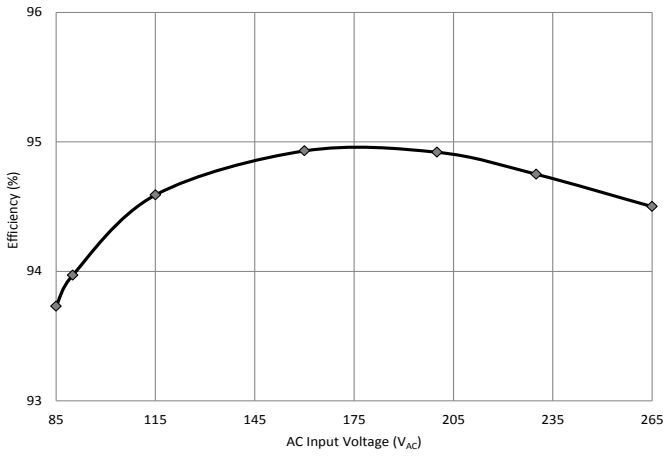


図 42. Full-Load Efficiency in Universal AC Line

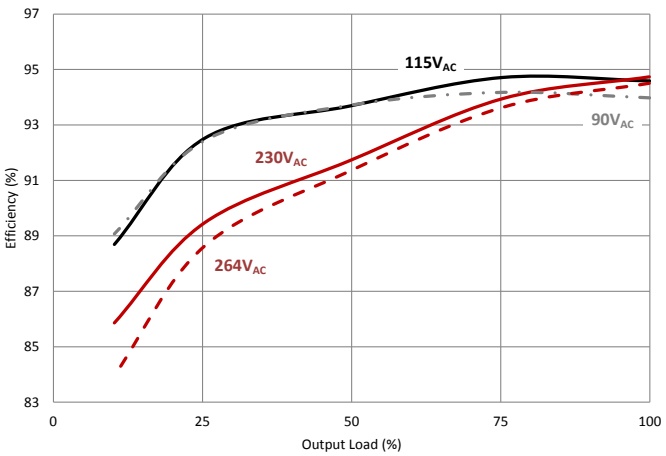


図 43. Light-Load Efficiency in Universal AC Line

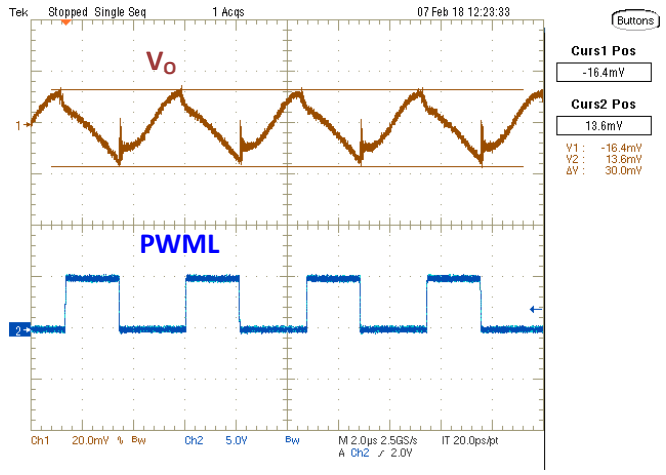


図 44. Output Voltage Ripple at V_{IN} = 115 V_{RMS} and I_O = 2.25 A

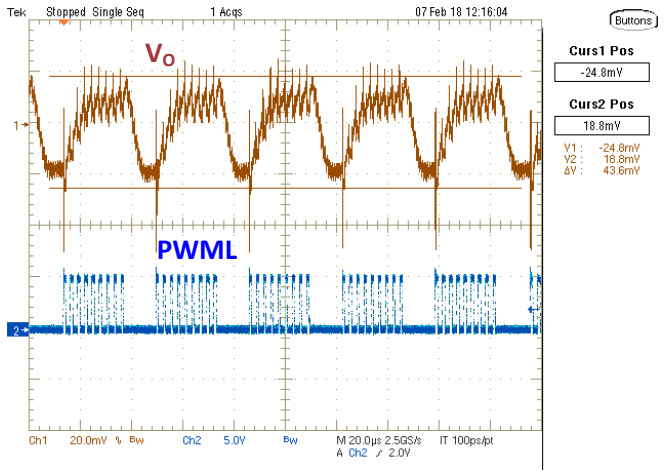


図 45. Output Voltage Ripple at V_{IN} = 115 V_{RMS} and I_O = 0.9 A

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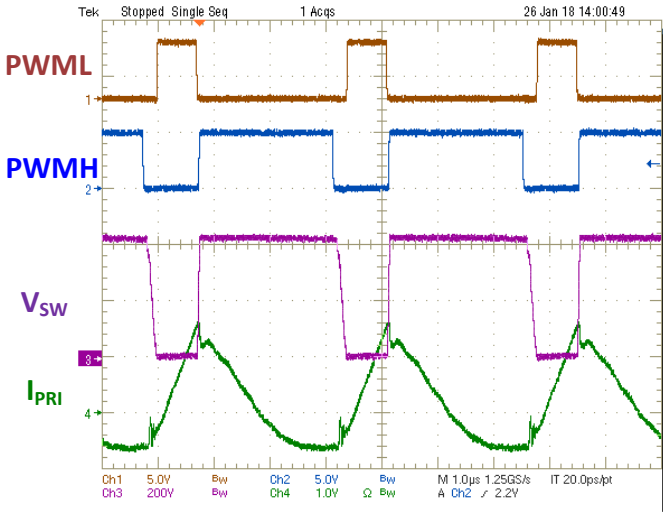


図 46. AAM Waveforms at V_{IN} = 230 V_{RMS} and I_O = 2.25 A

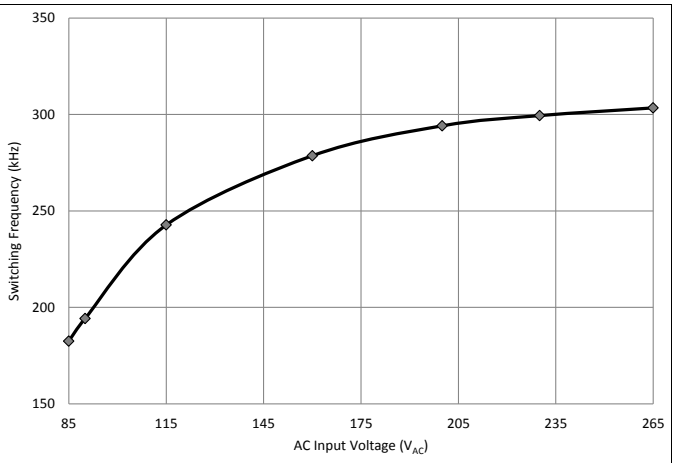


図 47. Switching Frequency in Universal Line and I_O = 2.25 A

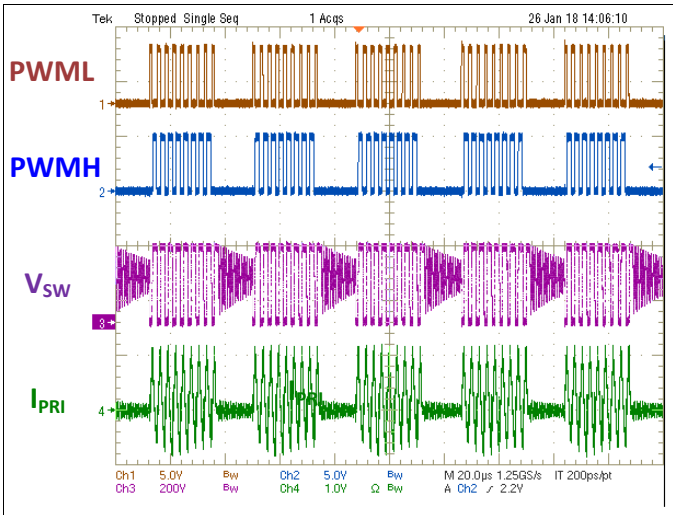


図 48. ABM Waveforms at V_{IN} = 115 V_{RMS} and I_O = 0.9 A

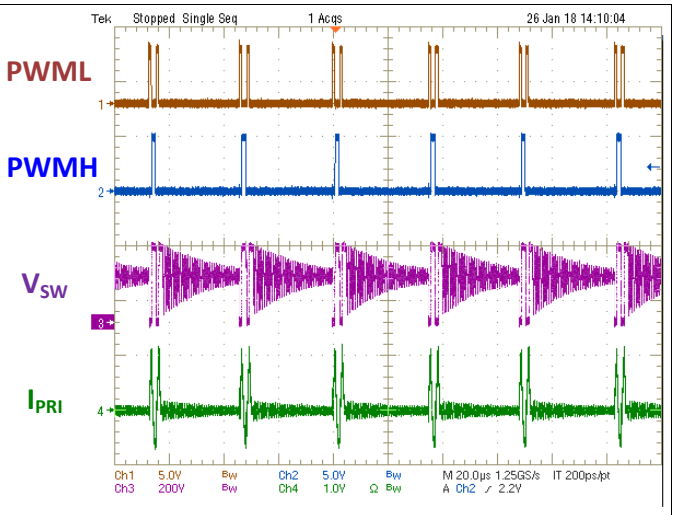


図 49. ABM Waveforms at V_{IN} = 115 V_{RMS} and I_O = 0.2 A

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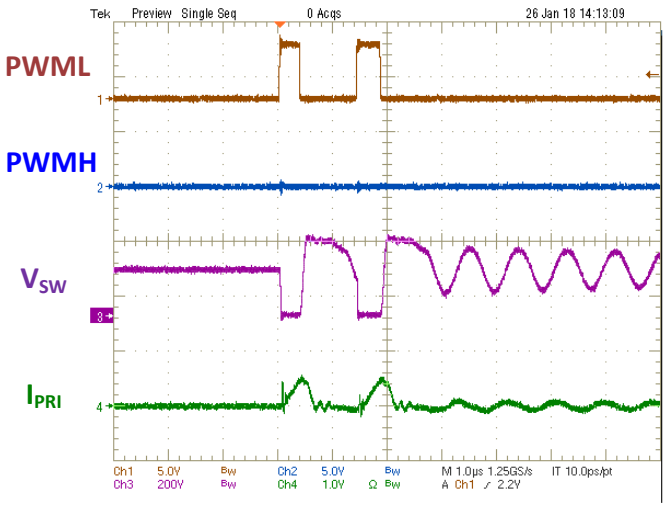


図 50. SBP Waveforms at V_{IN} = 115 V_{RMS} and I_O = 0 A

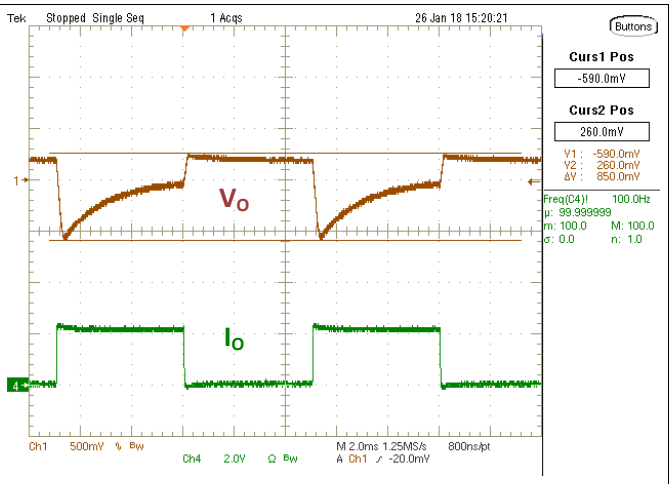


図 51. Load Transient between 0 A to 2.25 A at V_{IN} = 115 V_{RMS}

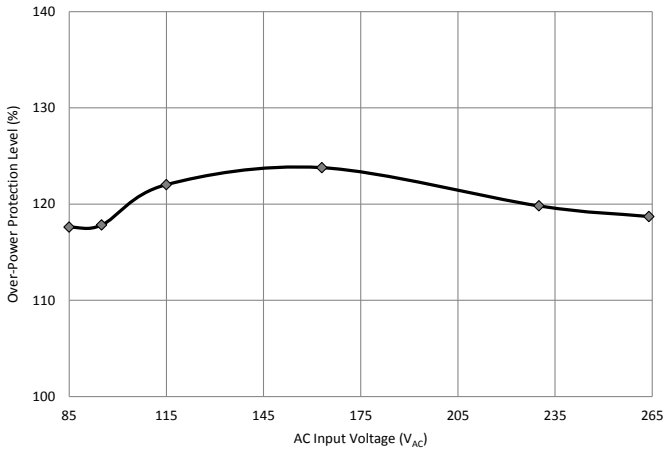


図 52. OPP Level in Universal AC Line

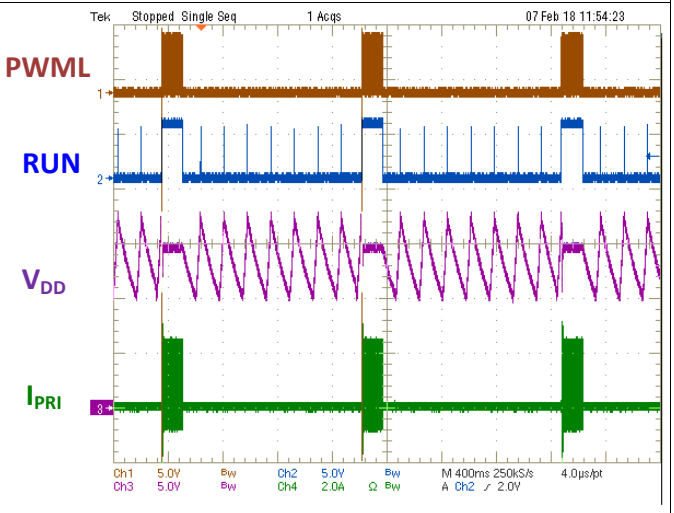


図 53. Fault Delay Recovery of OPP

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9 Power Supply Recommendations

The UCC28780 is intended to control active clamp flyback (ACF) converters in high efficiency offline applications, and is optimized to be used with universal AC input, from 85 V_{AC} to 265 V_{AC}, at 47 Hz to 63 Hz. An external depletion-mode MOSFET connected between the switch node of the converter and the SWS / HVG pins of this controller is required to charge the VDD capacitor during start-up, and to perform ZVS sensing during normal operation. Once the V_{VDD} reaches the UVLO turn-on threshold at 17.5 V, the VDD rail should be kept within the limits of the Bias Supply Input section of Specifications. To avoid the possibility that the device might stop switching, V_{VDD} must not be allowed to fall below the UVLO turn-off threshold at 9.8 V.

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10 Layout

10.1 Layout Guidelines

The active clamp flyback converter (ACF) designed with the UCC28780 not only recovers clamp energy but also eliminates switching loss with minimum circulating energy, so higher switching frequencies, efficiencies, and greater power densities can be achieved. However, when designing for higher switching frequencies, good layout practices as discussed below need to be followed to ensure for a more reliable and robust design.

10.1.1 General Considerations

Designing for high power density requires to consider noise coupling and thermal management. A four-layer PCB structure is highly recommended to use inner layers to help reduce current loop areas and provide heat-spreading for surface-mount semiconductors.

- Provide internal-layer copper areas to improve heat dissipation of high-power SMDs, particularly for MOSFETs and power diodes.
- To avoid capacitive noise coupling, do not cross outer-layer signals over copper areas with high-frequency switching voltage.
- To avoid inductive noise coupling, keep switching current loops as small as possible, and do not run signal tracks in parallel with such loops.

図 54 summarizes the critical layout guidelines, and more detail will be also be further elaborated in the descriptions below.

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Layout Guidelines (continued)

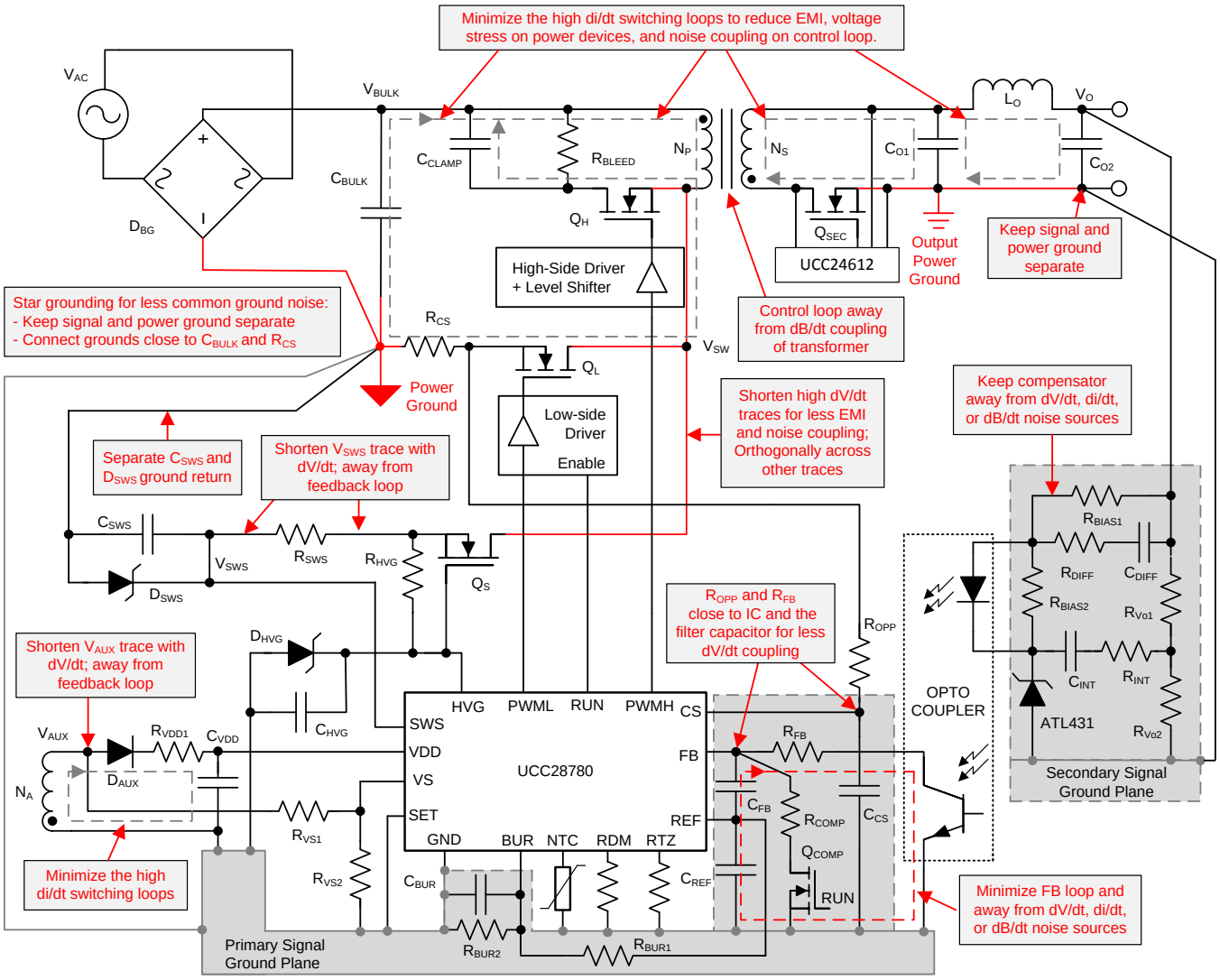


図 54. Schematic with Layout Considerations

10.1.2 RDM and RTZ Pins

Minimize stray capacitance to RDM and RTZ pins.

- Place R_{RDM} and R_{RTZ} as close as possible between the controller pins and GND pin.
- Avoid putting ground plane under RDM and RTZ pins to reduce parasitic capacitance. This can be accomplished by putting cutouts in the ground plane below these pins.

10.1.3 SWS Pin

Minimize potential stray noise coupling from SWS pin to noise-sensitive signals.

- Keep some distance between SWS pin and other connections.
- The RC damping network (R_{sws}, C_{sws}) and the TVS diode (D_{SWS}) should be as close to the source pin of Q_S as possible instead of SWS pin, so the gate-to-source pin of Q_S can be effectively protected.
- Keep the return path for di/dt current through C_{SWS} and D_{SWS} separate from the IC local GND and FB signal return paths.

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Layout Guidelines (continued)

10.1.4 VS Pin

Minimize stray capacitance at the VS pin to reduce the time delay effect on ZVS control.

- Avoid putting GND plane under VS Pin to reduce parasitic capacitance. This can be accomplished by putting a cutout in the ground plane below this pin.

10.1.5 BUR Pin

The resistor divider (R_{BUR1} and R_{BUR2}) and the filter capacitor (C_{BUR}) on the BUR pin should to be as close to the BUR pin and IC GND as possible.

- It is recommended to provide shielding on the BUR-pin trace with ground planes to minimize the noise-coupling effect on peak current variation during burst-mode operation. This can be accomplished by adding a ground plane under the BUR traces and pins.

10.1.6 FB Pin

This pin can be noise-sensitive to capacitive coupling from the high dV/dt switch nodes, or the flux coupling from magnetic components and high di/dt switching loops.

- Minimize the loop area for the PCB traces from the opto-coupler to the FB pin in order to avoid the possible flux coupling effect.
- Keep PCB traces away from the high dV/dt signals, such as the switch node of the converter (V_{SW}), the auxiliary winding voltage (V_{AUX}), and the SWS-pin voltage (V_{SWS}). If possible, it is recommended to provide shielding for the FB trace with ground planes.
- The filter capacitor between FB pin and REF pin (C_{FB}) needs to be as close to the two IC pins as possible.
- The current-limiting resistor of FB pin (R_{FB}) should be as close to the FB pin as possible to enhance the noise rejection of nearby capacitively-coupled noise sources.

10.1.7 CS Pin

The OPP-programming resistor (R_{OPP}) and the filter capacitor (C_{CS}) should be as close to the CS pin as possible to improve the noise rejection of nearby capacitively-coupled noise sources, and to filter any ringing that may be present during non-ZVS conditions.

10.1.8 GND Pin

The GND pin is the bias-power and signal ground connection for the controller. The effectiveness of the filter capacitors on the signal pins depends upon the integrity of the ground return.

- Place the decoupling and filter capacitors on VDD, REF, CS, and HVG pins as close as possible to the device pins and GND pin with short traces.
- The device ground and power ground should meet at the return of the current-sense resistor (R_{CS}). Try to ensure that high frequency/high current from the power stage does not go through the signal ground.
- The thermal pad of the QFN package should be tied to the IC GND pin with a short trace, and be connected to the signal ground plane with multiple vias which becomes a low-impedance ground return of external components to the GND pin.

10.2 Layout Example

The layout techniques described in above sections were applied to the layout of the 45-W 20-V high-density GaN active clamp flyback converter. 図 55 and 図 56 are the schematics of the evaluation module (EVM), the other figures are the layout of each layer, which critical traces are highlighted.

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Layout Example (continued)

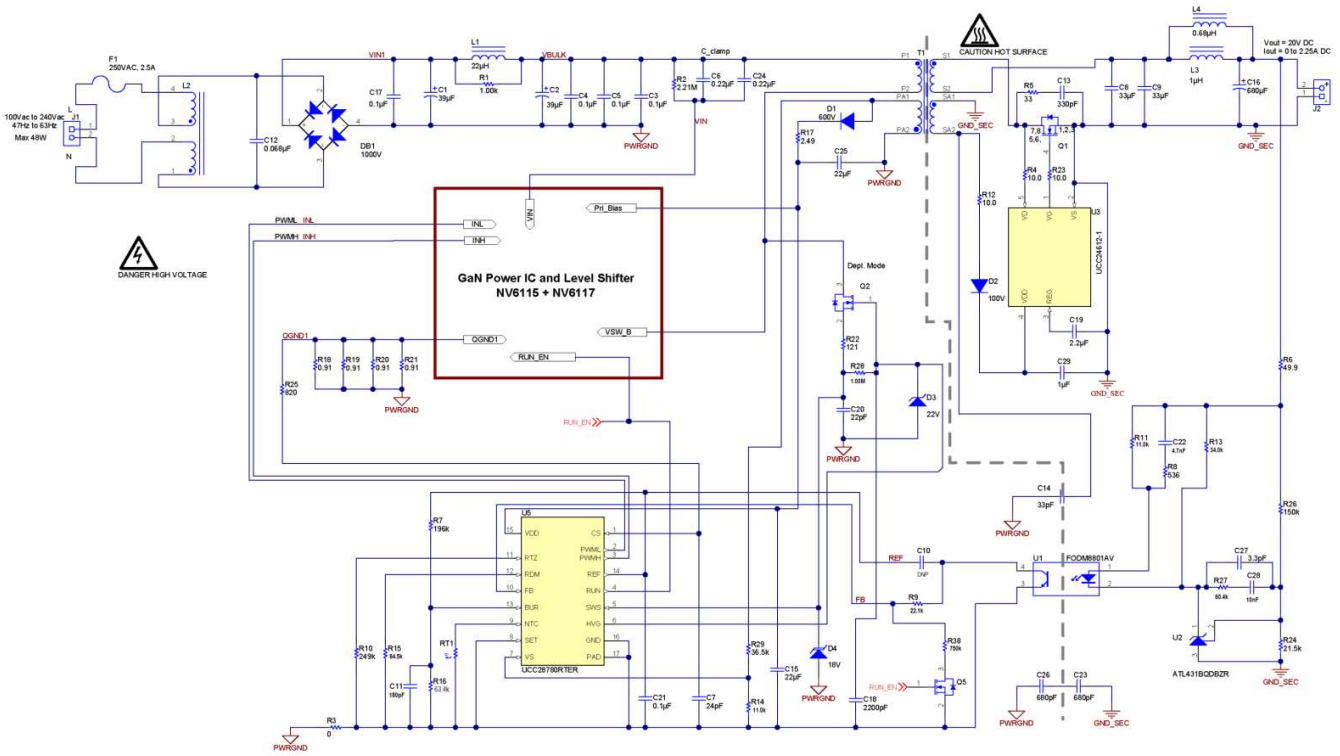


図 55. Schematic A of the 45-W EVM

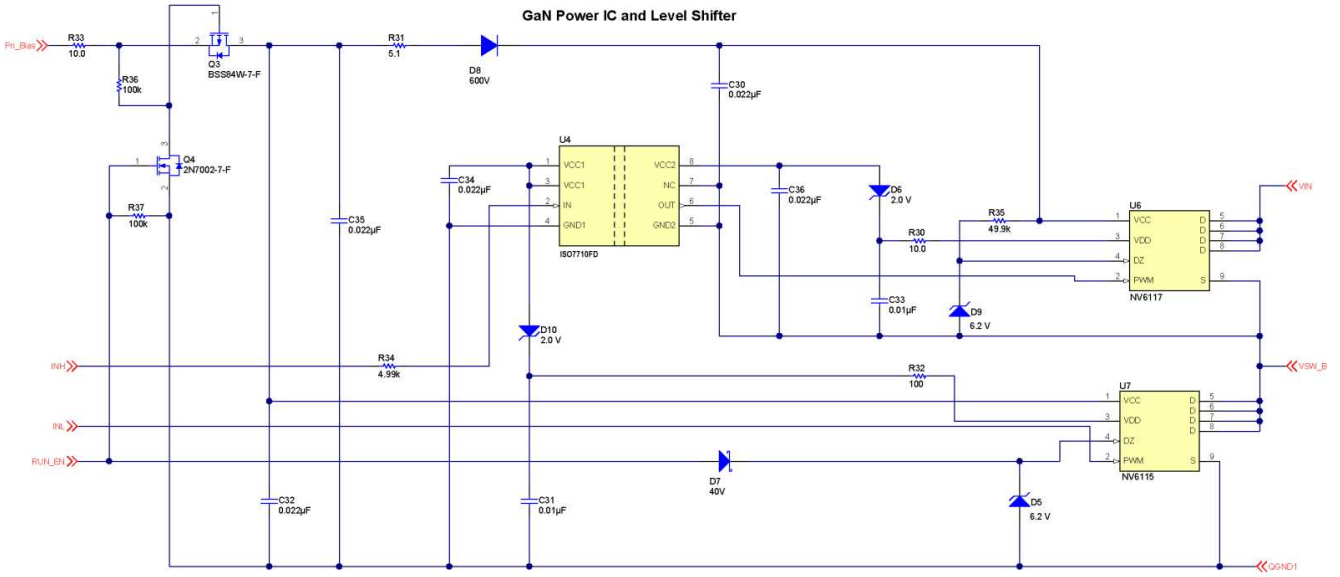


図 56. Schematic B of the 45-W EVM

Layout Example (continued)

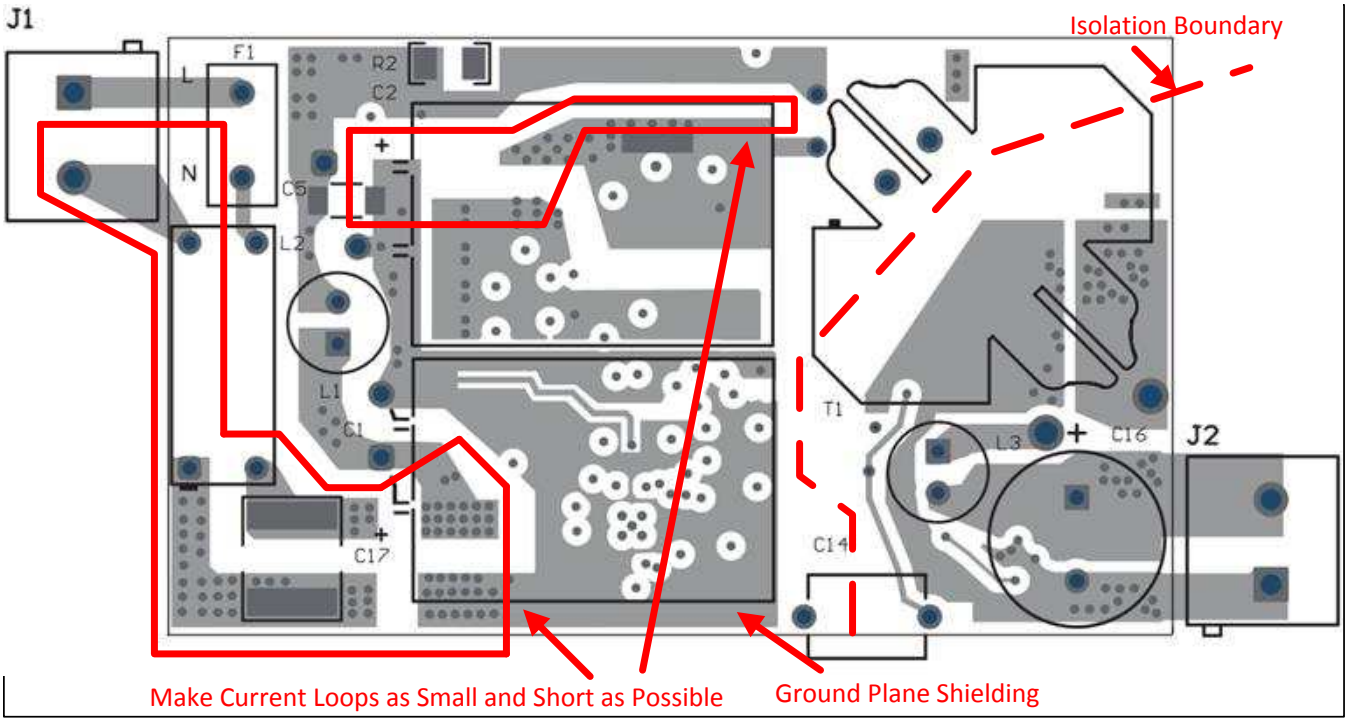


図 57. Top Assembly and First Layer of PCB

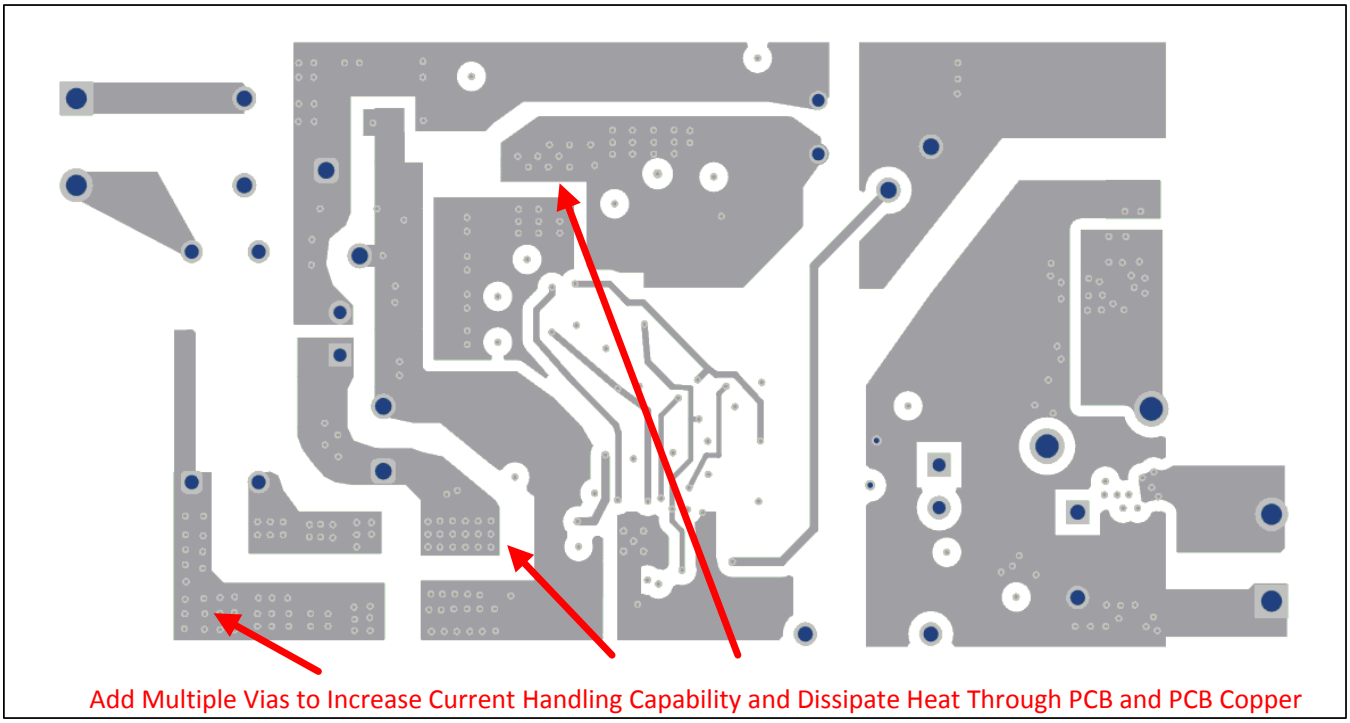


図 58. Second Layer of PCB

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Layout Example (continued)

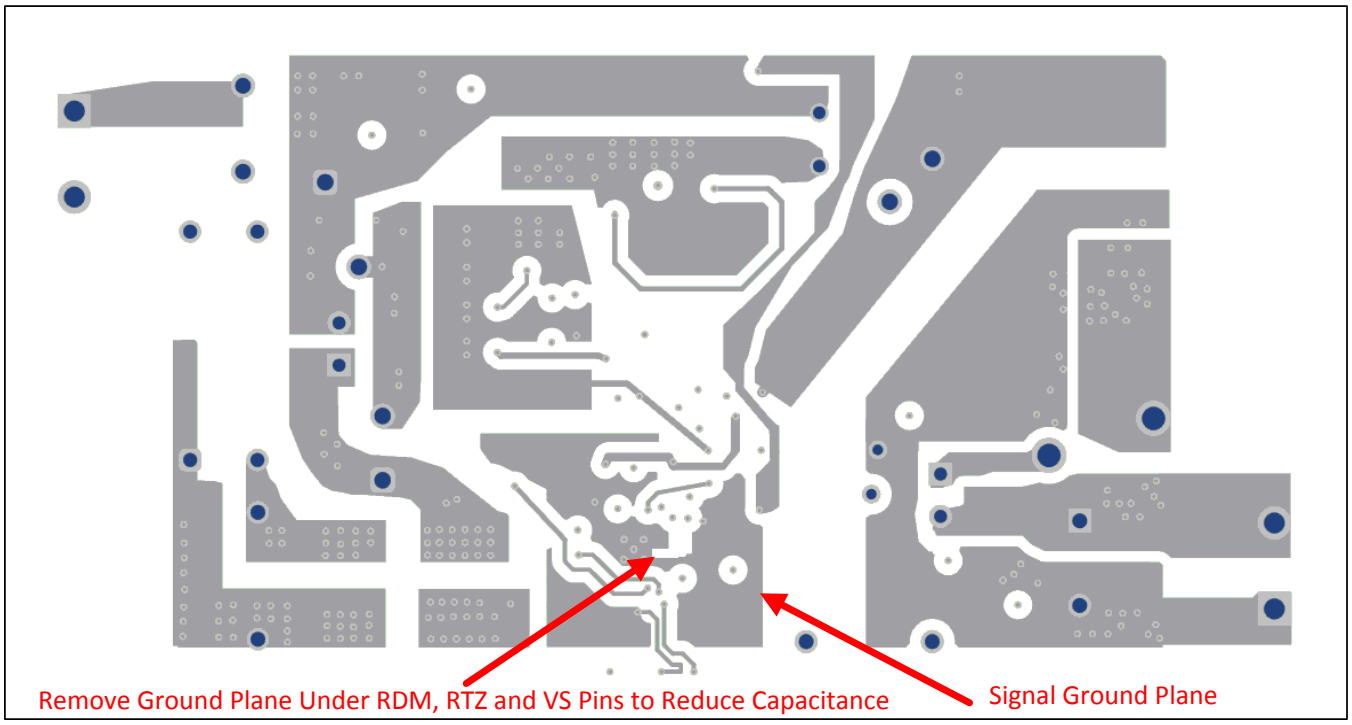


図 59. Third Layer of PCB

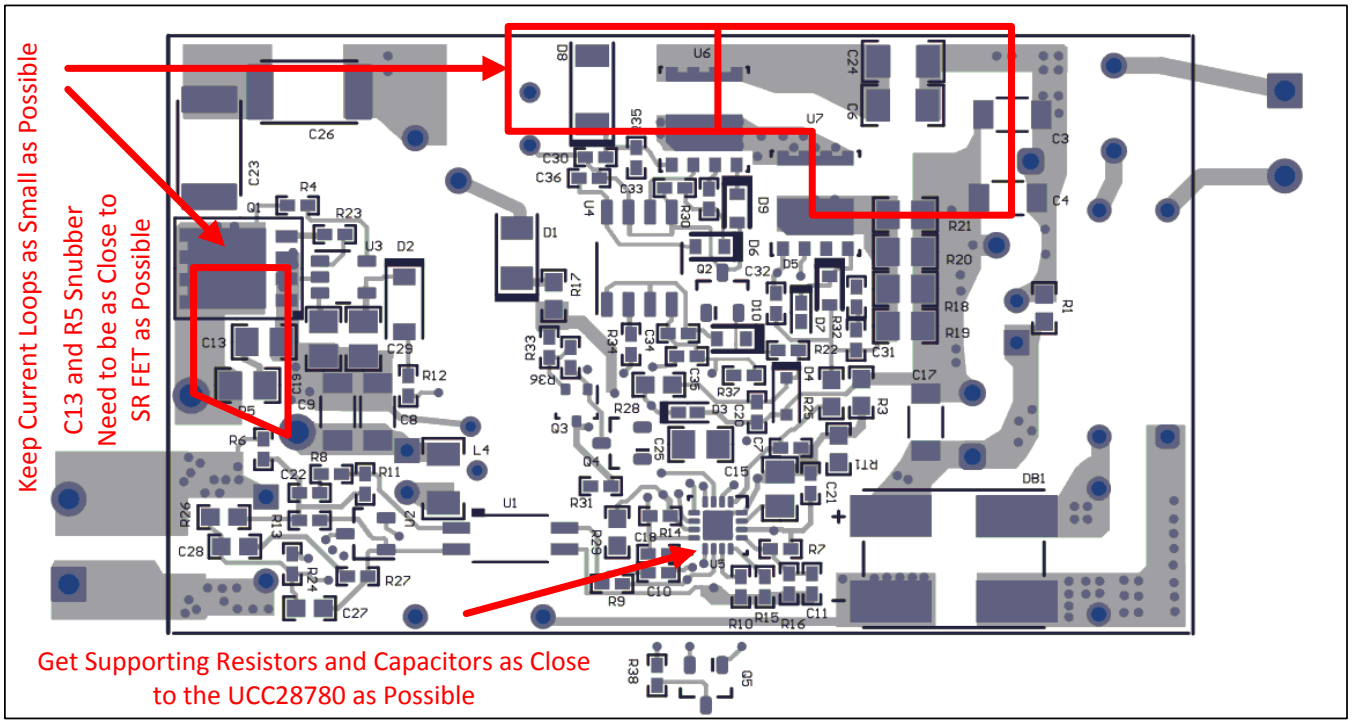


図 60. Bottom Assembly and Fourth Layer of PCB

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11 デバイスおよびドキュメントのサポート

11.1 ドキュメントのサポート

11.1.1 関連資料

関連資料については、以下を参照してください。

- 『UCC28780EVM-002の使用法: 45W、20Vの高密度GaNアクティブ・クランプ・フライバック・コンバータ』

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11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC28780D	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UCC28780
UCC28780D.B	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UCC28780
UCC28780DR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UCC28780
UCC28780DR.B	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UCC28780
UCC28780RTER	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	U28780
UCC28780RTER.B	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	U28780
UCC28780RTET	Active	Production	WQFN (RTE) | 16	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	U28780
UCC28780RTET.B	Active	Production	WQFN (RTE) | 16	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	U28780

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

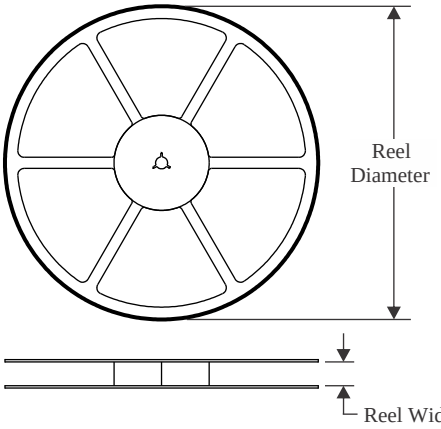
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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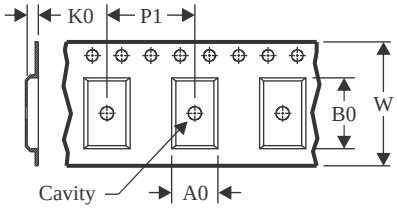
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

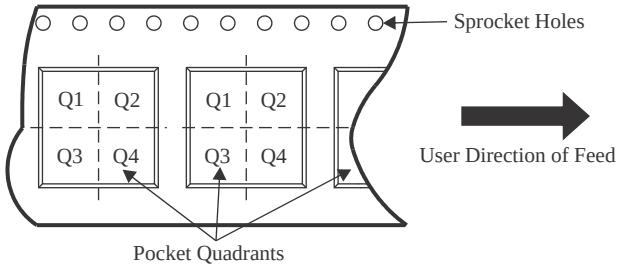


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

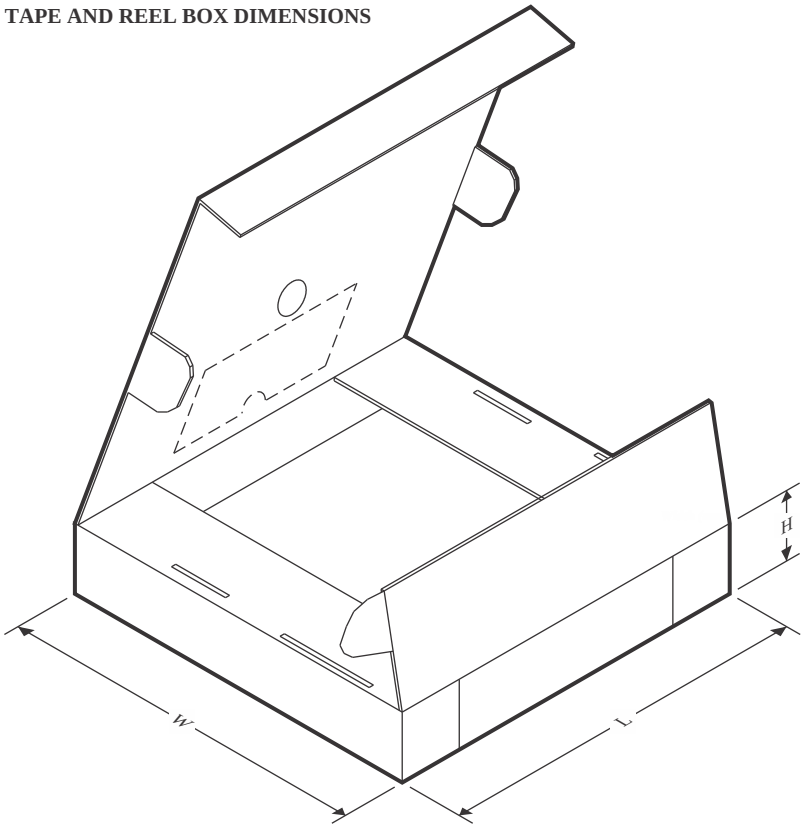
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC28780DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
UCC28780RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
UCC28780RTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

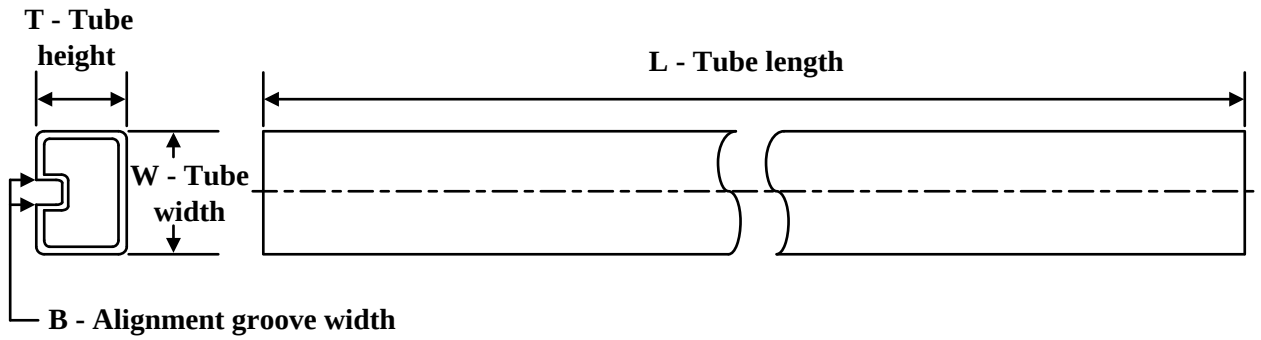
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC28780DR	SOIC	D	16	2500	353.0	353.0	32.0
UCC28780RTER	WQFN	RTE	16	3000	360.0	360.0	36.0
UCC28780RTET	WQFN	RTE	16	250	210.0	185.0	35.0

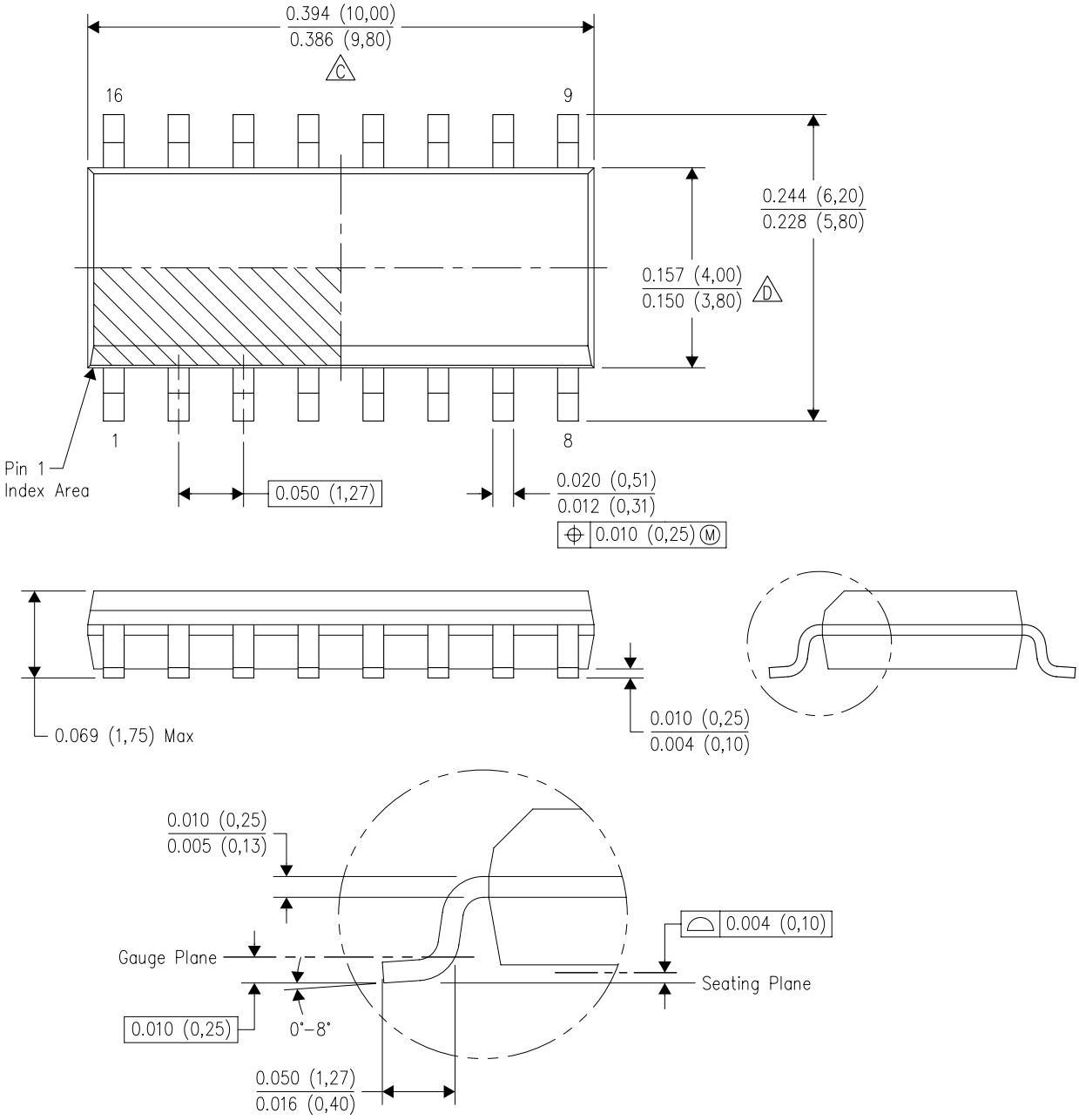
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UCC28780D	D	SOIC	16	40	507	8	3940	4.32
UCC28780D.B	D	SOIC	16	40	507	8	3940	4.32

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

GENERIC PACKAGE VIEW

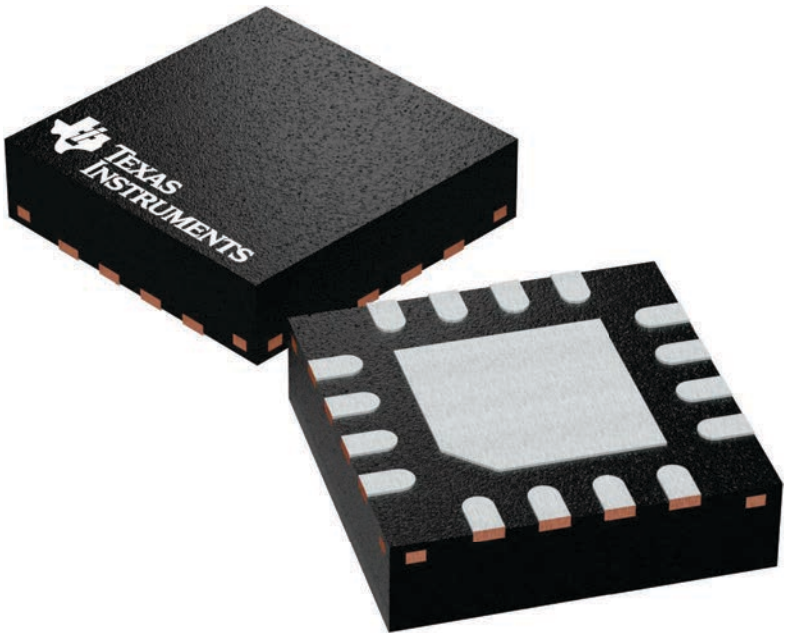
RTE 16

WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

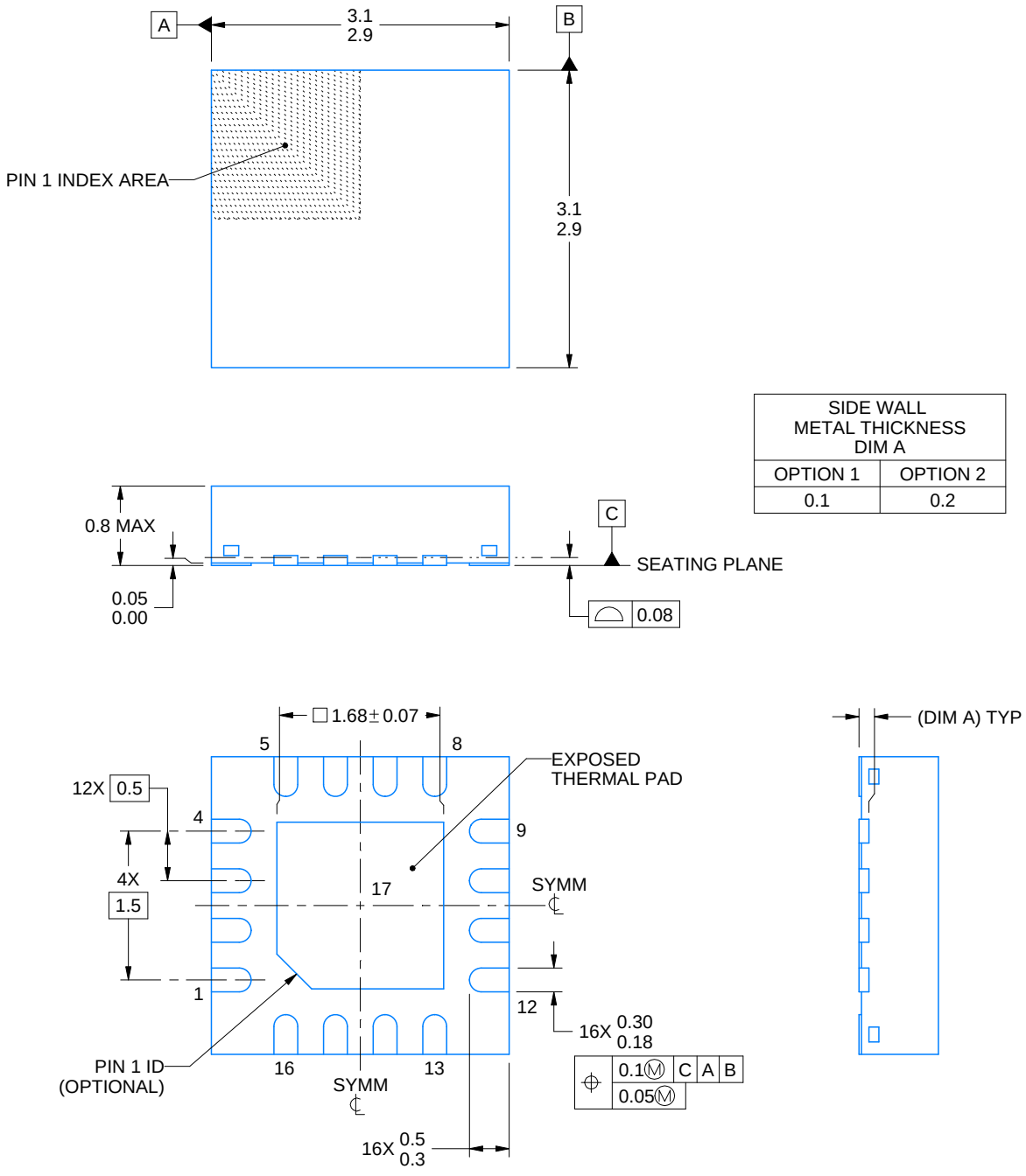


RTE0016C

PACKAGE OUTLINE

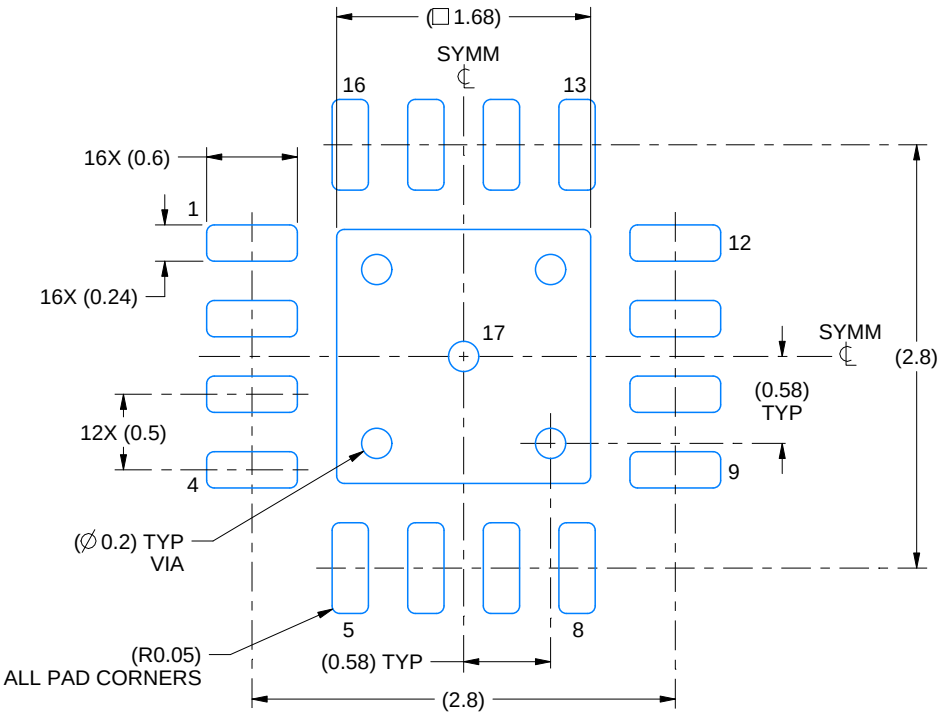
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

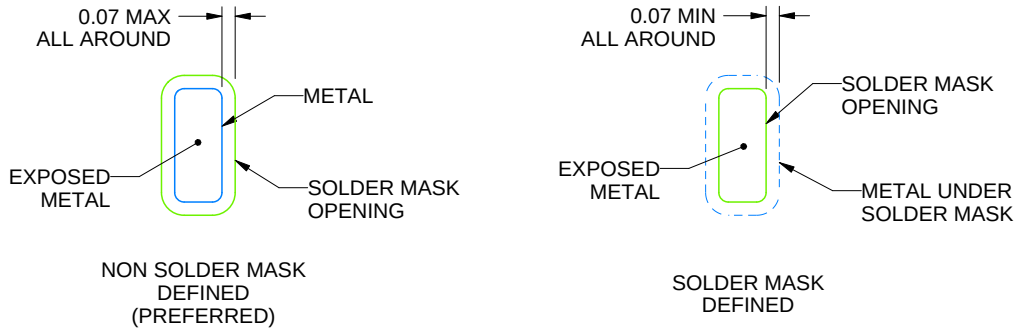


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

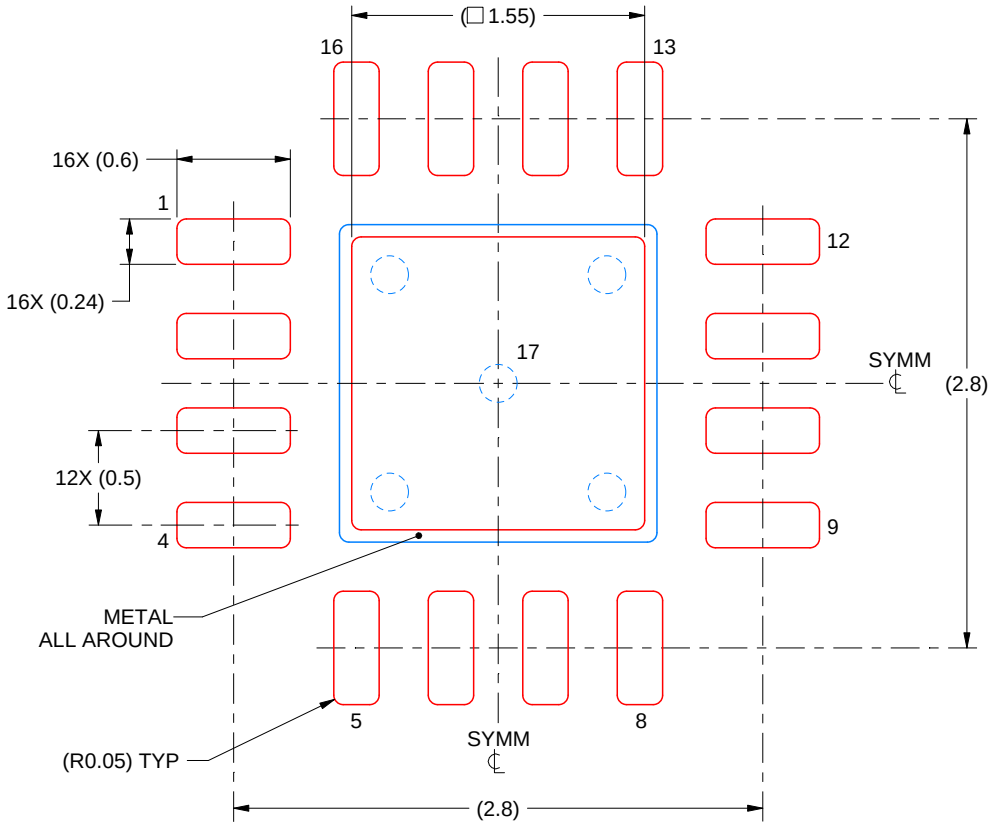


SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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