TEXAS INSTRUMENTS
UCC29002, UCC39002
JAJSSI7J – AUGUST 2001 – REVISED DECEMBER 2023

UCC29002 および UCC39002 高機能 8 ピン負荷共有コントローラ

1 特長

- 高精度、全負荷時に 1% 未満の電流共有誤差を実現
- ハイサイドまたはローサイド (GND 基準) の電流検出機能
- 超低オフセットの電流センス アンプ
- 1 線式負荷共有バス
- フルスケール調整機能
- Intel® SSI 負荷共有仕様に準拠
- スタンバイ時に負荷共有バスから切断
- GND または電源レールへの短絡に対する負荷共有バスの保護機能
- スペースを最小限に抑える 8 ピン VSSOP パッケージ
- 無鉛アセンブリ

2 アプリケーション

- リモート センス機能を搭載したモジュール
- OEM 電源ユニットの内部フィードバック E/A と組み合わせる

製品情報

部品番号	機能差
UCC29002 UCC39002	スタートアップ時に強制的に最大値に設定される調整電流
UCC29002-1	スタートアップ時に誤差電圧に追従する調整電流

3 概要

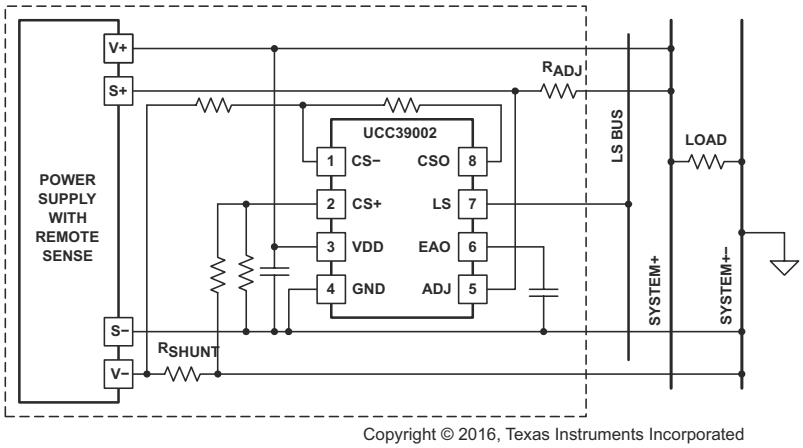
UCC29002 デバイス ファミリは、高機能、高性能、低コストの負荷共有コントローラで構成されており、複数の独立した電源または DC/DC モジュールを並列接続するために必要なすべての機能を提供します。このコントローラは、サーバー、ワークステーション、テレコム、その他の分散電源システムの高信頼性アプリケーションを対象としており、既製の電源の並列接続が必要な N+1 冗長システムや大電流アプリケーションに適しています。

BiCMOS UCC29002 は、旧世代の UC3902 および UC3907 負荷共有コントローラの自動リーダー / フォロワ アーキテクチャをベースにしています。パッケージで調整された非常に低いオフセットの電流センス アンプと、高ゲインの負帰還ループを使用することで、全負荷時のモジュール間の電流共有誤差を 1% 以内に抑えることができます。アンプの同相範囲が VDD 電源レールまで 0V であるため、電流検出抵抗 R_{SHUNT} は GND のリターン パス、または電源の正の出力レールのいずれかに配置できます。

パッケージ情報

部品番号	パッケージ(1)	パッケージ・サイズ (公称)(2)
UCC29002 UCC29002-1(3) UCC39002	SOIC (8)	4.90mm × 6.00mm
UCC29002 UCC39002	VSSOP (8)	3.00mm × 4.90mm
	PDIP (8)	9.81mm × 9.43mm

(1) 詳細は、このデータシートの末尾にある「メカニカル、パッケージ、および注文情報」セクションを参照してください。
(2) パッケージ サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。
(3) UCC29002-1 では、注文用型番に「/1」接尾辞を使用しています。



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代表的なローサイド電流センシング アプリケーション

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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4 Pin Configuration and Functions

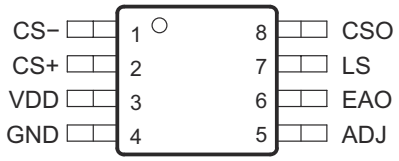


図 4-1. D or DGK Package 8-Pin SOIC or VSSOP Top View

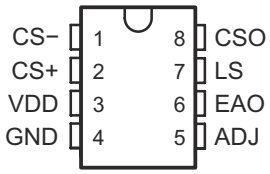


図 4-2. P Package 8-Pin PDIP Top View

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
ADJ	5	O	Adjust amplifier output. This is the buffered output of the error-amplifier block to adjust the output voltage of the power supply being controlled. This voltage on this pin must always be equal to or greater than V_{EAO} + 1V.
CS–	1	I	Current-sense amplifier inverting input.
CS+	2	I	Current-sense amplifier noninverting input.
CSO	8	O	Current-sense amplifier output.
EAO	6	O	Output for load-share error amplifier. (Transconductance error amplifier.)
GND	4	–	Ground. Reference ground and power ground for all device functions. Connect this pin to the negative voltage sense (S-) path of the converter.
LS	7	I/O	Load-share bus. Output of the load-share bus-driver amplifier and input to the load-share bus receiver.
VDD	3	I	Power supply input providing bias voltage to the device. Bypass with a good-quality, low-ESL capacitor with value from 0.1µF to 1µF, placed as close as possible to the VDD and GND pins.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
V_{VDD}	Supply voltage, current-limited source	−0.3	15	V
V_{VDD}	Supply voltage, low-impedance voltage source	−0.3	13.5	V
V_{CS+}, V_{CS-}	Input voltage, current-sense amplifier	–0.3	V_{VDD} + 0.3	V
V_{CSO}	Current-sense amplifier output voltage	−0.3	V_{VDD}	V
V_{LS}	Load-share bus voltage	−0.3	V_{VDD}	V
I_{VDD}	Supply current (I_{VDDq} + I_{CLAMP})		10	mA
V_{ADJ}	Adjust pin input voltage	V_{EAO}+1 V < V_{ADJ} ≤ V_{VDD}		V
I_{ADJ}	Adjust pin sink current		6	mA
T_J	Operating junction temperature	−55	150	°C
T_{stg}	Storage temperature	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{VDD}	Supply voltage, low-impedance voltage source	4.575	13.5	V
V_{CSO}	Current-sense amplifier output voltage	0	V_{VDD} – 1.7	V
V_{LS}	Load-share bus voltage	0	V_{VDD} – 1.7	V
I_{ADJ}	Adjust pin sink current		6	mA

5.4 Thermal Information

THERMAL METRIC(1)		UCC29002, UCC29002-1, UCC39002			UNIT
		D (SOIC)	DGK (VSSOP)	P (PDIP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	111.9	168.0	54.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	58.6	61.9	43.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	52.6	88.8	31.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	12.9	7.3	21.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	52.0	87.2	31.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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5.5 Electrical Characteristics

0 °C < T_A < 70 °C for UCC39002, –40 °C < T_A < 105 °C for UCC29002 and UCC29002-1, T_J = T_A, V_{VDD} = 12V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
GENERAL							
I_{VDDq}	Supply current, idle state	LS = floating (open pin), V_{ADJ} = 5V			2.5	3.5	mA
	VDD clamp voltage	I_{VDD} = 6mA		13.5	14.25	15	V
UNDERVOLTAGE LOCKOUT (UVLO)							
$V_{VDD(on)}$	Start-up voltage threshold[1]	VDD rising		4.175	4.375	4.575	V
	Hysteresis to UVLO	VDD falling		0.2	0.375	0.55	V
CURRENT-SENSE AMPLIFIER							
V_{IO_CS}	Input offset voltage	T_A = 25 °C, V_{IC} = 0.5V or 11.5V, V_{CSO} = 5 V		−100		100	µV
		Variation over operating temperature range			±10		µV/°C
I_{BIAS}	Input bias current (CS+, CS−)			−0.6		0.6	µA
A_V	Voltage gain, DC			75	90		dB
CMRR	Common-mode rejection ratio			75	90		dB
GBW	Gain-bandwidth product[2]				2		MHz
V_{OH_CS}	High-level output voltage (CSO)	0.1V ≤ ([CS+] − [CS−]) ≤ 0.4V, I_{OUT_CSO} = 0mA		10.7	11	11.8	V
V_{OL_CS}	Low-level output voltage (CSO)	−0.4V ≤ ([CS+] − [CS−]) ≤ −0.1V, I_{OUT_CSO} = 0mA		0	0.1	0.15	V
I_{OH_CS}	High-level output current (CSO)	V_{CSO} = 10V		−1	−1.5		mA
I_{OL_CS}	Low-level output current (CSO)	V_{CSO} = 1V		1	1.5		mA
LOAD-SHARE DRIVER (LS)							
V_{RANGE}	Input voltage range			0		10	V
V_{LS}	Output voltage	V_{CSO} = 1V		0.995	1	1.005	V
		V_{CSO} = 10V		9.95	10	10.05	V
V_{OL_LS}	Low-level output voltage	V_{CSO} = 0V, I_{OUT_LS} = 0mA		0	0.1	0.15	V
V_{OH_LS}	High-level output voltage[2]				V_{VDD} − 1.7		V
I_{OUT_LS}	Output current capability	0.5V ≤ V_{LS} ≤ 10V		−1	−1.5		mA
I_{SC_LS}	Short-circuit current	V_{CSO} = 10V, V_{LS} = 0V		−10	−20		mA
V_{SHTDN}	LS driver shutdown threshold	V_{CS-} − V_{CS+}		0.3	0.5	0.7	V
LOAD-SHARE BUS PROTECTION							
I_{ADJ}	Adjust amplifier current, LS protection active	V_{CSO} = 2V, V_{EAO} = 2V, V_{ADJ} = 5V, V_{LS} = V_{VDD}		0	5	10	µA
		V_{CSO} = 2V, V_{EAO} = 2V, V_{ADJ} = 5V, V_{LS} = 0V		0	5	10	µA
ERROR AMPLIFIER							
V_{OH_EA}	High-level output voltage	I_{EAO} = 0mA		3.5	3.65	3.8	V
g_M	Transconductance	−50µA ≤ I_{EAO} ≤ +50µA			14		mS
I_{OH_EA}	High-level output current	V_{LS} − V_{CSO} = 0.4V, R_{EAO} = 2.2kΩ		0.7	0.85	1	mA
ADJ BUFFER							
V_{IO_ADJ}	Input offset voltage[2]	V_{EAO} = 0V, V_{ADJ} = 1.5V			–60		mV
I_{SINK}	ADJ zero-input leakage current	V_{EAO} = 0V, V_{ADJ} = 5.0V		0	5	10	µA
I_{SINK}	ADJ sink current	V_{ADJ} = 5 V, V_{EAO} = 2 V, LS = floating (open)	T_A = 25 °C	3.6	3.95	4.3	mA
			0 °C ≤ T_A ≤ 70 °C	3.45	3.95	4.45	mA
			−40 °C ≤ T_A ≤ 105 °C[3]	3.35	3.95	4.55	mA

(1) Enables the load-share bus at start-up.
(2) Specified by design. Not production tested.
(3) This temperature range does not apply to UCC39002.

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5.6 Typical Characteristics

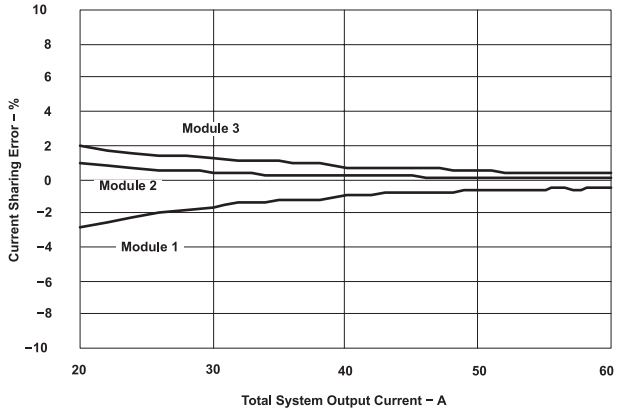


図 5-1. Resultant Load Current Sharing Accuracy, as Measured Across Shunts from the Output of Each Module

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6 Detailed Description

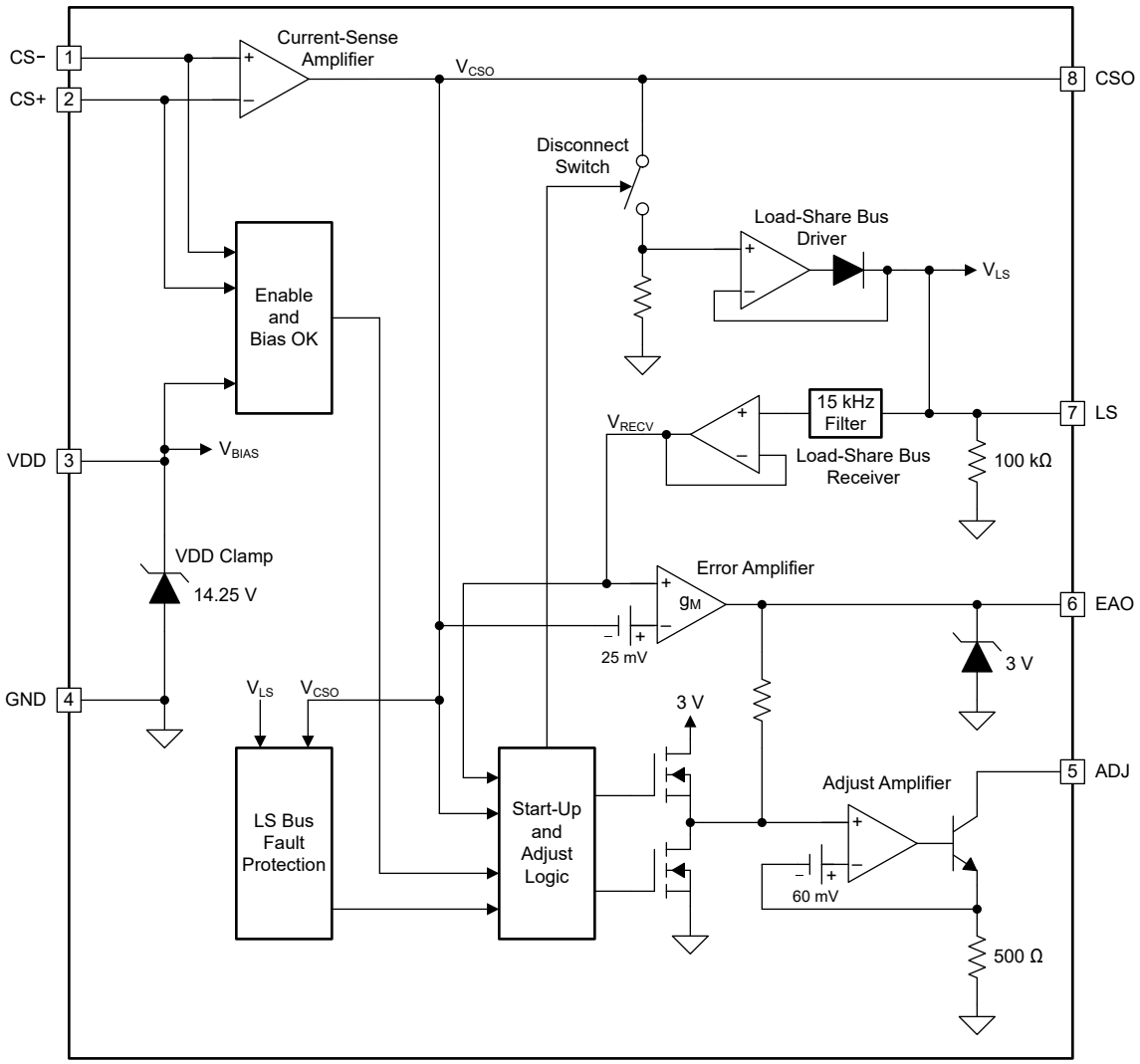
6.1 Overview

The UCC29002 is an advanced, high-performance, low-cost load-share controller that provides all the necessary functions to operate multiple independent power supplies and modules in parallel. The UCC29002 can easily parallel currently available and popular synchronous buck converters, such as those designed with the TPS4005x family of controllers or the newer LM25145 and similar controllers (for example).

Except for reduced operating temperature range and orderable part numbering, all parameters, values, functions, device behavior, and discussions that apply to UCC29002 also apply to UCC39002 throughout this document.

Except where explicitly stated otherwise, all parameters, values, functions, device behavior, and discussions that apply to UCC29002 also apply to UCC29002-1 throughout this document. Different start-up behavior of the UCC29002-1 is discussed in the *Start-Up and Adjust Logic* section.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Differential Current-Sense Amplifier (CS+, CS−, CSO)

The UCC29002 device features a high-gain and high-precision amplifier to measure and amplify the voltage across a low-value current-sense resistor. Because the amplifier is fully uncommitted, the current-sense gain is user-programmable. The current-sense amplifier is not unity-gain stable and must have a minimum gain of 3.

The extremely-low input offset voltage of the UCC29002 current-sense amplifier makes it suitable to measure current information across a low-value resistance to reduce power loss. Furthermore, the amplifier's input common-mode range includes the ground and positive supply rails (GND and VDD) of the UCC29002. Accordingly, the current-sense resistor can be placed either in the ground return path or in the positive output rail of the power supply V_{OUT} as long as $V_{OUT} \leq V_{VDD}$.

6.3.2 Load-Share Bus Driver Amplifier (CSO, LS)

The load-share bus driver is a unity-gain buffer amplifier to provide separation between the output of the current-sense amplifier and the load-share bus voltage. The circuit implements an *ideal diode* with virtually 0V forward voltage drop by placing the diode inside the feedback loop of the amplifier. The diode function is used to automatically establish the role of the leader module in the overall load-sharing system. In the system, the UCC29002 device that becomes the leader uses the load-share bus driver amplifier to drive its output-current information onto the load-share bus for all follower modules to emulate.

Assuming identical module design, any UCC29002 may assume the role of leader at any time depending on input and output conditions. Leadership is not fixed to one specific module. All follower modules will have lower output current levels by definition, and their *ideal diodes* are reversed biased ($V_{CSO} < V_{LS}$). Consequently, the follower V_{CSO} and V_{LS} signals will be separated. This separation allows the error amplifier of the follower UCC29002 device to compare its respective module output current to the output current of the leader module and make the necessary feedback-loop adjustments to achieve a balanced current distribution.

Because the LS bus is always driven by a single load-share bus driver (in the leader module), the total number of load-sharing modules (N_m) that may be connected to the LS bus is limited by the output-current capability of the leader's bus-driver amplifier according to 式 1.

$$N_m = \frac{I_{OUT,\,MIN}}{\left(V_{LS,\,FULL_SCALE}/100\ k\Omega\right)} \tag{1}$$

where

- $I_{OUT,MIN}$ is the minimum limit of I_{OUT_LS} given in the *Electrical Characteristics* table.
- $V_{LS,FULL_SCALE}$ is the maximum voltage on the LS bus at full load.
- 100kΩ is the input impedance of the LS pin as shown in the *Functional Block Diagram*.

注

The number of parallel modules N_m can be increased by reducing the full-scale LS bus voltage, that is, by reducing the current-sense amplifier gain A_{CSA} of all modules (provided that $A_{CSA} > 3$). However, lower A_{CSA} reduces current-sharing accuracy.

6.3.3 Load-Share Bus Receiver Amplifier (LS)

The load-share bus receiver amplifier is a unity-gain buffer that monitors the voltage on the LS bus. The primary purpose of this amplifier is to ensure that the LS bus is not loaded by internal impedances (other than the 100kΩ) of the UCC29002 device. The LS bus receiver amplifier is internally compensated and has a 15kHz filter on its non-inverting input. To maintain stability, avoid adding significant external capacitance to the LS pin.

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6.3.4 Error Amplifier (EAO)

As shown in the *Functional Block Diagram*, the UCC29002 uses an operational transconductance amplifier (OTA) often referred to as a g_M-type error amplifier. The g_M amplifier is chosen because it requires only one pin – the output – to be accessible for compensation. This amplifier generates an output current that is proportional to the difference of its noninverting and inverting input voltages. This output current flows out of the EAO pin and developes an error voltage V_{EAO} across the current-loop compensation components connected between the EAO pin and ground.

The purpose of the error amplifier (EA) is to compare the output current level of the respective module monitored by the UCC29002 device (represented by V_{CSO}) to the leader module's current level (represented by V_{LS}) and generate V_{EAO}. V_{EAO} is then used by the Adjust amplifier to adjust the respective module's voltage feedback signal in a way which tends to minimize V_{EAO}. This process results in nearly-equal output currents among the parallel-operated power supply modules.

In cases where the UCC29002 device assumes the role of the leader load-share controller in the system or it is used together with a stand-alone power module, its V_{LS} voltage is approximately equal to its amplified current signal V_{CSO}. To avoid erroneous output voltage adjustment, the input of the error amplifier incorporates an offset to ensure that its inverting input is biased 25mV (typical) higher than its noninverting input. Consequently, when the two input signals to the EA are equal, no adjustment is made and the initial output voltage set-point of the leader module is maintained. The V_{CSO} of follower modules are necessarily at least 25mV lower than the leader's V_{CSO}.

The EA output V_{EAO} is clamped to V_{OH_EA} as specified in the *Electrical Characteristics* table.

6.3.5 Adjust Amplifier Output (ADJ)

A feedback-loop adjustment current I_{ADJ}, proportional to the error voltage V_{EAO} on pin 6, is sunk by the ADJ pin. This current flows through the parallel combination of the module's remote-sense resistor R_{SENSE} and the adjust resistor, R_{ADJ}. The effect of I_{ADJ} is to increase the output voltage of the module influenced by the UCC29002 device. The amplitude of I_{ADJ} is set by the 500Ω internal resistor between the emitter of the amplifier's open-collector output transistor and ground shown in the *Functional Block Diagram*. Use 式 2 to calculate the magnitude of I_{ADJ}. Maximum I_{ADJ} occurs at maximum V_{EAO}.

$$I_{ADJ} = \frac{V_{EAO}}{500\ \Omega} \tag{2}$$

At the leader module, V_{EAO} is 0V and consequently the adjust current must be zero as well. Therefore, the output voltage of the leader module remains at its initial output voltage set point at all times.

During the start-up mode of the UCC29002, the noninverting input of the Adjust amplifier is switched to 3V to increase the module's output voltage significantly and quickly match the starting module's output current to the other modules' currents.

In cases of insufficient VDD bias level, LS bus fault, or disabled UCC29002 (by CS+, CS- inputs), the noninverting input of the Adjust amplifier is switched to ground to prevent erroneous adjustment of the module's output voltage by the load-share controller.

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6.3.6 Enable Function (CS+, CS−)

The two inputs of the current-sense amplifier are also used with an Enable Comparator to implement an ENABLE function in the UCC29002 device. During normal operation, the difference between CS− and CS+ voltages is very small and the internal -0.5V offset added between the CS− pin and the inverting input of the comparator ensures that the UCC29002 is always enabled.

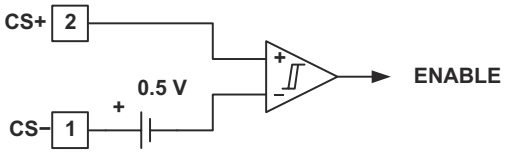


図 6-1. Enable Comparator

By forcing the CS− pin at least 0.5V higher than the CS+ pin, the ENABLE signal becomes false and the UCC29002 is set into a disabled mode. While disabled, the UCC29002 disconnects from the load-share bus and the Adjust amplifier current is forced to zero.

When using high-side current-sensing (R_{SHUNT} located in the module output voltage rail), CS− must not be forced higher than 0.3V above VDD. Instead, in this configuration CS+ should be pulled at least 0.5V below CS− to disable the UCC29002.

The ENABLE signal is combined with the BIAS OK signal (logical AND function) and affects the UCC29002 operating mode through the *Start-Up and Adjust Logic* block.

6.3.7 Fault Protection on LS Bus

Accidentally, the load-share bus might be short-circuited to the positive bias voltage of the UCC29002 device or to ground. These events can result in erroneous output voltage adjustment. For that reason, the LS bus voltage is continuously monitored by a window comparator as shown in 図 6-2. An LS-bus FAULT condition is asserted if either [V_{LS} > (V_{VDD} - 0.7 V)] or [V_{LS} < (2/3 × V_{CSO})] is true.

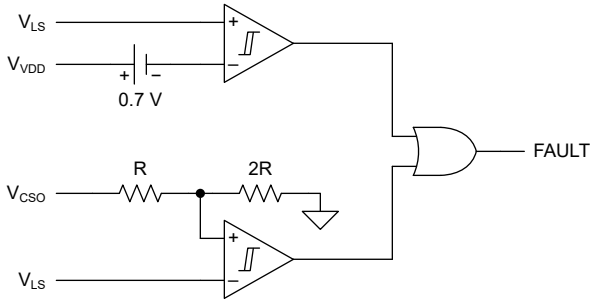


図 6-2. LS Bus Fault Protection Comparators

The LS-bus FAULT signal is handled by the *Start-Up and Adjust Logic* block to affect the UCC29002 operating mode. If the FAULT signal is asserted true, the UCC29002 is disabled.

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6.3.8 Start-Up and Adjust Logic

The start-up and adjust logic imposes certain operating modes on the load-share controller during start-up, fault, and disable conditions. Under these circumstances the information obtainable by the error amplifier of the UCC29002 device may not be sufficient to make the correct output voltage adjustment, therefore the adjust amplifier may be forced to a known state. Additionally, the LS bus driver of UCC29002 device is disabled during these conditions.

The start-up and adjust logic in the UCC29002-1 is different than that in the UCC29002 and UCC39002. The behavior of the UCC29002, UCC39002, and UCC29002-1 are identical for LS bus fault and disable conditions. However for the initial start-up condition, the UCC29002-1 behavior is different from the other devices and this difference is discussed in the following paragraphs.

The UCC29002 and UCC39002 devices have a defined start-up mode which is active as long as V_{CSO} of the module that is starting up is less than 80% of the voltage on the LS pin. Because the output current of the starting module is low compared to the currents of the other modules in the system (represented by V_{LS}), the start-up mode logic disables the LS Bus Driver by the disconnect switch and applies 3V to the Adjust amplifier noninverting input to sink the maximum current through the adjust resistor. This operating mode causes the starting module to very quickly engage in sharing the load current because its output is adjusted to a sufficiently high voltage immediately at turn-on. Start-up mode is exited as soon as V_{CSO} exceeds 80% of V_{LS}, and the load-share bus driver and the adjust amplifier revert to normal operation.

In contrast, the UCC29002-1 device has some of the start-up logic disabled and has no defined start-up mode. Specifically, the UCC29002-1 does not apply 3V to the Adjust amplifier regardless of V_{CSO} level at any time and the LS bus driver is not disabled at start-up. The Adjust amplifier current rises as V_{EAO} rises. This difference allows the starting module with UCC29002-1 to engage its load-sharing at a slower rate. The UCC29002-1 version may be preferable for applications where the disturbance of rapid load-sharing start-up may be undesireable.

In cases of detecting the VDD bias voltage less than the minimum operating level, external disabling of the controller using the CS+ and CS− pins, or detecting an LS-bus fault condition, all three versions UCC29002, UCC39002, and UCC29002-1 act to disconnect the LS Bus Driver and ground the Adjust amplifier input.

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6.3.9 Bias Input and Bias_OK Circuit (VDD)

The UCC29002 device is built on a high-performance 15V BiCMOS process. Therefore, the absolute maximum voltage across the VDD and GND pins (pin 3 and 4 respectively) is limited to 15V. The recommended maximum operating voltage is 13.5V which corresponds to the minimum tolerance limit of the on-board 14.25V Zener-like active clamp circuit. In case the bias voltage source exceeds the 13.5V limit, the UCC29002 device can be powered through a current-limiting resistor. The total current into the VDD pin (I_{VDDq} + I_{CLAMP}) must be limited to 10mA as listed in the *Absolute Maximum Ratings* table.

The bypass capacitor for the VDD pin is also the compensation for the input active clamp of the device and, as such, must be placed as close to the device pins (VDD and GND) as possible, using a good-quality, low-ESL capacitor, including trace length. The device is optimized for a capacitor value of 0.1µF to 1µF.

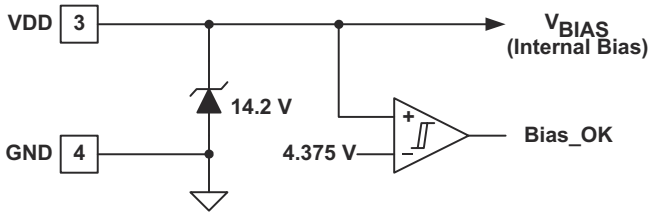


図 6-3. VDD Clamp and Bias Monitor

The UCC29002 device uses a comparator with hysteresis to monitor the VDD bias voltage for minimum sufficiency. does not have an undervoltage lockout circuit. On initial power-up while VDD < 4.375V, the load-share control functions are disabled. The Bias_OK comparator works as an enable function when VDD rises above the 4.375V enable threshold. After the device is enabled, the Bias_OK signal will remain true until VDD falls below the 4.0V disable threhsold. While this might be inconvenient for some low-voltage applications, this feature is necessary to obtain high accuracy. The load-share accuracy is dependent on working with relatively large signal amplitudes on the load-share bus. If the internal offsets, current-sense error, and ground potential difference between the UCC29002 controllers are comparable in amplitude to the load-share bus voltage, they can cause a significant current-distribution error in the system.

The maximum voltage on the load-share bus is limited to approximately 1.7V below the bias voltage level (V_{VDD}) which would result in an unacceptably low load-share bus amplitude and therefore poor accuracy at low VDD levels. To circumvent this potential design problem, the UCC29002 device does not operate below the previously mentioned 4.0V bias voltage disable threshold. If the system does not have a suitable bias voltage source available to power the UCC29002, TI suggests using an inexpensive charge pump from the output rail which can generate the bias voltage for one or all of the UCC29002 devices in the load-share system.

The maximum VDD of the UCC29002 device is 15V. For load-sharing applications with higher-voltage outputs, use the application solution as recommended in 図 7-2. A Zener-like clamp on the VDD pin is provided internally so the device can be powered from higher-voltage rails using a minimum number of external components.

The current-sense amplifier (CSA) inputs must be configured so that their absolute maximum voltage ratings are not exceeded. It is not a simple matter to level-shift mV-level current-sense signals from a high-voltage power supply rail down to the CSA inputs without incurring severe distortion from noise, divider tolerances, and offsets. This means that in most high-voltage applications, it is best practice to locate the current-sense resistor R_{SHUNT} in the GND-return path of the power supply output.

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6.4 Device Functional Modes

6.4.1 Start-Up Mode

During the start-up mode of the UCC29002 and UCC39002 devices, the Load-Share Bus Driver is disabled and the Adjust amplifier is forced to sink the maximum current through the adjust resistor.
Start-up mode ends when $V_{CSO} > 0.8 \times V_{LS}$.

During the start-up mode of the UCC29002-1 device, the Load-Share Bus Driver is disabled and the Adjust amplifier is allowed to follow the programming of the Voltage Error Amplifier output voltage.
Start-up mode ends when $V_{CSO} > 0.8 \times V_{LS}$.

For details about Start-Up Mode, see the *Start-Up and Adjust Logic* section.
Start-Up Mode can only be entered when Disable Mode and Fault Mode are not active.

6.4.2 Normal Running Mode

The UCC29002 device operates in the Normal Running Mode when not starting up, when not faulted, and when not disabled. In Normal Running Mode, the CSO output is connected to the LS Bus Driver and the Adjust amplifier input follows the Error Amplifier output voltage to sink a current at the ADJ pin.

The LS Bus Driver output drives the LS Bus in the system if the CSO voltage is higher than all other CSO voltages in the system. In this case, the UCC29002 assumes the role of load-share leader. If the CSO output is lower than the voltage at the LS pin, the device assumes the role of load-share follower. Depending on system conditions, the UCC29002 device can change roles from leader to follower, or vice-versa, and back again any number of times. Either situation is a normal running condition.

6.4.3 Fault Mode

Operation in this mode occurs if the LS pin is short-circuited high (to the VDD rail) or low (to GND). Under either of these conditions the device responds by pulling the inverting input of the Adjust amplifier to GND, which forces I_{ADJ} to zero. For details, see the *Fault Protection on LS Bus* section.

6.4.4 Disabled Mode

The UCC29002 device operates in this mode when the current-sense amplifier inputs are biased as described in the *Enable Function (CS+, CS–)* section, or when the VDD voltage is below the start-up threshold as described in the *Bias and Bias OK Circuit (VDD)* section, or when a bus-fault condition has been detected as described in the *Fault Protection on LS Bus* section.

In this mode, the UCC29002 device CSO output is disconnected from the LS Bus and the Adjust amplifier input is grounded to set the ADJ current to zero.

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7 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

The UCC29002 device is an advanced, high-performance load-share controller that provides all the necessary functions to parallel multiple independent power supplies or DC-to-DC modules. This load-share circuit is based upon the automatic leader/follower architecture used in the earlier-generation UC3907 and UC3902 load-share controllers, providing better than 1% current-share error between the parallelled modules at full system load.

7.2 Paralleling the Power Modules

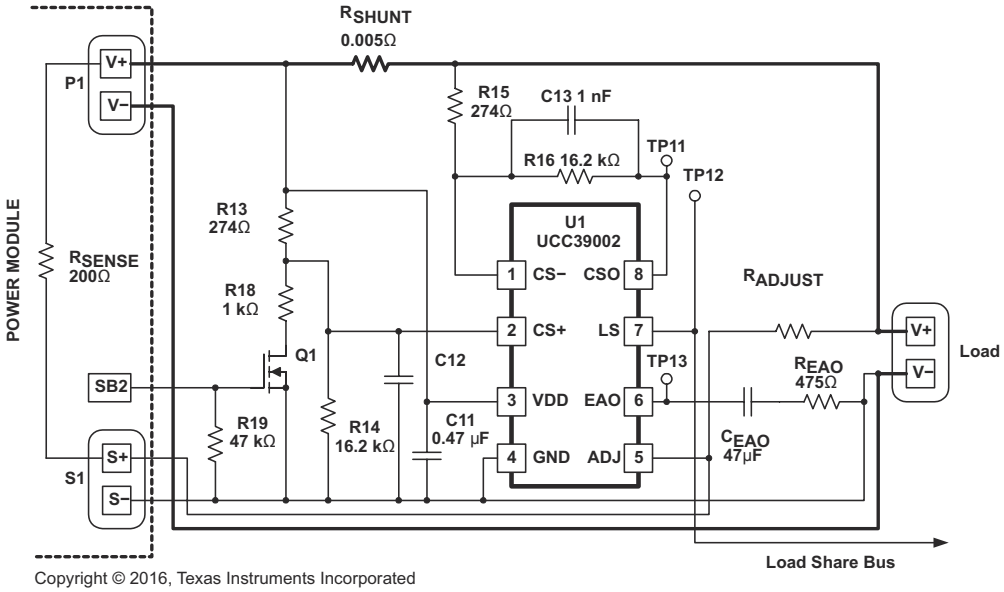
The symbols used in this section are defined as:

V_{OUT}	The nominal output voltage of the modules to be paralleled.
$I_{OUT(max)}$	The maximum output current of each module to be paralleled.
$\Delta V_{ADJ(max)}$	The maximum output voltage adjustment range of the power modules to be paralleled.
N_m	The number of power modules to be paralleled.

注

The power modules to be paralleled must be equipped with true remote-sense inputs or with access to the feedback divider network of the module's error amplifier.

図 7-1 shows a typical high-side current-sense configuration for a single module which is repeated for each module to be paralleled. Direct connection of the VDD pin to the power module V_{OUT} rail (V+) is valid for V_{OUT} less than 13.5V.



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図 7-1. Typical High-Side Application for a Single Power Module

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In 図 7-1, P1 represents the output-voltage connector terminals of the module and S1 represents the remote-sense connector terminals of the module. In this example, a signal on the SB2 terminal enables the disconnect feature of the device. The Load-Share Bus is the common bus between all of the paralleled load-share controllers. The VDD supply must be decoupled with a good-quality ceramic capacitor returned directly to GND.

For applications where the module output voltage is higher than the maximum VDD rating, it is best practice to configure R_{SHUNT} in the GND-return rail as shown in 図 7-2. The VCC pin is biased from V_{OUT} using dropping resistor R_{BIAS1} to limit current and the ADJ pin is buffered from V_{OUT} by an NPN transistor.

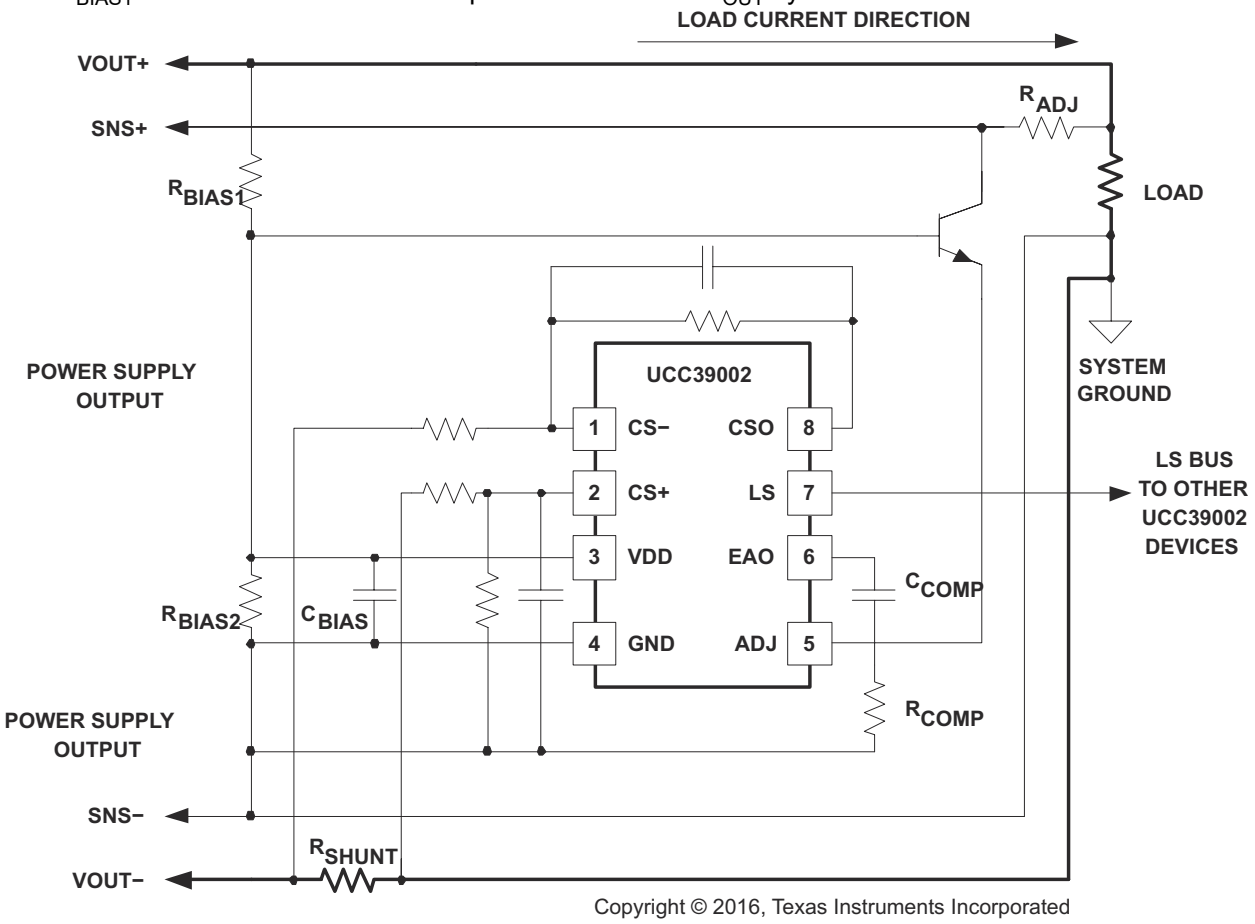


図 7-2. High-Voltage Application with Low-side Current-Sensing

7.3 Typical Application

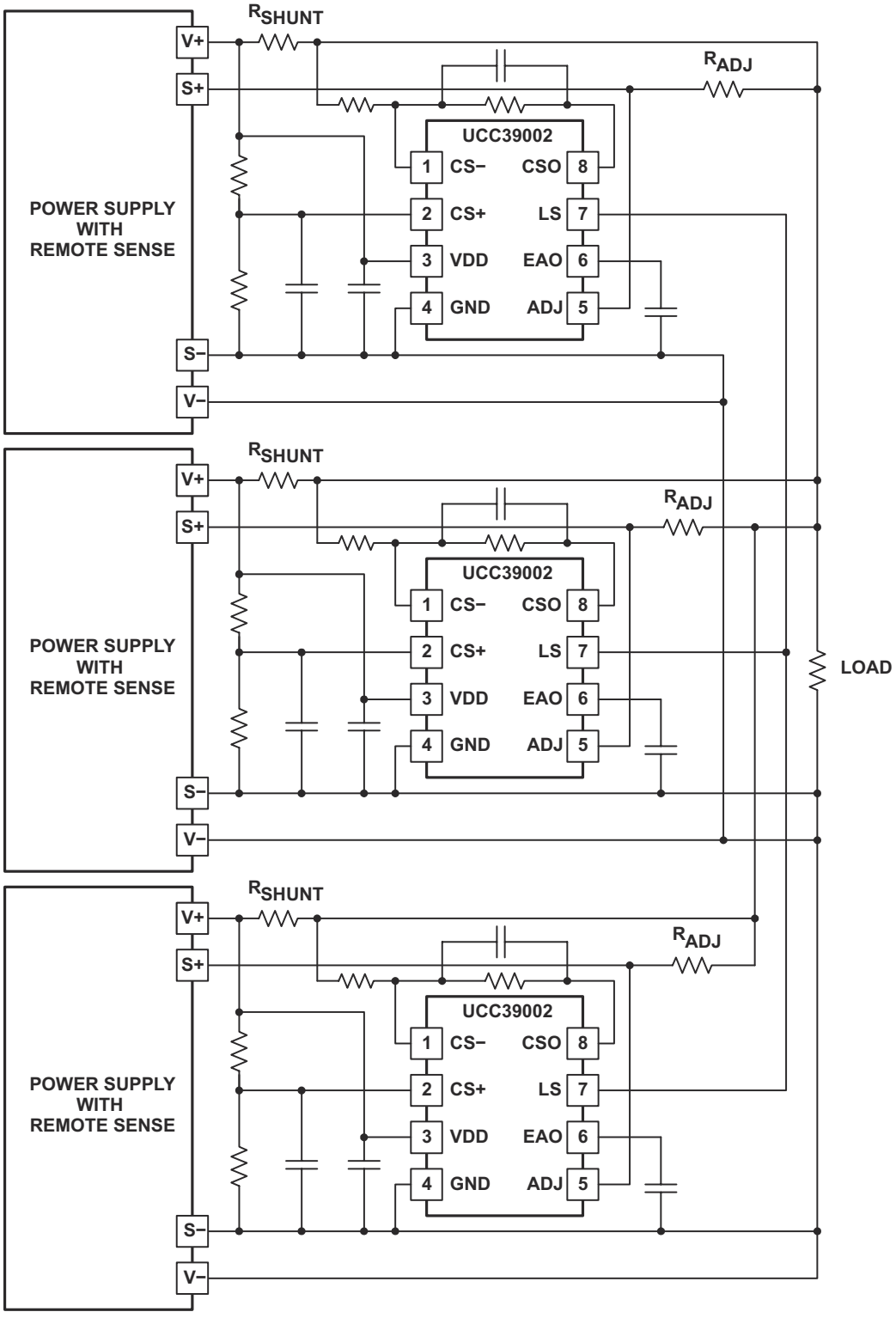


図 7-3. Three-Module Sharing Example with High-Side Current-Sensing, System V_{OUT} < 13.5V

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7.3.1 Measuring the Voltage Loop of a Power Module

Using the test configuration shown in 図 7-4, measure the unity-gain crossover frequency of each power module to be paralleled. Set the load to the maximum output current ($I_{OUT(max)}$) to be shared by each module. 図 7-5 shows a typical resultant Bode plot. Select the plot with the lowest 0dB crossover frequency and assign that frequency to $f_{CO(module)}$ for design use.

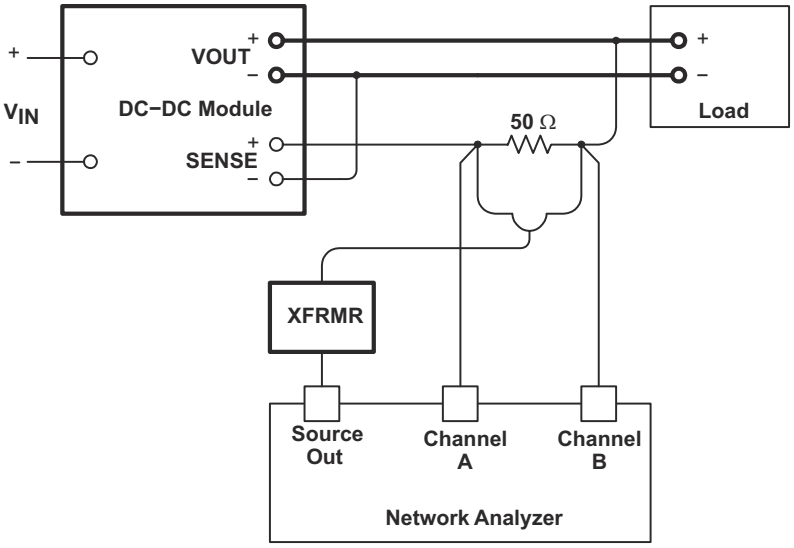


図 7-4. Connection Diagram for Unity-Gain Crossover Frequency Measurement

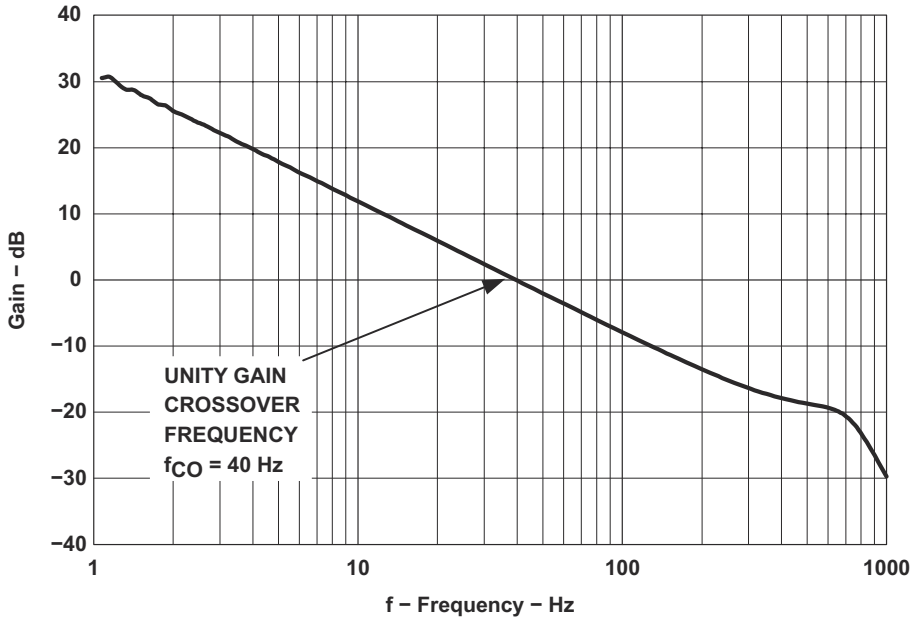


図 7-5. Power Module Bode Plot

7.3.2 Detailed Design Procedure

This section is a practical step-by-step design procedure on how to set up the UCC29002 to parallel power modules for load sharing.

7.3.2.1 The Shunt Resistor

Selection of the shunt resistor R_{SHUNT} value is limited (in part) by the voltage drop that is developed by the maximum load-sharing current of the module. This voltage drop should be much less than the maximum voltage adjustment range $\Delta V_{ADJ(max)}$ of the module by at least a factor of 10, as shown in 式 3.

$$I_{OUT(max)} \times R_{SHUNT} << \Delta V_{ADJ(max)} \tag{3}$$

Other limitations for R_{SHUNT} include the maximum allowable power dissipation and available component ratings. On the other hand, the value of R_{SHUNT} should be high enough to avoid signal degradation from noise or requiring excessive amplification by the CSA.

7.3.2.2 The CSA Gain

The gain of the current-sense amplifier (CSA) is set by the compensation components connected to the CS− and CSO pins of the load-share device. The maximum allowable voltage at CSO is limited by the internal saturation level of the CSA and must be at least 1.7V less than VDD as seen in 式 4.

$$V_{CSO(max)} < V_{VDD} - 1.7\ V \tag{4}$$

$V_{CSO(max)}$ can be targeted lower than this limit and the maximum current-sense amplifier gain is determined by 式 5.

$$A_{CSA} = \frac{V_{CSO(max)}}{I_{OUT(max)} \times R_{SHUNT}} \tag{5}$$

Referring to 図 7-1, the DC gain of the CSA is equal to R16/R15, and a high-frequency roll-off pole used for noise filtering is set by C13. These component values are repeated at R14, R13, and C12 on the CS+ pin of the differential amplifier, as shown.

The CSA output voltage, V_{CSO}, serves as the input to the unity-gain LS-bus driver. In the overall system, the module with the highest V_{CSO} output voltage becomes the leader module. It forward-biases the internal diode at the output of its respective LS-bus driver and determines the voltage on the load-share bus, V_{LS}. All other modules with lower V_{CSO} act as followers and they present a load on the I_{VDD} of the leader module because of their internal 100kΩ resistors at their respective LS pins. The total additional bias-supply current for the leader module is equal to $N_m \times (V_{LS(max)}/100k\Omega)$.

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7.3.2.3 Determining R_{ADJ}

The ADJ pin of the load-share controller is connected to the positive remote-sense terminal (SENSE+, SNS+, S+) of the power supply module. In cases where the remote-sense function of a module is not used, an internal low-value resistor, herein designated as R_{SENSE}, connects the module's internal feedback divider network to its output voltage rail to maintain regulation. A controlled current pulled through R_{SENSE} by the ADJ pin can adjust the output voltage of the module slightly higher to overcome unbalanced distribution impedances and offsets that degrade current-sharing between multiple power modules operating in parallel. Since no current can flow out of the ADJ pin, the output voltage of a module cannot be decreased below its normal set-point.

In cases where the R_{SENSE} value is relatively high, the maximum ADJ current $I_{ADJ(max)}$ may increase the module's V_{OUT} too much. In such cases, an external adjustment resistor R_{ADJ} is connected between the ADJ pin and the V_{OUT} rail after R_{SHUNT}. This arrangement places R_{ADJ} effectively in parallel with R_{SENSE} and an artificial SENSE+ voltage is created by the voltage drop across $R_{ADJ} \| R_{SHUNT}$ due to the current sunk by the internal NPN transistor at the ADJ pin. R_{ADJ} scales the portion of I_{ADJ} that can flow through R_{SENSE} to limit the maximum amount of voltage adjustment $\Delta V_{ADJ(max)}$ allowable for the module. There are two operating requirements that determine the minimum value of R_{ADJ}.

The voltage at the ADJ pin must be maintained at least 1V above the voltage at the EAO pin which is necessary to keep the transistor at the output of the internal adjust amplifier from saturating. To fulfill this requirement, use 式 6 to calculate the R_{ADJ} value.

$$R_{ADJ} = \frac{\left(\Delta V_{ADJ(max)} - I_{OUT(max)} \times R_{SHUNT}\right)}{\left[\left(\frac{V_{OUT} - \Delta V_{ADJ(max)} - 1\,V}{500\,\Omega}\right) - \left(\frac{\Delta V_{ADJ(max)}}{R_{SENSE}}\right)\right]} \tag{6}$$

where (referring to 図 7-1)

- R_{SHUNT} is the external current-sense resistor.
- R_{SENSE} is the internal remote-sense resistance between V+ (same as V_{OUT}) and S+ within the power module.

The total current into the ADJ pin must also be considered. The maximum sink current for ADJ, $I_{ADJ(max)}$, is 6mA as determined by the internal 500Ω emitter resistor and the 3V clamp. The value of adjust resistor, R_{ADJ}, is based upon the maximum adjustment range of the module, ΔV_{ADJmax}. Use 式 7 to calculate the value of the adjust resistor.

$$R_{ADJ} \geq \frac{\left(\Delta V_{ADJ(max)} - I_{OUT(max)} \times R_{SHUNT}\right)}{\left[I_{ADJ(max)} - \left(\frac{\Delta V_{ADJ(max)}}{R_{SENSE}}\right)\right]} \tag{7}$$

By selecting a resistor value that meets both of these requirements, the ADJ pin is at least 1V greater than the EAO voltage and the ADJ pin sink current should not exceed the 6mA maximum. 式 6 tends to dominate the requirements when the power module output voltage is relatively low (close to the UCC29002 start-up threshold $V_{VDD(on)}$), whereas 式 7 tends to dominate the requirements when V_{OUT} is relatively high.

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7.3.2.4 Error Amplifier Compensation

The total load-share loop unity-gain crossover frequency, f_{CO}, must be set at least one decade below the lowest measured crossover frequency of the paralleled modules previously measured, $f_{CO(module)}$ (see 図 7-5). Compensation of the transconductance error amplifier is accomplished by connecting a compensation resistor, R_{EAO}, in series with a capacitor, C_{EAO}, between EAO and GND. Use 式 8 and 式 13 to calculate the values of these components. C_{EAO} is calculated first.

$$C_{EAO} \geq \left(\frac{g_M}{2\pi \times f_{CO}}\right) \times \sqrt{2} \times A_{CSA} \times A_V \times A_{ADJ} \times \left|A_{PWR}(f_{CO})\right| \quad (8)$$

where

- g_M is the transconductance of the Error Amplifier, typically 14mS.
- f_{CO} is the targeted crossover frequency of the load-share loop, minimally $f_{CO(module)}/10$, preferably even lower
- A_{CSA} is the DC gain of the Current-Sense Amplifier. (R15, R16 refer to 図 7-1.)
- A_V is the maximum voltage gain.
- A_{ADJ} is the gain associated with the Adjust amplifier.
- $|A_{PWR}(f_{CO})|$ is the measured gain of the power module at the targeted load-share crossover frequency, f_{CO}, converted from dB to V/V.

$$A_{CSA} = \frac{R16}{R15} \quad (9)$$

$$A_V = \frac{R_{SHUNT}}{R_{LOAD}} = \frac{I_{OUT(max)} \times R_{SHUNT}}{V_{OUT}} \quad (10)$$

$$A_{ADJ} = \frac{R_{ADJ} \parallel R_{SENSE}}{500\ \Omega} = \frac{R_{ADJ} \times R_{SENSE}}{\left(R_{ADJ} + R_{SENSE}\right) \times 500\ \Omega} \quad (11)$$

$$\left|A_{PWR}(f_{CO})\right| = 10\left(\frac{G_{MODULE}(f_{CO})}{20}\right) \quad (12)$$

where

- $G_{MODULE}(f_{CO})$ is the measured value of the gain (in dB) from 図 7-5, at the targeted load-share crossover frequency.

After the value of the C_{EAO} capacitor is determined, the R_{EAO} value is calculated to achieve the desired current-sharing loop response using 式 13.

$$R_{EAO} = \frac{1}{2\pi \times f_{CO} \times C_{EAO}} \quad (13)$$

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7.3.3 Application Curve

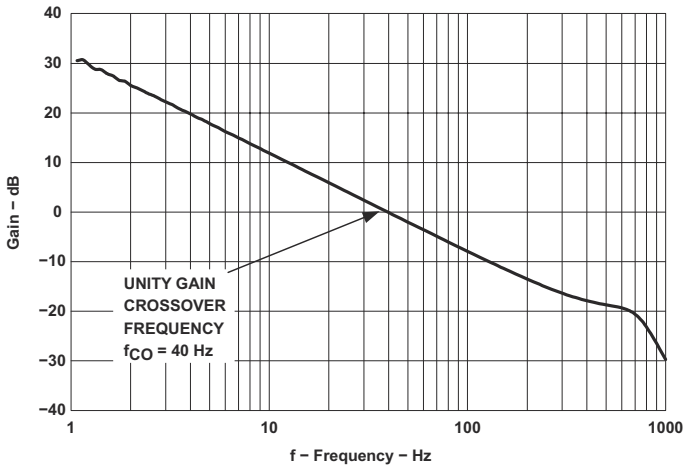


図 7-6. Power Module Bode Plot

7.4 Power Supply Recommendations

The VDD bias voltage to the UCC29002 device is limited to a maximum of 13.5V when powered from a low-impedance source. An internal clamp-circuit (nominally 14.25V) allows the use of higher bias-supply source voltages provided that a suitable resistance is connected between the high-voltage source and the VDD pin to limit the total VDD current to below its absolute maximum rating.

When used with a series resistor to limit I_{VDD}, the VDD pin must be decoupled directly to the GND pin with a good-quality ceramic capacitor. The device is optimized for a capacitor value from 0.1µF to 1µF. Values outside of this range may result in unstable clamping voltage.

7.5 Layout

7.5.1 Layout Guidelines

The bypass capacitor for the VDD supply is also the compensation for the input active clamp of the device and, as such, must be placed as close to the device pins (VDD and GND) as possible using a good-quality, low-ESL capacitor, minimizing trace length.

7.5.2 Layout Example

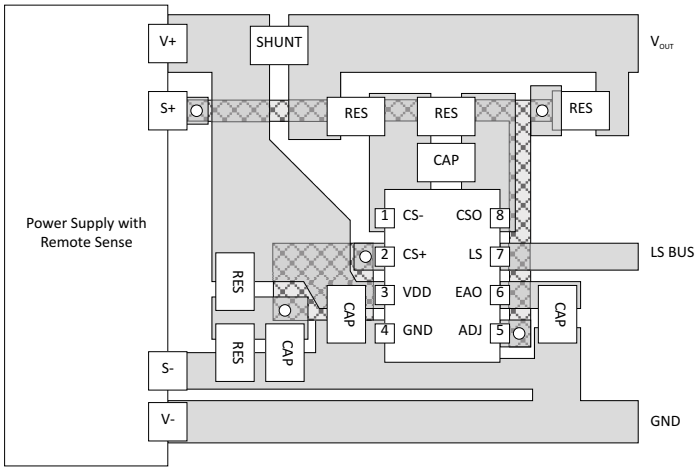


図 7-7. Layout Example (2-Layer PCB)

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.1.1 Documentation Support

8.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 8-1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
UCC29002 UCC29002-1	Click here	Click here	Click here	Click here	Click here
UCC39002	Click here	Click here	Click here	Click here	Click here

8.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision I (May 2016) to Revision J (December 2023)	Page
• 「製品情報」表の「パッケージ情報」を変更	1
• Corrected unit for LS Driver output current parameter and min/max limits for LS Driver output voltage in the *Electrical Characteristics* table, plus numerous editorial clarifications	5
• Changed Functional Block Diagram	7

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- Changed LS Bus Fault Comparators diagram....10
- Changed Start-up description for UCC29002-1 device 11
- Updated and expanded *Device Functional Modes* 13
- Moved *Paralleling the Power Modules* and *Measuring the Voltage Loop of a Power Module* to this section.. 14
- Corrected equations and clarified text....18

Changes from Revision H (August 2007) to Revision I (May 2016) **Page**

- 「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加....1

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

注

Orderable part numbers for the UCC29002-1 device use a "/1" suffix instead of "-1" suffix due to ordering-system restrictions on the "-" character.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC29002D/1	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 105	290021
UCC29002DGK	Obsolete	Production	VSSOP (DGK) | 8	-	-	Call TI	Call TI	-40 to 105	29002
UCC29002DGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 105	29002
UCC29002DGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 105	29002
UCC29002DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	29002
UCC29002DR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	29002
UCC29002DR/1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	290021
UCC29002DR/1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	290021
UCC29002DR/1.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	290021
UCC29002DRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	29002
UCC29002DRG4.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	29002
UCC29002P	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 105	UCC29002P
UCC29002P.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 105	UCC29002P
UCC39002D	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	39002
UCC39002DGK	Obsolete	Production	VSSOP (DGK) | 8	-	-	Call TI	Call TI	0 to 70	39002
UCC39002DGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG | SN	Level-2-260C-1 YEAR	0 to 70	39002
UCC39002DGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	0 to 70	39002
UCC39002DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	39002
UCC39002DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	39002
UCC39002DR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	39002
UCC39002P	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UCC39002P
UCC39002P.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UCC39002P

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

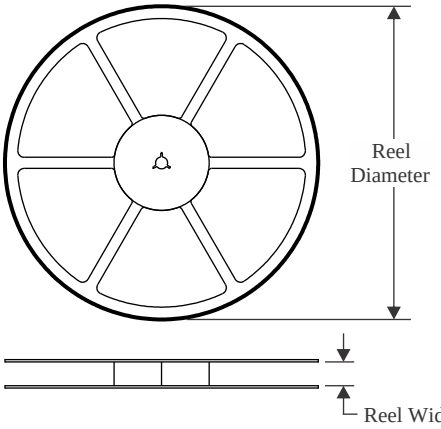
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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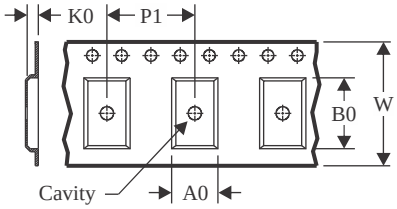
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

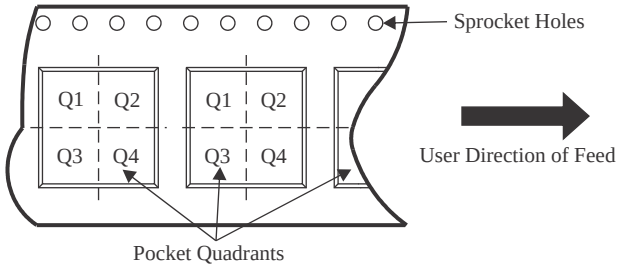


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

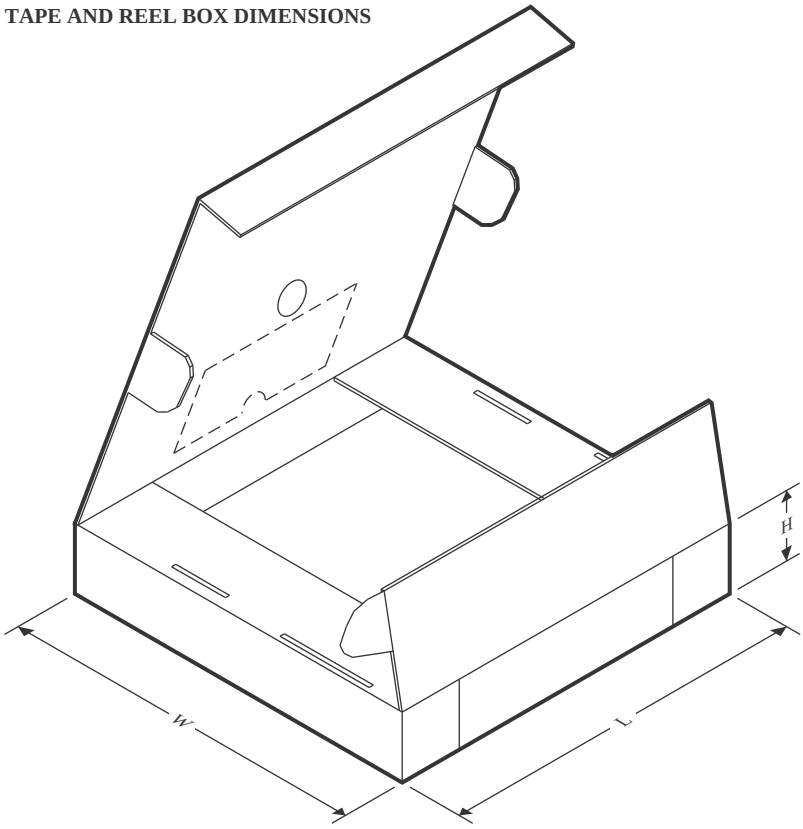
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC29002DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
UCC29002DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC29002DR/1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC29002DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC39002DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
UCC39002DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

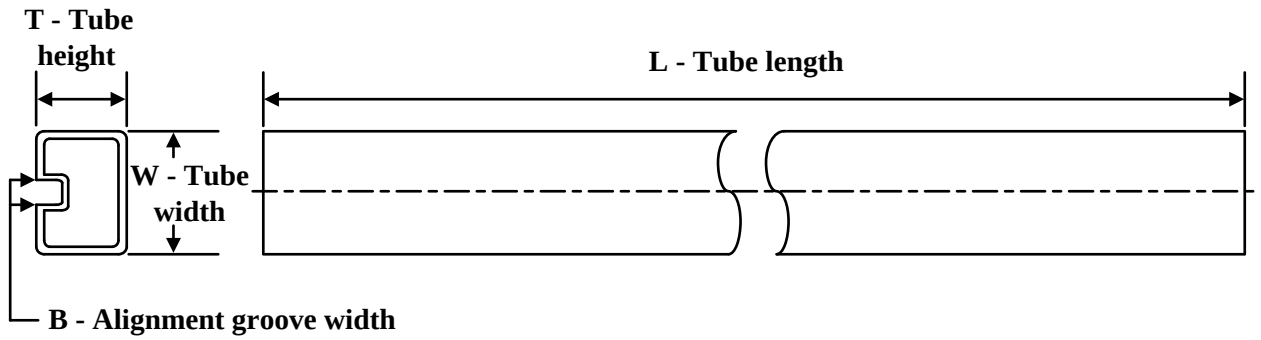
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

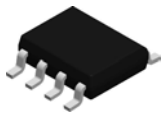
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC29002DGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
UCC29002DR	SOIC	D	8	2500	353.0	353.0	32.0
UCC29002DR/1	SOIC	D	8	2500	353.0	353.0	32.0
UCC29002DRG4	SOIC	D	8	2500	353.0	353.0	32.0
UCC39002DGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
UCC39002DR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UCC29002P	P	PDIP	8	50	506	13.97	11230	4.32
UCC29002P.A	P	PDIP	8	50	506	13.97	11230	4.32
UCC39002P	P	PDIP	8	50	506	13.97	11230	4.32
UCC39002P.A	P	PDIP	8	50	506	13.97	11230	4.32

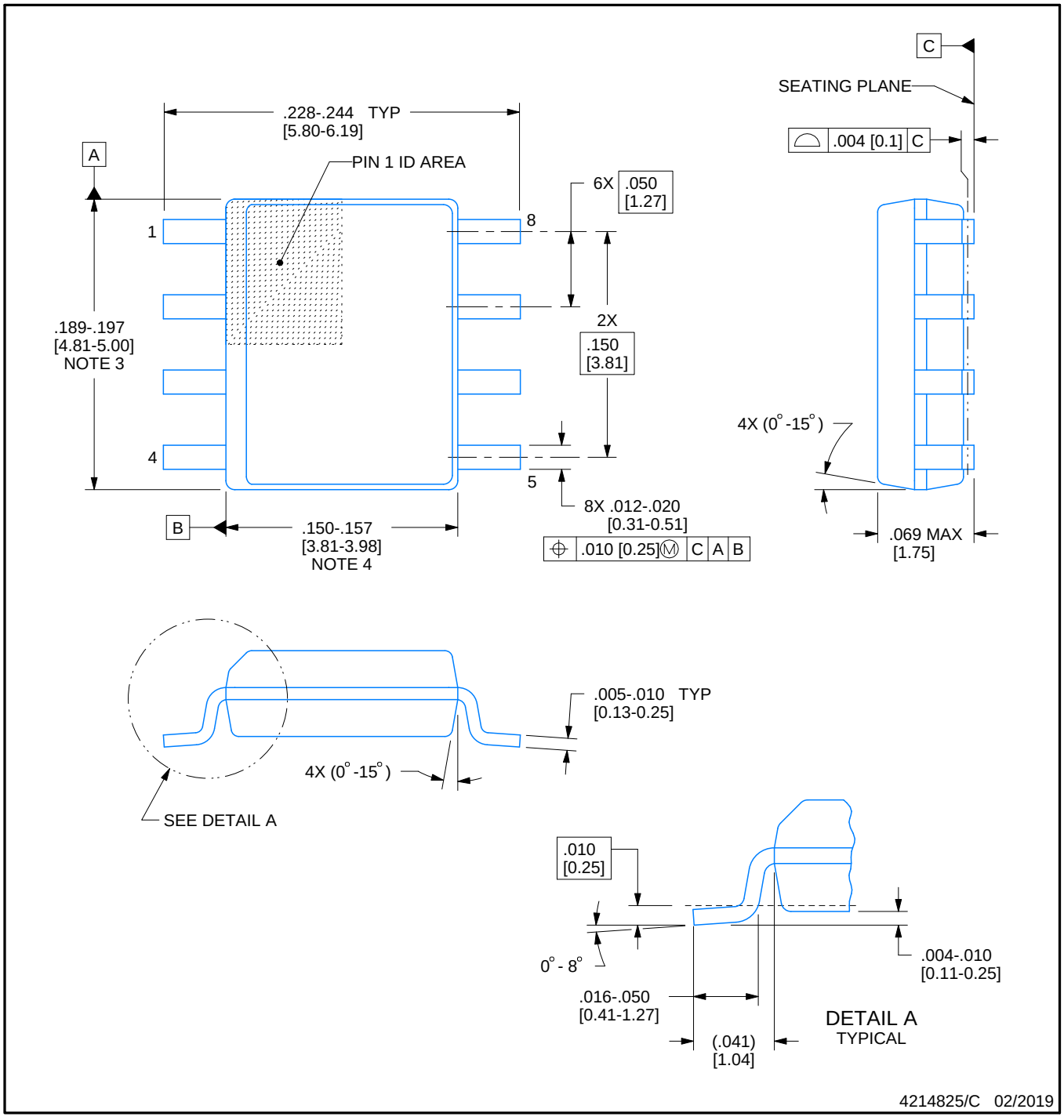


PACKAGE OUTLINE

D0008A

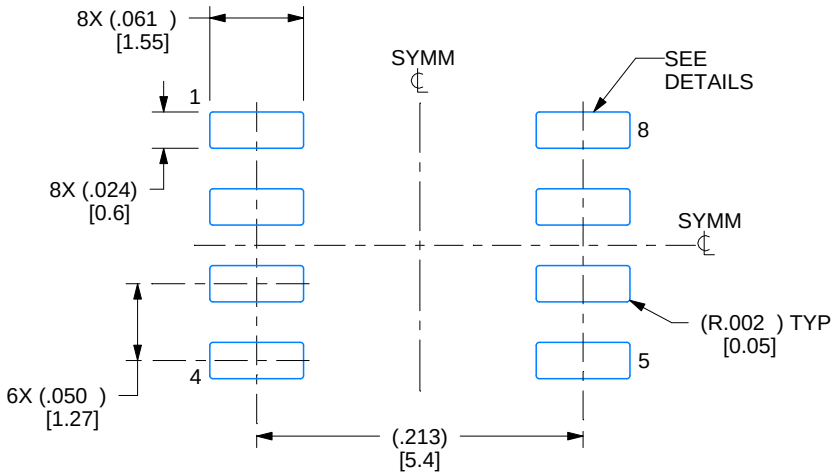
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

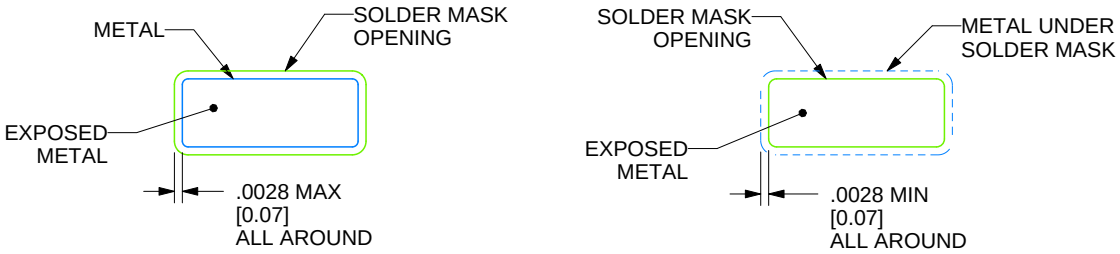


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

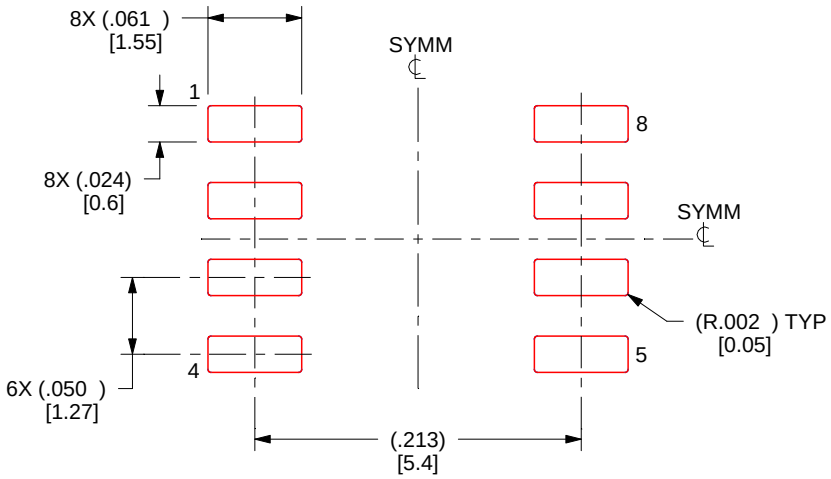
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



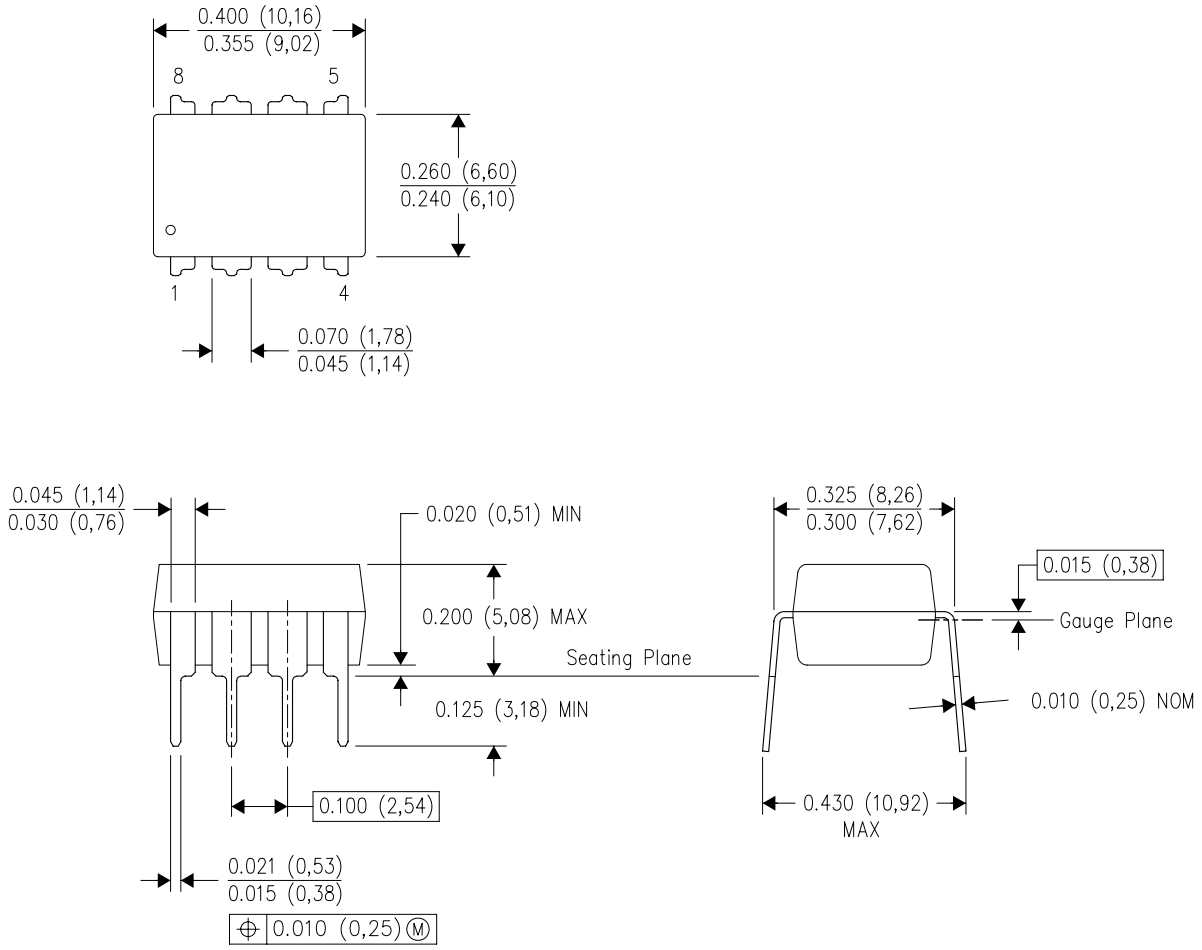
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



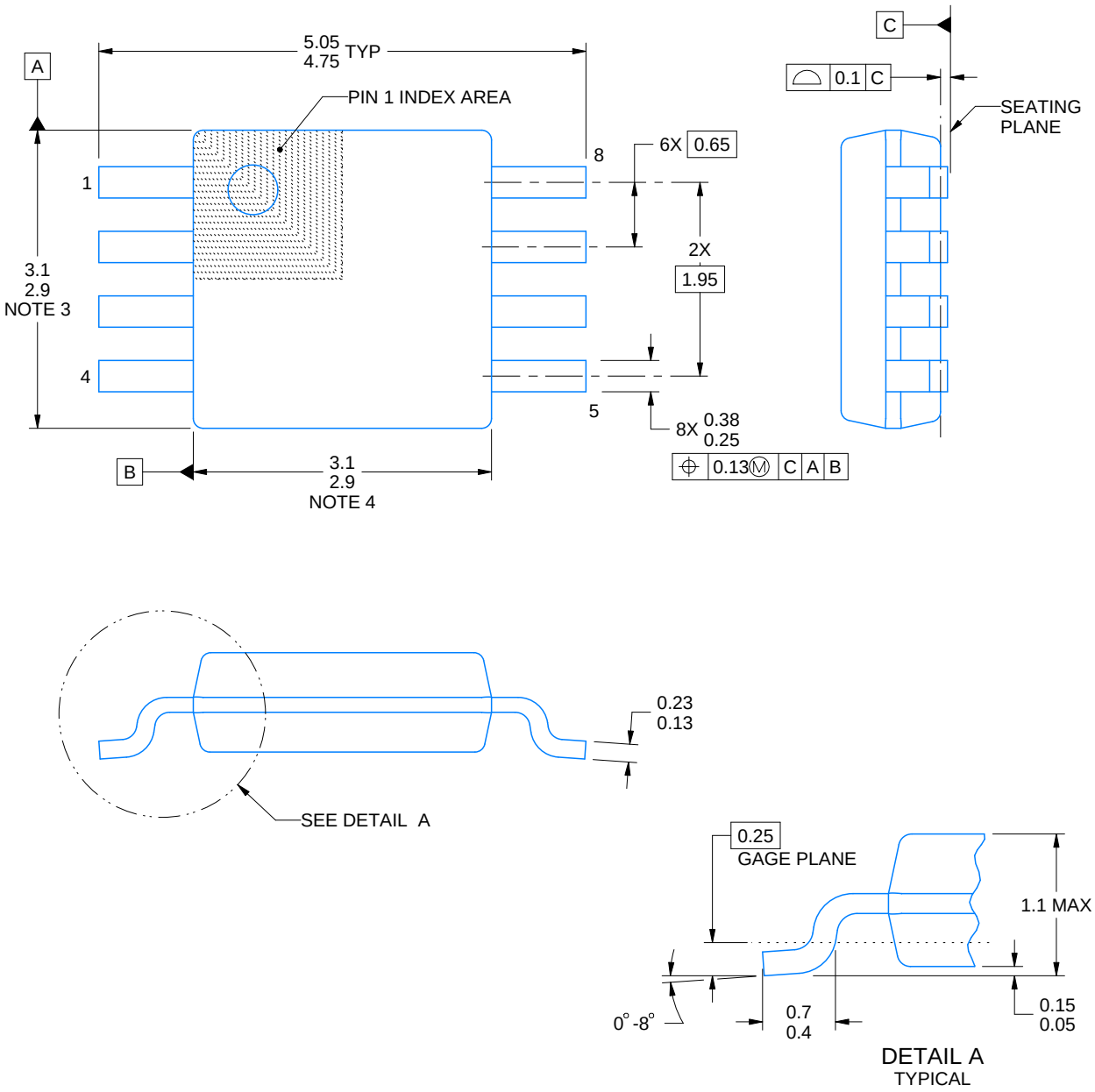
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

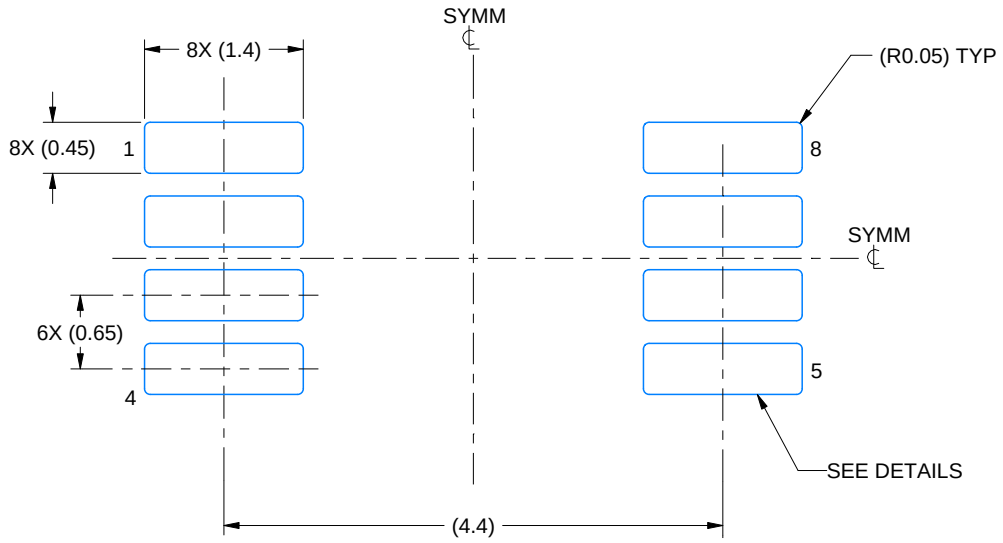
SMALL OUTLINE PACKAGE



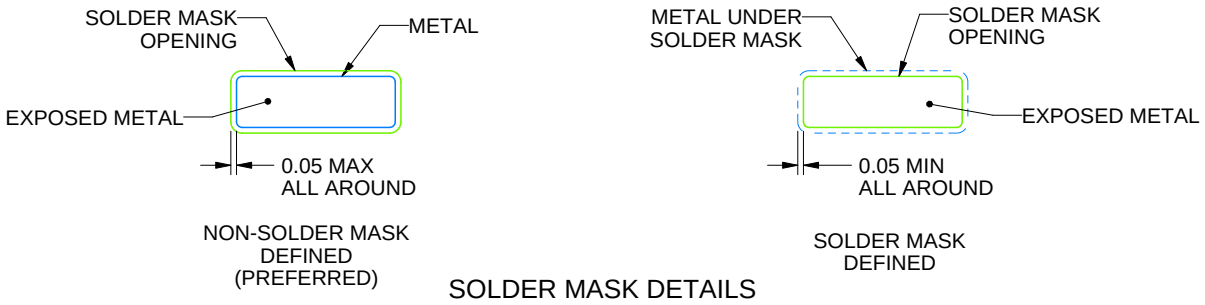
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

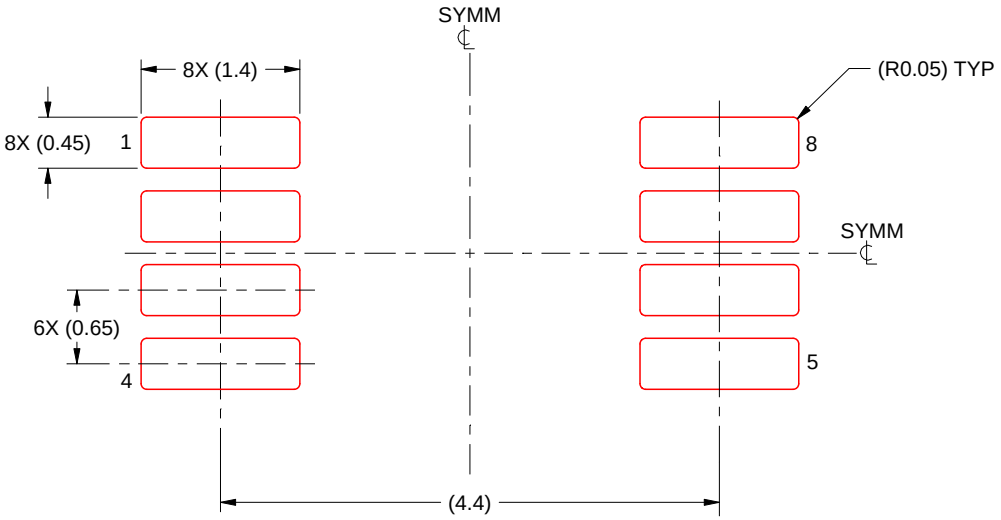


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月