UCD3138 高集積デジタル・コントローラ、絶縁電源向け

1 特長

- 最大 3 つの独立したフィードバック・ループをデジタル制御
  - PID ベースの専用ハードウェア
  - 2 極 / 2 零点の構成が可能
  - 非線形制御
- 最大 16MHz の誤差 A/D コンバータ (EADC)
  - 分解能を 1mV/LSB まで設定可能
  - 分解能自動選択
  - 最大 8 倍のオーバーサンプリング
  - ハードウェア・ベースの平均化 (最大 8 倍)
  - 14 ビット有効の D/A コンバータ (DAC)
  - サンプル・トリガの適応型タイミング決定
- 最大 8 チャネルの 高分解能デジタル PWM (DPWM) 出力
  - パルス幅分解能:250ps
  - 周波数分解能:4ns
  - 位相分解能:4ns
  - 出力間で位相シフトを調整可能
  - ペア間でデッドバンドを調整可能
  - サイクルごとのデューティ・サイクル一致
  - 最大 2MHz のスイッチング周波数
- PWM エッジの移動を設定可能
  - 立ち下がり変調
  - 立ち上がり変調
  - 三角波変調
- フィードバック制御を設定可能
  - 電圧モード
  - 平均電流モード
  - ピーク電流モード制御
  - 定電流
  - 定電力
- 変調方法を設定可能
  - 周波数変調
  - 位相シフト変調
  - パルス幅変調
- 高速で自動的かつ滑らかなモード切り替え
  - 周波数変調と PWM
  - 位相シフト変調と PWM
- 高効率および軽負荷管理
  - バースト・モード
  - 理想ダイオード・エミュレーション
  - 同期整流器のソフト・オン / オフ
  - 低い IC スタンバイ電力
- ソフト・スタート / ストップ、プリバイアスあり / なし
- 高速入力電圧フィード・フォワード・ハードウェア
- 1 次側電圧センシング
- 銅配線パターンの電流センシング
- ピーク電流以外のモード制御アプリケーションでの磁束および位相電流バランス
- 電流シェア・バスをサポート
  - アナログ平均
  - マスタおよびスレーブ
- 多様なフォルト保護オプション
  - 7 個の高速アナログ・コンパレータ
  - サイクル単位の電流制限
  - プログラム可能なフォルト・カウント
  - 外部フォルト入力
  - 10 個のデジタル・コンパレータ
  - プログラム可能なブランキング時間
- 複数の UCD3138 ファミリ・デバイス間の DPWM 波形同期
- 14 チャネル、12 ビット、267kSPS 汎用 ADC、以下の機能を内蔵
  - プログラム可能な平均化フィルタ
  - デュアル・サンプル / ホールド
- 内部温度センサ
- 完全にプログラム可能な、高性能、31.25MHz、32 ビット ARM7TDMI-S™ プロセッサ
  - 32KB プログラム用フラッシュ
  - 2KB のデータ・フラッシュ、ECC 付き
  - 4KB のデータ RAM
  - 4KB のブート ROM、I^2C または UART を介してフィールドでファームウェアのブート・ロードが可能
- 通信ペリフェラル
  - I^2C/PMBus
  - 2 つの UART (UCD3138RGC (64 ピン QFN) の場合)
  - 1 つの UART (UCD3138RHA/UCD3138RMH (40 ピン QFN) および UCD3138RJA (40 ピン VQFN) の場合)
- 入力ピンを選択可能なタイマ・キャプチャ
- 最大 5 つの追加汎用タイマ
- 内蔵ウォッチドッグ:BOD および POR
- 64 ピン QFN および 40 ピン QFN パッケージ
- 動作温度:-40℃～125℃
- Fusion Digital Power Studio GUI をサポート

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2 アプリケーション

- 電源およびテレコム整流器
- 力率補正
- 絶縁型 DC-DC モジュール

3 概要

UCD3138 は、シングルチップ・ソリューションで高度な統合と性能を実現するデジタル電源コントローラです。UCD3138 は柔軟性が高いので、さまざまな電力変換アプリケーションに最適です。さらに、デバイス内部の複数のペリフェラルは、AC-DC および絶縁型 DC-DC アプリケーションの性能を向上し、IT およびネットワーク・インフラ分野でソリューション部品数を削減するために特に最適化されています。

UCD3138 コントローラは、完全にプログラマブルなソリューションであり、アプリケーションの包括的な制御を実現し、ソリューションの差別化を可能にします。これと同時に、アプリケーション・ファームウェア、 Code Composer Studio™ ソフトウェア開発環境、 主要なシステム・パラメータの設定と監視ができる TI の電源開発 GUI など、クラス最高の開発ツールを提供することにより、TI は、お客様の開発作業を簡素化します。

UCD3138 コントローラの中核には、デジタル制御ループ・ペリフェラル、または DPP (デジタル電源ペリフェラル) とも呼ばれるものがあります。各 DPP には、専用の誤差 A/D コンバータ (EADC)、PID ベースの 2 極 / 2 零点デジタル補償器、およびパルス幅分解能 250ps の DPWM 出力で構成される高速デジタル制御ループが実装されています。このデバイスには、12 ビット、267ksps の汎用 ADC が搭載されており、最大 15 チャネル、タイマ、割り込み制御、PMBus 、UART 通信ポートを備えています。このデバイスは、リアルタイムの監視、ペリフェラルの設定、通信の管理を行う、32 ビット ARM7TDMI-S RISC マイクロコントローラをベースにしています。この ARM マイクロコントローラは、プログラム可能なフラッシュ・メモリと、オンチップ RAM および ROM を使ってプログラムを実行します。

FDPP の他に、個別のパワー・マネージメント・ペリフェラルが追加されました。これにより、幅広い制御方式とトポロジをサポートして、全動作範囲にわたる高い効率、高集積による電力密度と信頼性の向上、総システム・コストの最小化、高い柔軟性を実現しています。このペリフェラルとしては、以下に示すものがあります。軽負荷バースト・モード、同期整流、 LLC とフェーズ・シフト・フルブリッジ・モードの切り替え、入力電圧フィード・フォワード、銅配線パターン電流センス、理想ダイオード・エミュレーション、定電流定電力制御、同期整流ソフト・オン / オフ、ピーク電流モード制御、磁束バランス、 2 次側入力電圧センシング、 高分解能の電流シェア、ハードウェアで構成可能なソフト・スタート (プリバイアスあり)、および他のいくつかの機能。トポロジのサポートについては、電圧モードおよびピーク電流モード制御のフェーズ・シフト・フル・ブリッジ、シングルおよびデュアル・フェーズ PFC 、ブリッジレス PFC 、ハード・スイッチ・フル・ブリッジおよびハーフ・ブリッジ、 LLC ハーフ・ブリッジおよびフル・ブリッジに最適化されています。

製品情報

部品番号(1)	パッケージ図	パッケージ・タイプ	本体サイズ
UCD3138	RGC	VQFN (64)	9.00mm × 9.00mm
	RHA	VQFN (40)	6.00mm × 6.00mm
	RMH	WQFN (40)	6.00mm × 6.00mm
	RJA	VQFN (40) (2)	6.00mm × 6.00mm

(1) 詳細については、セクション 14、「*メカニカル、パッケージ、および注文情報*」を参照してください。
(2) 基板レベルの信頼性 (BLR) のための温度サイクルテスト性能向上に最適化されており、新しい 40 ピン設計に推奨。

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4 機能ブロック図

デバイスの機能ブロック図を図 4-1 に示します。

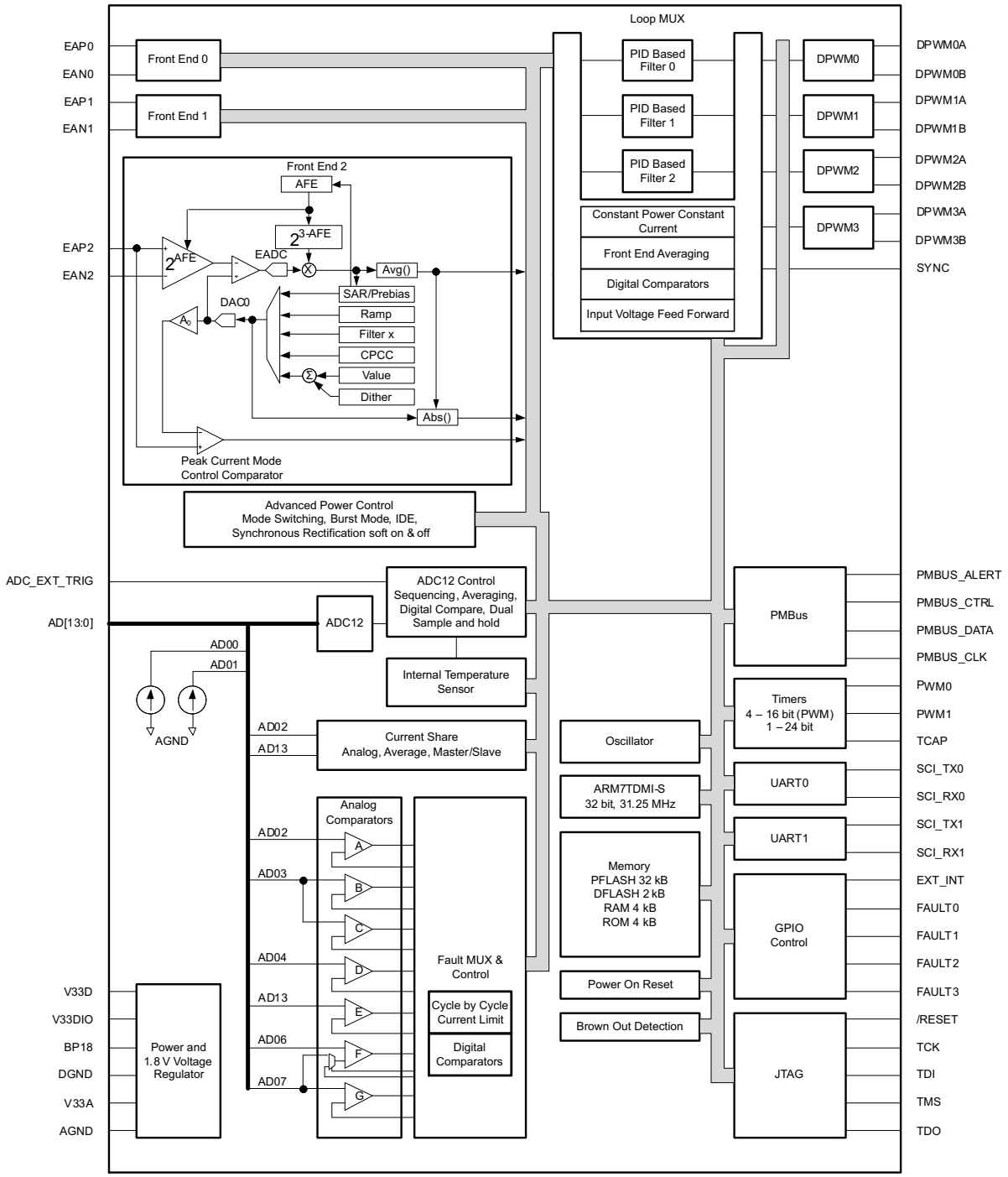

図 4-1. 機能ブロック図

NOTE

ピーク電流モード制御にはフロント・エンド 2 を推奨

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5 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision I (January 2017) to Revision J (November 2021) — **Page**

- 同期機能の説明を変更し、UCD3138064 だけではなく UCD3138 ファミリのすべてのメンバーと連携して動作する旨を記述 TI データシートの標準に合わせて「デバイスの概要」セクションを 4 つのセクションに分割 1
- 14 の外部チャネルと 1 つの内部温度センサがあるため、ADC チャネル数を 15 に変更 2
- update Product Family Comparison to show full UCD family 7
- Added mention of debugging capability to the JTAG pin descriptions and added note that the RMH package is not recommended for new designs 9
- Added DAC Output as an alternative pin out for pins 2, 3, and 4 13
- Correct location of PMBus/SMBus/I^2C rise and fall time test conditions 表 8-1 17
- Added "using the EADCs as a source" to the digital comparator description 39
- Replaced the Power Suppply and Layout Guidelines Section with the Power Supply Recommendations Section and Layout Section. The new content is copied directly from the UCD3138 Family Practical Design Guideline Application Note. 68
- Updated FUSION_DIGITAL_POWER_STUDIO URLs. Moved all CCS references to the Code Composer Studio section and updated them. Also updated the list of documents 82
- Changed References section 83

Changes from Revision H (October 2016) to Revision I (January 2017) — **Page**

- Added updated Layout Guidelines section and added Layout Example images 68

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Changes from Revision G (September 2016) to Revision H (October 2016) **Page**

- 「製品情報」表に パッケージ図面欄を追加 2
- 注 2 を「高度な BLR 性能を備え、新しい 40 ピン設計に推奨」から「基板レベルの信頼性 (BLR) のための温度サイクルテスト性能向上に最適化されており、新しい 40 ピン設計に推奨」に変更。 2
- Deleted 図 7-3 note, "These features help to improve solder-joint reliability". 9

Changes from Revision F (November 2013) to Revision G (September 2016) **Page**

- 「*デバイスおよびドキュメントのサポート*」セクション、「*ESD 定格*」表を追加。 2
- UCD3138A と一致するようにドキュメントのフローを変更。 2
- 「*特長*」および「*製品情報*」表に RJA パッケージを追加 2
- Added RJA package. 9
- Added the RJA package to the *Thermal Information* table 14

Changes from Revision E (August 2013) to Revision F (November 2013) **Page**

- 「注文情報」表で、上面のマーキング情報を「3138」から「3138RMH」に変更 2

Changes from Revision D (August 2013) to Revision E (August 2013) **Page**

- 「特長」の箇条書きに UCD3138RMH を追加 1
- Added RMH package pinout drawing 9
- Added RMH package thermal specifications 14
- Changed Global I/O registers ordered list, item 5 text from "Connecting pin/pins to high rail through internal pull up resistors." to "Configuring pin/pins as open drain or push-pull (Normal)" 45

Changes from Revision C (March 2013) to Revision D (August 2013) **Page**

- Changed T_{OPT} spec to T_J in Abs Max table with MAX temp of 150°C 14
- Added BP18 Voltage vs Temperature graphic 25

Changes from Revision B (July 2012) to Revision C (March 2013) **Page**

- 特長の「JTAG デバッグ・ポート」の箇条書き項目を削除 1
- 「概要」セクションから文字列「JTAG デバッグ」を削除。 2
- 「機能ブロック図」の下に注を追加 3
- Deleted "JTAG" option from Product Selection Matrix 8
- Added text to Pin 54 description 11
- Added text to Pin 35 description 13
- Added BP18 spec to Abs Max Ratings and Recommended Operating Conditions Tables 14
- Deleted V_{DD} specification from System Performance section of *Electrical Characteristics* 15
- Added footnote to 表 8-1 17
- Added text string regarding front-end 2 in the Front End section 20
- Deleted text string reference to "JTAG port" in ARM Processor section 26
- Changed text strings in *Tools and Documentation* 82
- Added document to References list 83

Changes from Revision A (March 2012) to Revision B (July 2012) **Page**

- 「特長」の箇条書き項目を追加 1
- 「特長」セクションの「デュアル・エッジ変調」を「三角波変調」に変更 1
- 「特長」セクションの「265ksps」を「267ksps」に変更 1
- 「特長」セクションの UART の数を明確化 1
- 全体を通して「DPP」を「DDP」に変更。 2
- 全体を通して「DPP」を「DDP」に変更。 2
- Changed Total GPIO pin count for the UCD3138 40-pin device from "17" to "18" in the Product Selection Matrix table 8
- Changed "VREG" to "BP18" in conditions statement for *Electrical Characteristics* 15

- Changed EAP – EAN Error voltage digital resolution MIN values for AFE = 3, AFE = 2, AFE = 1, AFE = 0 from 0.95, 1.90, 3.72, and 7.3 respectively; to, 0.8, 1.7, 3.55, and 6.90 respectively.....15
- Changed conditions for V_{OL} and V_{OH} specifications in *Electrical Characteristics* 15
- Added TWD specification to *Electrical Characteristics* 15
- Changed "PWM" to "DPWM" in *DPWM Module* 21
- Changed waveforms graphic for "Phase Shifted Full Bridge Example" for clarification 30
- Added text to section*LLC Example* 32
- Changed typical conversion speed from "268 ksps" to "267 ksps" in the General Purpose ADC12 section....43
- Added package ID information for the UCD3138RGC and UCD3138RHA devices.....45
- Added bullet "AD02 has a special ESD protection mechanism that prevents the pin from pulling down the current-share bus if power is missing from the UCD3138" to *Current Sharing Control*.....47
- Changed "PWMA" and "PWMB" to "DPWMA" and "DPWMB" in Normal Mode. 49
- Changed " Mechanical Data" section to "References" section.....83

Changes from Revision * (March 2012) to Revision A (March 2012)	**Page**
• 「製品プレビュー」のバナーを削除、脚注に量産データの記述を追加	1

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6 Device Comparison Table

6.1 Product Family Comparison

	UCD					
FEATURE	**3138 3138A RHA/RMH**	**3138064 3138064A RMH**	**3138 3138A RGC**	**3138064 3138064A RGC**	**3138128 3138128A PFC**	**3138A64 PFC**
Package Offering	40 Pin QFN (6mm x 6mm)	40 Pin QFN (6mm x 6mm)	64 Pin QFN (9mm x 9mm)	64 Pin QFN (9mm x 9mm)	80 Pin QFP (14mm x 14mm) (Includes leads)	80 Pin QFP (14mm x 14mm) (Includes leads)
ARM7TDMI-S Core Processor	31.25 MHz	31.25 MHz	31.25 MHz	31.25 MHz	31.25 MHz	31.25 MHz
High Resolution DPWM Outputs (250ps Resolution)	8	8	8	8	8	8
Number of High Speed Independent Feedback Loops (# Regulated Output Voltages	3	3	3	3	3	3
12-bit, 256kps, General Purpose ADC Channels	7	7	14	14	15	15
Digital Comparators at ADC Outputs	4	4	4	4	4	4
Flash Memory (Program)	32 kB	64 kB	32 kB	64 kB	128 kB	64 kB
Number of Memory 32kB Flash Memory Banks	1	2	1	2	4	Only 1 bank of 64 kB Flash available
Flash Memory (Data)	2 kB	2 kB	2 kB	2 kB	2 kB	2 kB
RAM	4 kB	4 kB	4 kB	4 kB	8 kB	8 kB
Programmable Fault Inputs	1 + 2[(1)]	1 + 2[(1)]	4	2 + 2[(1)]	4	4
High Speed Analog Comparators with Cycle-by-Cycle Current Limiting	6	6	7	7	7	7
UART (SCI)	1[(1)]	1[(1)]	2	2	2	2
PMBus/I^2C	1	1	1	1	1	1
Additional I^2C	0	0	0	1[(1)]	1	1
SPI	0	0	0	1[(1)]	1	1
Timers	4 (16 bit) and 1 (24 bit)	4 (16 bit) and 1 (24 bit)	4 (16 bit) and 1 (24 bit)	4 (16 bit) and 1 (24 bit)	4 (16 bit) and 2 (24 bit)	4 (16 bit) and 2 (24 bit)
Timer PWM Outputs	1[(1)]	1[(1)]	2	2	4	4
Timer Capture Inputs	2[(1)]	2[(1)]	1 + 3[(1)]	1 + 3[(1)]	2 + 2[(1)]	2 + 2[(1)]
Total Digital GPIOs	18	18	30	30	43	43
External Interrupts	0	0	1	1	1	1
External Crystal Clock Support	no	no	no	no	Yes (pins #61, 62)	Yes (pins #61, 62)
Peak Current Mode Control	EADC2 Only	All EADC channels	EADC Only	All EADC channels	All EADC Channels	All EADC Channels

(1) Represents an alternate pinout configuration that is programmable via firmware.

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6.2 Product Selection Matrix

FEATURE	UCD3138 64 PIN (RGC)	UCD3138 40 PIN (RHA/RMH/RJA)
ARM7TDMI-S core processor	31.25 MHz	31.25 MHz
High resolution dPWM outputs (250-ps resolution)	8	8
Number of high speed independent feedback loops (number of regulated output voltages)	3	3
12-bit, 267ksps, general-purpose ADC channels	14	7
Digital comparators at ADC outputs	4	4
Flash memory (program)	32 KB	32 KB
Flash memory (data)	2 KB	2 KB
Flash security	√	√
RAM	4 KB	4 KB
DPWM switching frequency	up to 2 MHz	up to 2 MHz
Programmable fault inputs	4	1 + 2(1)
High speed analog comparators with cycle-by-cycle current limiting	7(2)	6(2)
UART (SCI)	2	1(1)
PMBus	√	√
Timers	4 (16 bit) and 1 (24 bit)	4 (16 bit) and 1 (24 bit)
Timer PWM outputs	2	1
Timer capture inputs	1	1(1)
Watchdog	√	√
On chip oscillator	√	√
Power-on reset and brown-out reset	√	√
Package offering	64 Pin QFN (9 mm × 9 mm)	40 Pin QFN (6 mm × 6 mm)
Sync IN and sync OUT functions	√	√
Total GPIO (includes all pins with multiplexed functions such as, DPWM, fault inputs, SCI, and so forth)	30	18
External interrupts	1	0

(1) This number represents an alternate pin out that is programmable via firmware. See the UCD3138 Digital Power Peripherals Programmer's Manual for details.
(2) To facilitate simple OVP and UVP connections both comparators B and C are connected to the AD03 pin.

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7 Pin Configuration and Functions

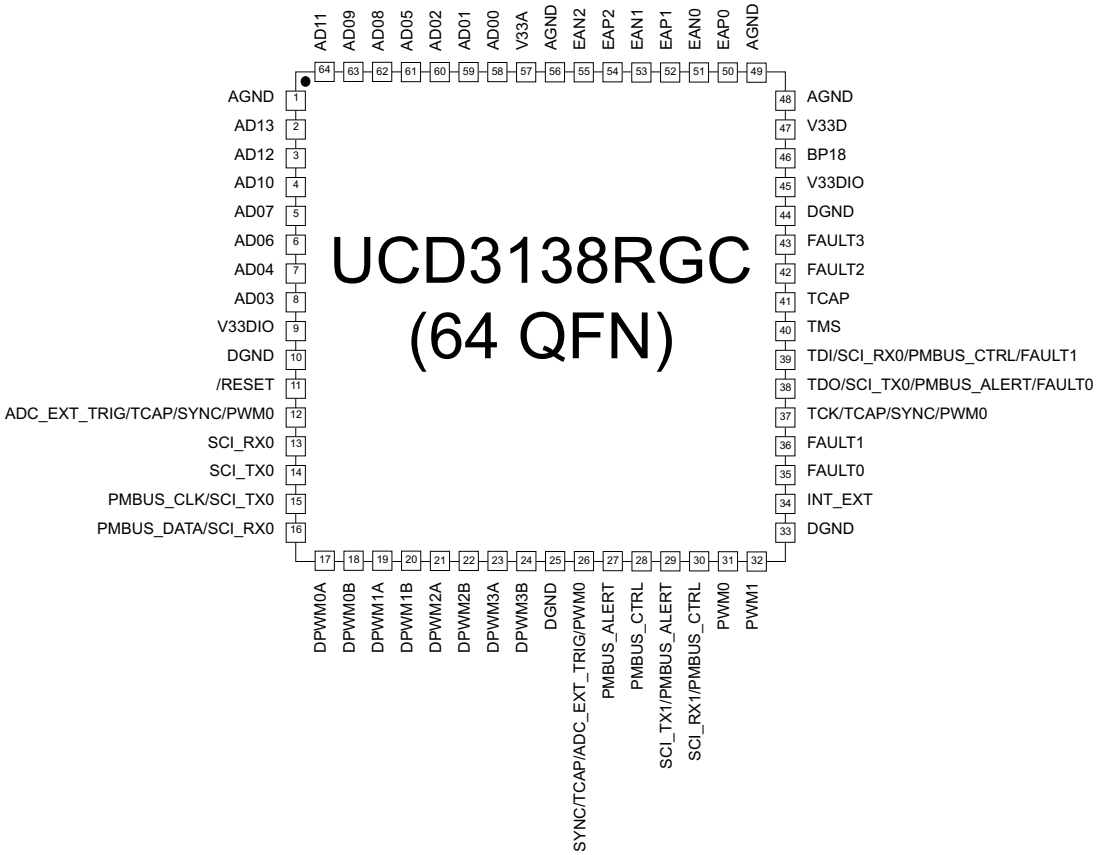


図 7-1. UCD3138RGC 64 QFN Pin Attributes

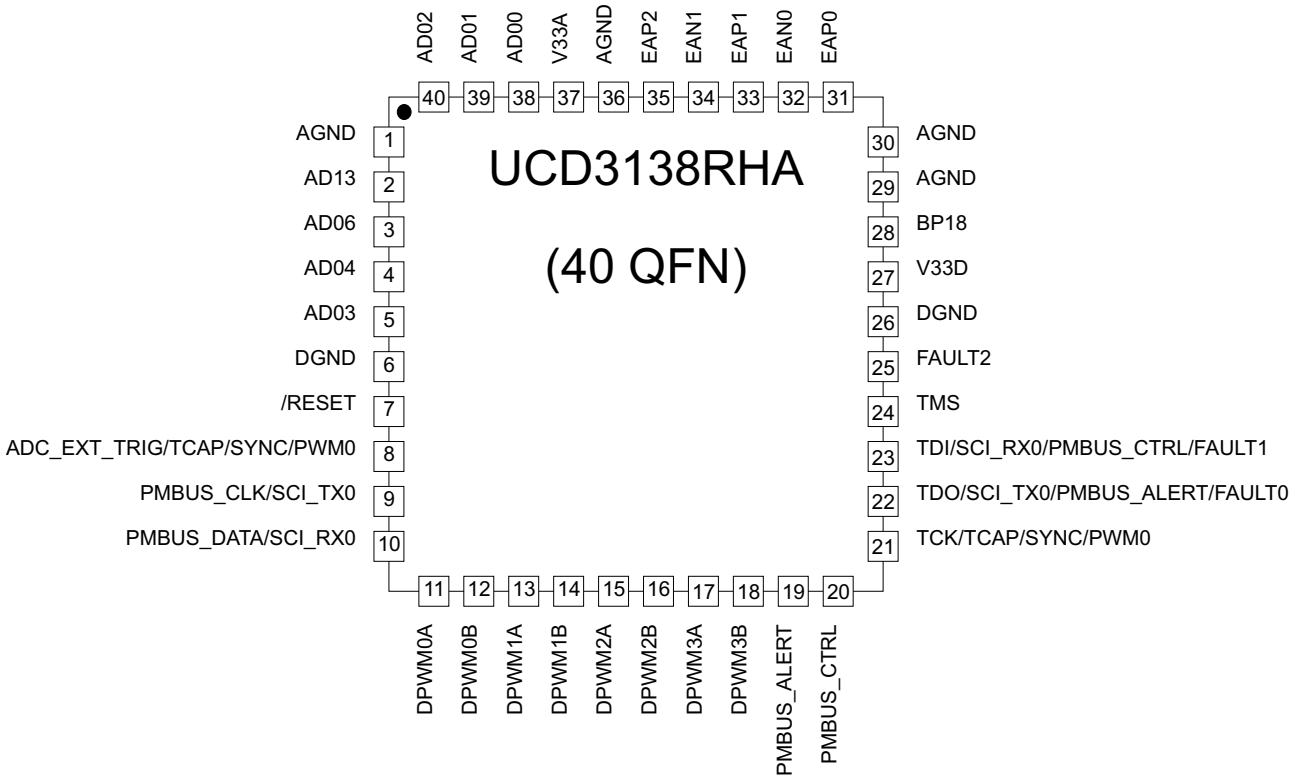
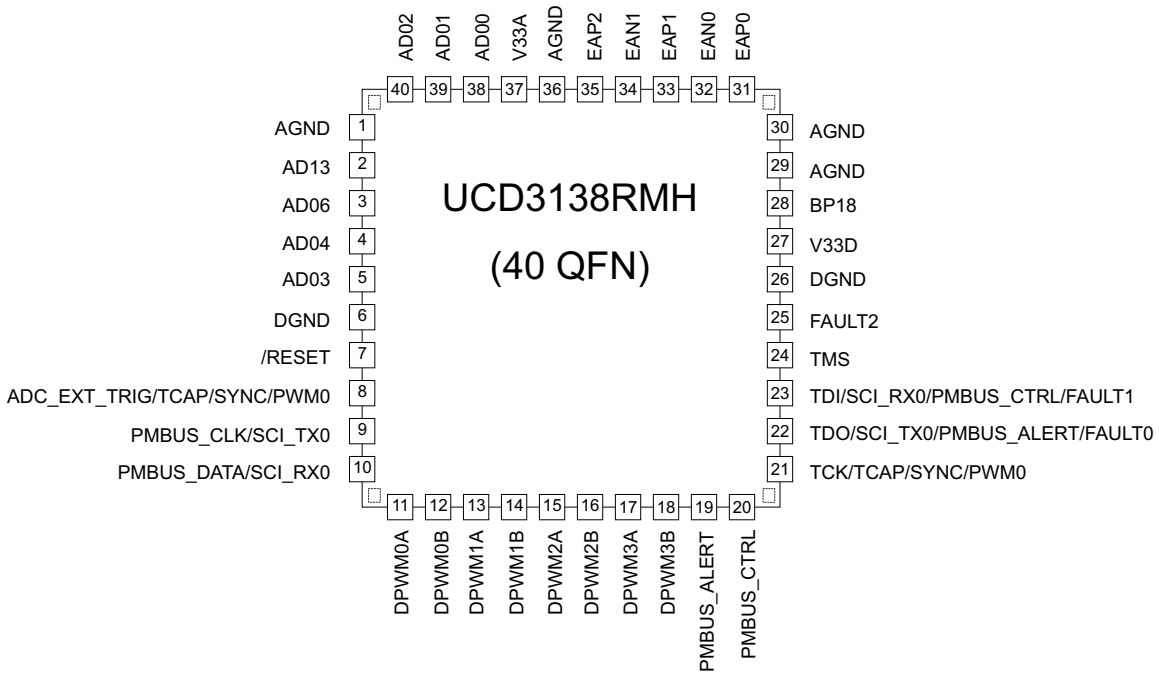


図 7-2. UCD3138RHA 40 QFN Pin Attributes



NOTE: The RMH package is not recommended for new designs. It has thinner package height compared to the RHA package. There are also four corner pins on the RMH package. The corner anchor pins and thermal pad should be soldered for robust mechanical performance and should be tied to the appropriate ground signal.

図 7-3. UCD3138RMH 40 QFN With Corner Anchors Pin Attributes

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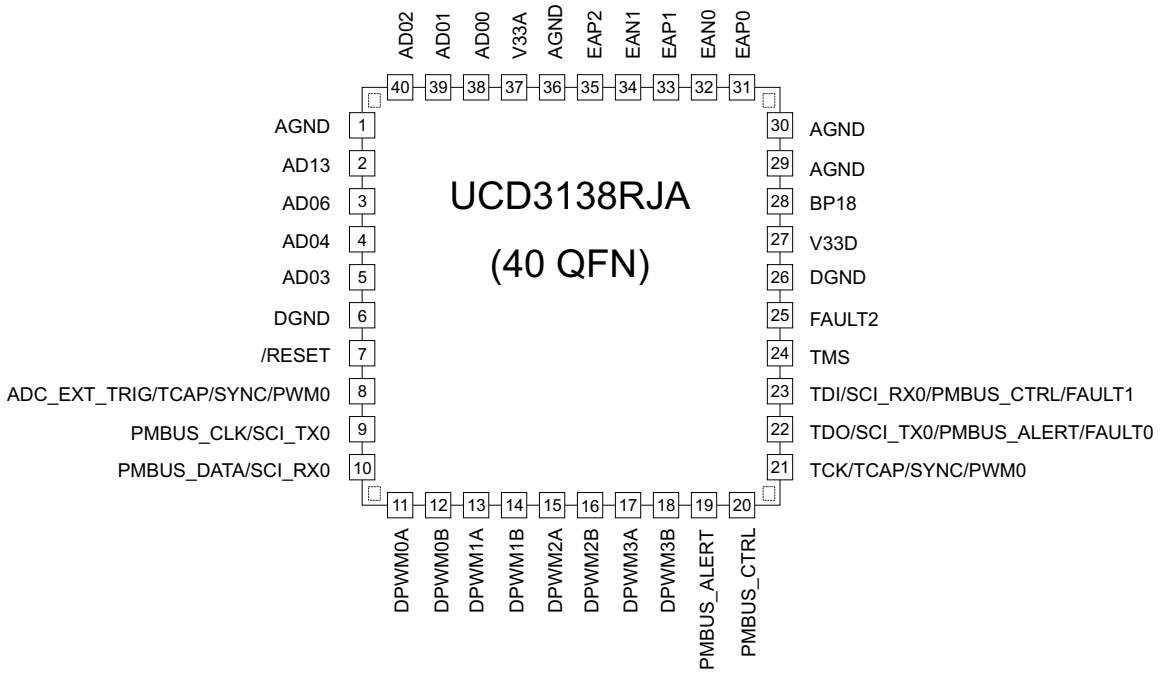

NOTE: The RJA package has thicker package height compared to the RMH package. There are also four corner pins on the RJA package. These features help to improve solder-joint reliability. The corner anchor pins and thermal pad should be soldered for robust mechanical performance and should be tied to the appropriate ground signal.

図 7-4. UCD3138RJA 40 QFN With Corner Anchors Pin Attributes

7.1 UCD3138RGC 64 QFN Pin Attributes

表 7-1. UCD3138RGC 64 QFN Pin Attributes

PIN NO.	NAME	PRIMARY ASSIGNMENT	ALTERNATE ASSIGNMENT			CONFIGURABLE AS A GPIO?
			NO. 1	NO. 2	NO. 3	
1	AGND	Analog ground				
2	AD13	12-bit ADC, Ch 13, comparator E, I-share	DAC output			
3	AD12	12-bit ADC, Ch 12				
4	AD10	12-bit ADC, Ch 10				
5	AD07	12-bit ADC, Ch 7, Connected to comparator F and reference to comparator G	DAC output			
6	AD06	12-bit ADC, Ch 6, Connected to comparator F	DAC output			
7	AD04	12-bit ADC, Ch 4, Connected to comparator D	DAC output			
8	AD03	12-bit ADC, Ch 3, Connected to comparator B and C				
9	V33DIO	Digital I/O 3.3V core supply				
10	DGND	Digital ground				
11	$\overline{\text{RESET}}$	Device Reset Input, active low				
12	ADC_EXT_TRIG	ADC conversion external trigger input	TCAP	SYNC	PWM0	Yes
13	SCI_RX0	SCI RX 0				Yes
14	SCI_TX0	SCI TX 0				Yes
15	PMBUS_CLK	PMBUS Clock (Open Drain)	SCI TX 0			Yes
16	PMBUS_DATA	PMBus data (Open Drain)	SCI RX 0			Yes
17	DPWM0A	DPWM 0A output				Yes
18	DPWM0B	DPWM 0B output				Yes
19	DPWM1A	DPWM 1A output				Yes
20	DPWM1B	DPWM 1B output				Yes
21	DPWM2A	DPWM 2A output				Yes

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表 7-1. UCD3138RGC 64 QFN Pin Attributes (continued)

PIN NO.	NAME	PRIMARY ASSIGNMENT	ALTERNATE ASSIGNMENT			CONFIGURABLE AS A GPIO?
			NO. 1	NO. 2	NO. 3	
22	DPWM2B	DPWM 2B output				Yes
23	DPWM3A	DPWM 3A output				Yes
24	DPWM3B	DPWM 3B output				Yes
25	DGND	Digital ground				
26	SYNC	DPWM Synchronize pin	TCAP	ADC_EXT_TRIG	PWM0	Yes
27	PMBUS_ALERT	PMBus Alert (Open Drain)				Yes
28	PMBUS_CTRL	PMBus Control (Open Drain)				Yes
29	SCI_TX1	SCI TX 1	PMBUS_ALERT			Yes
30	SCI_RX1	SCI RX 1	PMBUS_CTRL			Yes
31	PWM0	General purpose PWM 0				Yes
32	PWM1	General purpose PWM 1				Yes
33	DGND	Digital ground				
34	INT_EXT	External Interrupt				Yes
35	FAULT0	External fault input 0				Yes
36	FAULT1	External fault input 1				Yes
37	TCK	JTAG TCK (For debugging or manufacturer test only)	TCAP	SYNC	PWM0	Yes
38	TDO	JTAG TDO (For debugging or manufacturer test only)	SCI_TX0	PMBUS_ALERT	FAULT0	Yes
39	TDI	JTAG TDI (For debugging or manufacturer test only)	SCI_RX0	PMBUS_CTRL	FAULT1	Yes
40	TMS	JTAG TMS (For debugging or manufacturer test only)				Yes
41	TCAP	Timer capture input				Yes
42	FAULT2	External fault input 2				Yes
43	FAULT3	External fault input 3				Yes
44	DGND	Digital ground				
45	V33DIO	Digital I/O 3.3V core supply				
46	BP18	1.8V Bypass				
47	V33D	Digital 3.3V core supply				
48	AGND	Substrate analog ground				
49	AGND	Analog ground				
50	EAP0	Channel 0, differential analog voltage, positive input				
51	EAN0	Channel 0, differential analog voltage, negative input				
52	EAP1	Channel 1, differential analog voltage, positive input				
53	EAN1	Channel 1, differential analog voltage, negative input				
54	EAP2	Channel 2, differential analog voltage, positive input (Recommended for peak currrent mode control)				
55	EAN2	Channel #2, differential analog voltage, negative input				
56	AGND	Analog ground				
57	V33A	Analog 3.3-V supply				
58	AD00	12-bit ADC, Ch 0, Connected to current source				
59	AD01	12-bit ADC, Ch 1, Connected to current source				
60	AD02	12-bit ADC, Ch 2, Connected to comparator A, I-share				
61	AD05	12-bit ADC, Ch 5				
62	AD08	12-bit ADC, Ch 8				
63	AD09	12-bit ADC, Ch 9				
64	AD11	12-bit ADC, Ch 11				

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7.2 UCD3138RHA, UCD3138RMH and UCD3138RJA Pin Attributes

表 7-2. UCD3138RHA, UCD3138RMH and UCD3138RJA Pin Attributes

PIN NO.	NAME	PRIMARY ASSIGNMENT	ALTERNATE ASSIGNMENT			CONFIGURABLE AS A GPIO?
			NO. 1	NO. 2	NO. 3	
1	AGND	Analog ground				
2	AD13	12-bit ADC, Ch 13, Connected to comparator E, I-share	DAC output			
3	AD06	12-bit ADC, Ch 6, Connected to comparator F	DAC output			
4	AD04	12-bit ADC, Ch 4, Connected to comparator D	DAC output			
5	AD03	12-bit ADC, Ch 3, Connected to comparator B and C				
6	DGND	Digital ground				
7	$\overline{\text{RESET}}$	Device Reset Input, active low				
8	ADC_EXT_TRIG	ADC conversion external trigger input	TCAP	SYNC	PWM0	Yes
9	PMBUS_CLK	PMBUS Clock (Open Drain)	SCI_TX0			Yes
10	PMBUS_DATA	PMBus data (Open Drain)	SCI_RX0			Yes
11	DPWM0A	DPWM 0A output				Yes
12	DPWM0B	DPWM 0B output				Yes
13	DPWM1A	DPWM 1A output				Yes
14	DPWM1B	DPWM 1B output				Yes
15	DPWM2A	DPWM 2A output				Yes
16	DPWM2B	DPWM 2B output				Yes
17	DWPM3A	DPWM 3A output				Yes
18	DPWM3B	DPWM 3B output				Yes
19	PMBUS_ALERT	PMBus Alert (Open Drain)				Yes
20	PMBUS_CTRL	PMBus Control (Open Drain)				Yes
21	TCK	JTAG TCK (For debugging or manufacturer test only)	TCAP	SYNC	PWM0	Yes
22	TDO	JTAG TDO (For debugging or manufacturer test only)	SCI_TX0	PMBUS_ALERT	FAULT0	Yes
23	TDI	JTAG TDI (For debugging or manufacturer test only)	SCI_RX0	PMBUS_CTRL	FAULT1	Yes
24	TMS	JTAG TMS (For debugging or manufacturer test only)				Yes
25	FAULT2	External fault input 2				Yes
26	DGND	Digital ground				
27	V33D	Digital 3.3V core supply				
28	BP18	1.8V Bypass				
29	AGND	Substrate analog ground				
30	AGND	Analog ground				
31	EAP0	Channel 0, differential analog voltage, positive input				
32	EAN0	Channel 0, differential analog voltage, negative input				
33	EAP1	Channel 1, differential analog voltage, positive input				
34	EAN1	Channel 1, differential analog voltage, negative input				
35	EAP2	Channel 2, differential analog voltage, positive input (Recommended for peak currrent mode control)				
36	AGND	Analog ground				
37	V33A	Analog 3.3-V supply				
38	AD00	12-bit ADC, Ch 0, Connected to current source				
39	AD01	12-bit ADC, Ch 1, Connected to current source				
40	AD02	12-bit ADC, Ch 2, Connected to comparator A, I-share				
Corner NA	Corner anchor pin (RMH and RJA only)	All four anchors should be soldered and tied to GND				

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V33D	V33D to DGND	–0.3	3.8	V
V33DIO	V33DIO to DGND	–0.3	3.8	V
V33A	V33A to AGND	–0.3	3.8	V
BP18	BP18 to DGND	–0.3	2.5	V
|DGND – AGND|	Ground difference		0.3	V
All pins, excluding AGND[2]	Voltage applied to any pin	–0.3	3.8	V
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Referenced to DGND

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V33D	Digital power	3.0	3.3	3.6	V
V33DIO	Digital I/O power	3.0	3.3	3.6	
V33A	Analog power	3.0	3.3	3.6	V
T_J	Junction temperature	–40		125	°C
BP18	1.8-V digital power	1.6	1.8	2.0	V

8.4 Thermal Information

THERMAL METRIC[1]		UCD3138 64 PIN QFN (RGC)	UCD3138 40 PIN QFN (RHA)	UCD3138 40 PIN QFN (RMH)	UCD3138 40 PIN QFN (RJA)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	25.1	31.8	31.0	30.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	10.5	18.5	16.5	13.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	4.6	6.8	6.3	4.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	0.2	0.2	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	4.6	6.7	6.3	4.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.2	1.8	1.1	0.7	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics* application report.

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8.5 Electrical Characteristics

V33A = V33D = V33DIO = 3.3 V; 1 µF from BP18 to DGND, T_J = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
	I33A	Measured on V33A. The device is powered up but all ADC12 and EADC sampling is disabled		6.3		mA
	I33DIO	All GPIO and communication pins are open		0.35		mA
	I33D	ROM program execution		60		mA
	I33D	Flash programming in ROM mode			70	mA
	I33	The device is in ROM mode with all DPWMs enabled and switching at 2 MHz. The DPWMs are all unloaded.			100	mA
ERROR ADC INPUTS EAP, EAN						
	EAP – AGND		–0.15		1.998	V
	EAP – EAN		–0.256		1.848	V
	Typical error range	AFE = 0	–256		248	mV
	EAP – EAN Error voltage digital resolution	AFE = 3	0.8	1	1.20	mV
		AFE = 2	1.7	2	2.30	mV
		AFE = 1	3.55	4	4.45	mV
		AFE = 0	6.90	8	9.10	mV
R_{EA}	Input impedance (See 図 8-4)	AGND reference	0.5			MΩ
I_{OFFSET}	Input offset current (See 図 8-4)		–5		5	µA
	EADC offset	Input voltage = 0 V at AFE = 0	–2		2	LSB
		Input voltage = 0 V at AFE = 1	–2.5		2.5	LSB
		Input voltage = 0 V at AFE = 2	–3		-3	LSB
		Input voltage = 0 V at AFE = 3	–4		4	LSB
	Sample Rate				16	MHz
	Analog Front End Amplifier Bandwidth			100		MHz
A_0	Gain	See 図 8-5		1		V/V
	Minimum output voltage				100	mV
EADC DAC						
	DAC range		0		1.6	V
	VREF DAC reference resolution	10 bit, No dithering enabled		1.56		mV
	VREF DAC reference resolution	With 4 bit dithering enabled		97.6		µV
	INL		–3.0		3.0	LSB
	DNL	Does not include MSB transition	–2.1		1.6	LSB
	DNL at MSB transition			–1.4		LSB
	DAC reference voltage		1.58		1.61	V
τ	Settling Time	From 10% to 90%		250		ns
ADC12						
I_{BIAS}	Bias current for PMBus address pins		9.5		10.5	µA
	Measurement range for voltage monitoring		0		2.5	V
	Internal ADC reference voltage	–40°C to 125°C	2.475	2.500	2.525	V
	Change in Internal ADC reference from 25°C reference voltage(1)	–40°C to 25°C		–0.4		mV
		25°C to 85°C		–1.8		
		25°C to 125°C		–4.2		

8.5 Electrical Characteristics (continued)

V33A = V33D = V33DIO = 3.3 V; 1 µF from BP18 to DGND, T_J = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
	ADC12 INL integral nonlinearity[1]	ADC_SAMPLINGSEL = 6 for all ADC12 data, 25 °C to 125 °C		±2.5		LSB
	ADC12 DNL differential nonlinearity[1]			–0.7/+2.5		LSB
	ADC Zero Scale Error		–7		7	mV
	ADC Full Scale Error		–35		35	mV
	Input bias	2.5 V applied to pin			400	nA
	Input leakage resistance[1]	ADC_SAMPLINGSEL= 6 or 0		1		MΩ
	Input Capacitance[1]			10		pF
	ADC single sample conversion time[1]	ADC_SAMPLINGSEL= 6 or 0		3.9		µs
DIGITAL INPUTS/OUTPUTS[2] [3]						
V_{OL}	Low-level output voltage[4]	I_{OH} = 4 mA, V33DIO = 3 V			DGND + 0.25	V
V_{OH}	High-level output voltage [4]	I_{OH} = –4 mA, V33DIO = 3 V	V33DIO – 0.6			V
V_{IH}	High-level input voltage	V33DIO = 3 V	2.1			V
V_{IL}	Low-level input voltage	V33DIO = 3 V			1.1	V
I_{OH}	Output sinking current				4	mA
I_{OL}	Output sourcing current		–4			mA
SYSTEM PERFORMANCE						
TWD	Watchdog time out range	Total time is: TWD × (WDCTRL.PERIOD + 1)	14.6	17	20.5	ms
	Time to disable DPWM output based on active FAULT pin signal	High level on FAULT pin		70		ns
	Processor master clock (MCLK)			31.25		MHz
t_{Delay}	Digital compensator delay[5]	(1 clock = 32 ns)			6	clocks
$t_{(reset)}$	Pulse width needed at reset[1]		10			µs
	Retention period of flash content (data retention and program)	T_J = 25°C	100			years
	Program time to erase one page or block in data flash or program flash			20		ms
	Program time to write one word in data flash or program flash			20		µs
$f_{(PCLK)}$	Internal oscillator frequency		240	250	260	MHz
	Sync-in/sync-out pulse width	Sync pin		256		ns
	Flash Read			1		MCLKs
	Flash Write			20		µs
I_{SHARE}	Current share current source (See 図 9-16)		238		259	µA
R_{SHARE}	Current share resistor (See 図 9-16)		9.75		10.3	kΩ
POWER ON RESET AND BROWN OUT (V33D pin, See 図 8-3)						
VGH		Voltage good high		2.7		V
VGL		Voltage good low		2.5		V
V_{res}		Voltage at which IReset signal is valid		0.8		V
T_{POR}		Time delay after power is good or RESET* relinquished		1		ms
	Brownout	Internal signal warning of brownout conditions		2.9		V
TEMPERATURE SENSOR[6]						
V_{TEMP}		Voltage range of sensor	1.46		2.44	V

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8.5 Electrical Characteristics (continued)

V33A = V33D = V33DIO = 3.3 V; 1 µF from BP18 to DGND, T_J = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
	Voltage resolution	V/°C		5.9		mV/°C
	Temperature resolution	°C per bit		0.1034		°C/LSB
	Accuracy(6) (7)	–40°C to 125°C	–10	±5	10	°C
	Temperature range	–40°C to 125°C	–40		125	°C
I_{TEMP}		Current draw of sensor when active		30		µA
T_{ON}		Turn on time / settling time of sensor		100		µs
V_{AMB}	Ambient temperature	Trimmed 25°C reading		1.85		V
ANALOG COMPARATOR						
DAC	Reference DAC Range		0		2.5	V
	Reference Voltage		2.478	2.5	2.513	V
	Bits			7		bits
	INL(6)		–0.42		0.21	LSB
	DNL(6)		0.06		0.12	LSB
	Offset		–5.5		19.5	mV
	Time to disable DPWM output based on 0 V to 2.5 V step input on the analog comparator.(1)				150	ns
	Reference DAC buffered output load(8)		0.5		1	mA
	Buffer offset (–0.5 mA)		4.6		8.3	mV
	Buffer offset (1.0 mA)		–0.05		17	mV

(1) As designed and characterized. Not 100% tested in production.
(2) DPWM outputs are low after reset. Other GPIO pins are configured as inputs after reset.
(3) On the 40-pin package V33DIO is connected to V33D internally.
(4) The maximum total current, IOHmax and IOLmax for all outputs combined, should not exceed 12 mA to hold the maximum voltage drop specified. Maximum sink current per pin = –6 mA at V_{OL}; maximum source current per pin = 6 mA at V_{OH}.
(5) Time from close of error ADC sample window to time when digitally calculated control effort (duty cycle) is available. This delay, which has no variation associated with it, must be accounted for when calculating the system dynamic response.
(6) Characterized by design and not production tested.
(7) Ambient temperature offset value should be used from the TEMPSENCTRL register to meet accuracy.
(8) Available from reference DACs for comparators D, E, F, and G.

8.6 Timing and Switching Characteristics

The timing characteristics and timing diagram for the communications interface that supports I²C, SMBus, and PMBus in Slave or Master mode are shown in PMBus/SMBus/I²C Timing, I²C/SMBus/PMBus Timing Diagram, and Bus Timing in Extended Mode. The numbers in PMBus/SMBus/I²C Timing arµe for 400 kHz operating frequency. However, the device supports all three speeds, standard (100 kHz), fast (400 kHz), and fast mode plus (1 MHz).

表 8-1. PMBus/SMBus/I²C Timing

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Typical values at T_A = 25°C and VCC = 3.3 V (unless otherwise noted)						
f_{SMB}	SMBus/PMBus operating frequency	Slave mode, SMBC 50% duty cycle		100	1000	kHz
f_{I2C}	I²C operating frequency	Slave mode, SCL 50% duty cycle		100	1000	kHz
$t_{(BUF)}$	Bus free time between start and stop			1.3		µs
$t_{(HD:STA)}$	Hold time after (repeated) start(1)			0.6		µs
$t_{(SU:STA)}$	Repeated start setup time(1)			0.6		µs
$t_{(SU:STO)}$	Stop setup time(1)			0.6		µs
$t_{(HD:DAT)}$	Data hold time	Receive mode		0		ns
$t_{(SU:DAT)}$	Data setup time			100		ns

表 8-1. PMBus/SMBus/I²C Timing (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(TIMEOUT)}$	Error signal/detect(2)				35	ms
$t_{(LOW)}$	Clock low period			1.3		µs
$t_{(HIGH)}$	Clock high period(3)			0.6		µs
$t_{(LOW:SEXT)}$	Cumulative clock low slave extend time(4)				25	ms
t_f	Clock/data fall time	Fall time t_f = 0.9 VDD to (V_{ILmax} – 0.15)	20 + 0.1 Cb(5)		300	ns
t_r	Clock/data rise time	Rise time t_r = (V_{ILmax} – 0.15) to (V_{IHmin} + 0.15)	20 + 0.1 Cb(5)		300	ns
C_b	Total capacitance of one bus line				400	pF

(1) Fast mode, 400 kHz
(2) The device times out when any clock low exceeds $t_{(TIMEOUT)}$.
(3) $t_{(HIGH)}$, Max, is the minimum bus idle time. SMBC = SMBD = 1 for t > 50 ms causes reset of any transaction that is in progress. This specification is valid when the NC_SMB control bit remains in the default cleared state (CLK[0] = 0).
(4) $t_{(LOW:SEXT)}$ is the cumulative time a slave device is allowed to extend the clock cycles in one message from initial start to the stop.
(5) C_b (pF)

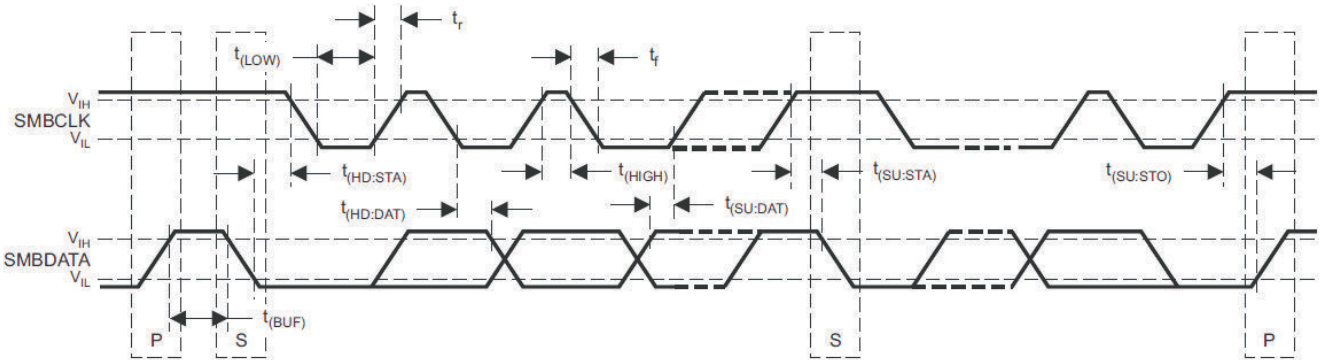

図 8-1. I²C/SMBus/PMBus Timing Diagram

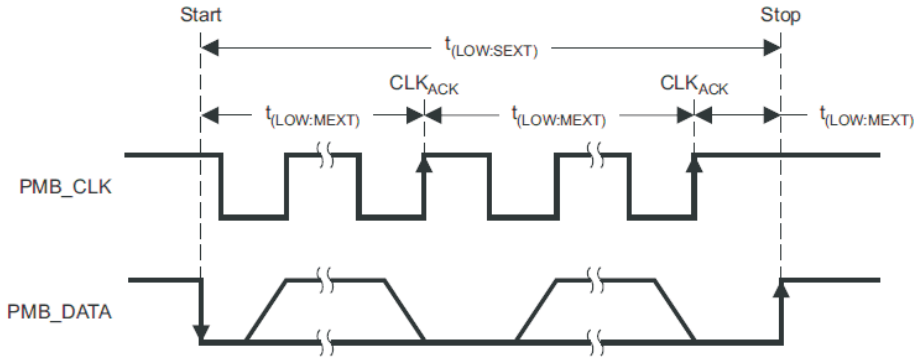

図 8-2. Bus Timing in Extended Mode

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8.7 Power Supply Sequencing

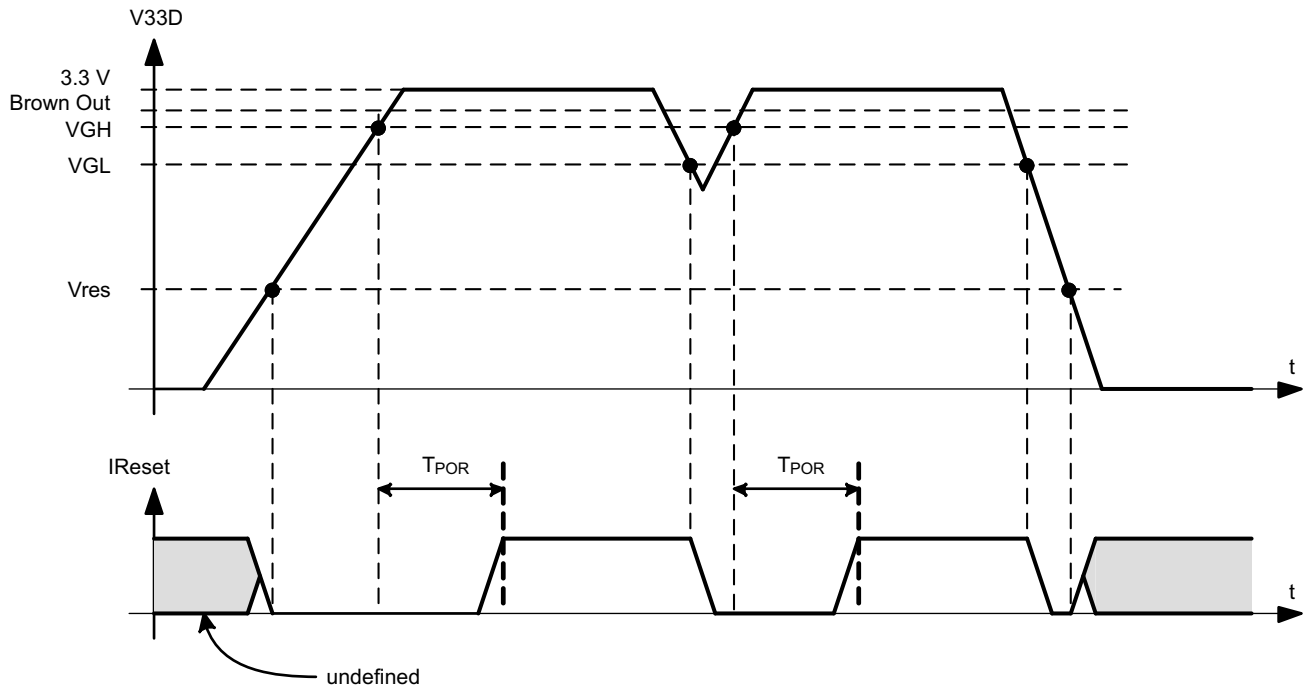

図 8-3. Power-On Reset (POR) and Brown-Out Reset (BOR)

表 8-2. Power-On Reset (POR) and Brown-Out Reset (BOR) Term Definitions

TERM	DEFINITION
VGH	This is the V33D threshold where the internal power is declared good. The UCD3138 comes out of reset when above this threshold.
VGL	This is the V33D threshold where the internal power is declared bad. The device goes into reset when below this threshold.
V_{res}	This is the V33D threshold where the internal reset signal is no longer valid. Below this threshold the device is in an indeterminate state.
I_{Reset}	This is the internal reset signal. When low, the device is held in reset. This is equivalent to holding the reset pin on the IC high.
T_{POR}	The time delay from when VGH is exceeded to when the device comes out of reset.
Brown out	This is the V33D voltage threshold at which the device sets the brown out status bit. In addition an interrupt can be triggered if enabled.

8.8 Peripherals

8.8.1 Digital Power Peripherals (DPPs)

At the core of the UCD3138 controller are three DDPs. Each DPP can be configured to drive from one to eight DPWM outputs. Each DPP consists of:

- Differential input error ADC (EADC) with sophisticated controls
- Hardware accelerated digital 2-pole/2-zero PID based compensator
- Digital PWM module with support for a variety of topologies

These can be connected in many different combinations, with multiple filters and DPWMs. They are capable of supporting functions like input voltage feed forward, current mode control, and constant current/constant power, and so forth. The simplest configuration is shown in the following figure:

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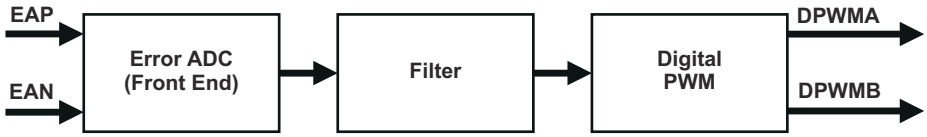

8.8.1.1 Front End

図 8-4 shows the block diagram of the front end module. It consists of a differential amplifier, an adjustable gain error amplifier, a high speed flash analog to digital converter (EADC), digital averaging filters and a precision high resolution set point DAC reference. The programmable gain amplifier in concert with the EADC and the adjustable digital gain on the EADC output work together to provide 9 bits of range with 6 bits of resolution on the EADC output. The output of the Front End module is a 9-bit sign extended result with a gain of 1 LSB / mV. Depending on the value of AFE selected, the resolution of this output could be either 1, 2, 4 or 8 LSBs. In addition Front End 0 has the ability to automatically select the AFE value such that the minimum resolution is maintained that still allows the voltage to fit within the range of the measurement. The EADC control logic receives the sample request from the DPWM module for initiating an EADC conversion. EADC control circuitry captures the EADC-9-bit-code and strobes the digital compensator for processing of the representative error. The set point DAC has 10 bits with an additional 4 bits of dithering resulting in an effective resolution of 14 bits. This DAC can be driven from a variety of sources to facilitate things like soft start, nested loops, and so forth. Some additional features include the ability to change the polarity of the error measurement and an absolute value mode which automatically adds the DAC value to the error.

It is possible to operate the controller in a peak current mode control configuration; front-end 2 is recommended for implementing peak current mode control. In this mode topologies like the phase shifted full bridge converter can be controlled to maintain transformer flux balance. The internal DAC can be ramped at a synchronously controlled slew rate to achieve a programmable slope compensation. This eliminates the sub-harmonic oscillation as well as improves input voltage feed-forward performance. A0 is a unity gain buffer used to isolate the peak current mode comparator. The offset of this buffer is specified in *セクション 8.5*.

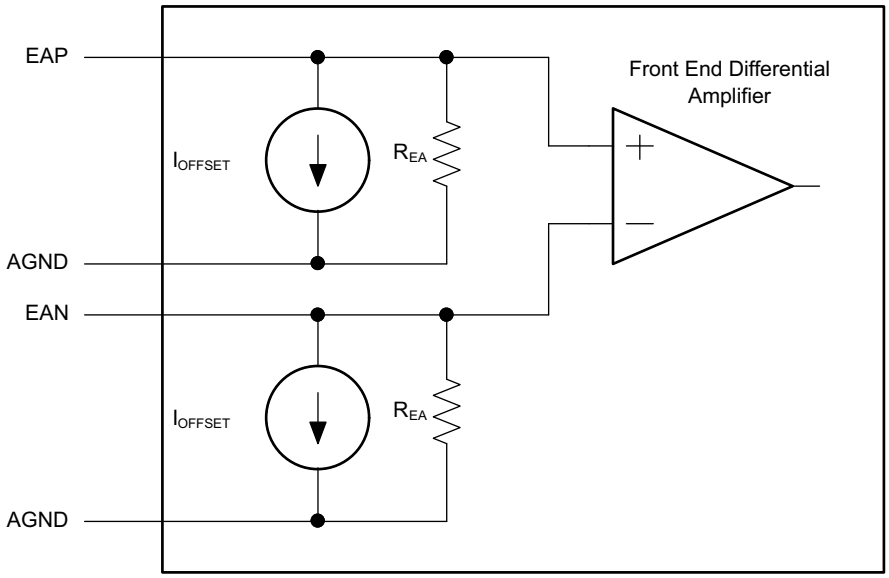

図 8-4. Input Stage of EADC Module

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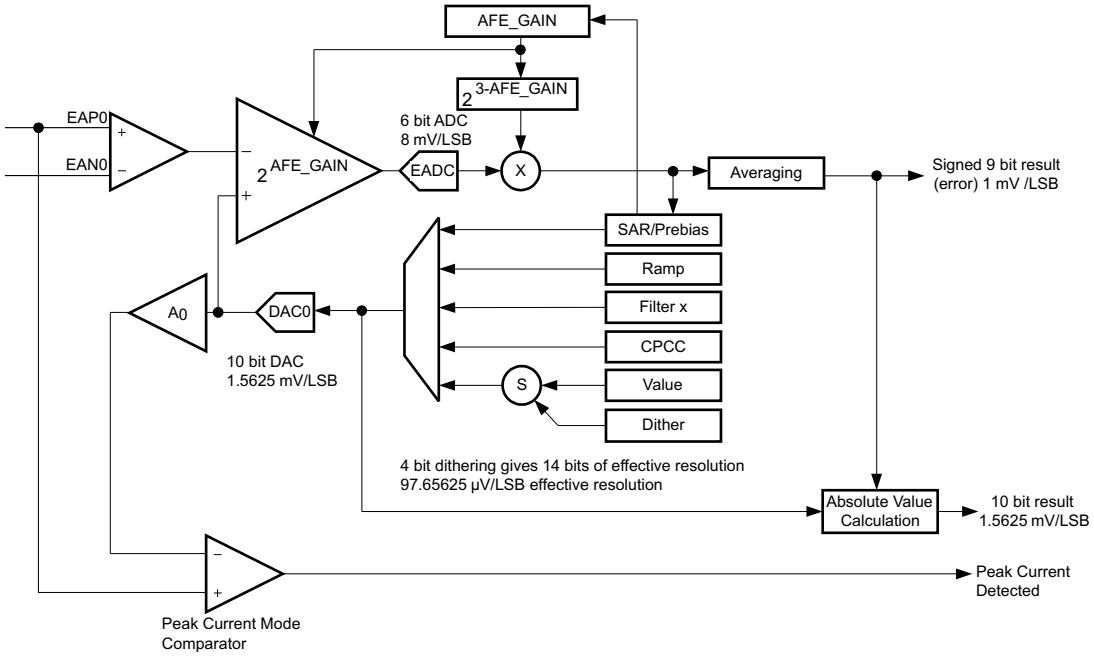

図 8-5. Front End Module (Front End 2 Recommended for Peak Current Mode Control)

8.8.1.2 DPWM Module

The DPWM module represents one complete DPWM channel with 2 independent outputs, A and B. Multiple DPWM modules within the UCD3138 system can be configured to support all key power topologies. DPWM modules can be used as independent DPWM outputs, each controlling one power supply output voltage rail. It can also be used as a synchronized DPWM—with user selectable phase shift between the DPWM channels to control power supply outputs with multiphase or interleaved DPWM configurations.

The output of the filter feeds the high resolution DPWM module. The DPWM module produces the pulse width modulated outputs for the power stage switches. The compensator calculates the necessary duty ratio as a 24-bit number in Q23 fixed point format (23 bit integer with 1 sign bit). This represents a value within the range 0.0 to 1.0. This duty ratio value is used to generate the corresponding DPWM output ON time. The resolution of the DPWM ON time is 250 psec.

Each DPWM module can be synchronized to another module or to an external sync signal. An input SYNC signal causes a DPWM ramp timer to reset. The SYNC signal outputs—from each of the four DPWM modules—occur when the ramp timer crosses a programmed threshold. In this way the phase of the DPWM outputs for multiple power stages can be tightly controlled.

The DPWM logic is probably the most complex of the Digital Peripherals. It takes the output of the compensator and converts it into the correct DPWM output for several power supply topologies. It provides for programmable dead times and cycle adjustments for current balancing between phases. It controls the triggering of the EADC. It can synchronize to other DPWMs or to external sources. It can provide synchronization information to other DPWMs or to external recipients. In addition, it interfaces to several fault handling circuits. Some of the control for these fault handling circuits is in the DPWM registers. Fault handling is covered in the Fault Mux section.

Each DPWM module supports the following features:

- Dedicated 14 bit time-base with period and frequency control
- Shadow period register for end of period updates.
- Quad-event control registers (A and B, rising and falling) (Events 1 to 4)
  - Used for on/off DPWM duty ratio updates.
- Phase control relative to other DPWM modules
- Sample trigger placement for output voltage sensing at any point during the DPWM cycle.
- Support for two independent edge placement DPWM outputs (same frequency or period setting)

- Dead-time between DPWM A and B outputs
- High Resolution capabilities – 250 ps
- Pulse cycle adjustment of up to ±8.192 µs (32768 × 250 ps)
- Active high/ active low output polarity selection
- Provides events to trigger both CPU interrupts and start of ADC12 conversions.

8.8.1.3 DPWM Events

Each DPWM can control the following timing events:

1. *Sample Trigger Count*–This register defines where the error voltage is sampled by the EADC in relationship to the DPWM period. The programmed value set in the register should be one fourth of the value calculated based on the DPWM clock. As the DCLK (DCLK = 62.5 MHz max) controlling the circuitry runs at one fourth of the DPWM clock (PCLK = 250 MHz max). When this sample trigger count is equal to the DPWM Counter, it initiates a front end calculation by triggering the EADC, resulting in a CLA calculation, and a DPWM update. Oversampling can be set for 2, 4, or 8 times the sampling rate.
2. *Phase Trigger Count* – count offset for slaving another DPWM (Multi-Phase/Interleaved operation).
3. *Period* – low resolution switching period count. (count of PCLK cycles)
4. *Event 1* – count offset for rising DPWM A event. (PCLK cycles)
5. *Event 2* – DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3* – DPWM count for rising DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
7. *Event 4* – DPWM count for falling DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
8. *Cycle Adjust* – Constant offset for Event 2 and Event 4 adjustments.

Basic comparisons between the programmed registers and the DPWM counter can create the desired edge placements in the DPWM. High resolution edge capability is available on Events 2, 3, and 4.

図 8-6 is for multi-mode, open loop. Open loop means that the DPWM is controlled entirely by its own registers, not by the filter output. In other words, the power supply control loop is not closed.

The Sample Trigger signals are used to trigger the front end to sample input signals. The Blanking signals are used to blank fault measurements during noisy events, such as FET turn on and turn off. Additional DPWM modes are described below.

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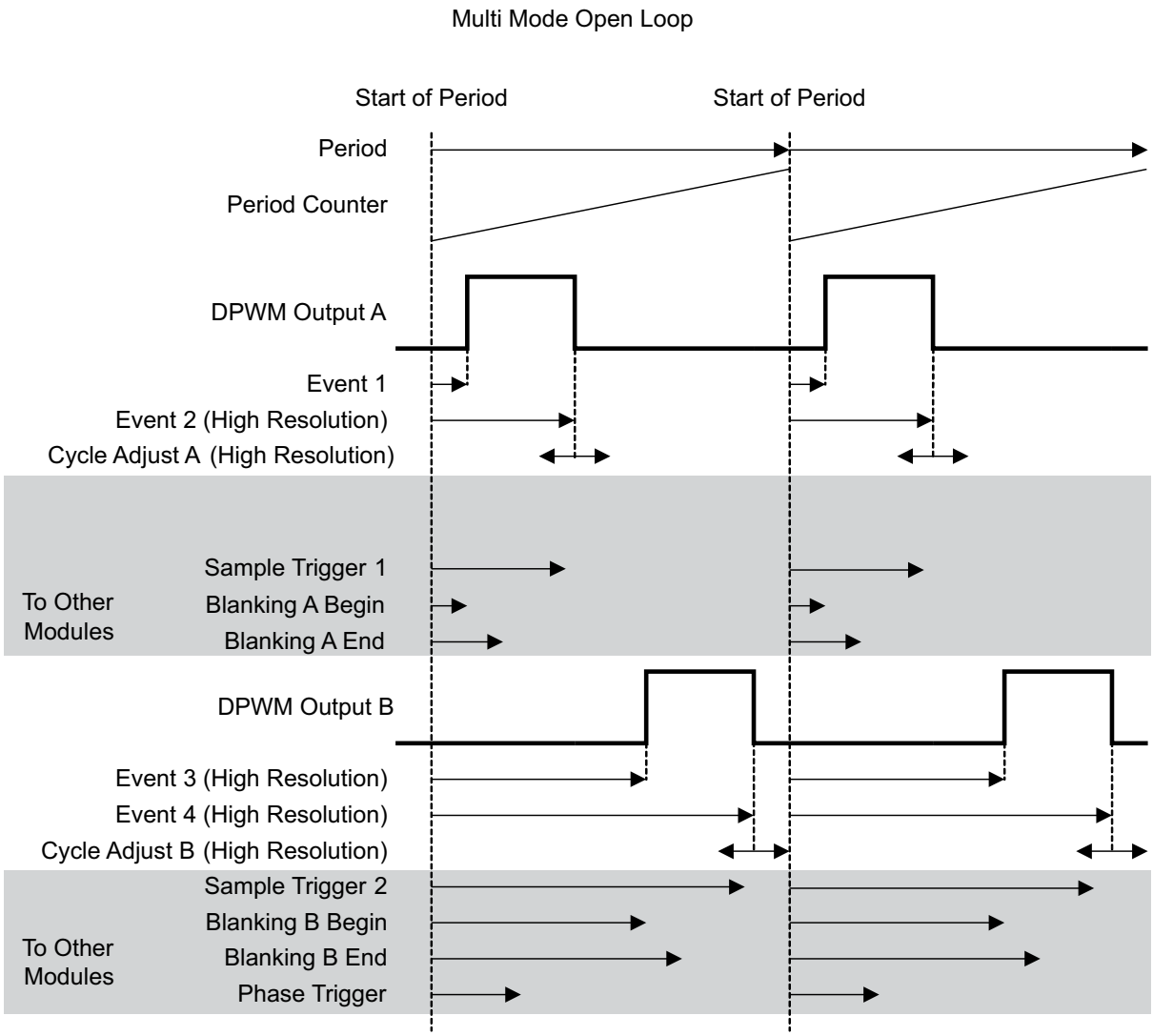

Events which change with DPWM mode:

DPWM A Rising Edge = Event 1
DPWM A Falling Edge = Event 2 + Cycle Adjust A
DPWM B Rising Edge = Event 3
DPWM B Falling Edge = Event 4 + Cycle Adjust B
Phase Trigger = Phase Trigger Register value

Events always set by their registers, regardless of mode:

Sample Trigger 1, Sample Trigger 2, Blanking A Begin, Blanking A End, Blanking B Begin, Blanking B End

図 8-6. Multi Mode Open Loop

8.8.1.4 High Resolution DPWM

Unlike conventional PWM controllers where the frequency of the clock dictates the maximum resolution of PWM edges, the UCD3138 DPWM can generate waveforms with resolutions as small as 250 ps. This is 16× the resolution of the clock driving the DPWM module.

This is achieved by providing the DPWM mechanism with 16 phase shifted clock signals of 250 MHz each. The high resolution section of DPWM can be enabled or disabled, also the resolution can be defined in several steps between 4ns to 250ps. This is done by setting the values of PWM_HR_MULTI_OUT_EN, HIRES_SCALE, and ALL_PHASE_CLK_ENA inside the DPWM Control register 1. See the Power Peripherals programmer's manual for details.

8.8.1.5 Oversampling

The DPWM module has the capability to trigger an oversampling event by initiating the EADC to sample the error voltage. The default 00 configuration has the DPWM trigger the EADC once based on the sample trigger register value. The over sampling register has the ability to trigger the sampling 2, 4 or 8 times per PWM period. Thus the time the over sample happens is at the divide by 2, 4, or 8 time set in the sampling register. The 01 setting triggers 2X oversampling, the 10 setting triggers 4X over sampling, and the 11 triggers oversampling at 8X.

8.8.1.6 DPWM Interrupt Generation

The DPWM has the capability to generate a CPU interrupt based on the PWM frequency programmed in the period register. The interrupt can be scaled by a divider ratio of up to 255 for developing a slower interrupt service execution loop. This interrupt can be fed to the ADC circuitry for providing an ADC12 trigger for sequence synchronization. 表 8-3 outlines the divide ratios that can be programmed.

8.8.1.7 DPWM Interrupt Scaling/Range

表 8-3. DPWM Interrupt Divide Ratio

Interrupt Divide Setting	Interrupt Divide Count	Interrupt Divide Count (hex)	Switching Period Frames (Assume 1-MHz Loop)	Number of 32-MHz Processor Cycles
1	0	00	1	32
2	1	01	2	64
3	3	03	4	128
4	7	07	8	256
5	15	0F	16	512
6	31	1F	32	1024
7	47	2F	48	1536
8	63	3F	64	2048
9	79	4F	80	2560
10	95	5F	96	3072
11	127	7F	128	4096
12	159	9F	160	5120
13	191	BF	192	6144
14	223	DF	224	7168
15	255	FF	256	8192

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8.9 Typical Temperature Characteristics

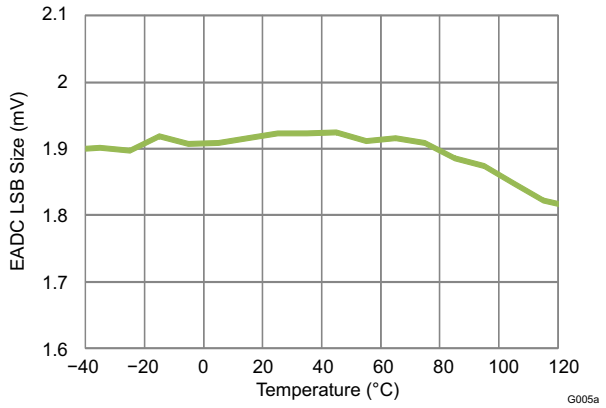

図 8-7. EADC LSB Size With 4X Gain (mV) vs Temperature

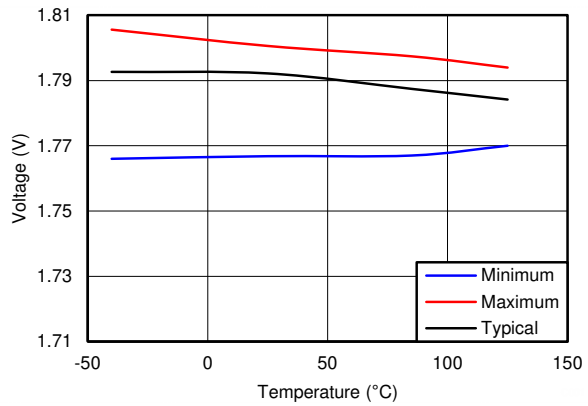

図 8-8. BP18 Voltage vs Temperature

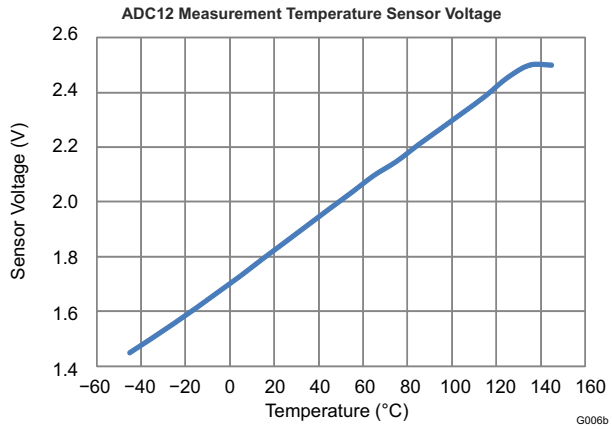

図 8-9. ADC12 Measurement Temperature Sensor Voltage vs Temperature

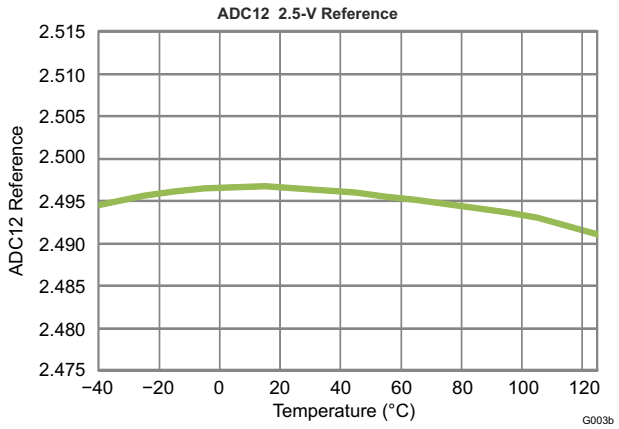

図 8-10. ADC12 2.5-V Reference vs Temperature

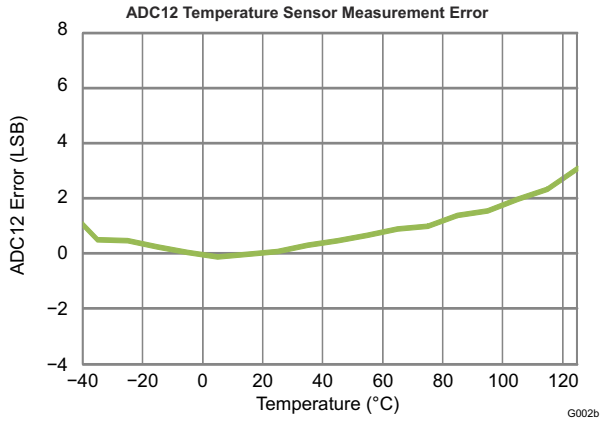

図 8-11. ADC12 Temperature Sensor Measurement Error vs Temperature

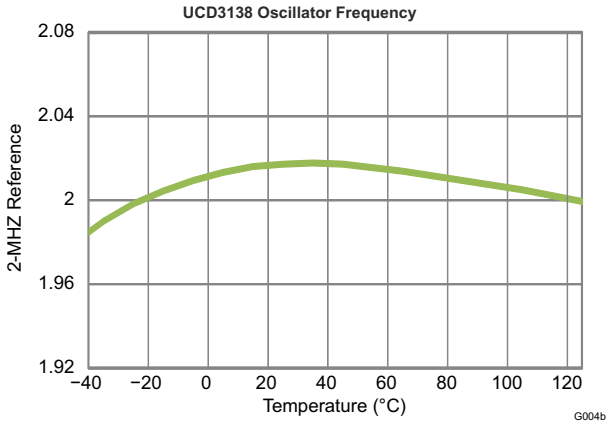

図 8-12. UCD3138 Oscillator Frequency (2-MHz Reference, Divided Down from 250 MHz) vs Temperature

9 Detailed Description

9.1 Overview

The UCD3138 family is a digital power supply controller from Texas Instruments offering superior levels of integration and performance in a single chip solution. The UCD3138x, in comparison to Texas Instruments UCD3138 digital power controller offers 32 kB of program Flash memory. The flexible nature of the UCD3138 family makes it suitable for a wide variety of power conversion applications.

In addition, multiple peripherals inside the device have been specifically optimized to enhance the performance of AC/DC and isolated DC/DC applications and reduce the solution component count in the IT and network infrastructure space. The UCD3138 family is a fully programmable solution offering customers complete control of their application, along with ample ability to differentiate their solution. At the same time, TI is committed to simplifying our customer's development effort through offering best in class development tools, including application firmware, Code Composer StudioTM software development environment, and TI's Fusion Power Development GUI which enables customers to configure and monitor key system parameters.

9.2 ARM Processor

The ARM7TDMI-S processor is a synthesizable member of the ARM family of general purpose 32-bit microprocessors. The ARM architecture is based on RISC (Reduced Instruction Set Computer) principles where two instruction sets are available. The 32-bit ARM instruction set and the 16-bit Thumb instruction set. The Thumb instruction allows for higher code density equivalent to a 16-bit microprocessor, with the performance of the 32-bit microprocessor.

The three-staged pipelined ARM processor has fetch, decode and execute stage architecture. Major blocks in the ARM processor include a 32-bit ALU, 32 x 8 multiplier, and a barrel shifter.

9.3 Memory

The UCD3138 (ARM7TDMI-S) is a Von-Neumann architecture, where a single bus provides access to all of the memory modules. All of the memory module addresses are sequentially aligned along the same address range. This applies to program flash, data flash, ROM and all other peripherals.

Within the UCD3138 architecture, there is a Boot ROM that contains the initial firmware startup routines for PMBUS communication and non-volatile (FLASH) memory download. This boot ROM is executed after power-up-reset checks if there is a valid FLASH program written. If a valid program is present, the ROM code branches to the main FLASH-program execution.

UCD3138 also supports customization of the boot program by allowing an alternative boot routine to be executed from program FLASH. This feature enables assignment of a unique address to each device; therefore, enabling firmware reprogramming even when several devices are connected on the same communication bus.

Two separate FLASH memory areas are present inside the device. The 32 kB Program FLASH is organized as an 8 k x 32 bit memory block and is intended to be for the firmware program. The block is configured with page erase capability for erasing blocks as small as 1kB per page, or with a mass erase for erasing the entire program FLASH array. The FLASH endurance is specified at 1000 erase/write cycles and the data retention is good for 100 years. The 2 kB data FLASH array is organized as a 512 x 32 bit memory (32 byte page size). The Data FLASH is intended for firmware data value storage and data logging. Thus, the Data FLASH is specified as a high endurance memory of 20 k cycles with embedded error correction code (ECC).

For run time data storage and scratchpad memory, a 4 kB RAM is available. The RAM is organized as a 1 k x 32 bit array.

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9.3.1 CPU Memory Map and Interrupts

When the device comes out of power-on-reset, the data memories are mapped to the processor as follows:

表 9-1. Memory Map (After Reset Operation)

Address	Size	Module
0x0000_0000 – 0x0000_FFFF In 16 repeated blocks of 4K each	16 X 4K	Boot ROM
0x0001_0000 – 0x0001_7FFF	32K	Program flash
0x0001_8800 – 0x0001_8FFF	2K	Data flash
0x0001_9000 – 0x0001_9FFF	4K	Data RAM

Just before the boot ROM program gives control to FLASH program, the ROM configures the memory as follows:

表 9-2. Memory Map (Normal Operation)

Address	Size	Module
0x0000_0000 – 0x0000_7FFF	32K	Program flash
0x0001_0000 – 0x0001_AFFF	4K	Boot ROM
0x0001_8800 – 0x0001_8FFF	2K	Data flash
0x0001_9000 – 0x0001_9FFF	4K	Data RAM

表 9-3. Memory Map (System and Peripherals Blocks)

Address	Size	Module
0x0002_0000 - 0x0002_00FF	256	Loop Mux
0x0003_0000 - 0x0003_00FF	256	Fault Mux
0x0004_0000 - 0x0004_00FF	256	ADC
0x0005_0000 - 0x0005_00FF	256	DPWM 3
0x0006_0000 - 0x0006_00FF	256	Filter 2
0x0007_0000 - 0x0007_00FF	256	DPWM 2
0x0008_0000 - 0x0008_00FF	256	Front End/Ramp I/F 2
0x0009_0000 - 0x0009_00FF	256	Filter 1
0x000A_0000 - 0x000A_00FF	256	DPWM 1
0x000B_0000 – 0x000B_00FF	256	Front End/Ramp I/F 1
0x000C_0000 - 0x000C_00FF	256	Filter 0
0x000D_0000 - 0x000D_00FF	256	DPWM 0
0x000E_0000 - 0x000E_00FF	256	Front End/Ramp I/F 0
0xFFF7_EC00 - 0xFFF7_ECFF	256	UART 0
0xFFF7_ED00 - 0xFFF7_EDFF	256	UART 1
0xFFF7_F000 - 0xFFF7_F0FF	256	Miscellaneous Analog Control
0xFFF7_F600 - 0xFFF7_F6FF	256	PMBus Interface
0xFFF7_FA00 - 0xFFF7_FAFF	256	GIO
0xFFF7_FD00 - 0xFFF7_FDFF	256	Timer
0xFFFF_FD00 - 0xFFFF_FDFF	256	MMC
0xFFFF_FE00 - 0xFFFF_FEFF	256	DEC
0xFFFF_FF20 - 0xFFFF_FF37	23	CIM
0xFFFF_FF40 - 0xFFFF_FF50	16	PSA
0xFFFF_FFD0 - 0xFFFF_FFEC	28	SYS

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The registers and bit definitions inside the system and peripheral blocks are detailed in the programmer's guide for each peripheral.

9.3.2 Boot ROM

The UCD3138 incorporates a 4k boot ROM. This boot ROM includes support for:

- Program download through the PMBus
- Device initialization
- Examining and modifying registers and memory
- Verifying and executing program FLASH automatically
- Jumping to a customer defined boot program

The Boot ROM is entered automatically on device reset. It initializes the device and then performs checksums on the Program FLASH. If the first 2 kB of program FLASH has a valid checksum, the program jumps to location 0 in the Program FLASH. This permits the use of a customer boot program. If the first checksum fails, it performs a checksum on the complete 32 kB of program flash. If this is valid, it also jumps to location 0 in the program flash. This permits full automated program memory checking, when there is no need for a custom boot program.

If neither checksum is valid, the Boot ROM stays in control, and accepts commands via the PMBus interface

These functions can be used to read and write to all memory locations in the UCD3138. Typically they are used to download a program to Program Flash, and to command its execution

9.3.3 Customer Boot Program

As described above, it is possible to generate a user boot program using 2 kB or more of the program flash. This can support things which the Boot ROM does not support, including:

- Program download via UART – useful especially for applications where the UCD3138 is isolated from the host (for example, PFC)
- Encrypted download – useful for code security in field updates.

9.3.4 Flash Management

The UCD3138 offers a variety of features providing for easy prototyping and easy flash programming. At the same time, high levels of security are possible for production code, even with field updates. Standard firmware will be provided for storing multiple copies of system parameters in data flash. This is minimizes the risk of losing information if programming is interrupted.

9.4 System Module

The System Module contains the interface logic and configuration registers to control and configure all the memory, peripherals and interrupt mechanisms. The blocks inside the system module are the address decoder, memory management controller, system management unit, central interrupt unit, and clock control unit.

9.4.1 Address Decoder (DEC)

The Address Decoder generates the memory selects for the FLASH, ROM and RAM arrays. The memory map addresses are selectable through configurable register settings. These memory selects can be configured from 1 kB to 16 MB. Power on reset uses the default addresses in the memory map for ROM execution, which is then configured by the ROM code to the application setup. During access to the DEC registers, a wait state is asserted to the CPU. DEC registers are only writable in the ARM privilege mode for user mode protection.

9.4.2 Memory Management Controller (MMC)

The MMC manages the interface to the peripherals by controlling the interface bus for extending the read and write accesses to each peripheral. The unit generates eight peripheral select lines with 1 kB of address space decoding.

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9.4.3 System Management (SYS)

The SYS unit contains the software access protection by configuring user privilege levels to memory or peripherals modules. It contains the ability to generate fault or reset conditions on decoding of illegal address or access conditions. A clock control setup for the processor clock (MCLK) speed, is also available.

9.4.4 Central Interrupt Module (CIM)

The CIM accepts 32 interrupt requests for meeting firmware timing requirements. The ARM processor supports two interrupt levels: FIQ and IRQ. FIQ is the highest priority interrupt. The CIM provides hardware expansion of interrupts by use of FIQ/IRQ vector registers for providing the offset index in a vector table. This numerical index value indicates the highest precedence channel with a pending interrupt and is used to locate the interrupt vector address from the interrupt vector table. Interrupt channel 0 has the lowest precedence and interrupt channel 31 has the highest precedence. To remove the interrupt request, the firmware should clear the request as the first action in the interrupt service routine. The request channels are maskable, allowing individual channels to be selectively disabled or enabled.

表 9-4. Interrupt Priority Table

NAME	MODULE COMPONENT OR REGISTER	DESCRIPTION	PRIORITY
BRN_OUT_INT	Brownout	Brownout interrupt	0 (lowest)
EXT_INT	External interrupts	Interrupt on external input pin	1
WDRST_INT	Watchdog control	Interrupt from watchdog exceeded (reset)	2
WDWAKE_INT	Watchdog control	Wakeup interrupt when watchdog equals half of set watch time	3
SCI_ERR_INT	UART or SCI control	UART or SCI error Interrupt. Frame, parity or overrun	4
SCI_RX_0_INT	UART or SCI control	UART0 RX buffer has a byte	5
SCI_TX_0_INT	UART or SCI control	UART0 TX buffer empty	6
SCI_RX_1_INT	UART or SCI control	UART1 RX buffer has a byte	7
SCI_TX_1_INT	UART or SCI control	UART1 TX buffer empty	8
PMBUS_INT		PMBus related interrupt	9
DIG_COMP_INT	12-bit ADC control	Digital comparator interrupt	10
FE0_INT	Front End 0	“Prebias complete”, “Ramp Delay Complete”, “Ramp Complete”, “Load Step Detected”, “Over-Voltage Detected”, “EADC saturated”	11
FE1_INT	Front End 1	“Prebias complete”, “Ramp Delay Complete”, “Ramp Complete”, “Load Step Detected”, “Over-Voltage Detected”, “EADC saturated”	12
FE2_INT	Front End 2	“Prebias complete”, “Ramp Delay Complete”, “Ramp Complete”, “Load Step Detected”, “Over-Voltage Detected”, “EADC saturated”	13
PWM3_INT	16-bit timer PWM 3	16-bit Timer PWM3 counter overflow or compare interrupt	14
PWM2_INT	16-bit timer PWM 2	16-bit Timer PWM2 counter Overflow or compare interrupt	15
PWM1_INT	16-bit timer PWM 1	16-bit Timer PWM1 counter overflow or compare interrupt	16
PWM0_INT	16-bit timer PWM 0	16-bit Timer PWM1 counter overflow or compare interrupt	17
OVF24_INT	24-bit timer control	24-bit Timer counter overflow interrupt	18
CAPTURE_1_INT	24-bit timer control	24-bit Timer capture 1 interrupt	19
COMP_1_INT	24-bit timer control	24-bit Timer compare 1 interrupt	20
CAPTURE_0_INT	24-bit timer control	24-bit Timer capture 0 interrupt	21
COMP_0_INT	24-bit timer control	24-bit Timer compare 0 interrupt	22
CPCC_INT	Constant power constant current	Mode switched in CPCC module Flag needs to be read for details	23
ADC_CONV_INT	12-bit ADC control	ADC end of conversion interrupt	24

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表 9-4. Interrupt Priority Table (continued)

NAME	MODULE COMPONENT OR REGISTER	DESCRIPTION	PRIORITY
FAULT_INT	Fault Mux interrupt	Analog comparator interrupts, overvoltage detection, undervoltage detection, LLM load step detection	25
DPWM3	DPWM3	Same as DPWM1	26
DPWM2	DPWM2	Same as DPWM1	27
DPWM1	DPWM1	1) Every (1 to 256) switching cycles 2) Fault detection 3) Mode switching	28
DPWM0	DPWM0	Same as DPWM1	29
EXT_FAULT_INT	External Faults	Fault pin interrupt	30
SYS_SSI_INT	System Software	System software interrupt	31 (highest)

9.5 Feature Description

9.5.1 Sync FET Ramp and IDE Calculation

The UCD3138 has built in logic for controlling MOSFETs for synchronous rectification (Sync FETs). This comes in two forms:

- Sync FET ramp
- Ideal Diode Emulation (IDE) calculation

When starting up a power supply, sometimes there is already a voltage on the output – this is called prebias. It is very difficult to calculate the ideal Sync FET on-time for this case. If it is not calculated correctly, it may pull down the prebias voltage, causing the power supply to sink current.

To avoid this, Sync FETs are not turned on until after the power supply has ramped up to the nominal voltage. The Sync FETs are turned on gradually in order to avoid an output voltage glitch. The Sync FET Ramp logic can be used to turn them on at a rate below the bandwidth of the filter.

In discontinuous mode, the ideal on-time for the Sync FETs is a function of Vin, Vout, and the primary side duty cycle (D). The IDE logic in the UCD3138 takes Vin and Vout data from the firmware and combines it with D data from the filter hardware. It uses this information to calculate the ideal on-time for the Sync FETs.

9.5.2 Automatic Mode Switching

Automatic Mode switching enables the DPWM module to switch between modes automatically, with no firmware intervention. This is useful to increase efficiency and power range. The following paragraphs describe phase-shifted full bridge and LLC examples:

9.5.2.1 Phase Shifted Full Bridge Example

In phase shifted full bridge topologies, efficiency can be increased by using pulse width modulation, rather than phase shift, at light load. This is shown below:

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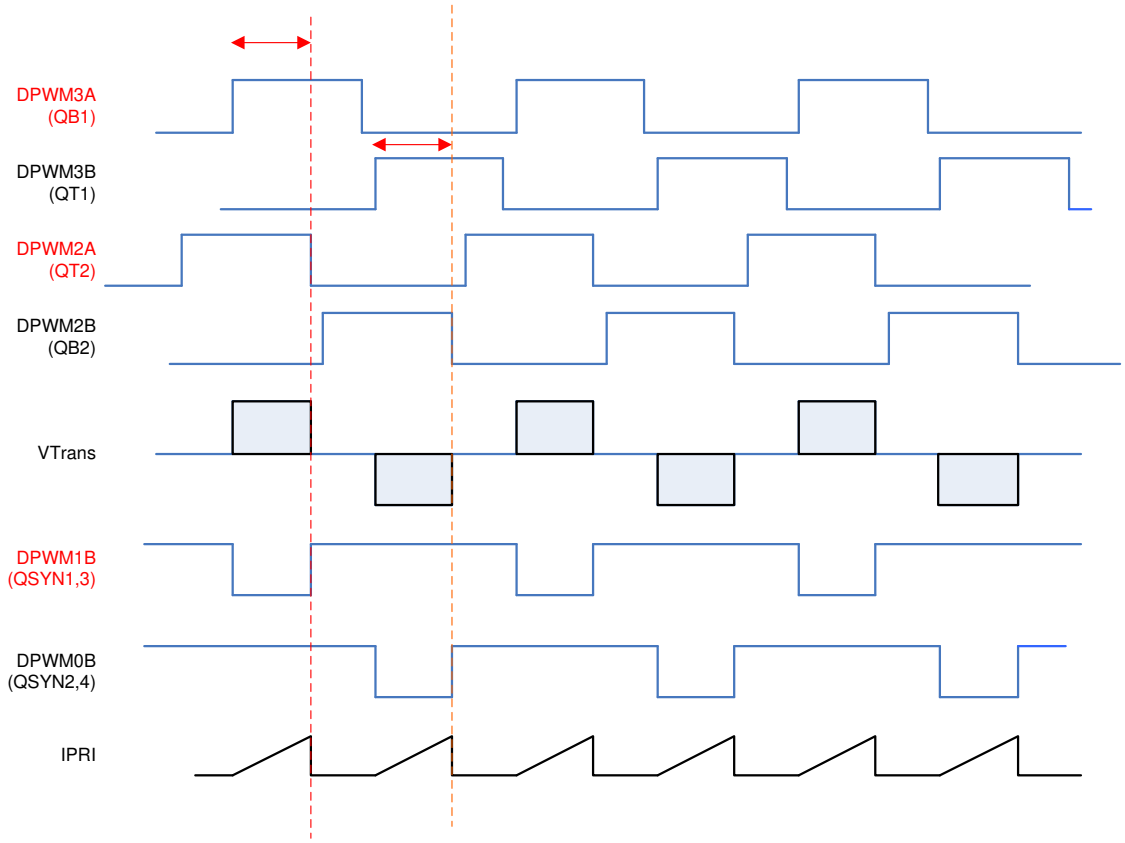


図 9-1. Phase Shifted Full Bridge

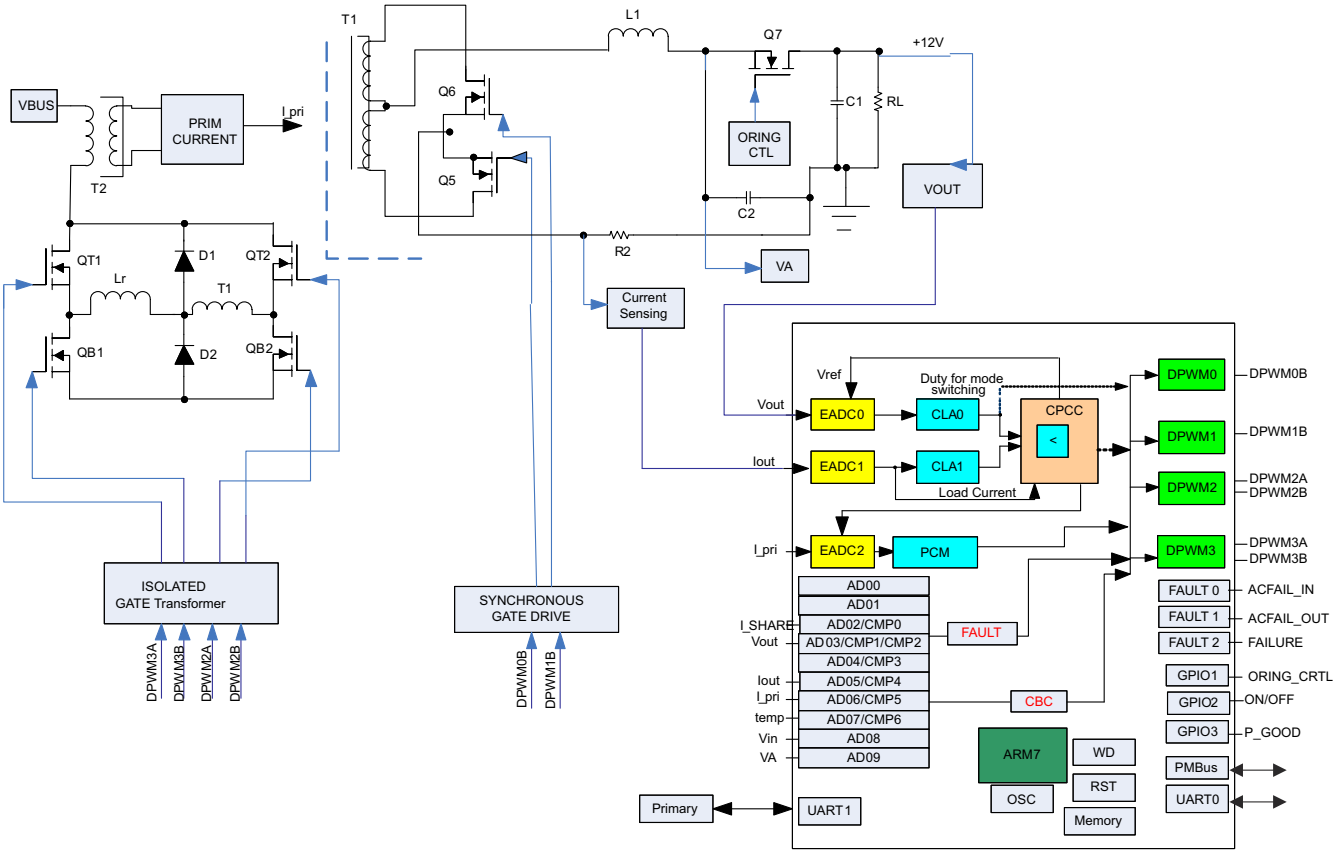
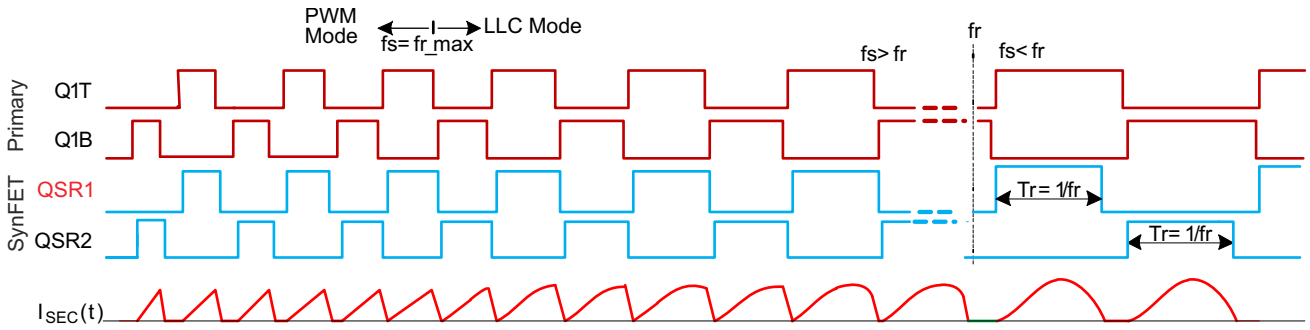


図 9-2. Secondary-Referenced Phase-Shifted Full Bridge Control With Synchronous Rectification

9.5.2.2 LLC Example

In LLC, three modes are used. At the highest frequency, a pulse width modulated mode (Multi Mode) is used. As the frequency decreases, resonant mode is used. As the frequency gets still lower, the synchronous MOSFET drive changes so that the on-time is fixed and does not increase. In addition, the LLC control supports cycle-by-cycle current limiting. This protection function operates by a comparator monitoring the maximum current during the DPWMA conduction time. Any time this current exceeds the programmable comparator reference the pulse is immediately terminated. Due to classic instability issues associated with half-bridge topologies it is also possible to force DPWMB to match the truncated pulse width of DPWMA. Here are the waveforms for the LLC:



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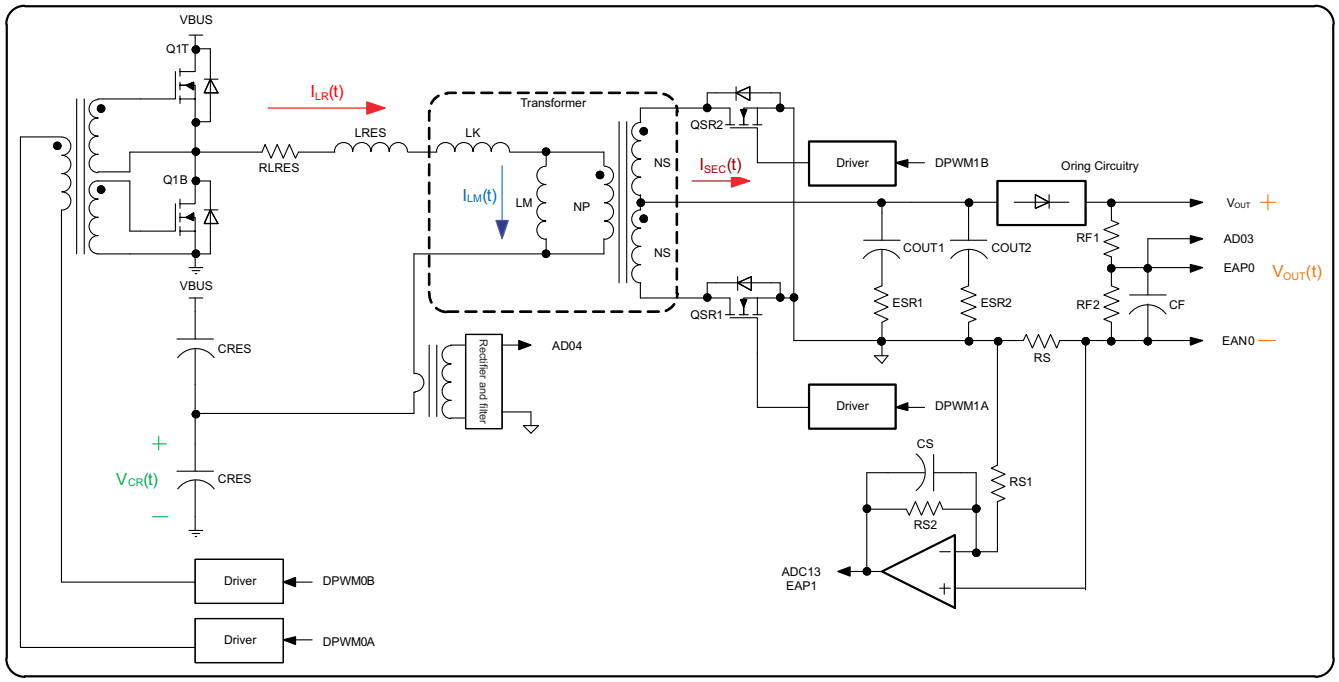

図 9-3. Secondary-Referenced Half-Bridge Resonant LLC Control With Synchronous Rectification

9.5.2.3 Mechanism for Automatic Mode Switching

The UCD3138 allows the customer to enable up to two distinct levels of automatic mode switching. These different modes are used to enhance light load operation, short circuit operation and soft start. Many of the configuration parameters for the DPWM are in DPWM Control Register 1. For automatic mode switching, some of these parameters are duplicated in the Auto Config Mid and Auto Config High registers.

If automatic mode switching is enabled, the filter duty signal is used to select which of these three registers is used. There are 4 registers which are used to select the points at which the mode switching takes place. They are used as shown below.

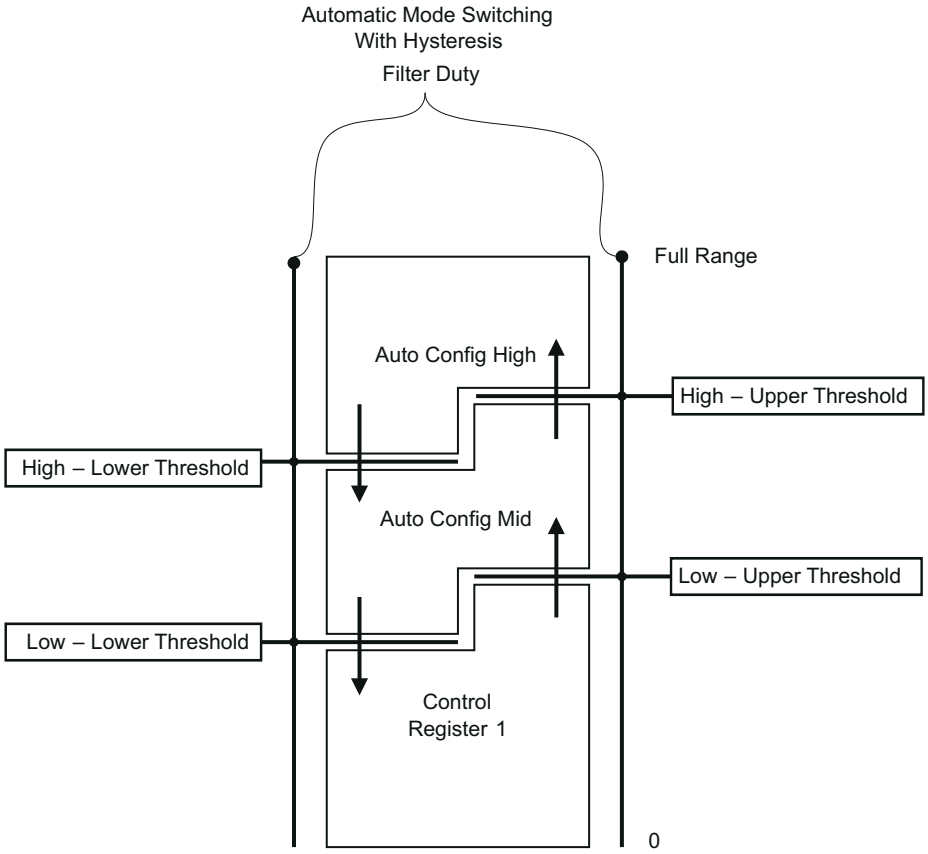

図 9-4. Automatic Mode Switching

As shown, the registers are used in pairs for hysteresis. The transition from Control Register 1 to Auto Config Mid only takes place when the Filter Duty goes above the Low Upper threshold. It does not go back to Auto Config Mid until the Low Lower Threshold is passed. This prevents oscillation between modes if the filter duty is close to a mode switching point.

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9.5.3 DPWMC, Edge Generation, IntraMux

The UCD3138 has hardware for generating complex waveforms beyond the simple DPWMA and DPWMB waveforms already discussed – DPWMC, the Edge Generation Module, and the IntraMux.

DPWMC is a signal inside the DPWM logic. It goes high at the Blanking A begin time, and low at the Blanking A end time.

The Edge Gen module takes DPWMA and DPWMB from its own DPWM module, and the next one, and uses them to generate edges for two outputs. For DPWM3, the DPWM0 is considered to be the next DPWM. Each edge (rising and falling for DPWMA and DPWMB) has 8 options which can cause it.

The options are:

0 = DPWM(n) A Rising edge
1 = DPWM(n) A Falling edge
2 = DPWM(n) B Rising edge
3 = DPWM(n) B Falling edge
4 = DPWM(n+1) A Rising edge
5 = DPWM(n+1) A Falling edge
6 = DPWM(n+1) B Rising edge
7 = DPWM(n+1) B Falling edge

Where “n" is the numerical index of the DPWM module of interest. For example n=1 refers to DPWM1.

The Edge Gen is controlled by the DPWMEDGEGEN register. It also has an enable/disable bit.

The IntraMux is controlled by the Auto Config registers. Intra Mux is short for intra multiplexer. The IntraMux takes signals from multiple DPWMs and from the Edge Gen and combines them logically to generate DPWMA and DPWMB signals This is useful for topologies like phase-shifted full bridge, especially when they are controlled with automatic mode switching. Of course, it can all be disabled, and DPWMA and DPWMB will be driven as described in the sections above. If the Intra Mux is enabled, high resolution must be disabled, and DPWM edge resolution goes down to 4 ns.

Here is a drawing of the Edge Gen/Intra Mux:

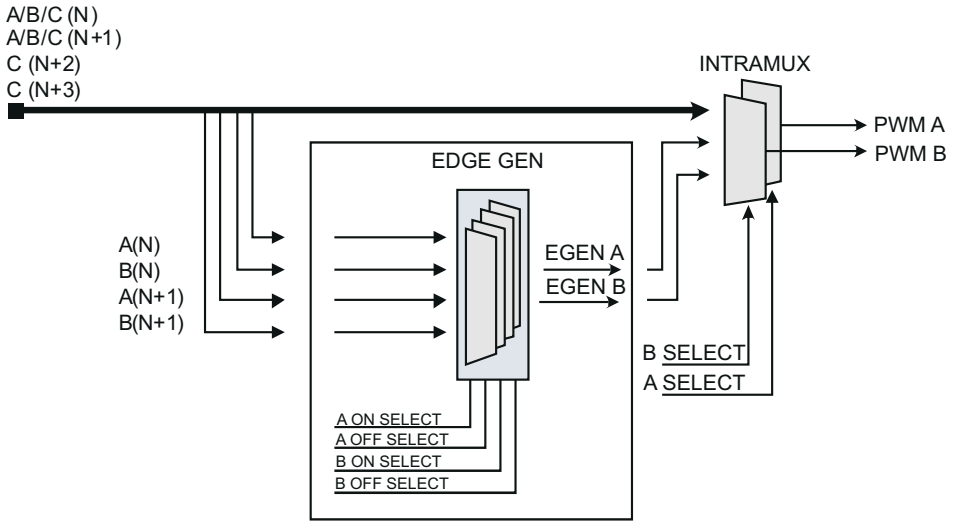

図 9-5. Edge Gen/Intra Mux

Here is a list of the IntraMux modes for DPWMA:

0 = DPWMA(n) pass through (default)
1 = Edge-gen output, DPWMA(n)
2 = DPWNC(n)

3 = DPWMB(n) (Crossover)
4 = DPWMA(n+1)
5 = DPWMB(n+1)
6 = DPWMC(n+1)
7 = DPWMC(n+2)
8 = DPWMC(n+3)

and for DPWMB:

0 = DPWMB(n) pass through (default)
1 = Edge-gen output, DPWMB(n)
2 = DPWNC(n)
3 = DPWMA(n) (Crossover)
4 = DPWMA(n+1)
5 = DPWMB(n+1)
6 = DPWMC(n+1)
7 = DPWMC(n+2)
8 = DPWMC(n+3)

The DPWM number wraps around just like the Edge Gen unit. For DPWM3 the following definitions apply:

DPWM(n)	DPWM3
DPWM(n+1)	DPWM0
DPWM(n+2)	DPWM1
DPWM(n+3)	DPWM2

9.5.4 Filter

The UCD3138 filter is a PID filter with many enhancements for power supply control. Some of its features include:

- Traditional PID Architecture
- Programmable non-linear limits for automated modification of filter coefficients based on received EADC error
- Multiple coefficient sets fully configurable by firmware
- Full 24-bit precision throughout filter calculations
- Programmable clamps on integrator branch and filter output
- Ability to load values into internal filter registers while system is running
- Ability to stall calculations on any of the individual filter branches
- Ability to turn off calculations on any of the individual filter branches
- Duty cycle, resonant period, or phase shift generation based on filter output.
- Flux balancing
- Voltage feed forward

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Here is the first section of the Filter :

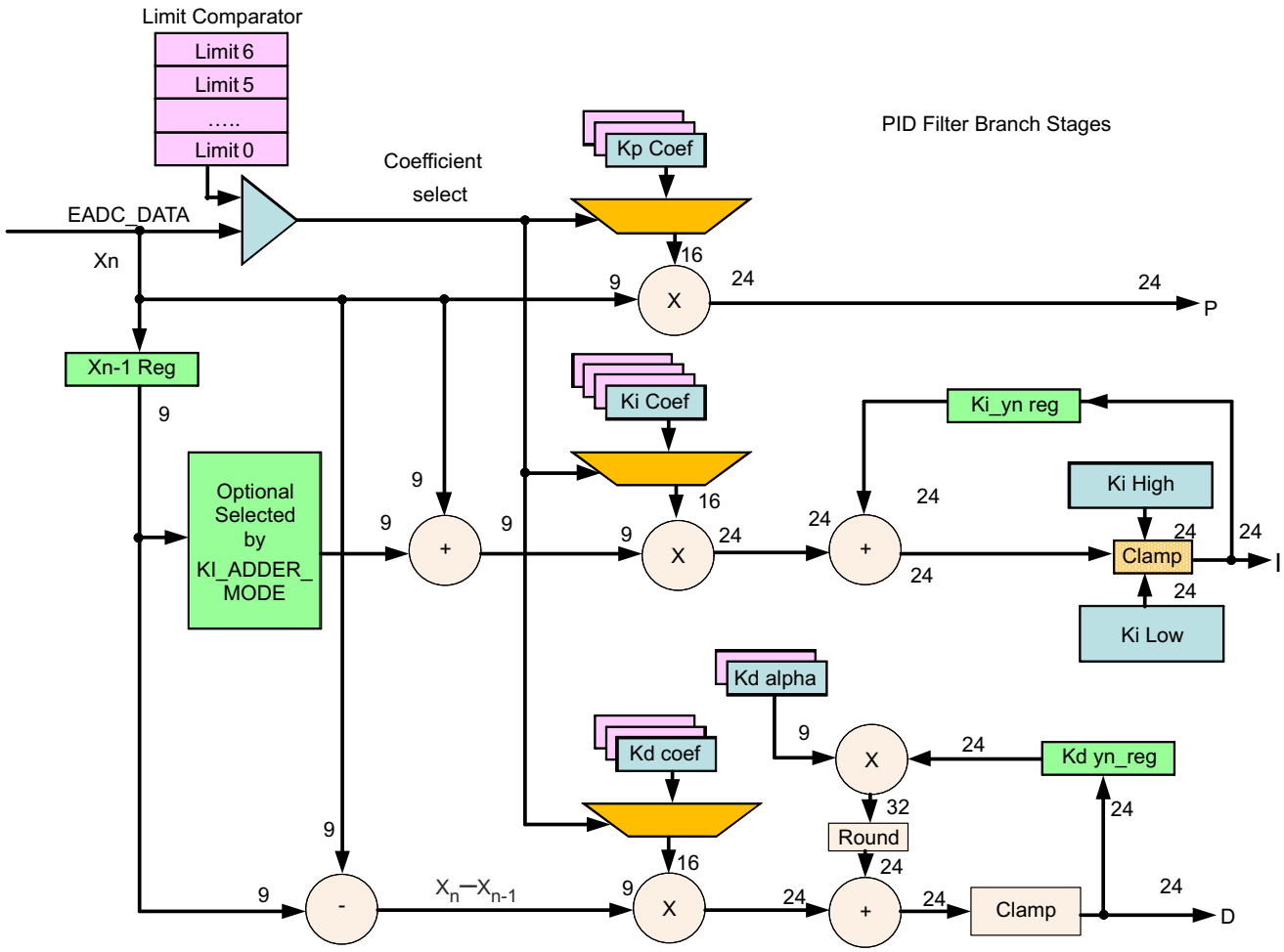

図 9-6. First Section of the Filter

The filter input, Xn, generally comes from a front end. Then there are three branches, P, I. and D. Note that the D branch also has a pole, Kd Alpha. Clamps are provided both on the I branch and on the D alpha pole.

The filter also supports a nonlinear mode, where up to 7 different sets of coefficients can be selected depending on the magnitude of the error input Xn. This can be used to increase the filter gain for higher errors to improve transient response.

Here is the output section of the filter (S0.23 means that there is 1 sign bit, 0 integer bits and 23 fractional bits):

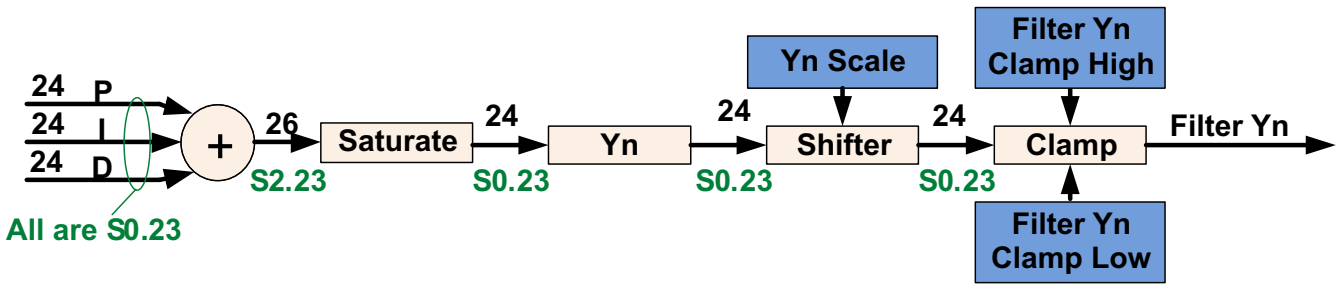

図 9-7. Output Section of the Filter

This section combines the P, I, and D sections, and provides for saturation, scaling, and clamping.

There is a final section for the filter, which permits its output to be matched to the DPWM:

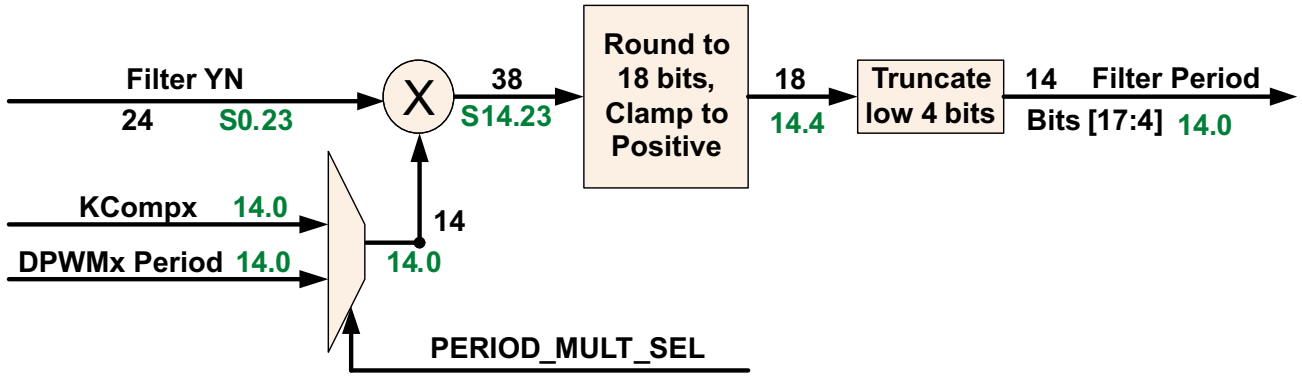

図 9-8. Final Section for the Filter

This permits the filter output to be multiplied by a variety of correction factors to match the DPWM Period, to provide for Voltage Feed Forward, or for other purposes. After this, there is another clamp. For resonant mode, the filter can be used to generate both period and duty cycle.

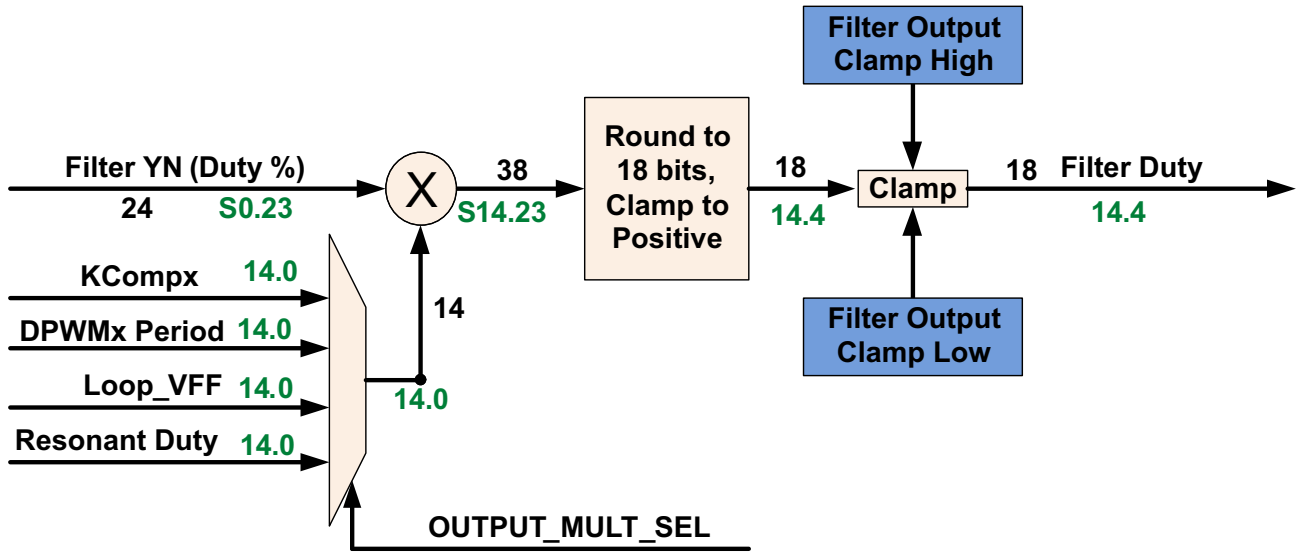

図 9-9. Resonant Mode

9.5.4.1 Loop Multiplexer

The Loop Mux controls interconnections between the filters, front ends, and DPWMs. Any filter, front end, and DPWM can be combined with each other in many configurations.

It also controls the following connections:

- DPWM to Front End
- Front End DAC control from Filters or Constant Current/Constant Power Module
- Filter Special Coefficients and Feed Forward
- DPWM synchronization
- Filter to DPWM

The following control modules are configured in the Loop Mux:

- Constant Power/Constant Current
- Cycle Adjustment (Current and flux balancing)
- Global Period
- Light Load (Burst Mode)

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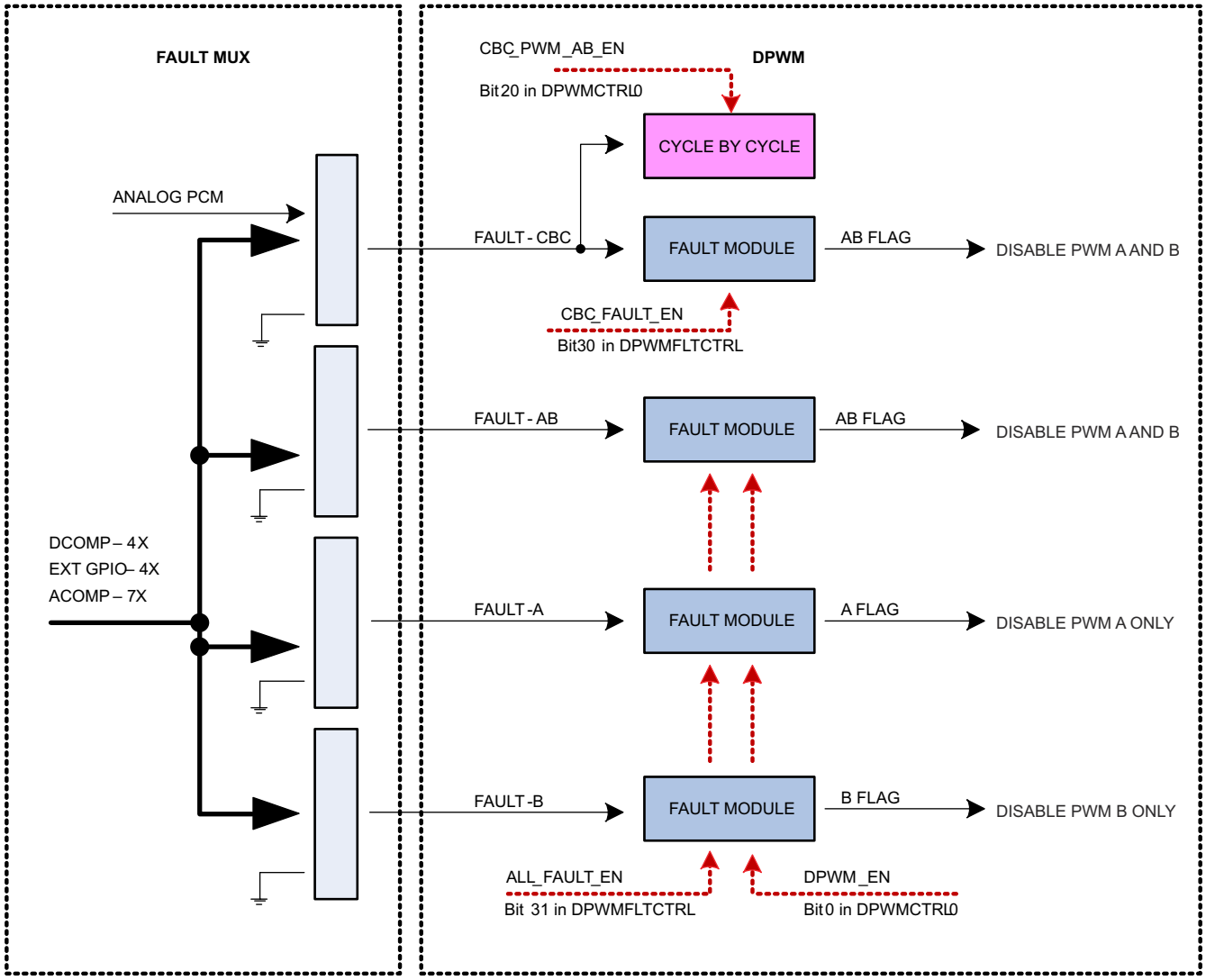
- Analog Peak Current Mode

9.5.4.2 Fault Multiplexer

In order to allow a flexible way of mapping several fault triggering sources to all the DPWMs channels, the UCD3138 provides an extensive array of multiplexers that are united under the name Fault Mux module.

The Fault Mux Module supports the following types of mapping between all the sources of fault and all different fault response mechanism inside each DPWM module.

- Many fault sources mapped to a single fault response mechanism. For instance an analog comparator in charge of over voltage protection, a digital comparator in charge of over current protection and an external digital fault pin can be all mapped to a fault-A signal connected to a single FAULT MODULE and shut down DPWM1-A.
- A single fault source can be mapped to many fault response mechanisms inside many DPWM modules. For instance an analog comparator in charge of over current protection can be mapped to DPWM-0 through DPWM-3 by way of several fault modules.
- Many fault sources can be mapped to many fault modules inside many DPWM modules.



The Fault Mux Module provides a multitude of fault protection functions within the UCD3138 high-speed loop (front end control, filter, DPWM and loop Mux modules). The Fault Mux Module allows highly configurable fault generation based on digital comparators, high-speed analog comparators and external fault pins. Each of the fault inputs to the DPWM modules can be configured to one or any combination of the fault events provided in the Fault Mux Module.

Each one of the DPWM engines has four fault modules. The modules are called CBC fault module, AB fault module, A fault module and B fault module.

The internal circuitry in all the four fault modules is identical, and the difference between the modules is limited to the way the modules are attached to the DPWMs.

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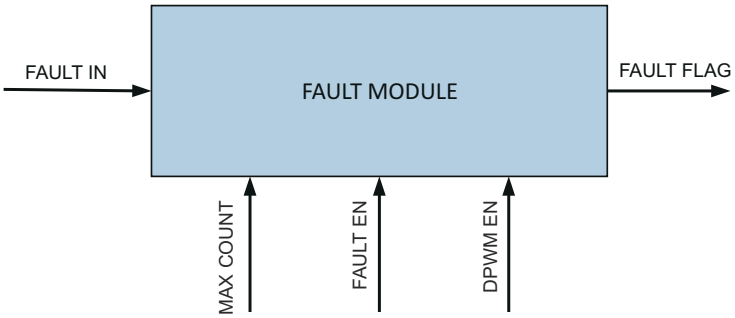

図 9-10. Fault Module

All fault modules provide immediate fault detection but only once per DPWM switching cycle. Each one of the fault modules own a separate max_count and the fault flag will be set only if sequential cycle-by-cycle faults count exceeds max_count.

Once the fault flag is set DPWMs need to be disabled by DPWM_EN going low in order to clear the fault flags.

Note

All four Fault Modules share the same DPWM_EN control, all fault flags (output of Fault Modules) will be cleared simultaneously.

All four Fault Modules share the same global FAULT_EN as well. Therefore a specific Fault Module cannot be enabled/ disabled separately.

図 9-11. Cycle by Cycle Block

Unlike fault modules, only one cycle by cycle block is available in each DPWM module.

The cycle by cycle block works in conjunction with CBC Fault Module and enables DPWM reaction to signals arriving from analog peak current mode (PCM) module.

The fault Mux module supports the following basic functions:

- 4 digital comparators using the EADC as a source with programmable thresholds and fault generation
- Configuration for 7 high-speed analog comparators with programmable thresholds and fault generation
- External GPIO detection control with programmable fault generation
- Configurable DPWM fault generation for DPWM current limit fault, DPWM overvoltage detection fault, DPWM A external fault, DPWM B external fault and DPWM IDE flag
- Clock failure detection for high and low frequency oscillator blocks
- Discontinuous conduction mode detection

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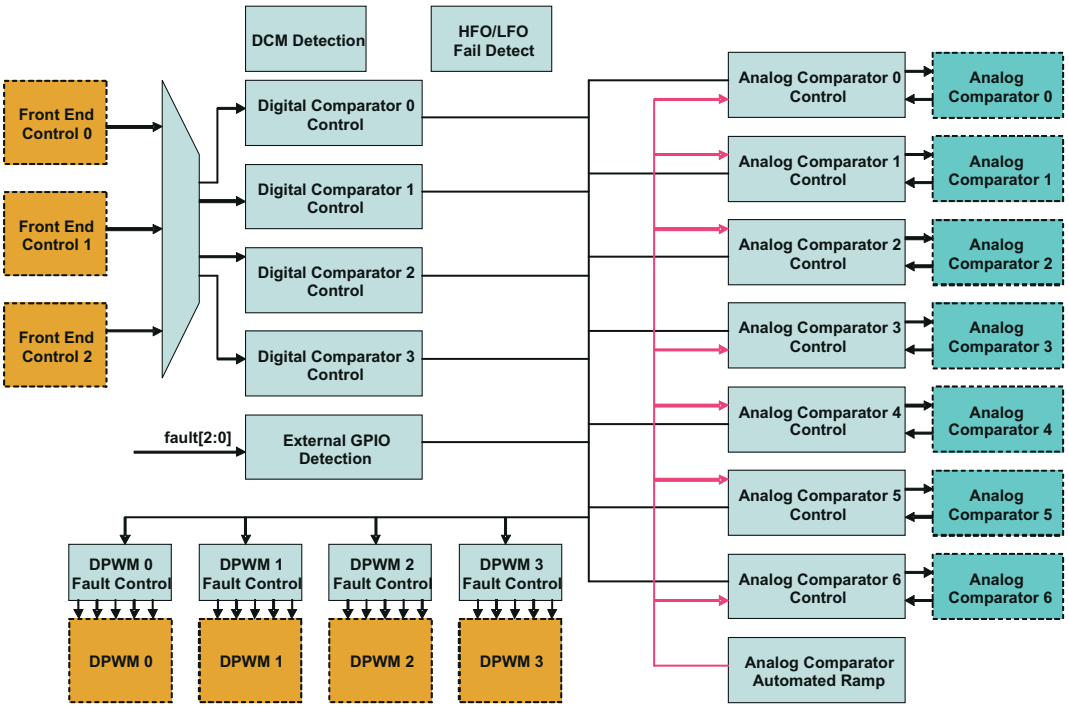

図 9-12. Fault Mux Block Diagram

9.5.5 Communication Ports

9.5.5.1 SCI (UART) Serial Communication Interface

A maximum of two independent Serial Communication Interface (SCI) or Universal Asynchronous Receiver/Transmitter pre-scaler (UART) interfaces are included within the device for asynchronous start-stop serial data communication (see the pin out sections for details) Each interface has a 24 bit for supporting programmable baud rates and has programmable data word and stop bit options. Half or full duplex operation is configurable through register bits. A loop back feature can also be setup for firmware verification. Both SCI-TX and SCI-RX pin sets can be used as GPIO pins when the peripheral is not being used.

9.5.5.2 PMBUS

The PMBus Interface supports independent master and slave modes controlled directly by firmware through a processor bus interface. Individual control and status registers enable firmware to send or receive I2C, SMBus or PMBus messages in any of the accepted protocols, in accordance with the I^2C Specification, SMBus Specification (Version 2.0) and the PMBUS Power System Management Protocol Specification.

The PMBus interface is controlled through a processor bus interface, utilizing a 32-bit data bus and 6-bit address bus. The PMBus interface is connected to the expansion bus, which features 4 byte write enables, a peripheral select dedicated for the PMBus interface, separated 32-bit data buses for reading and writing of data and active-low write and output enable control signals. In addition, the PMBus Interface connects directly to the I^2C/SMBus/PMBus Clock, Data, Alert, and Control signals.

Example: PMBus Address Decode via ADC12 Reading

The user can allocate 2 pins of the 12-bit ADC input channels, AD_00 and AD_01, for PMBus address decoding. At power-up the device applies I_{BIAS} to each address detect pin and the voltage on that pin is captured by the internal 12-bit ADC.

Where bin(V_{AD0x}) is the address bin for one of 12 address as shown in 図 9-13.

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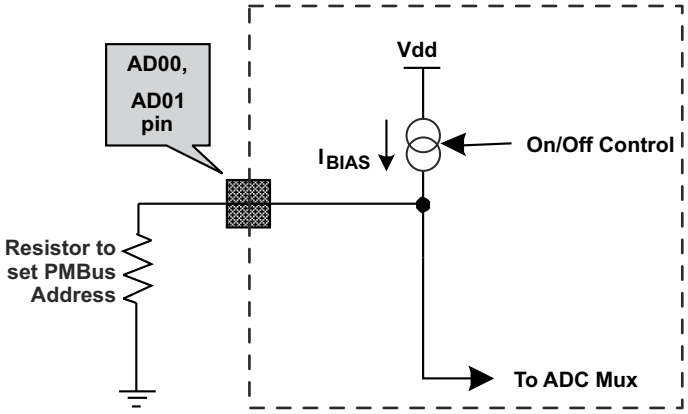

図 9-13. PMBus Address Detection Method

9.5.5.3 General Purpose ADC12

The ADC12 is a 12 bit, high speed analog to digital converter, equipped with the following options:

- Typical conversion speed of 267 ksps
- Conversions can consist from 1 to 16 ADC channel conversions in any desired sequence
- Post conversion averaging capability, ranging from 4X, 8X, 16X or 32X samples
- Configurable triggering for ADC conversions from the following sources: firmware, DPWM rising edge, ADC_EXT_TRIG pin or Analog Comparator results
- Interrupt capability to embedded processor at completion of ADC conversion
- Six digital comparators on the first 6 channels of the conversion sequence using either raw ADC data or averaged ADC data
- Two 10 µA current sources for excitation of PMBus addressing resistors
- Dual sample and hold for accurate power measurement
- Internal temperature sensor for temperature protection and monitoring

The control module *ADC12 Contol Block Diagram* contains the control and conversion logic for auto-sequencing a series of conversions. The sequencing is fully configurable for any combination of 16 possible ADC channels through an analog multiplexer embedded in the ADC12 block. Once converted, the selected channel value is stored in the result register associated with the sequence number. Input channels can be sampled in any desired order or programmed to repeat conversions on the same channel multiple times during a conversion sequence. Selected channel conversions are also stored in the result registers in order of conversion, where the result 0 register is the first conversion of a 16-channel sequence and result 15 register is the last conversion of a 16-channel sequence. The number of channels converted in a sequence can vary from 1 to 16.

Unlike EADC0 through EADC2, which are primarily designed for closing high speed compensation loops, the ADC12 is not usually used for loop compensation purposes. The EADC converters have a substantially faster conversion rate, thus making them more attractive for closed loop control. The ADC12 features make it best suited for monitoring and detection of currents, voltages, temperatures and faults. Please see the *Typical Characteristics* plots for the temperature variation associated with this function.

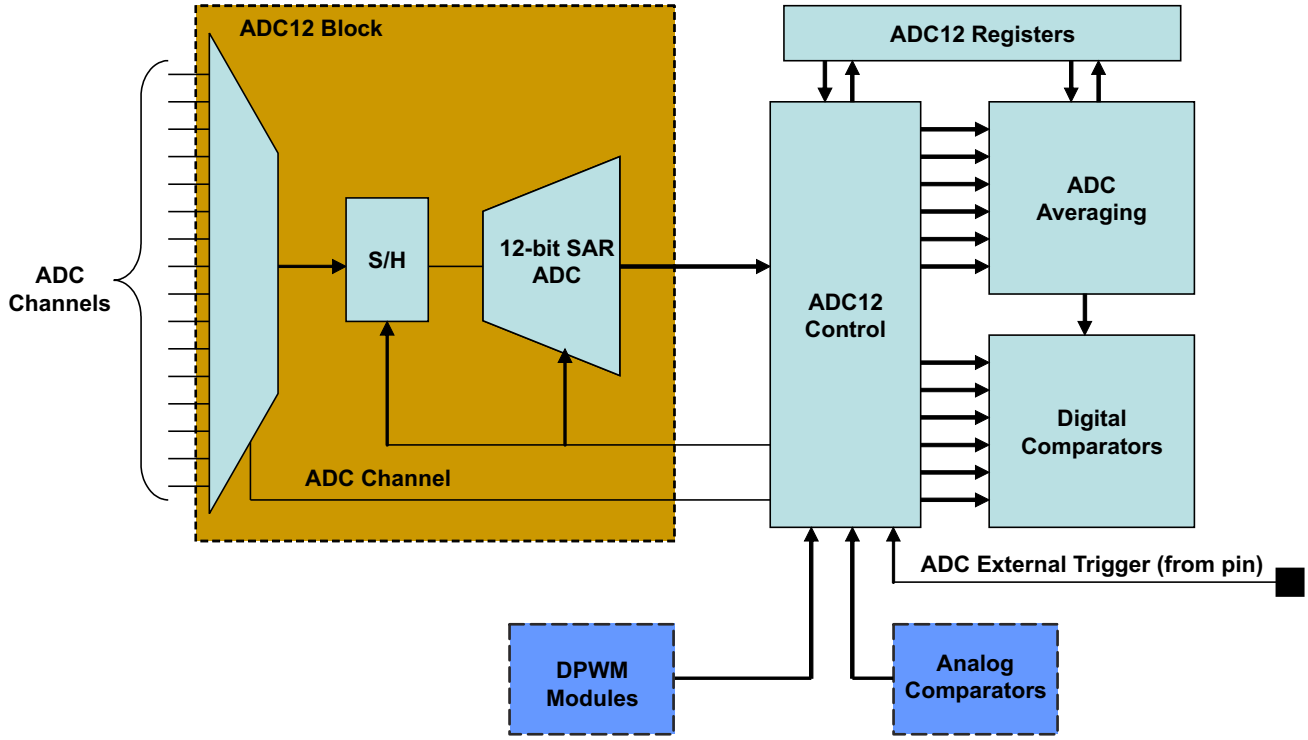

図 9-14. ADC12 Control Block Diagram

9.5.5.4 Timers

External to the Digital Power Peripherals there are 3 different types of timers in UCD3138. They are the 24-bit timer, 16-bit timer and the Watchdog timer

9.5.5.4.1 24-bit PWM Timer

There is one 24 bit counter PWM timer which runs off the Interface Clock and can further be divided down by an 8-bit pre-scalar to generate a slower PWM time period. The timer has two compare registers (Data Registers) for generating the PWM set/unset events. Additionally, the timer has a shadow register (Data Buffer register) which can be used to store CPU updates of the compare events while still using the timer. The selected shadow register update mode happens after the compare event matches.

The two capture pins TCMP0 and TCMP1 are inputs for recording a capture event. A capture event can be set either to rising, falling, or both edges of the capture pin. Upon this event, the counter value is stored in the corresponding capture data register.

The counter reset can be configured to happen on a counter roll over, a compare equal event, or by software controlled register. Five Interrupts from the PWM timer can be set, which are the counter rollover event (overflow), either capture event 0 or 1, or the two comparison match events. Each interrupt can be disabled or enabled.

Upon an event comparison on only the second event, the TCMP pin can be configured to set, clear, toggle or have no action at the output. The value of PWM pin output can be read for status or simply configured as general purpose I/O for reading the value of the input at the pin. The first compare event can only be used as an interrupt.

9.5.5.4.2 16-Bit PWM Timers

There are four 16 bit counter PWM timers which run off the Interface Clock and can further be divided down by a 8-bit pre-scaler to generate slower PWM time periods. Each timer has two compare registers (Data Registers) for generating the PWM set/unset events. Additionally, each timer has a shadow register (Data Buffer register) which can be used to store CPU updates of compare events while still using the timer. The selected shadow register update mode happens after the compare event matches.

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The counter reset can be configured to happen on a counter roll over, a compare equal event, or by a software controlled register. Interrupts from the PWM timer can be set due to the counter rollover event (overflow) or by the two comparison match events. Each comparison match and the overflow interrupts can be disabled or enabled.

Upon an event comparison, the PWM pin can be configured to set, clear, toggle or have no action at the output. The value of PWM pin output can be read for status or simply configured as General Purpose I/O for reading the value of the input at the pin.

9.5.5.4.3 Watchdog Timer

A watchdog timer is provided on the device for ensuring proper firmware loop execution. The timer is clocked off of a separate low speed oscillator source. If the timer is allowed to expire, a reset condition is issued to the ARM processor. The watchdog is reset by a simple CPU write bit to the watchdog key register by the firmware routine. On device power-up the watchdog is disabled. Yet after it is enabled, the watchdog cannot be disabled by firmware. Only a device reset can put this bit back to the default disabled state. A half timer flag is also provided for status monitoring of the watchdog.

9.5.6 Miscellaneous Analog

The Miscellaneous Analog Control (MAC) Registers are a catch-all of registers that control and monitor a wide variety of functions. These functions include device supervisory features such as Brown-Out and power saving configuration, general purpose input/output configuration and interfacing, internal temperature sensor control and current sharing control.

The MAC module also provides trim signals to the oscillator and AFE blocks. These controls are usually used at the time of trimming at manufacturing; therefore this document will not cover these trim controls.

The MAC registers and peripherals are all available in the UCD3138 (64 pin version). Other UCD3138 devices may have reduced resources. See the device pin out description for details.

9.5.7 Package ID Information

Package ID register includes information regarding the package type of the device and can be read by firmware for reporting through PMBus or for other package sensitive decisions.

BIT NUMBER	1:0
Bit Name	PKG_ID
Access	R/W
Default	0 – UCD3138RGC, 1 – UCD3138RHA

9.5.8 Brownout

Brownout function is used to determine if the device supply voltage is lower than a threshold voltage, a condition that may be considered unsafe for proper operation of the device.

The brownout threshold is higher than the reset threshold voltage; therefore, when the supply voltage is lower than brownout threshold, it still does not necessarily trigger a device reset.

The brownout interrupt flag can be polled or alternatively can trigger an interrupt to service such case by an interrupt service routine. Please see the *Power On Reset (POR) / Brown Out Reset (BOR)* section.

9.5.9 Global I/O

Up to 30 pins in UCD3138 can be configured to serve as a general purpose input or output pin (GPIO). This includes all digital input or output pins except for the RESET pin.

The pins that cannot be configured as GPIO pins are the supply pins, ground pins, ADC-12 analog input pins, EADC analog input pins and the RESET pin.

There are two ways to configure and use the digital pins as GPIO pins:

1. Through the centralized Global I/O control registers.

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2. Through the distributed control registers in the specific peripheral that shares it pins with the standard GPIO functionality.

The Global I/O registers offer full control of:

1. Configuring each pin as a GPIO.
2. Setting each pin as input or output.
3. Reading the pin's logic state, if it is configured as an input pin.
4. Setting the logic state of the pin, if it is configured as an output pin.
5. Configuring pin/pins as open drain or push-pull (Normal)

The Global I/O registers include Global I/O EN register, Global I/O OE Register, Global I/O Open Drain Control Register, Global I/O Value Register and Global I/O Read Register.

The following is showing the format of Global I/O EN Register (GLBIOEN) as an example:

BIT NUMBER	**29:0**
Bit Name	GLOBAL_IO_EN
Access	R/W
Default	00_0000_0000_0000_0000_0000_0000_0000

Bits 29-0: GLOBAL_IO_EN – This register enables the global control of digital I/O pins
0 = Control of IO is done by the functional block assigned to the IO (Default)
1 = Control of IO is done by Global IO registers.

BIT	**PIN_NAME**	**PIN NUMBER**	
		UCD3138-64 PIN	**UCD3138-40 PIN**
29	FAULT[3]	43	NA
28	ADC_EXT_TRIG	12, 26	8
27	TCK	37	21
26	TDO	38	20
25	TMS	40	24
24	TDI	39	23
23	SCI_TX[1]	29	NA
22	SCI_TX[0]	14	22
21	SCI_RX[1]	30	NA
20	SCI_RX[0]	13	23
19	TMR_CAP	12, 26, 41	8, 21
18	TMR_PWM[1]	32	NA
17	TMR_PWM[0]	12, 26, 31, 37	21
16	PMBUS-CLK	15	9
15	PMBUS-DATA	16	10
14	CONTROL	30	20
13	ALERT	29	19
12	EXT_INT	26, 34	NA
11	FAULT[2]	42	25
10	FAULT[1]	36	23
9	FAULT[0]	35, 39	22
8	SYNC	12, 26,37	8, 21
7	DPWM3B	24	18
6	DPWM3A	23	17
5	DPWM2B	22	16

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BIT	PIN_NAME	PIN NUMBER	
		UCD3138-64 PIN	UCD3138-40 PIN
4	DPWM2A	21	15
3	DPWM1B	20	14
2	DPWM1A	19	13
1	DPWM0B	18	12
0	DPWM0A	17	11

9.5.10 Temperature Sensor Control

Temperature sensor control register provides internal temperature sensor enabling and trimming capabilities. The internal temperature sensor is disabled as default.

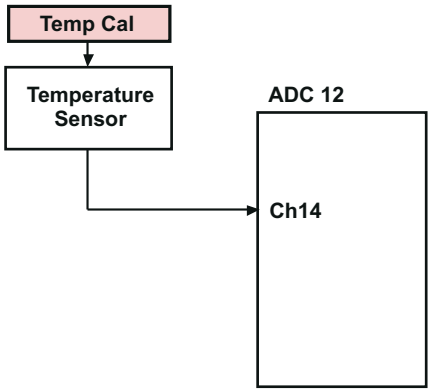

図 9-15. Internal Temp Sensor

Temperature sensor is calibrated at room temperature (25 °C) via a calibration register value.

The temperature sensor is measured using ADC12 (via Ch14). The temperature is then calculated using a mathematical formula involving the calibration register (this effectively adds a delta to the ADC measurement).

The temperature sensor can be enabled or disabled.

9.5.11 I/O Mux Control

In different packages of UCD3138 several I/O functions are multiplexed and routed toward a single physical pin. I/O Mux Control register may be used in order to choose a single specific functionality that is desired to be assigned to a physical device pin for your application.

9.5.12 Current Sharing Control

UCD3138 provides three separate modes of current sharing operation.

- Analog bus current sharing
- PWM bus current sharing
- Master/Slave current sharing
- AD02 has a special ESD protection mechanism that prevents the pin from pulling down the current-share bus if power is missing from the UCD3138

The simplified current sharing circuitry is shown in the drawing below:

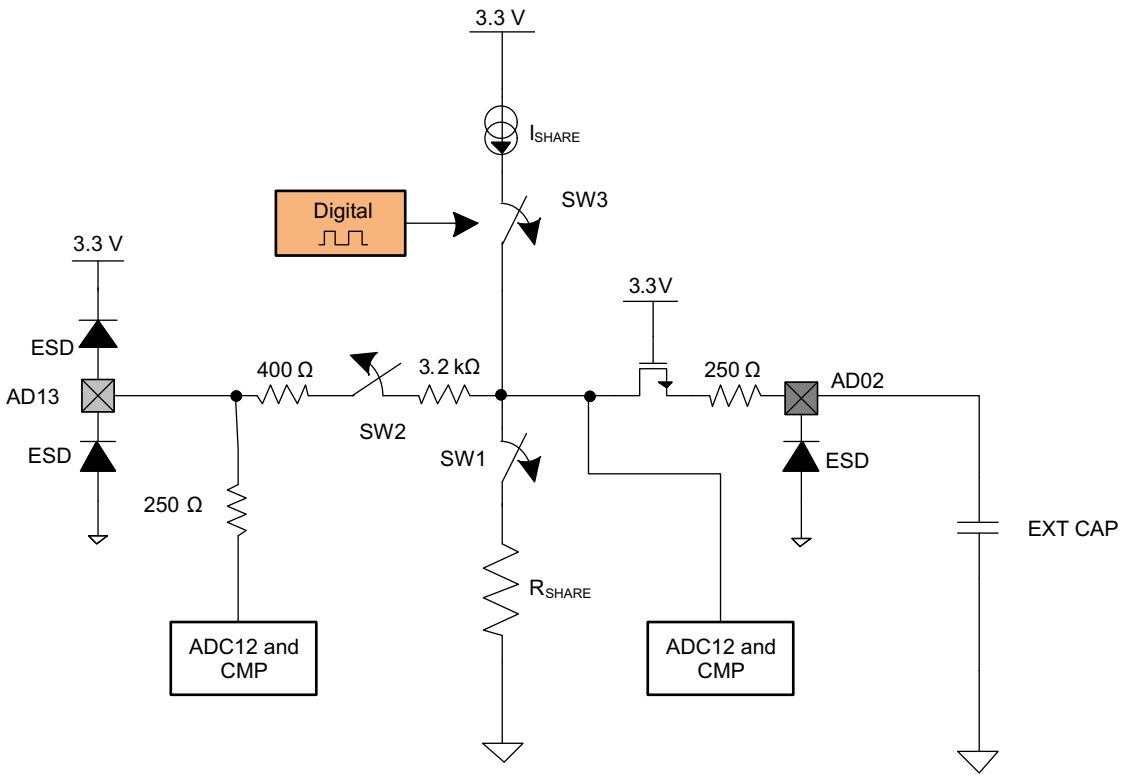

図 9-16. Simplified Current Sharing Circuitry

CURRENT SHARING MODE	FOR TEST ONLY, ALWAYS KEEP 00	CS_MODE	EN_SW1	EN_SW2	DPWM
Off or Slave Mode (3-state)	00	00 (default)	0	0	0
PWM Bus	00	01	1	0	ACTIVE
Off or Slave Mode (3-state)	00	10	0	0	0
Analog Bus or Master	00	11	0	1	0

The period and the duty of 8-bit PWM current source and the state of the SW1 and SW2 switches can be controlled through the current sharing control register (CSCTRL).

9.5.13 Temperature Reference

The temperature reference register (TEMPREF) provides the ADC12 count when ADC12 measures the internal temperature sensor (channel 14) during the factory trim and calibration.

This information can be used by different periodic temperature compensation routines implemented in the firmware. But it should not be overwritten by firmware, otherwise this factory written value will be lost.

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9.6 Device Functional Modes

The DPWM is a complex logic system which is highly configurable to support several different power supply topologies. The discussion below will focus primarily on waveforms, timing and register settings, rather than on logic design.

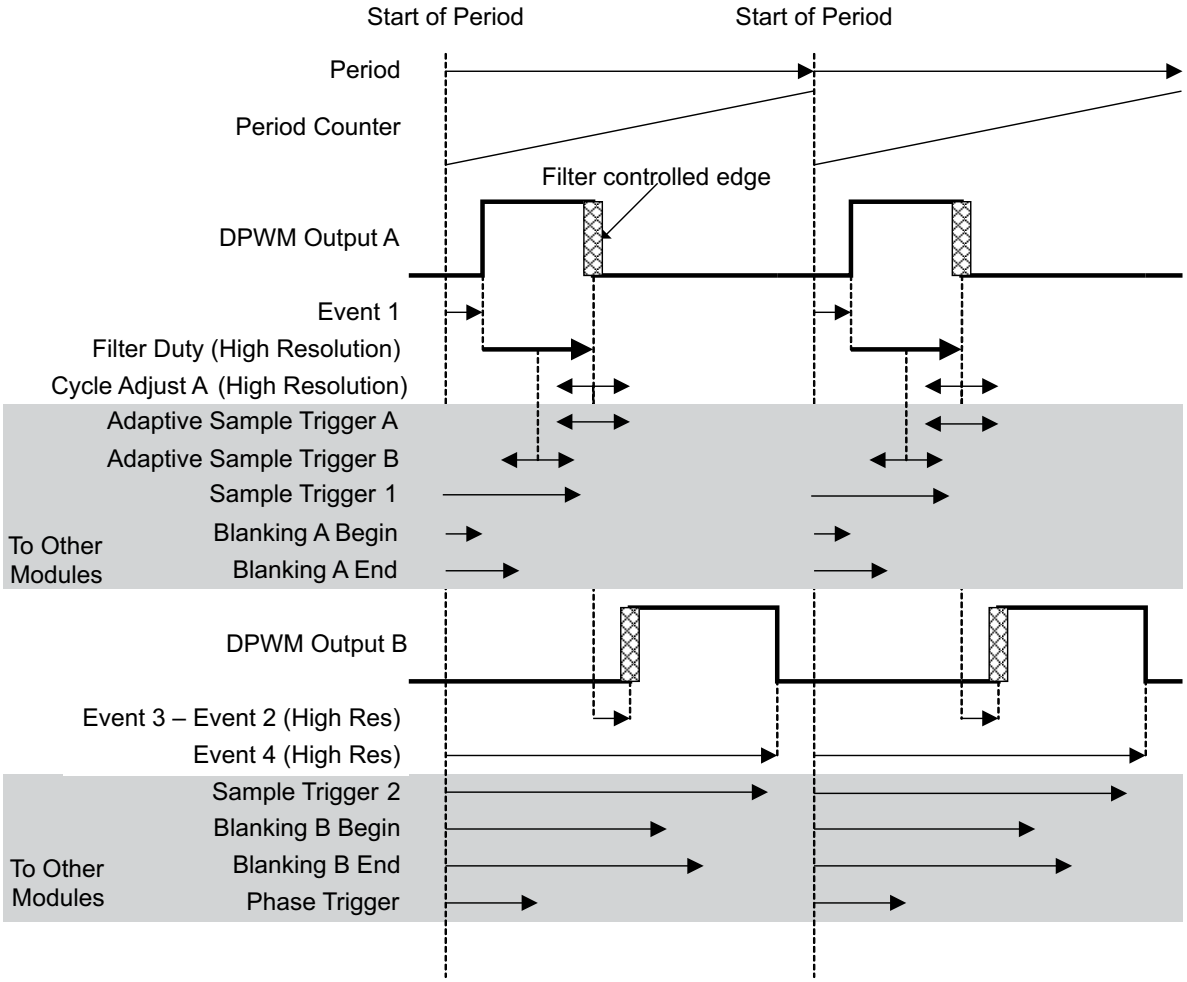
The DPWM is centered on a period counter, which counts up from 0 to PRD, and then is reset and starts over again.

The DPWM logic causes transitions in many digital signals when the period counter hits the target value for that signal.

9.6.1 Normal Mode

In Normal mode, the Filter output determines the pulse width on DPWM A. DPWM B fits into the rest of the switching period, with a dead time separating it from the DPWM A on-time. It is useful for buck topologies, among others. Here is a drawing of the Normal Mode waveforms:

Normal Mode Closed Loop



Events which change with DPWM mode:

DPWM A Rising Edge = Event 1
DPWM A Falling Edge = Event 1 + Filter Duty + Cycle Adjust A
Adaptive Sample Trigger A = Event 1 + Filter Duty + Adaptive Sample Register or
Adaptive Sample Trigger B = Event 1 + Filter Duty/2 + Adaptive Sample Register
DPWM B Rising Edge = Event 1 + Filter Duty + Cycle Adjust A + (Event 3 – Event 2)
DPWM B Falling Edge = Event 4
Phase Trigger = Phase Trigger Register value or Filter Duty

Events always set by their registers, regardless of mode:

Sample Trigger 1, Sample Trigger 2, Blanking A Begin, Blanking A End, Blanking B Begin, Blanking B End

図 9-17. Normal Mode Closed Loop

Cycle adjust A can be used to adjust pulse widths on individual phases of a multi-phase system. This can be used for functions like current balancing. The Adaptive Sample Triggers can be used to sample in the middle of the on-time (for an average output), or at the end of the on-time (to minimize phase delay) The Adaptive Sample Register provides an offset from the center of the on-time. This can compensate for external delays, such as MOSFET and gate driver turn on times.

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Blanking A-Begin and Blanking A-End can be used to blank out noise from the MOSFET turn on at the beginning of the period (DPWMA rising edge). Blanking B could be used at the turn off time of DPWMB. The other edges are dynamic, so blanking is more difficult.

Cycle Adjust B has no effect in Normal Mode.

9.6.2 Phase Shifting

In most modes, it is possible to synchronize multiple DPWM modules using the phase shift signal. The phase shift signal has two possible sources. It can come from the Phase Shift register. This provides a fixed value, which is useful for an interleaved PFC, for example.

The phase shift value can also come from the filter output. In this case, the changes in the filter output causes changes in the phase relationship of two DPWM modules. This is useful for phase shifted full bridge topologies.

The following figure shows the mechanism of phase shift:

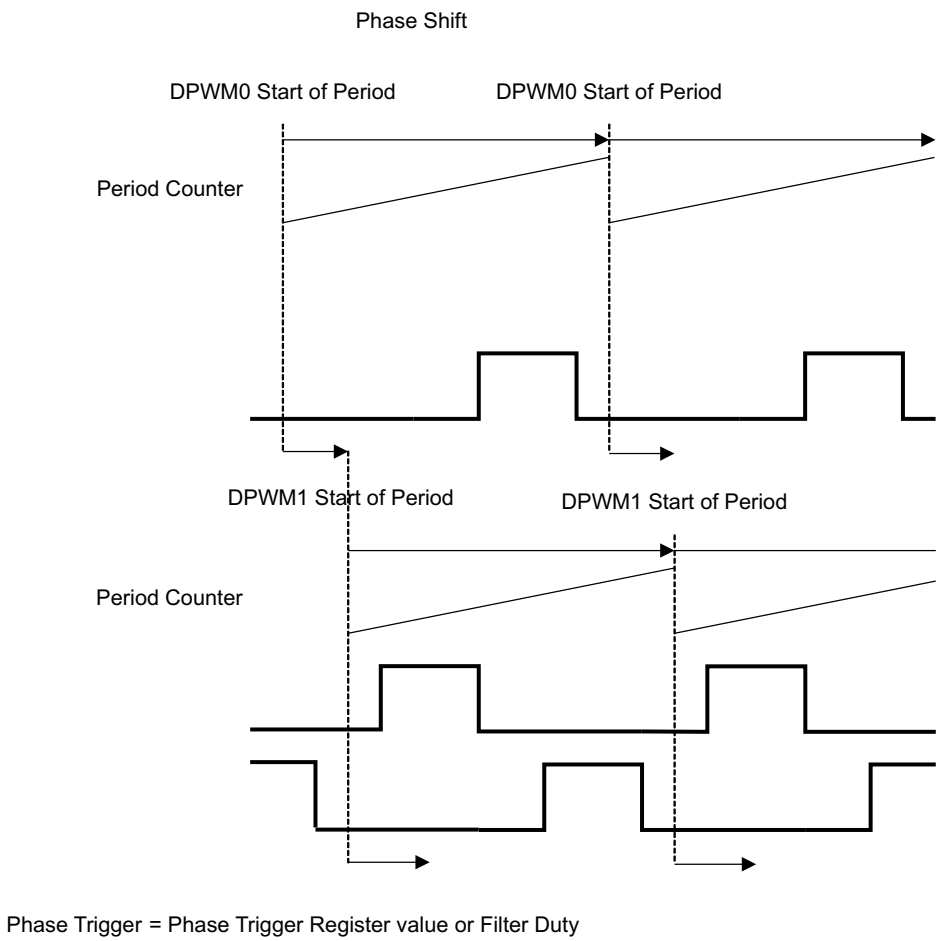
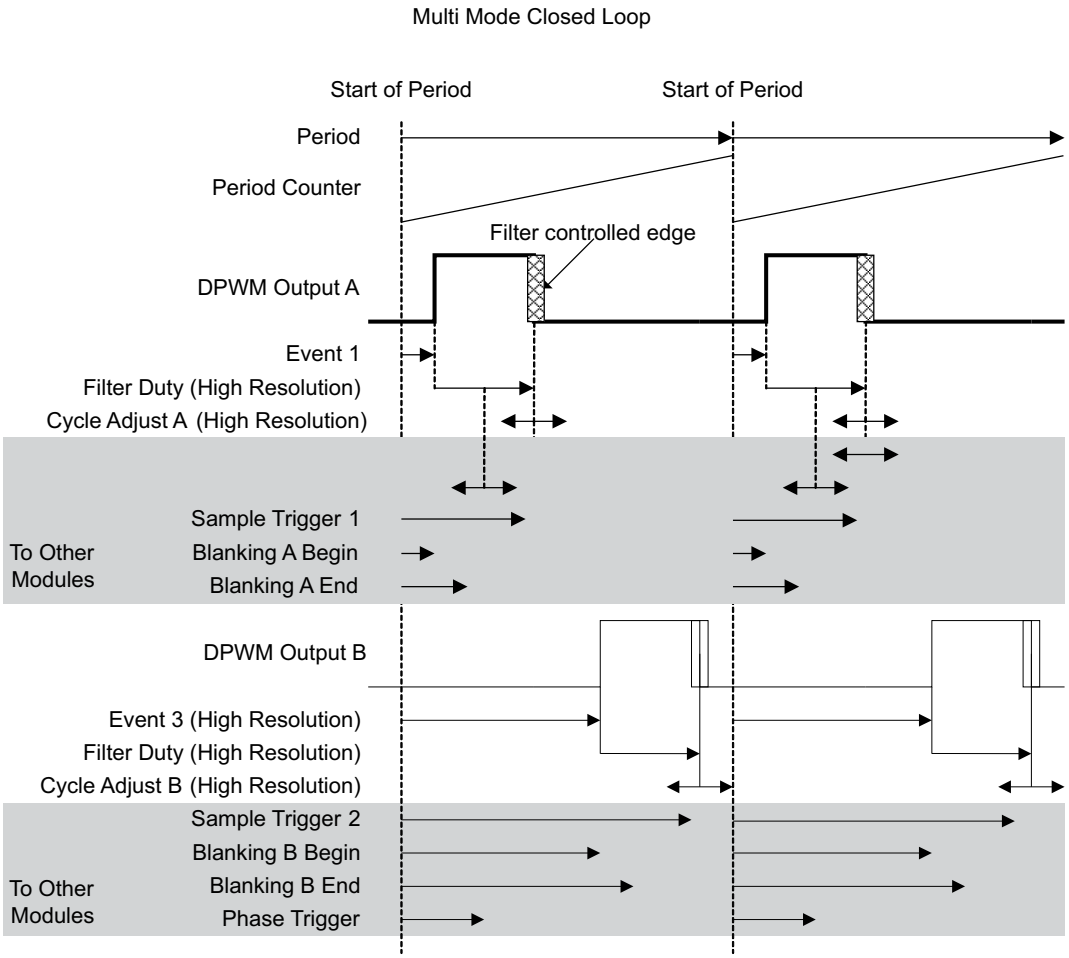


図 9-18. Phase Shift

9.6.3 DPWM Multiple Output Mode

Multi mode is used for systems where each phase has only one driver signal. It enables each DPWM peripheral to drive two phases with the same pulse width, but with a time offset between the phases, and with different cycle adjusts for each phase.

Here is a diagram for Multi-Mode:



Events which change with DPWM mode:

DPWM A Rising Edge = Event 1
DPWM A Falling Edge = Event 1 + Filter Duty + Cycle Adjust A
Adaptive Sample Trigger A = Event 1 + Filter Duty + Adaptive Sample Register or
Adaptive Sample Trigger B = Event 1 + Filter Duty/2 + Adaptive Sample Register
DPWM B Rising Edge = Event 3
DPWM B Falling Edge = Event 3 + Filter Duty + Cycle Adjust B
Phase Trigger = Phase Trigger Register value or Filter Duty

Events always set by their registers, regardless of mode:

Sample Trigger 1, Sample Trigger 2, Blanking A Begin, Blanking A End, Blanking B Begin, Blanking B End

図 9-19. Multi Mode Closed Loop

Event 2 and Event 4 are not relevant in Multi mode.

DPWMB can cross over the period boundary safely, and still have the proper pulse width, so full 100% pulse width operation is possible. DPWMA cannot cross over the period boundary.

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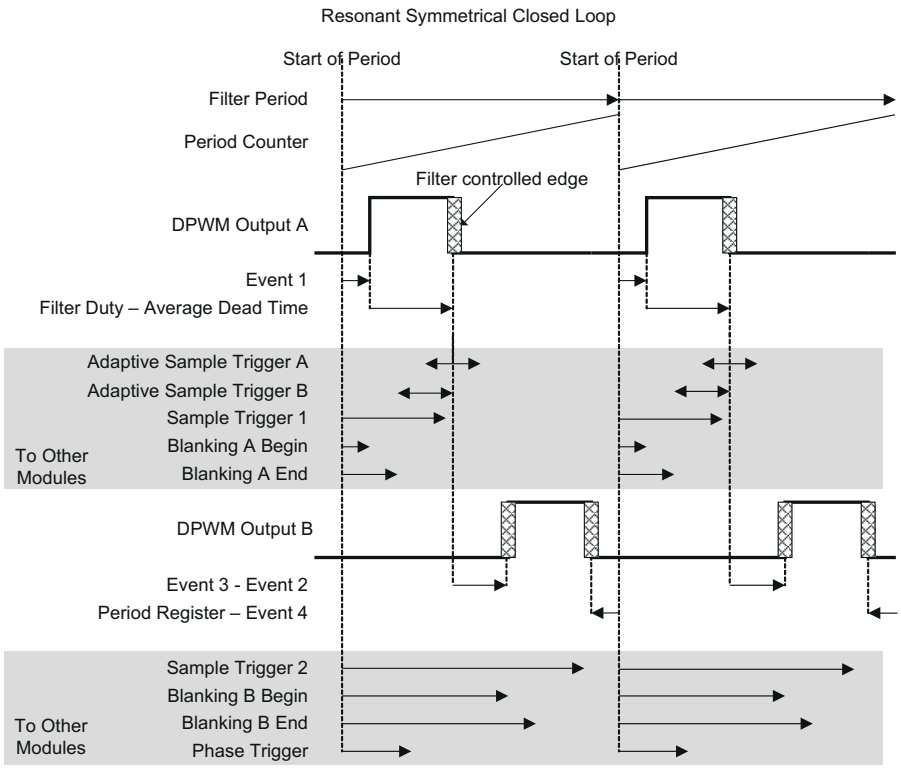
Since the rising edge on DPWM B is also fixed, Blanking B-Begin and Blanking B-End can be used for blanking this rising edge.

And, of course, Cycle Adjust B is usable on DPWM B.

9.6.4 DPWM Resonant Mode

This mode provides a symmetrical waveform where DPWMA and DPWMB have the same pulse width. As the switching frequency changes, the dead times between the pulses remain the same.

The equations for this mode are designed for a smooth transition from PWM mode to resonant mode, as described in *セクション 9.5.2.2*. Here is a diagram of this mode:



Events which change with DPWM mode:

Dead Time 1 = Event 3 – Event 2
Dead Time 2 = Event 1 + Period Register – Event 4)
Average Dead Time = (Dead Time 1 + Dead Time 2)/2

DPWM A Rising Edge = Event 1
DPWM A Falling Edge = Event 1 + Filter Duty – Average Dead Time
Adaptive Sample Trigger A = Event 1 + Filter Duty + Adaptive Sample Register
Adaptive Sample Trigger B = Event 1 + Filter Duty/2 + Adaptive Sample Register
DPWM B Rising Edge = Event 1 + Filter Duty – Average Dead Time + (Event 3 – Event 2)
DPWM B Falling Edge = Filter Period – (Period Register – Event 4)
Phase Trigger = Phase Trigger Register value or Filter Duty

Events always set by their registers, regardless of mode:

Sample Trigger 1, Sample Trigger 2, Blanking A Begin, Blanking A End, Blanking B Begin, Blanking B End

図 9-20. Resonant Symmetrical Closed Loop

The Filter has two outputs, Filter Duty and Filter Period. In this case, the Filter is configured so that the Filter Period is twice the Filter Duty. So if there were no dead times, each DPWM pin would be on for half of the period. For dead time handling, the average of the two dead times is subtracted from the Filter Duty for both DPWM pins. Therefore, both pins will have the same on-time, and the dead times will be fixed regardless of the period. The only edge which is fixed relative to the start of the period is the rising edge of DPWM A. This is the only edge for which the blanking signals can be used easily.

9.6.5 Triangular Mode

Triangular mode provides a stable phase shift in interleaved PFC and similar topologies. In this case, the PWM pulse is centered in the middle of the period, rather than starting at one end or the other. In Triangular Mode, only DPWM-B is available. Here is a diagram for Triangular Mode:

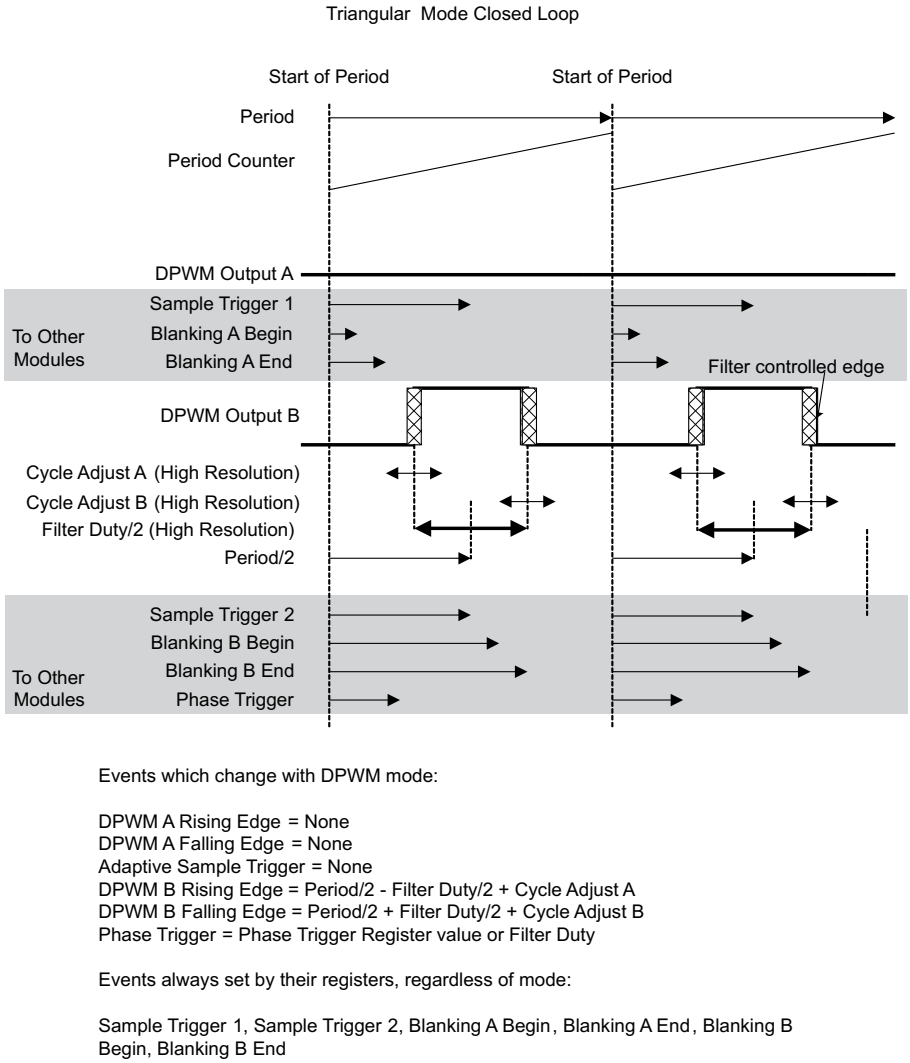


図 9-21. Triangular Mode Closed Loop

All edges are dynamic in triangular mode, so fixed blanking is not that useful. The adaptive sample trigger is not needed. It is very easy to put a fixed sample trigger exactly in the center of the FET on-time, because the center of the on-time does not move in this mode.

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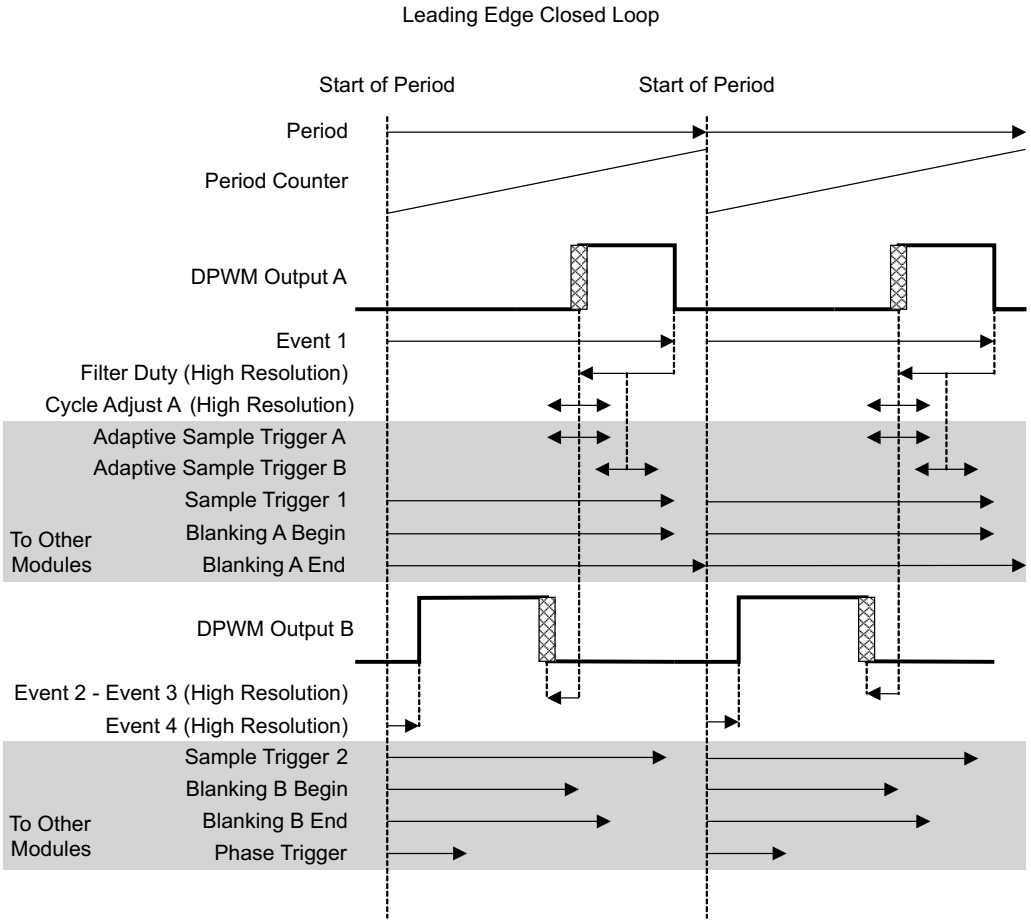
9.6.6 Leading Edge Mode

Leading edge mode is very similar to Normal mode, reversed in time. The DPWM A falling edge is fixed, and the rising edge moves to the left, or backwards in time, as the filter output increases. The DPWM B falling edge stays ahead of the DPWMA rising edge by a fixed dead time. Here is a diagram of the Leading Edge Mode:



Events which change with DPWM mode:

DPWM A Falling Edge = Event 1
DPWM A Rising Edge = Event 1 - Filter Duty + Cycle Adjust A
Adaptive Sample Trigger A = Event 1 - Filter Duty + Adaptive Sample Register or
Adaptive Sample Trigger B = Event 1 - Filter Duty/2 + Adaptive Sample Register
DPWM B Rising Edge = Event 4
DPWM B Falling Edge = Event 1 - Filter Duty + Cycle Adjust A -(Event 2 – Event 3)
Phase Trigger = Phase Trigger Register value or Filter Duty

Events always set by their registers, regardless of mode:

Sample Trigger 1, Sample Trigger 2, Blanking A Begin, Blanking A End, Blanking B Begin, Blanking B End

図 9-22. Leading Edge Closed Loop

As in the Normal mode, the two edges in the middle of the period are dynamic, so the fixed blanking intervals are mainly useful for the edges at the beginning and end of the period.

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

The UCD3138x has an extensive set of fully-programmable, high-performance peripherals that make it suitable for a wide range of power supply applications. In order to make the part easier to use, TI has prepared an extensive set of materials to demonstrate the features of the device for several key applications. In each case the following items are available:

1. Full featured EVM hardware that demonstrates classic power supply functionality.
2. An EVM user guide that contains schematics, bill-of-materials, layout guidance and test data showcasing the performance and features of the device and the hardware.
3. A firmware programmers manual that provides a step-by-step walk through of the code.

表 10-1. Application Information

APPLICATION	EVM DESCRIPTION
Phase shifted full bridge	This EVM demonstrates a PSFB DC-DC power converter with digital control using the UCD3138x device. Control is implemented by using PCMC with slope compensation. This simplifies the hardware design by eliminating the need for a series blocking capacitors and providing the inherent input voltage feed-forward that comes from PCMC. The controller is located on a daughter card and requires firmware in order to operate. This firmware, along with the entire source code, is made available through TI. A free, custom function GUI is available to help the user experiment with the different hardware and software enabled features. The EVM accepts a DC input from 350 VDC to 400 VDC, and outputs a nominal 12 VDC with full load output power of 360 W, or full output current of 30 A.
LLC resonant converter	This EVM demonstrates an LLC resonant half-bridge DC-DC power converter with digital control using the UCD3138x device. The controller is located on a daughter card and requires firmware in order to operate. This firmware, along with the entire source code, is made available through TI. A free, custom function GUI is available to help the user experiment with the different hardware and software enabled features. The EVM accepts a DC input from 350 VDC to 400 VDC, and outputs a nominal 12 VDC with full load output power of 340 W, or full output current of 29 A.

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10.2 Typical Application

This section summarizes the PSFB EVM DC-DC power converter.

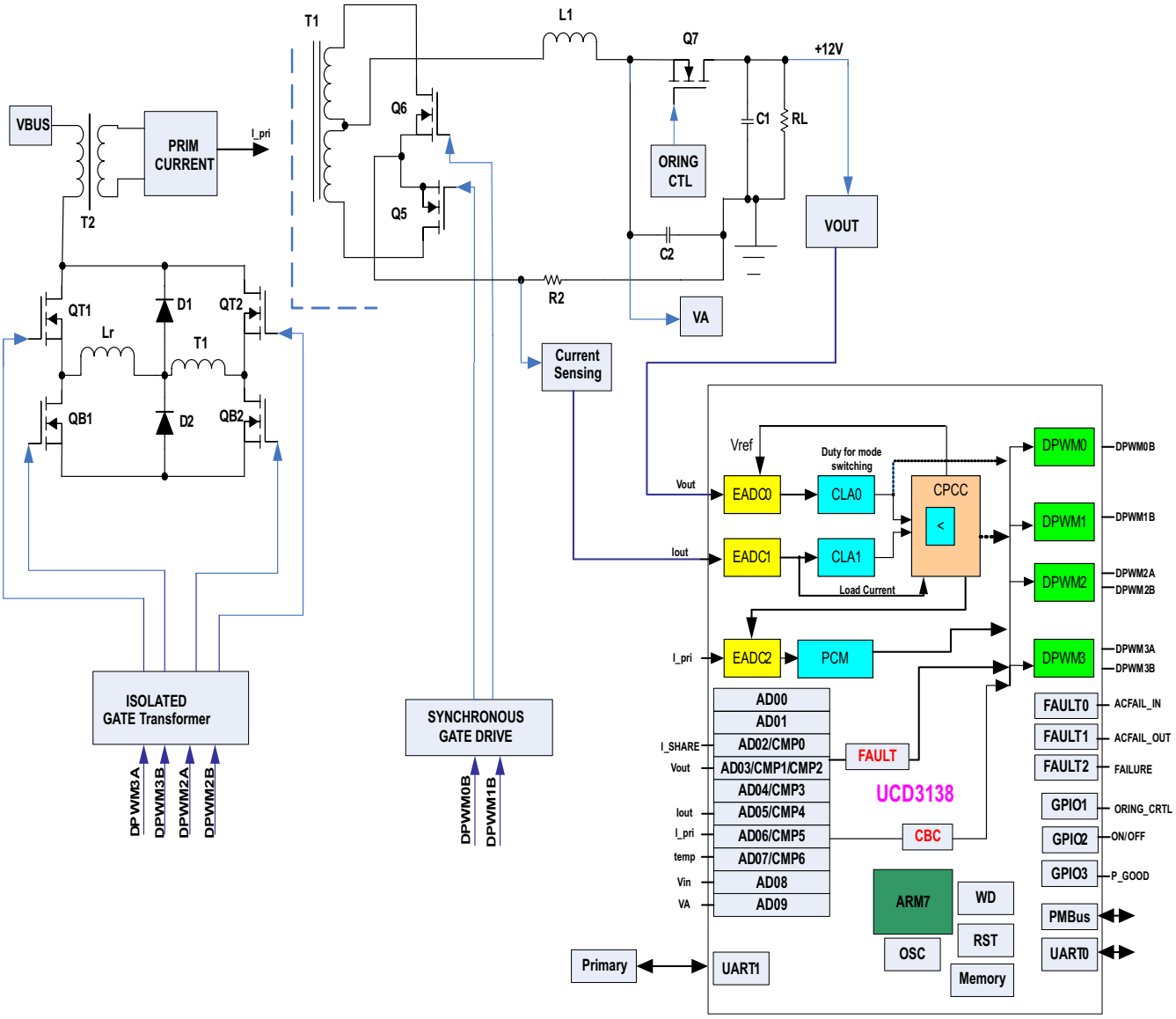

図 10-1. Phase-Shifted Full-Bridge

10.2.1 Design Requirements

表 10-2. Input Characteristics

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
ALL SPECIFICATIONS at Vin=400V and 25°C AMBIENT UNLESS OTHERWISE NOTED.						
V_{in}	Input voltage range	Normal Operating	350	385	420	V
V_{inmax}	Max input voltage	Continuous			420	V
I_{in}	Input current	Vin=350V, Full Load		1.15		A
I_{stby}	Input no load current	Output current is 0A		30		mA
V_{on}	Under voltage lockout	V_{in} Decreasing (input voltage is detected on secondary side)		340		V
V_{hys}		V_{in} Increasing		360		V

表 10-3. Output Characteristics

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
ALL SPECIFICATIONS at Vin=400V and 25°C AMBIENT UNLESS OTHERWISE NOTED.						
V_O	Output voltage setpoint	No load on outputs		12		V
Reg_{line}	Line regulation	All outputs; $360 \le V_{in} \le 420$; $I_O = I_{Omax}$			0.5	%
Reg_{load}	Load regulation	All outputs; $0 \le I_O \le I_{Omax}$; V_{in} = 400 V			1	%
V_n	Ripple and noise(1)	5Hz to 20 MHz		100		mVpp
I_O	Output current		0		30	A
η	Efficiency at phase-shift mode	Vo = 12 V, Io = 15 A		93%		
η	Efficiency at PWM ZVS mode	Vo = 12 V, Io = 15 A		93%		
η	Efficiency at hard switching mode	Vo = 12 V, Io = 15 A		90%		
V_{adj}	Output adjust range		11.4		12.6	V
V_{tr}	Transient response overshoot/ undershoot	50% Load Step at 1AμS, min load at 2A		±0.36		V
$t_{settling}$	Transient response settling time			100		μS
t_{start}	Output rise time	10% to 90% of Vout		50		mS
	Overshoot	At Startup			2	%
fs	Switching frequency	Over V_{in} and I_O ranges		150		kHz
I_{share}	Current sharing accuracy	50% - full load		±5		%
φ	Loop phase margin	10% - Full load		45		degree
G	Loop gain margin	10% - Full load		10		dB

(1) Ripple and noise are measured with 10μF Tantalum capacitor and 0.1μF ceramic capacitor across output.

10.2.2 Detailed Design Procedure

10.2.2.1 PCMC (Peak Current Mode Control) PSFB (Phase Shifted Full Bridge) Hardware Configuration Overview

The hardware configuration of the UCD3138x PCMC PSFB converter contains two critical elements that are highlighted in the subsequent sections.

- DPWM initialization - This section will highlight the key register settings and considerations necessary for the UCD3138x to generate the correct MOSFET waveforms for this topology. This maintains the proper phase relationship between the MOSFETs and synchronous rectifiers as well as the proper set up required to function correctly with PCMC.
- PCMC initialization - This section will discuss the register settings and hardware considerations necessary to modulate the DPWM pins with PCMC and internal slope compensation.

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10.2.2.2 DPWM Initialization for PSFB

The UCD3138x DPWM peripheral provides flexibility for a wide range of topologies. The PSFB configuration utilizes the Intra-Mux and Edge Generation Modules of the DPWM. For a diagram showing these modules, see the UCD3138x Digital Power Peripherals Manual.

Here is a schematic of the power stage of the PSFB:

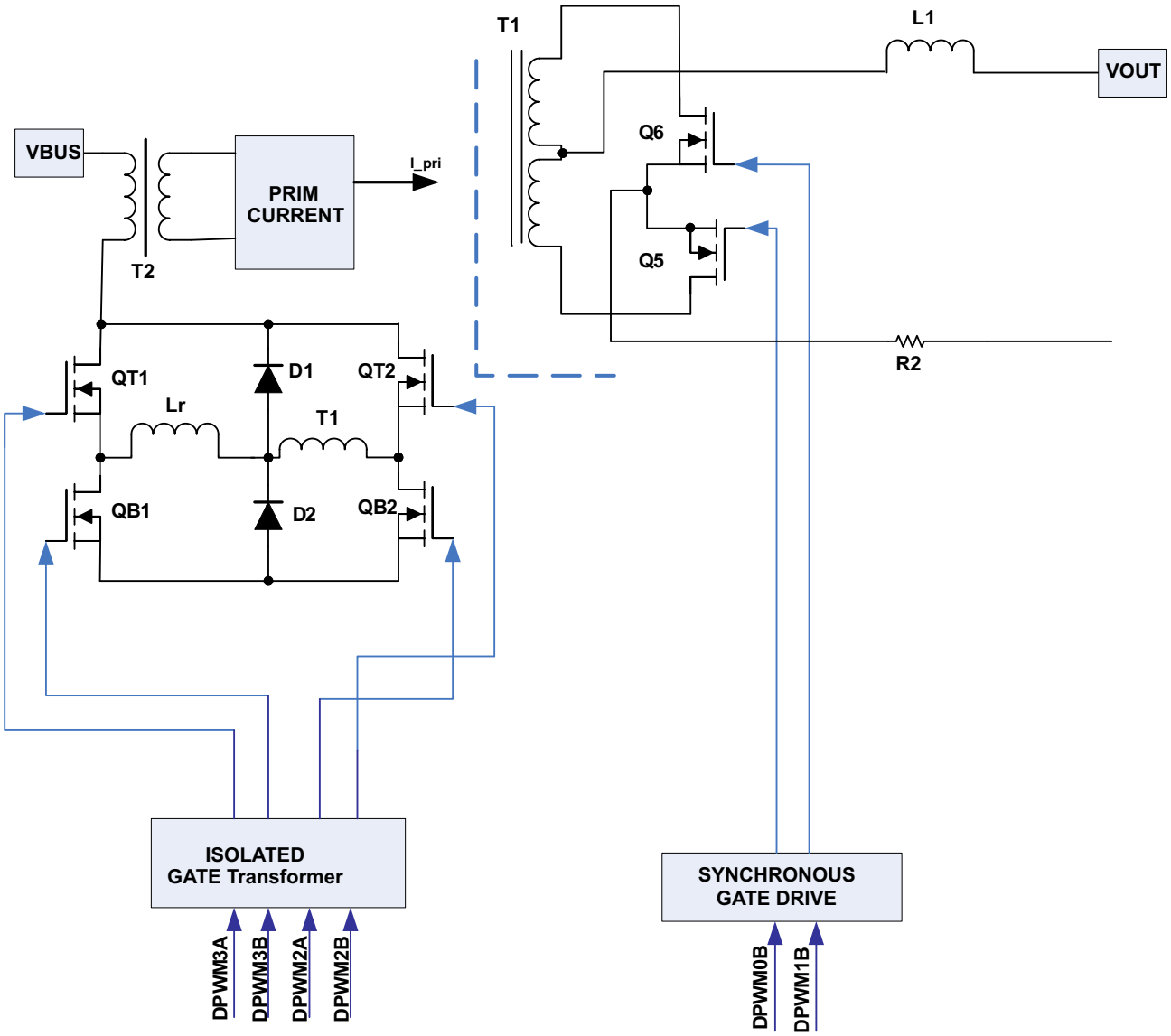
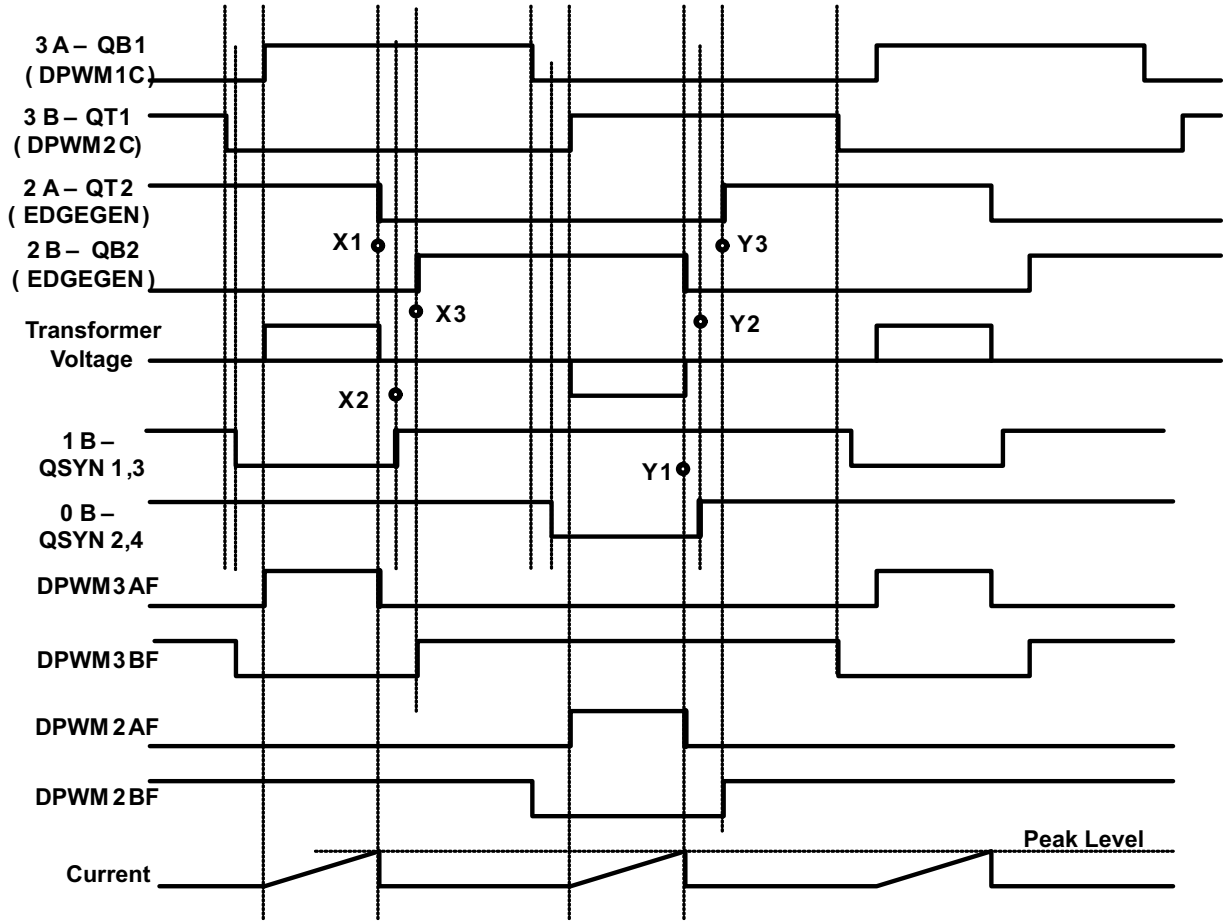


図 10-2. Schematic – PSFB Power Stage

Here is an overview of the key PSFB signals:



X1, X2, X3 and Y1, Y2, Y3 are sets of moving edges
All other edges are fixed .

図 10-3. Key PSFB Signals

10.2.2.3 DPWM Synchronization

DPWM1 is synchronized to DPWM0, DPWM2 is synchronized to DPWM1, and DPWM3 is synchronized to DPWM2, ½ period out of phase using these commands:

```
Dpwm1Regs.DPWMCTRL0.bit.MSYNC_SLAVE_EN = 1; //configured to slave
Dpwm2Regs.DPWMCTRL0.bit.MSYNC_SLAVE_EN = 1; // configured to slave
Dpwm3Regs.DPWMCTRL0.bit.MSYNC_SLAVE_EN = 1; // configured to slave

Dpwm0Regs.DPWMPHASETRIG.all = PWM_SLAVESYNC;
Dpwm1Regs.DPWMPHASETRIG.all = PWM_SLAVESYNC;
Dpwm2Regs.DPWMPHASETRIG.all = PWM_SLAVESYNC;

LoopMuxRegs.DPWMMUX.bit.DPWM1_SYNC_SEL = 0;          // Slave to dpwm-0
LoopMuxRegs.DPWMMUX.bit.DPWM2_SYNC_SEL = 1;          // Slave to dpwm-1
LoopMuxRegs.DPWMMUX.bit.DPWM3_SYNC_SEL = 2;          // Slave to dpwm-2
```

If the event registers on the DPWMs are the same, the two pairs of signals will be symmetrical. All code examples are taken from the PSFB EVM code, unless otherwise stated.

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10.2.2.4 Fixed Signals to Bridge

The two top signals in the above drawing have fixed timing. The DPWM1CF and DPWM2CF signals are used for these pins. DPWMCxF refers to the signal coming out of the fault module of DPWMx, as shown in 図 10-4.

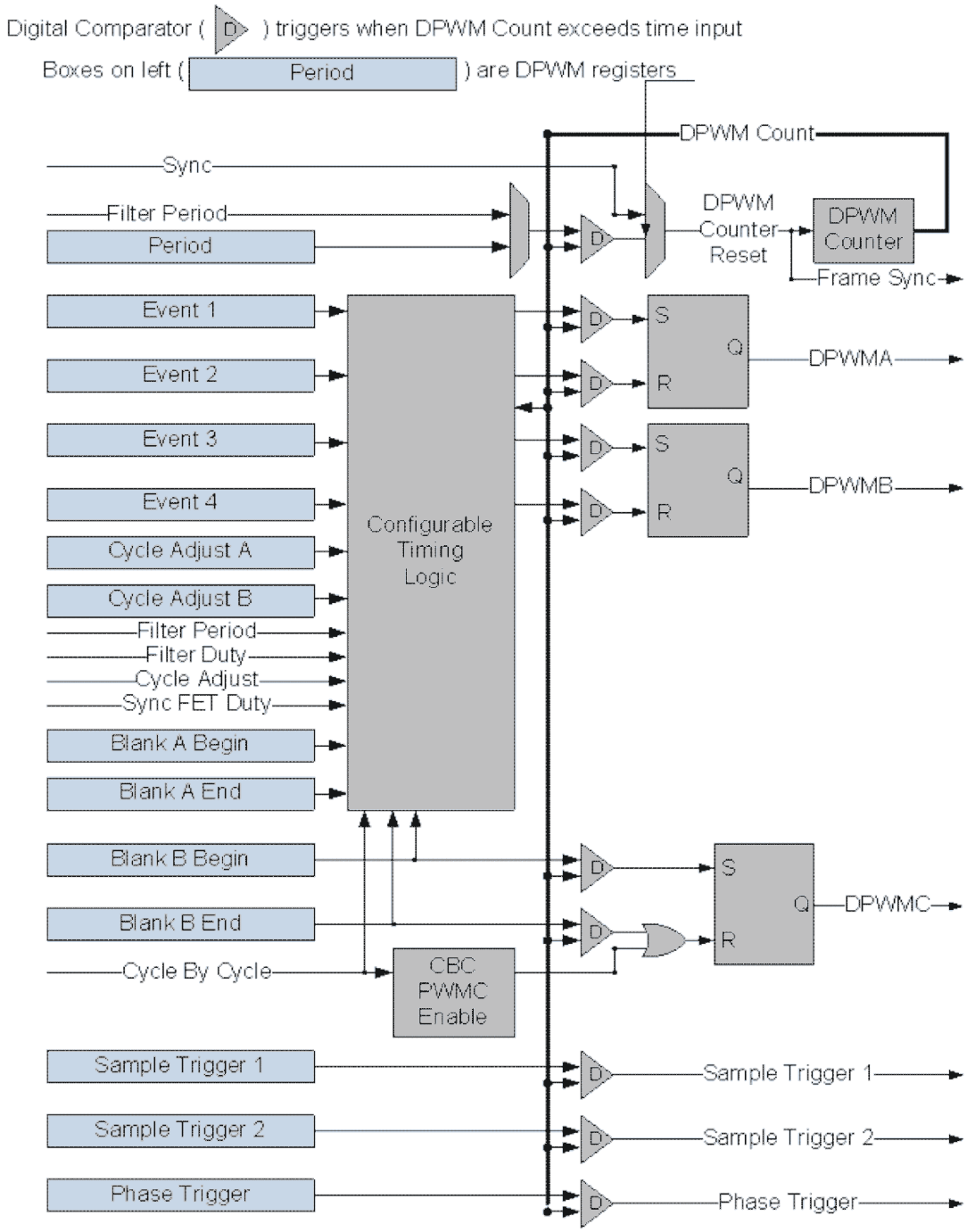

図 10-4. Fixed Signals to Bridge

These signals are actually routed to pins DPWM3A and 3B using the Intra Mux with these statements:

```
Dpwm3Regs.DPWMCTRL0.bit.PWM_A_INTRA_MUX = 7; // Send DPWM1C
Dpwm3Regs.DPWMCTRL0.bit.PWM_B_INTRA_MUX = 8; // Send DPWM2C
```

Since these signals are really being used as events in the timer, the #defines are called EV5 and EV6. Here are the statements which initialize them:

```
// Setup waveform for DPWM-C (re-using blanking B regs)
Dpwm2Regs.DPWMBLKBBEG.all = PWM2_EV5 + (4 *16);
Dpwm2Regs.DPWMBLKBEND.all = PWM2_EV6;
```

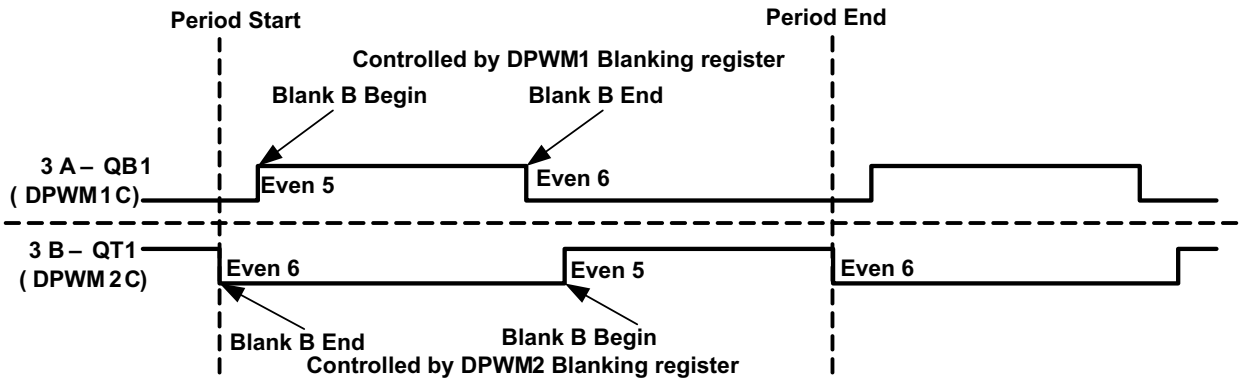

図 10-5. Blank B Timing Information

The statements for DPWM1 are the same. Remember that DPWMC reuses the Blank B registers for timing information.

10.2.2.5 Dynamic Signals to Bridge

DPWM0 and 1 are set at normal mode. PCMC triggering signal (fault) chops DPWM0A and 1A cycle by cycle. The corresponding DPWM0B and 1B are used for synchronous rectifier MOSFET control. The same PCMC triggering signal is applied to DPWM2 and DPWM3. Both of these are set to normal mode as well. DPWM2 and 3 are chopped and their edges are used to generate the next two dynamic signals to the bridge. They are generated using the Edge Generator Module in DPWM2. The Edge Generator sources are DPWM2 and DPWM3. The edges used are:

DPWM2A turned on by a rising edge on DPWM2BF
DPWM2A turned off by a falling edge on DPWM3AF
DPWM2B turned on by a rising edge on DPWM3BF
DPWM2B turned off by a falling edge on DPWM2AF

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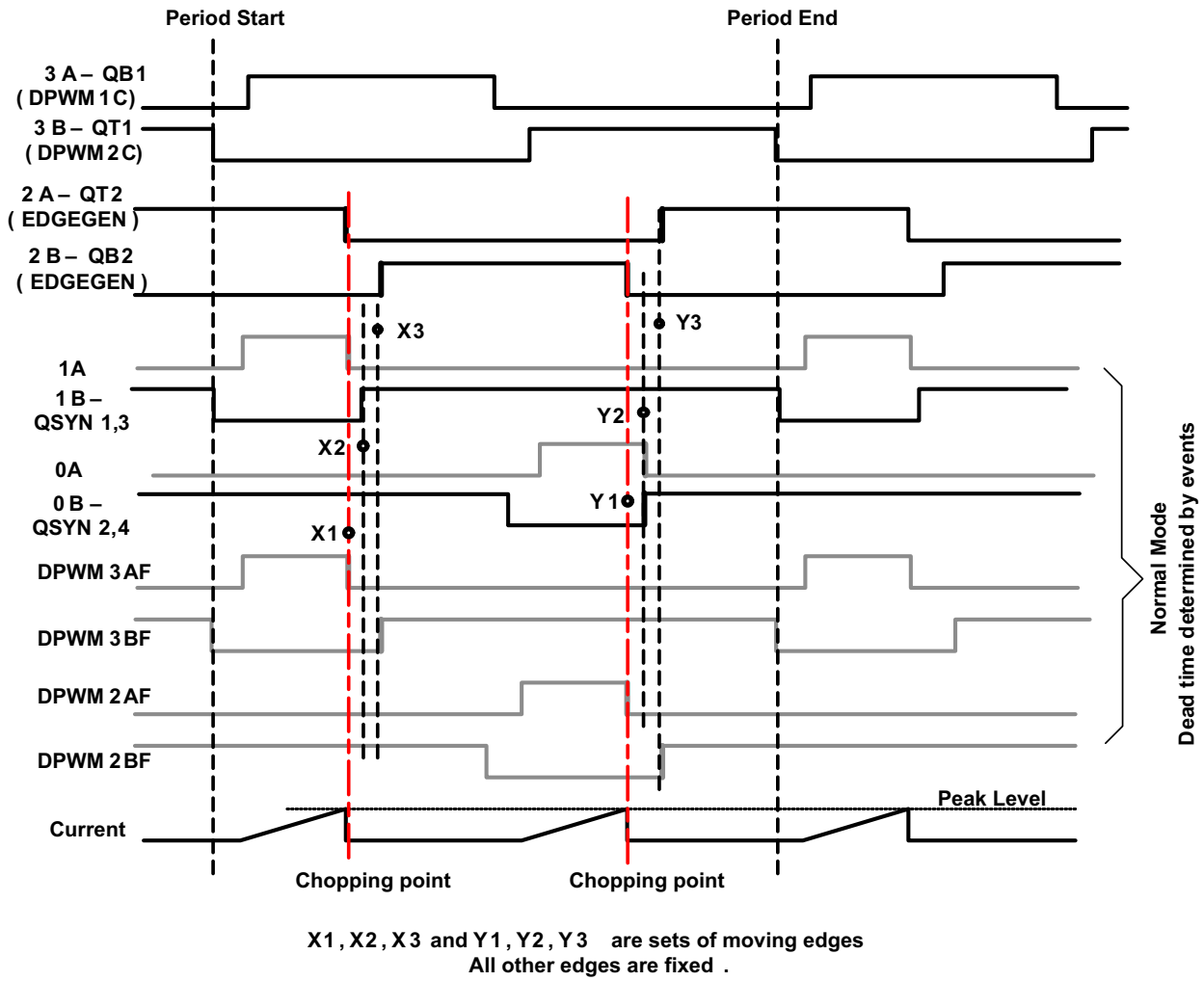

図 10-6. Dynamic Signals to Bridge

The Edge Generator is configured with these statements:

```
Dpwm2Regs.DPWMEDGEGEN.bit.A_ON_EDGE = 2;
Dpwm2Regs.DPWMEDGEGEN.bit.A_OFF_EDGE = 5;
Dpwm2Regs.DPWMEDGEGEN.bit.B_ON_EDGE = 6;
Dpwm2Regs.DPWMEDGEGEN.bit.B_OFF_EDGE = 1;

Dpwm2Regs.DPWMCTRL0.bit.PWM_A_INTRA_MUX = 1; // EDGEGEN-A out the A output
Dpwm2Regs.DPWMCTRL0.bit.PWM_B_INTRA_MUX = 1; // EDGEGEN-B out the B output

Dpwm2Regs.DPWMEDGEGEN.bit.EDGE_EN = 1;
```

The EDGE_EN bits are set for all 4 DPWMs. This is done to ensure that all signals have the same timing delay through the DPWM.

The finial 6 gate signals are shown in 図 10-7.

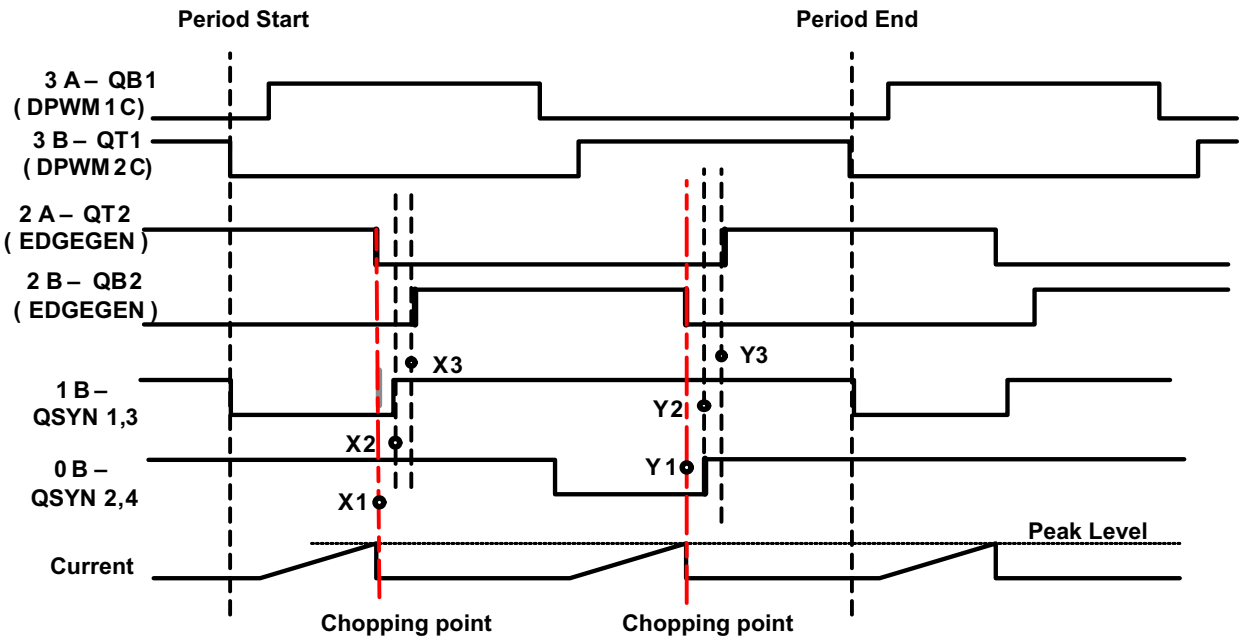

図 10-7. Final 6 Gate Signals

Note how the falling edge of DPWM2AF aligns with the X1 edge, and how the rising edge of DPWM2BF aligns with the X3 edge. The falling edges on DPWM2AF and DPWM3AF are caused by the peak detection logic. This is fed through the Cycle By Cycle logic. The Cycle By Cycle logic also has a special feature to control the rising edges of DPWM2BF (X1 and X3) and DPWM3BF (Y1 and Y3). It uses the value of Event3 – Event2 to control the time between the edges. The same feature is used with DPWM0 and DPWM1 to control the X2 and Y2 signals. Using the other 2 DPWMs permits these signals to have a different dead time.

The same setup can be used for voltage mode control. In this case, the Filter output sets the timing of the falling edge on DPWMxAF.

All DPWMs are configured in Normal mode, with CBC enabled. If external slope compensation is used, DPWM1A and DPWM1B are used to reset the external compensator at the beginning of each half cycle. If no PCMC event occurs, the values of Events 2 and 3 determine the locations of the edges, just as in open loop mode.

10.2.2.6 System Initialization for PCM

PCM (Peak Current Mode) is a specialized configuration for the UCD3138x which involves several peripherals. This section describes how it works across the peripherals.

10.2.2.6.1 Use of Front Ends and Filters in PSFB

All three front ends are used in PSFB. The same signals are used in the same places for both PCMC and voltage mode. The same hardware can be used for both control modes, with the mode determined by which firmware is loaded into the device. FE0 and FE1 are used with their associated filters, but Filter 2 is not used at all.

FE0 – Vout – voltage loop
FE1 – Iout – current loop
FE2 – Ipri – PCM

In PCMC mode, FE2 is used for PCMC, and the voltage loop is normally used to provide the start point for the compensation ramp. If the CPCC firmware detects a need for constant current mode, it switches to the current loop for the start point.

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10.2.2.6.2 Peak Current Detection

Peak current detection involves all the major modules of the DPPs, the Front End, Filter, Loop Mux, Fault Mux and the DPWMs. A drawing of the major elements is shown in 図 10-8.

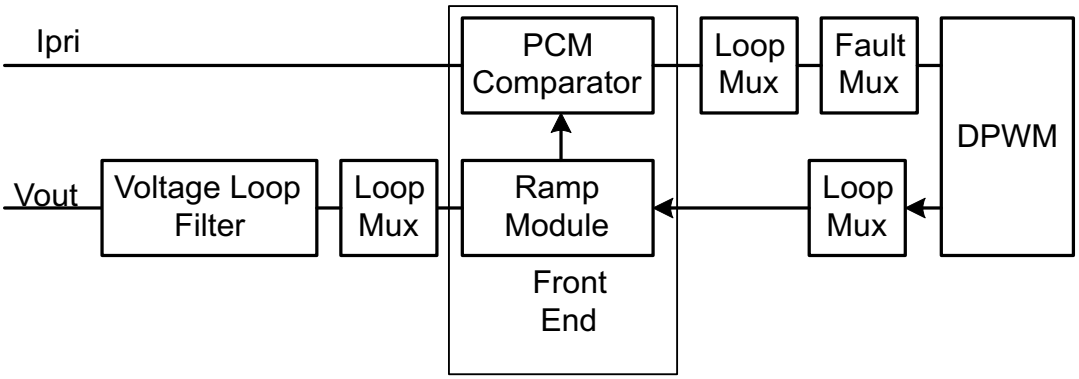

図 10-8. Peak Current Detection Function

All signals without arrows flow from left to right. The voltage loop is used to select a peak current level. This level is fed to the Ramp module to generate a compensation ramp. The compensation ramp is compared to the primary current by the PCMC comparator in the Front End. When the ramp value is greater than the primary current, the APCMC signal is sent to the DPWM, causing the events described in the previous sections.

The DPWM frame start and output pin signals can be used to trigger the Ramp Module. In this case, unlike in the case of other ramp module functions, each DPWM frame triggers the start of the ramp. The ramp steps every 32 ns.

The Filter is configured normally, there is no real difference for PCMC. The PCM_FILTER_SEL bits in the LoopMux.PCMCTRL register are used to select which filter is connected to the ramp module:

LoopMuxRegs.PCMCTRL.bit.PCM_FILTER_SEL =0; //select filter0

With Firmware Constant Power/Constant current, Filter 1 and Front End 1 are used as a current control loop, with the EADCDAC set to high current. If the voltage loop value becomes higher than the current loop value, then Filter 1 is used to control the PCM ramp start value:

LoopMuxRegs.PCMCTRL.bit.PCM_FILTER_SEL =1;
//select filter1 for slope compensation source

In the ramp module, there are 2 bitfields in the RAMPCTRL register which must be configured. The PCM_START_SEL must be set to a 1 to enable the Filter to be used as a ramp start source. The RAMP_EN bit must be set, of course.

The DAC_STEP register sets the slope of the compensation ramp. The DAC value is in volts, of course, so it is necessary to calculate the slope after the current to voltage conversion. Here is the formula for converting from millivolts per microsecond to DACSTEP.

m = compensation slope in millivolts per microsecond

ACSTEP = 335.5 × M

In C, this can be written:

```
#define COMPENSATION_SLOPE 150 //compensation slope in millivolts per microsecond
#define DACSTEP_COMP_VALUE ((int) (COMPENSATION_SLOPE*335.5) )
        //value in DACSTEP for desired compensation slope

        FeCtrl0Regs.DACSTEP.all = DACSTEP_COMP_VALUE;
```

It may also be necessary to set a ramp ending value in the RAMPDACEND register.

In addition, it is necessary to set the D2S_COMP_EN bit in the EADCCTRL register. This is for enabling the differential to single ended comparator function. The front end diagram leaves it out for simplicity, but the connection between the DAC and the EADC amplifier is actually differential. The PCMC comparator, however, is single ended. So a conversion is necessary as shown in 図 10-9.

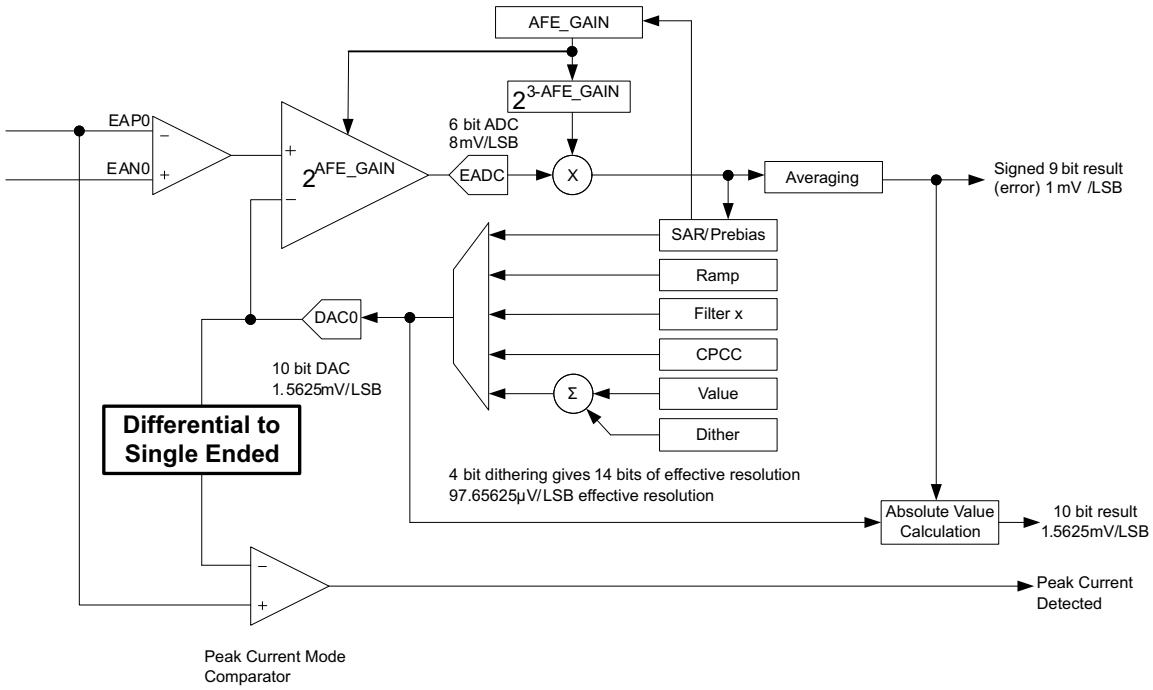

図 10-9. Differential to Single-Ended Comparator Function

The EADC_MODE bit in EADCCTRL should be set to a 5 for peak current mode.

The peak current detection signal next goes to the Loop Mux. The Fault Mux has only 1 APCM input, but there are 3 front ends. So the PCM_FE_SEL bits in APCMCTRL must be used to select which front end is used:

LoopMuxRegs.APCMCTRL.bit.PCM_FE_SEL = 2; // use FE2 for PCM */

The PCM_EN bit must also be set.

LoopMuxRegs.APCMCTRL.bit.PCM_EN = 1; // Enable PCM

Next the Fault Mux is used to enable the APCM bit to the CLIM/CBC signal to the DPWM. There are 4 DPWMxCLIM registers, one for each DPWM. The ANALOG_PCM_EN bit must be set in each one to connect the PCM detection signal to the CLIM/CBC signal on each DPWM. For the latest configuration information on all of these bits, consult the appropriate EVM firmware. To avoid errors, it is best to configure your hardware design using the same DPWMs, filters, and front ends for the same functions as the EVM.

DPWM timing is used to trigger the start of the ramp. This is selected by the FECTRLxMUX registers in the Loop Mux. DPWMx_FRAME_SYNC_EN bits, when set, cause the ramp to be triggered at the start of the DPWM period.

10.2.2.6.3 Peak Current Mode (PCM)

There is one peak current mode control module in the device however any front end can be configured to use this module.

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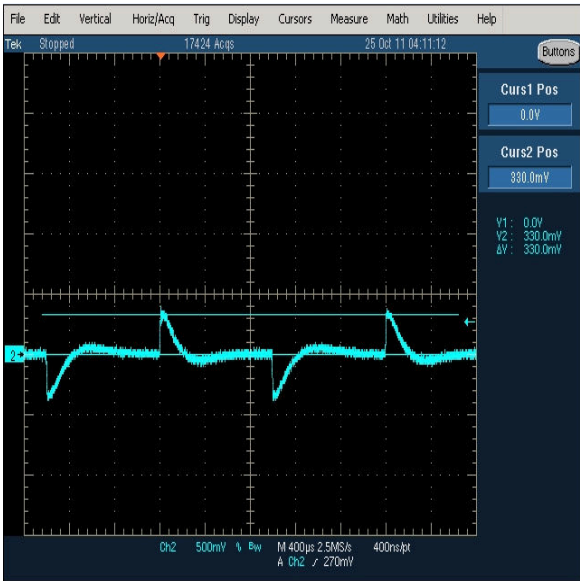
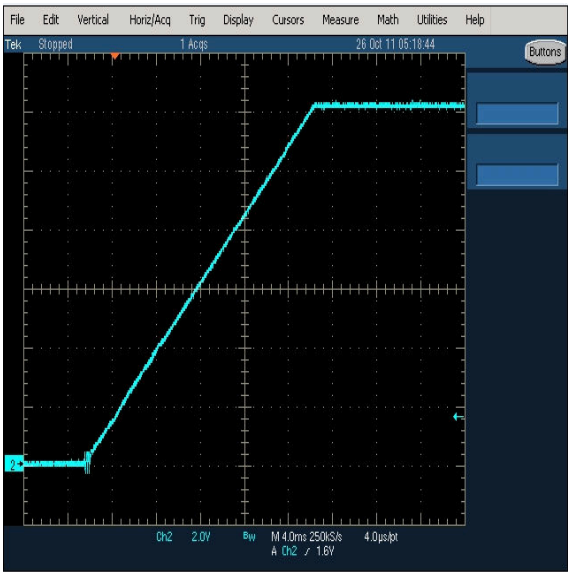
10.2.3 Application Curves



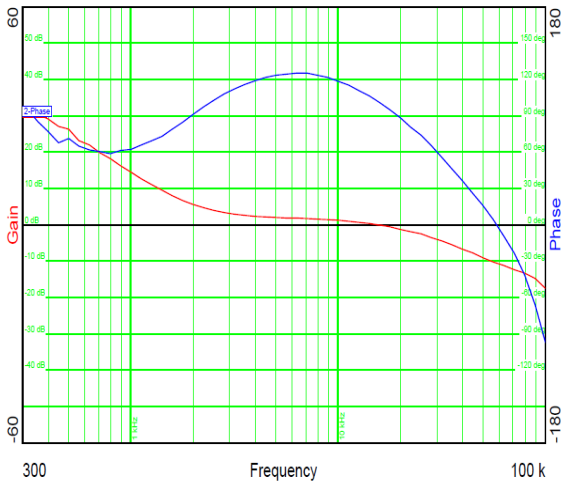
1A-16A-1A Vin =385V

図 10-10. Load Transient



30A Load syncFETs off

図 10-11. V_{OUT} Soft Start



Kp =14000 Kd =2000
Ki =300 Alpha = –2

図 10-12. Bode Plot

11 Power Supply Recommendations

For additonal power supply and layout recommendations, see the UCD3138 Family - Practical Design Guideline SLUA779

11.1 Introduction To Power Supply and Layout Recommendations

This is an introduction for the sections on Power Supply and Layout.

There are multiple grounds and bias power pins for digital controllers such as the UCD3138 family products. They are separated from each other because of the digital circuitry and analog circuitry inside the device. Normally, digital circuits draw more current and generate more noise, but the digital signal is not sensitive to the noise; while the analog circuit needs quiet power and grounding. A deliberate grounding and power separation outside the controller can reduce the interference between analog circuits and digital circuits, and therefore, the controller can have better performance. When they are separated from each other, take care of how the analog circuit and digital circuit are grouped, respectively, and then how and where they are tied together. With improper grounding, the device performance can be negatively impacted including DPWM abnormal, device reset, ADC results, output voltage ripple, and so on.

These sections supersede all older guidelines on UCD family board design and layout. Older EVM designs may not meet all of these guidelines.

In the PCB design, there are two options. One is to have two separate grounds - digital ground and analog ground. The other is to use a single ground plane for both digital ground and analog ground. With two separate ground planes, how to connect digital ground and analog ground is very important, and the PCB must be designed very carefully. With a single ground plane, there is no concern regarding where two grounds are tied together, and it makes the PCB design easier. Here, TI recommends using a single ground plane.

In these sections, digital ground is denoted as DGND; analog ground is denoted as AGND; a single ground plane is denoted as SGND.

11.2 3.3-V Supply Pins

+3.3 V bias normally is produced by a LDO or Buck converter. +5 V (or +12 V) normally are generated by a flyback converter and it is referenced to the Power Return. A 10 µF capacitor is locally used for LDO or buck between +3.3 V and Power RTN node. From there, use a single plane (SGND) for both digital ground and analog ground. A 1Ω resistor is needed between V33D and V33A. V33D and V33DIO should be shorted externally if they are available and have a wider trace or preferably through its own power plane to connect them. As an example, a 4.7-µF decoupling capacitor is used for V33A and V33D respectively and these decoupling capacitors should be placed close to the device pins. In addition, a 10nF capacitor is used for V33A, V33D and V33DIO respectively to filter out the high frequency noise and placed as close to the pin as possible, for example the distance is less than 25mils from the capacitor to the pin V33D (or V33DIO) and from the capacitor to the pin DGND. 10 nF uses smaller package such as 0402 and low ESR capacitor. Refer to the Layout section. There should not be any voltage delta between the DGND pins and AGND pins. Multiple vias are required to connect the extended power pad (for example, copper plane under the device power pad) to the internal single ground (SGND) plane layer. All digital and analog ground pins are directly connected to the extended power pad and connected to the internal SGND plane through vias.

11.3 Recommendation for V33 Ramp up Slew Rate for UCD3138 and UCD3138064

UCD3138 and UCD3138064 need a 2.2-µF pullup capacitor from BP18 to V33 as described before. Capacitors with a value of 2.2 µF and 1 µF create a capacitor divider which pull BP18 up as V33 rises. Ensure that as V33 rises, the slew rate is not fast enough to cause BP18 to overshoot, resulting in a reliability issue. TI requires that the maximum voltage of BP18 does not exceed 1.95 V. By calculation, if V33 ramps up linearly, the maximum V33 slew rate should be less than 6 V/ms.

Also, the internal BP18 regulator is enabled when V33 is higher than V_{GH} and POR is activated. V33 charges the capacitor of BP18 through the internal regulator. This charge causes a voltage dip in the V33 pin as shown in 図 11-1 and the charge may trigger a V33 undervoltage (POR) event, causing a chip reset. To prevent POR trigger signal oscillation and successive chip resets, TI recommends a minimum slew rate of 2.6 V/ms.

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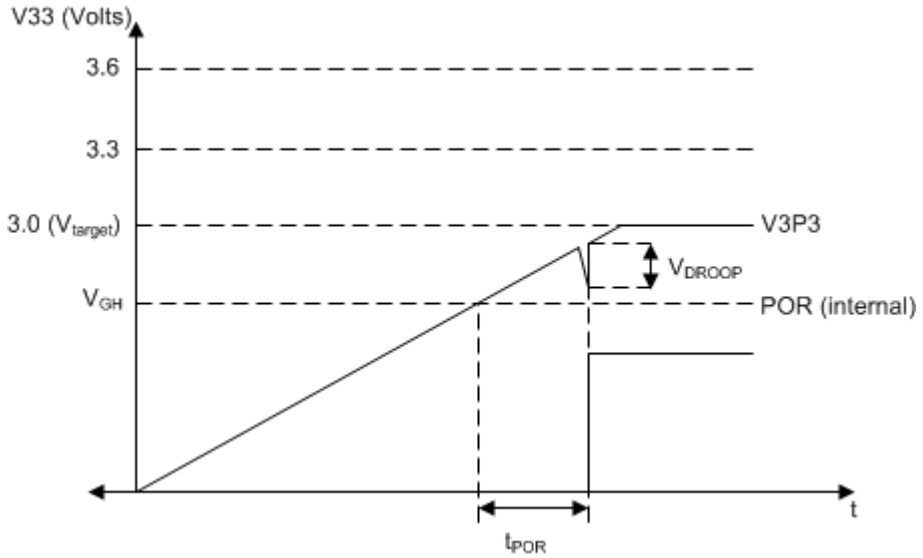

図 11-1. V33 Voltage Dip When POR is Activated

From the 図 11-1 recommendations, the slew rate using the 2.2 uF/1uF capacitor combination requires that the slew rate must be as follows:

$$6\,V/ms \geq SR \geq 2.6\,V/ms \tag{1}$$

11.4 Recommendation for RC Time Constant of $\overline{\text{RESET}}$ Pin for UCD3138 and UCD3138064

Ideally, the ARM core should begin execution of ROM code only after V33>3V. The ROM code reads trim values and loads trim registers. Lack of sufficient voltage during this operation can result in unexpected device functioning. Depending on V33 slew rate, the duration for which there is insufficient voltage on V33 is varied. During this time, a reliable trim operation is not ensured. Applying an RC filter between V33 and the $\overline{\text{RESET}}$ pin can increase the delay from V33 power up to the device coming out of reset.

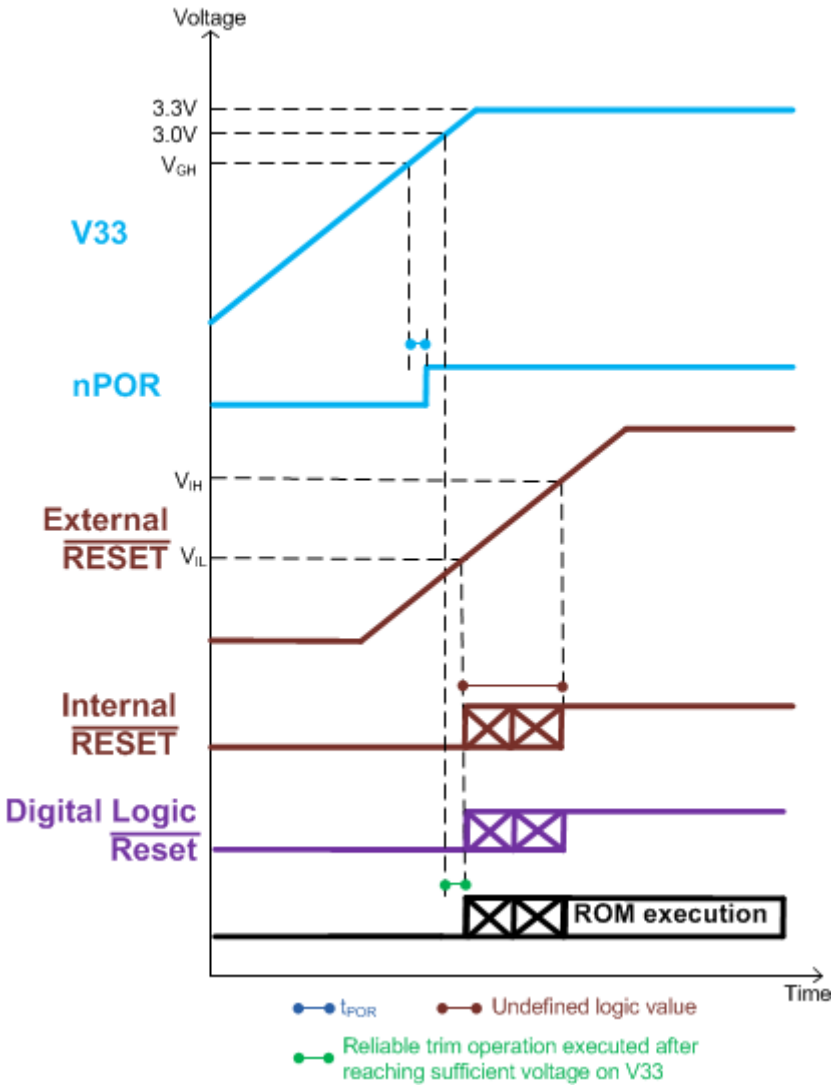

図 11-2. Recommended Timing Diagram of V33 and $\overline{\text{RESET}}$ for UCD3138 and UCD3138064

Example Solution:

If the V33 supply slew rate is 0.6 V/ms, then the minimum τ required is calculated as follows:

$$\tau_{RESET} = \frac{V_{target} - V_{IL}}{SR} \tag{2}$$

$$\tau_{RESET_min} = \frac{3\,V - 1.1\,V}{0.6\,V/ms} \approx 3.16\ ms \tag{3}$$

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If R and C are 2.21 k and 2.2 uF, then τ evaluates as:

$$\tau = R \times C \approx 2.21\,k\Omega \times 2.2\,\mu F = 4.862\,ms \tag{4}$$

These values of 2.21 kΩ and 2.2 μF will ensure that the $\overline{RESET}$ will be a logic-0 until V33 crosses 3V. [τ > τRESET_MIN]

12 Layout

12.1 Layout Guidelines

12.1.1 EMI and EMC Mitigation Guidelines

Every design is different in terms of EMI and EMC mitigation, and all designs require their own solution.

- Apply multiple different capacitors for different frequency range on decoupling circuits. Each capacitor has different ESL, capacitance and ESR, and different frequency responses.
- Avoid long traces close to radiation sources, and place them into an internal layer. It is preferred to have ground shielding and add a termination circuit at the end of the trace.
- TI recommends single ground: SGND. A multilayer such as 4 layers board is recommended so that one solid SGND is dedicated for return current path.
  - Use one whole layer (L2) for SGND plane as shown in 図 12-1. Use many vias (such as 9 vias) to connect the extended power pad to the internal SGND plane layer. It is preferred to have the vias close to AGND pins and DGND pins of the device.

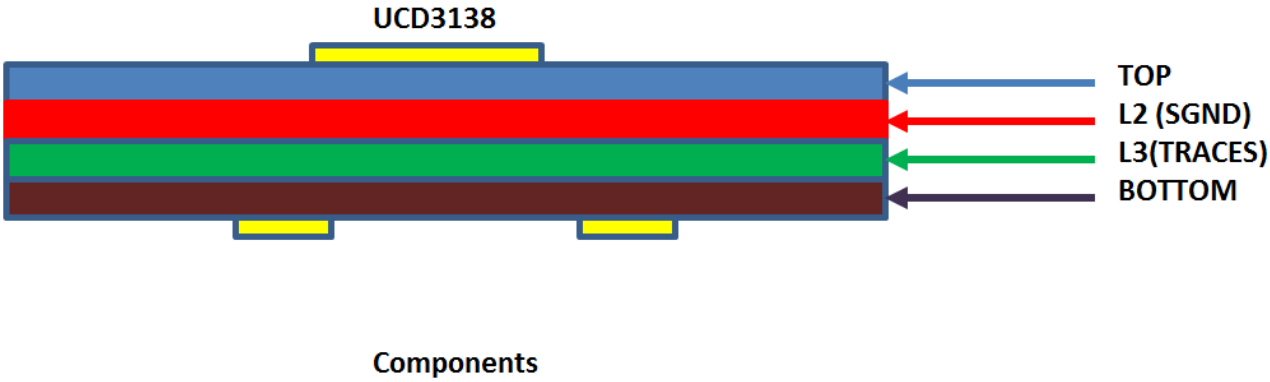

図 12-1. Optional Ground Layer Assignment

- Add LPF on analog signals close to the header connecting the control card and the power board.
- Do not use a ferrite bead to connect V33A and V33D instead of using 1-Ω resistor.
- Avoid negative current and negative voltage on all pins. Schottky diodes may be needed to clamp the voltage; avoid the voltage spike on all pins to exceed 3.8 V or below –0.3 V; add Schottky diodes on the pins which could have voltage spikes during surge test; be aware that Schottky diode has relatively higher leakage current, which can affect the voltage sensing at high temperatures. The need for external Schottky diodes is conditional. For example, the DPWM pins only need external Schottky diodes when there is a long distance, for example, more than 3 inches, between the control card and main power stage because in this case, the trace can pick up noise and cause electrical overstress on the device pins. The same is true for GPIO and PMBus pins.
- The auxiliary supply is normally a flyback converter, and its power transformer can generate a large electromagnetic field which can interfere with other electronic circuitry. By shielding the primary side windings, the EMI can be effectively reduced so that the surrounding circuits can have a quieter working environment.

12.1.2 BP18 Pin

Two parallel capacitors, 1μF and 10nF, are used between BP18 and SGND. The 10nF is placed closer to the pin than 1uF. Please note that only for the UCD3138 (40-pin and 64-pin) and UCD3138064 (40-pin and 64-pin) devices, it is required to have a 2.2-μF decoupling capacitor between V33D to BP18. The 2.2-μF capacitor is required to ramp BP18 when V33D is ramping up. Place the capacitors close to the device pins, and keep the return loop as small as possible.

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12.1.3 Additional Bias Guidelines

- Apply multiple different capacitors for different frequency range on decoupling circuits. Each capacitor has different ESL, capacitance, ESR and different frequency response.
- Avoid long traces close to radiation components and place them into an internal layer. It is preferred to have grounding shield and add a termination circuit at the end of long traces.
- Do NOT use a ferrite bead or a resistor with a value of 3-Ω or larger resistor to connect between V33A and V33D.
- Avoid negative current/negative voltage (–0.3 V) on all pins. Avoid voltage spikes of more than 3.8V on all pins. Schottky diodes may be required to clamp the voltage on any pins that could have voltage spikes during surge tests. Note that Schottky diodes have relatively higher leakage current, which can affect the voltage sensing at high temperature.
- If the bias supply to the device is a switching supply, ripple should be minimized. The higher the peak-to-peak magnitude and frequency of the ripple, the more the oscillator frequency changes.

12.1.4 UCD3138 Pin Connection Recommendation

The UCD3138 device is a highly integrated controller with a large number of mixed signals. It is important to group each pin, select good components, have appropriate connections to each pin, and make good component placement on the PCB to reduce noise coupling and to prevent chip mal-function. First, group all digital circuitry and analog circuitry. Second, place digital circuitry close to each other, place analog circuitry close to each other, and then make connections among them by a solid plane(SGND). To achieve a robust design, TI recommends at least a 4-layer board.

Next, layout considerations and examples are provided for some critical pins or signals.

12.1.4.1 Current Amplifier With EADC Connection

As shown in 図 12-2, if a current amplifier is used for current sensing, a differential input is recommended to suppress common mode noise. Then it is followed by a local low-pass filter (LPF), LPF should be placed close to the EAP and EAN pins of the UCD device. Both filters must be connected to the same ground plane (SGND).

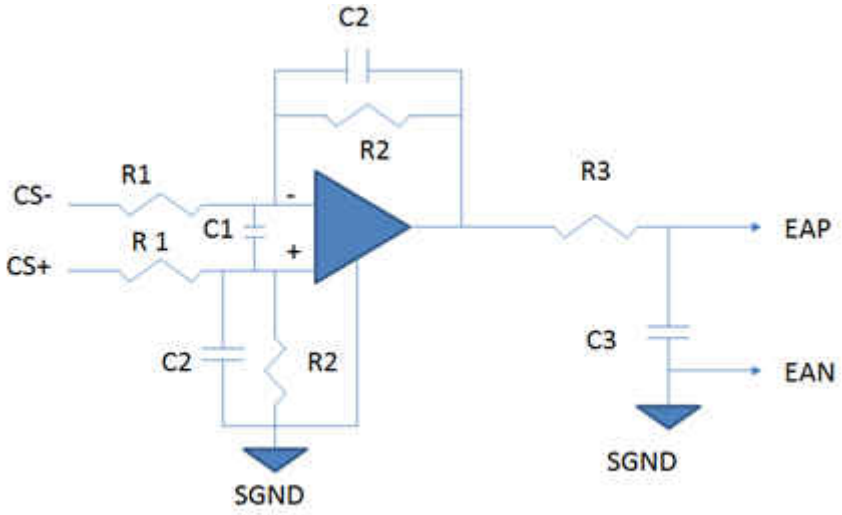

図 12-2. Current Amplifier Connected With EADC

12.1.4.2 DPWM Synchronization

For half bridge or full-bridge converter, where more than one DPWM modules are used to drive multiple pairs of MOSFETs, synchronization between DPWM modules is required. The synchronization can be achieved by using Master-Slave mode. A slaved DPWM can be synchronized with other Master DPWM or Slave DPWM. Without synchronization, the DPWM could go out of synchronization at large currents which can cause catastrophic damage.

Please note: For UCD3138ARMH and UCD3138ARJA, if the system use case is below -30C, DPWM fixed edge alignment should be avoided and at least a 4ns gap should be configured.

12.1.4.3 GPIOS

GPIO is referenced to DGND internally. When GPIO pins are not used connect the pins to SGND. Alternatively, they can be configured as output pins and set as low in the firmware. When GPIOs are used to drive other circuit like LED, be aware that traces can pick up noise. A local resistor close to the signal receiver (like LED) is used to terminate the coupled noise. If the big voltage swings, clamping diodes are needed for GPIO inputs, as shown in 図 12-3.

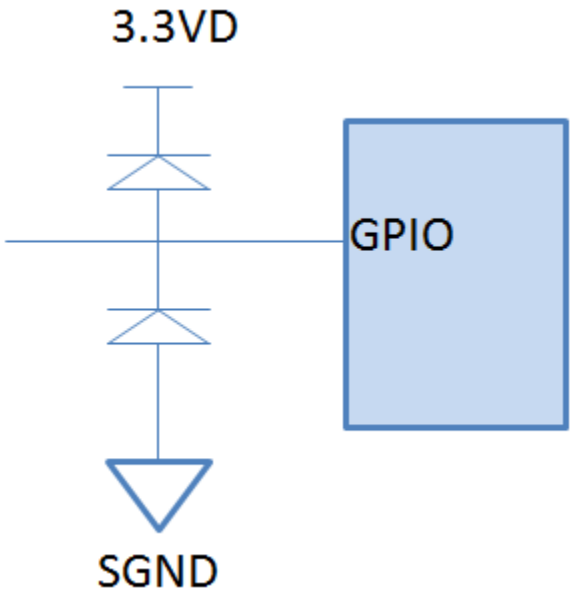

図 12-3. Clamping Diodes for GPIO

12.1.4.4 DPWM PINS

If DPWMs travel for a longer distance than 3 inches from the control card to a main power stage, a Schottky clamping diode may be needed as shown in 図 12-4to prevent electrical overstress on the device during lightning test. The long trace may also pick up the noise from other switching sources. Avoid DPWM signals to cross switching nodes.

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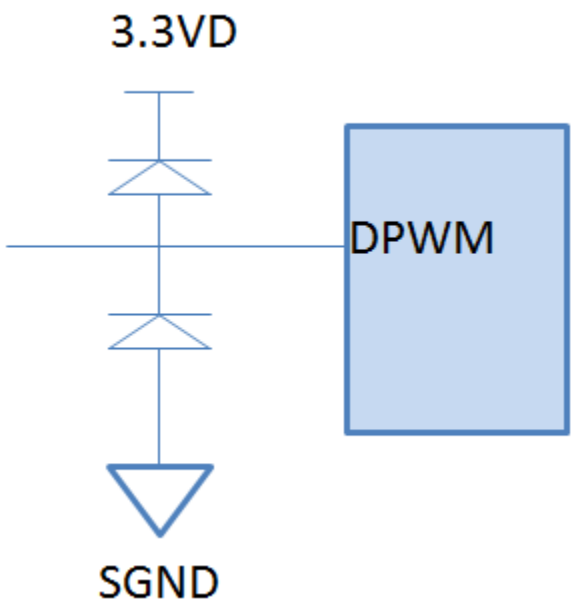

図 12-4. Clamping Diodes for DPWM

12.1.4.5 EAP and EAN Pins

There are three front-end ADCs to sense the feedback signals in the UCD family. These ADCs are dual-ended sensing input circuitry with good common mode noise rejection. Keep the distance between the two traces as short as possible when the differential sensing method is used. A local filter close to the EAP and EAN pins is required as shown in 図 12-5. Because EAP and EAN are used for feedback loop, C must be selected from the range of 100 pF to 1000 pF. R is preferred to use low resistance.

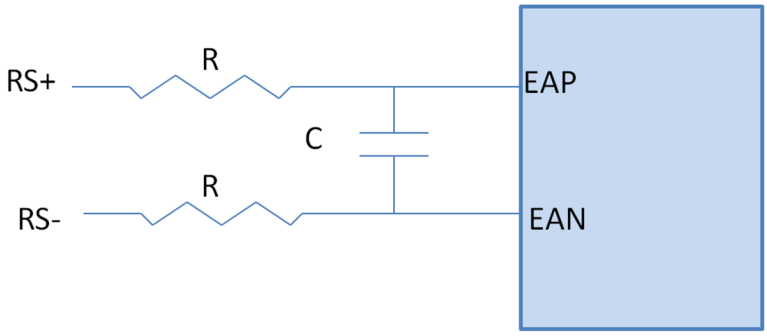

図 12-5. Local Filter on EAPx and EANx Pins

12.1.4.6 ADC Pins

Use low ESL and ESR ceramic capacitors on ADC pins to decouple with SGND. The capacitor value is selected such that the cut-off frequency is at least one tenth the sampling frequency if there is no dynamic requirement. This can help reduce noise coupled during signal transmission.

ADC input is a single-ended signal. If the sensing trace is long, move it away from radiation sources and add ground shielding between the signal and radiation sources. If there exists a resistor between signal output and ADC input, the resistor should be located close to the ADC pin. The resistance needs to be less than 1 kΩ.

For example, the sampling frequency is 10 kHz. The cut off frequency of LPF is 1 kHz. With a 1-kΩ equivalent resistor, select a 0.15-μF capacitor.

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12.1.5 UART Communication Port

UART is used for communicating between the primary side and secondary side with isolation boundary. Normally, the communication wires are long. These wires can easily be interfered by EMI and pick up noise of switching power supplies. First, the wires must be routed without directly exposing the traces to the switching noise source, and then a termination is needed at the end of the trace, as shown in 図 12-6. For example, R = 50 Ω, C = 47 pF if they don't significantly slow down the slew rate of the signals. When the pins are not used, tie them to the single ground plane SGND.

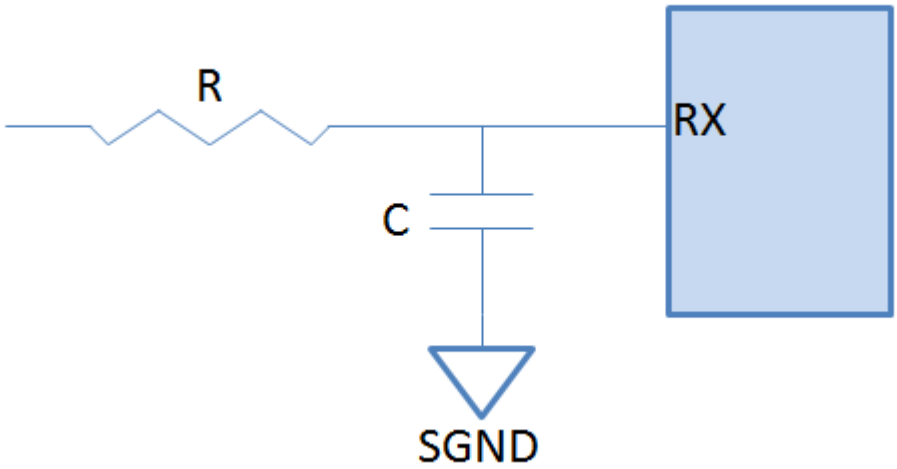

図 12-6. Termination for Communication Port (UART)

12.1.6 Special Considerations

- The first thing that must be done in any layout is to set up the basic grounding strategy and the placement of the decoupling capacitors. This needs to be prioritized over anything else, even the routing of sensitive feedback signals.
- If a gate driver device such as UCC27524 or UCC27511 is on the control card and there is a PGND connection, a net-short resistor or large copper trace must be used to tie the PGND to the Power RTN by multiple vias. Also, the net-short element between Power RTN and PGND must be close to the driver IC.
- Unused ADC pins must be tied to SGND.
- Avoid putting V33D and V33A long traces or planes close to radiation components. Place them into an internal layer. It is preferred to have ground shielding.
- Avoid putting bias supplies or SGND or Power RTN directly to across the switching power train where they can couple switching noise. If the grounds are coupled with noise, the decoupling capacitors may not be effective at filtering the noise out.
- Local capacitors are preferred to provide a short path for switching current, and be careful to select a quiet RETURN point to connect.
- In a power module or a tiny PCB design, a single solid plane without the grounding separation is shown in 図 12-7and has a single point connection with power RTN or SGND near the connector. Ensure there is no current flow from power train into the signal ground plane.

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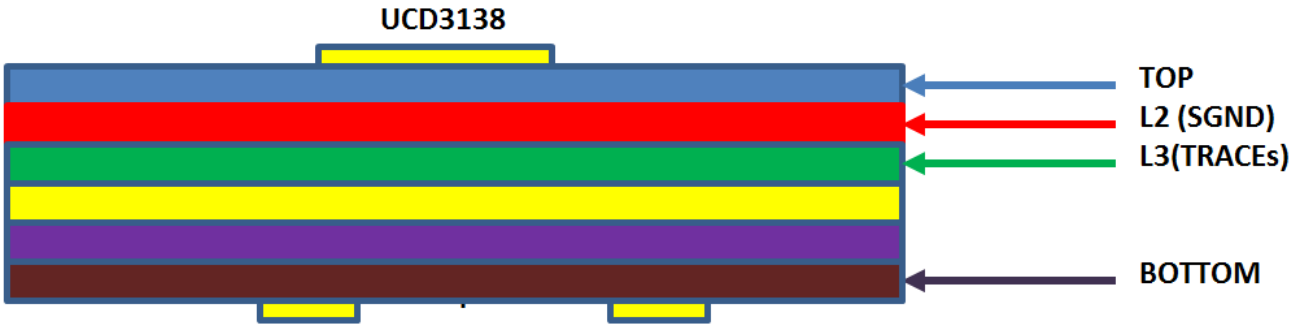

図 12-7. Single Ground Plane for a Power Module Design

12.2 Layout Example

図 12-8.

12.2.1 UCD3138 and UCD3138064 40 Pin

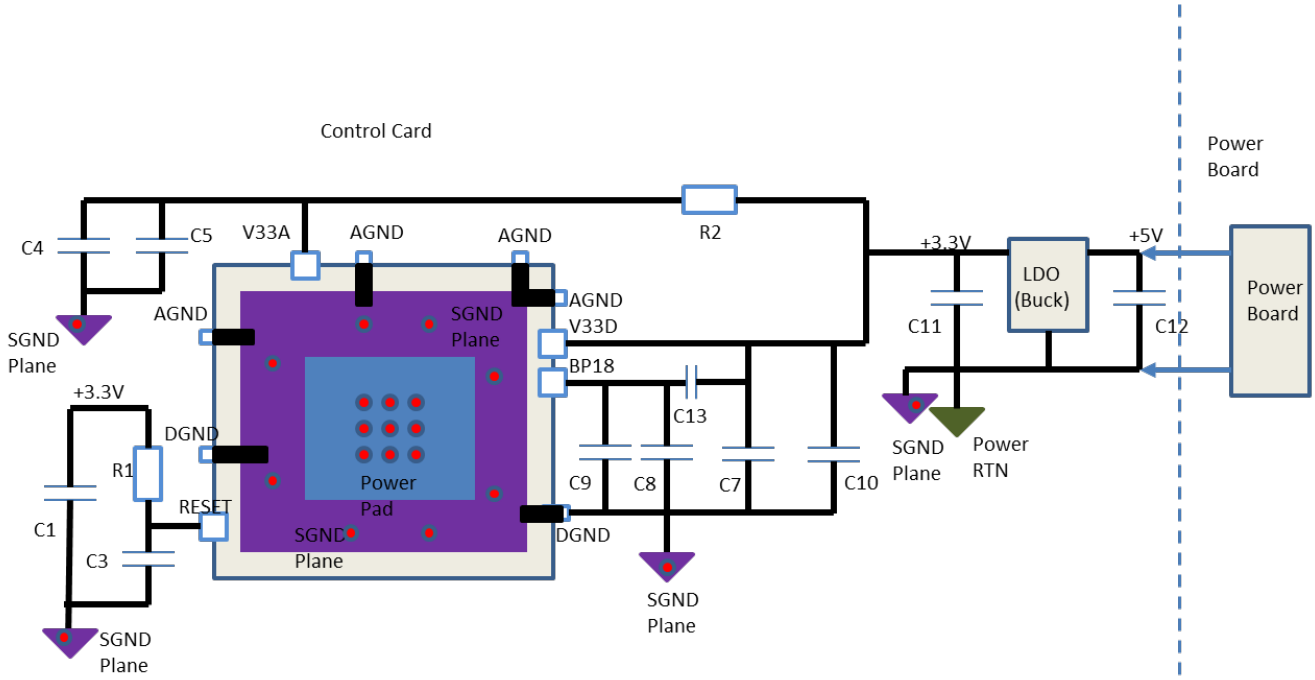

図 12-9. Power and Ground Schematic for UCD3138 and UCD3138064 40 Pin

表 12-1. Power and Ground Connection Components for UCD3138 and UCD3138064 40 Pin

COMPONENT	VALUE
C1	1 µF
C3	2.2 µF
R1	2.2 kΩ
C4	4.7 µF
C5	10 nF
C7	10 nF
C8	1 µF
C9	10 nF
C10	4.7 µF

表 12-1. Power and Ground Connection Components for UCD3138 and UCD3138064 40 Pin (continued)

COMPONENT	VALUE
R2	1 Ω
C11	10 µF
C12	10 µF
C13	2.2 µF

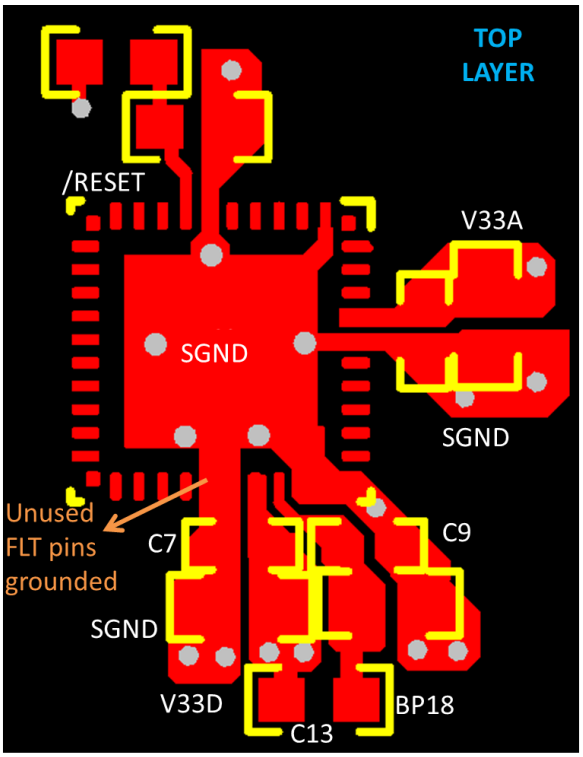

図 12-10. UCD3138 and UCD3138064 40 Pin Layout Top Layer

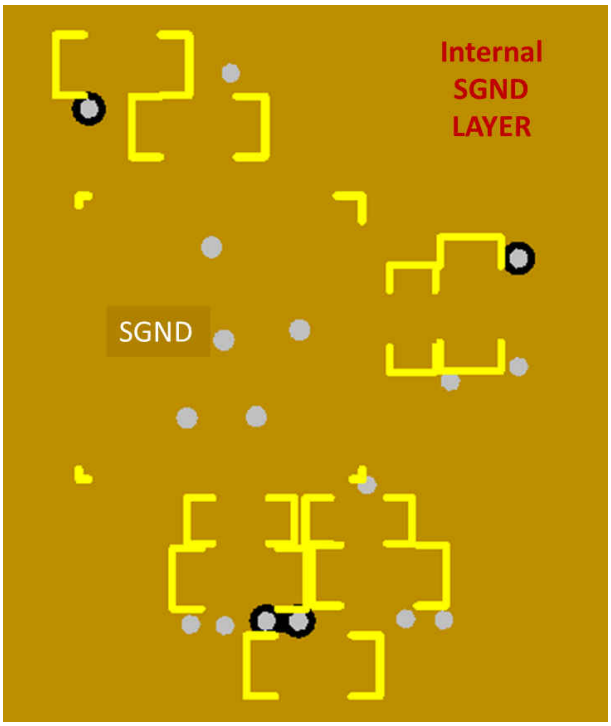

図 12-11. UCD3138 and UCD3138064 40 Pin Layout Internal SGND Layer

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12.2.2 UCD3138 and UCD3138064 64 Pin

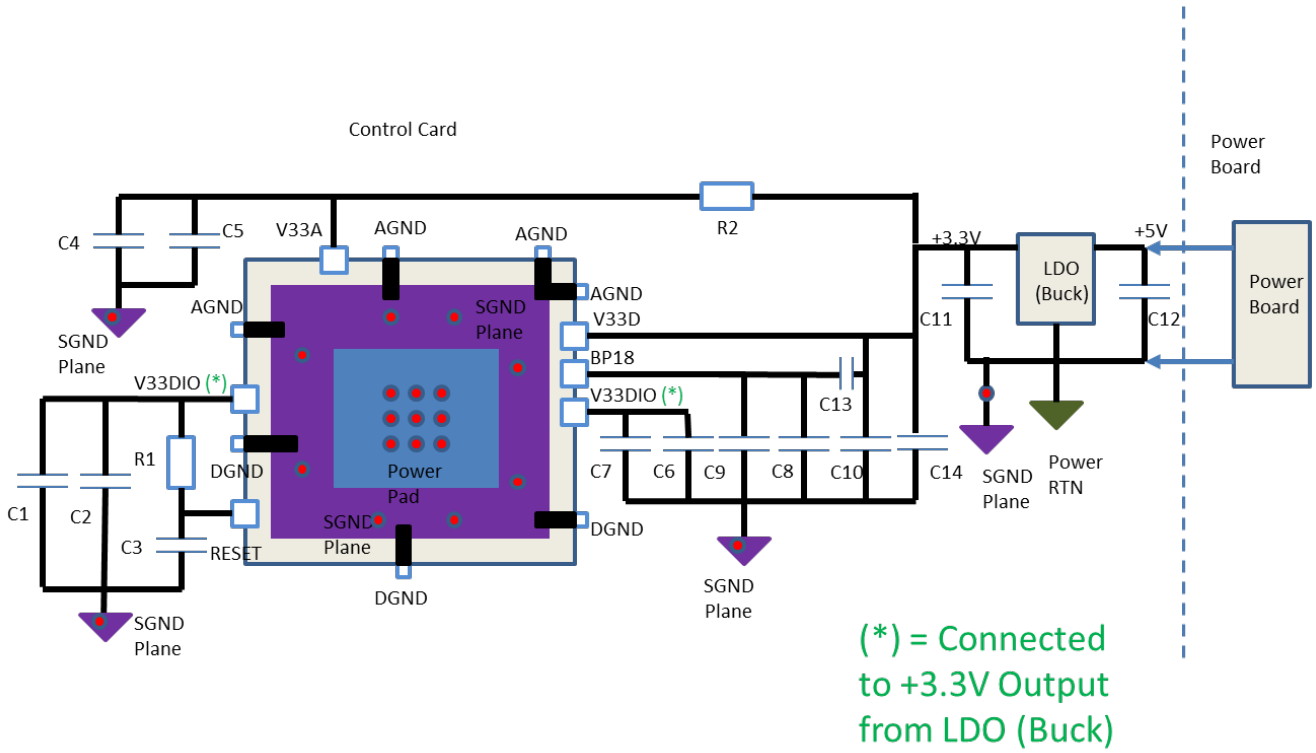

図 12-12. Power and Ground Schematic for UCD3138 and UCD3138064 64 Pin

表 12-2. Power and Ground Connection Components for UCD3138 and UCD3138064 64 Pin

COMPONENT	VALUE
C1	4.7 µF
C2	10 nF
C3	2.2 µF
R1	2.2 kΩ
C4	4.7 µF
C5	10 nF
C6	4.7 µF
C7	10 nF
C8	1 µF
C9	10 nF
C10	4.7 µF
R2	1 Ω
C11	10 µF
C12	10 µF
C13	2.2 µF
C14	10 nF

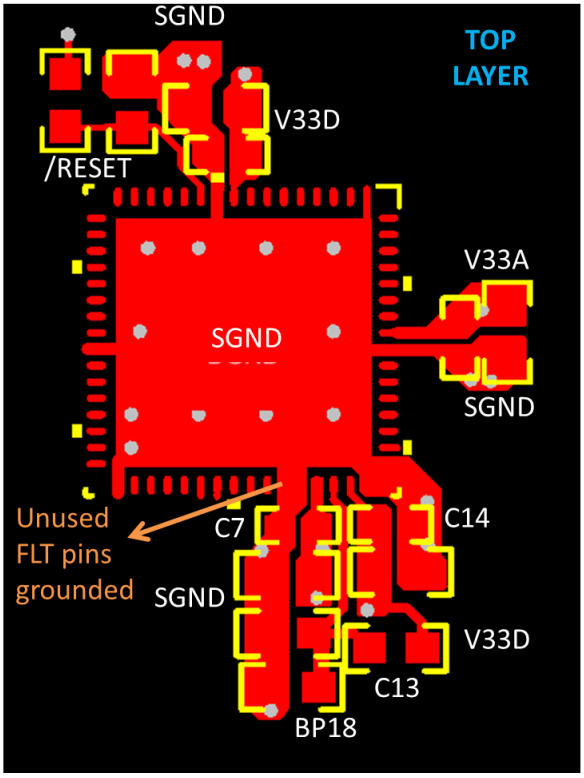

図 12-13. UCD3138 and UCD3138064 64 Pin Layout Top Layer

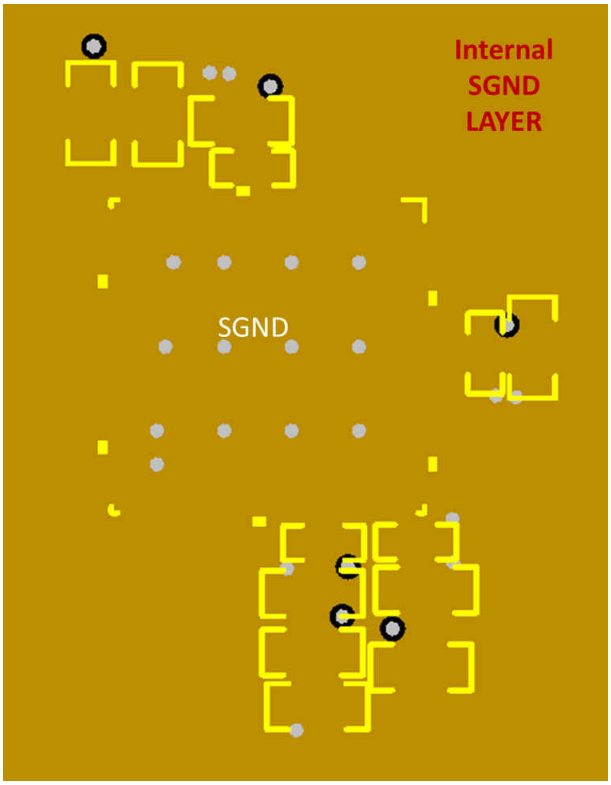

図 12-14. 64 Pin UCD3138 and UCD3138064 Layout Internal SGND Layer

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If it is not possible to fit all the capacitors on the top layer, there is an alternative recommended layout with the BP18 capacitors located on the bottom layer, directly underneath the UCD.

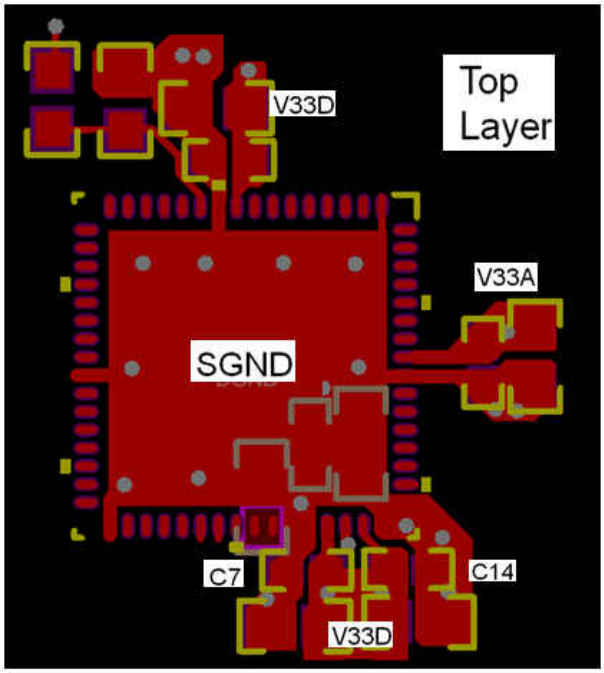

図 12-15. Alternative UCD3138 and UCD3138064 64 Pin Layout Top Layer

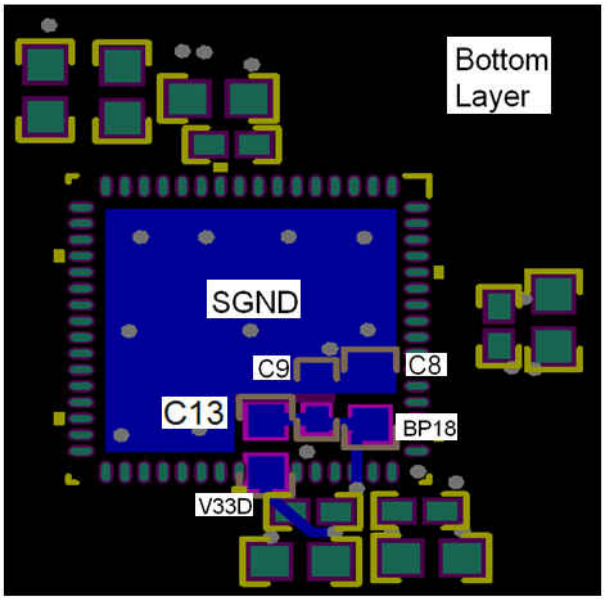

図 12-16. Alternative 64 Pin UCD3138 and UCD3138064 Layout Bottom Layer

13 Device and Documentation Support

13.1 Device Support

13.1.1 Code Composer Studio

TI offers the Code Composer Studio™ Integrated Development Environment (IDE): including Editor C/C++/Assembly Code Generation, and Debug. The tool's support documentation is electronically available within the Code Composer Studio™ Integrated Development Environment (IDE).

13.1.2 Tools and Documentation

Device programming, real time debug and monitoring/configuration of key device parameters for certain power topologies are all available through Texas Instruments' Fusion Digital Power Studio Graphical User Interface (https://www.ti.com/tool/FUSION-DIGITAL-POWER-STUDIO).

The Fusion Digital Power Studio software application uses the PMBus protocol to communicate with the device over a serial bus using an interface adaptor known as the USB-TO-GPIO, available as an EVM from Texas Instruments (http://www.ti.com/tool/usb-to-gpio). PMBUS-based real-time debug capability is available through the 'Memory Debugger' tool within the Device GUI module of the Fusion Digital Power Studio GUI, which represents a powerful alternative over traditional JTAG-based approaches.

The software application can also be used to program the devices, with a version of the tool known as Fusion Production Tool optimized for manufacturing environments (https://www.ti.com/tool/FUSION-PRODUCTION-GUI). The Fusion Production Tool supports multiple devices on a board, and includes built-in logging and reporting capabilities.

In terms of reference documentation, the following programmer's manuals are available offering detailed information regarding the application and usage of UCD3138 digital controller:

1. UCD3138 Technical Reference Manual - Key topics covered in this manual include:
   - Digital Pulse Width Modulator (DPWM)
     - Modes of Operation (Normal/Multi/Phase-shift/Resonant etc)
     - Automatic Mode Switching
     - DPWMC, Edge Generation & Intra-Mux
   - Front End
     - Analog Front End
     - Error ADC or EADC
     - Front End DAC
     - Ramp Module
     - Successive Approximation Register Module
   - Filter
     - Filter Math
   - Loop Mux
     - Analog Peak Current Mode
     - Constant Current/Constant Power (CCCP)
     - Automatic Cycle Adjustment
   - Fault Mux
     - Analog Comparators
     - Digital Comparators
     - Fault Pin functions
     - DPWM Fault Action
     - Ideal Diode Emulation (IDE), DCM Detection
     - Oscillator Failure Detection
   - ADC12
     - Control, Conversion, Sequencing & Averaging
     - Digital Comparators
     - Temperature Sensor
     - PMBUS Addressing

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  - Dual Sample & Hold
- Miscellaneous Analog Controls (Current Sharing, Brown-Out, Clock-Gating)
- PMBUS Interface
- General Purpose Input Output (GPIO)
- Timer Modules
- PMBus
- Boot ROM & Boot Flash
  - BootROM Function
  - Memory Read/Write Functions
  - Checksum Functions
  - Flash Functions
  - Avoiding Program Flash Lock-Up
- ARM7 Architecture
  - Modes of Operation
  - Hardware/Software Interrupts
  - Instruction Set
  - Dual State Inter-working (Thumb 16-bit Mode/ARM 32-bit Mode)
- Memory & System Module
  - Address Decoder, DEC (Memory Mapping)
  - Memory Controller (MMC)
  - Central Interrupt Module
- Register Map for all of the above peripherals in UCD3138

2. Fusion Digital Power Studio for Isolated Power Applications – User Guide

In addition to the tools and documentation described above, for the most up to date information regarding evaluation modules, reference application firmware and application notes/design tips, please visit http://www.ti.com/product/ucd3138.

13.2 Documentation Support

For related documentation see the following:

13.2.1 References

1. UCD3138 Technical Reference Manual (SNIU028)
2. Fusion Digital Power Studio for Isolated Power Applications (SLUA676)
3. UCD3138 Digital Power Training Series Video Training
4. UCD3138 Family - Practical Design Guideline Applications Note, (SLUA779)
5. ARM7TDMI-S Technical Reference Manual
6. System Management Bus (SMBus) Specification
7. PMBus™ Power System Management Protocol Specification

13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.4 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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13.5 Trademarks

ARM7TDMI-S™ is a trademark of ARM.

PMBus™ is a trademark of SMIF, Inc..
TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

13.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical Packaging and Orderable Information

14.1 Packaging Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCD3138RGCR	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCD3138
UCD3138RGCR.A	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCD3138
UCD3138RGCR.B	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCD3138
UCD3138RGCRG4	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCD3138
UCD3138RGCRG4.A	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCD3138
UCD3138RGCRG4.B	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCD3138
UCD3138RGCT	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCD3138
UCD3138RGCT.A	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCD3138
UCD3138RGCT.B	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCD3138
UCD3138RHAR	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	UCD3138
UCD3138RHAR.A	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	UCD3138
UCD3138RHAR.B	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	UCD3138
UCD3138RHAT	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	UCD3138
UCD3138RHAT.A	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	UCD3138
UCD3138RHAT.B	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	UCD3138
UCD3138RJAR	Active	Production	VQFN (RJA) | 40	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	UCD3138
UCD3138RJAR.A	Active	Production	VQFN (RJA) | 40	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	UCD3138
UCD3138RJAR.B	Active	Production	VQFN (RJA) | 40	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	UCD3138
UCD3138RJAT	Active	Production	VQFN (RJA) | 40	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	UCD3138
UCD3138RJAT.A	Active	Production	VQFN (RJA) | 40	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	UCD3138
UCD3138RJAT.B	Active	Production	VQFN (RJA) | 40	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	UCD3138
UCD3138RMHR	NRND	Production	WQFN (RMH) | 40	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	3138RMH
UCD3138RMHR.A	NRND	Production	WQFN (RMH) | 40	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	3138RMH
UCD3138RMHT	NRND	Production	WQFN (RMH) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	3138RMH
UCD3138RMHT.A	NRND	Production	WQFN (RMH) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	3138RMH

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

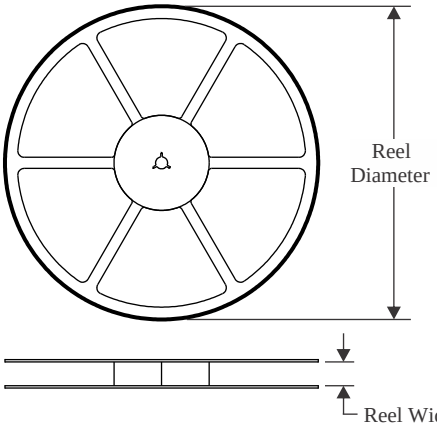
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

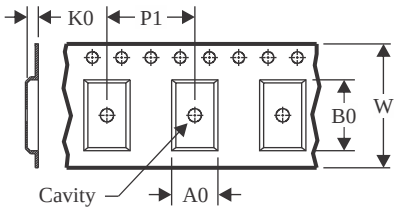
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

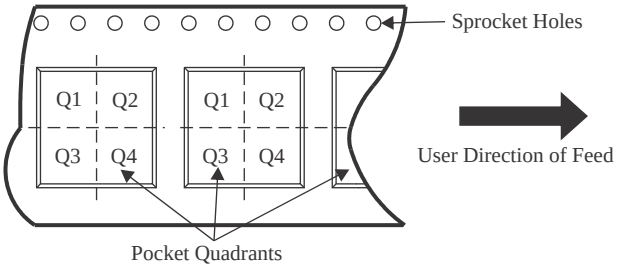


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

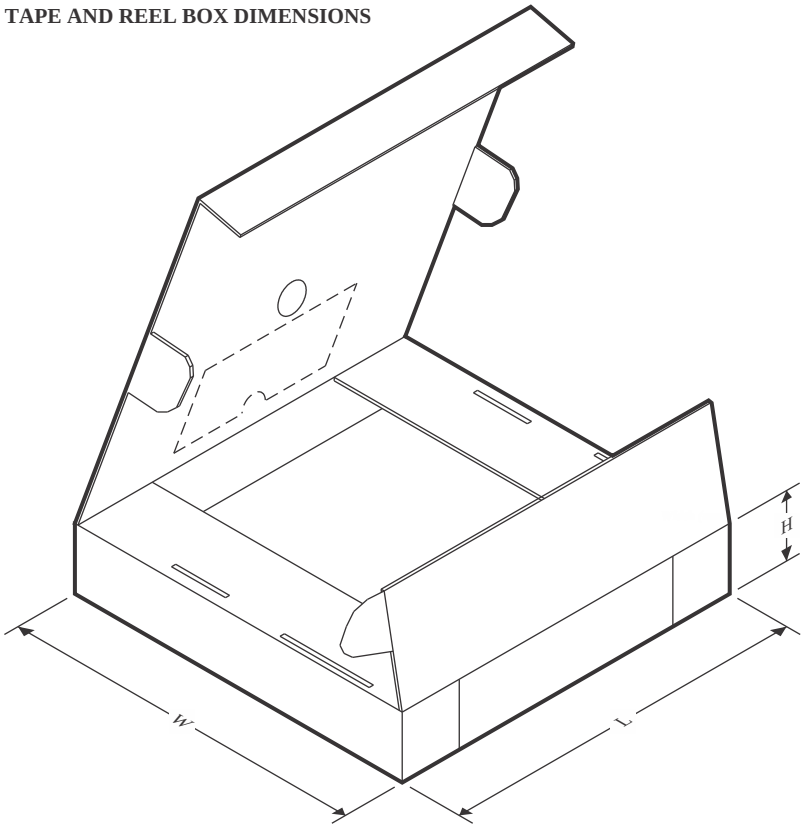
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCD3138RGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
UCD3138RGCRG4	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
UCD3138RGCT	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
UCD3138RHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
UCD3138RJAR	VQFN	RJA	40	3000	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
UCD3138RJAT	VQFN	RJA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
UCD3138RMHR	WQFN	RMH	40	2000	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
UCD3138RMHT	WQFN	RMH	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCD3138RGCR	VQFN	RGC	64	2000	367.0	367.0	38.0
UCD3138RGCRG4	VQFN	RGC	64	2000	367.0	367.0	38.0
UCD3138RGCT	VQFN	RGC	64	250	210.0	185.0	35.0
UCD3138RHAR	VQFN	RHA	40	2500	367.0	367.0	38.0
UCD3138RJAR	VQFN	RJA	40	3000	367.0	367.0	38.0
UCD3138RJAT	VQFN	RJA	40	250	210.0	185.0	35.0
UCD3138RMHR	WQFN	RMH	40	2000	367.0	367.0	38.0
UCD3138RMHT	WQFN	RMH	40	250	210.0	185.0	35.0

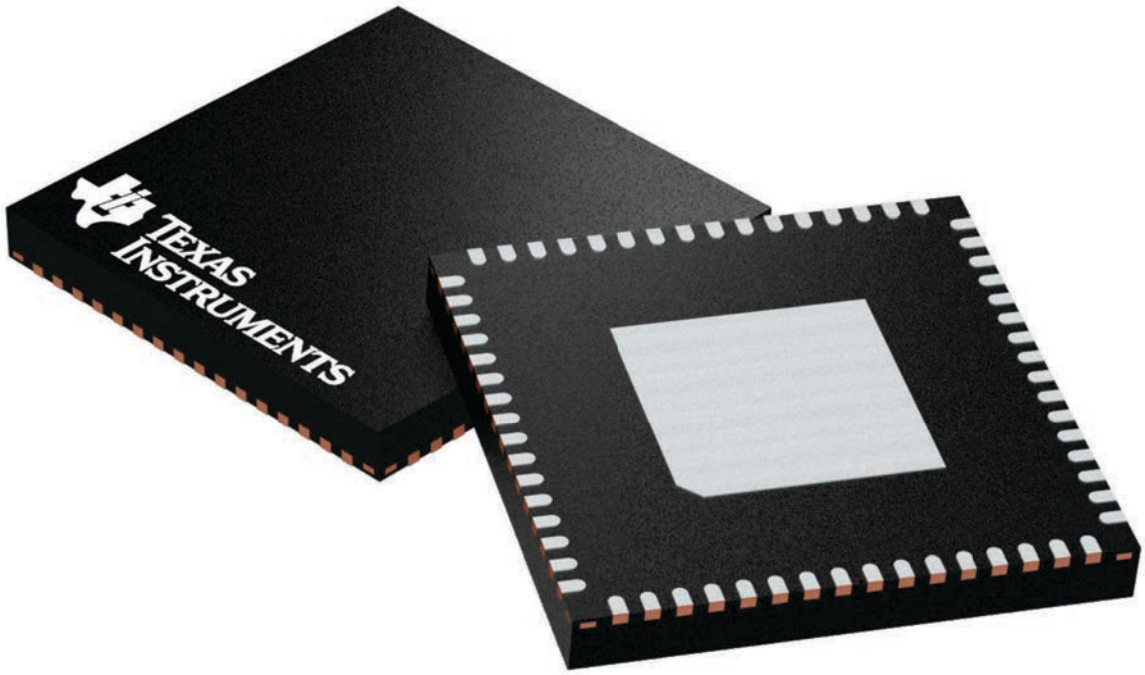
GENERIC PACKAGE VIEW

RGC 64

VQFN - 1 mm max height

9 x 9, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

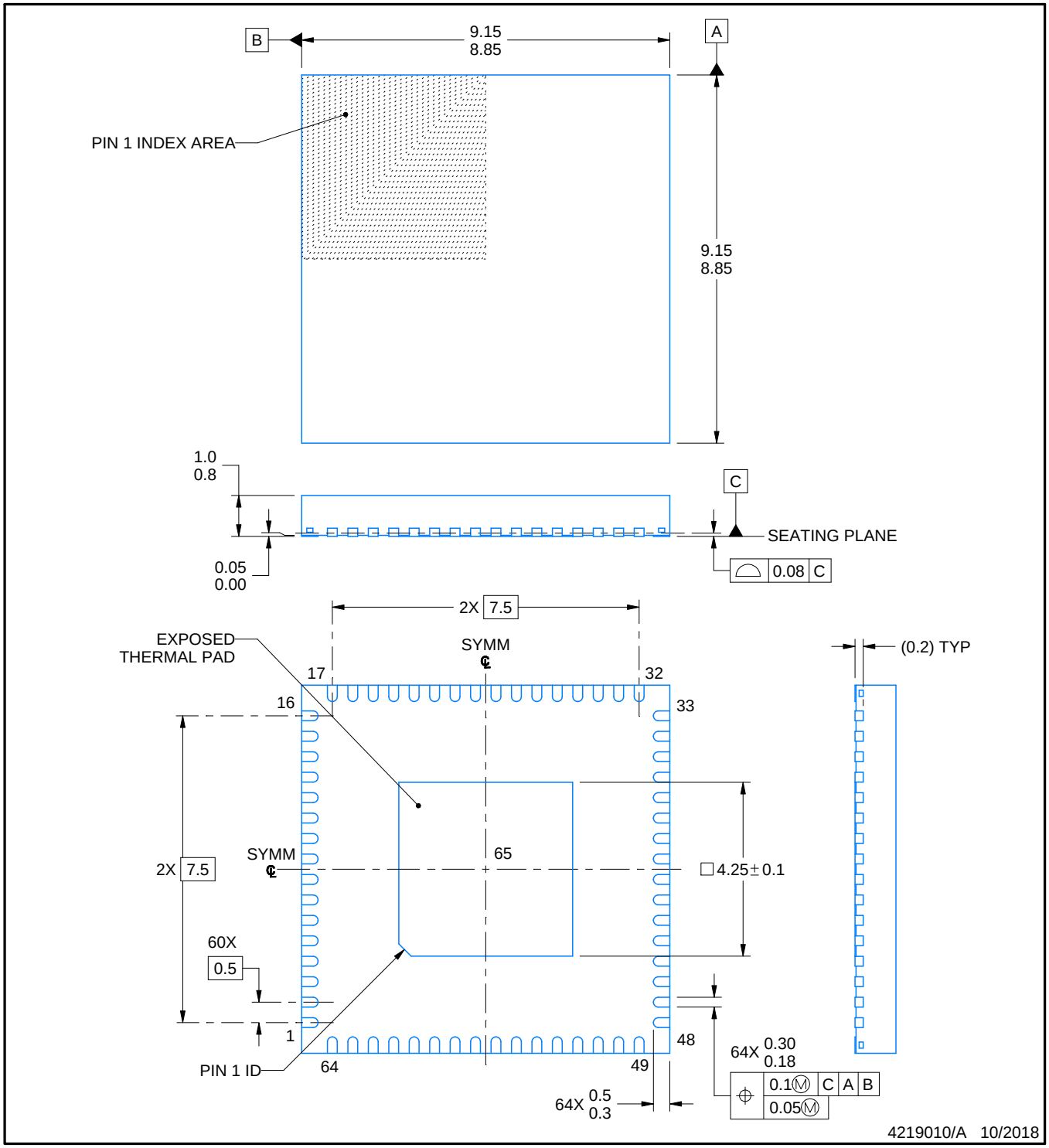
4224597/A

PACKAGE OUTLINE

RGC0064B

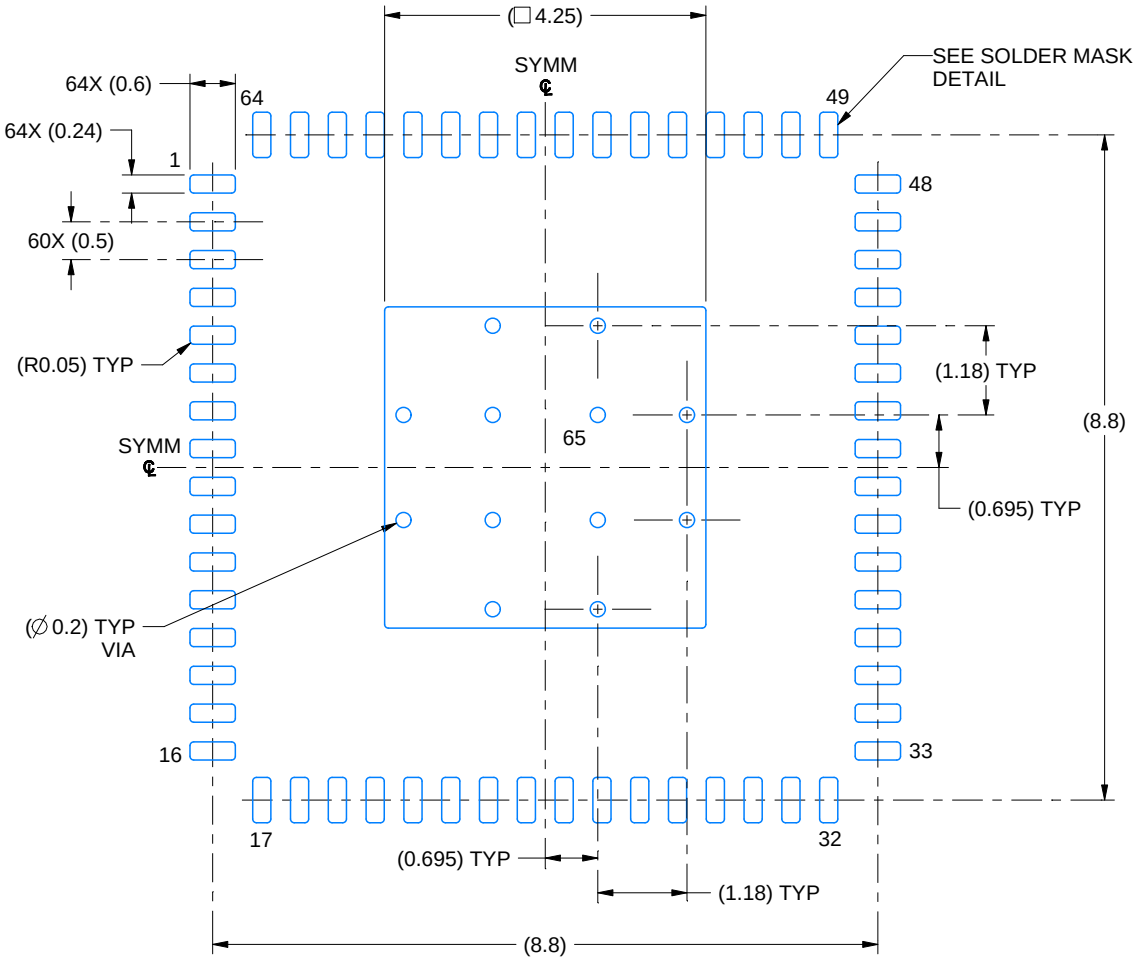
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

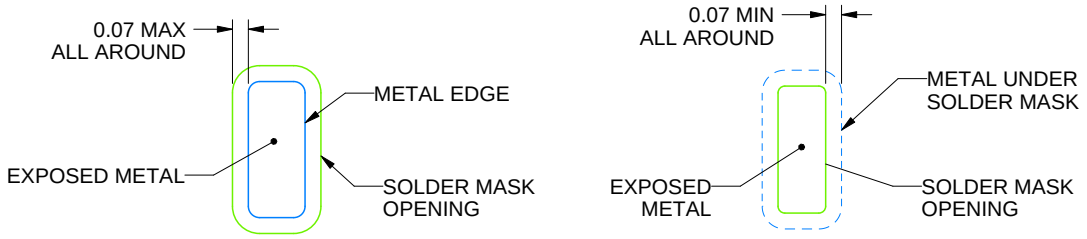


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



NON SOLDER MASK DEFINED (PREFERRED)

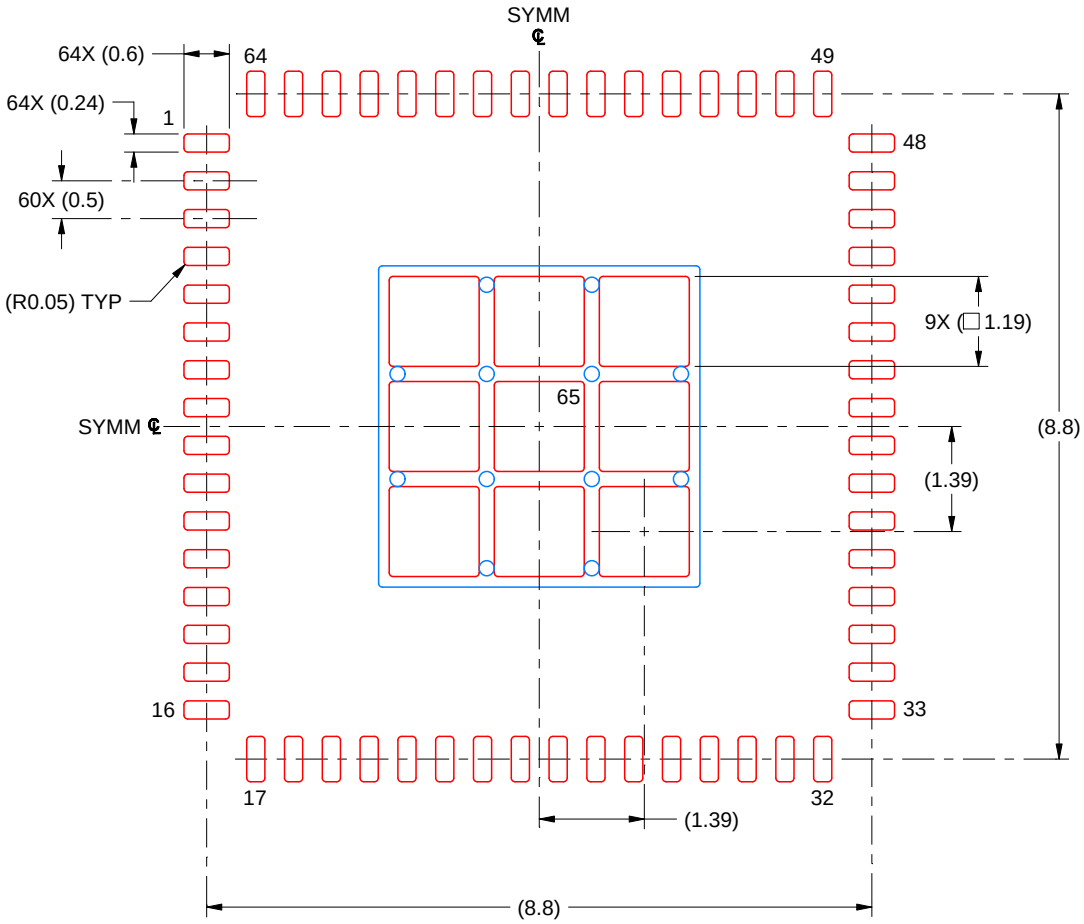
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4219010/A 10/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 65
71% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4219010/A 10/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

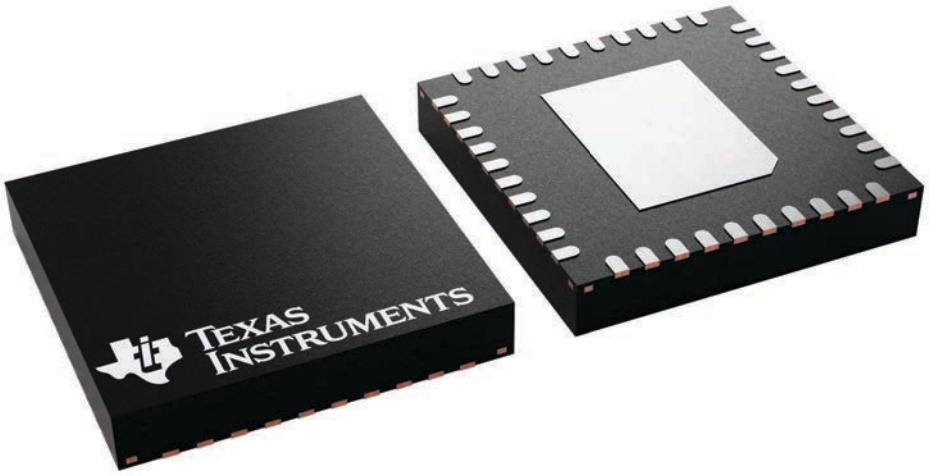
RHA 40

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225870/A

GENERIC PACKAGE VIEW

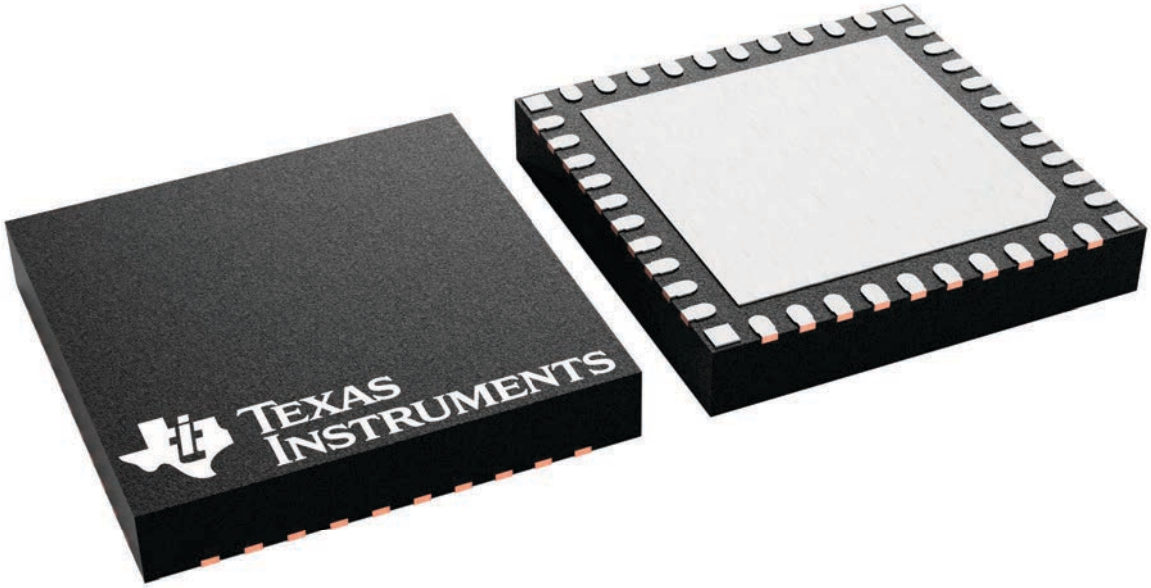
RJA 40

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



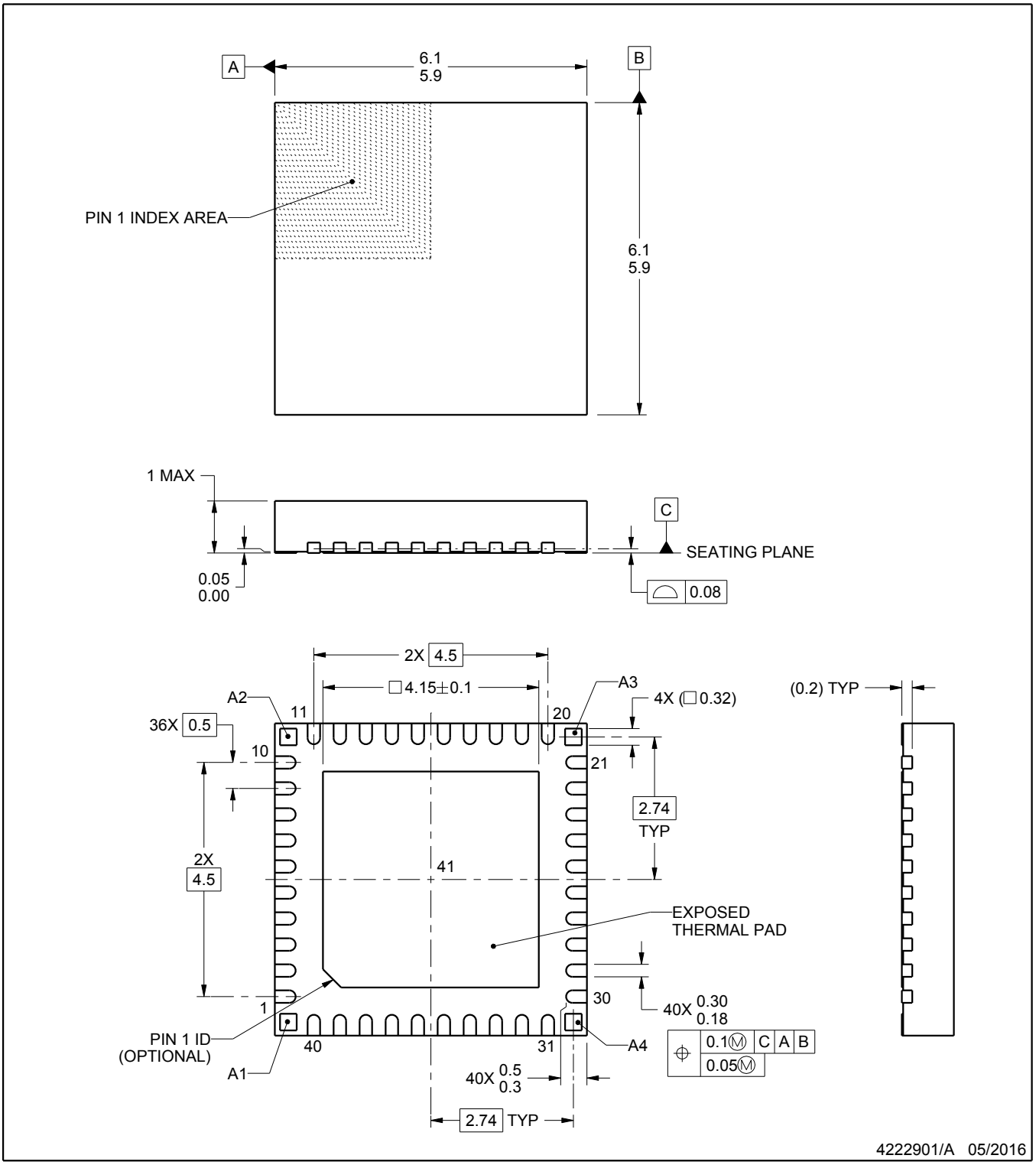
4231077/A

PACKAGE OUTLINE

RJA0040A

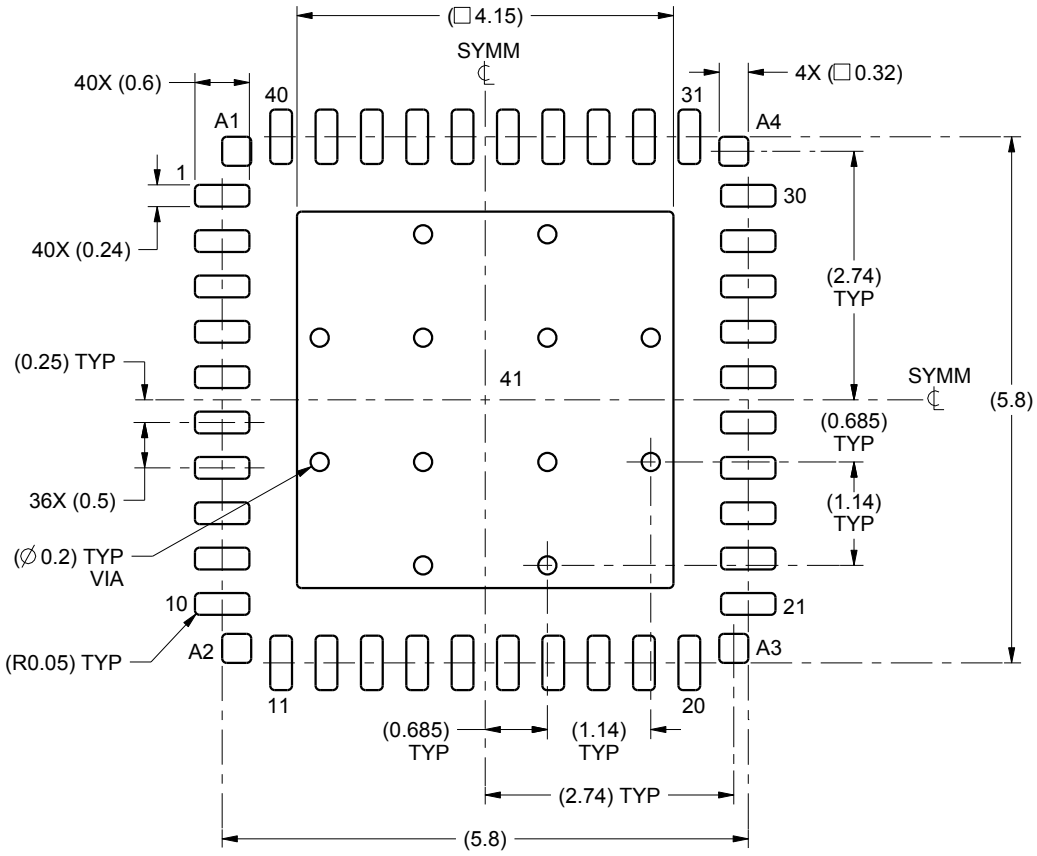
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

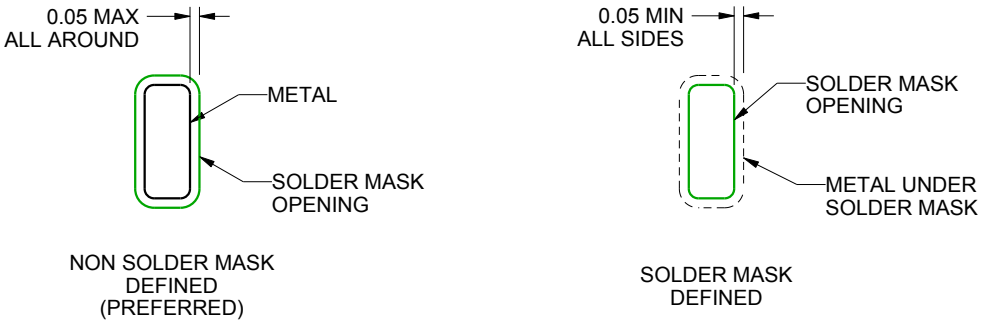


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:12X

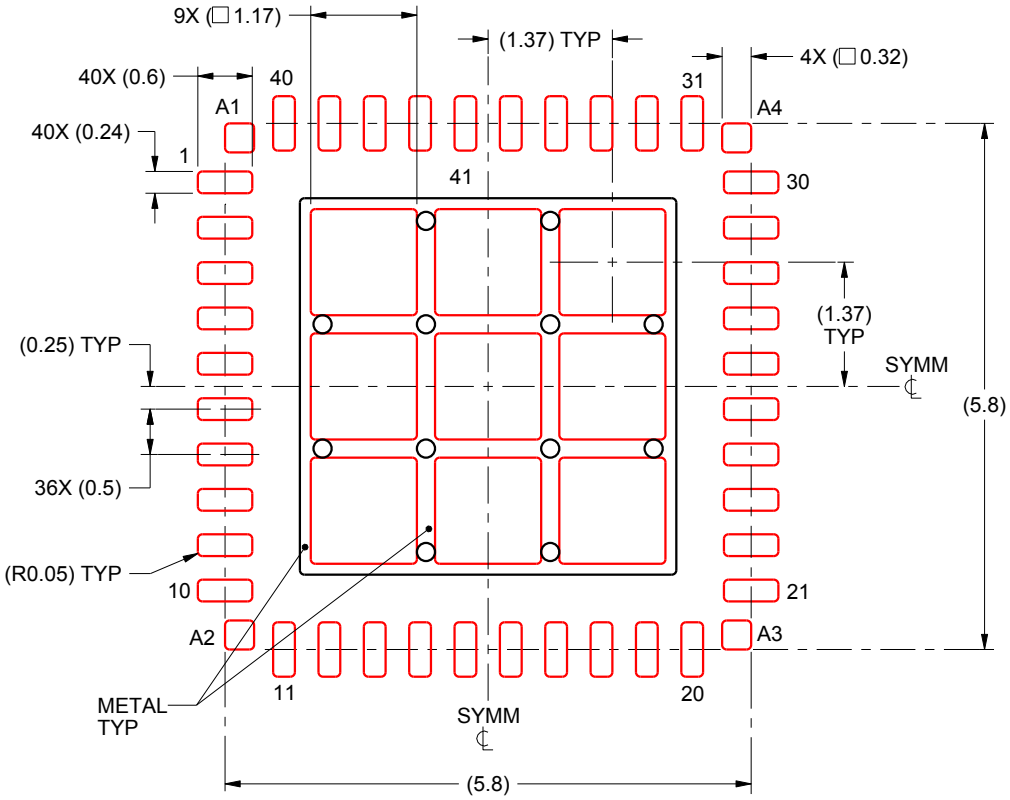


SOLDER MASK DETAILS

4222901/A 05/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 41:
72% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:12X

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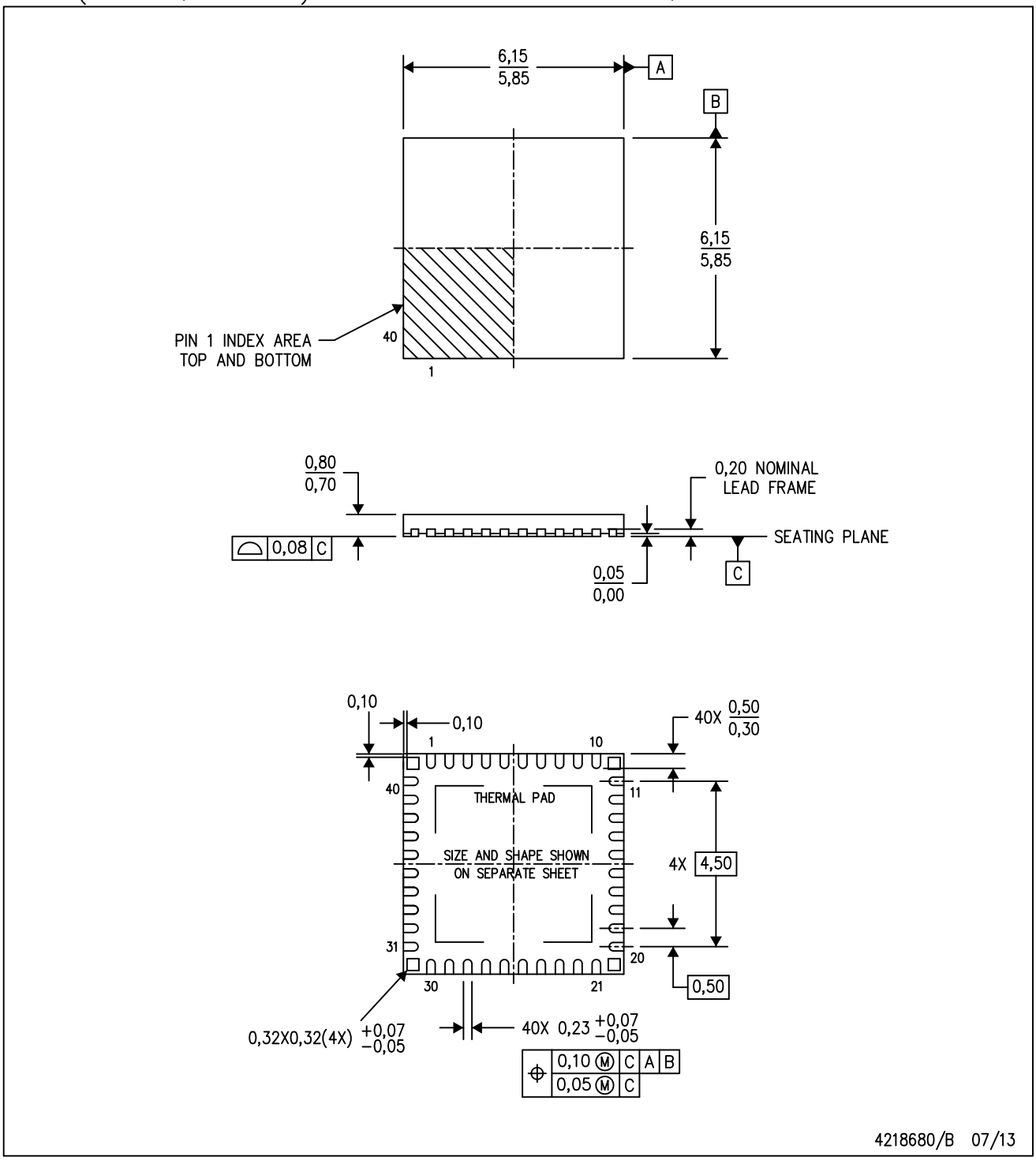
NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

RMH (S–PWQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

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