TEXAS INSTRUMENTS
ADC3244E
JAJSGZ4 – FEBRUARY 2019

ADC3244E デュアル・チャネル、14ビット、125MSPSのA/Dコンバータ

1 特長

- デュアル・チャネル
- 14 ビット分解能
- 単一電源：1.8V
- シリアル LVDS インターフェイス (SLVDS)
- 1、2、4 分周が可能な柔軟性の高い入力クロック・バッファ
- f_{IN} = 70MHz で SNR = 72.4dBFS、SFDR = 87dBc
- 超低消費電力
  - 125MSPS で 116mW/Ch
- チャネル分離：105dB
- ディザおよびチョッパを内蔵
- マルチチップの同期をサポート
- 12 ビット・バージョンとピン互換
- パッケージ：VQFN-48 (7mm × 7mm)
- 拡張温度範囲：-50°C～+105°C

2 アプリケーション

- マルチキャリア、マルチモードのセルラー基地局
- レーダーおよびスマート・アンテナ・アレイ
- 兵器の誘導
- モータ制御の帰還
- ネットワークおよびベクトル解析
- 通信テスト機器
- 非破壊試験
- マイクロ波受信機
- ソフトウェア無線 (SDR)
- 直交およびダイバーシティ無線受信器
- ハンドヘルド無線および測定器

3 概要

ADC3244E は線形性が高く、超低消費電力で、デュアル・チャネル、14 ビット、25MSPS～125MSPS の A/D コンバータ (ADC) です。このデバイスは、広いダイナミック・レンジを必要とする、条件の厳しい高周波の入力信号をサポートするために特に設計されています。入力クロック分周器により、システム・クロック・アーキテクチャを柔軟に設計でき、SYSREF 入力によりシステムの完全な同期を実現できます。

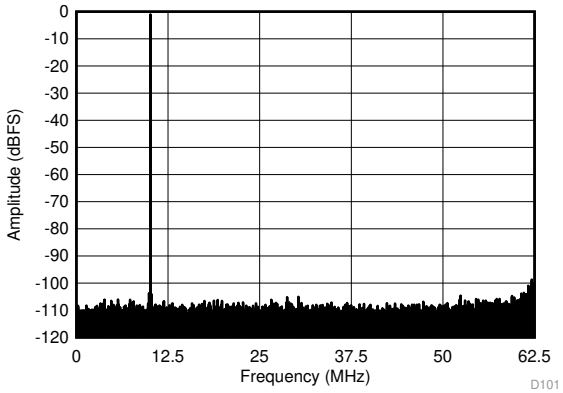
ADC3244E は、インターフェイスの配線数を減らすためにシリアル低電圧差動信号処理 (LVDS) をサポートしています。その結果、システムの集積密度を高めることができます。シリアル LVDS インターフェイスは 2 線式であり、各 ADC からのデータはシリアル化され、2 対の LVDS ペアで出力されます。内蔵のフェーズ・ロック・ループ (PLL) は、入力された ADC サンプリング・クロックを逓倍して、各チャネルの 14 ビットのデータをシリアル化するため使用されるビット・クロックを生成します。シリアル・データ・ストリームに加え、フレームとビット・クロックも LVDS 出力として送信されます。

製品情報(1)

型番	パッケージ	本体サイズ（公称）
ADC3244E	VQFN（48）	7.00mm×7.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にあるパッケージ・オプションについての付録を参照してください。

f_S = 125MSPS、f_{IN} = 10MHz での性能



目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

日付	リビジョン	注
2019 年 2 月	*	初版

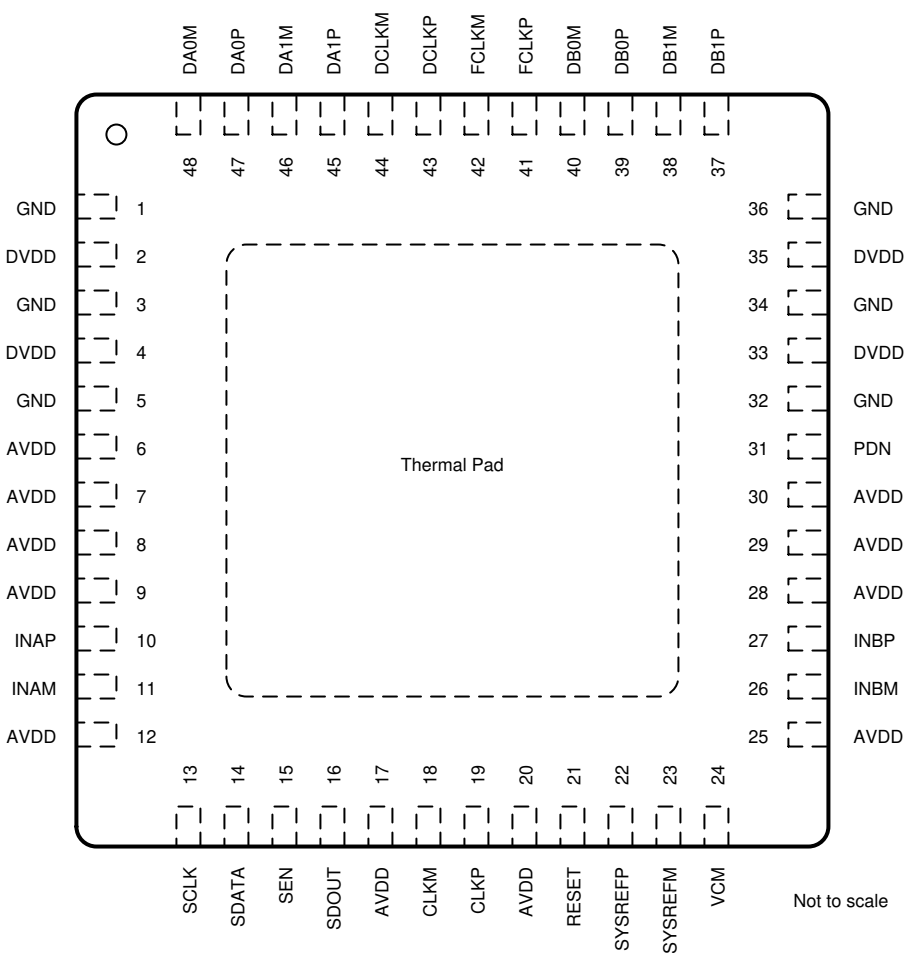
5 Device Comparison Table

INTERFACE	RESOLUTION (Bits)	25 MSPS	50 MSPS	80 MSPS	125 MSPS	160 MSPS
Serial LVDS	12	ADC3221	ADC3222	ADC3223	ADC3224	—
	14	ADC3241	ADC3242	ADC3243	ADC3244	—
		—	—	—	ADC3244E(1)	—
JESD204B	12	—	ADC32J22	ADC32J23	ADC32J24	ADC32J25
	14	—	ADC32J42	ADC32J43	ADC32J44	ADC32J45

(1) The ADC3244E is specified at extended temperature range of –50°C to +105°C. Other devices in the table are specified at standard industrial temperature range of –40°C to +85°C.

6 Pin Configuration and Functions

RGZ Package
48-Pin VQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AVDD	6-9, 12, 17, 20, 25, 28-30	I	Analog 1.8-V power supply
CLKM	18	I	Negative differential clock input for the ADC
CLKP	19	I	Positive differential clock input for the ADC
DA0M	48	O	Negative serial LVDS output for channel A0
DA0P	47	O	Positive serial LVDS output for channel A0
DA1M	46	O	Negative serial LVDS output for channel A1
DA1P	45	O	Positive serial LVDS output for channel A1
DB0M	40	O	Negative serial LVDS output for channel B0
DB0P	39	O	Positive serial LVDS output for channel B0
DB1M	38	O	Negative serial LVDS output for channel B1
DB1P	37	O	Positive serial LVDS output for channel B1
DCLKM	44	O	Negative bit clock output
DCLKP	43	O	Positive bit clock output
DVDD	2, 4, 33, 35	I	Digital 1.8-V power supply
FCLKM	42	O	Negative frame clock output
FCLKP	41	O	Positive frame clock output
GND	1, 3, 5, 32, 34, 36	I	Ground, 0 V
INAM	11	I	Negative differential analog input for channel A
INAP	10	I	Positive differential analog input for channel A
INBM	26	I	Negative differential analog input for channel B
INBP	27	I	Positive differential analog input for channel B
PDN	31	I	Power-down control. This pin can be configured using the SPI. This pin has an internal 150-kΩ pulldown resistor.
RESET	21	I	Hardware reset; active high. This pin has an internal 150-kΩ pulldown resistor.
SCLK	13	I	Serial interface clock input. This pin has an internal 150-kΩ pulldown resistor.
SDATA	14	I	Serial interface data input. This pin has an internal 150-kΩ pulldown resistor.
SDOUT	16	O	Serial interface data output
SEN	15	I	Serial interface enable; active low. This pin has an internal 150-kΩ pullup resistor to AVDD.
SYSREFM	23	I	Negative external SYSREF input
SYSREFP	22	I	Positive external SYSREF input
VCM	24	O	Common-mode voltage for analog inputs
Thermal Pad		I	Thermal pad. Connect to ground.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
	Analog supply voltage, AVDD		–0.3	2.1	V
	Digital supply voltage, DVDD		–0.3	2.1	V
	Voltage applied to input pins	INAP, INBP, INAM, INBM	–0.3	min (1.9, AVDD + 0.3)	V
		CLKP, CLKM	–0.3	AVDD + 0.3	
		SYSREFP, SYSREFM	–0.3	AVDD + 0.3	
		SCLK, SEN, SDATA, RESET, PDN	–0.3	3.9	
T_J	Operating junction temperature			125	ºC
T_{stg}	Storage temperature		–65	150	ºC

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	NOM	MAX	UNIT
SUPPLIES						
AVDD	Analog supply voltage		1.7	1.8	1.9	V
DVDD	Digital supply voltage		1.7	1.8	1.9	V
ANALOG INPUT						
V_{ID}	Differential input voltage	For input frequencies < 450 MHz		2		V_{PP}
		For input frequencies < 600 MHz		1		
V_{IC}	Input common-mode voltage			VCM ± 0.025		V
CLOCK INPUT						
	Input clock frequency(2)	Sampling clock frequency	10		125	MSPS
	Input clock amplitude (differential)	Sine wave, ac-coupled	0.2	1.5		V_{PP}
		LVPECL, ac-coupled		1.6		
		LVDS, ac-coupled		0.7		
	Input clock duty cycle		35%	50%	65%	
	Input clock common-mode voltage			0.95		V
DIGITAL OUTPUTS						
C_{LOAD}	Maximum external load capacitance from each output pin to GND			3.3		pF
R_{LOAD}	Differential load resistance placed externally			100		Ω
TEMPERATURE						
T_A	Operating free-air temperature		–50		105	°C

(1) After power-up, to reset the device for the first time, only use the RESET pin; see the *Register Initialization* section.
(2) With the clock divider enabled by default for divide-by-1. Maximum sampling clock frequency for the divide-by-4 option is 500 MSPS.

7.4 Thermal Information

THERMAL METRIC[1]		ADC3244E RGZ (VQFN) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	25.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	18.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	3.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics: General

typical values at T_A = 25°C, ADC sampling rate = 125 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input (unless otherwise noted); minimum and maximum values at full temperature range of –50°C to +105°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	ADC clock frequency				125	MSPS
	1.8-V analog supply current			65	106	mA
	1.8-V digital supply current			64	95	mA
	Total power dissipation			233	325	mW
	Global power-down dissipation			5	17	mW
	Standby power-down dissipation			78	103	mW
RESOLUTION						
	Resolution		14			Bits
ANALOG INPUT						
	Differential input full-scale			2.0		V_{PP}
R_{IN}	Input resistance	Differential at dc		6.6		kΩ
C_{IN}	Input capacitance	Differential at dc		3.7		pF
$V_{OC(VCM)}$	VCM common-mode voltage output			0.95		V
	VCM output current capability			10		mA
	Input common-mode current	Per analog input pin		1.5		µA/MSPS
	Analog input bandwidth (3 dB)	50-Ω differential source driving 50-Ω termination across INP and INM		540		MHz
DC ACCURACY						
E_O	Offset error		–25		25	mV
α_{EO}	Temperature coefficient of offset error			±0.024		°C
$E_{G(REF)}$	Gain error as a result of internal reference inaccuracy alone		–2		2	%FS
$E_{G(CHAN)}$	Gain error of channel alone			–2		%FS
$\alpha_{(EGCHAN)}$	Temperature coefficient of $E_{G(CHAN)}$			±0.008		Δ%FS/°C
CHANNEL-TO-CHANNEL ISOLATION						
	Crosstalk[1]	f_{IN} = 10 MHz		105		dB
		f_{IN} = 100 MHz		105		
		f_{IN} = 200 MHz		105		
		f_{IN} = 230 MHz		105		
		f_{IN} = 300 MHz		105		

(1) Crosstalk is measured with a –1-dBFS input signal on one channel and no input on the other channel.

7.6 Electrical Characteristics: AC Performance

typical values at T_A = 25°C, ADC sampling rate = 125 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input (unless otherwise noted); minimum and maximum values at full temperature range of –50°C to +105°C

PARAMETER		TEST CONDITIONS	f_S = 125 MSPS						UNIT
			DITHER ON			DITHER OFF			
			MIN	TYP	MAX	MIN	TYP	MAX	
DYNAMIC AC CHARACTERISTICS									
SNR	Signal-to-noise ratio (from 1-MHz offset)	f_{IN} = 10 MHz		72.9			73.3		dBFS
		f_{IN} = 70 MHz	71	72.6			73		
		f_{IN} = 100 MHz		72.4			72.8		
		f_{IN} = 170 MHz		71.7			72.2		
		f_{IN} = 230 MHz		71			71.6		
	Signal-to-noise ratio (full Nyquist band)	f_{IN} = 10 MHz		72.5			72.9		
		f_{IN} = 70 MHz		72.2			72.6		
		f_{IN} = 100 MHz		72.1			72.5		
		f_{IN} = 170 MHz		71.4			71.9		
		f_{IN} = 230 MHz		70.7			71.3		
NSD(1)	Noise spectral density (averaged across Nyquist zone)	f_{IN} = 10 MHz		–150.8			–151.1		dBFS/Hz
		f_{IN} = 70 MHz		–150.5	–148.9		–150.9		
		f_{IN} = 100 MHz		–150.3			–150.7		
		f_{IN} = 170 MHz		–149.6			–150.1		
		f_{IN} = 230 MHz		–148.9			–149.5		
SINAD(1)	Signal-to-noise and distortion ratio	f_{IN} = 10 MHz		72.8			73		dBFS
		f_{IN} = 70 MHz	69.6	72.6			72.9		
		f_{IN} = 100 MHz		72.3			72.5		
		f_{IN} = 170 MHz		71.5			71.9		
		f_{IN} = 230 MHz		70.7			71.1		
ENOB(1)	Effective number of bits	f_{IN} = 10 MHz		11.8			11.8		Bits
		f_{IN} = 70 MHz	11.3	11.8			11.8		
		f_{IN} = 100 MHz		11.7			11.8		
		f_{IN} = 170 MHz		11.6			11.6		
		f_{IN} = 230 MHz		11.5			11.5		
SFDR	Spurious-free dynamic range	f_{IN} = 10 MHz		93			86		dBc
		f_{IN} = 70 MHz	82	94			89		
		f_{IN} = 100 MHz		89			85		
		f_{IN} = 170 MHz		85			85		
		f_{IN} = 230 MHz		83			82		

(1) Reported from a 1-MHz offset.

Electrical Characteristics: AC Performance (continued)

typical values at T_A = 25°C, ADC sampling rate = 125 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input (unless otherwise noted); minimum and maximum values at full temperature range of –50°C to +105°C

PARAMETER		TEST CONDITIONS	f_S = 125 MSPS						UNIT
			DITHER ON			DITHER OFF			
			MIN	TYP	MAX	MIN	TYP	MAX	
HD2	Second-order harmonic distortion	f_{IN} = 10 MHz		95			96		dBc
		f_{IN} = 70 MHz	82	96			95		
		f_{IN} = 100 MHz		91			90		
		f_{IN} = 170 MHz		85			85		
		f_{IN} = 230 MHz		83			83		
HD3	Third-order harmonic distortion	f_{IN} = 10 MHz		94			86		dBc
		f_{IN} = 70 MHz	83	94			89		
		f_{IN} = 100 MHz		91			85		
		f_{IN} = 170 MHz		97			89		
		f_{IN} = 230 MHz		87			85		
Non HD2, HD3	Spurious-free dynamic range (excluding HD2, HD3)	f_{IN} = 10 MHz		100			95		dBc
		f_{IN} = 70 MHz	86	99			95		
		f_{IN} = 100 MHz		99			95		
		f_{IN} = 170 MHz		100			91		
		f_{IN} = 230 MHz		96			92		
THD	Total harmonic distortion	f_{IN} = 10 MHz		91			85		dBc
		f_{IN} = 70 MHz	76	91			86		
		f_{IN} = 100 MHz		87			83		
		f_{IN} = 170 MHz		84			82		
		f_{IN} = 230 MHz		81			80		
IMD3	Two-tone, third-order intermodulation distortion	f_{IN1} = 45 MHz, f_{IN2} = 50 MHz		–97			–95		dBFS
		f_{IN1} = 185 MHz, f_{IN2} = 190 MHz		–91			–90		

7.7 Digital Characteristics

dc specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level of 0 or 1, AVDD = DVDD = 1.8 V, and –1-dBFS differential input (unless otherwise noted)

)PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS (RESET, SCLK, SDATA, SEN, PDN)							
V_{IH}	High-level input voltage		All digital inputs support 1.8-V and 3.3-V CMOS logic levels	1.3			V
V_{IL}	Low-level input voltage		All digital inputs support 1.8-V and 3.3-V CMOS logic levels			0.4	V
I_{IH}	High-level input current	RESET, SDATA, SCLK, PDN	V_{HIGH} = 1.8 V		10		µA
		SEN(1)	V_{HIGH} = 1.8 V		0		
I_{IL}	Low-level input current	RESET, SDATA, SCLK, PDN	V_{LOW} = 0 V		0		µA
		SEN	V_{LOW} = 0 V		10		
DIGITAL INPUTS (SYSREFP, SYSREFM)							
V_{IH}	High-level input voltage				1.3		V
V_{IL}	Low-level input voltage				0.5		V
	Common-mode voltage for SYSREF				0.9		V
DIGITAL OUTPUTS, CMOS INTERFACE (SDOUT)							
V_{OH}	High-level output voltage			DVDD – 0.1	DVDD		V
V_{OL}	Low-level output voltage				0	0.1	V
DIGITAL OUTPUTS, LVDS INTERFACE							
V_{ODH}	High-level output differential voltage		With an external 100-Ω termination	280	410	460	mV
V_{ODL}	Low-level output differential voltage		With an external 100-Ω termination	–460	–410	–280	mV
V_{OCM}	Output common-mode voltage				1.05		V

(1) SEN has an internal 150-kΩ pull-up resistor to AVDD. Because the pull-up resistor is weak, SEN can also be driven by 1.8-V or 3.3-V CMOS buffers.

7.8 Timing Requirements: General

typical values at T_A = 25°C, AVDD = DVDD = 1.8 V, and –1-dBFS differential input (unless otherwise noted); minimum and maximum values at full temperature range of –50°C to +105°C

			MIN	TYP	MAX	UNIT
t_A	Aperture delay		1.24	1.44	1.64	ns
	Aperture delay matching between two channels of the same device			±70		ps
	Variation of aperture delay between two devices at the same temperature and supply voltage			±150		ps
t_J	Aperture jitter			130		f_S rms
	Wake-up time	Time to valid data after exiting standby power-down mode		35	65	µs
		Time to valid data after exiting global power-down mode (in this mode, both channels power down)		85	140	
	ADC latency(1)	2-wire mode (default)		9		Clock cycles
		1-wire mode		8		
t_{SU_SYSREF}	SYSREF reference setup time	Setup time for SYSREF referenced to input clock rising edge	1000			ps
t_{H_SYSREF}	SYSREF reference hold time	Hold time for SYSREF referenced to input clock rising edge	100			

(1) Overall latency = ADC latency + t_{PDI}.

7.9 Timing Requirements: LVDS Output

typical values at 25°C, AVDD = DVDD = 1.8 V, –1-dBFS differential input, 7x serialization, C_{LOAD} = 3.3 pF(1), and R_{LOAD} = 100 Ω(2) (unless otherwise noted); minimum and maximum values at full temperature range of –50°C to +105°C(3)(4)

			MIN	TYP	MAX	UNIT
t_{SU}	Data setup time: data valid to zero-crossing of differential output clock (CLKOUTP – CLKOUTM)(5)		0.36	0.42		ns
t_{HO}	Data hold time: zero-crossing of differential output clock (CLKOUTP – CLKOUTM) to data becoming invalid(5)		0.36	0.47		ns
	LVDS bit clock duty cycle: duty cycle of differential clock (CLKOUTP – CLKOUTM)			49%		
t_{PDI}	Clock propagation delay: input clock falling edge cross-over to frame clock rising edge cross-over 10 MSPS < sampling frequency < 125 MSPS	1-wire mode	2.7	4.5	6.5	ns
		2-wire mode	0.44 × t_S + t_{DELAY}			
t_{DELAY}	Delay time		3	4.5	5.9	ns
t_{FALL}, t_{RISE}	Data fall time, data rise time: rise time measured from –100 mV to 100 mV, *10 MSPS ≤ Sampling frequency ≤ 125 MSPS*			0.11		ns
$t_{CLKRISE}$, $t_{CLKFALL}$	Output clock rise time, output clock fall time: rise time measured from –100 mV to 100 mV, *10 MSPS ≤ Sampling frequency ≤ 125 MSPS*			0.11		ns

(1) C_{LOAD} is the effective external single-ended load capacitance between each output pin and ground
(2) R_{LOAD} is the differential load resistance between the LVDS output pair.
(3) Measurements are done with a transmission line of a 100-Ω characteristic impedance between the device and load. Setup and hold time specifications take into account the effect of jitter on the output data and clock.
(4) Timing parameters are specified by design and characterization and are not tested in production.
(5) Data valid refers to a logic high of +100 mV and a logic low of –100 mV.

Table 1. LVDS Timings at Lower Sampling Frequencies: 7x Serialization (2-Wire Mode)

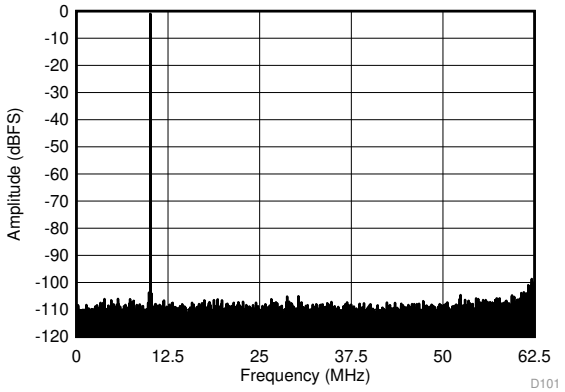
SAMPLING FREQUENCY (MSPS)	SETUP TIME (t_{SU}, ns)			HOLD TIME (t_{HO}, ns)		
	MIN	TYP	MAX	MIN	TYP	MAX
25	2.27	2.6		2.41	2.6	
40	1.44	1.6		1.51	1.7	
50	1.2	1.32		1.24	1.4	
60	0.95	1.04		0.97	1.09	
80	0.68	0.75		0.72	0.81	
100	0.5	0.57		0.53	0.62	

Table 2. LVDS Timings at Lower Sampling Frequencies: 14x Serialization (1-Wire Mode)

SAMPLING FREQUENCY (MSPS)	SETUP TIME (t_{SU}, ns)			HOLD TIME (t_{HO}, ns)		
	MIN	TYP	MAX	MIN	TYP	MAX
25	1.1	1.24		1.19	1.34	
40	0.66	0.72		0.74	0.82	
50	0.48	0.55		0.54	0.64	
60	0.35	0.41		0.42	0.51	
80	0.17	0.24		0.3	0.38	

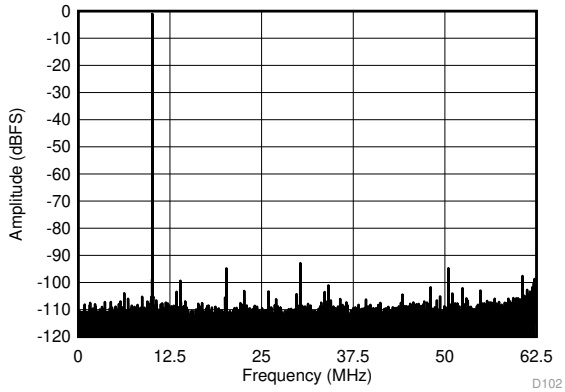
7.10 Typical Characteristics

typical values at T_A = 25°C, ADC sampling rate = 125 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from f_S / 2 when chopper is enabled (unless otherwise noted)



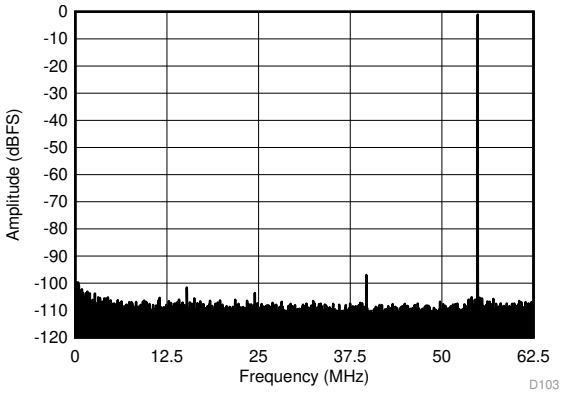
SFDR = 102.6 dBc, SNR = 72.9 dBFS, SINAD = 72.8 dBFS, THD = 99.8 dBc, HD2 = –108.6 dBc, HD3 = –104.0 dBc

図 1. FFT for 10-MHz Input Signal (Chopper On, Dither On)



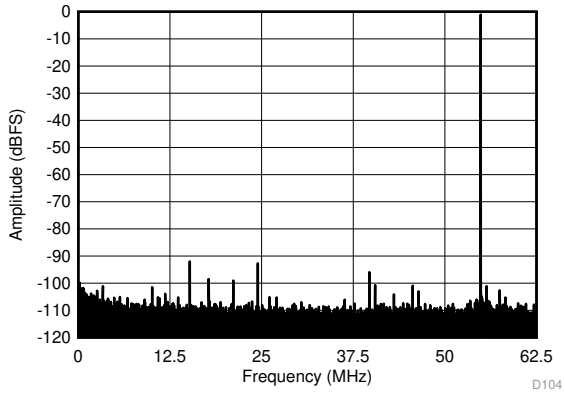
SFDR = 91.8 dBc, SNR = 73.5 dBFS, SINAD = 73.4 dBFS, THD = 87.3 dBc, HD2 = –93.8 dBc, HD3 = –91.8 dBc

図 2. FFT for 10-MHz Input Signal (Chopper On, Dither Off)



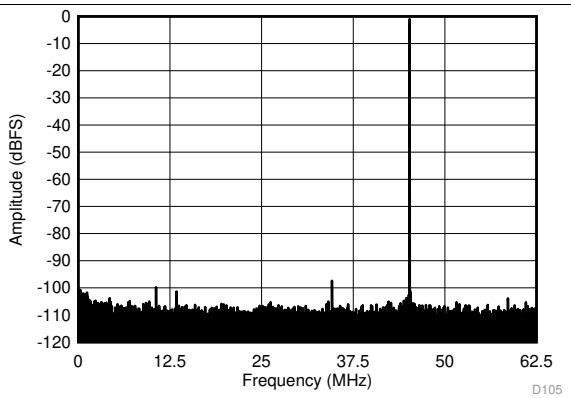
SFDR = 95.9 dBc, SNR = 72.7 dBFS, SINAD = 72.7 dBFS, THD = 93.6 dBc, HD2 = –100.6 dBc, HD3 = –95.9 dBc

図 3. FFT for 70-MHz Input Signal (Dither On)



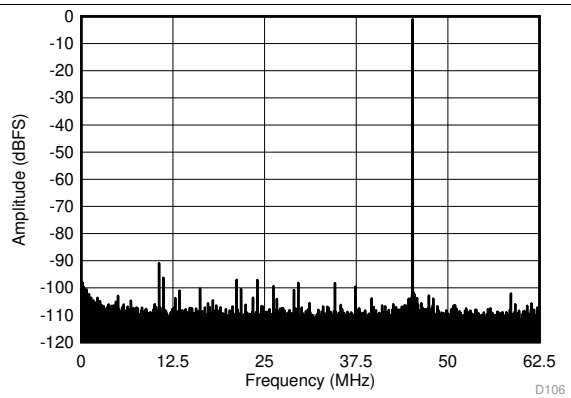
SFDR = 90.9 dBc, SNR = 73.3 dBFS, SINAD = 73.1 dBFS, THD = 87 dBc, HD2 = –90.9 dBc, HD3 = –94.9 dBc

図 4. FFT for 70-MHz Input Signal (Dither Off)



SFDR = 96.4 dBc, SNR = 72.1 dBFS, SINAD = 72.0 dBFS, THD = 92.6 dBc, HD2 = –96.4 dBc, HD3 = –98.8 dBc

図 5. FFT for 170-MHz Input Signal (Dither On)

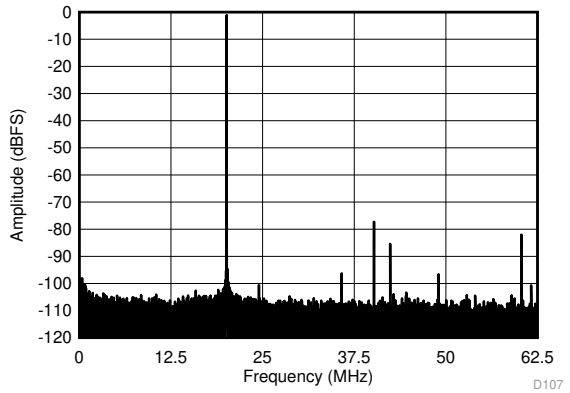


SFDR = 89.9 dBc, SNR = 72.8 dBFS, SINAD = 72.6 dBFS, THD = 87.1 dBc, HD2 = –97.2 dBc, HD3 = –89.9 dBc

図 6. FFT for 170-MHz Input Signal (Dither Off)

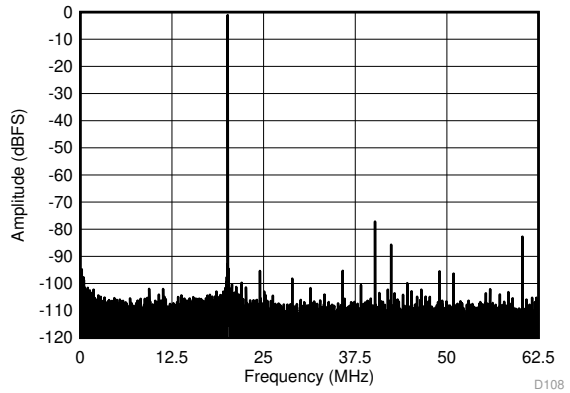
Typical Characteristics (continued)

typical values at T_A = 25°C, ADC sampling rate = 125 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from f_S / 2 when chopper is enabled (unless otherwise noted)



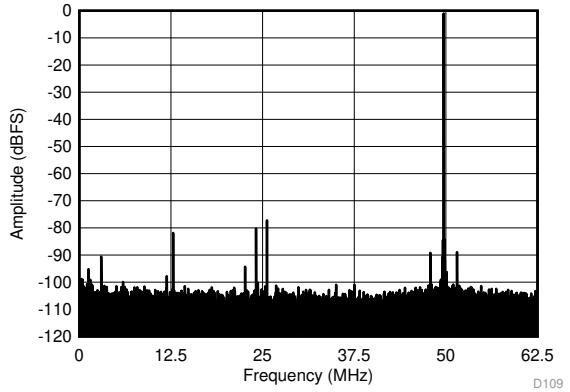
SFDR = 76.1 dBc, SNR = 70.8 dBFS, SINAD = 69.8 dBFS, THD = 74.8 dBc, HD2 = –76.1 dBc, HD3 = –80.9 dBc

図 7. FFT for 270-MHz Input Signal (Dither On)



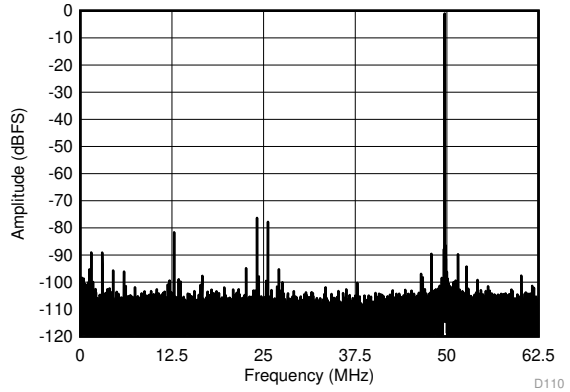
SFDR = 76.1 dBc, SNR = 71.2 dBFS, SINAD = 70.2 dBFS, THD = 74.9 dBc, HD2 = –76.1 dBc, HD3 = –81.6 dBc

図 8. FFT for 270-MHz Input Signal (Dither Off)



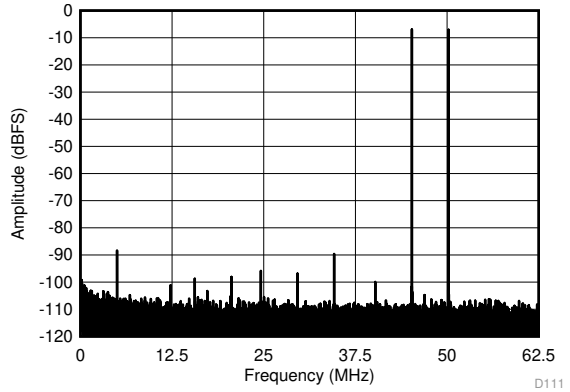
SFDR = 76.2 dBc, SNR = 68.3 dBFS, SINAD = 67.5 dBFS, THD = 74.3 dBc, HD2 = –76.2 dBc, HD3 = –79.2 dBc

図 9. FFT for 450-MHz Input Signal (Dither On)



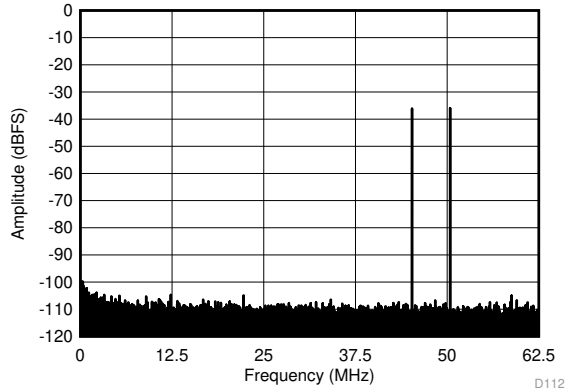
SFDR = 75.3 dBc, SNR = 69.1 dBFS, SINAD = 67.8 dBFS, THD = 72.7 dBc, HD2 = –76.7 dBc, HD3 = –75.3 dBc

図 10. FFT for 450-MHz Input Signal (Dither Off)



f_{IN1} = 46 MHz, f_{IN2} = 50 MHz, IMD3 = 88.3 dBFS, each tone at –7 dBFS

図 11. FFT for Two-Tone Input Signal

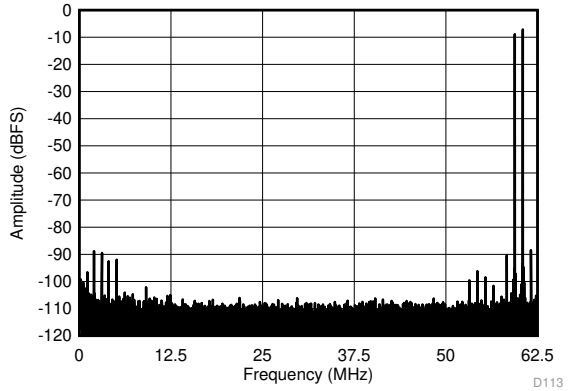


f_{IN1} = 46 MHz, f_{IN2} = 50 MHz, IMD3 = 90.8 dBFS, each tone at –36 dBFS

図 12. FFT for Two-Tone Input Signal

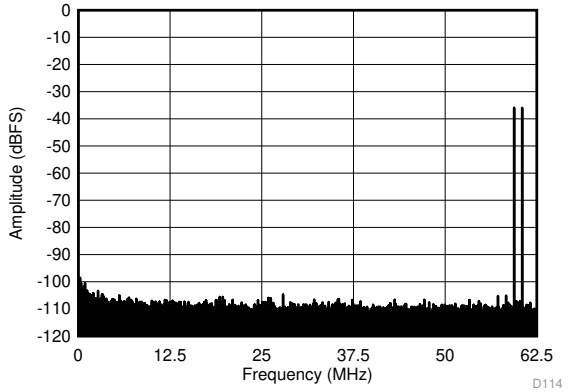
Typical Characteristics (continued)

typical values at T_A = 25°C, ADC sampling rate = 125 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from f_S / 2 when chopper is enabled (unless otherwise noted)



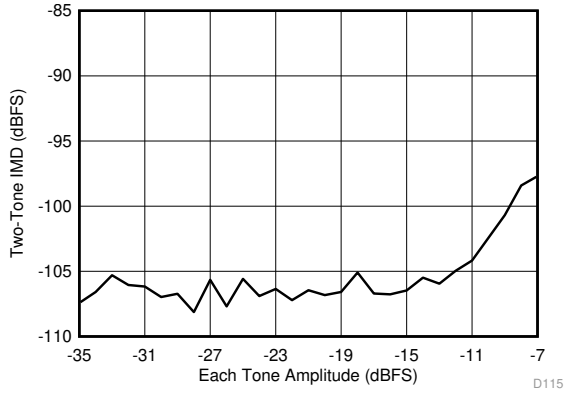
f_{IN1} = 185 MHz, f_{IN2} = 190 MHz, IMD3 = 86.4 dBFS, each tone at –7 dBFS

図 13. FFT for Two-Tone Input Signal



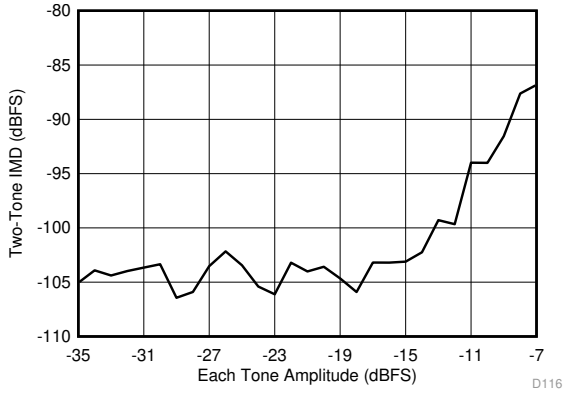
f_{IN1} = 185 MHz, f_{IN2} = 190 MHz, IMD3 = 87.28 dBFS, each tone at –36 dBFS

図 14. FFT for Two-Tone Input Signal



f_{IN1} = 46 MHz, f_{IN2} = 50 MHz

図 15. Intermodulation Distortion vs Input Amplitude



f_{IN1} = 185 MHz, f_{IN2} = 190 MHz

図 16. Intermodulation Distortion vs Input Amplitude

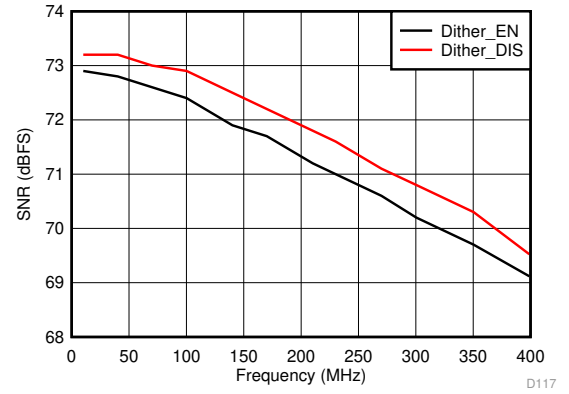


図 17. Signal-to-Noise Ratio vs Input Frequency

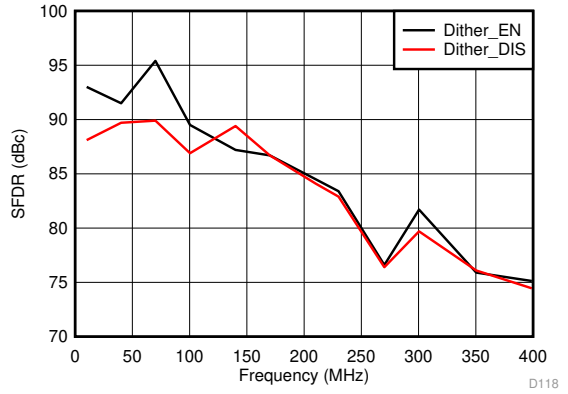
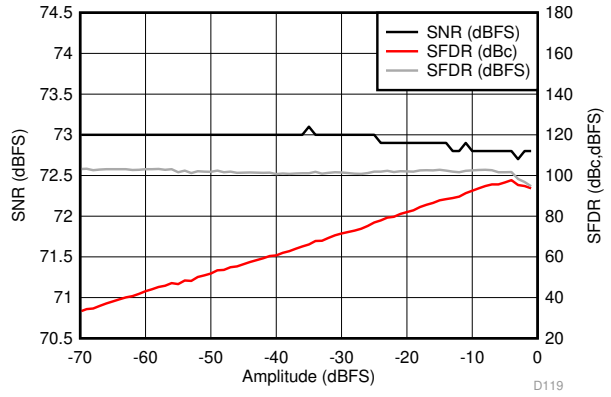


図 18. Spurious-Free Dynamic Range vs Input Frequency

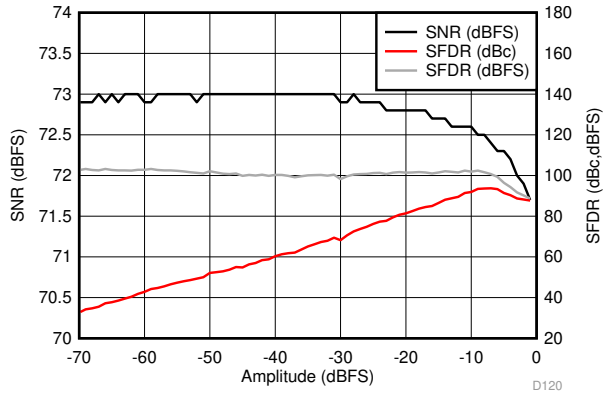
Typical Characteristics (continued)

typical values at T_A = 25°C, ADC sampling rate = 125 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from f_S / 2 when chopper is enabled (unless otherwise noted)



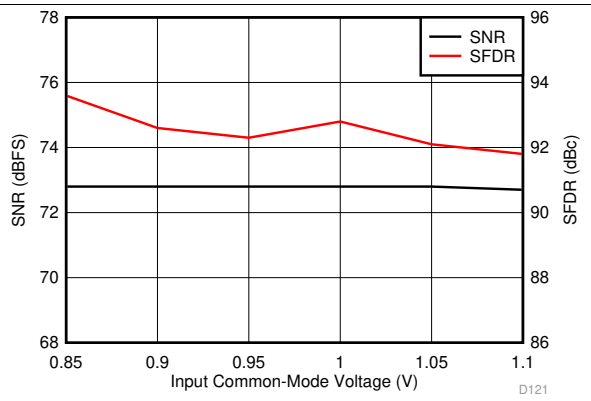
f_{IN} = 30 MHz

図 19. Performance vs Input Amplitude



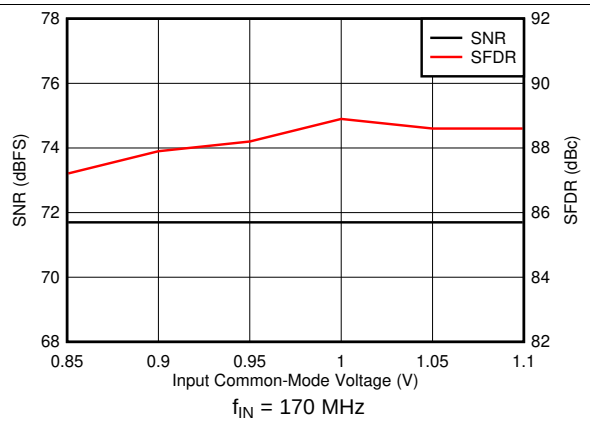
f_{IN} = 170 MHz

図 20. Performance vs Input Amplitude



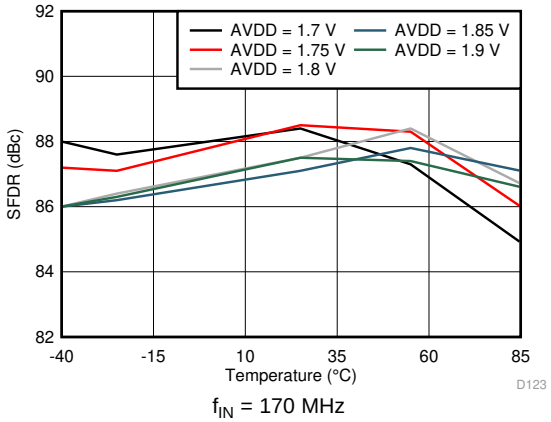
f_{IN} = 30 MHz

図 21. Performance vs Input Common-Mode Voltage



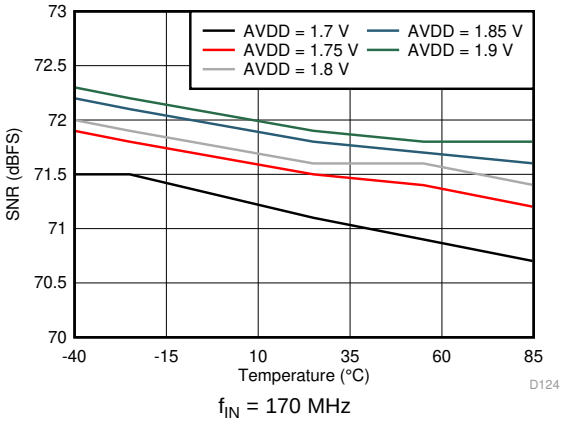
f_{IN} = 170 MHz

図 22. Performance vs Input Common-Mode Voltage



f_{IN} = 170 MHz

図 23. Spurious-Free Dynamic Range vs AVDD Supply and Temperature

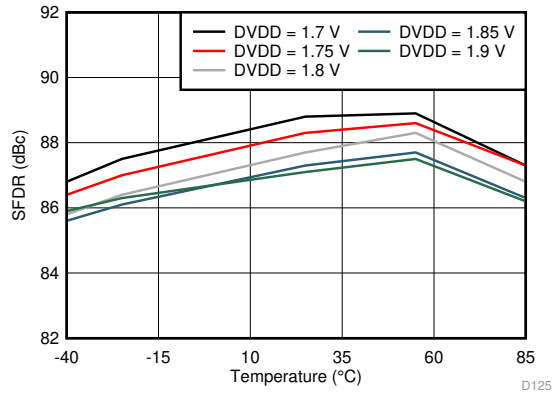


f_{IN} = 170 MHz

図 24. Signal-to-Noise Ratio vs AVDD Supply and Temperature

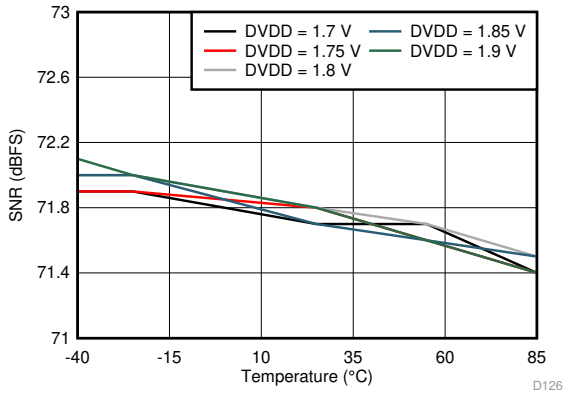
Typical Characteristics (continued)

typical values at T_A = 25°C, ADC sampling rate = 125 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from f_S / 2 when chopper is enabled (unless otherwise noted)



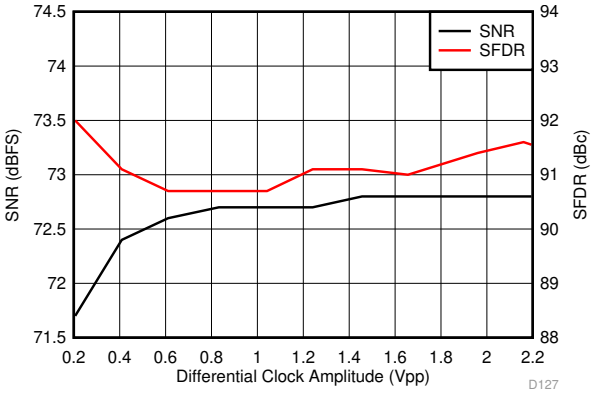
f_{IN} = 170 MHz

図 25. Spurious-Free Dynamic Range vs DVDD Supply and Temperature



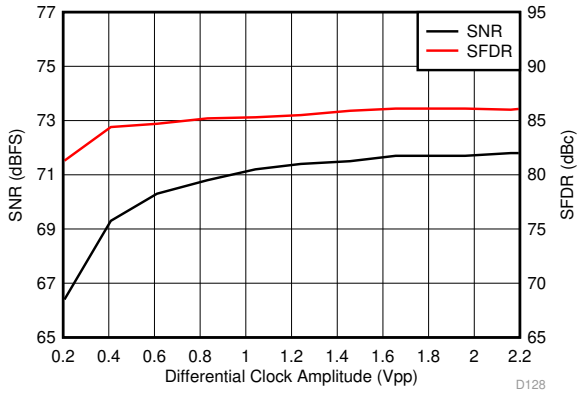
f_{IN} = 170 MHz

図 26. Signal-to-Noise Ratio vs DVDD Supply and Temperature



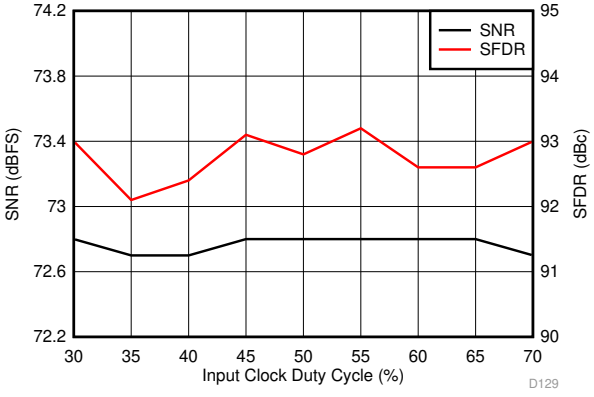
f_{IN} = 40 MHz

図 27. Performance vs Clock Amplitude



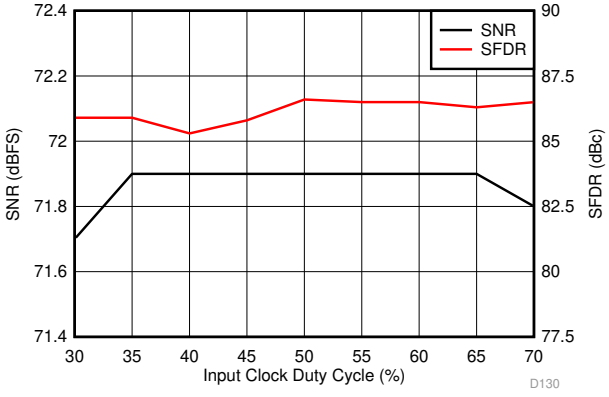
f_{IN} = 150 MHz

図 28. Performance vs Clock Amplitude



f_{IN} = 30 MHz

図 29. Performance vs Clock Duty Cycle

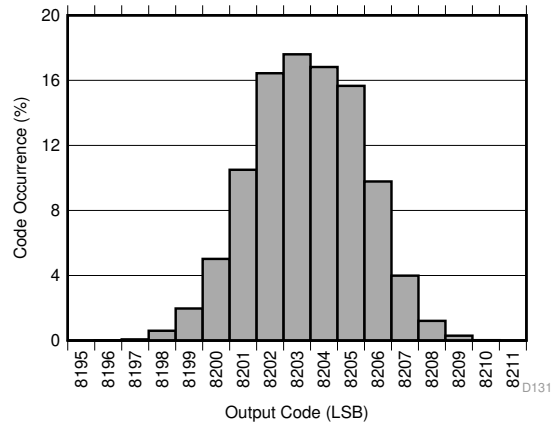


f_{IN} = 150 MHz

図 30. Performance vs Clock Duty Cycle

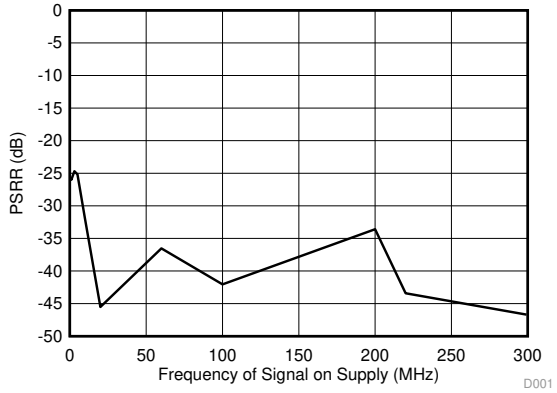
Typical Characteristics (continued)

typical values at T_A = 25°C, ADC sampling rate = 125 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from f_S / 2 when chopper is enabled (unless otherwise noted)



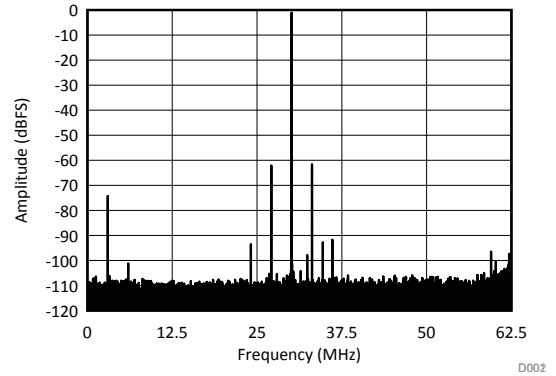
RMS Noise = 1.4 LSBs

図 31. Idle Channel Histogram



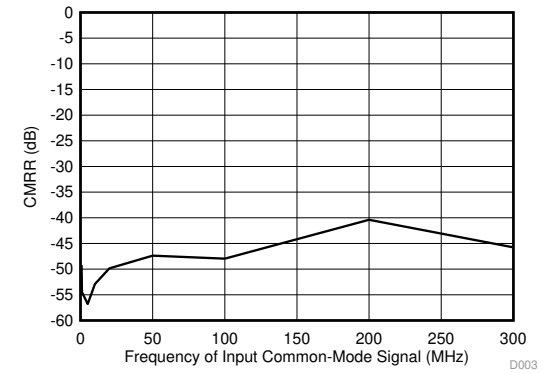
f_{IN} = 30 MHz, A_{IN} = –1 dBFS,
test signal amplitude = 50 mV_{PP}

図 32. Power-Supply Rejection Ratio vs Test Signal Frequency



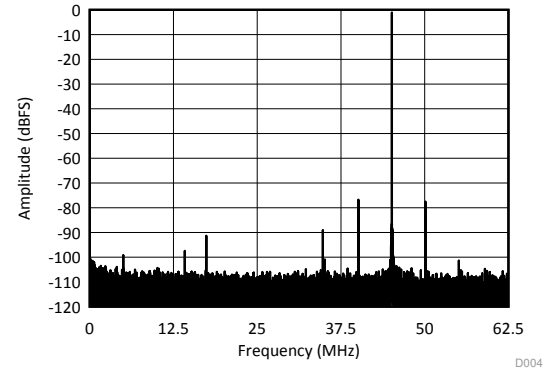
f_{IN} = 30.1 MHz, f_{PSRR} = 3 MHz, A_{PSRR} = 50 mV_{PP},
SNR = 58.51 dBFS, SINAD = 58.51 dBFS, SFDR = 60.53 dBc,
THD = –90.71 dBc, SFDR = 60.53 dBc (non 23)

図 33. Power-Supply Rejection Ratio Spectrum



f_{IN} = 30 MHz, A_{IN} = –1 dBFS,
test signal amplitude = 50 mV_{PP}

図 34. Common-Mode Rejection Ratio vs Test Signal Frequency



f_{IN} = 170.1 MHz, f_{CMRR} = 5 MHz, A_{CMRR} = 50 mV_{PP},
SNR = 69.72 dBFS, SINAD = 69.66 dBFS, SFDR = 75.66 dBc,
THD = –86.98 dBc, SFDR = 75.66 dBc (non 23)

図 35. Common-Mode Rejection Ratio Spectrum

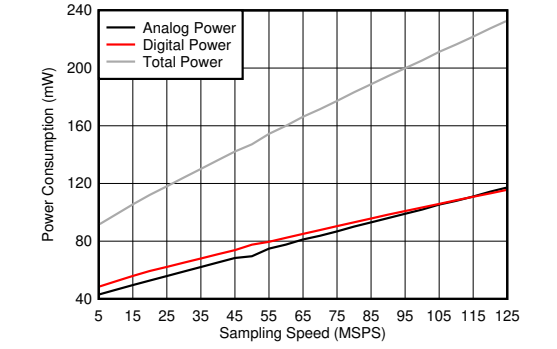


図 36. Power vs Sampling Frequency (1-Wire Mode)

7.11 Typical Characteristics: Contour

typical values at T_A = 25°C, ADC sampling rate = 125 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from f_S / 2 when is chopper enabled (unless otherwise noted)

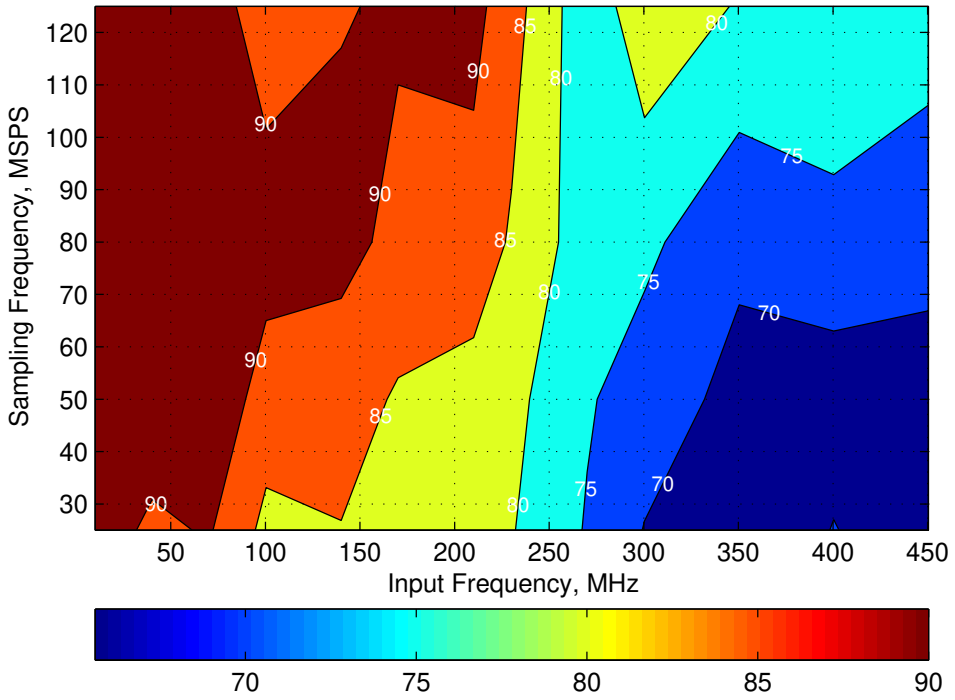


図 37. Spurious-Free Dynamic Range (SFDR)

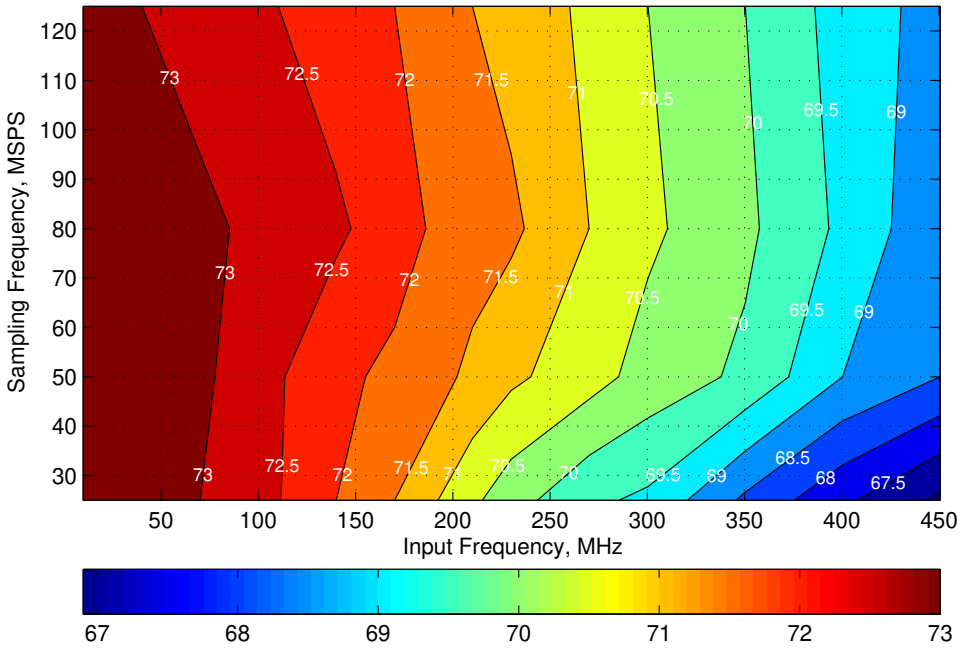
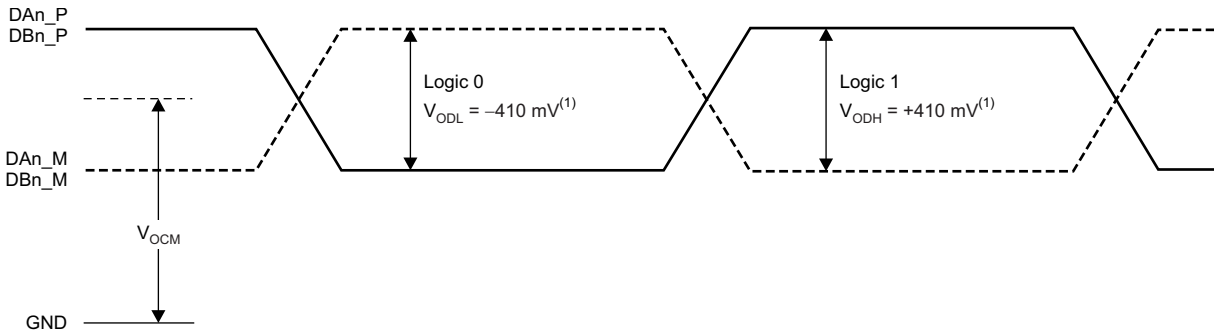


図 38. Signal-to-Noise Ratio (SNR)

8 Parameter Measurement Information

8.1 Timing Diagrams



(1) With an external 100-Ω termination.

図 39. Serial LVDS Output Voltage Levels

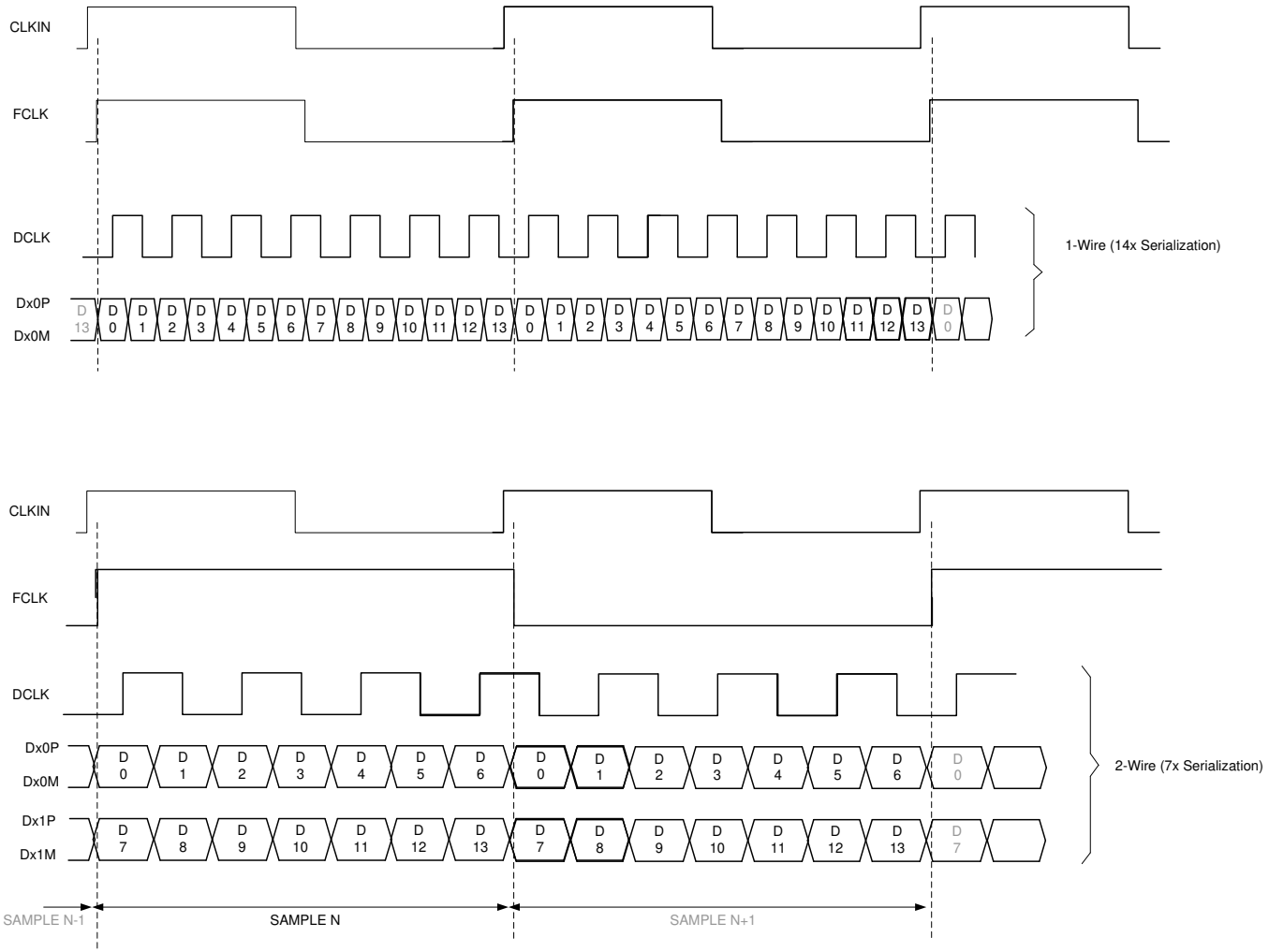


図 40. Output Timing Diagram

Timing Diagrams (continued)

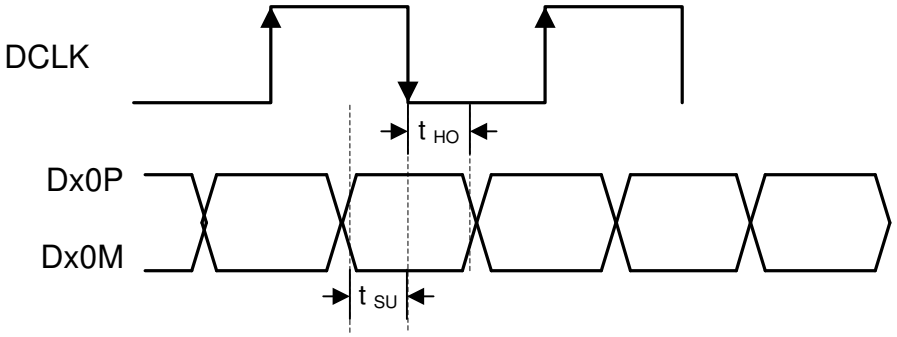
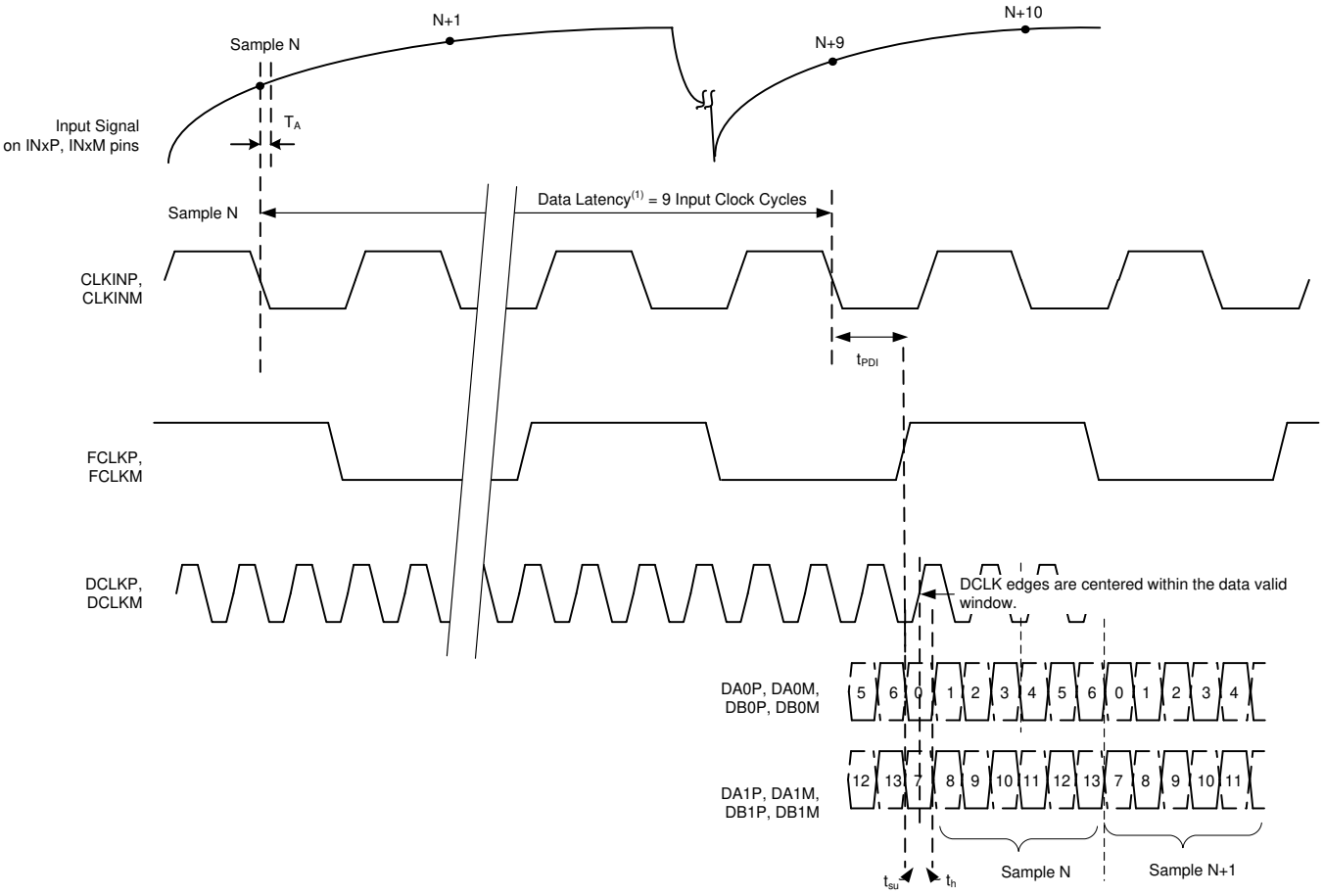


図 41. Setup and Hold Time



(1) Overall latency = data latency + t_{PDI}.

図 42. Latency Diagram

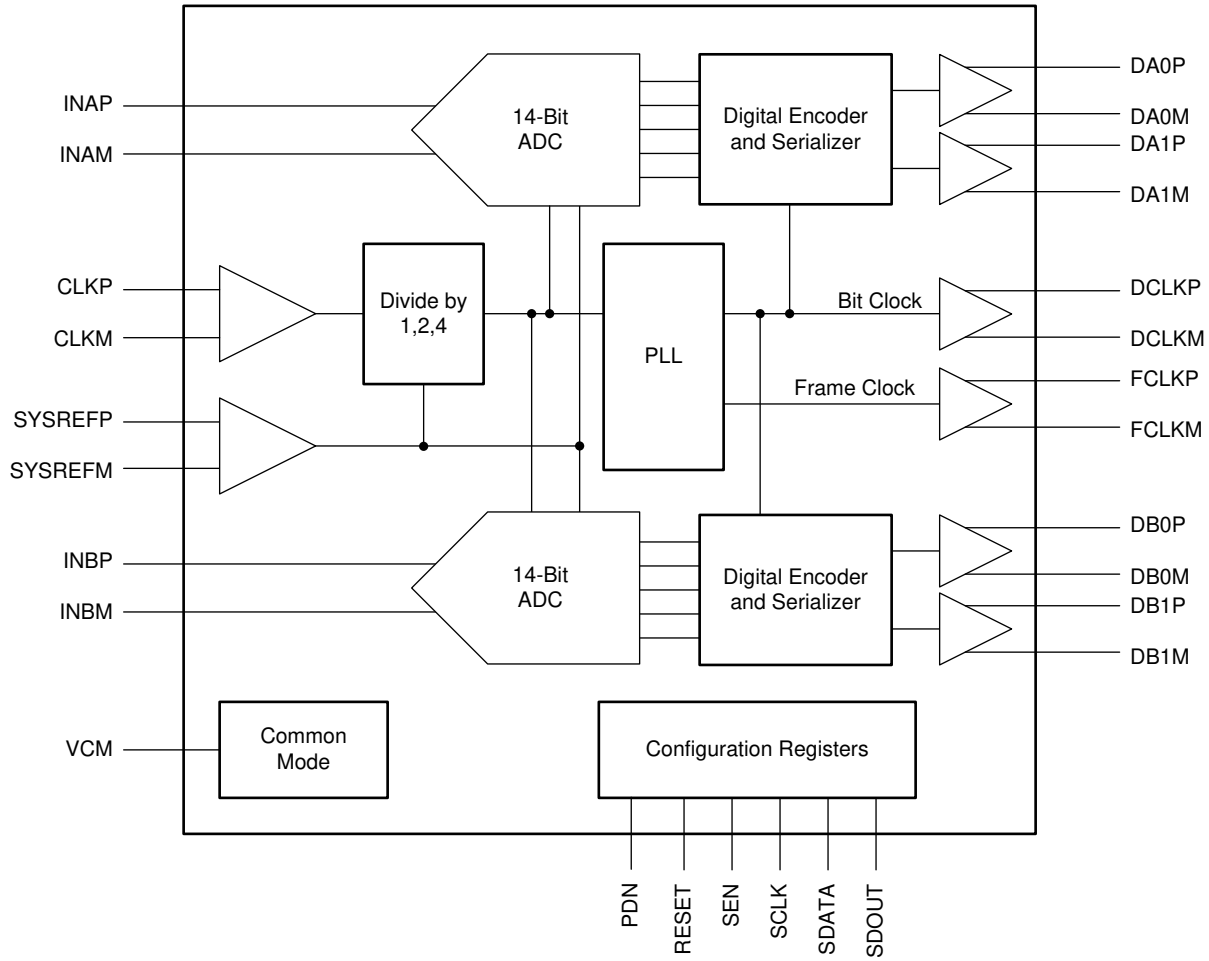
9 Detailed Description

9.1 Overview

The ADC3244E is a high-performance, 14-bit, 125-MSPS, dual channel analog-to-digital converter (ADC) with ultra-low power consumption. The ADC3244E supports the extended ambient temperature range of –50°C to +105°C, making this device a great choice for extreme temperature conditions while delivering excellent noise and linearity performance.

The LVDS output interface reduces number of connections between the ADC and receiving device, such as an FPGA, which results in power saving and higher system integration. The device supports an input dynamic range of 2 V_{PP}, and is equipped with digital features such as chopper function and dither algorithm. The chopper function helps in shifting the ADC 1/f noise spectrum to the Nyquist frequency, while preserving the signal spectrum, thus making this device useful for dc-coupling applications. The internal dither algorithms help clean higher-order harmonic spurs from the ADC output spectrum. See the *Chopper Functionality* and *Internal Dither Algorithm* sections for more details on chopper and dither functions, respectively.

9.2 Functional Block Diagram



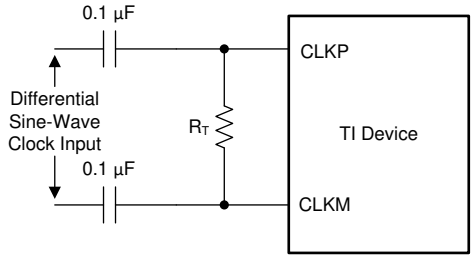
9.3 Feature Description

9.3.1 Analog Inputs

The ADC3244E analog signal inputs are designed to be driven differentially. Each input pin (INP, INM) must swing symmetrically between (VCM + 0.5 V) and (VCM – 0.5 V), resulting in a 2-V_{PP} (default) differential input swing. The input sampling circuit has a 3-dB bandwidth that extends up to 540 MHz (50-Ω source driving 50-Ω termination between INP and INM).

9.3.2 Clock Input

The device clock inputs can be driven differentially (sine, LVPECL, or LVDS) or single-ended (LVCMOS), with little or no difference in performance between them. The common-mode voltage of the clock inputs is set to 0.95 V using internal 5-kΩ resistors. The self-bias clock inputs of the ADC3244E are driven by the transformer-coupled, sine-wave clock source or by the ac-coupled, LVPECL and LVDS clock sources, as shown in 図 43, 図 44, and 図 45. See 図 46 for details regarding the internal clock buffer.



NOTE: R_T = termination resistor, if necessary.

図 43. Differential Sine-Wave Clock Driving Circuit

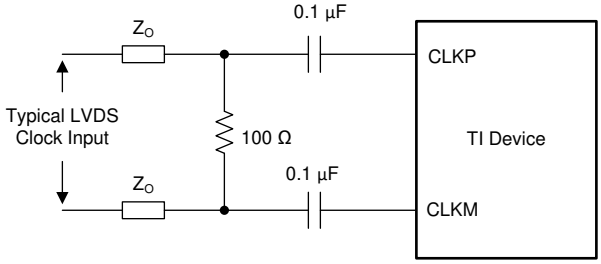


図 44. LVDS Clock Driving Circuit

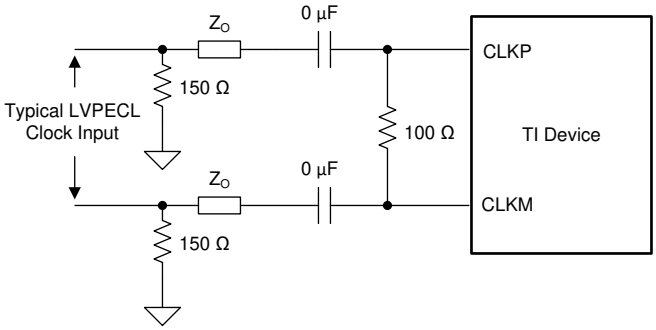
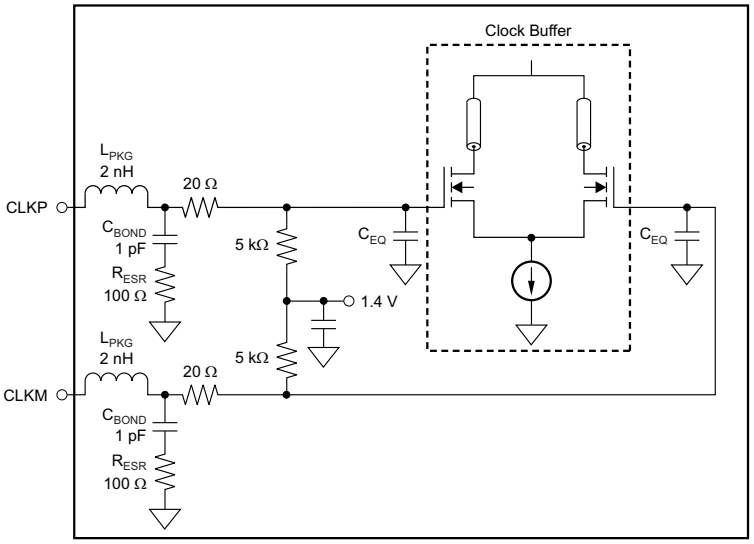


図 45. LVPECL Clock Driving Circuit



NOTE: C_{EQ} is 1 pF to 3 pF and is the equivalent input capacitance of the clock buffer.

図 46. Internal Clock Buffer

A single-ended CMOS clock can be ac-coupled to the CLKP input, with CLKM connected to ground with a 0.1-µF capacitor, as shown in 図 47. However, for best performance the clock inputs must be driven differentially, thereby reducing susceptibility to common-mode noise. For high input frequency sampling, TI recommends using a clock source with very low jitter. Band-pass filtering of the clock source can help reduce the effects of jitter. There is no change in performance with a non-50% duty cycle clock input.

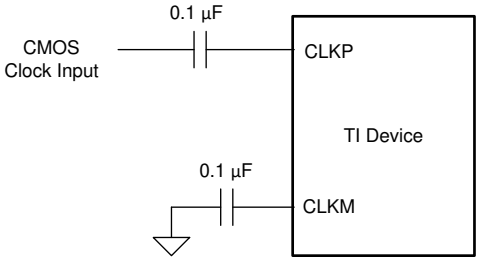


図 47. Single-Ended Clock Driving Circuit

9.3.2.1 SNR and Clock Jitter

The signal-to-noise ratio of the ADC is limited by three different factors, as shown in 式 1. Quantization noise (typically 86 dB for a 14-bit ADC) and thermal noise limit SNR at low input frequencies while the clock jitter sets SNR for higher input frequencies.

$$SNR_{ADC}[dBc] = -20 \cdot \log \sqrt{\left(10^{-\frac{SNR_{Quantization\_Noise}}{20}}\right)^2 + \left(10^{-\frac{SNR_{Thermal\_Noise}}{20}}\right)^2 + \left(10^{-\frac{SNR_{Jitter}}{20}}\right)^2} \quad (1)$$

The SNR limitation resulting from sample clock jitter can be calculated with 式 2.

$$SNR_{Jitter}[dBc] = -20 \cdot \log\left(2\pi \cdot f_{in} \cdot t_{Jitter}\right) \quad (2)$$

The total clock jitter (t_{Jitter}) has two components: the internal aperture jitter (130 fs for the device) that is set by the noise of the clock input buffer and the external clock. t_{Jitter} can be calculated with 式 3.

$$t_{Jitter} = \sqrt{\left(t_{Jitter,Ext.Clock\_Input}\right)^2 + \left(t_{Aperture\_ADC}\right)^2} \quad (3)$$

External clock jitter can be minimized by using high-quality clock sources and jitter cleaners as well as bandpass filters at the clock input while a faster clock slew rate improves the ADC aperture jitter. The ADC3244E has a typical thermal noise of 73.5 dBFS and internal aperture jitter of 130 fs. 図 48 shows SNR (from 1 MHz offset leaving the 1/f flicker noise) for different jitter of clock driver.

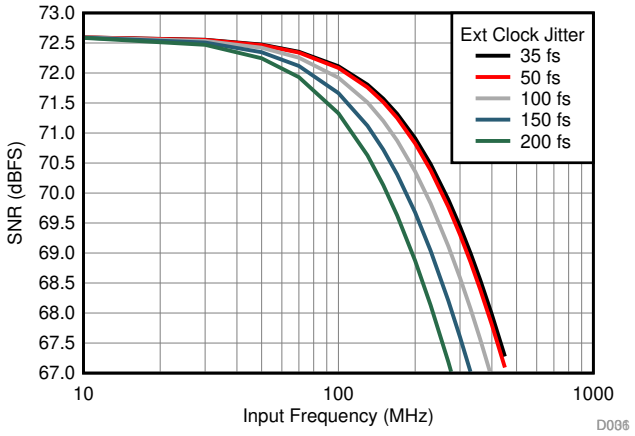


図 48. SNR vs Frequency for Different Clock Jitter

9.3.3 Digital Output Interface

The devices offer two different output format options, thus making interfacing to a field-programmable gate array (FPGA) or an application-specific integrated circuit (ASIC) easy. Each option can be easily programmed using the serial interface, as shown in 表 3. The output interface options are:

- One-wire, 1x frame clock, 14x serialization with the DDR bit clock and
- Two-wire, 0.5x frame clock, 7x serialization with the DDR bit clock.

表 3. Interface Rates

INTERFACE OPTIONS	SERIALIZATION	RECOMMENDED SAMPLING FREQUENCY (MSPS)		BIT CLOCK FREQUENCY (MHz)	FRAME CLOCK FREQUENCY (MHz)	SERIAL DATA RATE (Mbps)
		MINIMUM	MAXIMUM			
1-wire	14x	15(1)	—	105	15	210
		—	80	560	80	1120
2-wire (default after reset)	7x	20(1)	—	70	10	140
		—	125	437.5	62.5	875

(1) Use the LOW SPEED ENABLE register bits for low speed operation; see 表 22.

9.3.3.1 One-Wire Interface: 14x Serialization

In this interface option, the device outputs the data of each ADC serially on a single LVDS pair (one-wire). The data are available at the rising and falling edges of the bit clock (DDR bit clock). The ADC outputs a new word at the rising edge of every frame clock, starting with the MSB. The data rate is 14x sample frequency (14x serialization).

9.3.3.2 Two-Wire Interface: 7x Serialization

The two-wire interface is recommended for sampling frequencies above 65 MSPS. The output data rate is 7x sample frequency because seven data bits are output every clock cycle on each differential pair. Each ADC sample is sent over the two wires with the seven MSBs on Dx1P, Dx1M and the seven LSBs on Dx0P, Dx0M, as shown in 図 49. Note that in two-wire mode, the frame clock (FCLK) frequency is half of sampling clock (CLKIN) frequency.

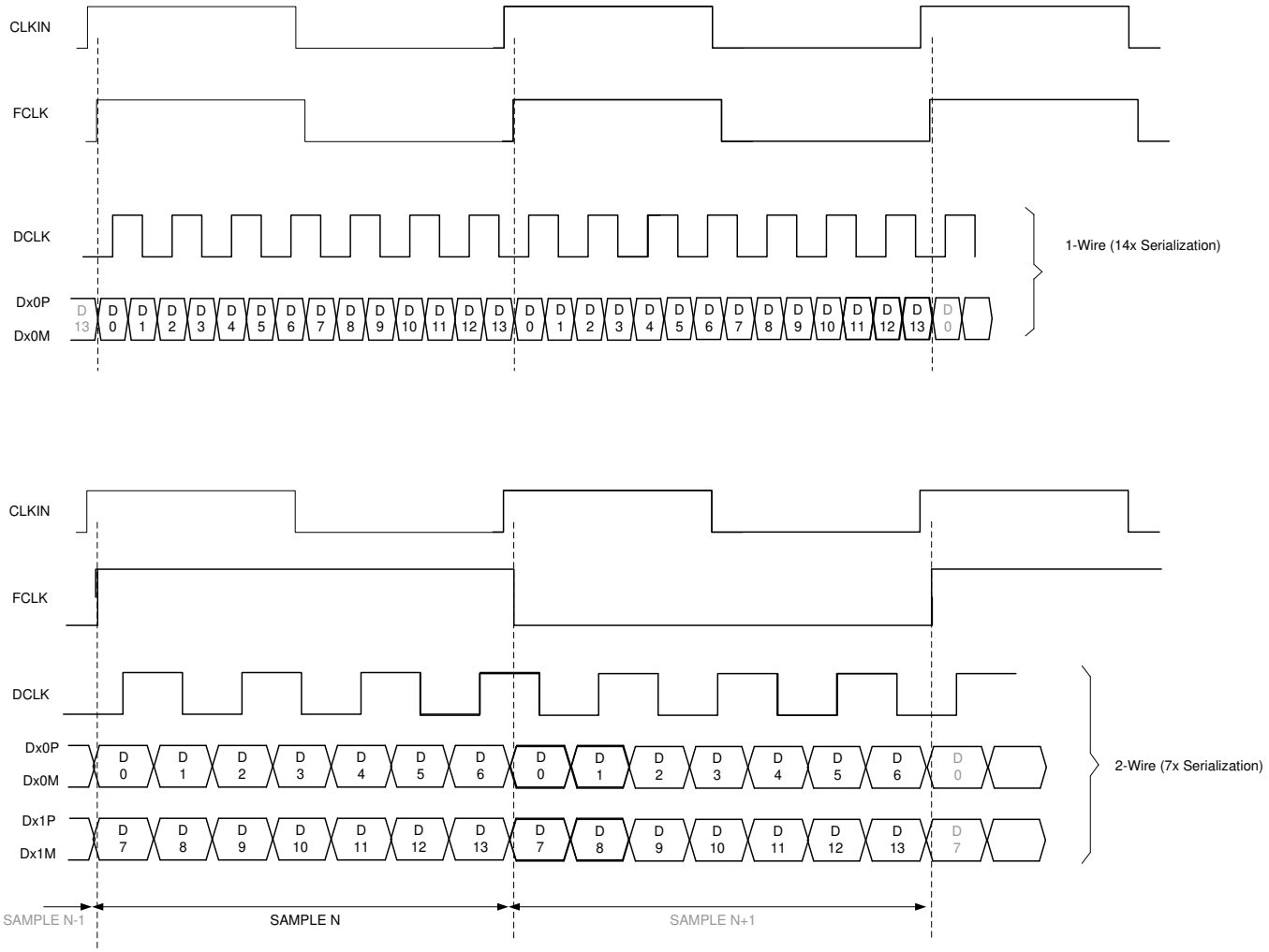


図 49. Output Timing Diagram

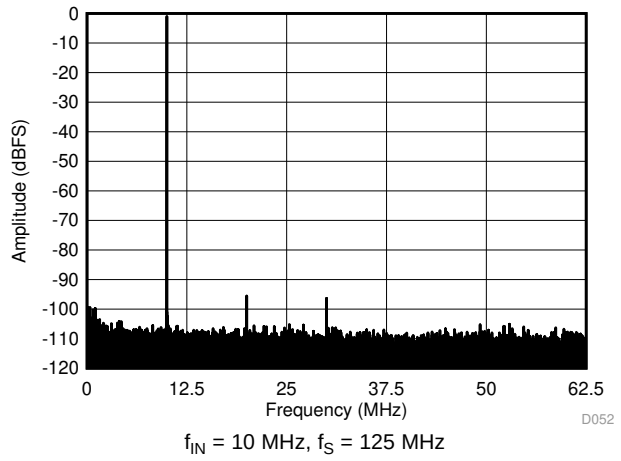
9.4 Device Functional Modes

9.4.1 Input Clock Divider

The devices are equipped with an internal divider on the clock input. The clock divider allows operation with a faster input clock, thus simplifying the system clock distribution design. The clock divider can be bypassed for operation with a 125-MHz clock while the divide-by-2 option supports a maximum input clock of 250 MHz and the divide-by-4 option provides a maximum input clock frequency of 500 MHz.

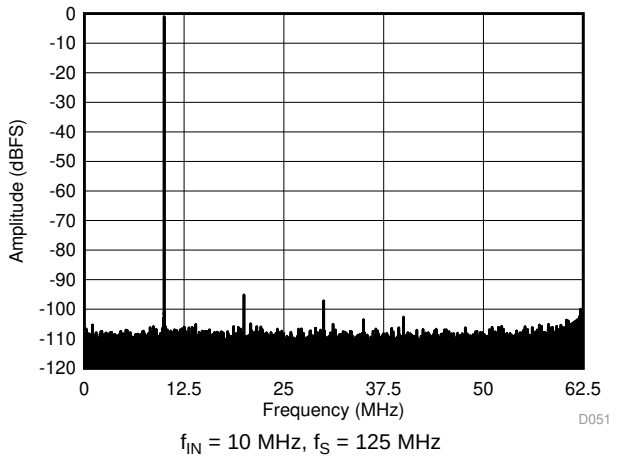
9.4.2 Chopper Functionality

The devices are equipped with an internal chopper front-end. Enabling the chopper function swaps the ADC noise spectrum by shifting the 1/f noise from dc to f_S / 2. 図 50 shows the noise spectrum with the chopper off and 図 51 shows the noise spectrum with the chopper on. This function is especially useful in applications requiring good ac performance at low input frequencies or in dc-coupled applications. The chopper can be enabled via SPI register writes and is recommended for input frequencies below 30 MHz. The chopper function creates a spur at f_S / 2 that must be filtered out digitally.



f_{IN} = 10 MHz, f_S = 125 MHz

図 50. ADC Output Spectrum With Chopper Off



f_{IN} = 10 MHz, f_S = 125 MHz

図 51. ADC Output Spectrum With Chopper On

9.4.3 Power-Down Control

The power-down functions of the ADC3244E can be controlled either through the parallel control pin (PDN) or through an SPI register setting (see register 15h). The PDN pin can also be configured using the SPI to a global power-down or standby functionality, as shown in 表 4.

表 4. Power-Down Modes

FUNCTION	POWER CONSUMPTION (mW)	WAKE-UP TIME (µs)
Global power-down	5	85
Standby	81	35

9.4.3.1 Improving Wake-Up Time From Global Power-Down

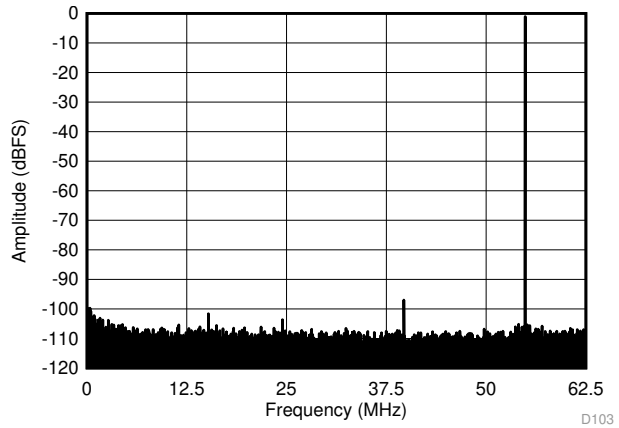
The device has an internal low-pass filter in the sampling clock path. This low-pass filter helps improve the aperture jitter of the device. However, in applications where input frequencies are < 200 MHz, noise from the aperture jitter does not dominate the overall SNR of the device. In such applications, the wake-up time from a global power-down can be reduced by bypassing the low-pass filter using the DIS CLK FILT register bit (write 80h to register address 70Ah). As shown in 表 5, setting the DIS CLK FILT bit improves the wake-up time from a global power-down from 85 µs to 55 µs.

表 5. Wake-Up Time From Global Power-Down

DIS CLK FILT REGISTER BIT	GLOBAL PDN REGISTER BIT	WAKE-UP TIME		
		TYP	MAX	UNIT
0	0→1→0	85	140	µs
1	0→1→0	55	81	µs

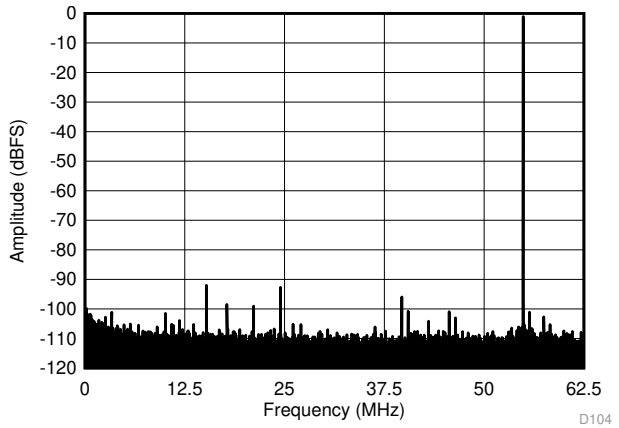
9.4.4 Internal Dither Algorithm

The ADC3244E uses an internal dither algorithm to achieve high SFDR and a clean spectrum. However, the dither algorithm marginally degrades SNR, creating a trade-off between SNR and SFDR. If desired, the dither algorithm can be turned off by using the DIS DITH CHx registers bits. 図 52 and 図 53 show the effect of using dither algorithms.



SFDR = 95.9 dBc, SNR = 72.7 dBFS, SINAD = 72.7 dBFS,
THD = 93.6 dBc, HD2 = –100.6 dBc, HD3 = –95.9 dBc

図 52. FFT with Dither On



SFDR = 90.9 dBc, SNR = 73.3 dBFS, SINAD = 73.1 dBFS,
THD = 87 dBc, HD2 = –90.9 dBc, HD3 = –94.9 dBc

図 53. FFT with Dither Off

9.5 Programming

The ADC3244E can be configured using a serial programming interface, as described in this section.

9.5.1 Serial Interface

The device has a set of internal registers that can be accessed by the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock), SDATA (serial interface data), and SDOUT (serial interface data output) pins. Serially shifting bits into the device is enabled when SEN is low. Serial data SDATA are latched at every SCLK rising edge when SEN is active (low). The serial data are loaded into the register at every 24th SCLK rising edge when SEN is low. When the word length exceeds a multiple of 24 bits, the excess bits are ignored. Data can be loaded in multiples of 24-bit words within a single active SEN pulse. The interface can function with SCLK frequencies from 20 MHz down to very low speeds (of a few hertz) and also with a non-50% SCLK duty cycle.

Programming (continued)

9.5.1.1 Register Initialization

After power-up, the internal registers **must be** initialized to their default values through a hardware reset by applying a high pulse on the RESET pin (of durations greater than 10 ns), as shown in 図 54. If required, the serial interface registers can be cleared during operation either:

1. Through a hardware reset, or
2. By applying a software reset. When using the serial interface, set the RESET bit (D0 in register address 06h) high. This setting initializes the internal registers to the default values and then self-resets the RESET bit low. In this case, the RESET pin is kept low.

9.5.1.1.1 Serial Register Write

The device internal register can be programmed with these steps:

1. Drive the SEN pin low,
2. Set the R/W bit to 0 (bit A15 of the 16-bit address),
3. Set bit A14 in the address field to 1,
4. Initiate a serial interface cycle by specifying the address of the register (A13 to A0) whose content must be written, and
5. Write the 8-bit data that are latched in on the SCLK rising edge.

図 54 and 表 6 show the timing requirements for the serial register write operation.

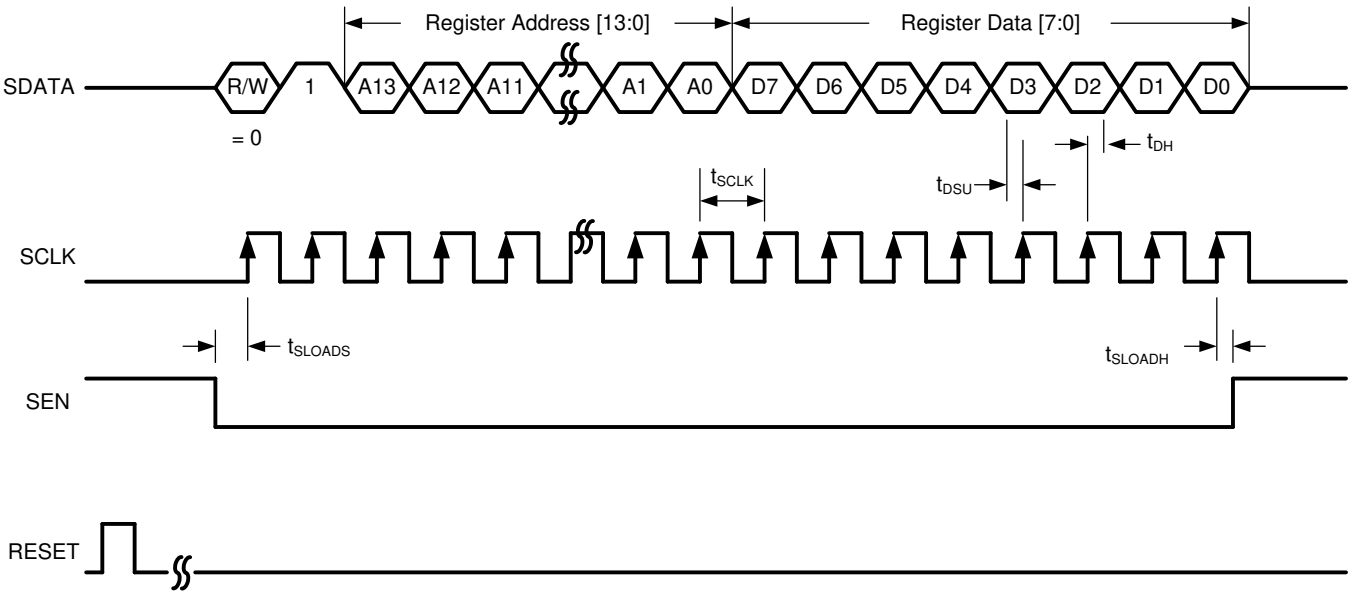


図 54. Serial Register Write Timing Diagram

表 6. Serial Interface Timing(1)

		MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK frequency (equal to 1 / t_{SCLK})	> dc		20	MHz
t_{SLOADS}	SEN to SCLK setup time	25			ns
t_{SLOADH}	SCLK to SEN hold time	25			ns
t_{DSU}	SDIO setup time	25			ns
t_{DH}	SDIO hold time	25			ns

(1) Full temperature range is from –50°C to +105°C, and AVDD = DVDD = 1.8 V.

9.5.1.1.2 Serial Register Readout

The device includes a mode where the contents of the internal registers can be read back using the SDOUT pin. This readback mode can be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC. Given below is the procedure to read contents of serial registers:

1. Drive the SEN pin low.
2. Set the R/W bit (A15) to 1. This setting disables any further writes to the registers.
3. Set bit A14 in the address field to 1.
4. Initiate a serial interface cycle specifying the address of the register (A13 to A0) whose content must be read.
5. The device outputs the contents (D7 to D0) of the selected register on the SDOUT pin.
6. The external controller can latch the contents at the SCLK rising edge.
7. To enable register writes, reset the R/W register bit to 0.

When READOUT is disabled, the SDOUT pin is in a high-impedance mode. If serial readout is not used, the SDOUT pin must float. 図 55 shows a timing diagram of the serial register read operation. Data appear on the SDOUT pin at the SCLK falling edge with an approximate delay (t_{SD_DELAY}) of 20 ns, as shown in 図 56.

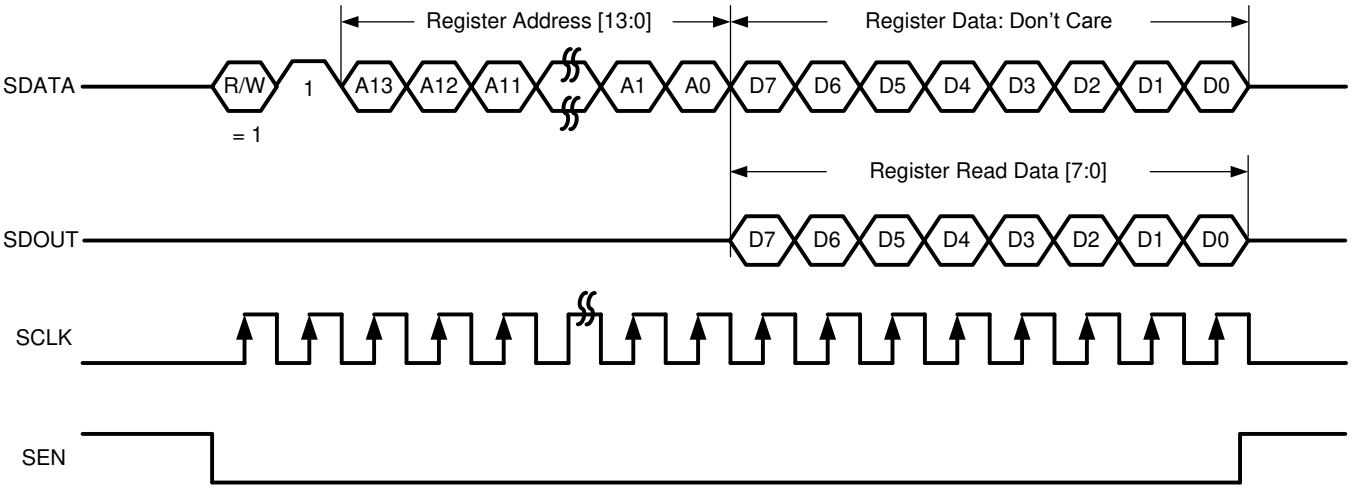


図 55. Serial Register Read Timing Diagram

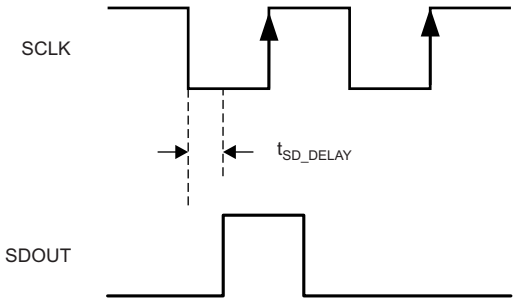


図 56. SDOUT Timing Diagram

9.5.2 Register Initialization

After power-up, the internal registers must be initialized to their default values through a hardware reset by applying a high pulse on the RESET pin, as shown in 図 57 and 表 7.

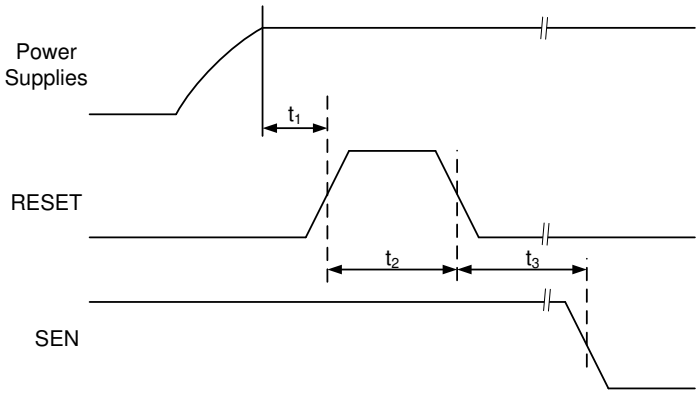


図 57. Initialization of Serial Registers after Power-Up

表 7. Power-Up Timing

		MIN	TYP	MAX	UNIT
t_1	Power-on delay: delay from power up to active high RESET pulse	1			ms
t_2	Reset pulse duration: active high RESET pulse duration	10		1000	ns
t_3	Register write delay: delay from RESET disable to SEN active	100			ns

If required, the serial interface registers can be cleared during operation either:

1. Through hardware reset, or
2. By applying a software reset. When using the serial interface, set the RESET bit (D0 in register address 06h) high. This setting initializes the internal registers to the default values and then self-resets the RESET bit low. In this case, the RESET pin is kept low.

9.6 Register Maps

表 8. Register Map Summary

REGISTER ADDRESS	REGISTER DATA							
A[13:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
01	0	0	DIS DITH CHA		DIS DITH CHB		0	0
03	0	0	0	0	0	0	0	ODD EVEN
04	0	0	0	0	0	0	0	FLIP WIRE
05	0	0	0	0	0	0	0	1W-2W
06	0	0	0	0	0	0	TEST PATTERN EN	RESET
07	0	0	0	0	0	0	0	OVR ON LSB
09	0	0	0	0	0	0	ALIGN TEST PATTERN	DATA FORMAT
0A	0	0	0	0	CHA TEST PATTERN			
0B	CHB TEST PATTERN			0	0	0	0	0
0E	CUSTOM PATTERN[13:6]							
0F	CUSTOM PATTERN[5:0]						0	0
13	0	0	0	0	0	0	LOW SPEED ENABLE	
15	0	CHA PDN	CHB PDN	0	STANDBY	GLOBAL PDN	0	CONFIG PDN PIN
25	LVDS SWING							
27	CLK DIV		0	0	0	0	0	0
41D	0	0	0	0	0	0	HIGH IF MODE0	0
422	0	0	0	0	0	0	DIS CHOP CHA	0
434	0	0	DIS DITH CHA	0	DIS DITH CHA	0	0	0
439	0	0	0	0	SP1 CHA	0	0	0
51D	0	0	0	0	0	0	HIGH IF MODE1	0
522	0	0	0	0	0	0	DIS CHOP CHB	0
534	0	0	DIS DITH CHB	0	DIS DITH CHB	0	0	0
539	0	0	0	0	SP1 CHB	0	0	0
608	HIGH IF MODE[3:2]		0	0	0	0	0	0
70A	DIS CLK FILT	0	0	0	0	0	0	PDN SYSREF

9.6.1 Summary of Special Mode Registers

表 9 lists the location, value, and functions of special mode registers in the device.

表 9. Special Modes Summary

MODE	REGISTER SETTINGS	DESCRIPTION
Special modes	Registers 439h (bit 3) and 539h (bit 3)	Always set these bits high for best performance
Disable dither	Registers 1h (bits 5-2), 434h (bits 5 and 3), and 534h (bits 5 and 3)	Disable dither to improve SNR
Disable chopper	Registers 422h (bit 1) and 522h (bit 1)	Disable chopper to shift 1/f noise floor at dc
High IF modes	Registers 41Dh (bit 1), 51Dh (bit 1), and 608h (bits 7-6)	Improves HD3 for IF > 100 MHz

9.6.2 Serial Register Description

9.6.2.1 Register 01h

図 58. Register 01h

7	6	5	4	3	2	1	0
0	0	DIS DITH CHA		DIS DITH CHB		0	0
W-0h	W-0h	R/W-0h		R/W-0h		W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

表 10. Register 01h Description

Bit	Field	Type	Reset	Description
7-6	0	W	0h	Must write 0
5-4	DIS DITH CHA	R/W	0h	These bits enable or disable the on-chip dither. Control this bit with bits 5 and 3 of register 434h. 00 = Default 11 = Dither is disabled for channel A. In this mode, SNR typically improves by 0.5 dB at 70 MHz.
3-2	DIS DITH CHB	R/W	0h	These bits enable or disable the on-chip dither. Control this bit with bits 5 and 3 of register 434h. 00 = Default 11 = Dither is disabled for channel B. In this mode, SNR typically improves by 0.5 dB at 70 MHz.
1-0	0	W	0h	Must write 0

9.6.2.2 Register 03h

図 59. Register 03h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	ODD EVEN
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

表 11. Register 03h Description

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	ODD EVEN	R/W	0h	This bit selects the bit sequence on the output lanes (in 2-wire mode only). 0 = Bits 0, 1, and 2 appear on lane 0; bits 7, 8, and 9 appear on lane 1 1 = Bits 0, 2, and 4 appear on lane 0; bits 1, 3, and 5 appear on lane 1

9.6.2.3 Register 04h

図 60. Register 04h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	FLIP WIRE
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

表 12. Register 04h Description

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	FLIP WIRE	R/W	0h	This bit flips the data on the output wires. Valid only in two wire configuration. 0 = Default 1 = Data on output wires is flipped. Pin D0x becomes D1x, and vice versa.

9.6.2.4 Register 05h

図 61. Register 05h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	1W-2W
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

表 13. Register 05h Description

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	1W-2W	R/W	0h	This bit transmits output data on either one or two wires. 0 = Output data are transmitted on two wires (Dx0P, Dx0M and Dx1P, Dx1M) 1 = Output data are transmitted on one wire (Dx0P, Dx0M). In this mode, the recommended f_S is less than 62.5 MSPS.

9.6.2.5 Register 06h

図 62. Register 06h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	TEST PATTERN EN	RESET
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

表 14. Register 06h Description

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0
1	TEST PATTERN EN	R/W	0h	This bit enables test pattern selection for the digital outputs. 0 = Normal output 1 = Test pattern output enabled
0	RESET	W	0h	This bit applies a software reset. This bit resets all internal registers to the default values and self-clears to 0.

9.6.2.6 Register 07h

図 63. Register 07h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	OVR ON LSB
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

表 15. Register 07h Description

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	OVR ON LSB	R/W	0h	This bit provides the overrange (OVR) information on the LSB bits. 0 = Output data bit 0 functions as the LSB of the 14-bit data 1 = Output data bit 0 carries the OVR information.

9.6.2.7 Register 09h

図 64. Register 09h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	ALIGN TEST PATTERN	DATA FORMAT
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

表 16. Register 09h Description

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0
1	ALIGN TEST PATTERN	R/W	0h	This bit aligns the test patterns across the outputs of both channels. 0 = Test patterns of both channels are free running 1 = Test patterns of both channels are aligned
0	DATA FORMAT	R/W	0h	This bit programs the digital output data format. 0 = Twos complement 1 = Offset binary

9.6.2.8 Register 0Ah

図 65. Register 0Ah

7	6	5	4	3	2	1	0
0	0	0	0	CHA TEST PATTERN			
W-0h	W-0h	W-0h	W-0h	R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

表 17. Register 0Ah Description

Bit	Field	Type	Reset	Description
7-4	0	W	0h	Must write 0
3-0	CHA TEST PATTERN	R/W	0h	These bits control the test pattern for channel A after the TEST PATTERN EN bit is set. 0000 = Normal operation 0001 = All 0's 0010 = All 1's 0011 = Toggle pattern: data alternate between 10101010101010 and 01010101010101 0100 = Digital ramp: data increment by 1 LSB every clock cycle from code 0 to 16383 0101 = Custom pattern: output data are the same as programmed by the CUSTOM PATTERN register bits 0110 = Deskew pattern: data are 2AAAh 1000 = PRBS pattern: data are a sequence of pseudo random numbers 1001 = 8-point sine-wave: data are a repetitive sequence of the following eight numbers that form a sine-wave: 0, 2399, 8192, 13984, 16383, 13984, 8192, 2399. Others = Do not use

9.6.2.9 Register 0Bh

図 66. Register 0Bh

7	6	5	4	3	2	1	0
CHB TEST PATTERN				0	0	0	0
R/W-0h				W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

表 18. Register 0Bh Description

Bit	Field	Type	Reset	Description
7-4	CHB TEST PATTERN	R/W	0h	These bits control the test pattern for channel B after the TEST PATTERN EN bit is set. 0000 = Normal operation 0001 = All 0's 0010 = All 1's 0011 = Toggle pattern: data alternate between 10101010101010 and 01010101010101 0100 = Digital ramp: data increment by 1 LSB every clock cycle from code 0 to 16383 0101 = Custom pattern: output data are the same as programmed by the CUSTOM PATTERN register bits 0110 = Deskew pattern: data are 2AAAh 1000 = PRBS pattern: data are a sequence of pseudo random numbers 1001 = 8-point sine-wave: data are a repetitive sequence of the following eight numbers that form a sine-wave: 0, 2399, 8192, 13984, 16383, 13984, 8192, 2399. Others = Do not use
3-0	0	W	0h	Must write 0

9.6.2.10 Register 0Eh

図 67. Register 0Eh

7	6	5	4	3	2	1	0
CUSTOM PATTERN[13:6]							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 19. Register 0Eh Description

Bit	Field	Type	Reset	Description
7-0	CUSTOM PATTERN[13:6]	R/W	0h	These bits set the 14-bit custom pattern (bits 13-6) for all channels.

9.6.2.11 Register 0Fh

図 68. Register 0Fh

7	6	5	4	3	2	1	0
CUSTOM PATTERN[5:0]						0	0
R/W-0h						W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

表 20. Register 0Fh Description

Bit	Field	Type	Reset	Description
7-2	CUSTOM PATTERN[5:0]	R/W	0h	These bits set the 14-bit custom pattern (bits 5-0) for all channels.
1-0	0	W	0h	Must write 0

9.6.2.12 Register 13h (address = 13h)

図 69. Register 13h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	LOW SPEED ENABLE	
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

表 21. Register 13h Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0.
1-0	LOW SPEED ENABLE	R/W	0h	Enables low speed operation in 1-wire and 2-wire mode. Depending upon sampling frequency, write this bit as per 表 22.

表 22. LOW SPEED ENABLE Register Bit Settings Across f_S

f_S (MSPS)		REGISTER BIT LOW SPEED ENABLE	
MIN	MAX	1-WIRE MODE	2-WIRE MODE
25	125	00	00
20	25	00	10
15	20	10	Not supported

9.6.2.13 Register 15h

図 70. Register 15h

7	6	5	4	3	2	1	0
0	CHA PDN	CHB PDN	0	STANDBY	GLOBAL PDN	0	CONFIG PDN PIN
W-0h	R/W-0h	R/W-0h	W-0h	R/W-0h	R/W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

表 23. Register 15h Description

Bit	Field	Type	Reset	Description
7	0	W	0h	Must write 0
6	CHA PDN	R/W	0h	0 = Normal operation 1 = Power-down channel A
5	CHB PDN	R/W	0h	0 = Normal operation 1 = Power-down channel B
4	0	W	0h	Must write 0
3	STANDBY	R/W	0h	The ADCs of both channels enter standby. 0 = Normal operation 1 = Standby
2	GLOBAL PDN	R/W	0h	0 = Normal operation 1 = Global power-down
1	0	W	0h	Must write 0
0	CONFIG PDN PIN	R/W	0h	This bit configures the PDN pin as either a global power-down or standby pin. 0 = Logic high voltage on the PDN pin sends the device into global power-down 1 = Logic high voltage on the PDN pin sends the device into standby

9.6.2.14 Register 25h

図 71. Register 25h

7	6	5	4	3	2	1	0
LVDS SWING							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 24. Register 25h Description

Bit	Field	Type	Reset	Description
7-0	LVDS SWING	R/W	0h	These bits control the swing of the LVDS outputs (including the data output, bit clock, and frame clock). For details see 表 25.

表 25. LVDS Output Swing

BITS 7-4	BITS 3-0	LVDS OUTPUT SWING
0h	0h	Default (±425 mV)
Dh	9h	Swing reduces by 50 mV
Eh	Ah	Swing reduces by 100 mV
Fh	Dh	Swing reduces by 300 mV
Ch	Eh	Swing increases by 100 mV
Others	Others	Do not use

9.6.2.15 Register 27h

図 72. Register 27h

7	6	5	4	3	2	1	0
CLK DIV		0	0	0	0	0	0
R/W-0h		W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

表 26. Register 27h Description

Bit	Field	Type	Reset	Description
7-6	CLK DIV	R/W	0h	These bits set the internal clock divider for the input sampling clock. 00 = Divide-by-1 01 = Divide-by-1 10 = Divide-by-2 11 = Divide-by-4
5-0	0	W	0h	Must write 0

9.6.2.16 Register 41Dh

図 73. Register 41Dh

7	6	5	4	3	2	1	0
0	0	0	0	0	0	HIGH IF MODE0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

表 27. Register 41Dh Description

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0
1	HIGH IF MODE0	R/W	0h	This bit improves HD3 for IF > 100 MHz. 0 = Normal operation For best HD3 at IF > 100 MHz, set HIGH IF MODE[3:0] to 1111.
0	0	W	0h	Must write 0

9.6.2.17 Register 422h

図 74. Register 422h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	DIS CHOP CHA	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

表 28. Register 422h Description

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0
1	DIS CHOP CHA	R/W	0h	Disable chopper. Set this bit to shift a 1/f noise floor at dc. 0 = 1/f noise floor is centered at f_S / 2 (default) 1 = Chopper mechanism is disabled; 1/f noise floor is centered at dc
0	0	W	0h	Must write 0

9.6.2.18 Register 434h

図 75. Register 434h

7	6	5	4	3	2	1	0
0	0	DIS DITH CHA	0	DIS DITH CHA	0	0	0
W-0h	W-0h	R/W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

表 29. Register 434h Description

Bit	Field	Type	Reset	Description
7-6	0	W	0h	Must write 0
5	DIS DITH CHA	R/W	0h	Set this bit with bits 5 and 4 of register 01h. 00 = Default 11 = Dither is disabled for channel A. In this mode, SNR typically improves by 0.5 dB at 70 MHz.
4	0	W	0h	Must write 0
3	DIS DITH CHA	R/W	0h	Set this bit with bits 5 and 4 of register 01h. 00 = Default 11 = Dither is disabled for channel A. In this mode, SNR typically improves by 0.5 dB at 70 MHz.
2-0	0	W	0h	Must write 0

9.6.2.19 Register 439h

図 76. Register 439h

7	6	5	4	3	2	1	0
0	0	0	0	SP1 CHA	0	0	0
W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

表 30. Register 439h Description

Bit	Field	Type	Reset	Description
7-4	0	W	0h	Must write 0
3	SP1 CHA	R/W	0h	Special mode for best performance on channel A. Always write 1 after reset.
2-0	0	W	0h	Must write 0

9.6.2.20 Register 51Dh

図 77. Register 51Dh

7	6	5	4	3	2	1	0
0	0	0	0	0	0	HIGH IF MODE1	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

表 31. Register 51Dh Description

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0
1	HIGH IF MODE1	R/W	0h	This bit improves HD3 for IF > 100 MHz. 0 = Normal operation For best HD3 at IF > 100 MHz, set HIGH IF MODE[3:0] to 1111.
0	0	W	0h	Must write 0

9.6.2.21 Register 522h

図 78. Register 522h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	DIS CHOP CHB	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

表 32. Register 522h Description

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0
1	DIS CHOP CHB	R/W	0h	Disable chopper. Set this bit to shift a 1/f noise floor at dc. 0 = 1/f noise floor is centered at f_S / 2 (default) 1 = Chopper mechanism is disabled; 1/f noise floor is centered at dc
0	0	W	0h	Must write 0

9.6.2.22 Register 534h

図 79. Register 534h

7	6	5	4	3	2	1	0
0	0	DIS DITH CHA	0	DIS DITH CHA	0	0	0
W-0h	W-0h	R/W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

表 33. Register 534h Description

Bit	Field	Type	Reset	Description
7-6	0	W	0h	Must write 0
5	DIS DITH CHA	R/W	0h	Set this bit with bits 3 and 2 of register 01h. 00 = Default 11 = Dither is disabled for channel B. In this mode, SNR typically improves by 0.5 dB at 70 MHz.
4	0	W	0h	Must write 0
3	DIS DITH CHA	R/W	0h	Set this bit with bits 3 and 2 of register 01h. 00 = Default 11 = Dither is disabled for channel B. In this mode, SNR typically improves by 0.5 dB at 70 MHz.
2-0	0	W	0h	Must write 0

9.6.2.23 Register 539h

図 80. Register 539h

7	6	5	4	3	2	1	0
0	0	0	0	SP1 CHB	0	0	0
W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

表 34. Register 539h Description

Bit	Field	Type	Reset	Description
7-4	0	W	0h	Must write 0
3	SP1 CHB	R/W	0h	Special mode for best performance on channel B. Always write 1 after reset.
0	0	W	0h	Must write 0

9.6.2.24 Register 608h

図 81. Register 608h

7	6	5	4	3	2	1	0
HIGH IF MODE[3:2]		0	0	0	0	0	0
R/W-0h		W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

表 35. Register 608h Description

Bit	Field	Type	Reset	Description
7-6	HIGH IF MODE[3:2]	R/W	0h	This bit improves HD3 for IF > 100 MHz. 0 = Normal operation For best HD3 at IF > 100 MHz, set HIGH IF MODE[3:0] to 1111.
5-0	0	W	0h	Must write 0

9.6.2.25 Register 70Ah

図 82. Register 70Ah

7	6	5	4	3	2	1	0
DIS CLK FILT	0	0	0	0	0	0	PDN SYSREF
R/W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

表 36. Register 70Ah Description

Bit	Field	Type	Reset	Description
7	DIS CLK FILT	R/W	0h	Set this bit to improve wake-up time from global power-down mode; see the *Improving Wake-Up Time From Global Power-Down* section for details.
6-1	0	W	0h	Must write 0
0	PDN SYSREF	R/W	0h	If the SYSREF pins are not used in the system, the SYSREF buffer must be powered down by setting this bit. 0 = Normal operation 1 = Powers down the SYSREF buffer

10 Applications and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

Typical applications involving transformer coupled circuits are discussed in this section. Transformers (such as ADT1-1WT or WBC1-1) can be used up to 250 MHz to achieve good phase and amplitude balances at ADC inputs. While designing the dc driving circuits, the ADC input impedance must be considered. 図 83 and 図 84 show the impedance ($Z_{in} = R_{in} || C_{in}$) across the ADC input pins.

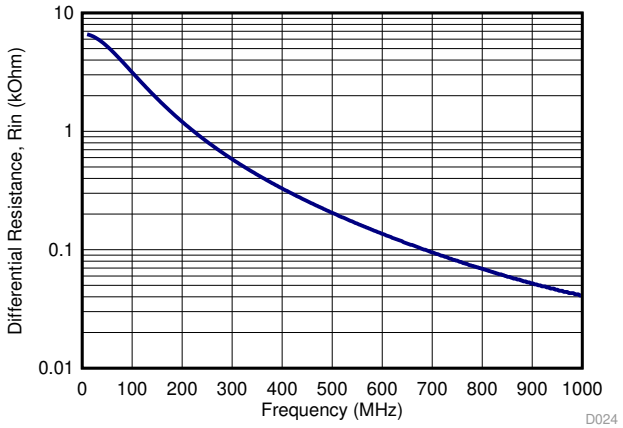


図 83. Differential Input Resistance (R_{IN})

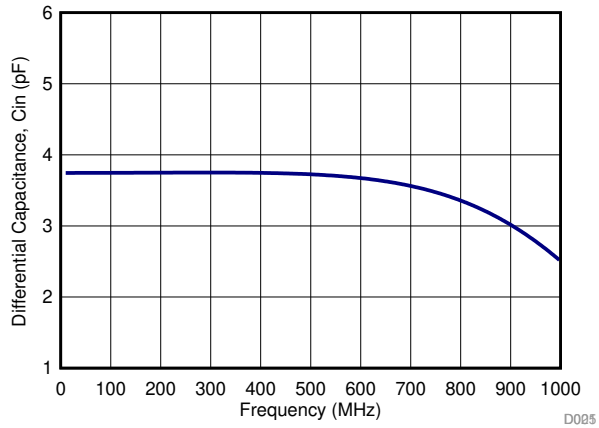


図 84. Differential Input Capacitance (C_{IN})

10.2 Typical Applications

10.2.1 Driving Circuit Design: Low Input Frequencies

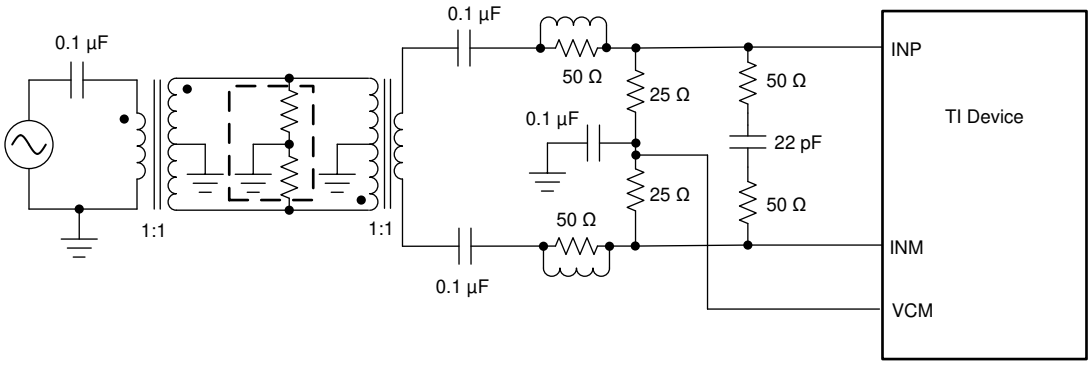


図 85. Driving Circuit for Low Input Frequencies

10.2.1.1 Design Requirements

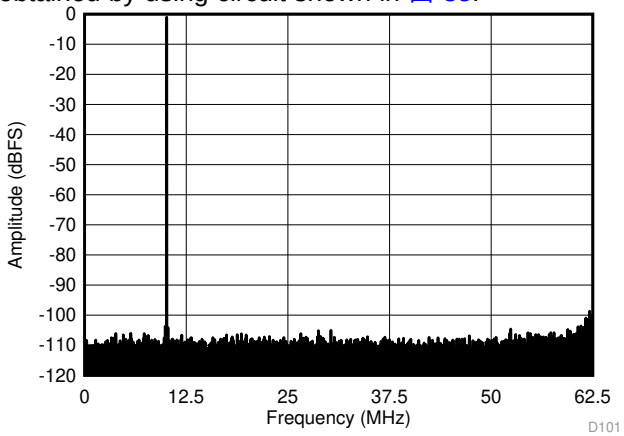
For optimum performance, the analog inputs must be driven differentially. An optional 5-Ω to 15-Ω resistor in series with each input pin can be kept to damp out ringing caused by package parasitic. The drive circuit may have to be designed to minimize the impact of kick-back noise generated by sampling switches opening and closing inside the ADC, as well as providing low insertion loss over the desired frequency range and matched impedance to the source.

10.2.1.2 Detailed Design Procedure

A typical application involving using two back-to-back coupled transformers is shown in 図 85. The circuit is optimized for low input frequencies. An external R-C-R filter using 50-Ω resistors and a 22-pF capacitor is used with the series inductor (39 nH), this combination helps absorb the sampling glitches.

10.2.1.3 Application Curve

図 86 shows the performance obtained by using circuit shown in 図 85.



SFDR = 102.6 dBc, SNR = 72.9 dBFS, SINAD = 72.8 dBFS,
THD = 99.8 dBc, HD2 = –108.6 dBc, HD3 = –104.0 dBc

図 86. Performance FFT at 10 MHz (Low Input Frequency)

Typical Applications (continued)

10.2.2 Driving Circuit Design: Input Frequencies Between 100 MHz to 230 MHz

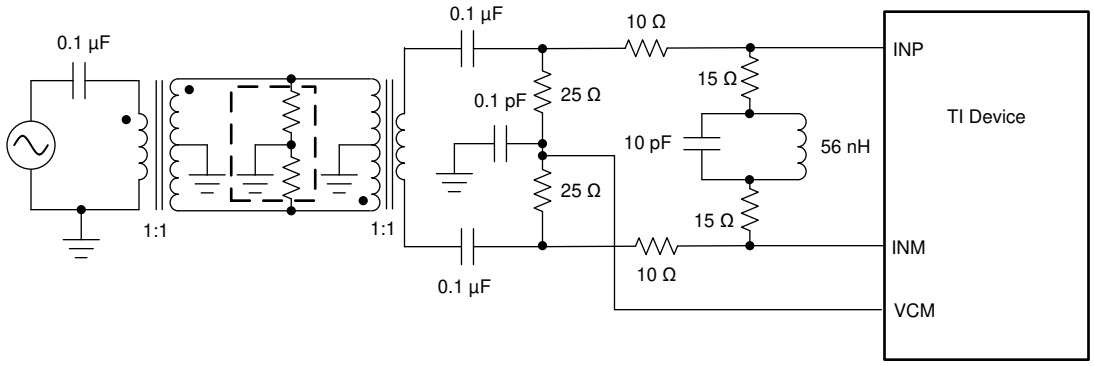


図 87. Driving Circuit for Mid-Range Input Frequencies (100 MHz < f_{IN} < 230 MHz)

10.2.2.1 Design Requirements

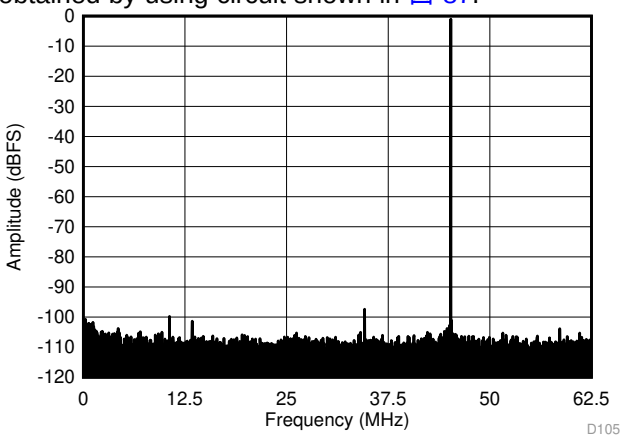
See the previous *Design Requirements* section for further details.

10.2.2.2 Detailed Design Procedure

When input frequencies are between 100 MHz to 230 MHz, an R-LC-R circuit can be used to optimize performance, as shown in 図 87.

10.2.2.3 Application Curve

図 88 shows the performance obtained by using circuit shown in 図 87.



SFDR = 96.4 dBc, SNR = 72.1 dBFS, SINAD = 72.0 dBFS,
THD = 92.6 dBc, HD2 = –96.4 dBc, HD3 = –98.8 dBc

図 88. Performance FFT at 170 MHz (Mid Input Frequency)

Typical Applications (continued)

10.2.3 Driving Circuit Design: Input Frequencies Greater than 230 MHz

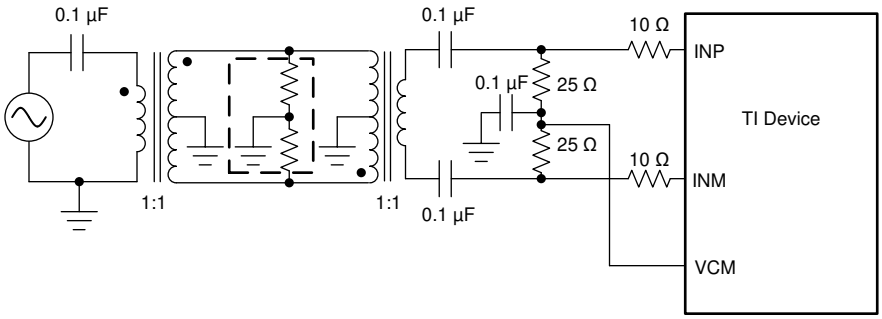


図 89. Driving Circuit for High input Frequencies (f_{IN} > 230 MHz)

10.2.3.1 Design Requirements

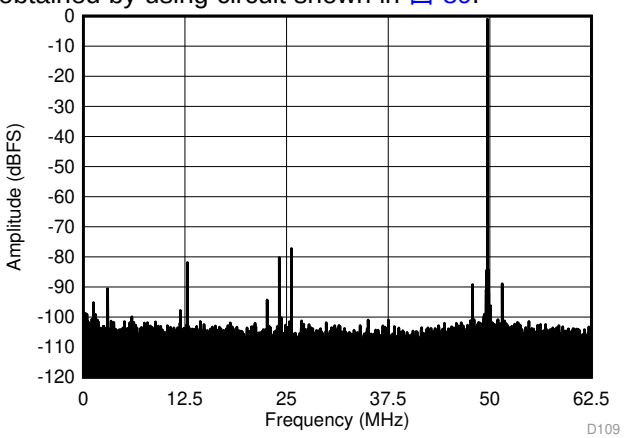
See the first *Design Requirements* section for further details.

10.2.3.2 Detailed Design Procedure

For high input frequencies (> 230 MHz), using the R-C-R or R-LC-R circuit does not show significant improvement in performance. However, a series resistance of 10 Ω can be used as shown in 図 89.

10.2.3.3 Application Curve

図 90 shows the performance obtained by using circuit shown in 図 89.



SFDR = 76.2 dBc, SNR = 68.3 dBFS, SINAD = 67.5 dBFS,
THD = 74.3 dBc, HD2 = –76.2 dBc, HD3 = –79.2 dBc

図 90. Performance FFT at 450 MHz (High Input Frequency)

11 Power Supply Recommendations

The device requires a 1.8-V nominal supply for AVDD and DVDD. There are no specific sequence power-supply requirements during device power-up. AVDD and DVDD can power up in any order.

12 Layout

12.1 Layout Guidelines

The ADC3244E EVM layout can be used as a reference layout to obtain the best performance. A layout diagram of the EVM top layer is provided in 図 91. Some important points to remember during laying out the board are:

1. Place the analog inputs on opposite sides of the device pin out to provide minimum crosstalk on the package level. To minimize crosstalk onboard, the analog inputs must exit the pin out in opposite directions, as shown in the reference layout of 図 91 as much as possible.
2. In the device pin out, place the sampling clock on a side perpendicular to the analog inputs in order to minimize coupling between them. This configuration is also maintained on the reference layout of 図 91 as much as possible.
3. Keep digital outputs away from the analog inputs. When these digital outputs exit the pin out, do not keep the digital output traces parallel to the analog input traces because this configuration can result in coupling from digital outputs to analog inputs and degrade performance. All digital output traces to the receiver [such as a field-programmable gate array (FPGA) or an application-specific integrated circuit (ASIC)] must be matched in length to avoid skew among outputs.
4. At each power-supply pin (AVDD and DVDD), keep a 0.1-µF decoupling capacitor close to the device. A separate decoupling capacitor group consisting of a parallel combination of 10-µF, 1-µF, and 0.1-µF capacitors can be kept close to the supply source.

12.2 Layout Example

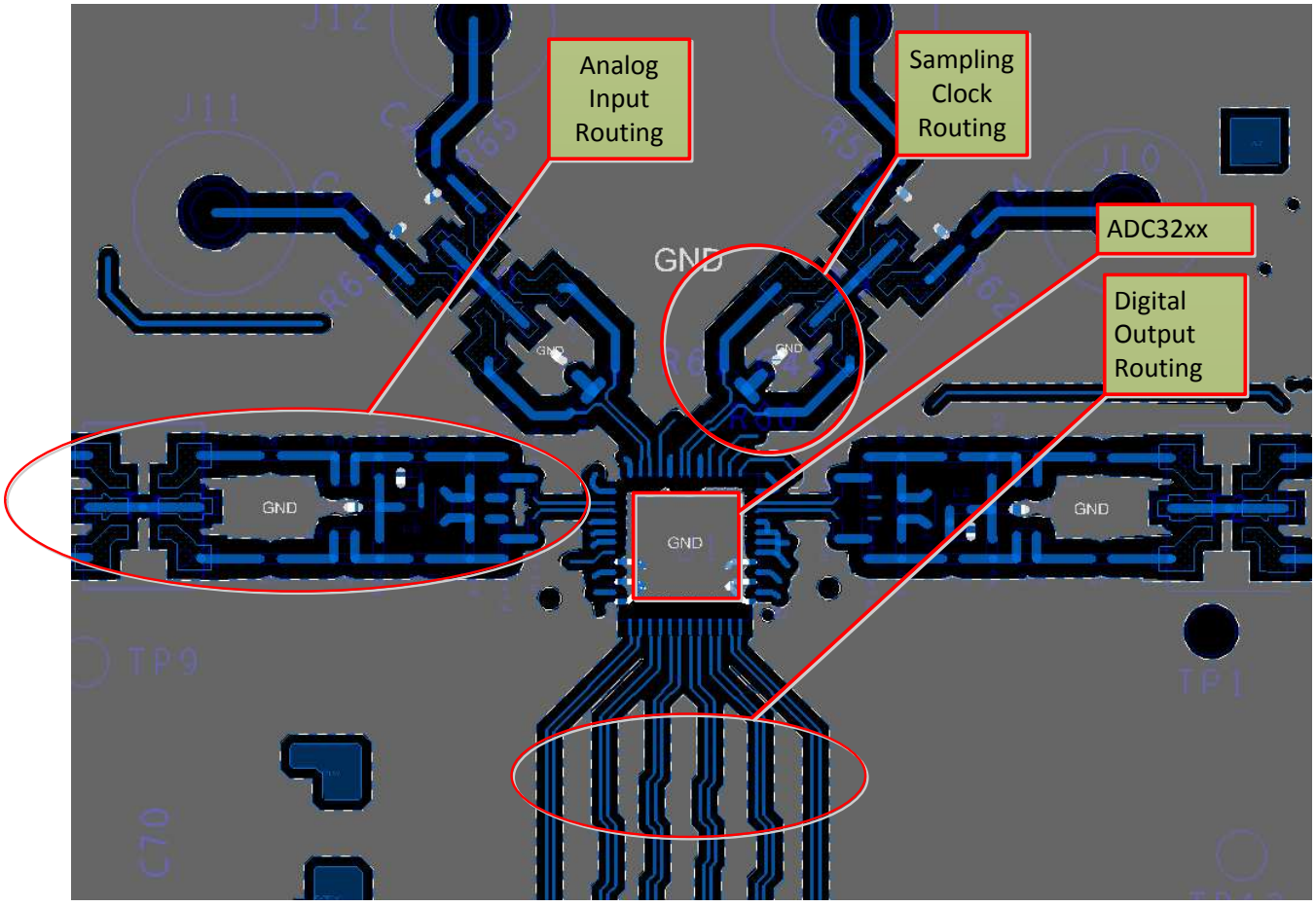


図 91. Typical Layout of the ADC3244E Board

13 デバイスおよびドキュメントのサポート

13.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

13.2 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 商標

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.4 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADC3244EIRGZT	ACTIVE	VQFN	RGZ	48	250	RoHS & Green	NIPDAUAG	Level-3-260C-168 HR	-50 to 105	AZ3244E	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

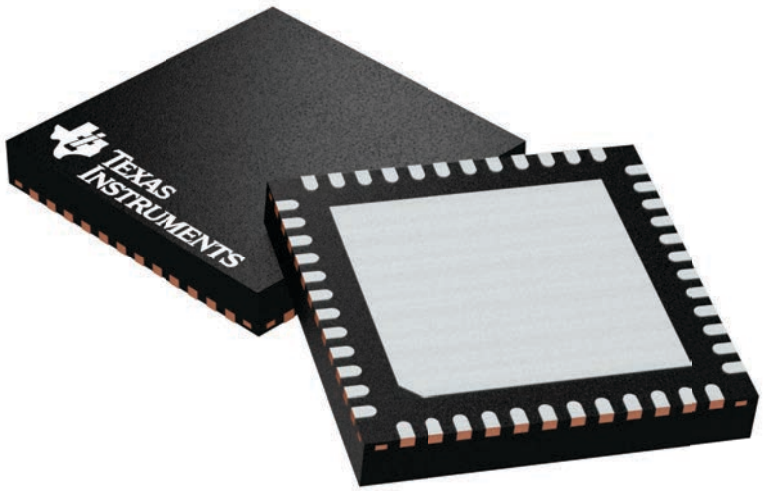
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

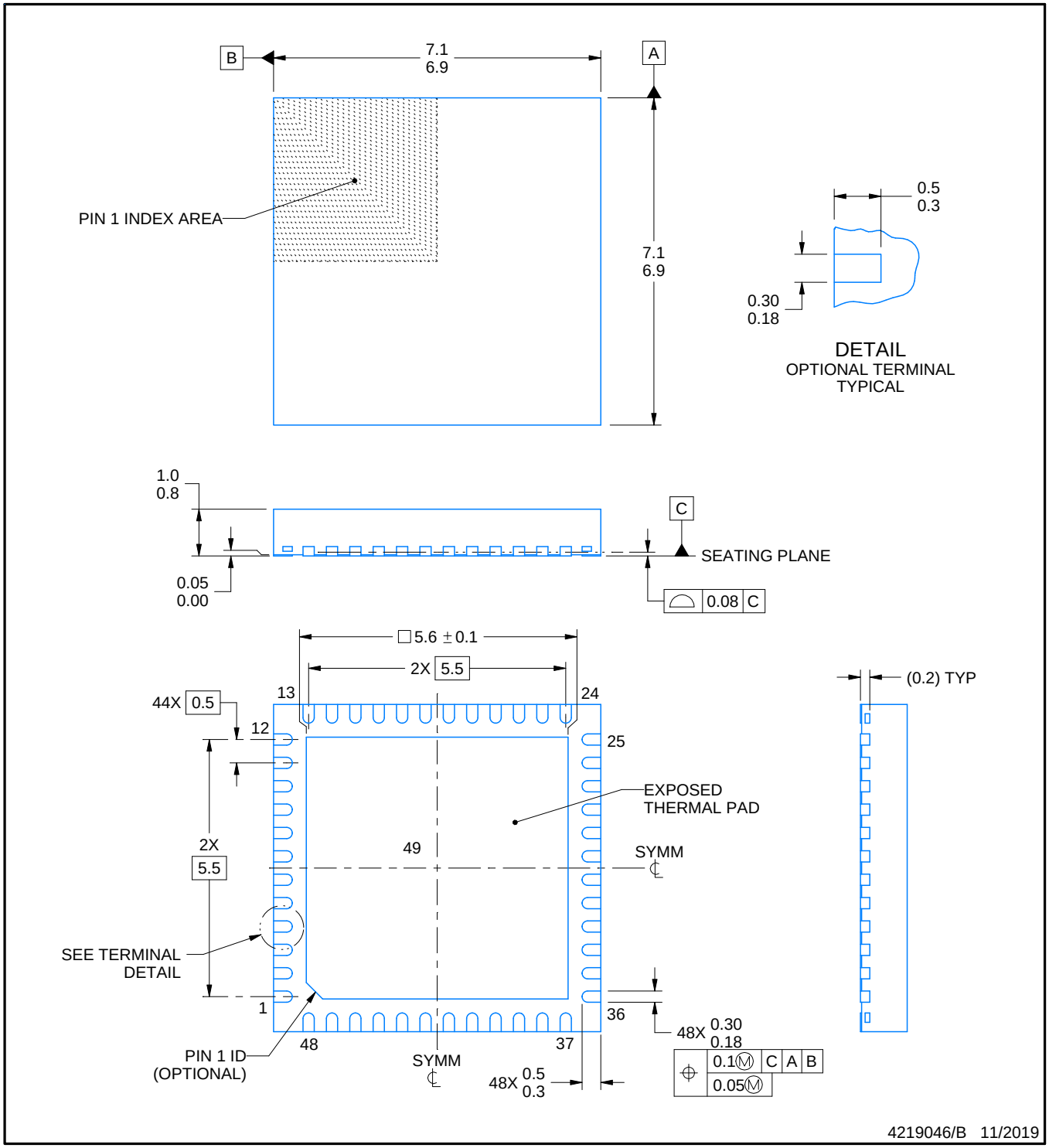
4224671/A

PACKAGE OUTLINE

RGZ0048D

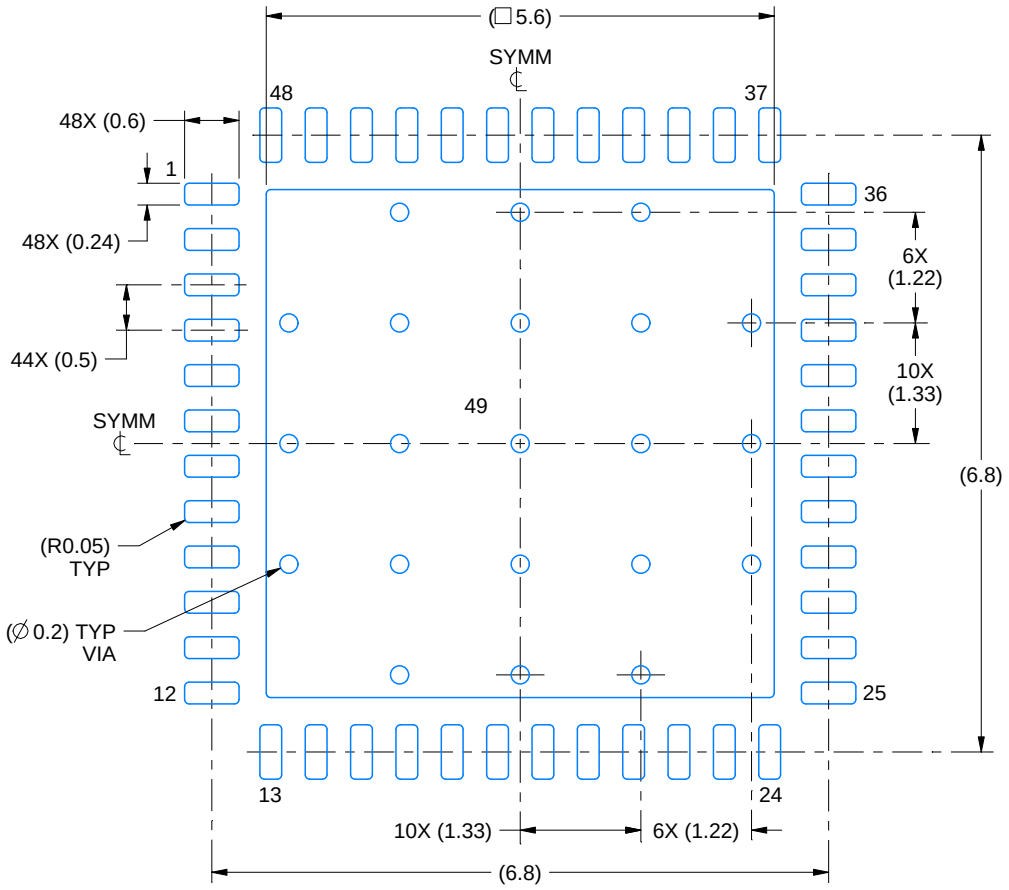
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

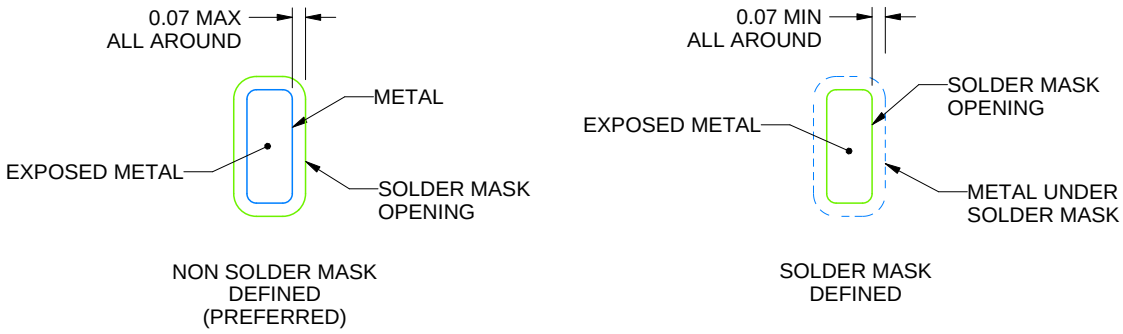


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X

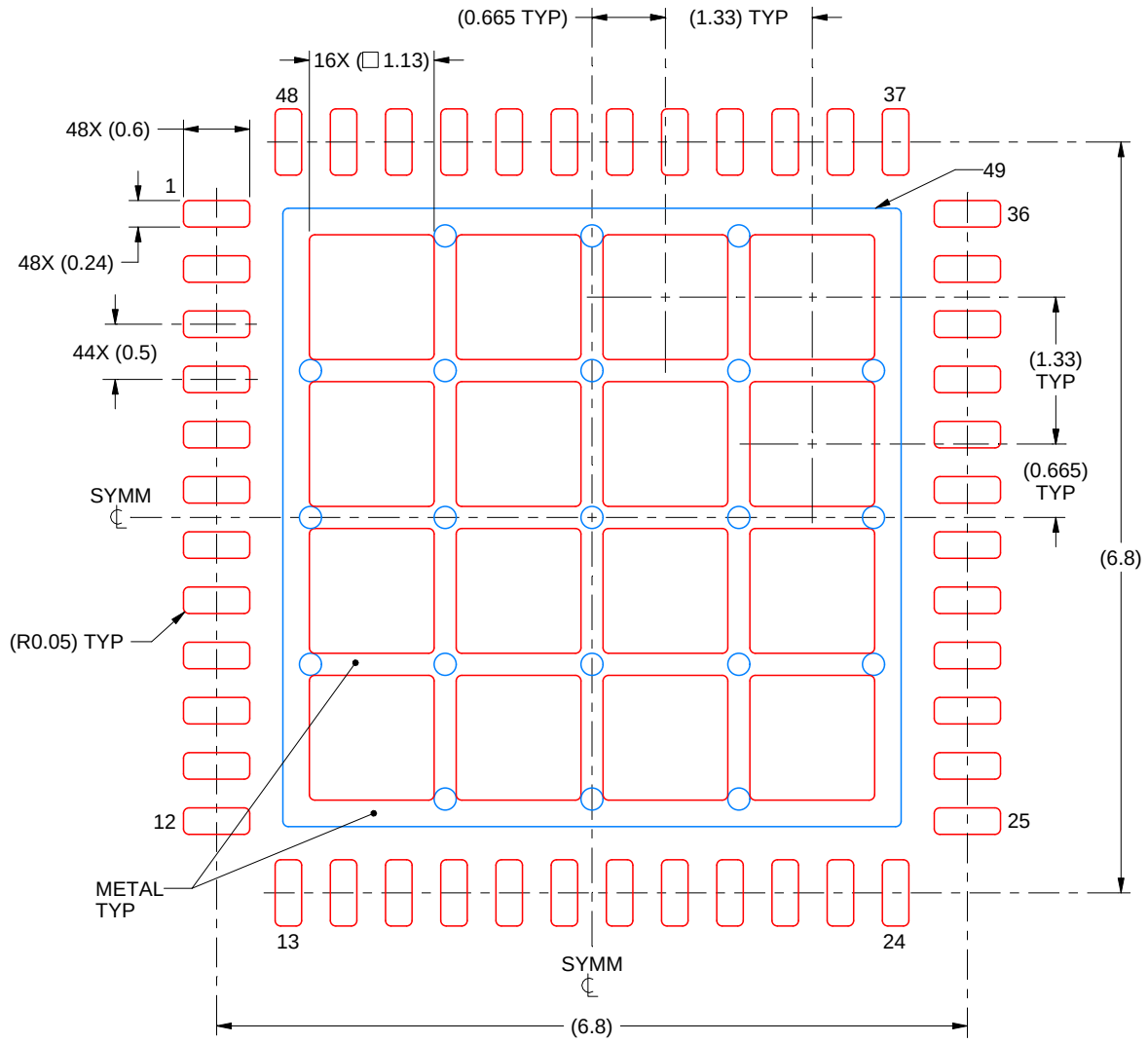


SOLDER MASK DETAILS

4219046/B 11/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
66% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

4219046/B 11/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス· デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件、または ti.com やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265