SBAS237E – DECEMBER 2001 – REVISED JUNE 2005

14-Bit, 40MHz Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **HIGH DYNAMIC RANGE:**
  - **High SFDR: 83dB at 10MHz f_{IN}**
  - **High SNR: 75dB at 10MHz f_{IN}**
- **ON-BOARD TRACK-AND-HOLD:**
  - **Differential Inputs**
  - **Selectable Full-Scale Input Range**
- **FLEXIBLE CLOCKING:**
  - **Differential or Single-Ended**
  - **Accepts Sine or Square Wave Clocking Down to $0.5V_{PP}$**
  - **Variable Threshold Level**

APPLICATIONS

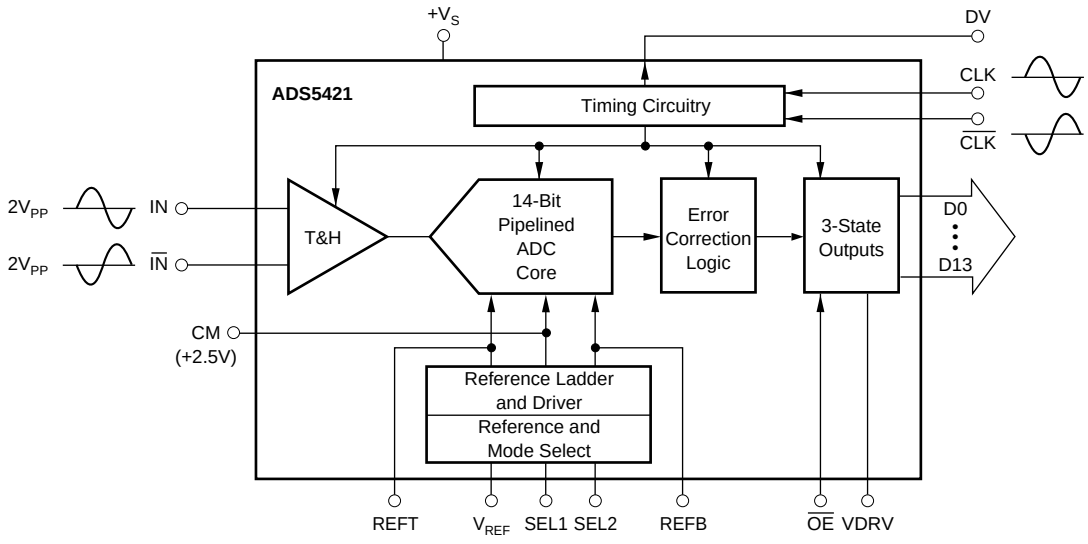
- **COMMUNICATIONS RECEIVERS**
- **TEST INSTRUMENTATION**
- **PROFESSIONAL CCD IMAGING**

DESCRIPTION

The ADS5421 is a high-dynamic range 14-bit, 40MHz, pipelined Analog-to-Digital Converter (ADC). It includes a high-bandwidth linear track-and-hold amplifier that gives excellent spurious performance up to and beyond the Nyquist rate. The clock input can accept a low-level differential sine wave or square wave signal down to $0.5V_{PP}$, further improving the Signal-to-Noise Ratio (SNR) performance.

The ADS5421 has a $4V_{PP}$ differential input range ($2V_{PP}$ • 2 inputs) for optimum Spurious-Free Dynamic Range (SFDR). The differential operation gives the lowest even-order harmonic components. A lower input voltage can also be selected using the internal references, further optimizing SFDR.

The ADS5421 is available in a small LQFP-64 package.



ABSOLUTE MAXIMUM RATINGS[1]

$+V_{SA}$, $+V_{SD}$, VDRV	+6V
Analog Input	(–0.3V) to ($+V_S$ + 0.3V)
Logic Input	(–0.3V) to ($+V_S$ + 0.3V)
Case Temperature	+100°C
Junction Temperature	+150°C
Storage Temperature	+150°C

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

EVALUATION BOARD

PRODUCT	DESCRIPTION	USER'S GUIDE
ADS5421EVM	Populated Evaluation Board	SBAU084

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION[1]

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS5421Y	LQFP-64	PM	–40°C to +85°C	ADS5421Y	ADS5421Y/T	Tape and Reel, 250
"	"	"	"	"	ADS5421Y/R	Tape and Reel, 1500

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ELECTRICAL CHARACTERISTICS

T_A = specified temperature range, typical at +25°C, $+V_{SA}$ = $+V_{SD}$ = +5V, differential input range = 1.5V to 3.5V each input ($4V_{PP}$), sampling rate = 40MHz, internal reference, VDRV = +3V, and –1dBFS, unless otherwise noted.

PARAMETER	CONDITIONS	ADS5421Y MIN	ADS5421Y TYP	ADS5421Y MAX	UNITS
RESOLUTION			14 Tested		Bits
SPECIFIED TEMPERATURE RANGE	Ambient Air		–40 to +85		°C
ANALOG INPUT					
Standard Differential Input Range	Full-Scale = $4V_{PP}$	1.5		3.5	V
Common-Mode Voltage			2.5		V
Optional Input Range	Selectable		$3V_{PP}$		V
Analog Input Bias Current			1		µA
Analog Input Bandwidth			500		MHz
Input Capacitance			9		pF
CONVERSION CHARACTERISTICS					
Sample Rate		1M		40M	Samples/sec
Data Latency			10		Clk Cyc
DYNAMIC CHARACTERISTICS					
Differential Linearity Error (largest code error)					
f = 1MHz			±0.5		LSB
f = 10MHz			±0.5	±1.0	LSB
No Missing Codes			Tested		
Integral Nonlinearity Error, f = 1MHz			±2.5		LSB
Spurious-Free Dynamic Range[1]					
f = 1MHz			88		dBFS[2]
f = 10MHz		78	85		dBFS
f = 30MHz			82		dBFS
2-Tone Intermodulation Distortion[3]					
f = 14.5MHz and 15.5MHz (–7dB each tone)			–90		dBc
Signal-to-Noise Ratio (SNR)					
f = 1MHz			76		dBFS
f = 10MHz		72	75		dBFS
f = 30MHz			75		dBFS
Signal-to-(Noise + Distortion) (SINAD)					
f = 1MHz			75		dB
f = 10MHz		72	74		dB
f = 30MHz			74		dBFS
Effective Number of Bits[4]	f = 1MHz		12.2		Bits
Output Noise	IN and $\overline{IN}$ tied to CM		0.4		LSB rms
Aperture Delay Time			3		ns
Aperture Jitter			1		ps rms
Over-Voltage Recovery Time			5		ns
Full-Scale Step Acquisition Time			5		ns

ELECTRICAL CHARACTERISTICS (Cont.)

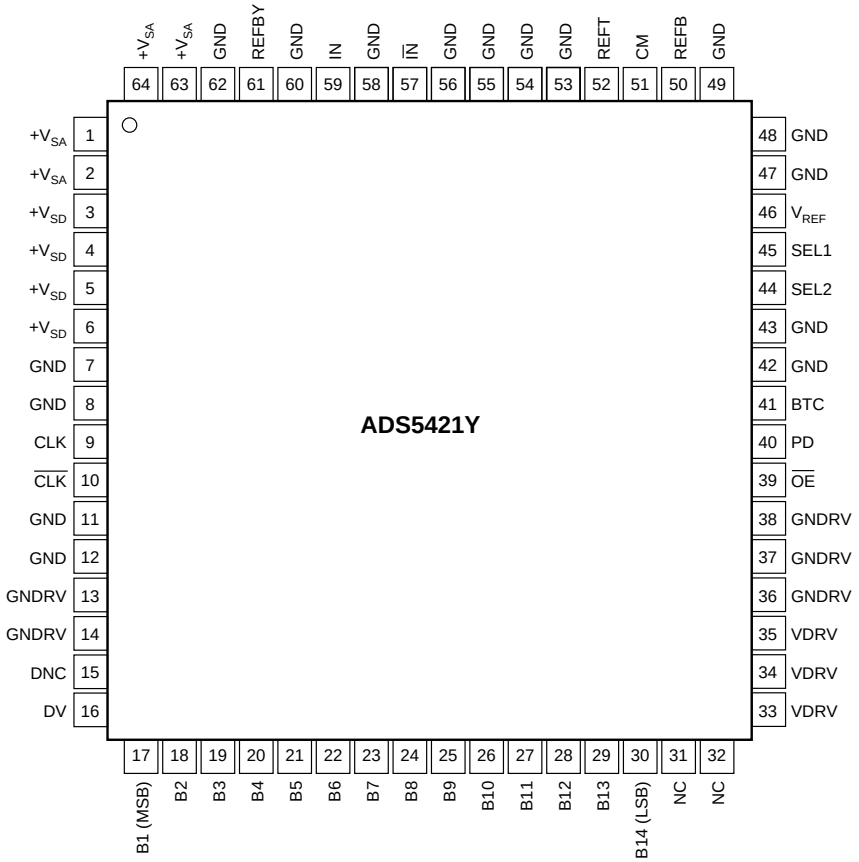
T_A = specified temperature range, typical at +25°C, $+V_{SA}$ = $+V_{SD}$ = +5V, differential input range = 1.5V to 3.5V each input ($4V_{PP}$), sampling rate = 40MHz, internal reference, VDRV = +3V, and –1dBFS, unless otherwise noted.

PARAMETER	CONDITIONS	ADS5421Y MIN	ADS5421Y TYP	ADS5421Y MAX	UNITS
DIGITAL INPUTS					
Clock Input	Rising Edge of Convert Clock	+0.5		$+V_{SD}$	V_{PP}
Logic Family (other than clock inputs)			+3V/+5V Compatible CMOS		
High Level Input Current[5] (V_{IN} = 5V)				100	µA
Low Level Input Current (V_{IN} = 0V)				10	µA
High Level Input Voltage		+2.0			V
Low Level Input Voltage				+1.0	V
Input Capacitance			5		pF
DIGITAL OUTPUTS[6]					
Logic Family			+3V/+5V Compatible CMOS		
Logic Coding			Straight Offset Binary		
Low Output Voltage (I_{OL} = 50µA to 0.5mA)	VDRV = 3V			+0.2	V
High Output Voltage (I_{OH} = 50µA to 0.5mA)		+2.5			V
Low Output Voltage (I_{OL} = 50µA to 1.6mA)	VDRV = 5V			+0.2	V
High Output Voltage (I_{OH} = 50µA to 1.6mA)		+2.5			V
3-State Enable Time	$\overline{OE}$ = LOW		20	40	ns
3-State Disable Time	$\overline{OE}$ = HIGH		2	10	ns
Output Capacitance			5		pF
ACCURACY					
Zero Error (Referred to –FS)	at +25°C		±0.5	±1.0	%FS
Zero Error Drift (Referred to –FS)			15		ppm/°C
Gain Error[7]	at +25°C		±0.2	±1.0	%FS
Gain Error Drift[7]			35		ppm/°C
Power-Supply Rejection of Gain	ΔV_S = ±5%		68		dB
Internal REF Tolerance (V_{REFT}, V_{REFB})	Deviation from Ideal		±10	±50	mV
External REF Voltage Range	(V_{REFT} – V_{REFB})	1.4	2	2.025	V
Reference Input Resistance			1.0		kΩ
POWER-SUPPLY REQUIREMENTS					
Supply Voltage: $+V_{SA}$, $+V_{SD}$	Operating, f_{IN} = 10MHz	+4.75	+5.0	+5.25	V
Supply Current: $+I_S$	Operating, f_{IN} = 10MHz		170		mA
Output Driver Supply Current (VDRV)			12		mA
Power Dissipation: VDRV = 5V			900		mW
VDRV = 3V			850	925	mW
Power Down	Operating		40		mW
Thermal Resistance, θ_{JA}					
LQFP-64			48		°C/W

NOTES: (1) Spurious-Free Dynamic Range refers to the magnitude of the largest harmonic. (2) dBFS means dB relative to Full-Scale. (3) 2-tone intermodulation distortion is referred to the largest fundamental tone. This number will be 6dB higher if it is referred to the magnitude of the 2-tone fundamental envelope. (4) Effective Number of Bits (ENOB) is defined by (SINAD – 1.76)/6.02. (5) A 50kΩ pull-down resistor is inserted internally. (6) Recommended maximum capacitance loading, 15pF. (7) Includes internal reference.

PIN CONFIGURATION

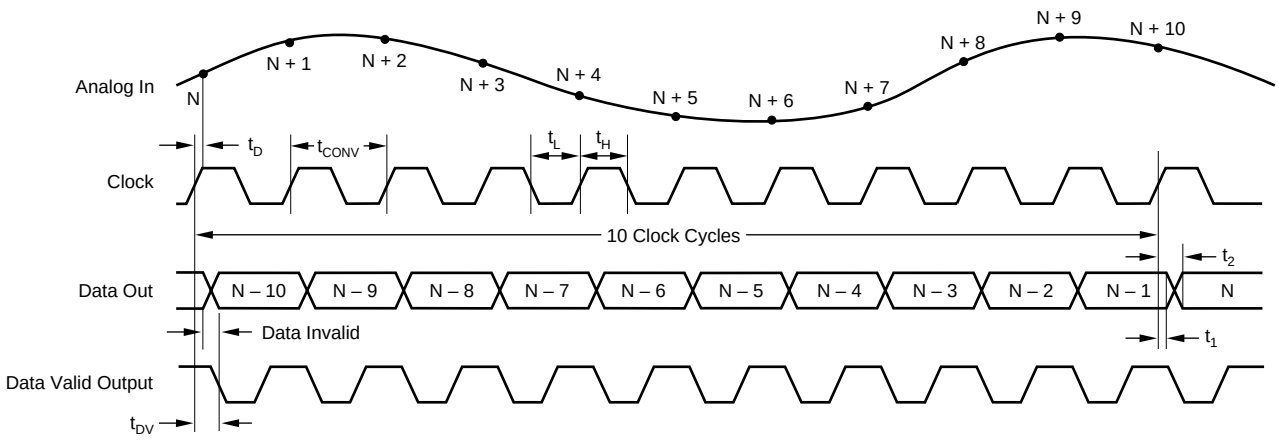
Top View **TQFP**



PIN DESCRIPTIONS

PIN	I/O	DESIGNATOR	DESCRIPTION	PIN	I/O	DESIGNATOR	DESCRIPTION
1		$+V_{SA}$	Analog Supply Voltage	33		VDRV	Output Driver Supply Voltage
2		$+V_{SA}$	Analog Supply Voltage	34		VDRV	Output Driver Supply Voltage
3		$+V_{SD}$	Digital Supply Voltage	35		VDRV	Output Driver Supply Voltage
4		$+V_{SD}$	Digital Supply Voltage	36		GNDRV	Ground
5		$+V_{SD}$	Digital Supply Voltage	37		GNDRV	Ground
6		$+V_{SD}$	Digital Supply Voltage	38		GNDRV	Ground
7		GND	Ground	39		$\overline{OE}$	Output Enable: HI = High Impedance
8		GND	Ground	40	I	PD	Power Down: HI = Power Down; LO = Normal
9	I	CLK	Clock Input	41	I	BTC	HI = Binary Two's Complement
10	I	$\overline{CLK}$	Complementary Clock Input	42		GND	Ground
11		GND	Ground	43		GND	Ground
12		GND	Ground	44		SEL2	Reference Select 2: See Table on Page 5
13		GNDRV	Ground	45		SEL1	Reference Select 1: See Table on Page 5
14		GNDRV	Ground	46		V_{REF}	Internal Reference Voltage
15		DNC	Do Not Connect	47		GND	Ground
16		DV	Data Valid Pulse: HI = Data Valid	48		GND	Ground
17	O	B1	Data Bit 1 (D13) (MSB)	49		GND	Ground
18	O	B2	Data Bit 2 (D12)	50		REFB	Bottom Reference Voltage Bypass
19	O	B3	Data Bit 3 (D11)	51		CM	Common-Mode Voltage (Midscale)
20	O	B4	Data Bit 4 (D10)	52		REFT	Top Reference Voltage Bypass
21	O	B5	Data Bit 5 (D9)	53		GND	Ground
22	O	B6	Data Bit 6 (D8)	54		GND	Ground
23	O	B7	Data Bit 7 (D7)	55		GND	Ground
24	O	B8	Data Bit 8 (D6)	56		GND	Ground
25	O	B9	Data Bit 9 (D5)	57	I	$\overline{IN}$	Complementary Analog Input
26	O	B10	Data Bit 10 (D4)	58		GND	Ground
27	O	B11	Data Bit 11 (D3)	59	I	IN	Analog Input
28	O	B12	Data Bit 12 (D2)	60		GND	Ground
29	O	B13	Data Bit 13 (D1)	61		REFBY	Reference Bypass
30	O	B14	Data Bit 14 (D0) (LSB)	62		GND	Ground
31		NC	No Internal Connection	63		$+V_{SA}$	Analog Supply Voltage
32		NC	No Internal Connection	64		$+V_{SA}$	Analog Supply Voltage

TIMING DIAGRAM



SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{CONV}	Convert Clock Period	25		1µs	ns
t_L	Clock Pulse LOW	11.5	$t_{CONV}/2$		ns
t_H	Clock Pulse HIGH	11.5	$t_{CONV}/2$		ns
t_D	Aperture Delay		3		ns
t_1	Data Hold Time, C_L = 0pF	3.9	7.2		ns
t_2	New Data Delay Time, C_L = 15pF max		12.7		ns
t_{DV}	Data Valid Output, C_L = 15pF		4.4		ns

REFERENCE AND FULL-SCALE RANGE SELECT TABLE

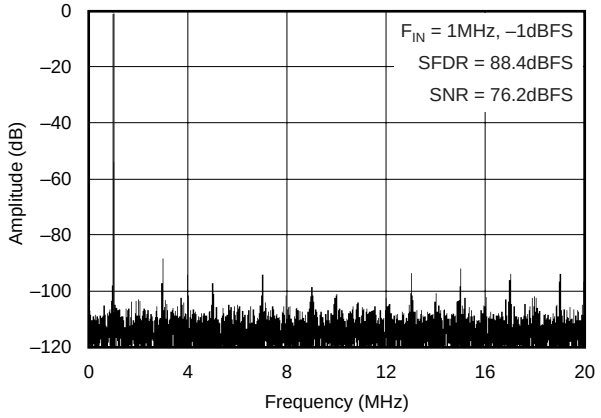
DESIRED FULL-SCALE RANGE	SEL1	SEL2	INTERNAL V_{REF}
$4V_{PP}$	GND	GND	2V
$3V_{PP}$	GND	$+V_{SA}$	1.5V

NOTE: For external reference operation, tie V_{REF} to $+V_{SA}$. The full-scale range will be 2x the reference value. For example, selecting a 2V external reference will set the full-scale values of 1.5V to 3.5V for both IN and $\overline{IN}$ inputs.

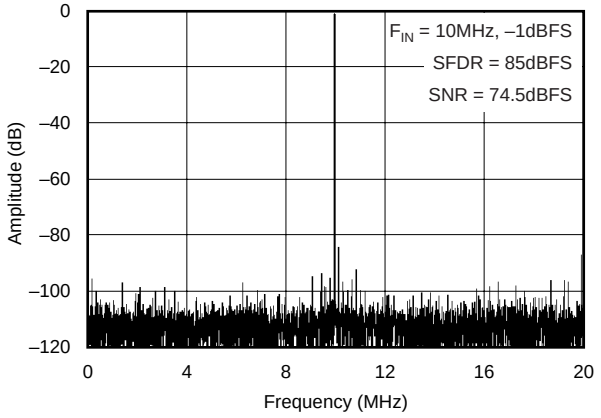
TYPICAL CHARACTERISTICS

T_A = 25°C, $+V_{SA}$ = $+V_{SD}$ = +5V, differential input range = 1.5V to 3.5V each input ($4V_{PP}$), sampling rate = 40MSPS, internal reference, and VDRV = 3V, unless otherwise noted.

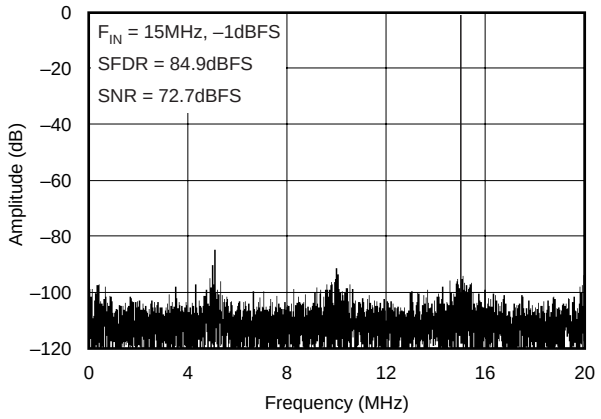
SPECTRAL PERFORMANCE



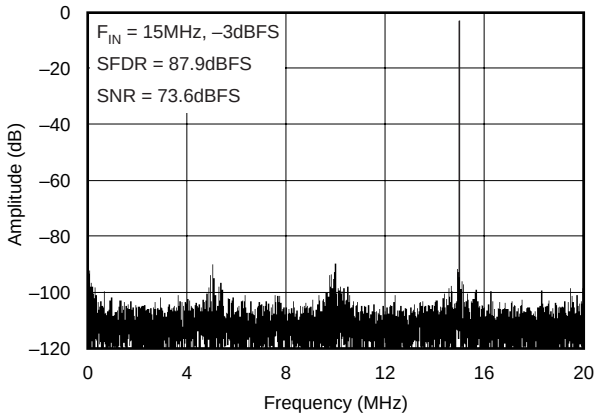
SPECTRAL PERFORMANCE



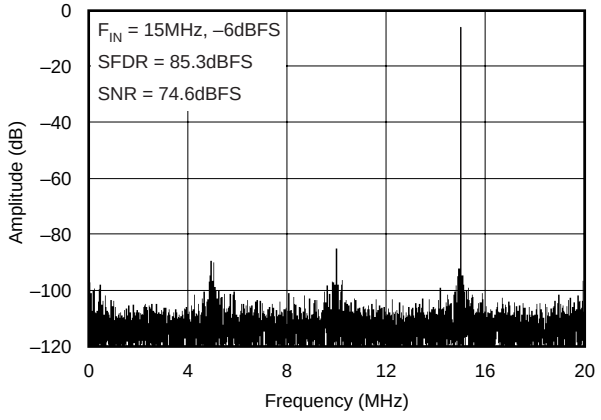
SPECTRAL PERFORMANCE



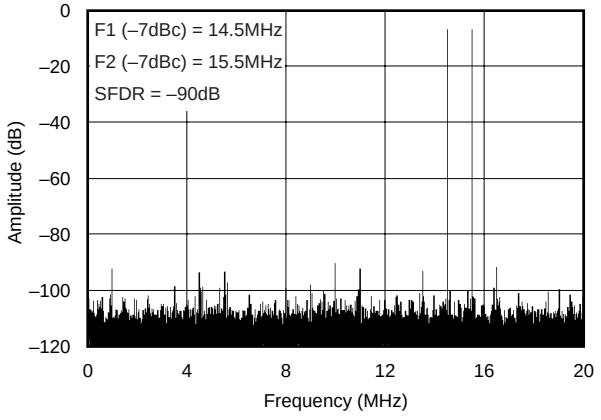
SPECTRAL PERFORMANCE



SPECTRAL PERFORMANCE



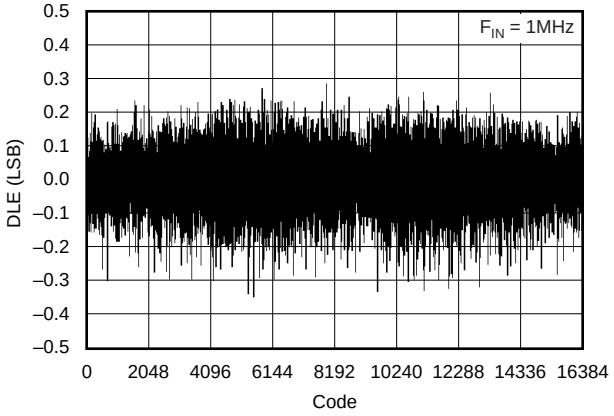
2-TONE INTERMODULATION



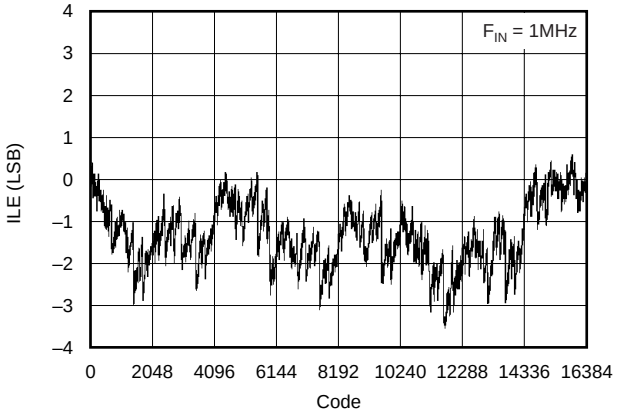
TYPICAL CHARACTERISTICS (Cont.)

T_A = 25°C, $+V_{SA}$ = $+V_{SD}$ = +5V, differential input range = 1.5V to 3.5V each input ($4V_{PP}$), sampling rate = 40MSPS, internal reference, and VDRV = 3V, unless otherwise noted.

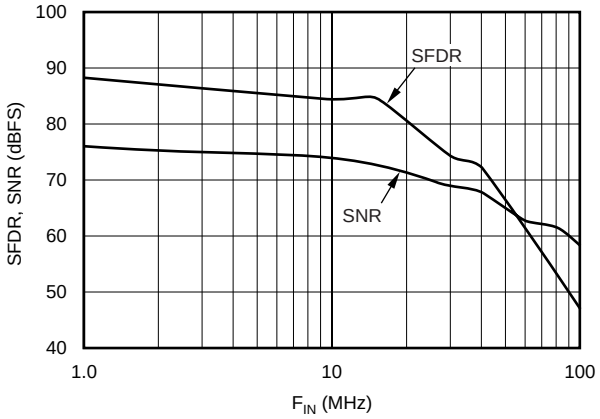
DIFFERENTIAL LINEARITY ERROR



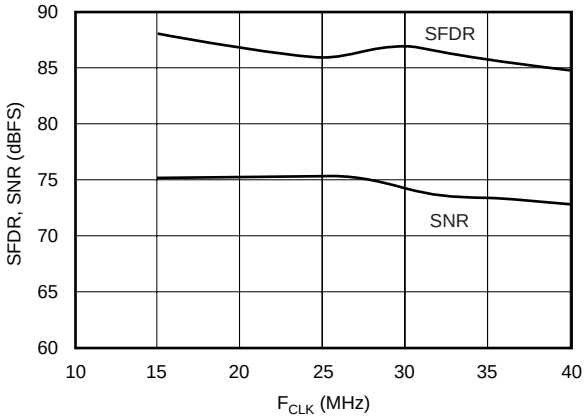
INTEGRAL LINEARITY ERROR



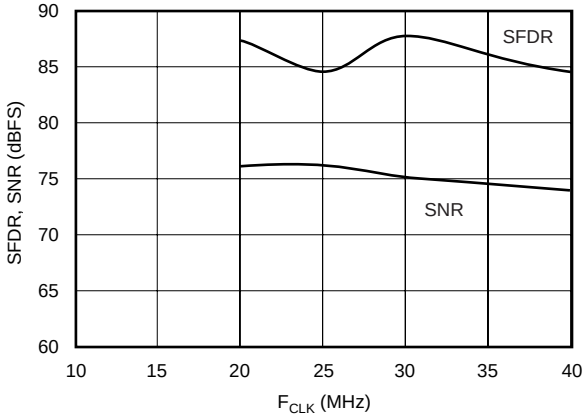
SFDR AND SNR vs INPUT FREQUENCY
(F_{CLK} = 40MHz)



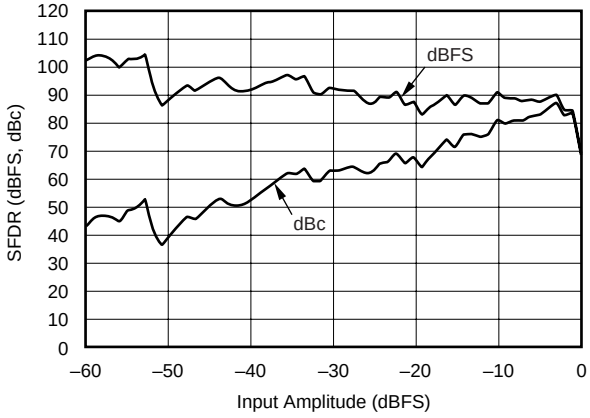
SFDR AND SNR vs CLOCK FREQUENCY
(F_{IN} = 15MHz)



SFDR AND SNR vs CLOCK FREQUENCY
(F_{IN} = 10MHz)

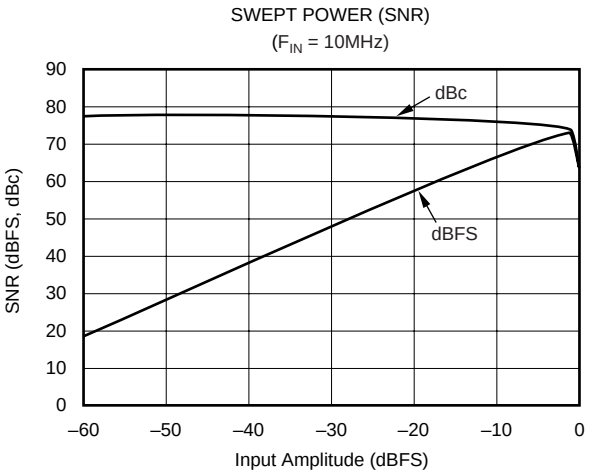


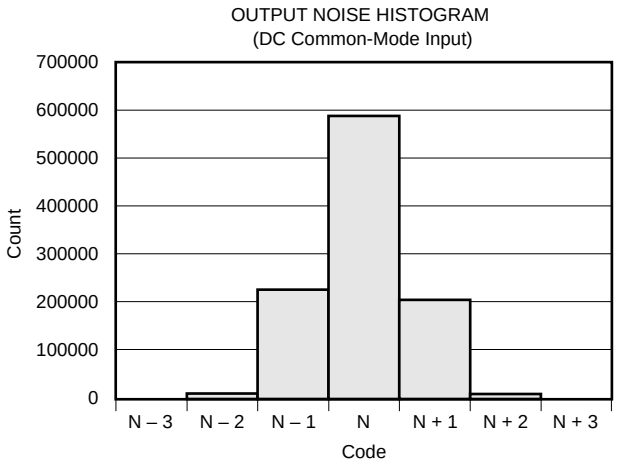
SWEPT POWER (SFDR)
(F_{IN} = 10MHz)



TYPICAL CHARACTERISTICS (Cont.)

T_A = 25°C, $+V_{SA}$ = $+V_{SD}$ = +5V, differential input range = 1.5V to 3.5V each input ($4V_{PP}$), sampling rate = 40MSPS, internal reference, and VDRV = 3V, unless otherwise noted.





APPLICATION INFORMATION

THEORY OF OPERATION

The ADS5421 is a high-speed, high-performance, CMOS ADC build with a fully differential pipeline architecture. Each stage contains a low-resolution quantizer and digital error correction logic ensuring good differential linearity. The conversion process is initiated by a rising edge of the external convert clock. Once the signal is captured by the input track-and-hold amplifier, the bits are sequentially encoded starting with the Most Significant Bit (MSB). This process results in a data latency of 10 clock cycles after which the output data is available as a 14-bit parallel word either coded in a Straight Offset Binary or Binary Two's Complement format.

The analog input of the ADS5421 consists of a differential track-and-hold circuit, as shown in Figure 1. The differential topology produces a high level of AC performance at high sampling rates. It also results in a very high usable input bandwidth—especially important for Intermediate Frequency (IF) or undersampling applications. Both inputs (IN, $\overline{IN}$) require external biasing up to a common-mode voltage that is typically at the mid-supply level ($+V_S/2$). This is because the on-resistance of the CMOS switches is lowest at this voltage, minimizing the effects of the signal-dependent, nonlinearity of R_{ON}. For ease of use, the ADS5421 incorporates a selectable voltage reference, a versatile clock input, and a logic output driver designed to interface to 3V or 5V logic.

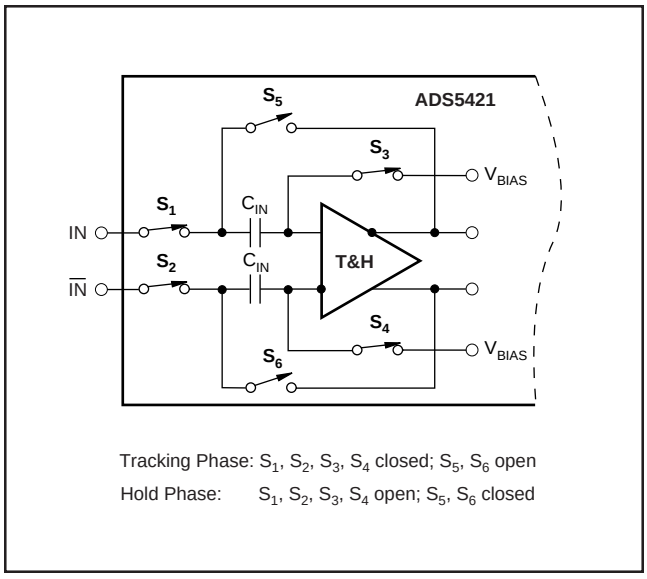


FIGURE 1. Simplified Circuit of Input Track-and-Hold Amplifier.

ANALOG INPUTS

TYPES OF APPLICATIONS

The analog input of the ADS5421 can be configured in various ways and driven with different circuits, depending on the application and the desired level of performance. Offering an extremely high dynamic range at high input frequencies, the ADS5421 is particularly well suited for communication systems that digitize wideband signals. Features on the ADS5421, like the input range selector, or the option of an external reference, provide the needed flexibility to accommodate a wide range of applications. In any case, the analog interface/driver requirements should be carefully examined before selecting the appropriate circuit configuration. The circuit definition should include considerations on the input frequency spectrum and amplitude, as well as the available power supplies.

DIFFERENTIAL INPUTS

The ADS5421 input structure is designed to accept the applied signal in differential format. Differential operation of the ADS5421 requires an input signal that consists of an in-phase and a 180° out-of-phase component simultaneously applied to the inputs (IN, $\overline{IN}$). Differential signals offer a number of advantages, which in many applications will be instrumental in achieving the best harmonic performance of the ADS5421:

- The signal amplitude is half of that required for the single-ended operation and is, therefore, less demanding to achieve while maintaining good linearity performance from the signal source.
- The reduced signal swing allows for more headroom of the interface circuitry and, therefore, a wider selection of the best suitable driver amplifier.
- Even-order harmonics are minimized.
- Improves the noise immunity based on the common-mode input rejection of the converter.

Both inputs are identical in terms of their impedance and performance with the exception that by applying the signal to the complementary input ($\overline{IN}$) instead of the IN input will invert the orientation of the input signal relative to the output code.

INPUT FULL-SCALE RANGE VERSUS PERFORMANCE

Employing dual-supply amplifiers and AC-coupling will usually yield the best results. DC-coupling and/or single-supply amplifiers impose additional design constraints due to their headroom requirements, especially when selecting the $4V_{PP}$ input range. The full-scale input range of the ADS5421 is defined either by the settings of the reference select pins (SEL1, SEL2) or by an external reference voltage (see Table I). By choosing between the different signal input ranges, trade-offs can be made between noise and distortion performance. For maximizing the SNR—important for time-domain applications—the $4V_{PP}$ range may be selected. This range may also be used with low-level (–6dBFS to –40dBFS) but high-frequency inputs (multi-tone). The $3V_{PP}$ range may be considered for achieving a combination of both low-noise and distortion performance. Here, the SNR number is typically 3dB down compared to the $4V_{PP}$ range, while an improvement in the distortion performance of the driver amplifier may be realized due to the reduced output power level required.

INPUT BIASING (V_{CM})

The ADS5421 operates from a single +5V supply, and requires each of the analog inputs to be externally biased to a common-mode voltage of typically +2.5V. This allows a symmetrical signal swing while maintaining sufficient headroom to either supply rail. Communication systems are usually AC-coupled in between signal processing stages, making it convenient to set individual common-mode voltages and allow optimizing the DC operating point for each stage. Other applications, such as imaging, process mainly unipolar or DC-restored signals. In this case, the common-mode voltage may be shifted such that the full input range of the converter is utilized.

It should be noted that the CM pin is not internally buffered, but ties directly to the reference ladder. Therefore, it is recommended to keep loading of this pin to a minimum (< 100µA) to avoid an increase in the nonlinearity of the converter. Additionally, the DC voltage at the CM pin is not precisely +2.5V, but is subject to the tolerance of the top and bottom references, as well as the resistor ladder. Furthermore, the common-mode voltage typically declines with an increase in sampling frequency. This, however, does not affect the performance.

INPUT IMPEDANCE

The input of the ADS5421 is capacitive, and the driving source needs to provide the slew current to charge or discharge the input sampling capacitor while the track-and-hold amplifier is in track mode (see Figure 1). This effectively results in a dynamic input impedance that is a function of the sampling frequency. Figure 2 depicts the differential input impedance of the ADS5421 as a function of the input frequency.

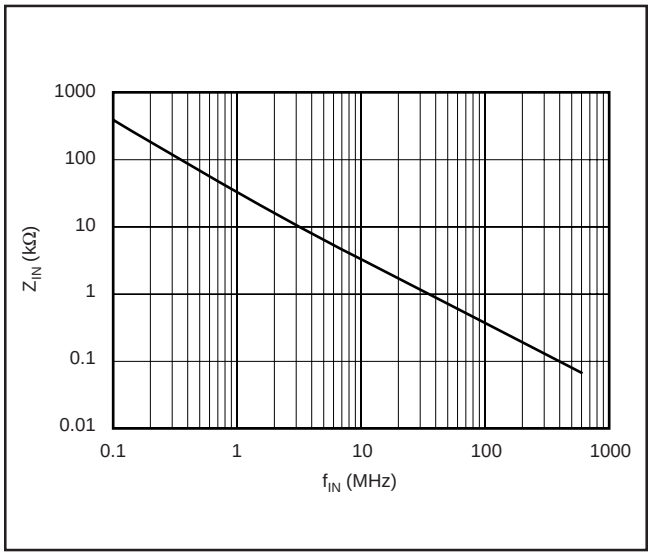


FIGURE 2. Differential Input Impedance vs Input Frequency.

For applications that use op amps to drive the ADC, it is recommended that a series resistor be added between the amplifier output and the converter inputs. This will isolate the capacitive input of the converter from the driving source and avoid gain peaking, or instability; furthermore, it will create a 1st-order, low-pass filter in conjunction with the specified input capacitance of the ADS5421. Its cutoff frequency can be adjusted further by adding an external shunt capacitor from each signal input to ground. The optimum values of this RC network, however, depend on a variety of factors, including the ADS5421 sampling rate, the selected op amp, the interface configuration, and the particular application (time domain versus frequency domain). Generally, increasing the size of the series resistor and/or capacitor will improve the SNR, however, depending on the signal source, large resistor values may be detrimental to the harmonic distortion performance. In any case, the use of the RC network is optional but optimizing the values to adapt to the specific application is encouraged.

ANALOG INPUT DRIVER CONFIGURATIONS

The following section provides some principal circuit suggestions on how to interface the analog input signal to the ADS5421. Applications that have a requirement for DC-coupling a new differential amplifier, such as the THS4502, can be used to drive the ADS5421, as shown in Figure 3. The THS4502 amplifier allows a single-ended to differential conversion to be performed easily, which reduces component cost. In addition, the V_{CM} pin on the THS4502 can be directly tied to the common-mode pin (CM) of the ADS5421 in order to set up the necessary bias voltage for the converter inputs. As shown in Figure 3, the THS4502 is configured for unity gain. If required, higher gain can easily be configured, and a low-pass filter can be created by adding small capacitors (e.g., 10pF) in parallel to the feedback resistors. Due to the THS4502 driving a capacitive load, small series resistors in the output ensure stable operation. Further details of this and other functions of the THS4502 may be found in its product datasheet located at the Texas Instruments web site (www.ti.com). In general, differential amplifiers provide for a high-performance driver solution for baseband applications, and different differential amplifier models can be selected depending on the system requirements.

TRANSFORMER-COUPLED INTERFACE CIRCUITS

If the application allows for AC-coupling but requires a signal conversion from a single-ended source to drive the ADS5421 differentially, using a transformer offers a number of advantages. As a passive component, it does not add to the total noise, and by using a step-up transformer, further signal amplification can be realized. As a result, the signal swing of the amplifier driving the transformer can be reduced, leading to an increased headroom for the amplifier and improved distortion performance.

A transformer interface solution is given in Figure 4. The input signal is assumed to be an IF and bandpass filtered prior to the IF amplifier. Dedicated IF amplifiers are commonly fixed-gain blocks and feature a very high bandwidth, low-noise figure, and a high intercept point, but at the expense of high quiescent currents, which are often around 100mA. The IF amplifier may be AC-coupled, or directly connected to the primary side of the transformer. A variety of miniature RF transformers are readily available from different manufacturers, (e.g., Mini-Circuits, Coilcraft, or Trak). For selection, it is important to carefully examine the application requirements and determine the correct model, the desired impedance ratio, and frequency characteristics. Furthermore, the appropriate model must support the targeted distortion level and should not exhibit any core saturation at full-scale voltage levels. The transformer center tap can be directly tied to the CM pin of the converter because it does not appreciably load the ADC reference (see Figure 4). The value of termination resistor R_T must be chosen to satisfy the termination requirements of the source impedance (R_S). It can be calculated using the equation $R_T = n^2 \bullet R_S$ to ensure proper impedance matching.

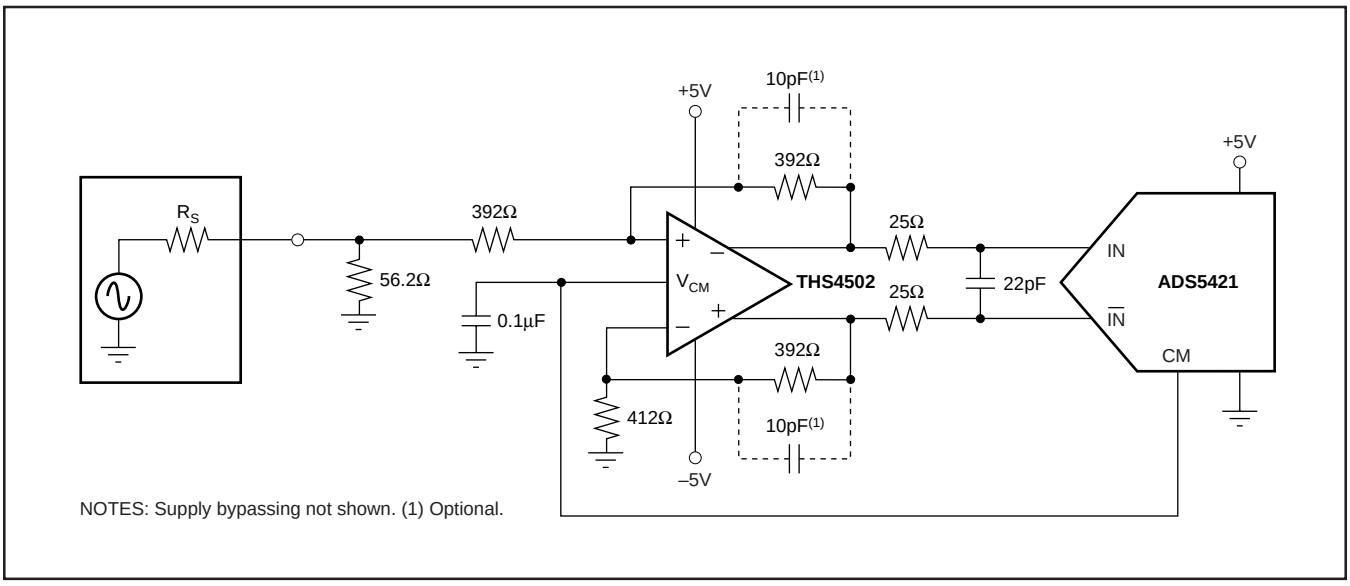


FIGURE 3. Using the THS4502 Differential Amplifier (Gain = 1) to Drive the ADS5421 in a DC-Coupled Configuration.

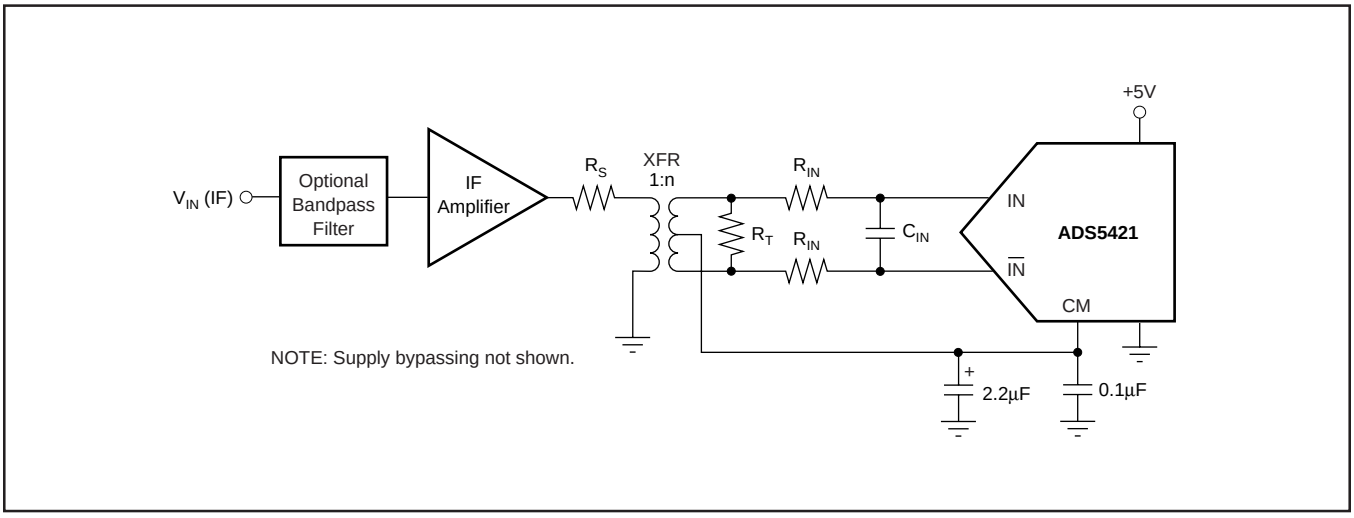


FIGURE 4. Driving the ADS5421 with a Low-Distortion IF Amplifier and a Transformer Suited for IF Sampling Applications.

TRANSFORMER-COUPLED, SINGLE-ENDED-TO-DIFFERENTIAL CONFIGURATION

For applications in which the input frequency is limited to approximately 10MHz (e.g., baseband), a high-speed operational amplifier may be used. The OPA847 is configured for the noninverting mode; this amplifies the single-ended input signal and drives the primary of a RF transformer (see Figure 5). To maintain the very low distortion performance of the OPA847, it may be advantageous to set the full-scale input range of the ADS5421 to $3V_{PP}$.

The circuit also shows the use of an additional RC low-pass filter placed in series with each converter input. This optional filter can be used to set a defined corner frequency and attenuate some of the wideband noise. The actual component values would need to be tuned for individual application requirements. As a guideline, resistor values are typically in the range of 10Ω to 50Ω, and capacitors in the range of 10pF to 100pF. In any case, the R_{IN} and C_{IN} values should have a low tolerance. This will ensure that the ADS5421 sees closely matched source impedances.

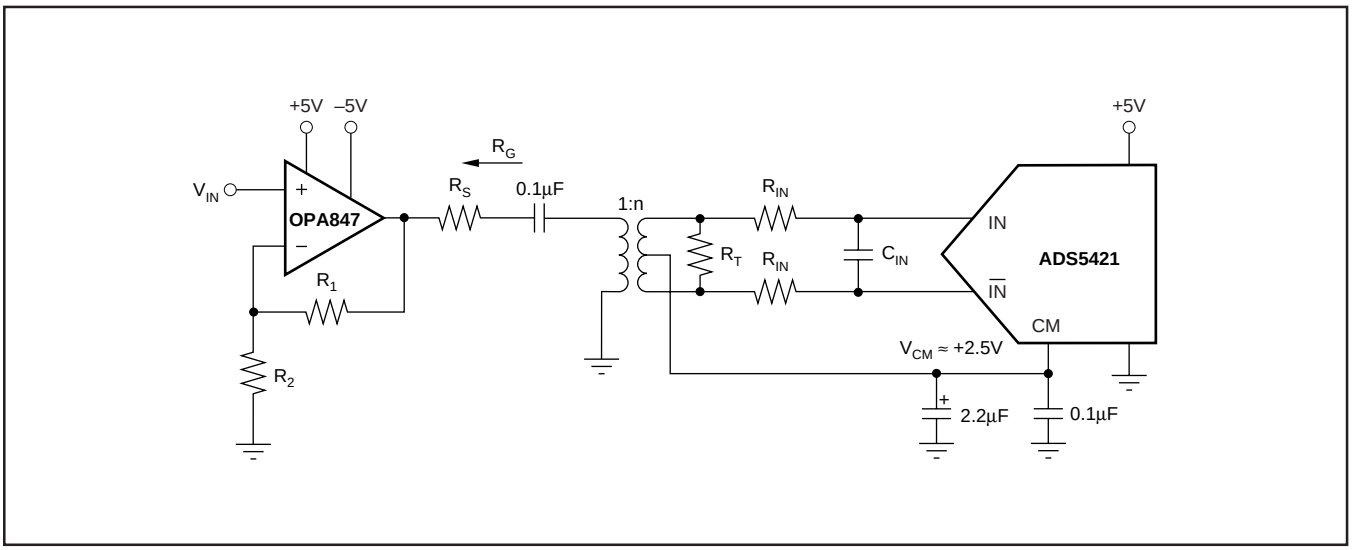


FIGURE 5. Converting a Single-Ended Input Signal into a Differential Signal Using a RF Transformer.

AC-COUPLED, DIFFERENTIAL INTERFACE WITH GAIN

The interface circuit example presented in Figure 6 employs two OPA687s, (decompensated voltage-feedback op amps), optimized for gains of 12V/V or higher. Implementing a new compensation technique allows the OPA847s to operate with a reduced signal gain of 8.5V/V, while maintaining the high loop gain and the associated excellent distortion performance offered by the decompensated architecture. For a detailed discussion on this circuit and the compensation scheme, refer to the OPA847 data sheet (SBOS251) located at www.ti.com. Input transformer, T1, converts the single-ended input signal to a differential signal required at the inverting inputs of the amplifier, which are tuned to provide a 50Ω impedance match to an assumed 50Ω source. To achieve the 50Ω input match at the primary of the 1:2 transformer, the secondary must see a 200Ω load impedance. Both amplifiers are configured for the inverting mode resulting in close gain and phase matching of the differential signal. This technique, along with a highly symmetrical layout, is instrumental in achieving a substantial reduction of the 2nd-harmonic, while retaining excellent 3rd-order performance. A common-mode voltage, V_{CM}, is applied to the noninverting inputs of the OPA847. Additional series 20Ω resistors isolate the output of the op amps from the capacitive load presented by the 40pF capacitors and the input capacitance of the ADS5421. This 20Ω/47pF combination sets a pole at approximately 85MHz and rolls off some of the wideband noise resulting in a reduction of the noise floor.

For the measured 2-tone, 3rd-order distortion for the amplifier portion of the circuit of Figure 6, see Figure 7. The curve is for a total 2-tone envelope of $4V_{PP}$, requiring two tones, each $2V_{PP}$ across the OPA847 outputs. The basic measurement dynamic range for the two close-in spurious tones is approximately 85dBc. The $4V_{PP}$ test does not show measurable 3rd-order spurious until 25MHz.

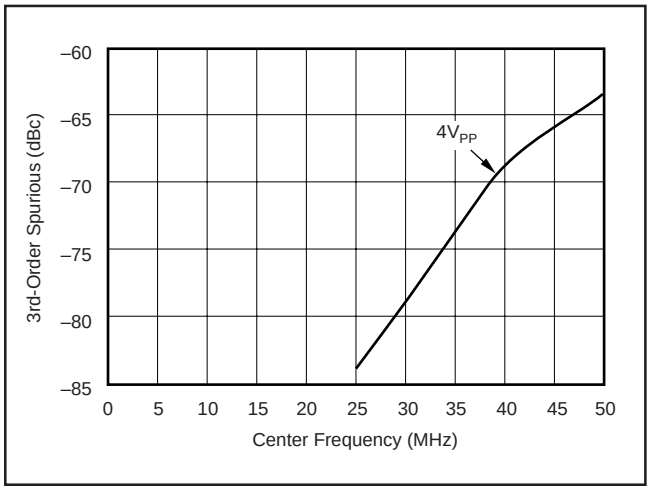


FIGURE 7. Measured 2-Tone, 3rd-Order Distortion for a Differential ADC Driver.

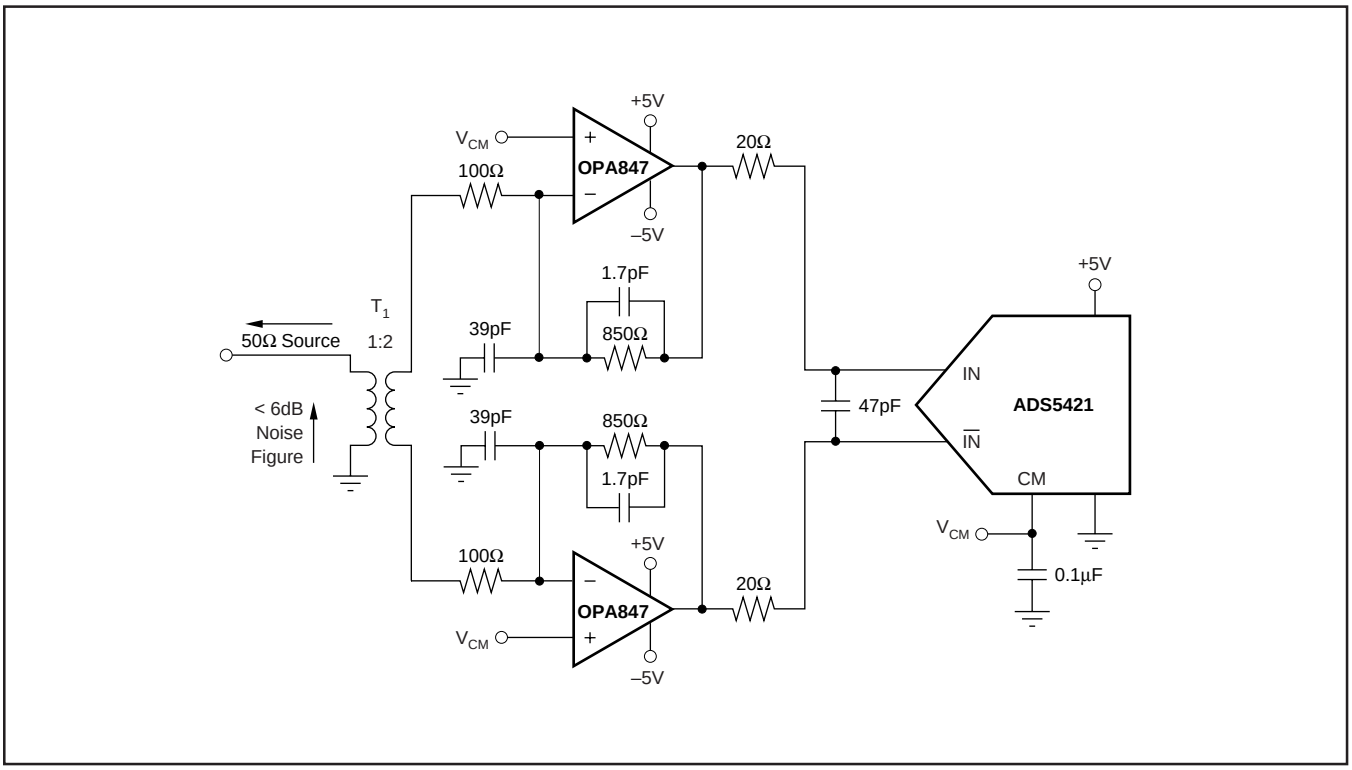


FIGURE 6. High Dynamic Range Interface Circuit with the OPA847 Set for a Gain of +8.5V/V.

REFERENCE

REFERENCE OPERATION

Integrated into the ADS5421 is a bandgap reference circuit, including logic that provides a +1.5V or +2V reference output by selecting the corresponding pin-strap configuration. Table I lists an overview of the possible reference options and pin configurations.

Figure 8 shows the basic model of the internal reference circuit. The functional blocks are a 1V bandgap voltage reference, a selectable gain amplifier, the drivers for the top and bottom reference (REFT, REFB), and the resistive reference ladder. The ladder resistance measures approximately 1kΩ between the REFT and REFB pins. The ladder is split into two equal segments establishing a common-mode voltage at the ladder midpoint, labeled CM. The ADS5421 requires solid bypassing for all reference pins to keep the effects of clock feedthrough to a minimum and to achieve the specified level of performance. Figure 8 shows the recommended decoupling scheme. All 0.1µF capacitors must be located as close to the pins as possible. In addition, pins REFT, CM, and REFB must be decoupled with tantalum surface-mount capacitors (2.2µF or 4.7µF).

When operating the ADS5421 with the internal reference, the effective full-scale input span for each of the inputs, IN and $\overline{IN}$, is determined by the voltage at the V_{REF} pin, given to:

(1)

Input Span (differential, each input) = V_{REF} = (REFT – REFB) in V_{PP}

The top and bottom reference outputs can be used to provide up to 1mA of current (sink or source) to external circuits. Degradation of the differential linearity (DNL) and, consequently, the dynamic performance, of the ADS5421 may occur if this limit is exceeded.

USING EXTERNAL REFERENCES

For even more design flexibility, the ADS5421 can be operated with external references. The utilization of an external reference voltage may be considered for applications requiring higher accuracy, improved temperature stability, or a continuous adjustment of the converter full-scale range. Especially in multichannel applications, the use of a common external reference offers the benefit of improving the gain matching between converters. Selection between internal or external reference operation is controlled through the V_{REF} pin. The internal reference will become disabled if the voltage applied to the V_{REF} pin exceeds +3.5V_{DC}. Once selected, the ADS5421 requires two reference voltages: a top reference voltage applied to the REFT pin and a bottom reference voltage applied to the REFB pin (see Table I). The full-scale range is determined by FSR = 2 x (V_{REFT} – V_{REFB}). It is recommended to maintain the common-mode voltage at +2.5V. As illustrated in Figure 9, a micropower reference (REF1004) and a dual, single-supply amplifier (OPA2234) can be used to generate a precision external reference. Note that the function of the range select pins, SEL1 and SEL2, are disabled while the converter is operating in external reference mode.

DESIRED FULL-SCALE RANGE (FSR) (DIFFERENTIAL)	CONNECT SEL1 (PIN 45) TO:	CONNECT SEL2 (PIN 44) TO:	VOLTAGE AT V_{REF} (PIN 46)	VOLTAGE AT REFT (PIN 52)	VOLTAGE AT REFB (PIN 50)
$4V_{PP}$ (+16dBm)	GND	GND	+2.0V	+3.5V	+1.5V
$3V_{PP}$ (+13dBm)	GND	$+V_{SA}$	+1.5V	+3.25V	+1.75V
External Reference	—	—	> +3.5V	+3.2V to +3.5V	+1.5V to +1.8V

TABLE I. Reference Pin Configurations and Corresponding Voltages on the Reference Pins.

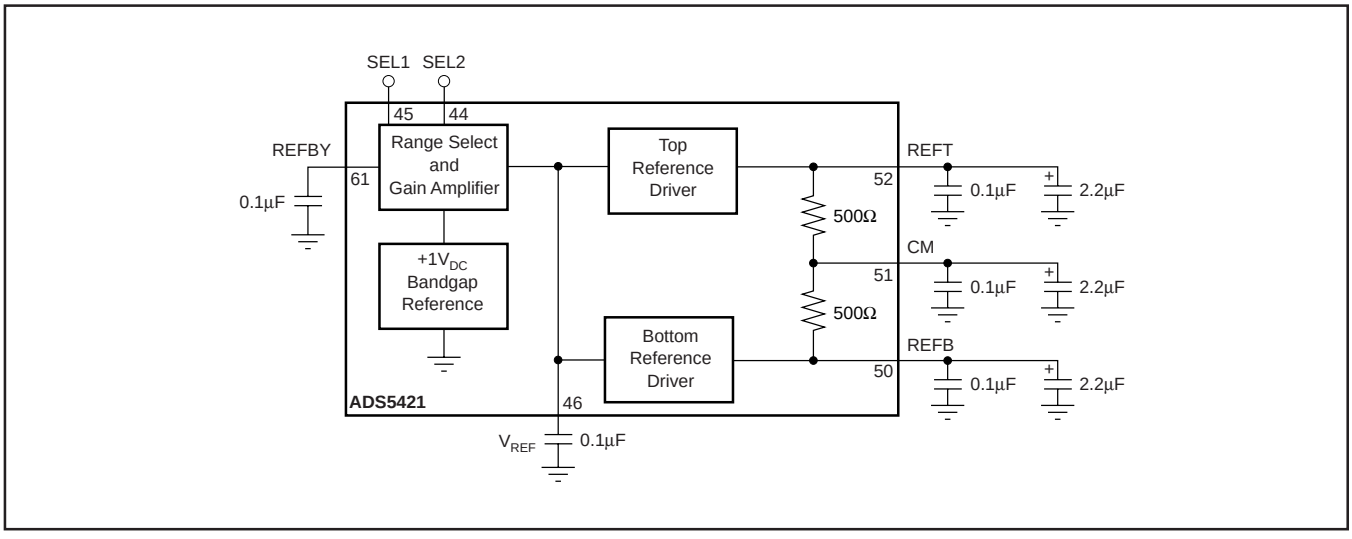


FIGURE 8. Internal Reference Circuit of the ADS5421 and Recommended Bypass Scheme.

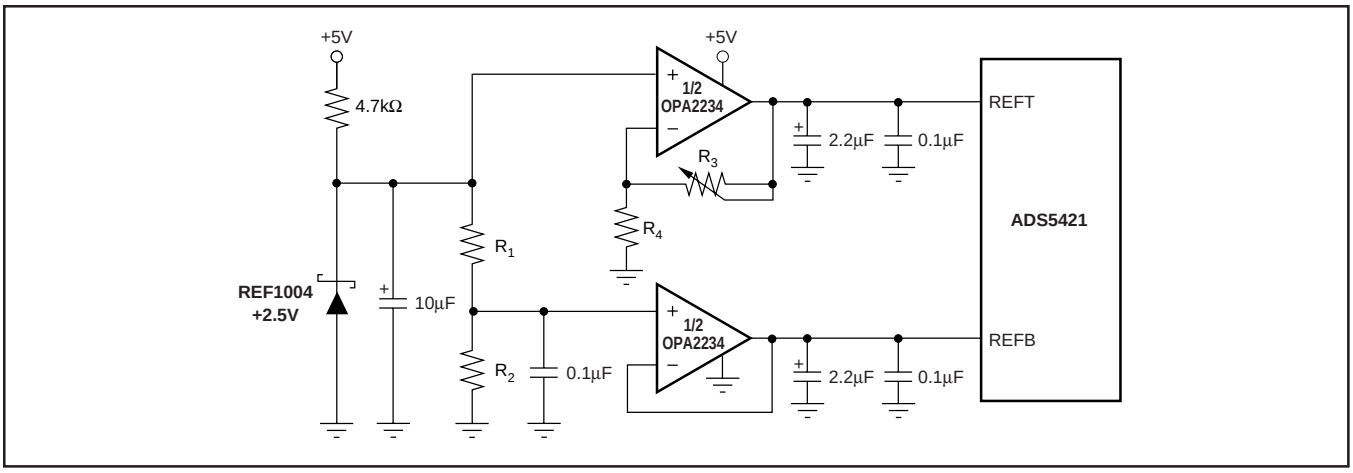


FIGURE 9. Example for an External Reference Circuit Using a Dual, Single-Supply Op Amp.

DIGITAL INPUTS AND OUTPUTS

CLOCK INPUT

Unlike most ADCs, the ADS5421 contains internal clock conditioning circuitry. This enables the converter to adapt to a variety of application requirements and different clock sources. With no input signal connected to either clock pin, the threshold level is set to approximately +1.6V by the on-chip resistive voltage divider, as shown in Figure 10. The parallel combination of R_1 || R_2 and R_3 || R_4 sets the input impedance of the clock inputs (CLK, $\overline{CLK}$) to approximately 2.7kΩ single-ended, or 5.5kΩ differentially. The associated ground referenced input capacitance is approximately 5pF for each input. If a logic voltage other than the nominal +1.6V is desired, the clock inputs can be externally driven to establish an alternate threshold voltage.

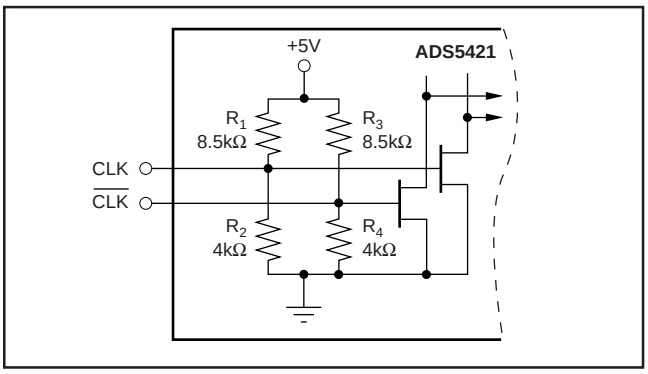


FIGURE 10. The Differential Clock Inputs are Internally Biased.

The ADS5421 can be interfaced to standard TTL or CMOS logic and accepts 3V or 5V compliant logic levels. In this case, the clock signal should be applied to the CLK input, whereas the complementary clock input ($\overline{CLK}$) should be bypassed to ground by a low-inductance ceramic chip capacitor, as shown in Figure 11. Depending on the quality of the signal, inserting a series, damping resistor can be beneficial to reduce ringing. When digitizing at high sampling rates the clock should have a 50% duty cycle ($t_H = t_L$) to maintain good distortion performance.

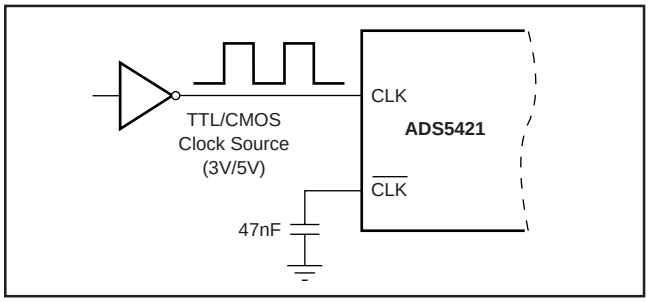


FIGURE 11. Single-Ended TTL/CMOS Clock Source.

Applying a single-ended clock signal will provide satisfactory results in many applications. However, unbalanced high-speed logic signals can introduce a high amount of disturbances, such as ringing or ground bouncing. In addition, a high amplitude can cause the clock signal to have unsymmetrical rise-and-fall times, potentially affecting the converter distortion performance. Proper termination practice and a clean PC board layout will help to keep those effects to a minimum.

To take full advantage of the excellent distortion performance of the ADS5421, it is recommended to drive the clock inputs differentially. A differential clock improves the digital feedthrough immunity and minimizes the effect of modulation between the signal and the clock. Figure 12 illustrates a simple method of converting a square wave clock from single-ended to differential using an RF transformer. Small surface-mount transformers are readily available from several manufacturers (e.g., model ADT1-1 by Mini-Circuits). A capacitor in series with the primary side may be inserted to block any DC voltage present in the signal. The secondary side connects directly to the two clock inputs of the converter because the clock inputs are self-biased.

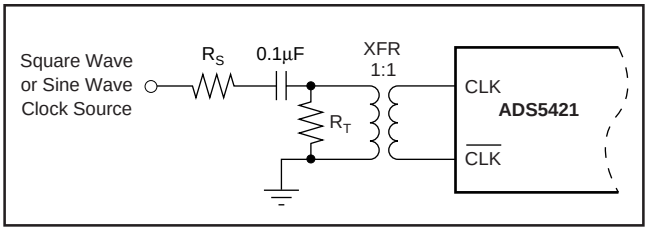


FIGURE 12. Connecting a Ground-Referenced Clock Source to the ADS5421 Using an RF Transformer.

The clock inputs of the ADS5421 can be connected in a number of ways. However, the best performance is obtained when the clock input pins are driven differentially. Operating in this mode, the clock inputs accommodate signal swings ranging from $2.5V_{PP}$ down to $0.5V_{PP}$ differentially. This allows direct interfacing of clock sources such as voltage-controlled crystal oscillators (VCXO) to the ADS5421. The advantage here is the elimination of external logic, usually necessary to convert the clock signal into a suitable logic (TTL or CMOS) signal that otherwise would create an additional source of jitter. In any case, a very low-jitter clock is fundamental to preserving the excellent AC performance of the ADS5421. The converter itself is specified for a low jitter, characterizing the outstanding capability of the internal clock and track-and-hold circuitry. Generally, as the input frequency increases, the clock jitter becomes more dominant for maintaining a good signal-to-noise ratio. This is particularly critical in IF sampling applications where the sampling frequency is lower than input frequency (undersampling). The following equation can be used to calculate the achievable SNR for a given input frequency and clock jitter (t_{JA} in ps rms):

$$SNR = 20 \log_{10} \frac{1}{\left(2\pi f_{IN} t_{JA}\right)} \quad (2)$$

Depending on the nature of the clock source output impedance, impedance matching might become necessary. For this, a termination resistor, R_T, can be installed (see Figure 12). To calculate the correct value for this resistor, consider the impedance ratio of the selected transformer and the differential clock input impedance of the ADS5421, which is approximately 5.5kΩ.

Shown in Figure 13 is one preferred method for clocking the ADS5421. Here, the single-ended clock source can be either a square wave or a sine wave. Using the high-speed differential translator SN65LVDS100 from Texas Instruments, a low-jitter clock can be generated to drive the clock inputs of the ADS5421 differentially.

MINIMUM SAMPLING RATE

The pipeline architecture of the ADS5421 uses a switched-capacitor technique in its internal track-and-hold stages. With each clock cycle, charges representing the captured signal level are moved within the ADC pipeline core. The high sampling speed necessitates the use of very small capacitor values. In order to hold the droop errors low, the capacitors require a minimum refresh rate. To maintain accuracy of the acquired sample charge, the sampling clock on the ADS5421 must not drop below the specified minimum of 1MHz.

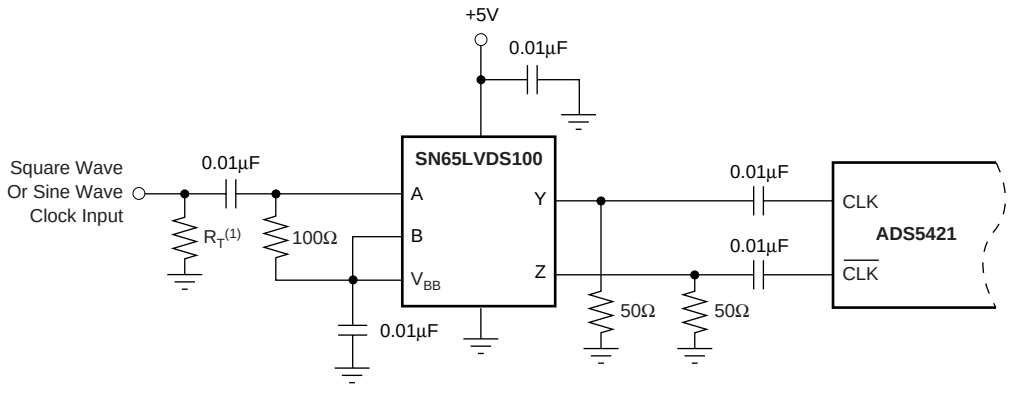
DATA OUTPUT FORMAT (BTC)

The ADS5421 makes two data output formats available, either the Straight Offset Binary (SOB) code or the Binary Two's Complement (BTC) code. The selection of the output coding is controlled through the BTC pin. Applying a logic HIGH will enable the BTC coding, whereas a logic LOW will enable the SOB code. The BTC output format is widely used to interface to microprocessors, for example. The two code structures are identical with the exception that the MSB is inverted for the BTC format, as shown in Table II.

If the input signal exceeds the full-scale range, the data outputs will exhibit the respective full-scale code depending on the selected coding format.

DIFFERENTIAL INPUT	STRAIGHT OFFSET BINARY (SOB)	BINARY TWO'S COMPLEMENT (BTC)
+FS – 1LSB (IN = +3.5V, $\overline{IN}$ = +1.5V)	11 1111 1111 1111	01 1111 1111 1111
+1/2 FS	11 0000 0000 0000	01 0000 0000 0000
Bipolar Zero (IN = $\overline{IN}$ = V_{CM})	10 0000 0000 0000	00 0000 0000 0000
–1/2 FS	01 0000 0000 0000	11 0000 0000 0000
–FS (IN = +1.5V, $\overline{IN}$ = +3.5V)	00 0000 0000 0000	10 0000 0000 0000

TABLE II. Coding Table for Differential Input Configuration and $4V_{PP}$ Full-Scale Input Range.



NOTE: (1) Additional termination resistor RT may be necessary depending on the source requirements

FIGURE 13. Differential Clock Driver Using an LVDS Translator.

OUTPUT ENABLE ($\overline{OE}$)

The digital outputs of the ADS5421 can be set to high impedance (tri-state), exercising the output enable pin ($\overline{OE}$). For normal operation, this pin must be at a logic LOW potential, whereas a logic HIGH voltage disables the outputs. Even though this function affects the output driver stage, the threshold voltages for the $\overline{OE}$ pin do not depend on the output driver supply (VDRV), but are fixed (see the Electrical Characteristics Table and the Digital Inputs Sections). Operating the $\overline{OE}$ function dynamically (e.g., high-speed multiplexing) should be avoided as it will corrupt the conversion process.

POWER-DOWN (PD)

A power-down pin is provided; when taken HIGH, this pin shuts down portions within the ADS5421 and reduces the power dissipation to less than 40mW. The remaining active blocks include the internal reference, ensuring a fast reactivation time. During power-down, data in the converter pipeline will be lost and new valid data will be subject to the specified pipeline delay. If the PD pin is not used, it should be tied to ground or a logic LOW level.

OUTPUT LOADING

It is recommended to keep the capacitive loading on the data output lines as low as possible, preferably below 15pF. Higher capacitive loading will cause larger dynamic currents as the digital outputs are changing. For example, with a typical output slew rate of 0.8V/ns and a total capacitive loading of 10pF (including 4pF output capacitance, 5pF input capacitance of external logic buffer, and 1pF PC board parasitics), a bit transition can cause a dynamic current of (10pF • 0.8V/1ns = 8mA). These high current surges can feed back to the analog portion of the ADS5421 and adversely affect the performance. If necessary, external buffers or latches close to the converter's output pins can be used to minimize the capacitive loading. They also provide the added benefit of isolating the ADS5421 from any digital activities on the bus coupling back high-frequency noise.

POWER SUPPLIES

When defining the power supplies for the ADS5421, it is highly recommended to consider linear supplies instead of switching types. Even with good filtering, switching supplies can radiate noise that could interfere with any high-frequency input signal and cause unwanted modulation products. At its full conversion rate of 40MHz, the ADS5421 typically requires 170mA of supply current on the +5V supplies. Note that this supply voltage should stay within a 5% tolerance.

POWER DISSIPATION

A majority of the ADS5421 total power consumption is used for biasing, therefore; it is independent of the applied clock frequency. Figure 14 shows the typical variation in power consumption versus the clock speed. The current on the VDRV supply is directly related to the capacitive loading of the data output pins and care must be taken to minimize such loading.

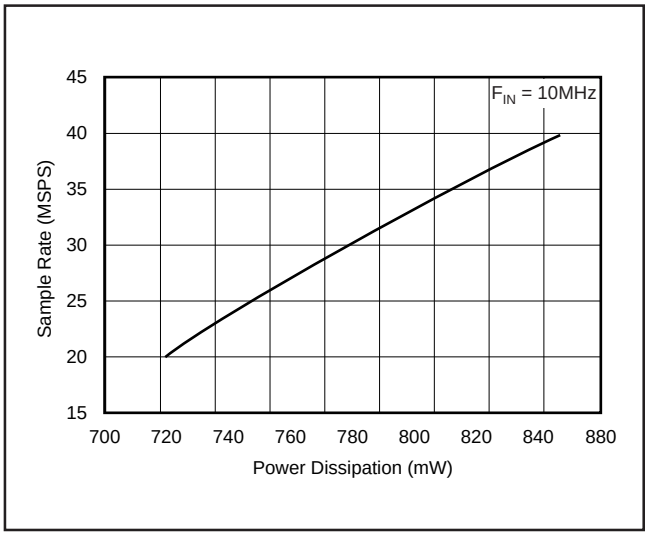


FIGURE 14. Power Dissipation vs Clock Frequency.

DIGITAL OUTPUT DRIVER SUPPLY (VDRV)

A dedicated supply pin, VDRV, provides power to the logic output drivers of the ADS5421 and can be operated with a supply voltage in the range of +3.0V to +5.0V. This can simplify interfacing to various logic families, in particular low-voltage CMOS. It is recommended to operate the ADS5421 with a +3.3V supply voltage on VDRV. This will lower the power dissipation in the output stages due to the lower output swing and reduce current glitches on the supply line that may affect the AC performance of the converter. The analog supply ($+V_{SA}$) and digital supply ($+V_{SD}$) may be tied together, with a ferrite bead or inductor between the supply pins. Each of the these supply pins must be bypassed separately with at least one 0.1µF ceramic chip capacitor, forming a pi-filter (see Figure 15). The recommended operation for the ADS5421 is +5V for the $+V_S$ pins and +3.3V on the output driver pin (VDRV).

The configuration of the supplies requires that a specific power-up sequence be followed for the ADS5421. Analog voltage must be applied to the analog supply pin ($+V_{SA}$) before applying a voltage to the driver supply (VDRV) or before bringing both the digital supply ($+V_{SD}$) and VDRV up simultaneously. Powering up $+V_{SD}$ and VDRV prior to $+V_{SA}$ will cause a large current on $+V_{SA}$ and result in the ADS5421 not functioning properly.

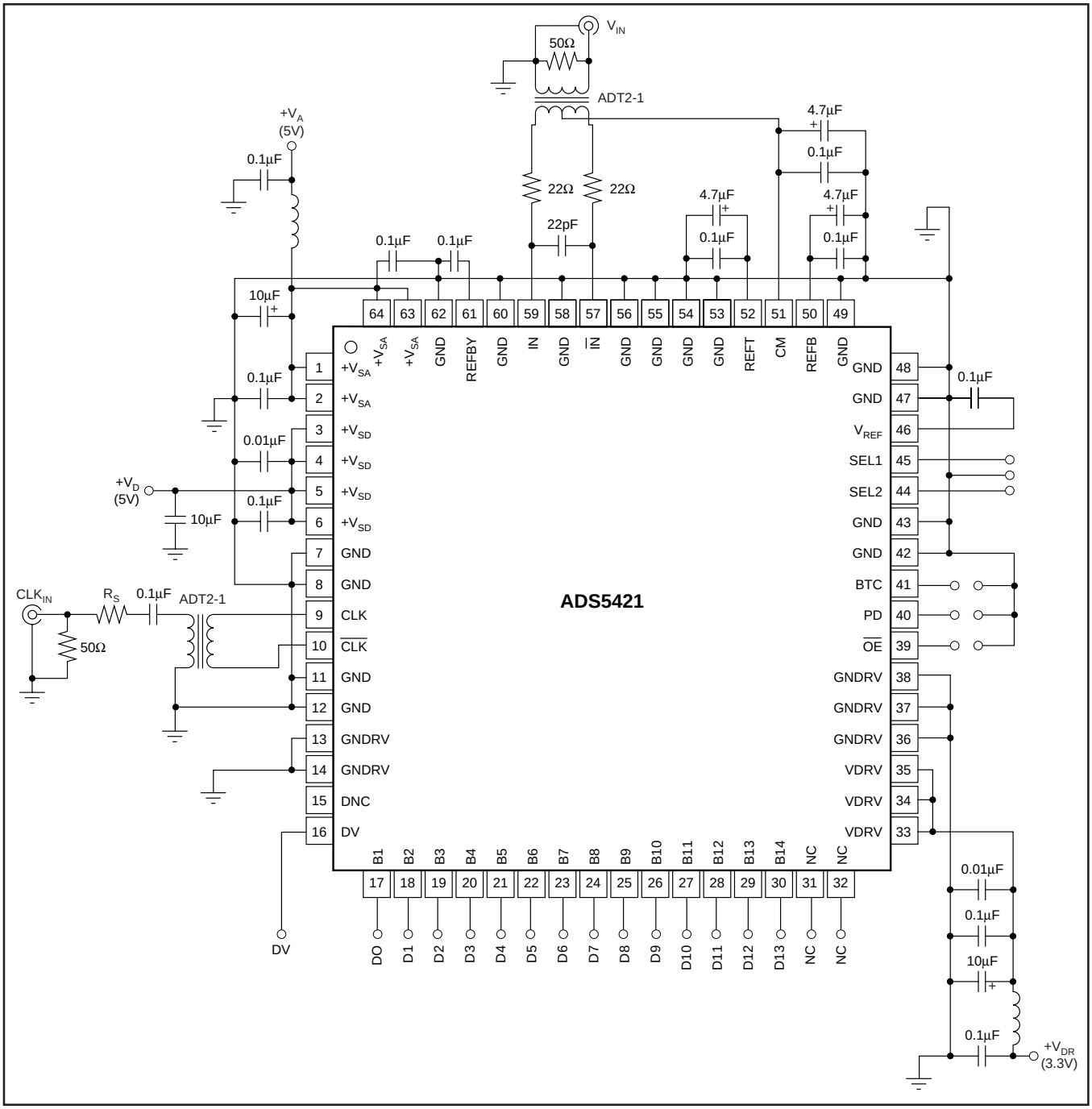


FIGURE 15. Basic Application Circuit of the ADS5421 Includes Recommended Supply and Reference Bypassing.

LAYOUT AND DECOUPLING CONSIDERATIONS

Proper grounding and bypassing, short lead length, and the use of ground planes are particularly important for high-frequency designs. Achieving optimum performance with a fast sampling converter like the ADS5421 requires careful attention to the PC board layout to minimize the effect of board parasitics and optimize component placement. A multilayer board usually ensures best results and allows convenient component placement.

The ADS5421 must be treated as an analog component and the $+V_{SA}$ pins connected to a clean analog supply. This ensures the most consistent results, because digital supplies often carry a high level of switching noise that could couple into the converter and degrade the performance. As mentioned previously, the driver supply pins (VDRV) must also be connected to a low-noise supply. Supplies of adjacent digital circuits can carry substantial current transients. The supply voltage must be thoroughly filtered before connecting to the VDRV supply of the converter. All ground connections on the ADS5421 are internally bonded to the metal flag (bottom of package) that forms a large ground plane. All ground pins must directly connect to an analog ground plane that covers the PC board area under the converter.

Due to its high sampling frequency, the ADS5421 generates high-frequency current transients and noise (clock feedthrough) that are fed back into the supply and reference lines. If not sufficiently bypassed, this adds noise to the conversion process. See Figure 15 for the recommended supply decoupling scheme for the ADS5421. All $+V_S$ pins should be bypassed with a combination of 10nF, 0.1µF ceramic chip capacitors (0805, low ESR) and a 10µF tantalum tank capacitor. A similar approach may be used on the driver supply pins, VDRV. In order to minimize the lead and trace inductance, the capacitors must be located as close to the supply pins as possible. They are best placed directly under the package where double-sided component mounting is allowed. In addition, larger bipolar decoupling capacitors (2.2µF to 10µF), effective at lower frequencies, must also be used on the main supply pins. They can be placed on the PC board in proximity (< 0.5") of the ADC.

If the analog inputs to the ADS5421 are driven differentially, it is especially important to optimize towards a highly symmetrical layout. Small trace length differences can create phase shifts compromising a good distortion performance. For this reason, the use of two single op amps rather than one dual amplifier enables a more symmetrical layout and a better match of parasitic capacitances. The pin orientation of the ADS5421 package follows a flow-through design with the analog inputs located on one side of the package whereas the digital outputs are located on the opposite side of the quad-flat package. This provides a good physical isolation between the analog and digital connections. While designing the layout, it is important to keep the analog signal traces separated from any digital lines to prevent noise coupling onto the analog portion.

Try to match trace length for the differential clock signal (if used) to avoid mismatches in propagation delays. Single-ended clock lines must be short and should not cross any other signal traces.

Short circuit traces on the digital outputs will minimize capacitive loading. Trace length must be kept short to the receiving gate (< 2") with only one CMOS gate connected to one digital output. If possible, the digital data outputs must be buffered (with the TI SN74AVC16244, for example). Dynamic performance can also be improved with the insertion of series resistors at each data output line. This sets a defined time constant and reduces the slew rate that would otherwise flow due to the fast edge rate. The resistor value may be chosen to result in a time constant of 15% to 25% of the used data rate.

Revision History

DATE	REVISION	PAGE	SECTION	DESCRIPTION
6/21/05	E	—	—	Changed all Vp-p to subscript (V_{PP}).
		1	Features	Changed PREMIUM to ON-BOARD. Deleted LOW POWER: 850mW.
			Front Page Diagram	Changed 1Vp-p to $2V_{PP}$.
		2	Electrical Characteristics	Changed Optional Input Ranges to Optional Input Range and deleted 2Vp-p, same line under TYP.
		3	Electrical Characteristics	Changed External REF Voltage Range from 9.9V to 1.4V (minimum). Added ($V_{REFT} - V_{REFB}$) to ACCURACY section under CONDITIONS column.
		5	Reference and Full-Scale Range Select Table	Deleted 2Vp-p row.
		9	Input Full-Scale Range Versus Performance	Deleted last sentence.
		11	Transformer-Coupled, Single-Ended-to-Differential Configuration	Deleted part of the last sentence in the first paragraph.
		12	AC-Coupled, Differential Interface with Gain	Text change in last paragraph.
			Figure 7	Deleted 2Vp-p curve.
		13	Reference Operation	Deleted +1V and the word *complete* in first paragraph.
			Using External References	Inserted text.
			Table I	Deleted 2Vp-p row. Changed voltages at REFT and REFB columns in External Reference row.
		16	Data Output Format (BTC)	Changed and deleted text in second paragraph.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS5421Y/T	Active	Production	LQFP (PM) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS5421Y
ADS5421Y/T.B	Active	Production	LQFP (PM) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS5421Y

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

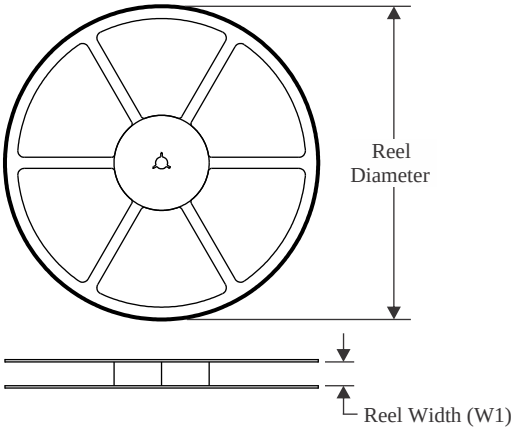
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

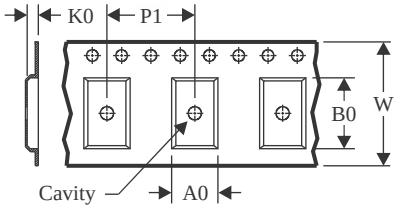
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

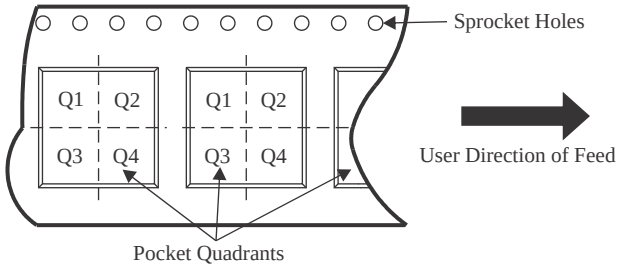


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

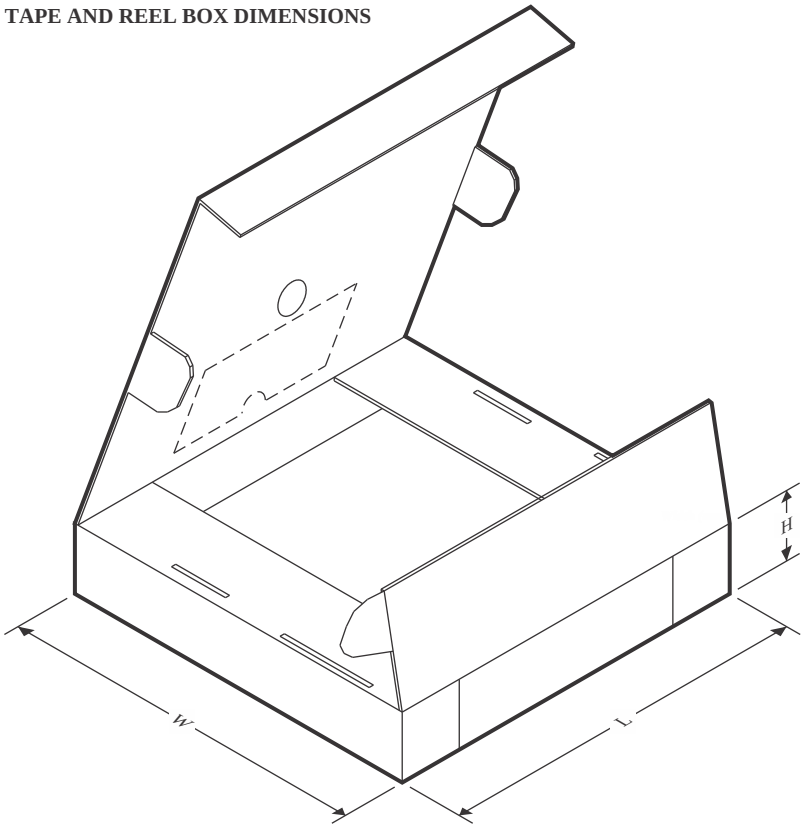
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS5421Y/T	LQFP	PM	64	250	180.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
ADS5421Y/TG4	LQFP	PM	64	250	180.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

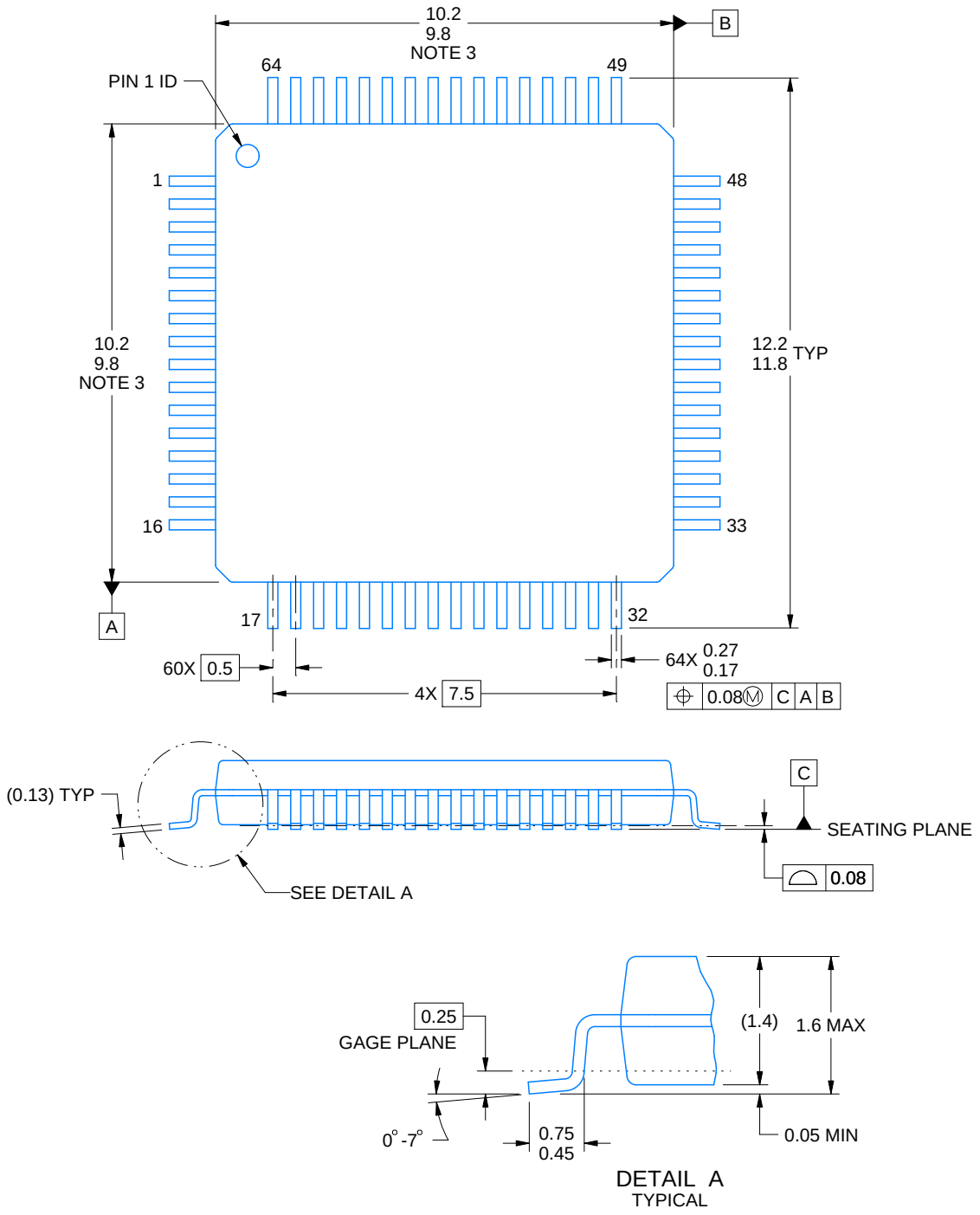
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS5421Y/T	LQFP	PM	64	250	213.0	191.0	55.0
ADS5421Y/TG4	LQFP	PM	64	250	213.0	191.0	55.0

PACKAGE OUTLINE

PM0064A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



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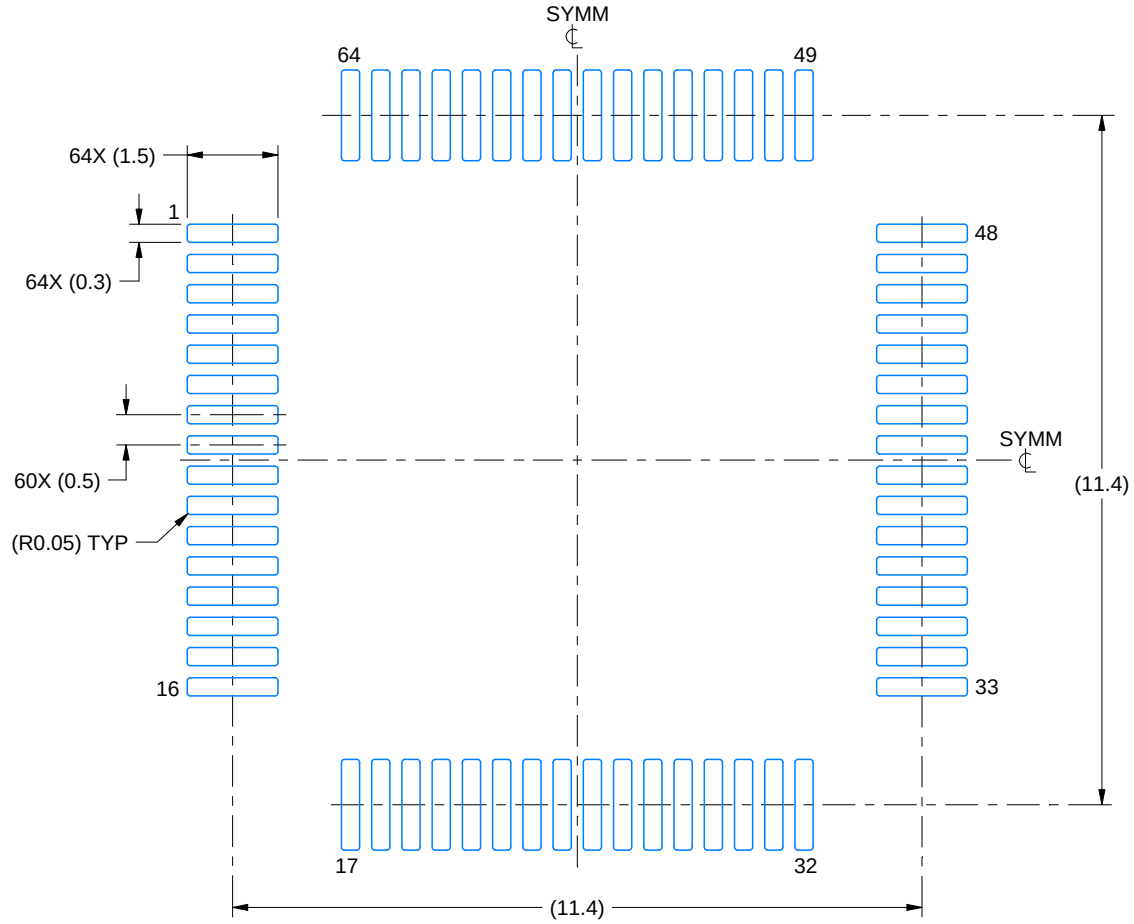
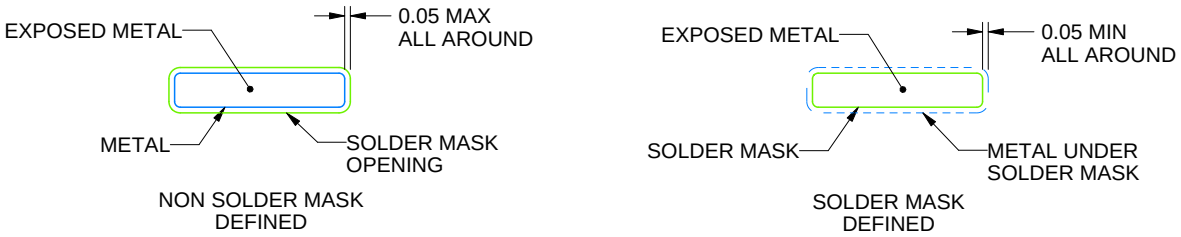
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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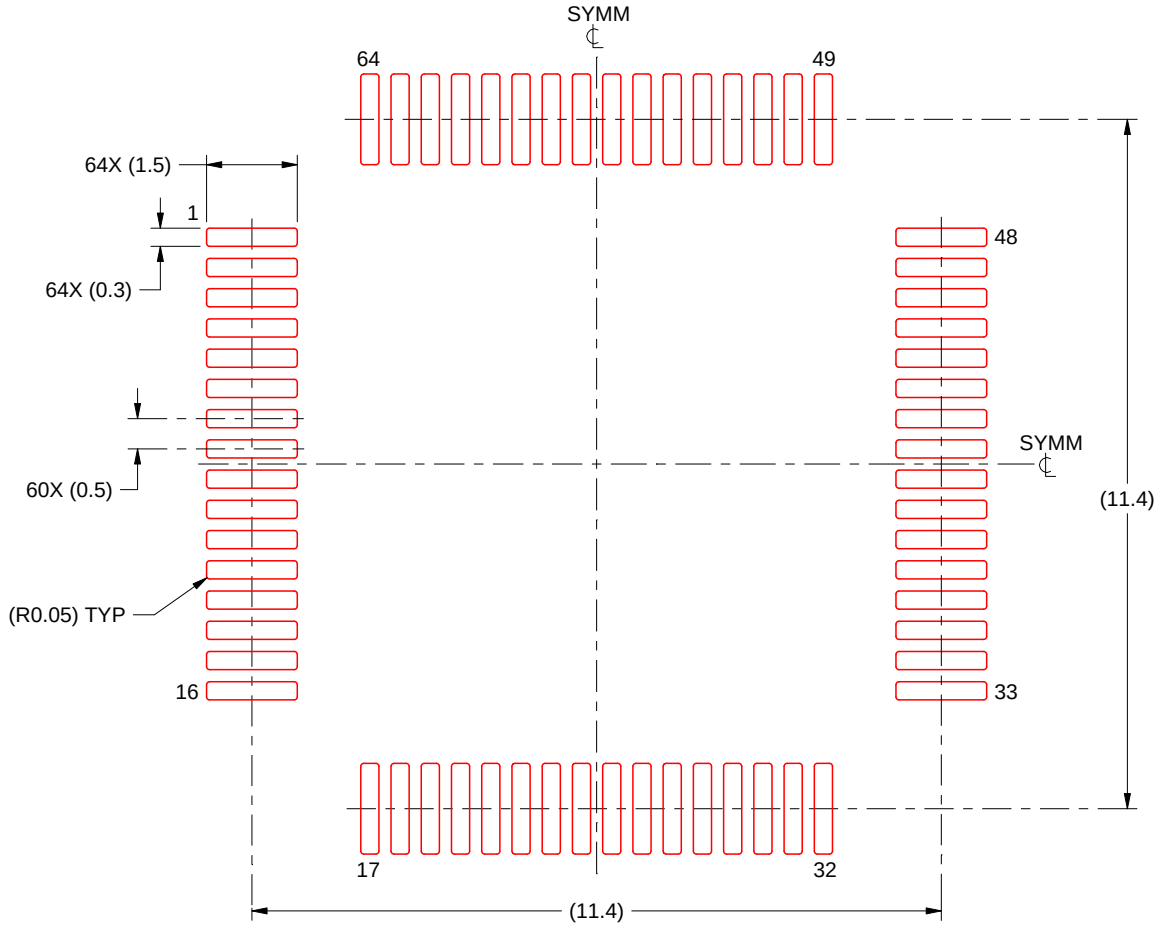
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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