ADSxx50 デュアル、750kSPS、16/14/12ビット、同時サンプリング、アナログ/デジタル・コンバータ

1 特長

- 16、14、12ビットのピン互換ファミリ
- 2つのチャネルを同時にサンプル
- 疑似差動アナログ入力
- 高いスループット: 750kSPS
- 非常に優れたDC性能
  - 直線性
    - ADS8350: 16ビットNMC DNL、±2.5 LSB、最大INL
    - ADS7850: 14ビットNMC DNL、±1.5 LSB、最大INL
    - ADS7250: 12ビットNMC DNL、±1 LSB、最大INL
- 優れたAC特性
  - ADS8350: 85dB SNR、-96dB THD
  - ADS7850: 81dB SNR、-90dB THD
  - ADS7250: 73dB SNR、-88dB THD
- 単純なシリアル・インターフェイス
- 拡張工業用温度範囲にわたって完全に動作を規定: -40℃～+125℃
- 小さな占有面積: WQFN-16 (3mm×3mm)

2 アプリケーション

- モータ制御: SinCosエンコーダを使用する位置測定
- 光学ネットワーク: EDFAゲイン制御ループ
- 保護リレー
- 電力品質測定
- 3相電源の制御
- プログラマブル・ロジック・コントローラ
- 産業用オートメーション

3 概要

ADS8350、ADS7850、ADS7250デバイスは、ピン互換のデュアル、高速、同時サンプリングのアナログ/デジタル・コンバータ(ADC)のファミリで、擬似差動アナログ入力をサポートしています。すべてのデバイスは、広い電源電圧範囲で動作可能な、単純なシリアル・インターフェイスをサポートしているため、多くの種類のホスト・コントローラと簡単に通信できます。

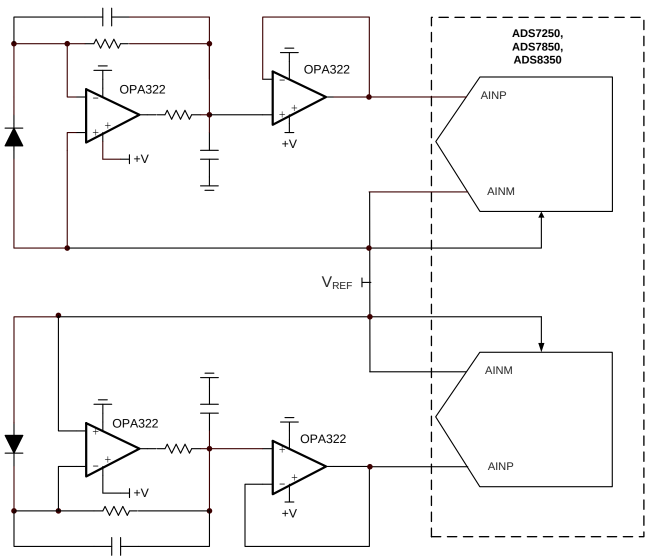
すべてのデバイスは、拡張工業用温度範囲(-40℃～125℃)で完全に動作が規定されており、ピン互換のWQFN-16 (3mm×3mm)パッケージで供給されます。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
ADS7250	WQFN (16)	3.00mm×3.00mm
ADS7850		
ADS8350		

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

機能ブロック図



目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision C (June 2014) から **Revision D** に変更 — **Page**

- Changed *ESD Ratings* title, updated to current format, moved *Storage temperature* parameter to *Absolute Maximum Ratings* table ... 4
- Changed *Timing Characteristics* table: split table into *Timing Requirements* and *Switching Characteristics* ... 9
- Deleted t_{SU_DOCK} and t_{HT_CKDO} parameters, replaced with t_{D_CKDO} parameter ... 9
- Changed *Timing Diagram* figure ... 9

Revision B (April 2014) から **Revision C** に変更 — **Page**

- デバイス情報表を現在の標準に合わせて変更 ... 1
- 機能ブロック図の擬似差動入力と基準接続を訂正 ... 1
- Changed Handling Ratings table to current standards ... 4

Revision A (January 2014) から **Revision B** に変更 — **Page**

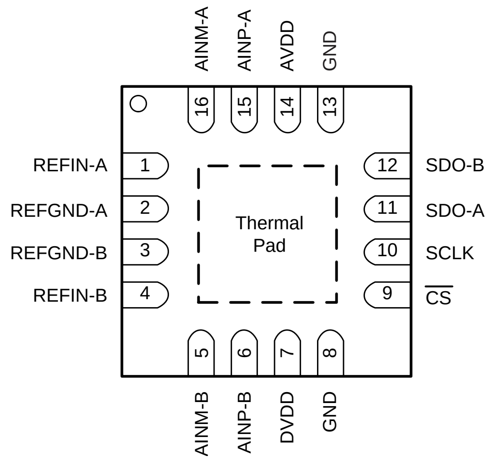
- 最新のデータシート標準に合わせてフォーマットを変更、「レイアウト」セクションを追加、既存のセクションを移動 ... 1
- Deleted Ordering Information section ... 3

2013年5月発行のものから更新 — **Page**

- 量産用にリリース ... 1

5 Pin Configuration and Functions

RTE Package
16-Pin WQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AINM-A	16	Analog input	Negative analog input, ADC_A
AINM-B	5	Analog input	Negative analog input, ADC_B
AINP-A	15	Analog input	Positive analog input, ADC_A
AINP-B	6	Analog input	Positive analog input, ADC_B
AVDD	14	Supply	ADC supply voltage
$\overline{\text{CS}}$	9	Digital input	Chip-select signal; active low
DVDD	7	Supply	Digital I/O supply
GND	8, 13	Supply	Device ground
REFGND-A	2	Supply	Reference ground potential, ADC_A
REFGND-B	3	Supply	Reference ground potential, ADC_B
REFIN-A	1	Analog input	Reference voltage input, ADC_A
REFIN-B	4	Analog input	Reference voltage input, ADC_B
SCLK	10	Digital input	Serial communication clock
SDO-A	11	Digital output	Data output for serial communication, ADC_A
SDO-B	12	Digital output	Data output for serial communication, ADC_B
Thermal pad		Supply	Exposed thermal pad. TI recommends connecting the thermal pad to the printed circuit board (PCB) ground.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	AVDD to GND	–0.3	7	V
	DVDD to GND	–0.3	7	
Analog input voltage	AINP_x to REFGND_x	REFGND_x – 0.3	AVDD + 0.3	V
	AINM_x to REFGND_x	REFGND_x – 0.3	AVDD + 0.3	
	REFIN_x to REFGND_x	REFGND_x – 0.3	AVDD + 0.3	
Digital input voltage	$\overline{CS}$, SCLK to GND	GND – 0.3	DVDD + 0.3	V
Ground voltage difference	| REFGND_x – GND |		0.3	V
Input current	Any pin except supply pins		±10	mA
Maximum virtual junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
AVDD	Analog power supply		5		V
DVDD	Digital power supply		3.3		V

6.4 Thermal Information

THERMAL METRIC		ADS7250, ADS7850, ADS8350 RTE (WQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33.3	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	29.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.4	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	0.9	°C/W

6.5 Electrical Characteristics: All Devices

minimum and maximum specifications are at T_A = –40°C to 125°C, AVDD = 5 V, V_{REFIN_A} = V_{REFIN_B} = V_{REF}, and t_{DATA} = 750 kSPS (unless otherwise noted); typical values are at T_A = 25°C, AVDD = 5 V, and DVDD = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
FSR	Full-scale input range, (AINP_x – AINM_x)	AVDD ≥ 2 x V_{REF} [1], AINM_x = V_{REF}	$–V_{REF}$		V_{REF}	V
V_{INP}	Absolute input voltage, (AINP_x to REFGND)	AVDD ≥ 2 x V_{REF} [1], AINM_x = V_{REF}	0		2 × V_{REF}	V
V_{INM}	Absolute input voltage, (AINM_x to REFGND)		V_{REF} – 0.1	V_{REF}	V_{REF} + 0.1	V
C_{IN}	Input capacitance	In sample mode		40		pF
		In hold mode		4		
I_{IN}	Input leakage current			1.5		nA
SAMPLING DYNAMICS						
f_{DATA}	Data rate				750	kSPS
t_A	Aperture delay			8		ns
	t_A match	ADC_A to ADC_B		40		ps
	Aperture jitter			10		ps
f_{CLK}	Clock frequency				24	MHz
VOLTAGE REFERENCE INPUT						
V_{REF}	Reference input voltage		2.25	2.5	AVDD / 2 [1]	V
I_{REF}	Reference input current			300		µA
	Reference leakage current				1	µA
C_{REF}	External ceramic reference capacitance			10		µF
DIGITAL INPUTS [2]						
V_{IH}	Input voltage, high		0.7 DVDD		DVDD + 0.3	V
V_{IL}	Input voltage, low		–0.3		0.3 DVDD	V
DIGITAL OUTPUTS [2]						
V_{OH}	Output voltage, high	I_{OH} = 500-µA source	0.8 DVDD		DVDD	V
V_{OL}	Output voltage, low	I_{OH} = 500-µA sink	0		0.2 DVDD	V
POWER SUPPLY						
AVDD	Analog supply voltage, AVDD to GND		4.5 [1]	5.0	5.5	V
DVDD	Digital supply voltage, DVDD to GND		1.65		5.5	V
$I_{A\text{-}DYNA}$	Analog supply current, during conversion	AVDD = 5 V, throughput = max		8	9	mA
$I_{A\text{-}STAT}$	Analog supply current, no conversion	AVDD = 5 V, static		5	7	mA
I_{DVDD}	Digital supply current	DVDD = 3.3 V		0.25		mA
$P_{D\text{-}DYNA}$	Power dissipation	AVDD = 5 V, throughput = max		40	45	mW
$P_{D\text{-}STAT}$		AVDD = 5 V, static		25	35	

(1) The AVDD supply voltage defines the permissible voltage swing on the analog input pins. To use the maximum dynamic range of the analog input pins, V_{REFIN_x} and AVDD must be in the respective permissible range with AVDD ≥ 2 x V_{REFIN_x}.
(2) Specified by design; not production tested.

6.6 Electrical Characteristics: ADS7250

minimum and maximum specifications are at T_A = –40°C to 125°C, AVDD = 5 V, V_{REFIN_A} = V_{REFIN_B} = V_{REF}, and t_{DATA} = 750 kSPS (unless otherwise noted); typical values are at T_A = 25°C, AVDD = 5 V, and DVDD = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RESOLUTION						
	Resolution		12			Bits
DC ACCURACY						
INL	Integral nonlinearity		–1	±0.5	1	LSB
DNL	Differential nonlinearity		–0.99	±0.4	1	LSB
V_{OS}	Input offset error		–2	±0.75	2	mV
	V_{OS} match	ADC_A to ADC_B	–2	±0.75	2	mV
dV_{OS}/dT	Input offset thermal drift			1		µV/°C
G_{ERR}	Gain error	Referenced to voltage at REFIN_x	–0.1%	±0.05%	0.1%	
	G_{ERR} match	ADC_A to ADC_B	–0.1%	±0.05%	0.1%	
G_{ERR}/dT	Gain error thermal drift	Referenced to voltage at REFIN_x		1		ppm/°C
CMRR	Common-mode rejection ratio	Both ADCs, dc to 20 kHz		74		dB
AC ACCURACY						
SINAD	Signal-to-noise + distortion	–0.5 dBFS at 20-kHz input	71.5	72.9		dB
		–0.5 dBFS at 100-kHz input		72.9		
		–0.5 dBFS at 250-kHz input		72.5		
SNR	Signal-to-noise ratio	–0.5 dBFS at 20-kHz input	72	73		dB
		–0.5 dBFS at 100-kHz input		73		
		–0.5 dBFS at 250-kHz input		73		
THD	Total harmonic distortion	–0.5 dBFS at 20-kHz input		–90		dB
		–0.5 dBFS at 100-kHz input		–90		
		–0.5 dBFS at 250-kHz input		–82		
SFDR	Spurious-free dynamic range	–0.5 dBFS at 20-kHz input		90		dB
		–0.5 dBFS at 100-kHz input		90		
		–0.5 dBFS at 250-kHz input		82		
	Isolation between ADC_A and ADC_B	f_{IN} = 15 kHz, f_{NOISE} = 25 kHz		–85		dB
$BW_{(FP)}$	Full-power bandwidth	At –3 dB		25		MHz
		At –0.1 dB		5		

6.7 Electrical Characteristics: ADS7850

minimum and maximum specifications are at T_A = –40°C to 125°C, AVDD = 5 V, V_{REFIN_A} = V_{REFIN_B} = V_{REF}, and t_{DATA} = 750 kSPS (unless otherwise noted); typical values are at T_A = 25°C, AVDD = 5 V, and DVDD = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RESOLUTION						
	Resolution		14			Bits
DC ACCURACY						
INL	Integral nonlinearity		–1.5	±0.8	1.5	LSB
DNL	Differential nonlinearity		–0.99	±0.7	1	LSB
V_{OS}	Input offset error		–1	±0.25	1	mV
	V_{OS} match	ADC_A to ADC_B	–1	±0.25	1	mV
dV_{OS}/dT	Input offset thermal drift			1		µV/°C
G_{ERR}	Gain error	Referenced to voltage at REFIN_x	–0.1%	±0.05%	0.1%	
	G_{ERR} match	ADC_A to ADC_B	–0.1%	±0.05%	0.1%	
G_{ERR}/dT	Gain error thermal drift	Referenced to voltage at REFIN_x		1		ppm/°C
CMRR	Common-mode rejection ratio	Both ADCs, dc to 20 kHz		74		dB
AC ACCURACY						
SINAD	Signal-to-noise + distortion	–0.5 dBFS at 20-kHz input	79	81		dB
		–0.5 dBFS at 100-kHz input		81		
		–0.5 dBFS at 250-kHz input		79.9		
SNR	Signal-to-noise ratio	–0.5 dBFS at 20-kHz input	79.5	81.5		dB
		–0.5 dBFS at 100-kHz input		81.5		
		–0.5 dBFS at 250-kHz input		81		
THD	Total harmonic distortion	–0.5 dBFS at 20-kHz input		–90		dB
		–0.5 dBFS at 100-kHz input		–90		
		–0.5 dBFS at 250-kHz input		–86		
SFDR	Spurious-free dynamic range	–0.5 dBFS at 20-kHz input		90		dB
		–0.5 dBFS at 100-kHz input		90		
		–0.5 dBFS at 250-kHz input		86		
	Isolation between ADC_A and ADC_B	f_{IN} = 15 kHz, f_{NOISE} = 25 kHz		–90		dB
$BW_{(FP)}$	Full-power bandwidth	At –3 dB		25		MHz
		At –0.1 dB		5		

6.8 Electrical Characteristics: ADS8350

minimum and maximum specifications are at T_A = –40°C to 125°C, AVDD = 5 V, V_{REFIN_A} = V_{REFIN_B} = V_{REF}, and t_{DATA} = 750 kSPS (unless otherwise noted); typical values are at T_A = 25°C, AVDD = 5 V, and DVDD = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RESOLUTION						
	Resolution		16			Bits
DC ACCURACY						
INL	Integral nonlinearity		–2.5	±1	2.5	LSB
DNL	Differential nonlinearity		–0.99	±0.7	2	LSB
V_{OS}	Input offset error		–1	±0.25	1	mV
	V_{OS} match	ADC_A to ADC_B	–1	±0.25	1	mV
dV_{OS}/dT	Input offset thermal drift			1		µV/°C
G_{ERR}	Gain error	Referenced to voltage at REFIN_x	–0.1%	±0.05%	0.1%	
	G_{ERR} match	ADC_A to ADC_B	–0.1%	±0.05%	0.1%	
G_{ERR}/dT	Gain error thermal drift	Referenced to voltage at REFIN_x		1		ppm/°C
CMRR	Common-mode rejection ratio	Both ADCs, dc to 20 kHz		74		dB
AC ACCURACY						
SINAD	Signal-to-noise + distortion	–0.5 dBFS at 20-kHz input	83.5	84.7		dB
		–0.5 dBFS at 100-kHz input		83.7		
		–0.5 dBFS at 250-kHz input		83		
SNR	Signal-to-noise ratio	–0.5 dBFS at 20-kHz input	84	85		dB
		–0.5 dBFS at 100-kHz input		84.8		
		–0.5 dBFS at 250-kHz input		84		
THD	Total harmonic distortion	–0.5 dBFS at 20-kHz input		–96		dB
		–0.5 dBFS at 100-kHz input		–90		
		–0.5 dBFS at 250-kHz input		–90		
SFDR	Spurious-free dynamic range	–0.5 dBFS at 20-kHz input		96		dB
		–0.5 dBFS at 100-kHz input		90		
		–0.5 dBFS at 250-kHz input		90		
	Isolation between ADC_A and ADC_B	f_{IN} = 15 kHz, f_{NOISE} = 25 kHz		–90		dB
$BW_{(FP)}$	Full-power bandwidth	At –3 dB		25		MHz
		At –0.1 dB		5		

6.9 Timing Requirements

			MIN	NOM	MAX	UNIT
$f_{THROUGHPUT}$	Sample taken to data read	f_{CLK} = max			750	kSPS
		f_{CLK} = max	1.33			µs
f_{CLK}	CLOCK frequency	$f_{THROUGHPUT}$ = max			24	MHz
t_{CLK}	CLOCK period	$f_{THROUGHPUT}$ = max	41.66			ns
t_{PH_CK}	CLOCK high time		0.4		0.6	t_{CLK}
t_{PL_CK}	CLOCK low time		0.4		0.6	t_{CLK}
t_{ACQ}	Acquisition time	ADS8350, f_{CLK} = max	120			ns
		ADS7850, f_{CLK} = max	100			
		ADS7250, f_{CLK} = max	70			
t_{PH_CS}	$\overline{CS}$ high time		20			ns
$t_{PH\_CS\_SHRT}$	$\overline{CS}$ high time after frame abort	ADS8350	120			ns
		ADS7850	100			
		ADS7250	70			
t_{D_CKCS}	Delay time from last SCLK falling to $\overline{CS}$ rising		15			ns
t_{SU_CSCK}	Setup time from $\overline{CS}$ falling to SCLK falling		15			ns

6.10 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{CONV}	Conversion time				590	ns
t_{DV_CSDO}	Delay time from $\overline{CS}$ falling to data enable				12	ns
t_{DZ_CSDO}	Delay time from $\overline{CS}$ rising to DOUT going to 3-state				10	ns
t_{D_CKDO}	Delay time from SCLK falling to (next) data valid on SDO		3		20	ns

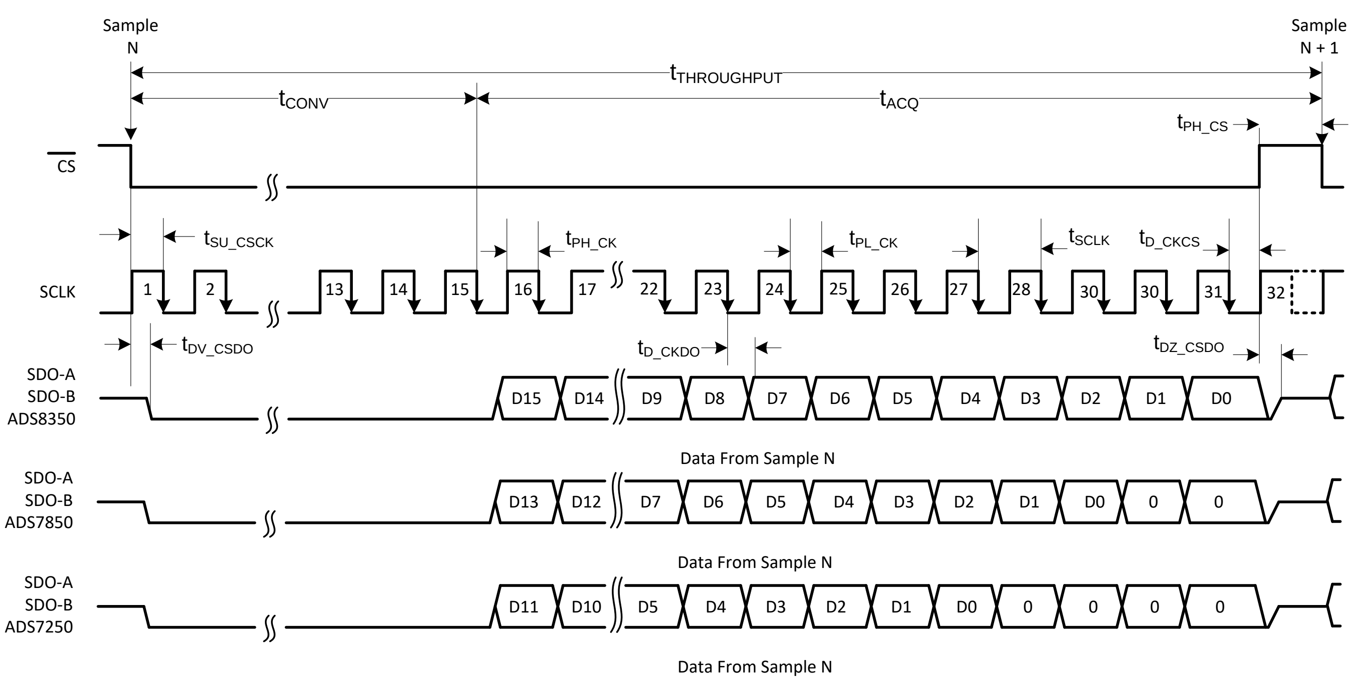


Figure 1. Timing Diagram

6.11 Typical Characteristics: ADS7250

at T_A = 25°C, AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 2.5 V, and f_{DATA} = 750 kSPS (unless otherwise noted)

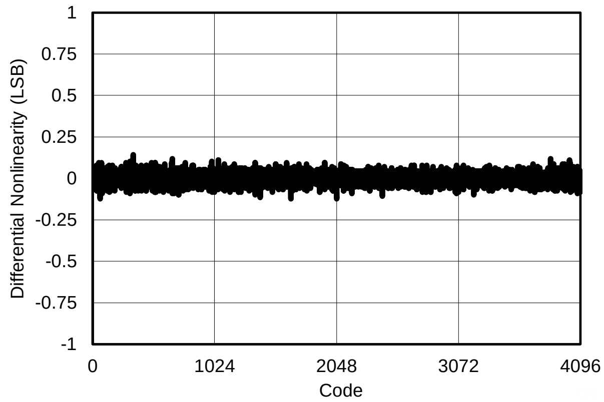


Figure 2. Typical DNL

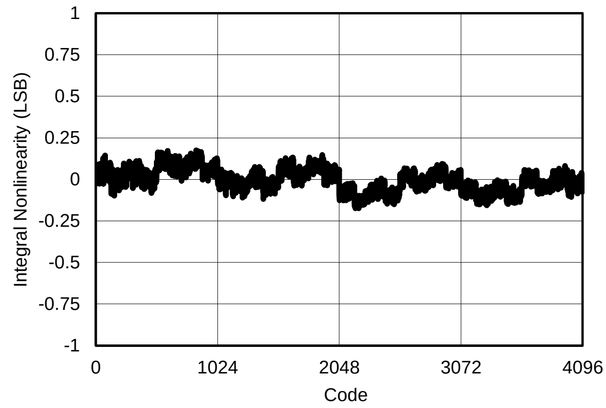


Figure 3. Typical INL

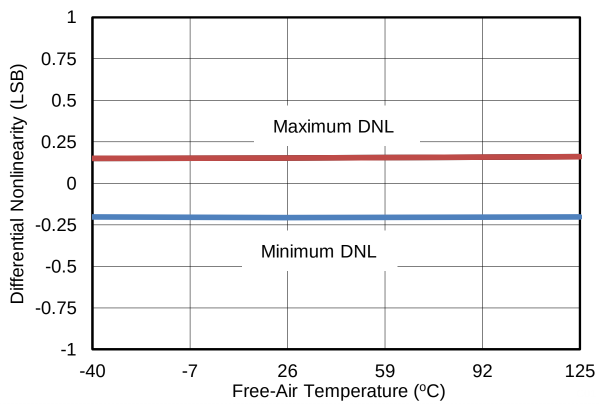


Figure 4. DNL vs Device Temperature

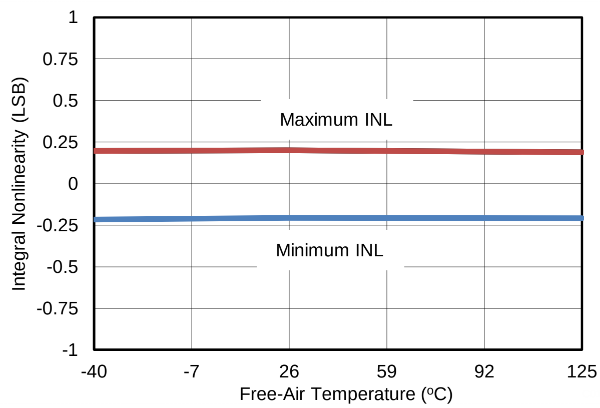


Figure 5. INL vs Device Temperature

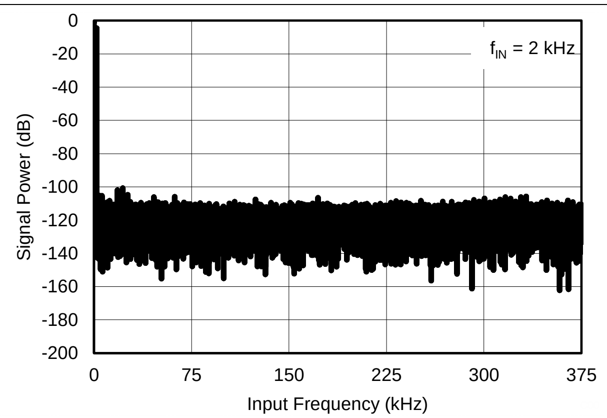


Figure 6. Typical FFT at 2-kHz Input

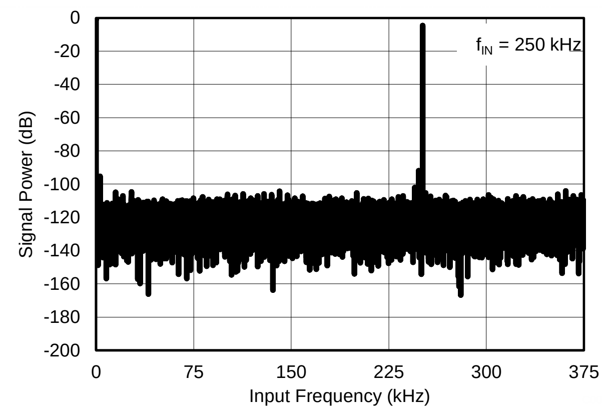


Figure 7. Typical FFT at 250-kHz Input

Typical Characteristics: ADS7250 (continued)

at T_A = 25°C, AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 2.5 V, and f_{DATA} = 750 kSPS (unless otherwise noted)

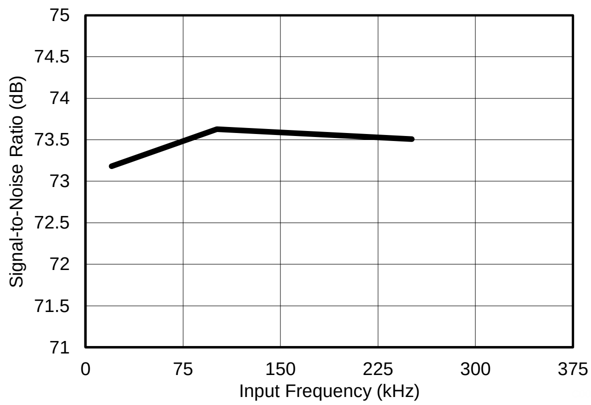


Figure 8. SNR vs Input Frequency

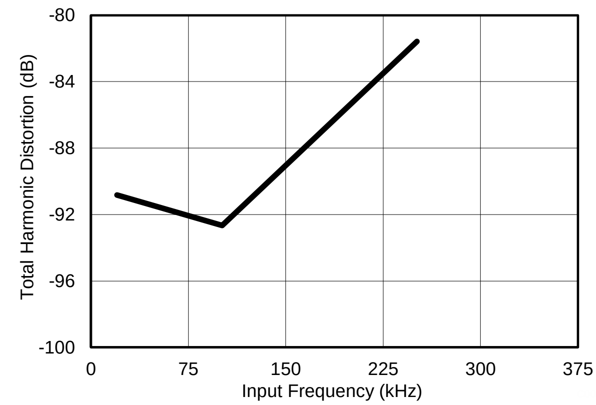


Figure 9. THD vs Input Frequency

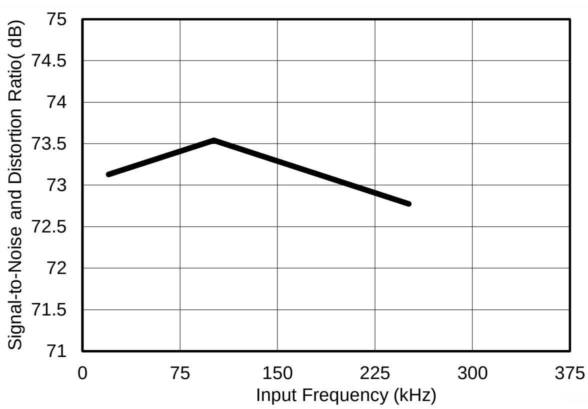


Figure 10. SINAD vs Input Frequency

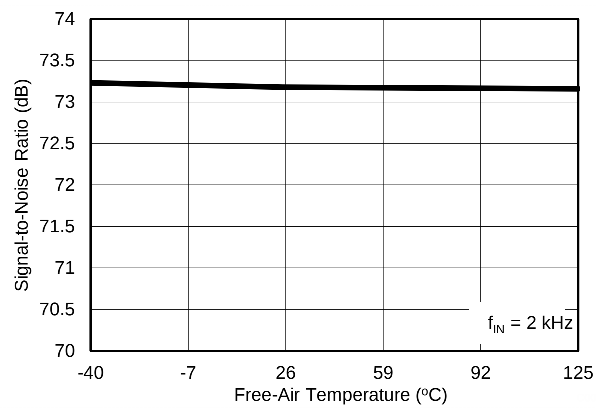


Figure 11. SNR vs Device Temperature

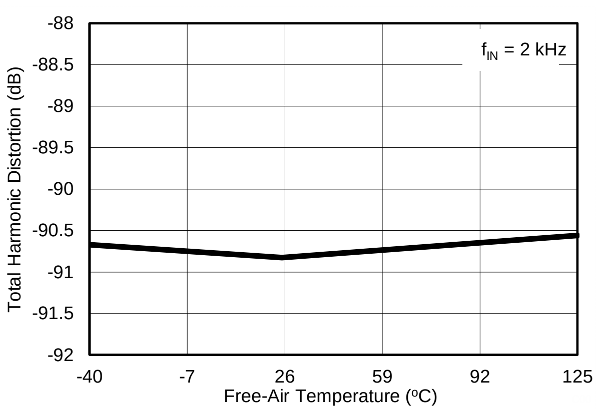


Figure 12. THD vs Device Temperature

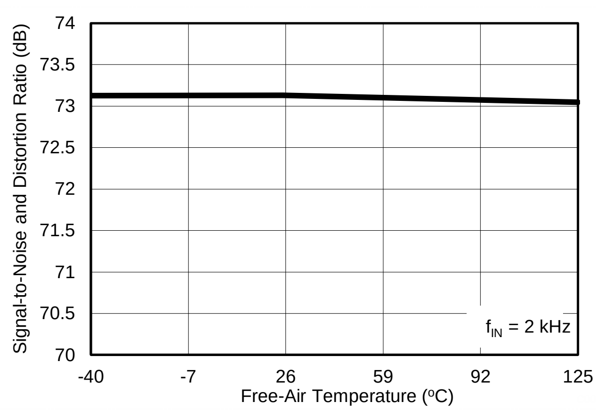


Figure 13. SINAD vs Device Temperature

Typical Characteristics: ADS7250 (continued)

at T_A = 25°C, AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 2.5 V, and f_{DATA} = 750 kSPS (unless otherwise noted)

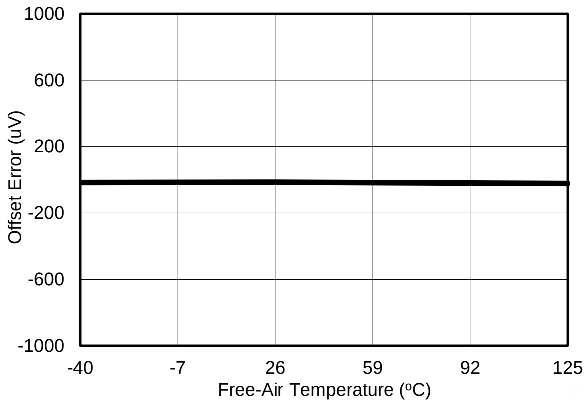


Figure 14. Offset Error vs Device Temperature

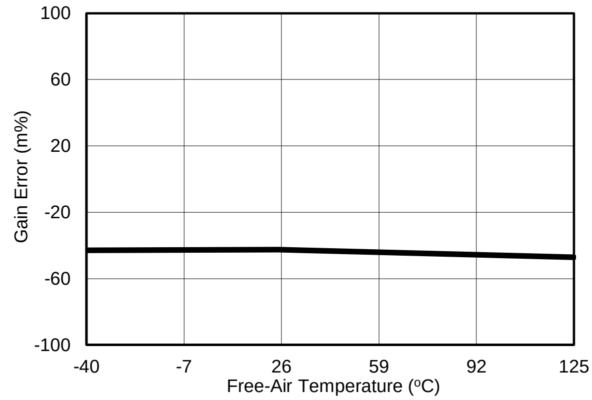


Figure 15. Gain Error vs Device Temperature

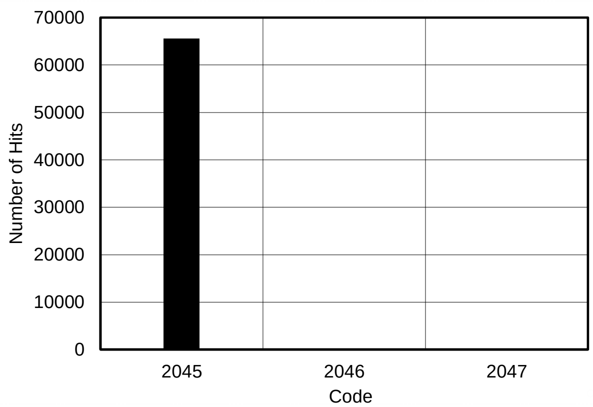


Figure 16. DC Histogram

6.12 Typical Characteristics: ADS7850

at T_A = 25°C, AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 2.5 V, and f_{DATA} = 750 kSPS (unless otherwise noted)

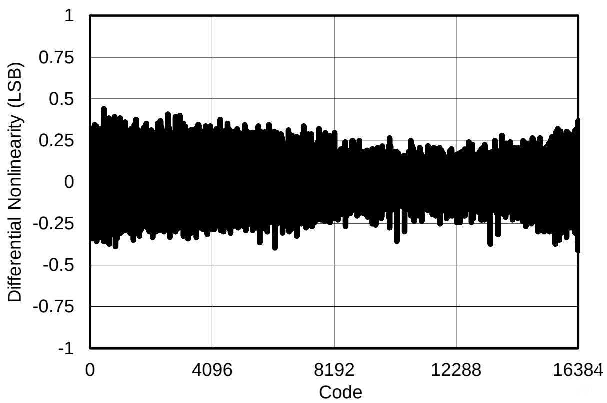


Figure 17. Typical DNL

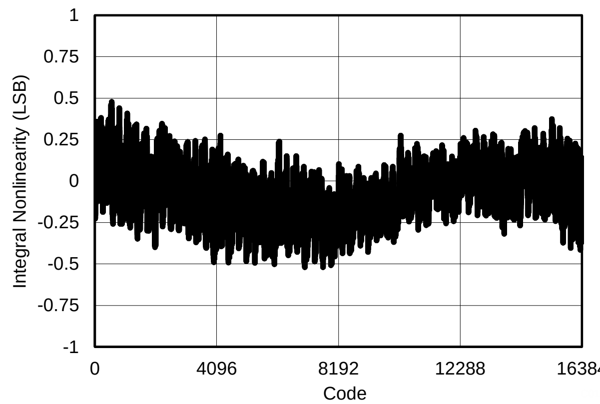


Figure 18. Typical INL

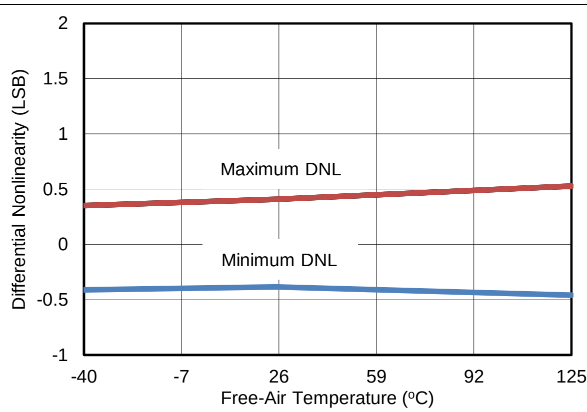


Figure 19. DNL vs Device Temperature

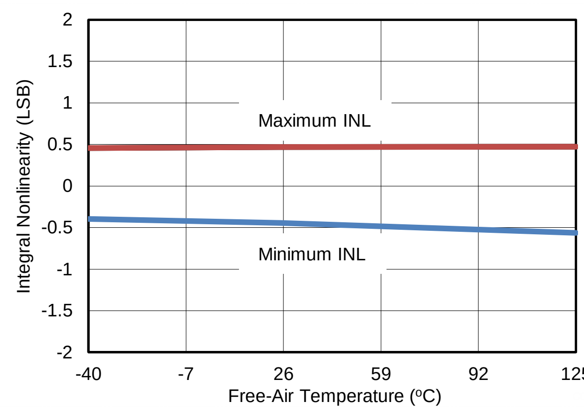


Figure 20. INL vs Device Temperature

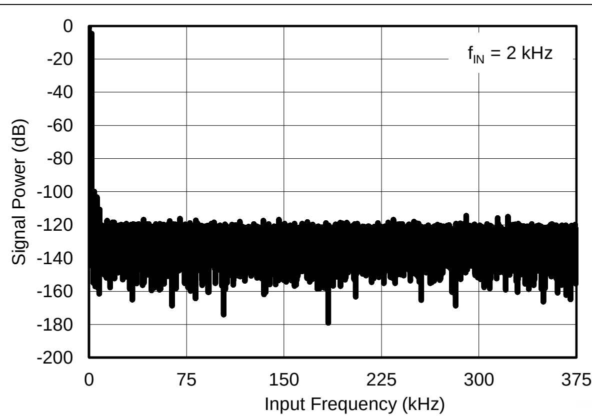


Figure 21. Typical FFT at 2-kHz Input

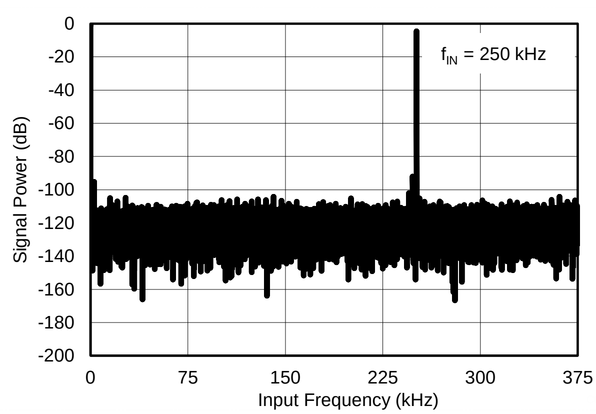


Figure 22. Typical FFT at 250-kHz Input

Typical Characteristics: ADS7850 (continued)

at T_A = 25°C, AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 2.5 V, and f_{DATA} = 750 kSPS (unless otherwise noted)

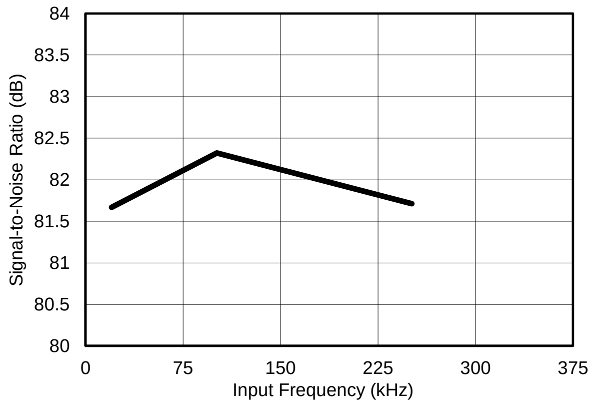


Figure 23. SNR vs Input Frequency

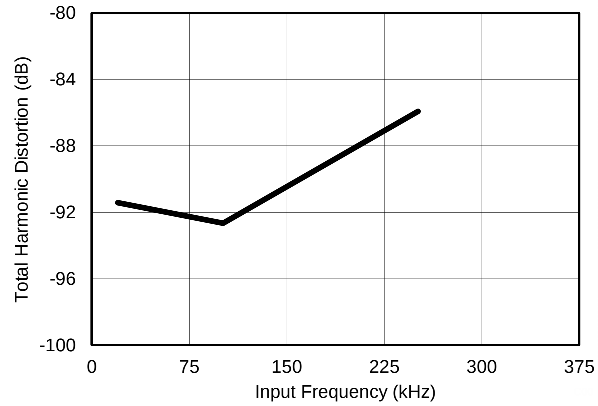


Figure 24. THD vs Input Frequency

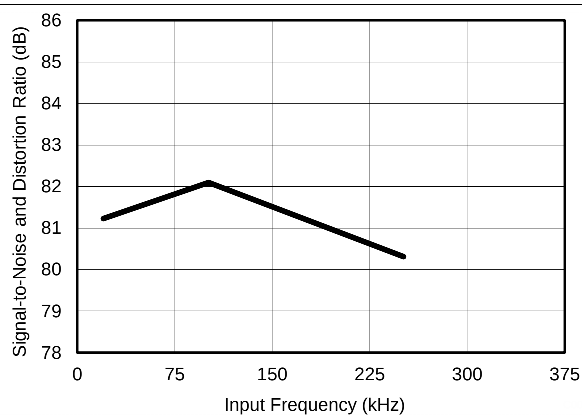


Figure 25. SINAD vs Input Frequency

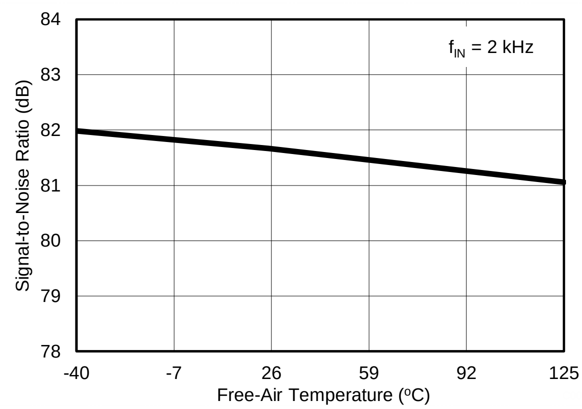


Figure 26. SNR vs Device Temperature

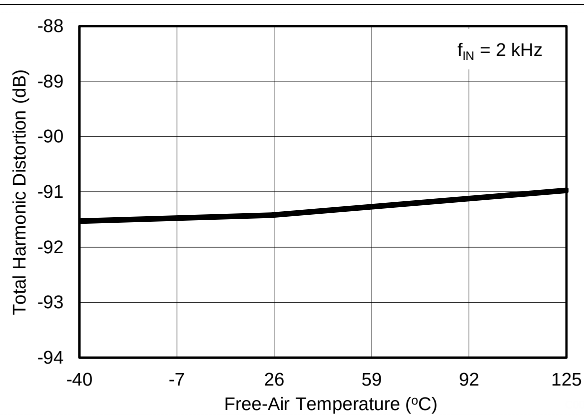


Figure 27. THD vs Device Temperature

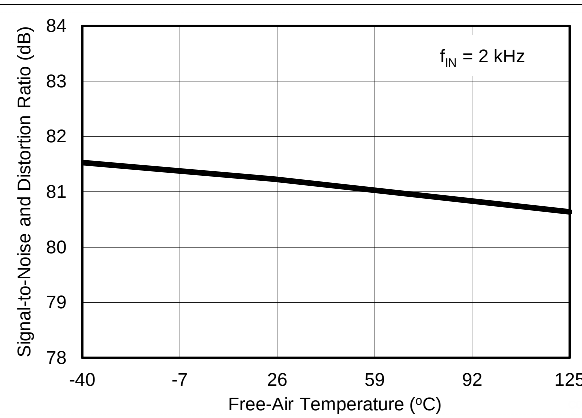


Figure 28. SINAD vs Device Temperature

Typical Characteristics: ADS7850 (continued)

at T_A = 25°C, AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 2.5 V, and f_{DATA} = 750 kSPS (unless otherwise noted)

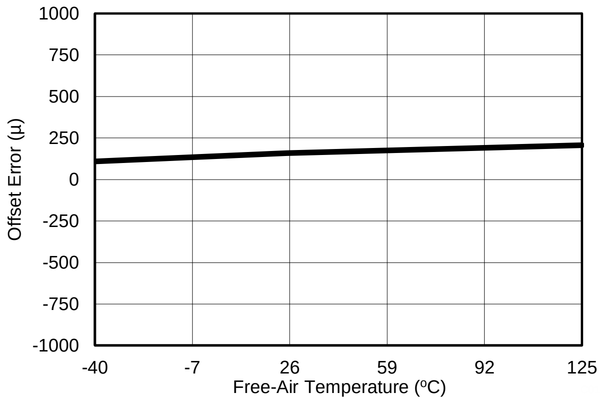


Figure 29. Offset Error vs Device Temperature

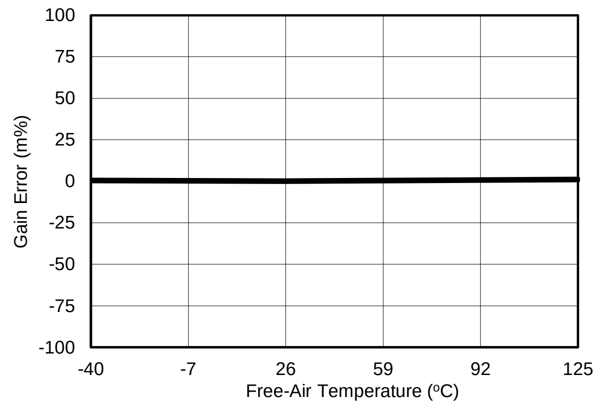


Figure 30. Gain Error vs Device Temperature

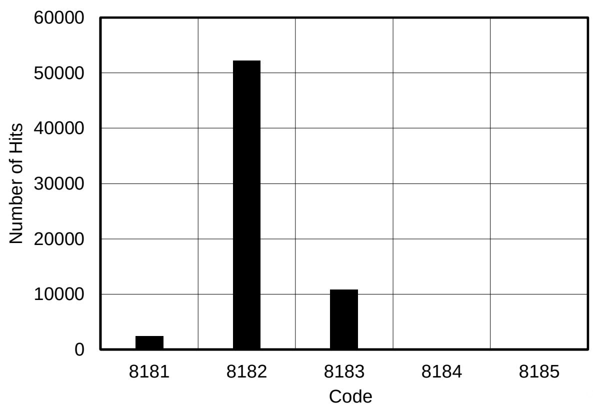


Figure 31. DC Histogram

6.13 Typical Characteristics: ADS8350

at T_A = 25°C, AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 2.5 V, and f_{DATA} = 750 kSPS (unless otherwise noted)

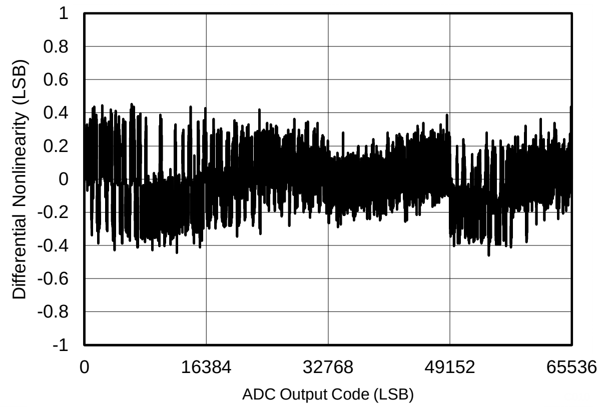


Figure 32. Typical DNL

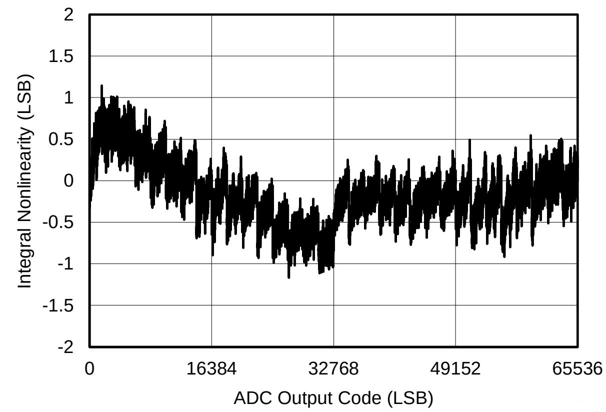


Figure 33. Typical INL

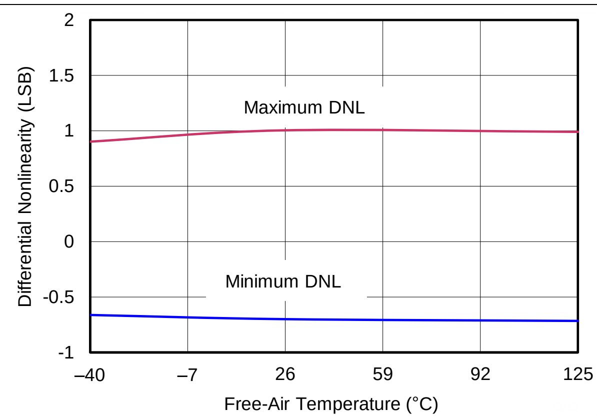


Figure 34. DNL vs Device Temperature

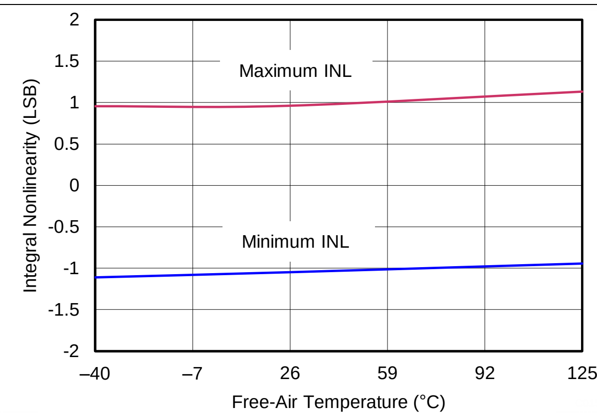


Figure 35. INL vs Device Temperature

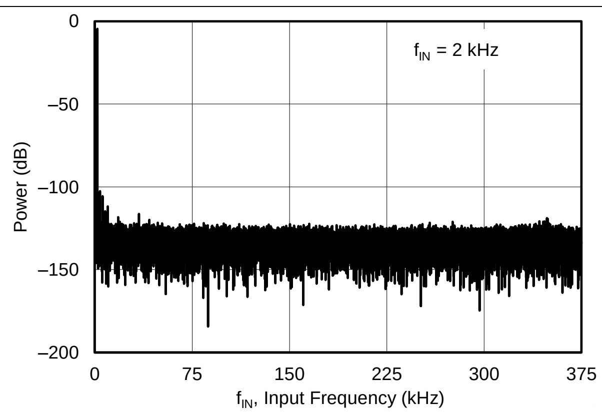


Figure 36. Typical FFT at 2-kHz Input

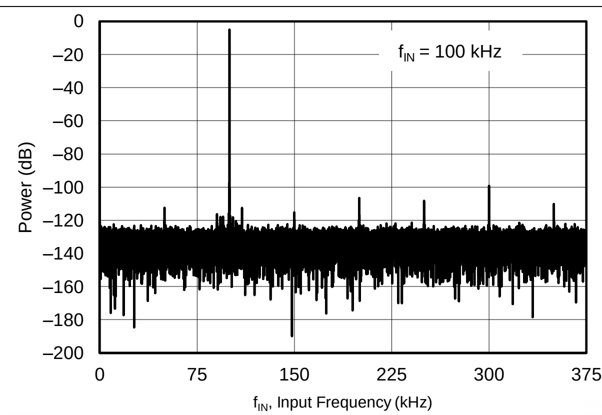


Figure 37. Typical FFT at 100-kHz Input

Typical Characteristics: ADS8350 (continued)

at T_A = 25°C, AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 2.5 V, and f_{DATA} = 750 kSPS (unless otherwise noted)

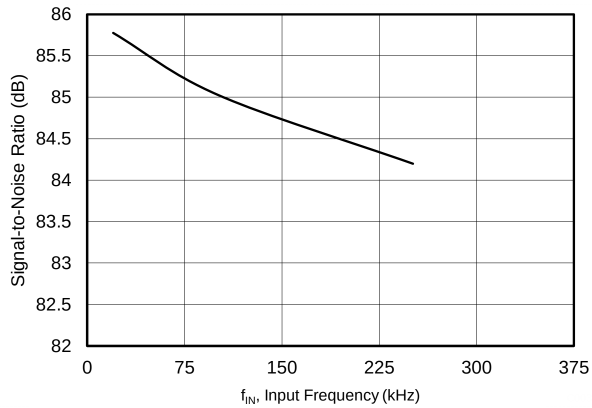


Figure 38. SNR vs Input Frequency

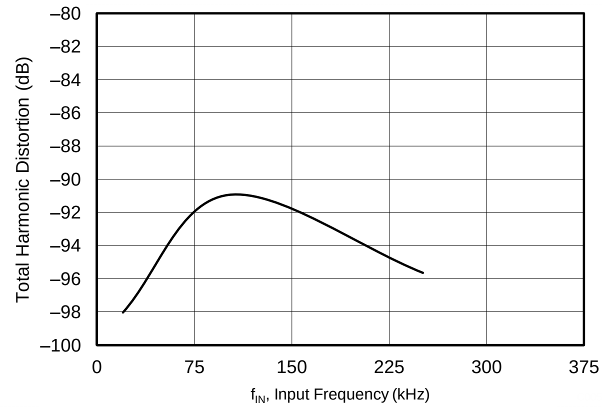


Figure 39. THD vs Input Frequency

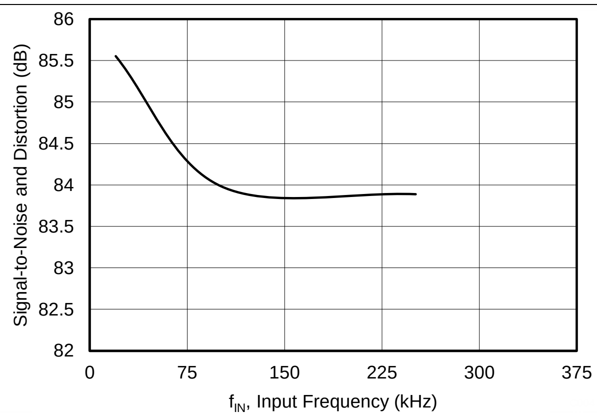


Figure 40. SINAD vs Input Frequency

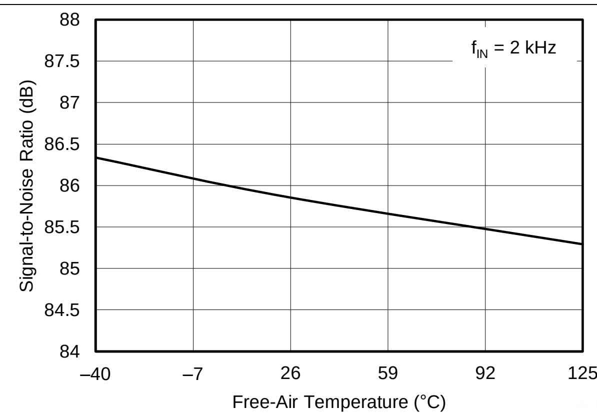


Figure 41. SNR vs Device Temperature

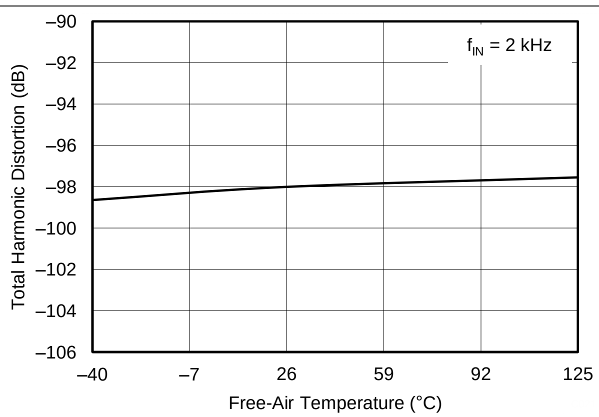


Figure 42. THD vs Device Temperature

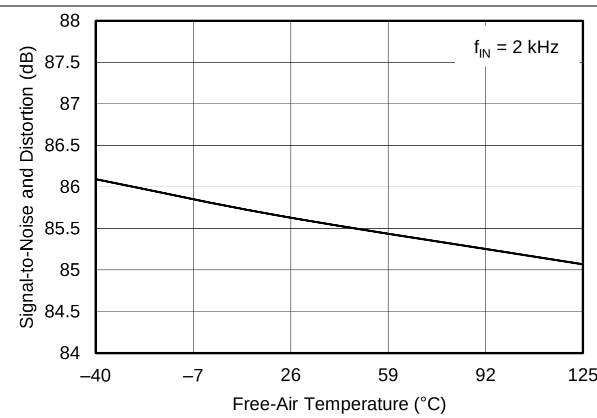


Figure 43. SINAD vs Device Temperature

Typical Characteristics: ADS8350 (continued)

at T_A = 25°C, AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 2.5 V, and f_{DATA} = 750 kSPS (unless otherwise noted)

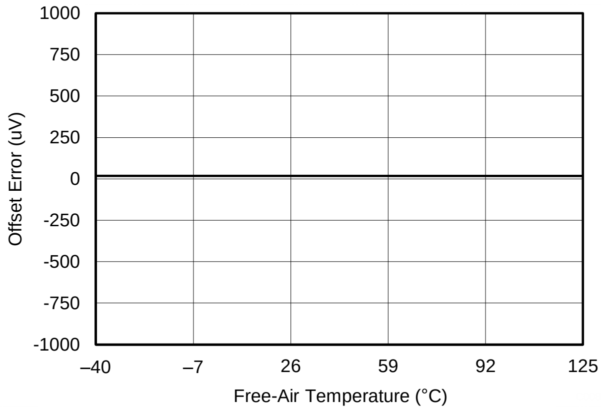


Figure 44. Offset Error vs Device Temperature

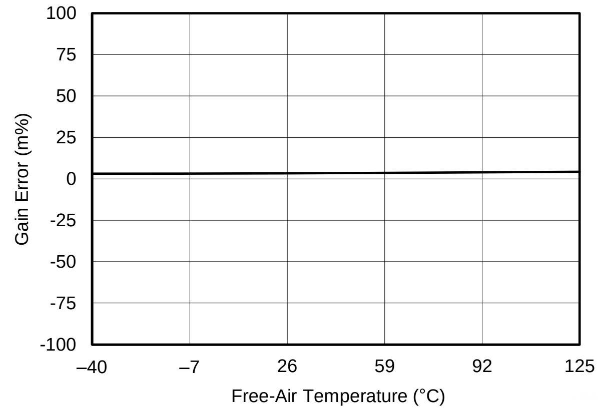


Figure 45. Gain Error vs Device Temperature

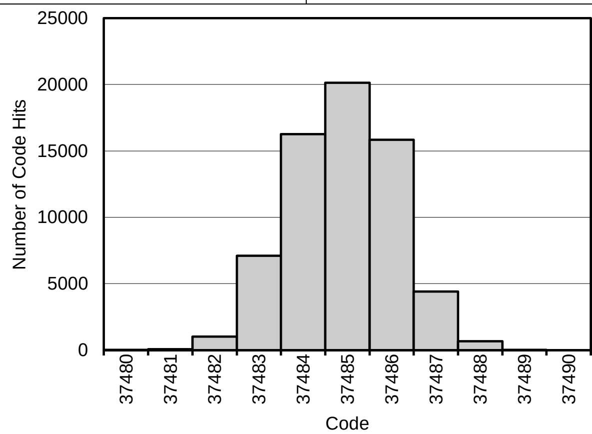


Figure 46. DC Histogram

6.14 Typical Characteristics: All Devices

at T_A = 25°C, AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 2.5 V, and f_{DATA} = 750 kSPS (unless otherwise noted)

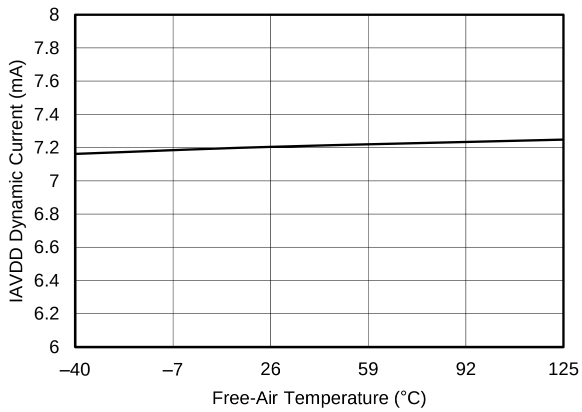


Figure 47. Dynamic Current vs Device Temperature

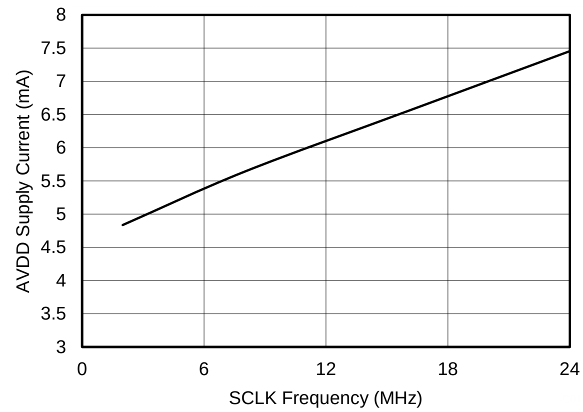


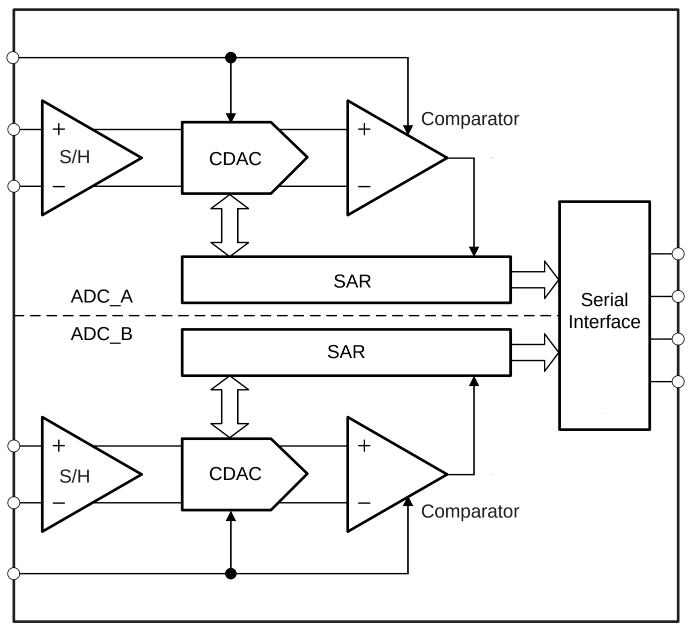
Figure 48. Supply Current vs SCLK Frequency

7 Detailed Description

7.1 Overview

The ADS8350, ADS7850, and ADS7250 belong to a family of dual, high-speed, simultaneous-sampling, analog-to-digital converters (ADCs). The devices support pseudo-differential input signals with the input common-mode equal to the reference voltage and the full-scale input range equal to twice the reference voltage. The devices provide a simple serial interface to the host controller and operate over a wide range of digital power supplies.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Reference

Each device has two simultaneous-sampling ADCs (ADC_A and ADC_B). ADC_A operates with reference voltage V_{REFIN_A} and ADC_B operates with reference voltage V_{REFIN_B}. These reference voltages must be provided on the REFIN_A and REFIN_B pins, respectively. REFIN_A and REFIN_B may be set to different values as per the application requirement.

As shown in Figure 49, decouple the REFIN_A and REFIN_B pins with the REFGND_A and REFGND_B pins, respectively, with individual 10-µF decoupling capacitors.

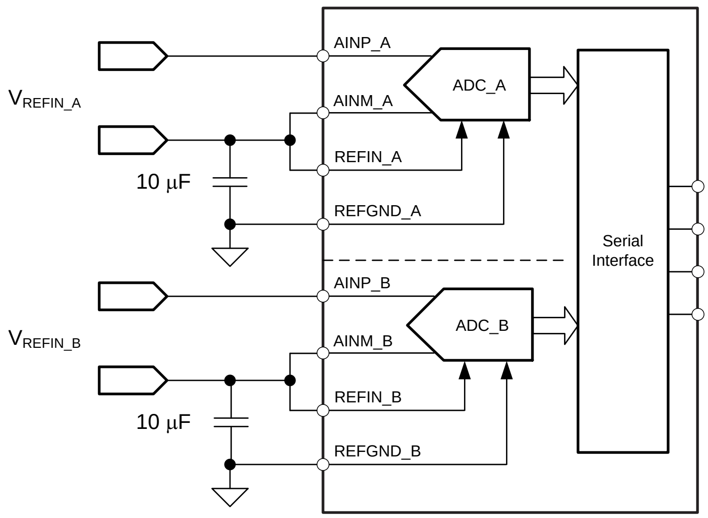


Figure 49. Reference Block Diagram

Feature Description (continued)

7.3.2 Analog Input

The devices support pseudo-differential analog input signals. These inputs are sampled and converted simultaneously by the two ADCs (ADC_A and ADC_B). ADC_A samples and converts ($V_{AINP\_A} - V_{AINM\_A}$), and ADC_B samples and converts ($V_{AINP\_B} - V_{AINM\_B}$).

Figure 50a and Figure 50b show equivalent circuits for the ADC_A and ADC_B analog input pins, respectively. R_S (typically 50 Ω) represents the on-state sampling switch resistance, and C_{SAMPLE} represents the device sampling capacitor (typically 40 pF).

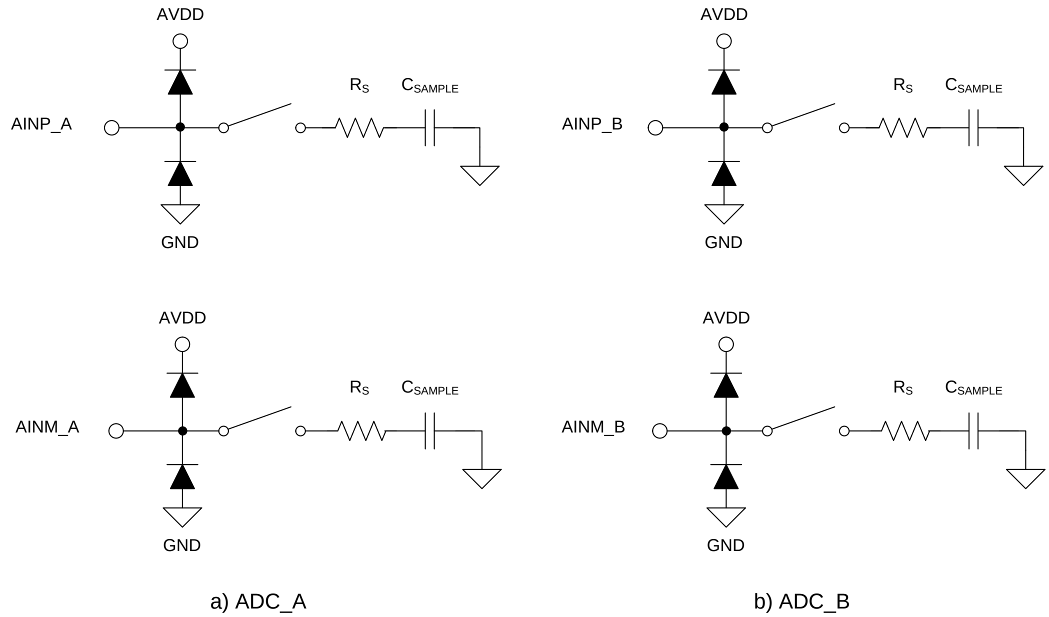


Figure 50. Equivalent Circuit for Analog Input Pins

7.3.2.1 Analog Input Full-Scale Range

The analog input full-scale range (FSR) for ADC_A and ADC_B is twice the reference voltage provided to the particular ADC. By providing different reference voltages (V_{REFIN_A} and V_{REFIN_B}), ADC_A and ADC_B can have different full-scale input ranges. Therefore, the FSR for ADC_A and ADC_B can be determined by Equation 1 and Equation 2, respectively:

$$FSR\_ADC\_A = 2 \times V_{REFIN\_A},\quad V_{AINP\_A} = 0 \text{ to } 2 \times V_{REFIN\_A},\quad V_{AINM\_A} = V_{REFIN\_A} \tag{1}$$

The REFIN_A and AINM_A pins must be shorted and connected to the external reference voltage, V_{REFIN_A}.

$$FSR\_ADC\_B = 2 \times V_{REFIN\_B},\quad V_{AINP\_B} = 0 \text{ to } 2 \times V_{REFIN\_B},\quad V_{AINM\_B} = V_{REFIN\_B} \tag{2}$$

The REFIN_B and AINM_B pins must be shorted and connected to the external reference voltage, V_{REFIN_B}.

To use the full dynamic input range on the analog input pins, AVDD must be as shown in Equation 3, Equation 4, and Equation 5:

$$AVDD \geq 2 \times V_{REFIN\_A} \tag{3}$$

$$AVDD \geq 2 \times V_{REFIN\_B} \tag{4}$$

$$4.5\text{ V} \leq AVDD \leq 5.5\text{ V} \tag{5}$$

Feature Description (continued)

7.3.3 ADC Transfer Function

The device output is in binary twos complement format. Device resolution is calculated by Equation 6:

$$1\ LSB = (FSR\_ADC\_x) / (2^N)$$

where:

- $FSR\_ADC\_x = 2 \times V_{REFIN\_x}$ and
- N is the resolution of the ADC : N = 16 for the ADS8350, N = 14 for the ADS7850, and N = 12 for the ADS7250 (6)

Table 1 shows the different input voltages and the corresponding device output codes.

Table 1. Transfer Characteristics

INPUT VOLTAGE (AINM_x)	INPUT VOLTAGE (AINP_x)	PSEUDO-DIFFERENTIAL INPUT TO ADC (AINP_x - AINM_x)		OUTPUT CODE (HEX)			
				CODE	ADS7250	ADS7850	ADS8350
V_{REFIN_x}	0	$-V_{REFIN\_x}$	NFSR	NFSC	800	2000	8000
	1 LSB	$-V_{REFIN\_x}$ + 1 LSB	NFSR + 1 LSB	NFSC + 1	801	2001	8001
	V_{REFIN_x} – 1 LSB	–1 LSB	–1 LSB	MC	FFF	3FFF	FFFF
	V_{REFIN_x}	0	0	PLC	000	0000	0000
	2 × V_{REFIN_x} – 1 LSB	V_{REFIN_x} – 1 LSB	PFSR – 1 LSB	PFSC	7FF	1FFF	7FFF

Figure 51 shows the ideal transfer characteristics for the device.

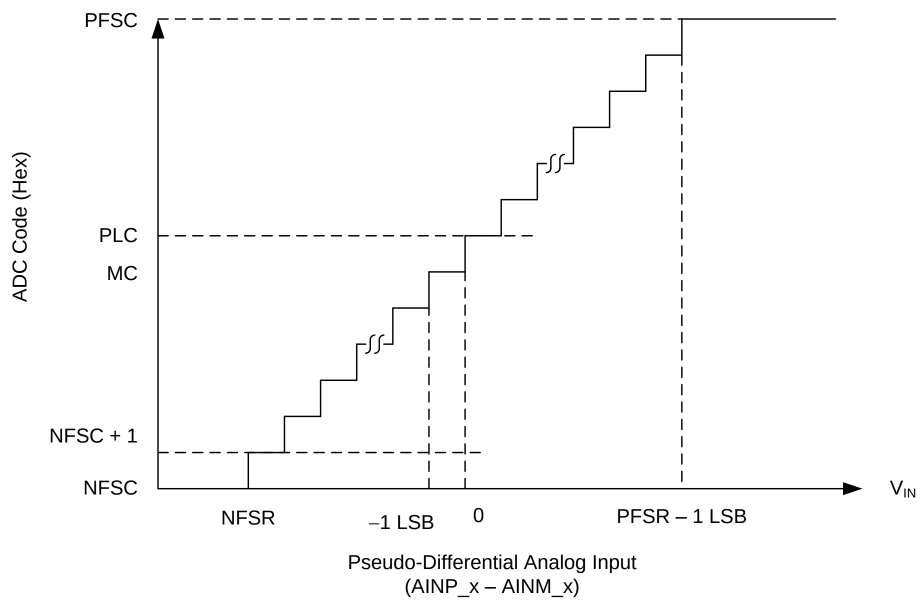


Figure 51. Ideal Transfer Characteristics

7.4 Device Functional Modes

7.4.1 Serial Interface

The devices support a simple, SPI-compatible serial interface to the external digital host. The $\overline{CS}$ signal defines one conversion and serial transfer frame. A frame starts with a $\overline{CS}$ falling edge and ends with a $\overline{CS}$ rising edge. The SDO_A and SDO_B pins output the ADC_A and ADC_B conversion results, respectively. Figure 52 shows a detailed timing diagram for these devices.

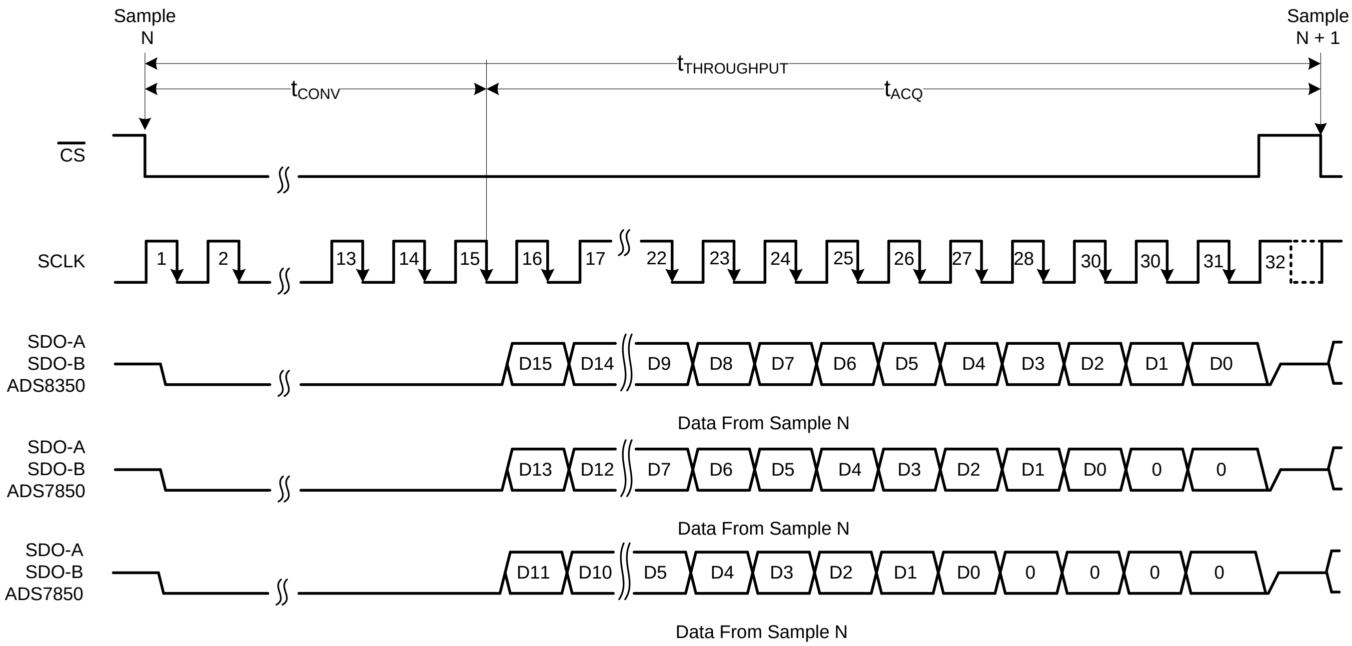


Figure 52. Serial Interface Timing Diagram

A $\overline{CS}$ falling edge brings the serial data bus out of 3-state and also outputs a '0' on the SDO_A and SDO_B pins. The device converts the sampled analog input during the next 14 clocks. SDO_A and SDO_B read '0' during this period. The sample-and-hold circuit goes back into sample mode on the 15th SCLK falling edge and the MSBs of ADC_A and ADC_B are output on SDO_A and SDO_B, respectively. The subsequent clock edges are used to shift out the conversion result using the serial interface, as shown in Table 2. Output data are in binary twos complement format. A $\overline{CS}$ rising edge ends the frame and puts the serial bus into 3-state.

Table 2. Data Launch Edge

		LAUNCH EDGE													
			SCLK												
DEVICE	PIN	$\overline{CS}$ ↓	↓1	…	↓14	↓15	…	↓26	↓27	↓28	↓29	↓30	↓31	…	$\overline{CS}$ ↑
ADS8350	SDO-A	0	0	…	0	D15_A	…	D4_A	D3_A	D2_A	D1_A	D0_A	0	…	Hi-Z
	SDO-B	0	0	…	0	D15_B	…	D4_B	D3_B	D2_B	D1_B	D0_B	0	…	Hi-Z
ADS7850	SDO-A	0	0	…	0	D13_A	…	D2_A	D1_A	D0_A	0	0	0	…	Hi-Z
	SDO-B	0	0	…	0	D13_B	…	D2_B	D1_B	D0_B	0	0	0	…	Hi-Z
ADS7250	SDO-A	0	0	…	0	D11_A	…	D0_A	0	0	0	0	0	…	Hi-Z
	SDO-B	0	0	…	0	D11_B	…	D0_B	0	0	0	0	0	…	Hi-Z

7.4.2 Short-Cycling, Frame Abort, and Reconversion Feature

Referring to Table 2, the ADS8350 requires a minimum of 31 SCLK falling edges between the beginning and end of the frame to complete the 16-bit data transfer, the ADS7850 requires a minimum of 29 SCLK falling edges between the beginning and end of the frame to complete the 14-bit data transfer, and the ADS7250 requires a minimum of 27 SCLK falling edges between the beginning and end of the frame to complete the 12-bit data transfer. However, CS can be brought high at any time during the frame to abort the frame or to *short-cycle* the converter.

As shown in Figure 53, if CS is brought high before the 15th SCLK falling edge, the device aborts the conversion and starts sampling the new analog input signal.

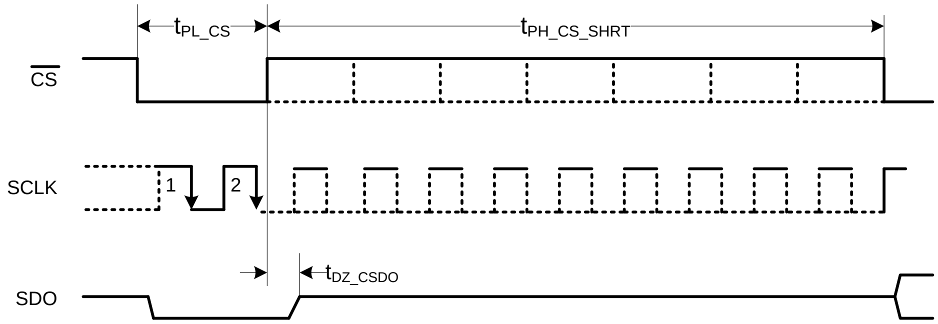


Figure 53. Frame Aborted before 15th SCLK Falling Edge

If CS is brought high after the 15th SCLK falling edge (as shown in Figure 54), the output data bits latched into the digital host before this CS rising edge are still valid data corresponding to sample *N*.

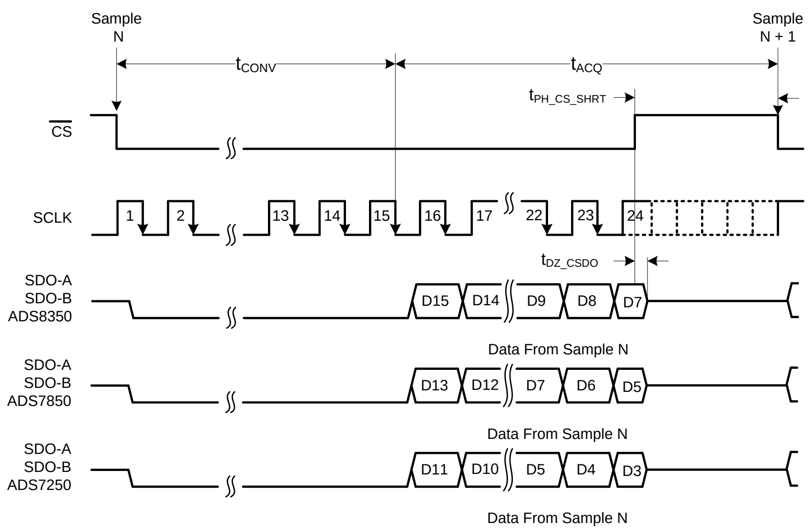


Figure 54. Frame Aborted after 15th SCLK Falling Edge

After aborting the current frame, CS must be kept high for $t_{PH\_CS\_SHRT}$ to ensure that the minimum acquisition time (t_{ACQ}) is provided for the next conversion.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The two primary circuits required to maximize the performance of a high-precision, successive approximation register (SAR), analog-to-digital converter (ADC) are the input driver and the reference driver circuits. This section details some general principles for designing these circuits and provides some application circuits designed using these devices.

8.2 Typical Applications

8.2.1 DAQ Circuit: Maximum SINAD for a 10-kHz Input Signal at 750-kSPS Throughput

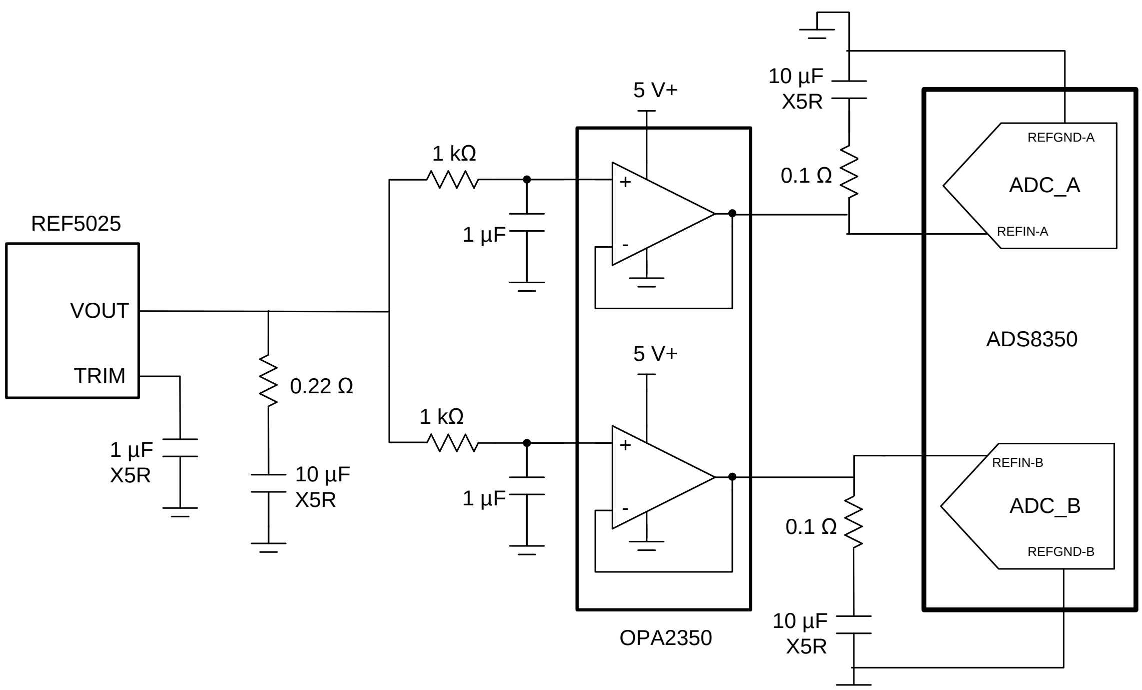


Figure 55. Reference Drive Circuit with V_{REF} = 2.5 V

Typical Applications (continued)

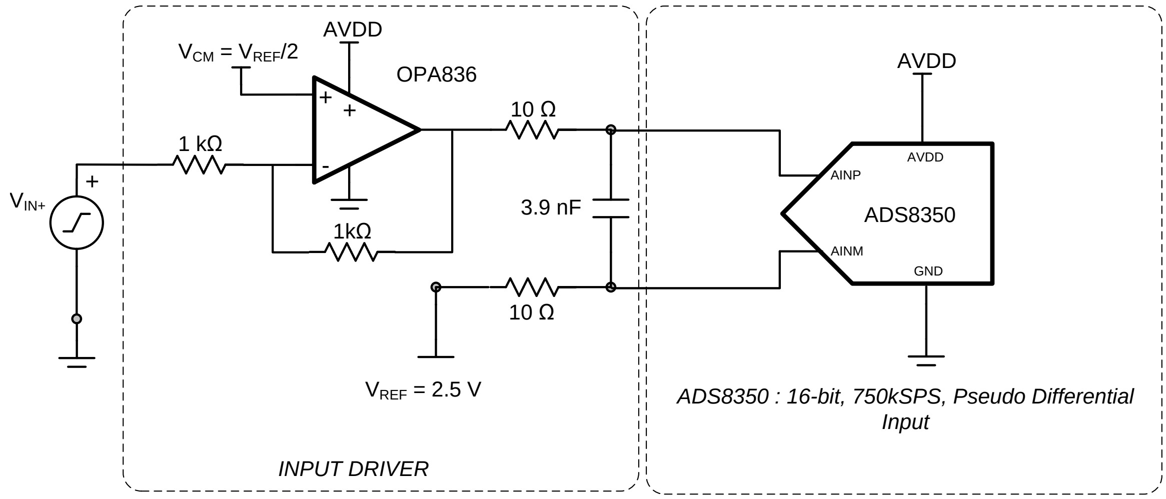


Figure 56. DAQ Circuit: Maximum SINAD for a 10-kHz Input Signal at 750-kSPS Throughput

8.2.1.1 Design Requirements

For the ADS8350, design an input driver and reference driver circuit to achieve > 84-dB SNR and < –90-dB THD at a 100-kHz input frequency.

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 ADC Reference Driver

The external reference source to the device must provide low-drift and very accurate voltage for the ADC reference input and support the dynamic charge requirements without affecting the noise and linearity performance of the device. The output broadband noise of most references can be in the order of a few 100 μV_{RMS}. Therefore, in order to prevent any degradation in the noise performance of the ADC, the output of the voltage reference must be appropriately filtered by using a low-pass filter with a cutoff frequency of a few hundred Hertz.

After band-limiting the noise from the reference source, the next important step is to design a reference buffer that can drive the dynamic load posed by the reference input of the ADC. At the start of each conversion, the reference buffer must regulate the voltage of the reference pin within 1 LSB of the intended value. This condition necessitates the use of a large filter capacitor at the reference pin of the ADC. The amplifier selected to drive this large capacitor should have low output impedance, low offset, and temperature drift specifications.

To reduce the dynamic current requirements and crosstalk between the channels, a separate reference buffer is recommended for driving the reference input of each ADC channel.

The application circuit in Figure 55 shows the schematic of a complete reference driver circuit that generates a voltage of 2.5-V dc using a single 5-V supply.

The 2.5-V reference voltage is generated by the high-precision, low-noise REF5025 circuit. The output broadband noise of the reference is heavily filtered by a low-pass filter with a 3-dB cutoff frequency of 160 Hz. The decoupling capacitor on each reference pin is selected to be 10 µF. The low output impedance, low noise, and fast settling time makes the OPA2350 a good choice for driving this high capacitive load.

8.2.1.2.2 ADC Input Driver

The input driver circuit for a high-precision ADC mainly consists of two parts: a driving amplifier and a fly-wheel RC filter. The amplifier is used for signal conditioning of the input voltage and its low output impedance provides a buffer between the signal source and the switched capacitor inputs of the ADC. The RC filter helps attenuate the sampling charge injection from the switched-capacitor input stage of the ADC and functions as an antialiasing filter to band-limit the wideband noise contributed by the front-end circuit. Careful design of the front-end circuit is critical to meet the linearity and noise performance of a high-precision ADC.

Typical Applications (continued)

8.2.1.2.2.1 Input Amplifier Selection

Selection criteria for the input amplifiers is highly dependent on the input signal type and the performance goals of the data acquisition system. Some key amplifier specifications to consider while selecting an appropriate amplifier to drive the inputs of the ADC are:

- *Small-signal bandwidth.* Select the small-signal bandwidth of the input amplifiers to be as high as possible after meeting the power budget of the system. Higher bandwidth reduces the closed-loop output impedance of the amplifier, thus allowing the amplifier to more easily drive the low cutoff frequency RC filter at the ADC inputs. Higher bandwidth also minimizes the harmonic distortion at higher input frequencies. In order to maintain the overall stability of the input driver circuit, the amplifier bandwidth should be selected as described in Equation 7:

$$Unity - Gain\ Bandwidth \geq 4 \times \left(\frac{1}{2\pi \times (R_{FLT} + R_{FLT}) \times C_{FLT}} \right) \tag{7}$$

- *Noise.* Noise contribution of the front-end amplifiers should be as low as possible to prevent any degradation in SNR performance of the system. As a rule of thumb, to ensure that the noise performance of the data acquisition system is not limited by the front-end circuit, the total noise contribution from the front-end circuit should be kept below 20% of the input-referred noise of the ADC. Noise from the input driver circuit is band-limited by designing a low cutoff frequency RC filter, as explained in Equation 8.

$$N_G \times \sqrt{2} \times \sqrt{\left(\frac{V_{1/f\_AMP\_PP}}{6.6} \right)^2 + e^2_{n\_RMS} \times \frac{\pi}{2} \times f_{-3dB}} \leq \frac{1}{5} \times \frac{V_{REF}}{\sqrt{2}} \times 10^{-\left(\frac{SNR(dB)}{20} \right)}$$

where:

- $V_{1\ /\ f\_AMP\_PP}$ is the peak-to-peak flicker noise in μV_{RMS},
- e_{n_RMS} is the amplifier broadband noise density in nV/$\sqrt{Hz}$,
- f_{-3dB} is the 3-dB bandwidth of the RC filter, and
- N_G is the noise gain of the front-end circuit, which is equal to '1' in a buffer configuration. (8)

- *Distortion.* Both the ADC and the input driver introduce nonlinearity in a data acquisition block. As a rule of thumb, to ensure that the distortion performance of the data acquisition system is not limited by the front-end circuit, the distortion of the input driver should be at least 10 dB lower than the distortion of the ADC, as shown in Equation 9.

$$THD_{AMP} \leq THD_{ADC} - 10\,(dB) \tag{9}$$

- *Settling Time.* For dc signals with fast transients that are common in a multiplexed application, the input signal must settle to the desired accuracy at the inputs of the ADC during the acquisition time window. This condition is critical to maintain the overall linearity performance of the ADC. Typically, the amplifier data sheets specify the output settling performance only up to 0.1% to 0.001%, which may not be sufficient for the desired accuracy. Therefore, the settling behavior of the input driver should always be verified by TINA™-SPICE simulations before selecting the amplifier.

Typical Applications (continued)

8.2.1.2.2.2 Antialiasing Filter

Converting analog-to-digital signals requires sampling an input signal at a constant rate. Any higher frequency content in the input signal beyond half the sampling frequency is digitized and folded back into the low-frequency spectrum. This process is called *aliasing*. Therefore, an analog, antialiasing filter must be used to remove the harmonic content from the input signal before being sampled by the ADC. An antialiasing filter is designed as a low-pass, RC filter, for which the 3-dB bandwidth is optimized based on specific application requirements. For dc signals with fast transients (including multiplexed input signals), a high-bandwidth filter is designed to allow accurately settling the signal at the ADC inputs during the small acquisition time window. For ac signals, the filter bandwidth should be kept low to band-limit the noise fed into the ADC input, thereby increasing the signal-to-noise ratio (SNR) of the system.

Besides filtering noise from the front-end drive circuitry, the RC filter also helps attenuate the sampling charge injection from the switched-capacitor input stage of the ADC. A filter capacitor, C_{FLT}, is connected across the ADC inputs (as shown in Figure 57).

$$f_{-3dB} = \frac{1}{2\pi \times (R_{FLT} + R_{FLT}) \times C_{FLT}}$$

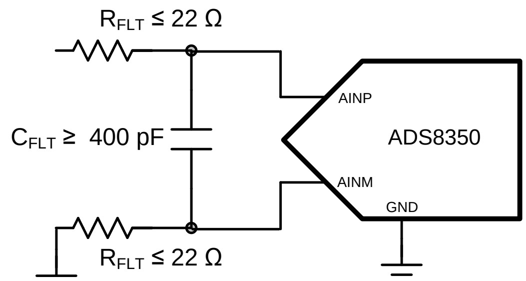


Figure 57. Antialiasing Filter

This capacitor helps reduce the sampling charge injection and provides a charge bucket to quickly charge the internal sample-and-hold capacitors during the acquisition process. As a rule of thumb, the value of this capacitor should be at least 10 times the specified value of the ADC sampling capacitance. For these devices, the input sampling capacitance is equal to 40 pF. Thus, the value of C_{FLT} should be greater than 400 pF. The capacitor should be a COG- or NPO-type because these capacitor types have a high-Q, low-temperature coefficient, and stable electrical characteristics under varying voltages, frequency, and time.

Note that driving capacitive loads can degrade the phase margin of the input amplifiers, thus making the amplifier marginally unstable. To avoid amplifier stability issues, series isolation resistors (R_{FLT}) are used at the output of the amplifiers. A higher value of R_{FLT} is helpful from the amplifier stability perspective, but adds distortion as a result of interactions with the nonlinear input impedance of the ADC. Distortion increases with source impedance, input signal frequency, and input signal amplitude. Therefore, the selection of R_{FLT} requires balancing the stability and distortion of the design. For these devices, TI recommends limiting the value of R_{FLT} to a maximum of 22 Ω in order to avoid any significant degradation in linearity performance. The tolerance of the selected resistors can be chosen as 1% because the use of a differential capacitor at the input balances the effects resulting from any resistor mismatch.

The input amplifier bandwidth should be much higher than the cutoff frequency of the antialiasing filter. TI strongly recommends performing a SPICE simulation to confirm that the amplifier has more than 40° phase margin with the selected filter. Simulation is critical because even with high-bandwidth amplifiers, some amplifiers might require more bandwidth than others to drive similar filters. If an amplifier has less than a 40° phase margin with 22-Ω resistors, using a different amplifier with higher bandwidth or reducing the filter cutoff frequency with a larger differential capacitor is advisable.

The application circuit shown in Figure 56 is optimized to achieve lowest distortion and lowest noise for a 10-kHz input signal. The input signal is processed through a high-bandwidth, low-distortion amplifier in an inverting gain configuration and a low-pass RC filter before being fed into the ADS8350 operating at 750-kSPS throughput.

Typical Applications (continued)

As a rule of thumb, the distortion from the input driver should be at least 10 dB less than the ADC distortion. The distortion resulting from variation in the common-mode signal is eliminated by using the amplifier in an inverting gain configuration that establishes a fixed common-mode level for the circuit. The low-power OPA836, used as an input driver, provides exceptional ac performance because of its extremely low-distortion, high-bandwidth specifications. In addition, the components of the antialiasing filter are such that the noise from the front-end circuit is kept low without adding distortion to the input signal.

NOTE

The same circuit can be used with the ADS7250 and ADS7850 to achieve their rated specifications.

8.2.1.3 Application Curve

Figure 58 shows FFT plot and test results obtained with circuit configuration shown in Figure 56.

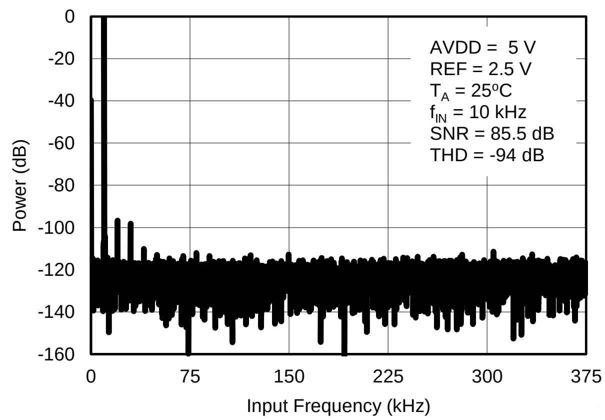


Figure 58. FFT Plot and Test Results with ADS8350

Typical Applications (continued)

8.2.2 DAQ Circuit: Maximum SINAD for a 100-kHz Input Signal at 750-kSPS Throughput

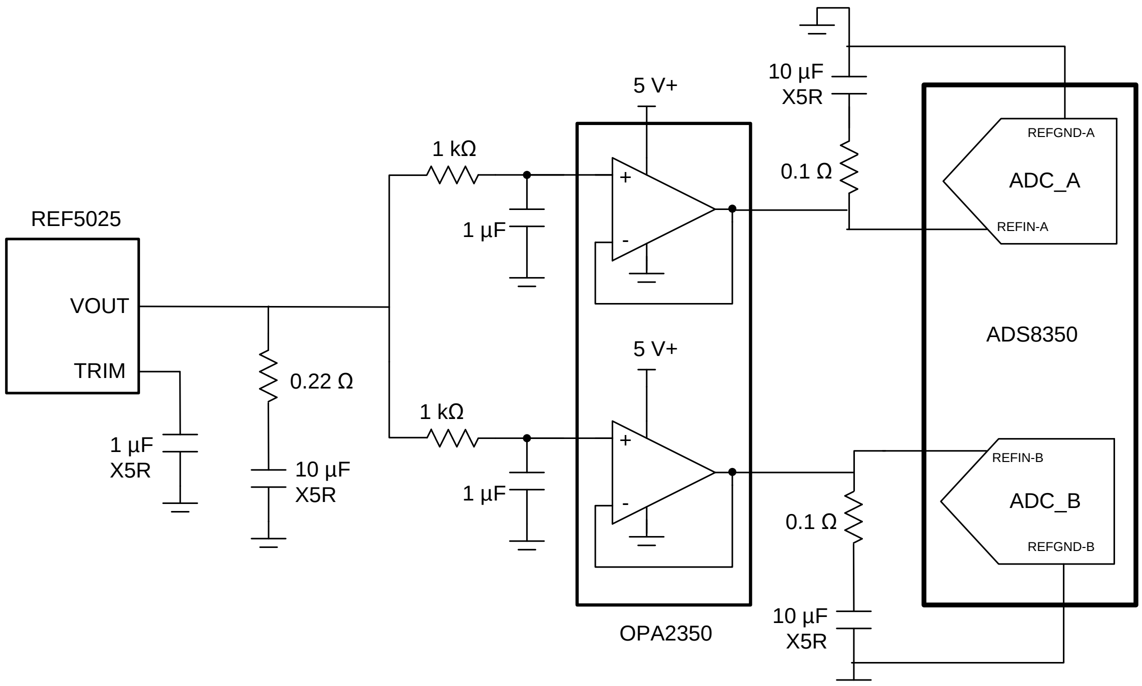


Figure 59. Reference Drive Circuit with V_{REF} = 2.5 V

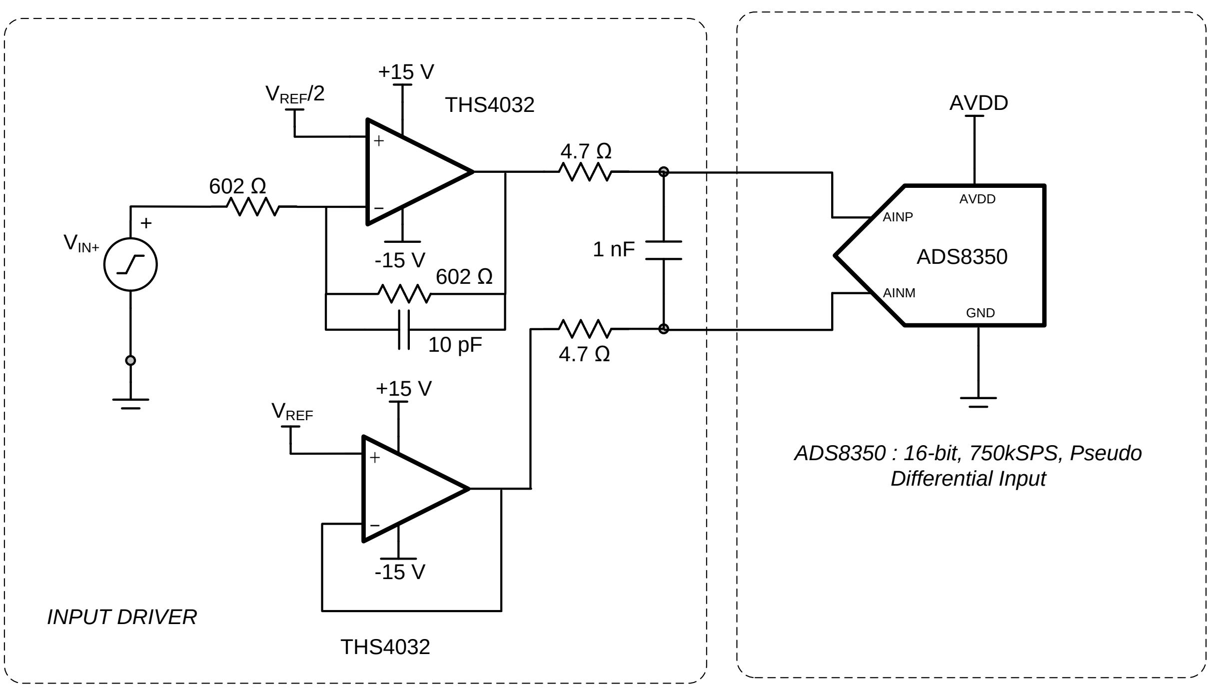


Figure 60. DAQ Circuit: Maximum SINAD for a 100-kHz Input Signal at 750-kSPS Throughput

Typical Applications (continued)

8.2.2.1 Design Requirements

For the ADS8350, design an input driver and reference driver circuit to achieve > 84-dB SNR and < –90-dB THD at a 100-kHz input frequency.

8.2.2.2 Detailed Design Procedure

8.2.2.2.1 ADC Reference Driver

Refer to the *ADC Reference Driver* section for a detailed design procedure for the ADC reference driver.

The application circuit in Figure 55 shows the schematic of a complete reference driver circuit that generates a voltage of 2.5-V dc using a single 5-V supply. This circuit is suitable to drive the reference of the ADS8350 at sampling rates up to 750 kSPS.

The 2.5-V reference voltage is generated by the high-precision, low-noise REF5025 circuit. The output broadband noise of the reference is heavily filtered by a low-pass filter with a 3-dB cutoff frequency of 160 Hz. The decoupling capacitor on each reference pin is selected to be 10 µF. The low output impedance, low noise, and fast settling time makes the OPA2350 a good choice for driving this high capacitive load.

8.2.2.2.2 ADC Input Driver

Refer to *ADC Input Driver* section for the detailed design procedure for an ADC input driver.

The application circuit shown in Figure 60 is optimized to achieve lowest distortion and lowest noise for a 100-kHz input signal. The input signal is processed through a high-bandwidth, low-distortion amplifier in an inverting gain configuration and a low-pass RC filter before being fed into the ADS8350 operating at 750-kSPS throughput.

As a rule of thumb, the distortion from the input driver should be at least 10 dB less than the ADC distortion. The distortion resulting from variation in the common-mode signal is eliminated by using the amplifier in an inverting gain configuration that establishes a fixed common-mode level for the circuit. This configuration also eliminates the requirement of a rail-to-rail swing at the input of the amplifier. The THS4032, used as an input driver, provides exceptional ac performance because of its extremely low-distortion, low-noise, and high-bandwidth specifications. The ADC AINM pin is also driven to V_{REF} with the same amplifier to match the source impedance and to take full advantage of the pseudo-differential input structure of the ADC. In addition, the components of the antialiasing filter are such that the noise from the front-end circuit is kept low without adding distortion to the input signal.

NOTE

The same circuit can be used with the ADS7250 and ADS7850 to achieve their rated specifications.

Typical Applications (continued)

8.2.2.3 Application Curve

Figure 61 shows FFT plot and test results obtained with circuit configuration shown in Figure 60.

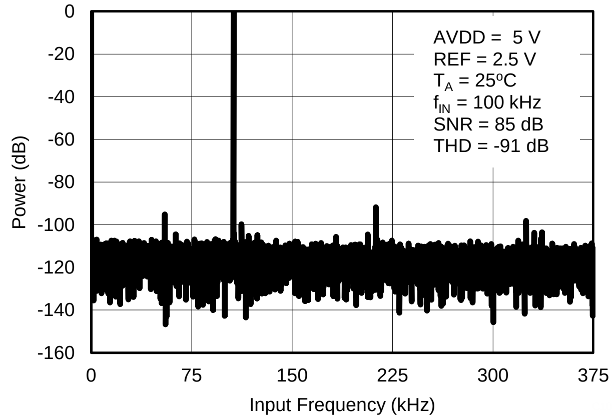


Figure 61. FFT Plot and Test Results with ADS8350

9 Power Supply Recommendations

The devices have two separate power supplies: AVDD and DVDD. The ADC operates on AVDD; DVDD is used for the interface circuits. AVDD and DVDD can be independently set to any value within the permissible range.

The AVDD supply voltage value defines the permissible voltage swing on the analog input pins. To avoid saturation of output codes, the external reference voltages V_{REFIN_A} and V_{REFIN_B} should be as shown in Equation 10:

$$2\text{ V} \leq V_{REFIN\_x} \leq \text{AVDD} / 2 \quad (10)$$

In other words, in order to use the V_{REFIN_x} external reference voltage and use the full dynamic range on the analog input pins, AVDD must be set as shown in Equation 11, Equation 12, and Equation 13:

$$\text{AVDD} \geq 2 \times V_{REFIN\_A} \quad (11)$$
$$\text{AVDD} \geq 2 \times V_{REFIN\_B} \quad (12)$$
$$4.5\text{ V} \leq \text{AVDD} \leq 5.5\text{ V} \quad (13)$$

Decouple the AVDD and DVDD pins with the GND pin using individual 10-µF decoupling capacitors, as shown in Figure 62.

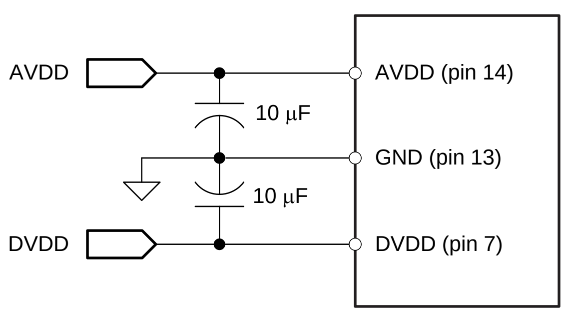


Figure 62. Power-Supply Decoupling

10 Layout

10.1 Layout Guidelines

Figure 63 shows a board layout example for the ADS7250, ADS7850, and ADS8350. Use a ground plane underneath the device and partition the PCB into analog and digital sections. Avoid crossing digital lines with the analog signal path and keep the analog input signals and the reference input signals away from noise sources. As shown in Figure 63, the analog input and reference signals are routed on the left side of the board and the digital connections are routed on the right side of the device.

The power sources to the ADS8350 must be clean and well-bypassed. Use 10-µF ceramic bypass capacitors in close proximity to the analog (AVDD) and digital (DVDD) power-supply pins. Avoid placing vias between the AVDD and DVDD pins and the bypass capacitors. Connect all ground pins to the ground plane using short, low-impedance paths.

The REFIN-A and REFIN-B reference inputs are bypassed with 10-µF, X7R-grade ceramic capacitors ($C_{REF\text{-}x}$). Although the reference inputs of the device draw little current on average, there are instantaneous dynamic current demands placed on the reference circuitry characteristic of SAR ADCs. Place the reference bypass capacitors as close as possible to the reference REFIN-x pins and connect the bypass capacitors using short, low-inductance connections. Avoid placing vias between the REFIN-x pins and the bypass capacitors. If the reference voltage originates from an op amp, make sure that the op amp can drive the bypass capacitor without oscillation. Small 0.1-Ω to 0.2-Ω resistors ($R_{REF\text{-}x}$) are used in series with the reference bypass capacitors to improve stability.

The fly-wheel RC filters are placed immediately next to the input pins. Among ceramic surface-mount capacitors, COG (NPO) ceramic capacitors provide the best capacitance precision. The type of dielectric used in COG (NPO) ceramic capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes. Figure 63 shows the $C_{IN\text{-}A}$ and $C_{IN\text{-}B}$ filter capacitors placed across the analog input pins of the device.

10.2 Layout Example

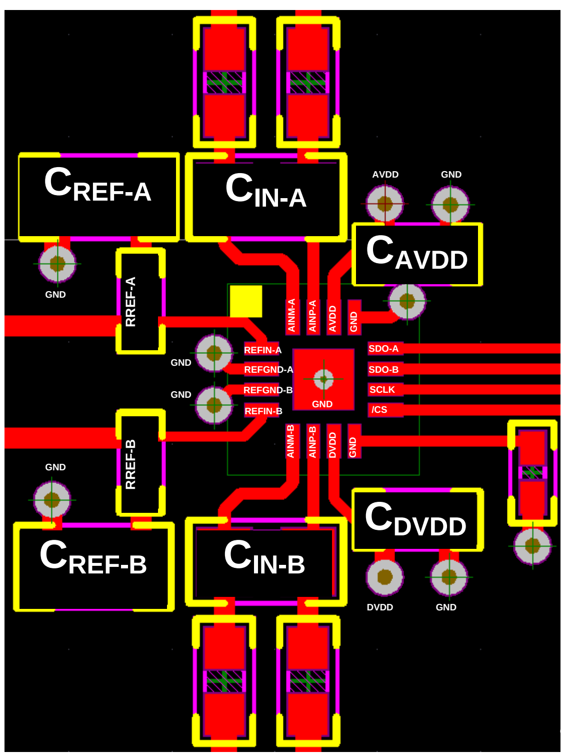


Figure 63. Layout Example

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントのサポート

11.1.1 関連資料

関連資料については、以下を参照してください。

- 『*REF50xx 低ノイズ、超低ドリフト係数、高精度基準電圧*』
- 『*OPAx350 MicroAmplifierシリーズの高速、単一電源、レール・ツー・レールのオペアンプ*』
- 『*OPAx836 超低消費電力、レール・ツー・レール出力、負のレール入力、電圧フィードバックのオペアンプ*』
- 『*THS403x 100MHz、低ノイズ、高速アンプ*』

11.2 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびご注文へのクイック・アクセスが含まれます。

表 3. 関連リンク

製品	プロダクト・フォルダ	ご注文はこちら	技術資料	ツールとソフトウェア	サポートとコミュニティ
ADS8350	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
ADS7850	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
ADS7250	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

11.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™オンライン・コミュニティ ***TIのE2E（Engineer-to-Engineer）コミュニティ。*** エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。

設計サポート ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

11.5 商標

TINA, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS7250IRTER	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7250
ADS7250IRTER.A	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7250
ADS7250IRTER.B	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7250
ADS7250IRTET	Active	Production	WQFN (RTE) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7250
ADS7250IRTET.A	Active	Production	WQFN (RTE) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7250
ADS7250IRTET.B	Active	Production	WQFN (RTE) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7250
ADS7850IRTER	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7850
ADS7850IRTER.A	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7850
ADS7850IRTER.B	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7850
ADS7850IRTET	Active	Production	WQFN (RTE) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7850
ADS7850IRTET.A	Active	Production	WQFN (RTE) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7850
ADS7850IRTET.B	Active	Production	WQFN (RTE) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7850
ADS8350IRTER	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8350
ADS8350IRTER.A	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8350
ADS8350IRTER.B	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8350
ADS8350IRTET	Active	Production	WQFN (RTE) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8350
ADS8350IRTET.A	Active	Production	WQFN (RTE) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8350
ADS8350IRTET.B	Active	Production	WQFN (RTE) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8350

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

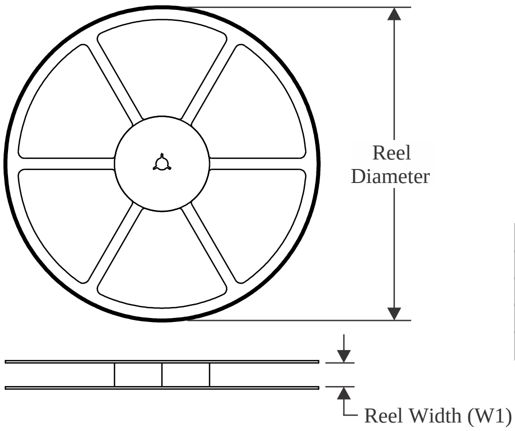
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

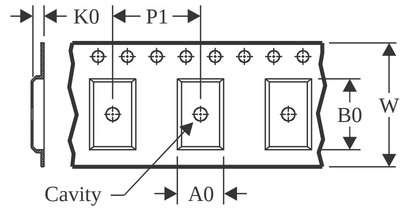
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

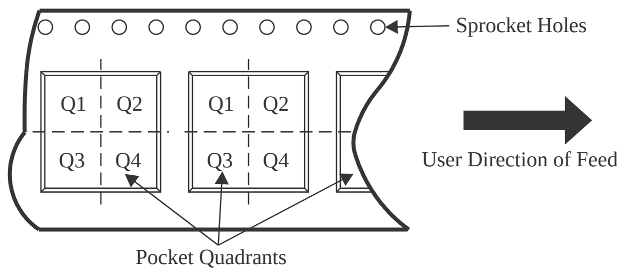


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

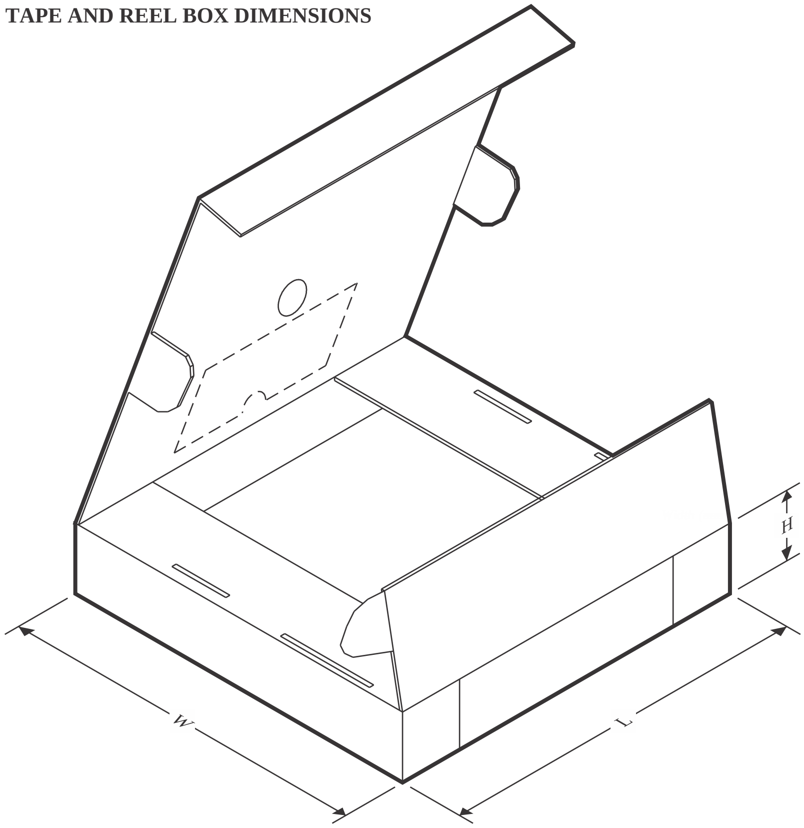
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7250IRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS7250IRTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS7850IRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS7850IRTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS8350IRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS8350IRTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

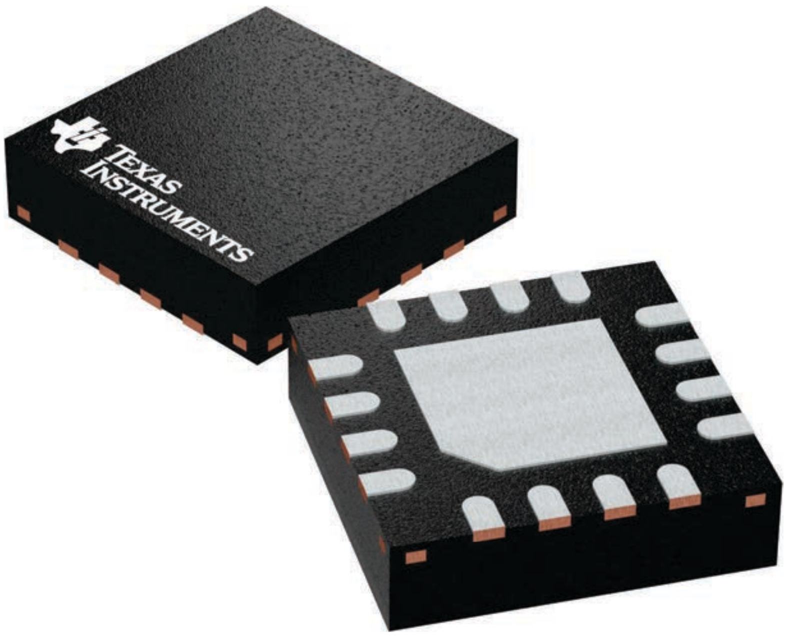
TAPE AND REEL BOX DIMENSIONS

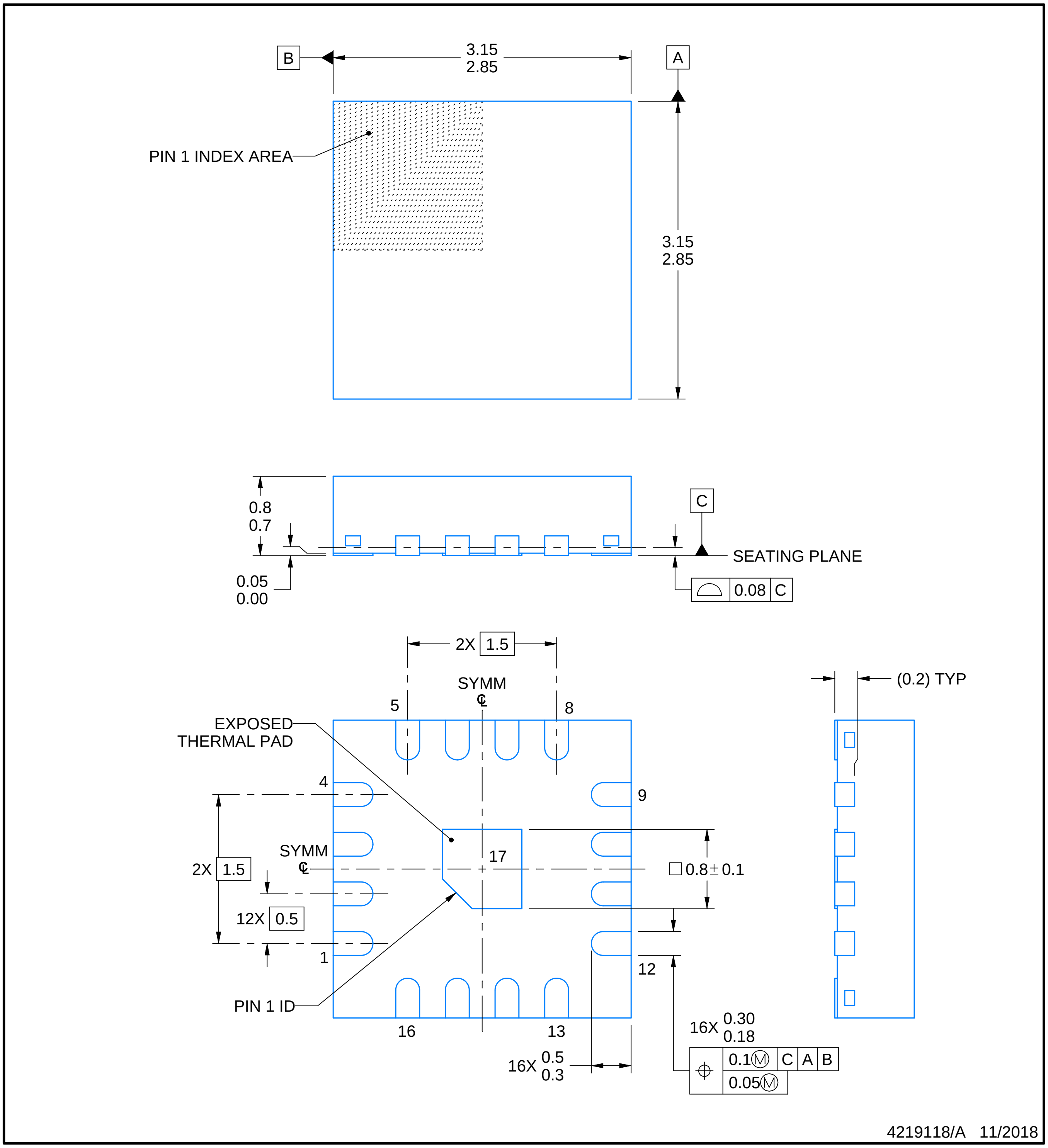


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7250IRTER	WQFN	RTE	16	3000	353.0	353.0	32.0
ADS7250IRTET	WQFN	RTE	16	250	213.0	191.0	35.0
ADS7850IRTER	WQFN	RTE	16	3000	353.0	353.0	32.0
ADS7850IRTET	WQFN	RTE	16	250	213.0	191.0	35.0
ADS8350IRTER	WQFN	RTE	16	3000	353.0	353.0	32.0
ADS8350IRTET	WQFN	RTE	16	250	213.0	191.0	35.0

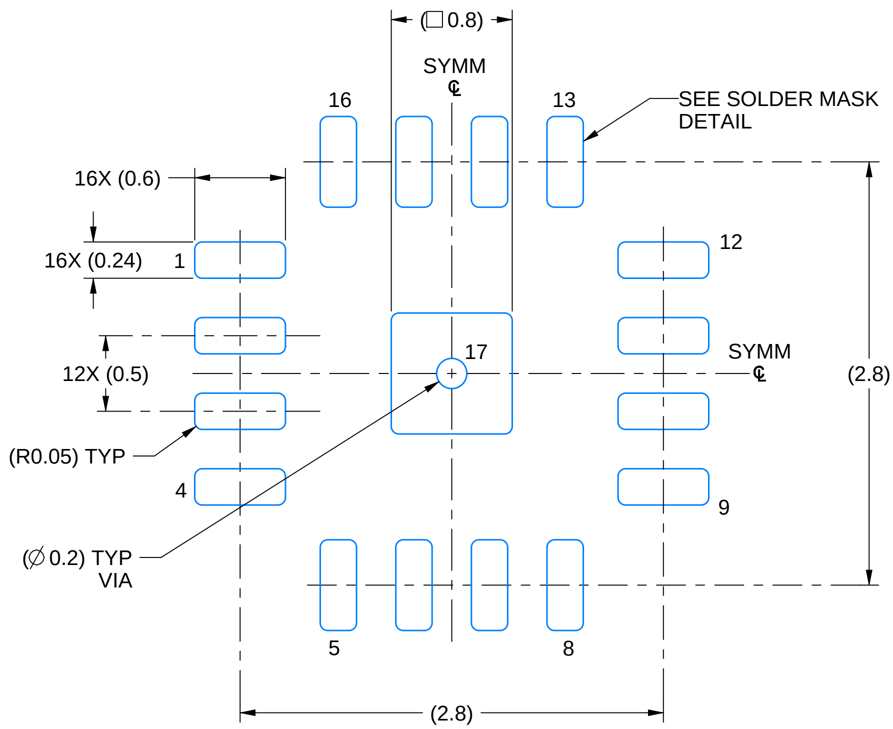
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



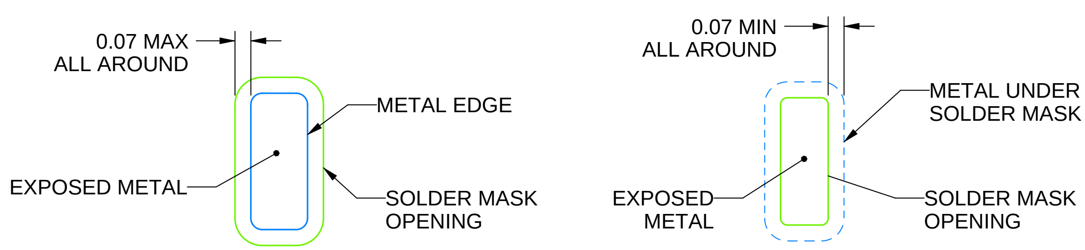


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON SOLDER MASK
DEFINED
(PREFERRED)

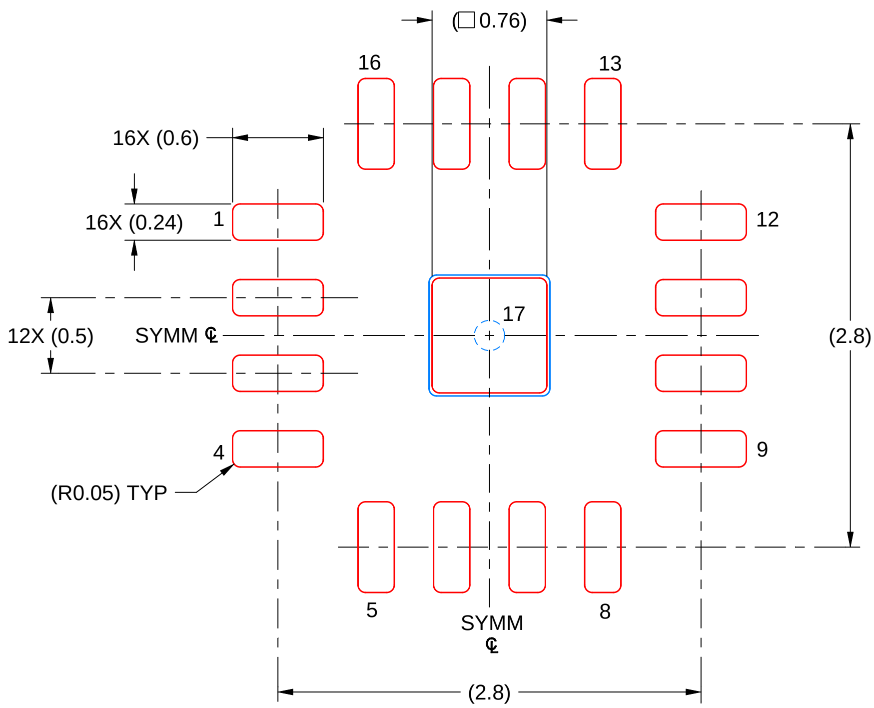
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4219118/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 17
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4219118/A 11/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、 TI の販売条件 、 TI の総合的な品質ガイドライン 、 ti.com または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。 TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。