AFEx3902-Q1 マルチスロープ・サーマル・フォールドバックおよび LUT ベース制御用、I²C および SPI 搭載のスマート・アナログ・フロント・エンド (AFE)

1 特長

- 車載アプリケーション用に AEC-Q100 認定済み：
  - 温度グレード 1：-40℃～+125℃、T_A
- マルチスロープ・サーマル・フォールドバック
  - 10 ビット A/D コンバータ (ADC) 入力
  - D/A コンバータ (DAC) 出力
    - 10 ビット (AFE53902-Q1)
    - 8 ビット (AFE43902-Q1)
  - デューティ・サイクル 7 ビットのパルス幅変調 (PWM) 出力
  - 不揮発性メモリ (NVM) からのスタンドアロン動作
  - ルックアップ・テーブル (LUT) ベースのパラメータ構成
  - サーミスタ用の区分線形化回路
- I²C または SPI を自動検出
  - V_{IH}：1.62V (V_{DD} = 5.5V の場合)
- VREF/MODE ピンにより、プログラミング・モードとスタンドアロン・モードのどちらかを選択
- ユーザーがプログラム可能な NVM
- 内部、外部、VDD の基準電圧
- 幅広い動作範囲
  - 電源：1.8V～5.5V
- 超小型パッケージ：16 ピン WQFN (3mm × 3mm)

2 アプリケーション

- 車載テール・ライト
- 車載ヘッドライト

3 概要

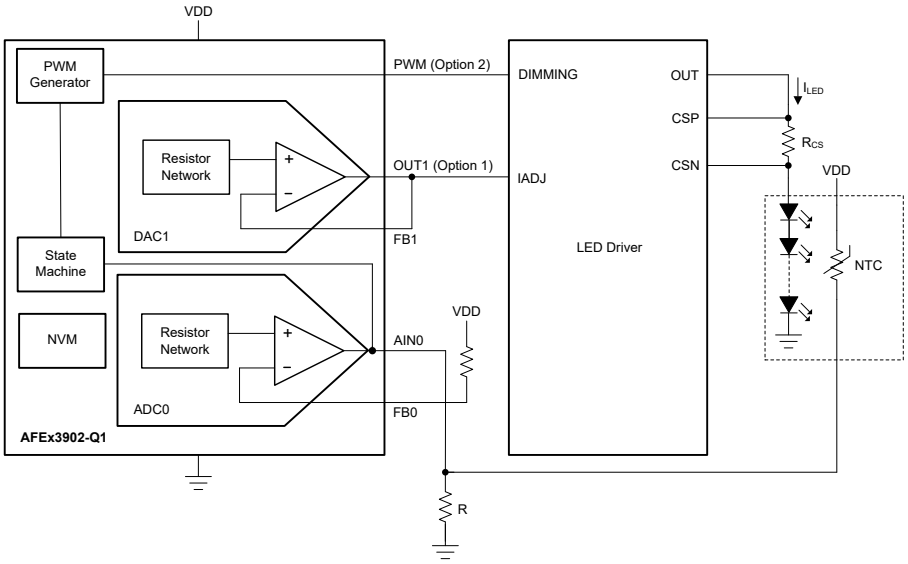
10 ビットの AFE53902-Q1 および 8 ビットの AFE43902-Q1 デバイス (AFEx3902-Q1) は、LED ライティングのマルチスロープ・サーマル・フォールドバックを目的としたデュアル・チャネルのスマート・アナログ・フロント・エンド (AFE) です。温度が上昇すると、LED ライトの出力が減少します。マルチスロープ・サーマル・フォールドバックにより、LED 温度をプログラムされたスレッショルドに制限しながら、温度変化に関係なく LED からの安定した光出力を維持できます。

AFEx3902-Q1 は、温度入力用の ADC と、出力として DAC または PWM ジェネレータを備えています。これらのデバイスは、マルチスロープのサーマル・フォールドバック・コントローラとしてあらかじめプログラムされたステート・マシンを内蔵しています。AFEx3902-Q1 は、車載用テール・ライトやヘッドライト、園芸用ライトのサーマル・フォールドバックに最適です。AFEx3902-Q1 は、NVM にプログラムされたパラメータとは独立して動作するため、プロセッサレス・アプリケーションや設計の再利用に適したスマート AFE を実現できます。これらのデバイスは、I²C と SPI を自動的に検出し、内部基準電圧を備えています。

製品情報

部品番号	分解能	パッケージ(1)
AFE53902-Q1	10 ビット	RTE (WQFN、16)
AFE43902-Q1	8 ビット	

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



AFEx3902-Q1 を使用したマルチスロープ・サーマル・フォールドバック

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4 Revision History

DATE	REVISION	NOTES
June 2023	*	Initial release

5 Pin Configuration and Functions

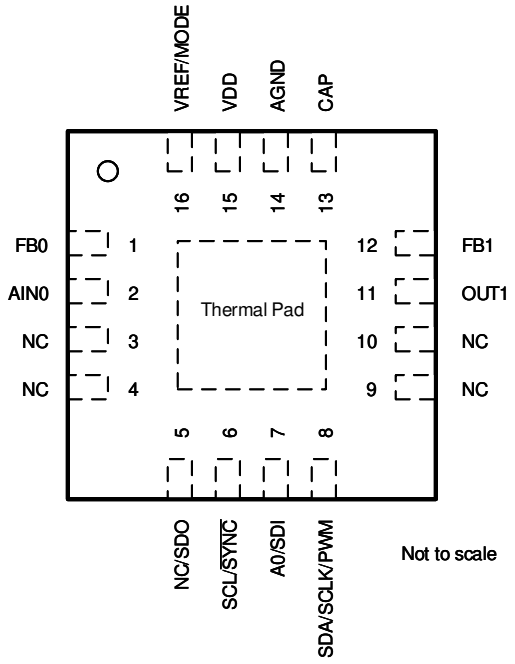


図 5-1. RTE Package, 16-pin WQFN (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	FB0	Input	Connect this pin to VDD with a pullup resistor.
2	AIN0	Input	Analog input for ADC0.
3	NC	—	Not connected.
4	NC	—	Not connected.
5	NC/SDO	Output	This pin is configurable as SDO. In SDO mode, connect this pin to the I/O voltage with an external pullup resistor.
6	SCL/$\overline{\text{SYNC}}$	Output	I^2C serial interface clock or SPI chip select input. Connect this pin to the I/O voltage using an external pullup resistor.
7	A0/SDI	Input	Address configuration input for I^2C or serial data input for SPI. For the A0 function, connect this pin to VDD, AGND, SDA, or SCL for address configuration. For the SDI function, this pin does not need to be pulled up or pulled down.
8	SDA/ SCLK/PWM	Input/Output	Bidirectional I^2C serial data bus or SPI clock input. Connect this pin to the I/O voltage using an external pullup resistor. This pin acts as the PWM output for multislope thermal foldback. Pull the MODE pin high to enable PWM output.
9	NC	—	Not connected.
10	NC	—	Not connected.
11	OUT1	Output	For voltage output, this pin is the analog output from DAC channel 0. In PWM output mode, keep this pin unconnected.
12	FB1	Input	For voltage output, this pin is the voltage feedback input for DAC channel 0. Connect this pin to OUT0 for closed-loop amplifier output. In PWM output mode, keep this pin unconnected.
13	CAP	Power	External bypass capacitor for the internal LDO. Connect a capacitor (approximately 1.5 µF) between CAP and AGND.
14	AGND	Ground	Ground reference point for all circuitry on the device.
15	VDD	Power	Supply voltage: 1.8 V to 5.5 V

表 5-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
16	VREF/ MODE	Input	External reference or interface mode select input. Connect a capacitor (approximately 0.1 µF) between VREF/MODE and AGND. Use a pullup resistor to VDD when the external reference is not used. Make sure that this pin does not ramp up before VDD. In case an external reference is used or when in interface select mode, make sure the reference ramps up after VDD. Pull this pin low to enable I^2C or SPI communication. Pull this pin high to enable PWM output.
Thermal Pad	Thermal Pad	Ground	Connect the thermal pad to AGND.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD}	Supply voltage, V_{DD} to AGND	–0.3	6	V
	Digital inputs to AGND	–0.3	V_{DD} + 0.3	V
	V_{FBX} to AGND	–0.3	V_{DD} + 0.3	V
	V_{OUTX} to AGND	–0.3	V_{DD} + 0.3	V
V_{REF}	External reference, V_{REF} to AGND	–0.3	V_{DD} + 0.3	V
	Current into any pin except the OUTx, VDD, and AGND pins	–10	10	mA
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD classification level 2		±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD classification level C4B	Corner pins (1, 4, 5, 8, 9, 12, 13, and 16)	±750	
			All pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Positive supply voltage to ground (AGND)	1.7		5.5	V
V_{REF}	External reference to ground (AGND)	1.7		V_{DD}	V
V_{IH}	Digital input high voltage, 1.7 V < V_{DD} ≤ 5.5 V	1.62			V
V_{IL}	Digital input low voltage			0.4	V
C_{CAP}	External capacitor on CAP pin	0.5		15	µF
T_A	Ambient temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		AFEx3902-Q1 RTE (WQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	24.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	24.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	8.7	°C/W

(1) For information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics application report.*

6.5 Electrical Characteristics: Voltage Output

minimum and maximum specifications at –40°C ≤ T_A ≤ +125°C and typical specifications at T_A = 25°C, 1.7 V ≤ V_{DD} ≤ 5.5 V, DAC reference tied to VDD, gain = 1 ×, DAC output pin (OUT) loaded with resistive load (R_L = 5 kΩ to AGND) and capacitive load (C_L = 200 pF to AGND), and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE						
	Resolution	AFE53902-Q1	10			Bits
		AFE43902-Q1	8			
INL	Integral nonlinearity(1)	AFE53902-Q1	–1.25		1.25	LSB
		AFE43902-Q1	–1		1	
DNL	Differential nonlinearity(1)		–1		1	LSB
	Zero-code error(2)	Code 0d into DAC, external reference, V_{DD} = 5.5 V		6	12	mV
		Code 0d into DAC, internal V_{REF}, gain = 4 ×, V_{DD} = 5.5 V		6	15	
	Zero-code error temperature coefficient(2)			±10		µV/°C
	Offset error(2)	1.7 V ≤ V_{DD} < 2.7 V, V_{FB} pin shorted to V_{OUT}, DAC code: 8d for 10-bit resolution, 2d for 8-bit resolution	–0.75	0.3	0.75	%FSR
		2.7 V ≤ V_{DD} ≤ 5.5 V, V_{FB} pin shorted to V_{OUT}, DAC code: 8d for 10-bit resolution, 2d for 8-bit resolution	–0.5	0.25	0.5	
	Offset-error temperature coefficient(2)	V_{FB} pin shorted to V_{OUT}, DAC code: 8d for 10-bit resolution, 2d for 8-bit resolution		±0.0003		%FSR/°C
	Gain error(2)	Between end-point codes: 8d to 1016d for 10-bit resolution, 2d to 254d for 8-bit resolution	–0.5	0.25	0.5	%FSR
	Gain-error temperature coefficient(2)	Between end-point codes: 8d to 1016d for 10-bit resolution, 2d to 254d for 8-bit resolution		±0.0008		%FSR/°C
	Full-scale error(2)	1.7 V ≤ V_{DD} < 2.7 V, DAC at full-scale	–1		1	%FSR
		2.7 V ≤ V_{DD} ≤ 5.5 V, DAC at full-scale, 10-bit resolution	–0.6		0.6	
		2.7 V ≤ V_{DD} ≤ 5.5 V, DAC at full-scale, 8-bit resolution	–0.65		0.65	
	Full-scale-error temperature coefficient(2)	DAC at full-scale		±0.0008		%FSR/°C
OUTPUT						
	Output voltage	Reference tied to V_{DD}	0		V_{DD}	V
C_L	Capacitive load(3)	R_L = infinite, phase margin = 30°			200	pF
		Phase margin = 30°			1000	
	Short-circuit current	V_{DD} = 1.7 V, full-scale output shorted to AGND or zero-scale output shorted to V_{DD}		15		mA
		V_{DD} = 2.7 V, full-scale output shorted to AGND or zero-scale output shorted to V_{DD}		50		
		V_{DD} = 5.5 V, full-scale output shorted to AGND or zero-scale output shorted to V_{DD}		60		
	Output-voltage headroom(3)	To V_{DD}, DAC output unloaded, internal reference = 1.21 V, V_{DD} ≥ 1.21 V × gain + 0.2 V	0.2			V
		To V_{DD} and to AGND, DAC output unloaded, external reference at V_{DD} (gain = 1 ×), the V_{REF} pin is not shorted to V_{DD}	0.8			%FSR
		To V_{DD} and to AGND, I_{LOAD} = 10 mA at V_{DD} = 5.5 V, I_{LOAD} = 3 mA at V_{DD} = 2.7 V, I_{LOAD} = 1 mA at V_{DD} = 1.8 V, external reference at V_{DD} (gain = 1 ×), the V_{REF} pin is not shorted to V_{DD}	10			

6.5 Electrical Characteristics: Voltage Output (continued)

minimum and maximum specifications at –40°C ≤ T_A ≤ +125°C and typical specifications at T_A = 25°C, 1.7 V ≤ V_{DD} ≤ 5.5 V, DAC reference tied to VDD, gain = 1 ×, DAC output pin (OUT) loaded with resistive load (R_L = 5 kΩ to AGND) and capacitive load (C_L = 200 pF to AGND), and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	V_{OUT} dc output impedance	DAC output enabled and DAC code = midscale, V_{DD} = 5.5 V, external reference mode		0.007		Ω
		DAC output enabled and DAC code = 8d, V_{DD} = 5.5 V, external reference mode		0.25		
		DAC output enabled and DAC code = 1016d, V_{DD} = 5.5 V, external reference mode		0.25		
Z_O	V_{FB} dc output impedance(4)	DAC output enabled, internal reference (gain = 1.5 × or 2 ×) or external reference at V_{DD} (gain = 1 ×), the V_{REF} pin is not shorted to V_{DD}	400	500	600	kΩ
		DAC output enabled, internal V_{REF}, gain = 3 × or 4 ×	325	400	485	
	Power supply rejection ratio (dc)	Internal V_{REF}, gain = 2 ×, DAC at midscale, V_{DD} = 5 V ±10%		0.25		mV/V
DYNAMIC PERFORMANCE						
t_{sett}	Output voltage settling time	1/4 to 3/4 scale and 3/4 to 1/4 scale settling to 10%FSR, V_{DD} = 5.5 V		20		µs
		1/4 to 3/4 scale and 3/4 to 1/4 scale settling to 10%FSR, V_{DD} = 5.5 V, internal V_{REF}, gain = 4 ×		25		
	Slew rate	V_{DD} = 5.5 V		0.3		V/µs
	Power-on glitch magnitude	At start-up, DAC output disabled		75		mV
		At start-up, DAC output disabled, R_L = 100 kΩ		200		
	Output-enable glitch magnitude	DAC output disabled to enabled, DAC registers at zero scale, R_L = 100 kΩ		250		mV
V_n	Output noise voltage (peak to peak)	f = 0.1 Hz to 10 Hz, DAC at midscale, V_{DD} = 5.5 V		50		μV_{PP}
		Internal V_{REF}, gain = 4 ×, f = 0.1 Hz to 10 Hz, DAC at midscale, V_{DD} = 5.5 V		90		
	Output noise density	f = 1 kHz, DAC at midscale, V_{DD} = 5.5 V		0.35		$\mu V/\sqrt{Hz}$
		Internal V_{REF}, gain = 4 ×, f = 1 kHz, DAC at midscale, V_{DD} = 5.5 V		0.9		
	Power supply rejection ratio (ac)(4)	Internal V_{REF}, gain = 4 ×, 200-mV 50-Hz or 60-Hz sine wave superimposed on power supply voltage, DAC at midscale		-68		dB
	Code change glitch impulse	±1 LSB change around midscale (including feedthrough)		10		nV-s
	Code change glitch impulse magnitude	±1 LSB change around midscale (including feedthrough)		15		mV

(1) Measured with DAC output unloaded. For external reference and internal reference V_{DD} ≥ 1.21 × gain + 0.2 V, between end-point codes: 8d to 1016d for 10-bit resolution and 2d to 254d for 8-bit resolution.
(2) Measured with DAC output unloaded.
(3) Specified by design and characterization, not production tested.
(4) Specified with 200-mV headroom with respect to reference value when internal reference is used.

6.6 Electrical Characteristics: ADC Input

minimum and maximum specifications at –40°C ≤ T_A ≤ +125°C and typical specifications at T_A = 25°C, 1.7 V ≤ V_{DD} ≤ 5.5 V, DAC reference tied to VDD, gain = 1 ×, and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE						
	Resolution		10			Bits
INL	Integral nonlinearity(1) (2)		–2		2	LSB
DNL	Differential nonlinearity(1) (2)		–1		1	LSB
	Offset error(1) (2) (3)	1.7 V ≤ V_{DD} < 2.7 V	–5	0	5	mV
		2.7 V ≤ V_{DD} ≤ 5.5 V	–5	0	5	
	Gain error(1) (2) (4)		–1		1	%FSR
INPUT						
	Input voltage range	External V_{REF} = V_{DD}, V_{FB} attenuation is 1	0		V_{DD}	V
DYNAMIC PERFORMANCE						
	Data rate(2)	ADC averaging setting is 4 samples	1406		2008	SPS
	Sampling capacitor			10		pF

(1) Measured with DAC output unloaded. For external reference and internal reference V_{DD} ≥ 1.21 x gain + 0.2 V, between end-point codes: 8d to 1016d for 10-bit resolution, 2d to 254d for 8-bit resolution.
(2) Specified by design and characterization, not production tested.
(3) Measured at DAC at mid-scale, comparator input at Hi-Z, and DAC operating with external reference.

6.7 Electrical Characteristics: General

minimum and maximum specifications at –40°C ≤ T_A ≤ +125°C and typical specifications at T_A = 25°C, 1.7 V ≤ V_{DD} ≤ 5.5 V, DAC reference tied to VDD, gain = 1 ×, and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL REFERENCE						
	Initial accuracy	T_A = 25°C for all measurements	1.1979	1.212	1.224	V
	Reference output temperature coefficient(1) (2)				60	ppm/°C
EXTERNAL REFERENCE						
	External reference input range		1.7		V_{DD}	V
	V_{REF} input impedance(1) (3)			192		kΩ-ch
EEPROM						
	Endurance(1)	–40°C ≤ T_A ≤ +85°C		20000		Cycles
		T_A = 125°C		1000		
	Data retention(1)			50		Years
	EEPROM programming write cycle time(1)				200	ms
	Device boot-up time(1)	Time taken from power valid (V_{DD} ≥ 1.7 V) to output valid state (output state as programmed in EEPROM), 0.5-µF capacitor on the CAP pin		5		ms
DIGITAL INPUTS						
	Digital feedthrough	Voltage output mode, DAC output static at midscale, fast mode plus, SCL toggling		20		nV-s
	Pin capacitance	Per pin		10		pF
POWER						
I_{DD}	Current flowing into VDD	DAC in sleep mode, internal reference powered down, external reference at 5.5 V			28	µA
	Current flowing into VDD(1)	DAC in sleep mode, internal reference enabled, additional current through internal reference		10		
		DAC and ADC channels enabled, internal reference enabled, additional current through internal reference per DAC or ADC channel		12.5		µA-ch
		Normal operation, state-machine enabled		1.05		mA
HIGH-IMPEDANCE OUTPUT						
I_{LEAK}	Current flowing into V_{OUTX} and V_{FBX}	DAC in Hi-Z output mode, 1.7 V ≤ V_{DD} ≤ 5.5 V		10		nA
		V_{DD} = 0 V, V_{OUT} ≤ 1.5 V, decoupling capacitor between V_{DD} and AGND = 0.1 µF		200		
		V_{DD} = 0 V, 1.5 V < V_{OUT} ≤ 5.5 V, decoupling capacitor between V_{DD} and AGND = 0.1 µF		500		
		100 kΩ between V_{DD} and AGND, V_{OUT} ≤ 1.25 V, series resistance of 10 kΩ at OUT pin		±2		µA

(1) Specified by design and characterization, not production tested.
(2) Measured at –40°C and +125°C and calculated the slope.
(3) Impedances for the DAC channels are connected in parallel.

6.8 Timing Requirements: I²C Standard Mode

all input signals are timed from VIL to 70% of $V_{pull-up}$, 1.7 V ≤ V_{DD} ≤ 5.5 V, –40°C ≤ T_A ≤ +125°C, and 1.7 V ≤ $V_{pull-up}$ ≤ V_{DD}

		MIN	NOM	MAX	UNIT
f_{SCLK}	SCL frequency			100	kHz
t_{BUF}	Bus free time between stop and start conditions	4.7			µs
t_{HDSTA}	Hold time after repeated start	4			µs
t_{SUSTA}	Repeated start setup time	4.7			µs
t_{SUSTO}	Stop condition setup time	4			µs
t_{HDDAT}	Data hold time	0			ns
t_{SUDAT}	Data setup time	250			ns
t_{LOW}	SCL clock low period	4700			ns
t_{HIGH}	SCL clock high period	4000			ns
t_F	Clock and data fall time			300	ns
t_R	Clock and data rise time			1000	ns
t_{VDDAT}	Data valid time, R = 360 Ω, C_{trace} = 23 pF, C_{probe} = 10 pF			3.45	µs
t_{VDACK}	Data valid acknowledge time, R = 360 Ω, C_{trace} = 23 pF, C_{probe} = 10 pF			3.45	µs

6.9 Timing Requirements: I²C Fast Mode

all input signals are timed from VIL to 70% of $V_{pull-up}$, 1.7 V ≤ V_{DD} ≤ 5.5 V, –40°C ≤ T_A ≤ +125°C, and 1.7 V ≤ $V_{pull-up}$ ≤ V_{DD}

		MIN	NOM	MAX	UNIT
f_{SCLK}	SCL frequency			400	kHz
t_{BUF}	Bus free time between stop and start conditions	1.3			µs
t_{HDSTA}	Hold time after repeated start	0.6			µs
t_{SUSTA}	Repeated start setup time	0.6			µs
t_{SUSTO}	Stop condition setup time	0.6			µs
t_{HDDAT}	Data hold time	0			ns
t_{SUDAT}	Data setup time	100			ns
t_{LOW}	SCL clock low period	1300			ns
t_{HIGH}	SCL clock high period	600			ns
t_F	Clock and data fall time			300	ns
t_R	Clock and data rise time			300	ns
t_{VDDAT}	Data valid time, R = 360 Ω, C_{trace} = 23 pF, C_{probe} = 10 pF			0.9	µs
t_{VDACK}	Data valid acknowledge time, R = 360 Ω, C_{trace} = 23 pF, C_{probe} = 10 pF			0.9	µs

6.10 Timing Requirements: I²C Fast Mode Plus

all input signals are timed from VIL to 70% of $V_{pull-up}$, 1.7 V ≤ V_{DD} ≤ 5.5 V, –40°C ≤ T_A ≤ +125°C, and 1.7 V ≤ $V_{pull-up}$ ≤ V_{DD}

		MIN	NOM	MAX	UNIT
f_{SCLK}	SCL frequency			1	MHz
t_{BUF}	Bus free time between stop and start conditions	0.5			µs
t_{HDSTA}	Hold time after repeated start	0.26			µs
t_{SUSTA}	Repeated start setup time	0.26			µs
t_{SUSTO}	Stop condition setup time	0.26			µs
t_{HDDAT}	Data hold time	0			ns
t_{SUDAT}	Data setup time	50			ns
t_{LOW}	SCL clock low period	0.5			µs
t_{HIGH}	SCL clock high period	0.26			µs
t_F	Clock and data fall time			120	ns
t_R	Clock and data rise time			120	ns
t_{VDDAT}	Data valid time, R = 360 Ω, C_{trace} = 23 pF, C_{probe} = 10 pF			0.45	µs
t_{VDACK}	Data valid acknowledge time, R = 360 Ω, C_{trace} = 23 pF, C_{probe} = 10 pF			0.45	µs

6.11 Timing Requirements: SPI Write Operation

all input signals are specified with $t_r = t_f$ = 1 V/ns (10% to 90% of V_{IO}) and timed from a voltage level of (VIL + VIH) / 2, 1.7 V ≤ V_{IO} ≤ 5.5 V, 1.7 V ≤ V_{DD} ≤ 5.5 V, and –40°C ≤ T_A ≤ +125°C

		MIN	NOM	MAX	UNIT
f_{SCLK}	Serial clock frequency			50	MHz
$t_{SCLKHIGH}$	SCLK high time	9			ns
$t_{SCLKLOW}$	SCLK low time	9			ns
t_{SDIS}	SDI setup time	8			ns
t_{SDIH}	SDI hold time	8			ns
t_{CSS}	$\overline{SYNC}$ to SCLK falling edge setup time	18			ns
t_{CSH}	SCLK falling edge to $\overline{SYNC}$ rising edge	10			ns
t_{CSHIGH}	$\overline{SYNC}$ high time	50			ns
$t_{DACWAIT}$	Sequential DAC update wait time (time between subsequent $\overline{SYNC}$ rising edges) for same channel	2			µs

6.12 Timing Requirements: SPI Read and Daisy Chain Operation (FSDO = 0)

all input signals are specified with $t_r = t_f$ = 1 V/ns (10% to 90% of V_{IO}) and timed from a voltage level of (VIL + VIH) / 2, 1.7 V ≤ V_{IO} ≤ 5.5 V, 1.7 V ≤ V_{DD} ≤ 5.5 V, –40°C ≤ T_A ≤ +125°C, and FSDO = 0

		MIN	NOM	MAX	UNIT
f_{SCLK}	Serial clock frequency			1.25	MHz
$t_{SCLKHIGH}$	SCLK high time	350			ns
$t_{SCLKLOW}$	SCLK low time	350			ns
t_{SDIS}	SDI setup time	8			ns
t_{SDIH}	SDI hold time	8			ns
t_{CSS}	$\overline{SYNC}$ to SCLK falling edge setup time	400			ns
t_{CSH}	SCLK falling edge to $\overline{SYNC}$ rising edge	400			ns
t_{CSHIGH}	$\overline{SYNC}$ high time	1			µs
t_{SDODLY}	SCLK rising edge to SDO falling edge, I_{OL} ≤ 5 mA, C_L = 20 pF.			300	ns

6.13 Timing Requirements: SPI Read and Daisy Chain Operation (FSDO = 1)

all input signals are specified with $t_r = t_f$ = 1 V/ns (10% to 90% of V_{IO}) and timed from a voltage level of (VIL + VIH) / 2, 1.7 V ≤ V_{IO} ≤ 5.5 V, 1.7 V ≤ V_{DD} ≤ 5.5 V, –40°C ≤ T_A ≤ +125°C, and FSDO = 1

		MIN	NOM	MAX	UNIT
f_{SCLK}	Serial clock frequency			2.5	MHz
$t_{SCLKHIGH}$	SCLK high time	175			ns
$t_{SCLKLOW}$	SCLK low time	175			ns
t_{SDIS}	SDI setup time	8			ns
t_{SDIH}	SDI hold time	8			ns
t_{CSS}	$\overline{SYNC}$ to SCLK falling edge setup time	300			ns
t_{CSH}	SCLK falling edge to $\overline{SYNC}$ rising edge	300			ns
t_{CSHIGH}	$\overline{SYNC}$ high time	1			µs
t_{SDODLY}	SCLK rising edge to SDO falling edge, I_{OL} ≤ 5 mA, C_L = 20 pF.			300	ns

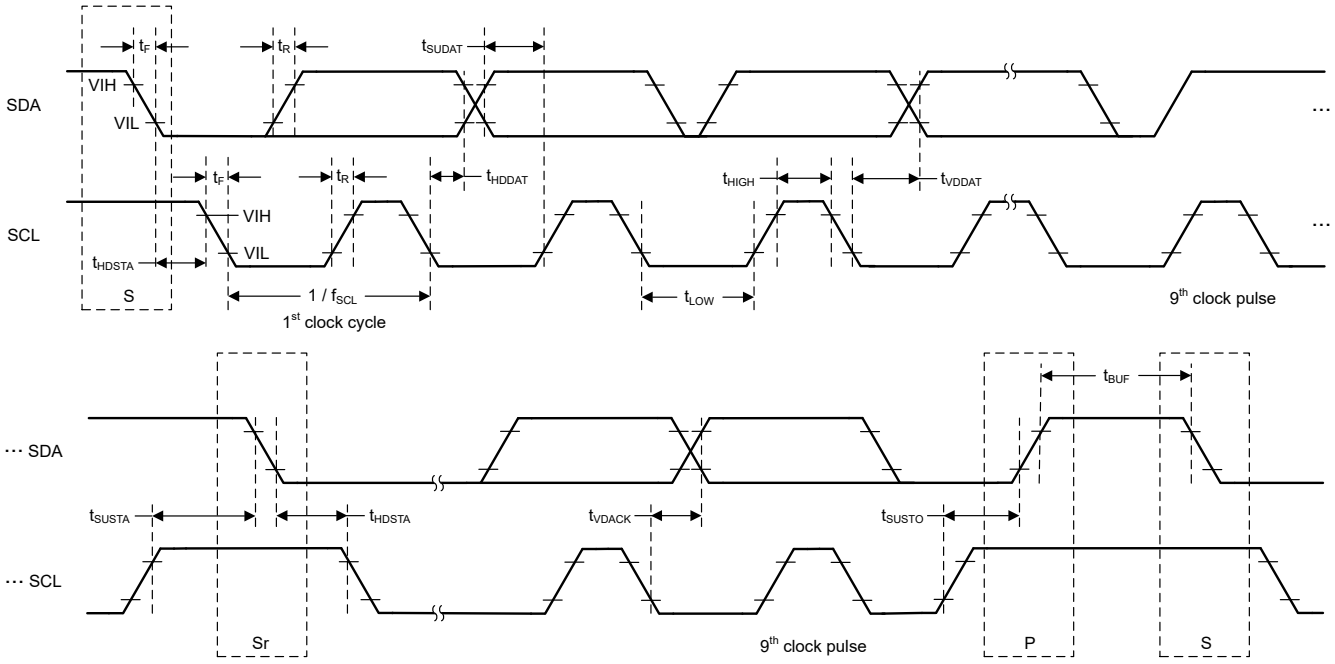
6.14 Timing Requirements: PWM Output

all input signals are timed from VIL to 70% of $V_{pull-up}$, 1.7 V ≤ V_{DD} ≤ 5.5, –40°C ≤ T_A ≤ +125°C, and 1.7 V ≤ $V_{pull-up}$ ≤ V_{DD}

		MIN	NOM	MAX	UNIT
f_{PWMOUT}	PWM frequency(1)	0.218		48.828	kHz
t_{PWMOHI}	PWM high time	1			µs
t_{PWMOLO}	PWM low time	1			µs
$t_{PWMODTY}$	PWM duty cycle	0.78		98.44	%

(1) The frequency range does not account for the internal oscillator frequency error.

6.15 Timing Diagrams



S: Start bit, **Sr**: Repeated start bit, **P**: Stop bit

図 6-1. I²C Timing Diagram

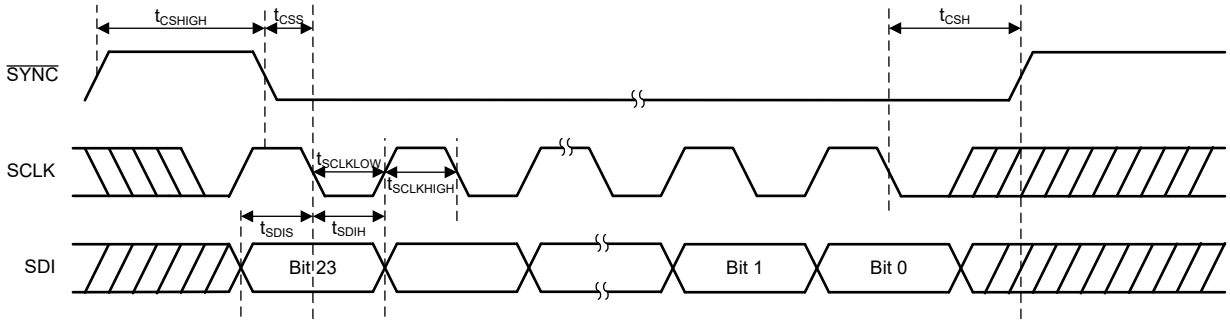


図 6-2. SPI Write Timing Diagram

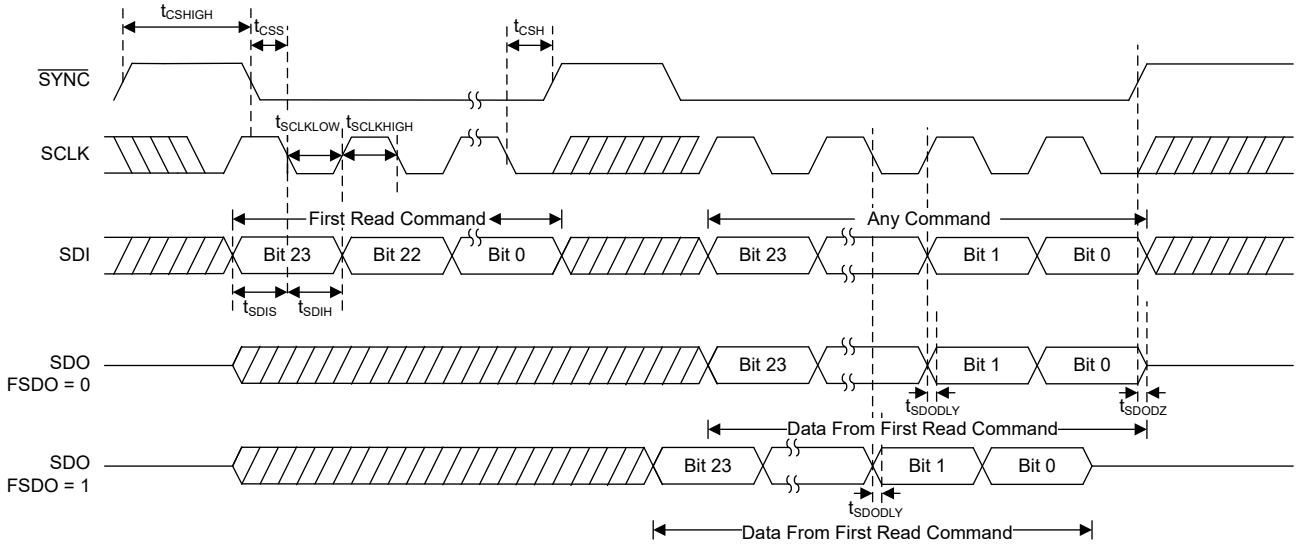


図 6-3. SPI Read Timing Diagram

6.16 Typical Characteristics: Voltage Output

at T_A = 25°C, V_{DD} = 5.5 V, external reference = 5.5 V, gain = 1 ×, and DAC outputs unloaded (unless otherwise noted)

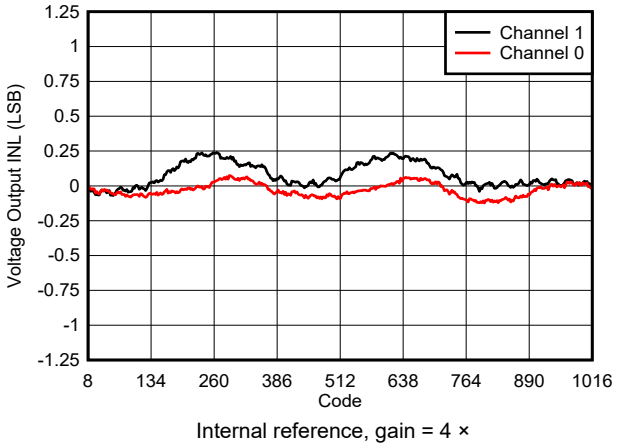


図 6-4. Voltage Output INL vs Digital Input Code

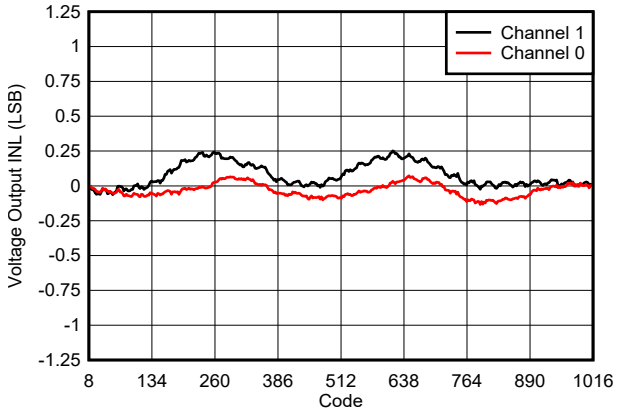


図 6-5. Voltage Output INL vs Digital Input Code

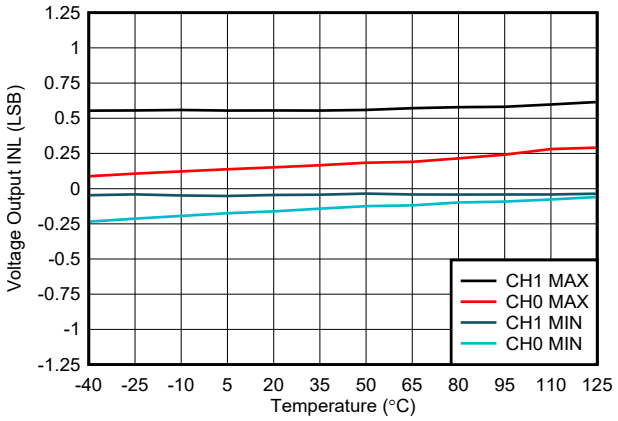


図 6-6. Voltage Output INL vs Temperature

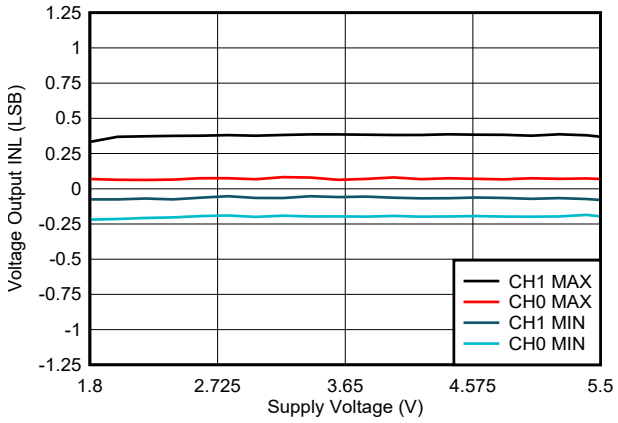


図 6-7. Voltage Output INL vs Supply Voltage

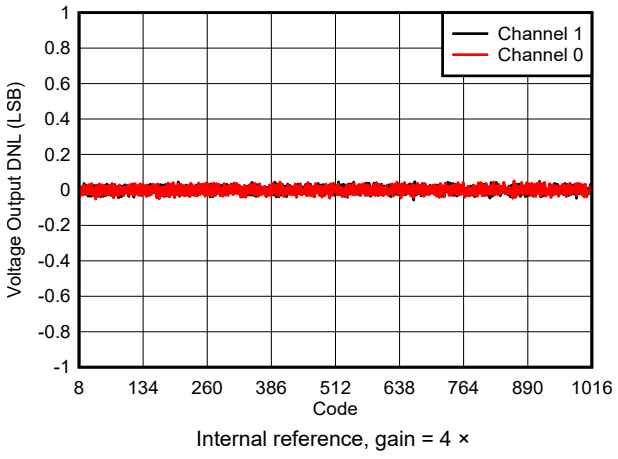


図 6-8. Voltage Output DNL vs Digital Input Code

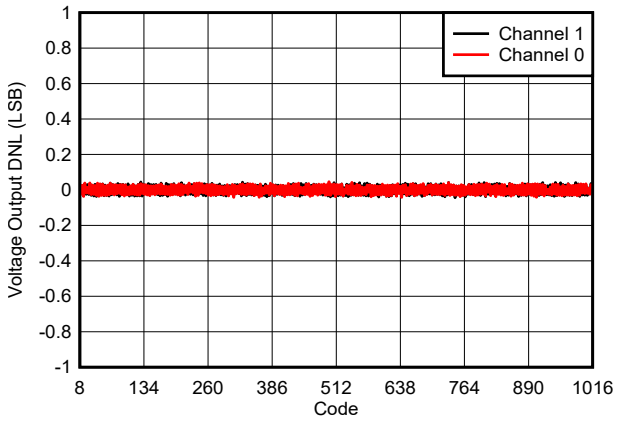


図 6-9. Voltage Output DNL vs Digital Input Code

6.16 Typical Characteristics: Voltage Output (continued)

at T_A = 25°C, V_{DD} = 5.5 V, external reference = 5.5 V, gain = 1 ×, and DAC outputs unloaded (unless otherwise noted)

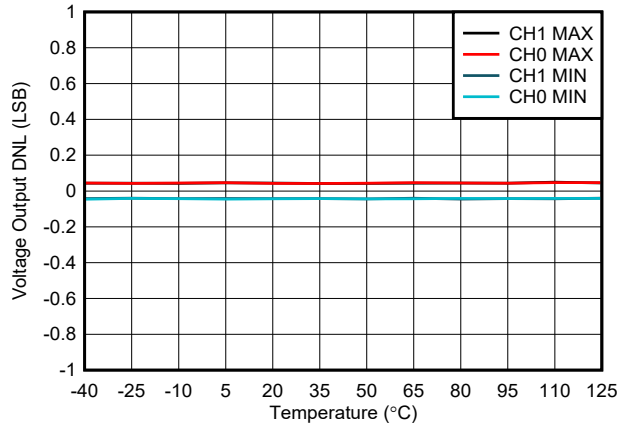


図 6-10. Voltage Output DNL vs Temperature

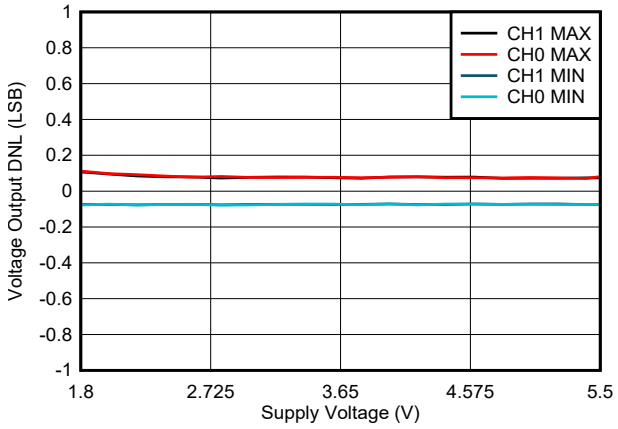
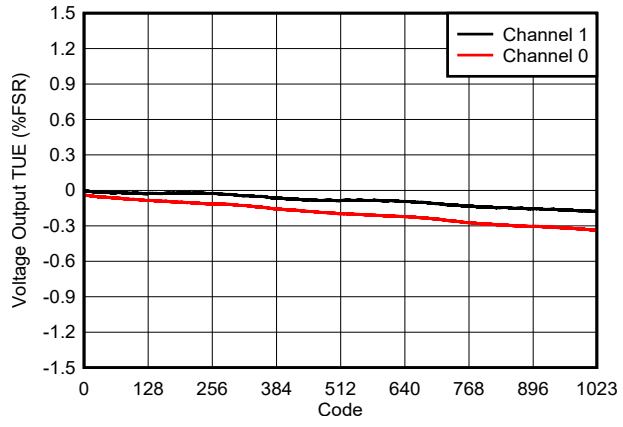


図 6-11. Voltage Output DNL vs Supply Voltage



Internal reference, gain = 4 ×

図 6-12. Voltage Output TUE vs Digital Input Code

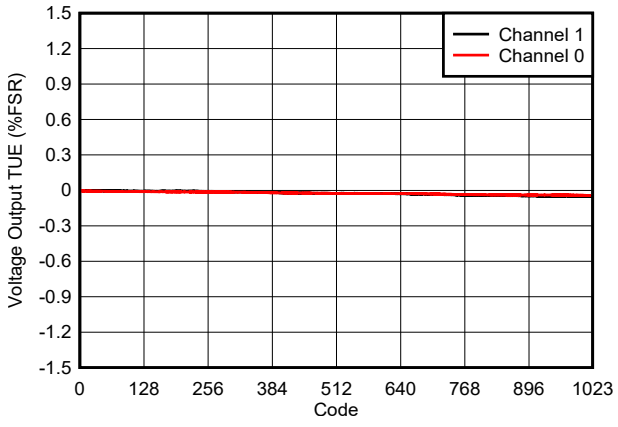
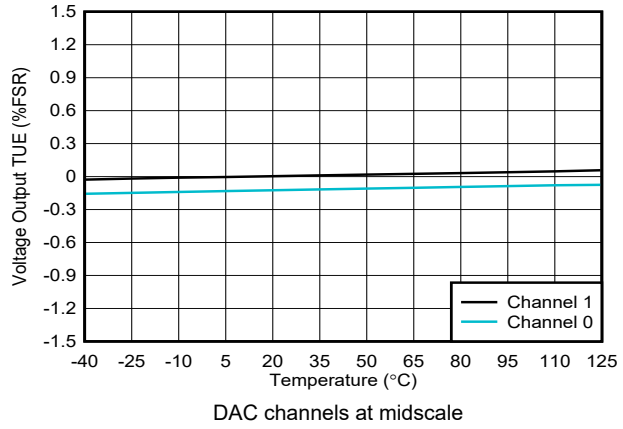
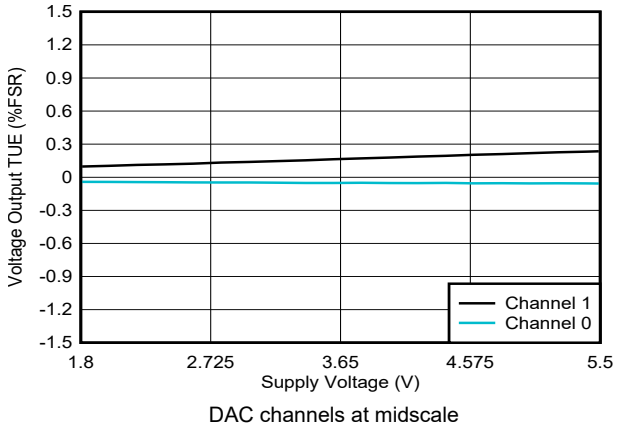


図 6-13. Voltage Output TUE vs Digital Input Code



DAC channels at midscale

図 6-14. Voltage Output TUE vs Temperature



DAC channels at midscale

図 6-15. Voltage Output TUE vs Supply Voltage

6.16 Typical Characteristics: Voltage Output (continued)

at T_A = 25°C, V_{DD} = 5.5 V, external reference = 5.5 V, gain = 1 ×, and DAC outputs unloaded (unless otherwise noted)

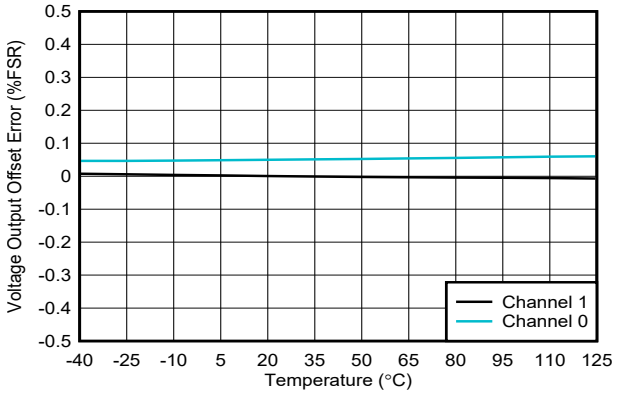


図 6-16. Voltage Output Offset Error vs Temperature

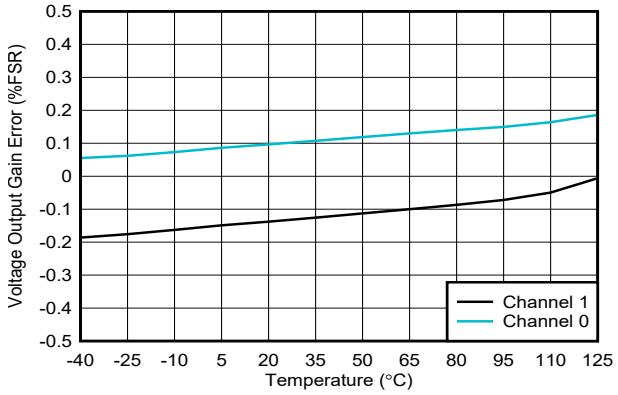


図 6-17. Voltage Output Gain Error vs Temperature

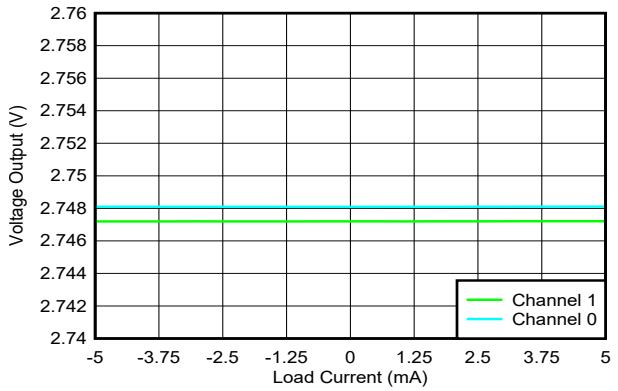


図 6-18. Voltage Output vs Load Current

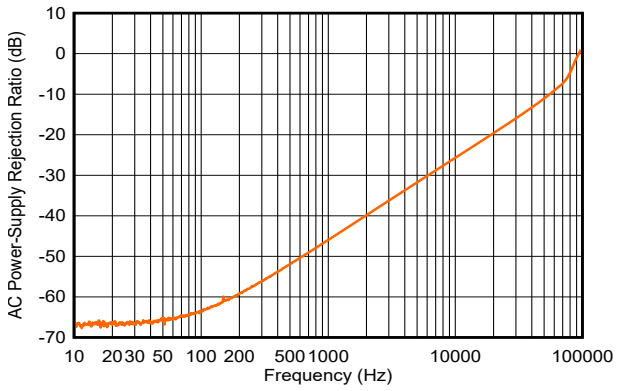


図 6-19. Voltage Output AC PSRR vs Frequency

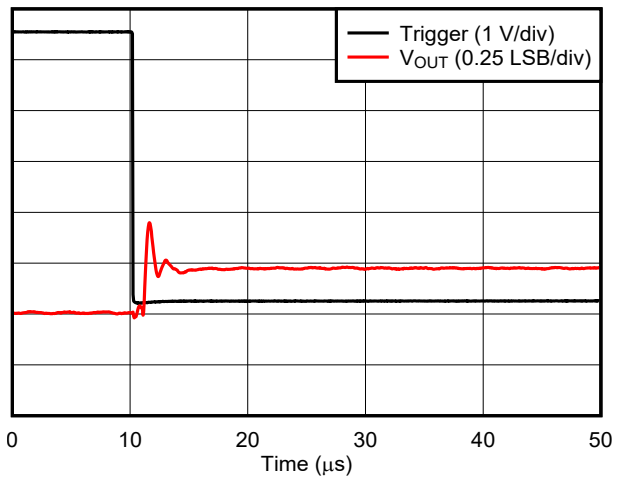


図 6-20. Voltage Output Code-to-Code Glitch - Rising Edge

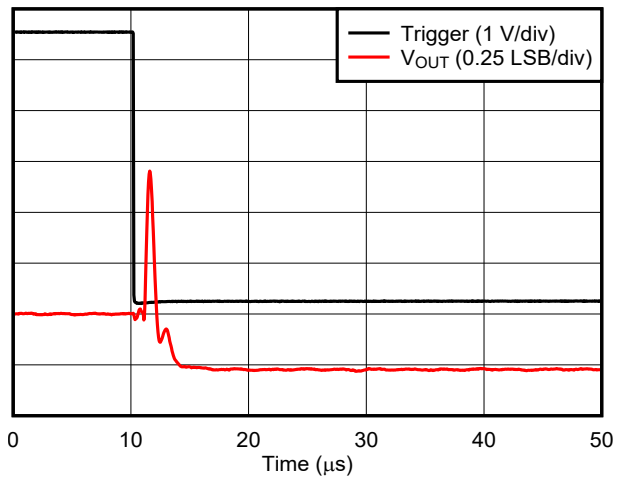
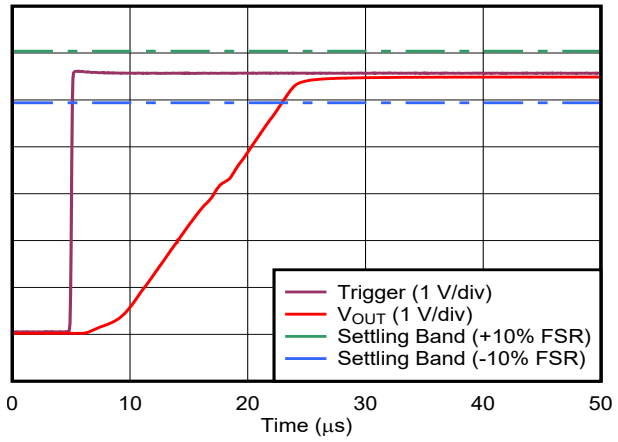


図 6-21. Voltage Output Code-to-Code Glitch - Falling Edge

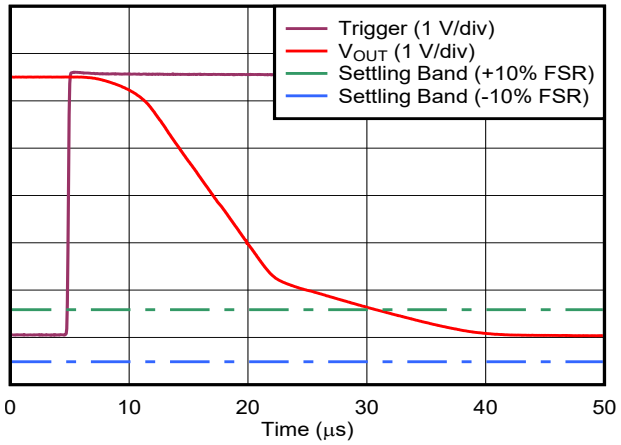
6.16 Typical Characteristics: Voltage Output (continued)

at T_A = 25°C, V_{DD} = 5.5 V, external reference = 5.5 V, gain = 1 ×, and DAC outputs unloaded (unless otherwise noted)



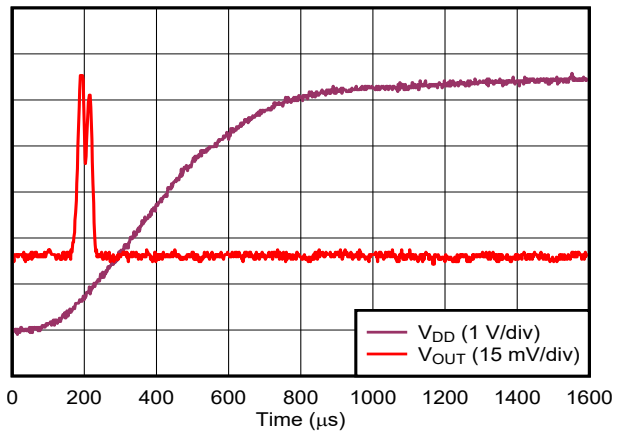
Zero scale to full scale swing

図 6-22. Voltage Output Setting Time - Rising Edge



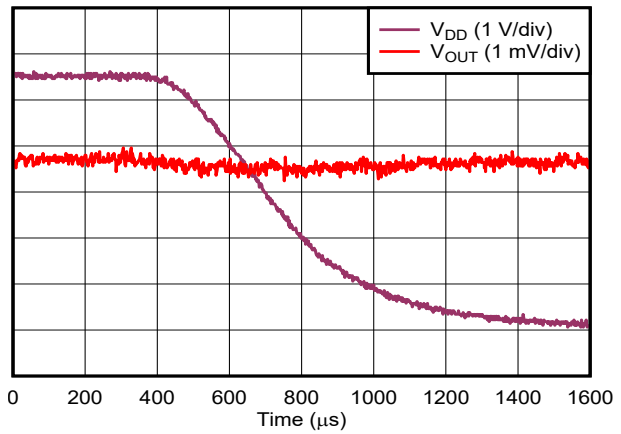
Full scale to zero scale swing

図 6-23. Voltage Output Setting Time - Falling Edge



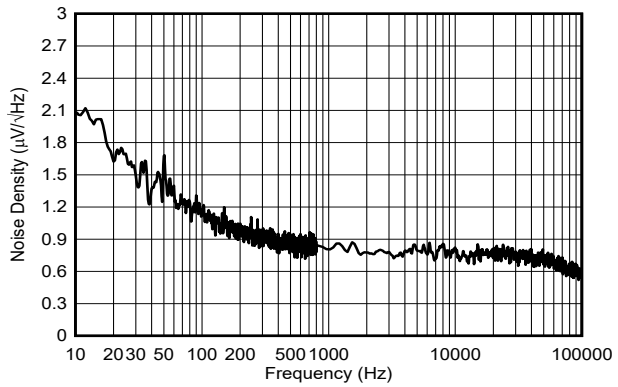
DAC in Hi-Z power-down mode

図 6-24. Voltage Output Power-On Glitch



DAC at zero scale

図 6-25. Voltage Output Power-Off Glitch



Internal reference, gain = 4 ×

図 6-26. Voltage Output Noise Density

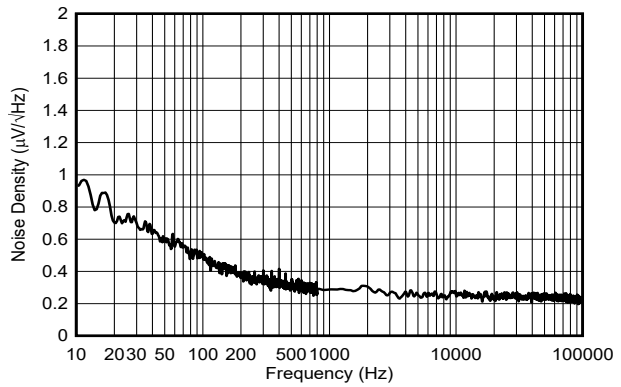
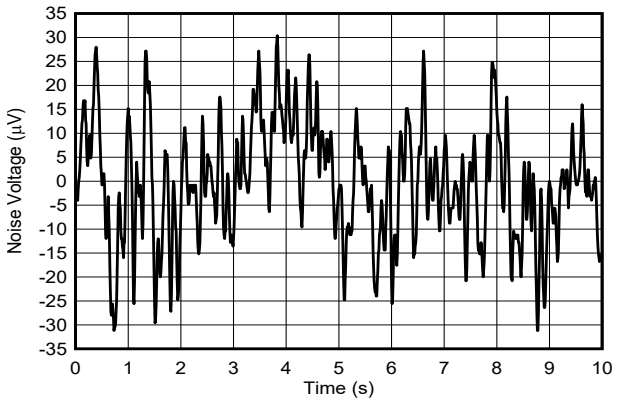


図 6-27. Voltage Output Noise Density

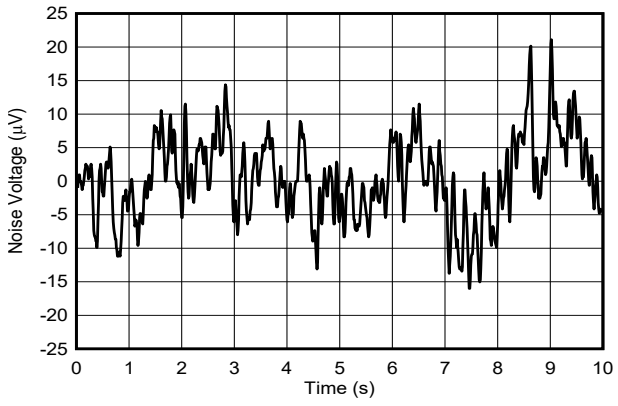
6.16 Typical Characteristics: Voltage Output (continued)

at T_A = 25°C, V_{DD} = 5.5 V, external reference = 5.5 V, gain = 1 ×, and DAC outputs unloaded (unless otherwise noted)



Internal reference, gain = 4x, f = 0.1 Hz to 10 Hz

図 6-28. Voltage Output Flicker Noise



f = 0.1 Hz to 10 Hz

図 6-29. Voltage Output Flicker Noise

6.17 Typical Characteristics: ADC

at T_A = 25°C, V_{DD} = 5.5 V, external reference = 5.5 V, gain = 1 ×, (unless otherwise noted)

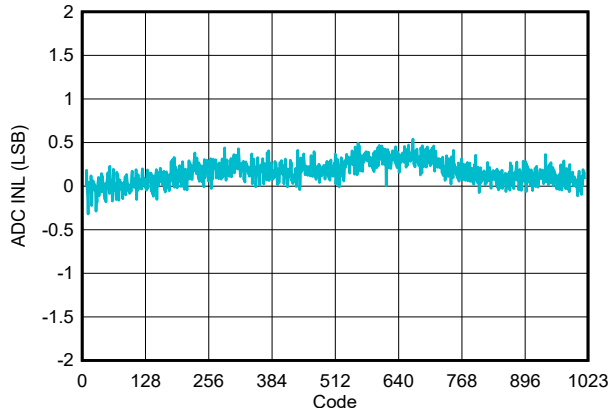


図 6-30. ADC INL vs Digital Output Code

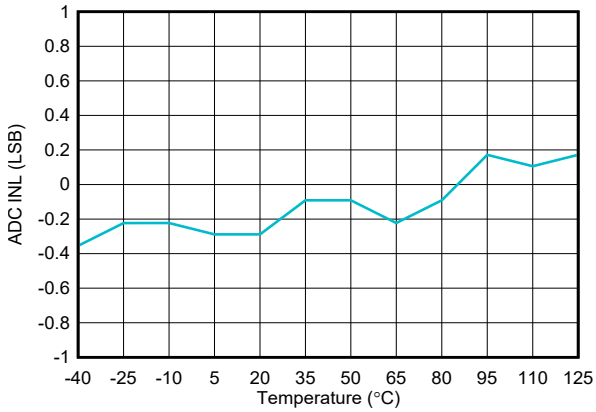


図 6-31. ADC INL vs Temperature

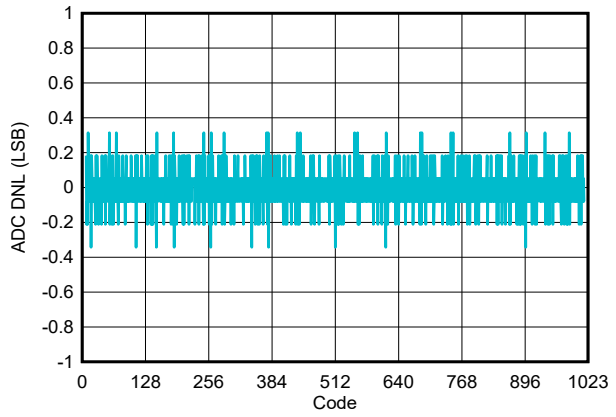


図 6-32. ADC DNL vs Digital Output Code

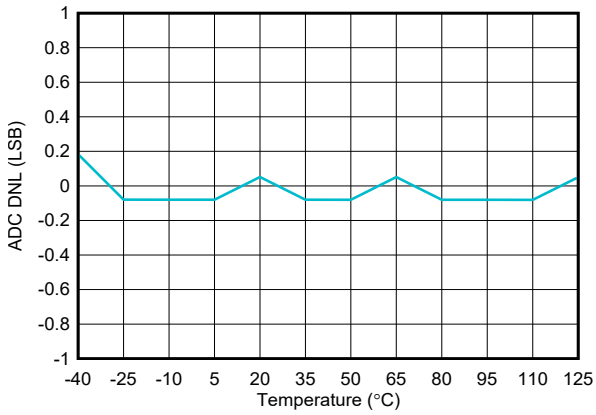


図 6-33. ADC DNL vs Temperature

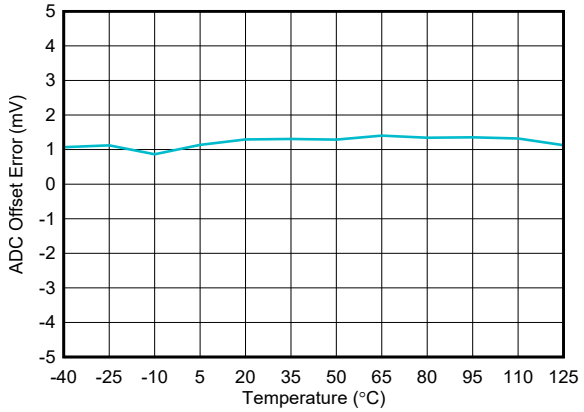


図 6-34. ADC Offset Error vs Temperature

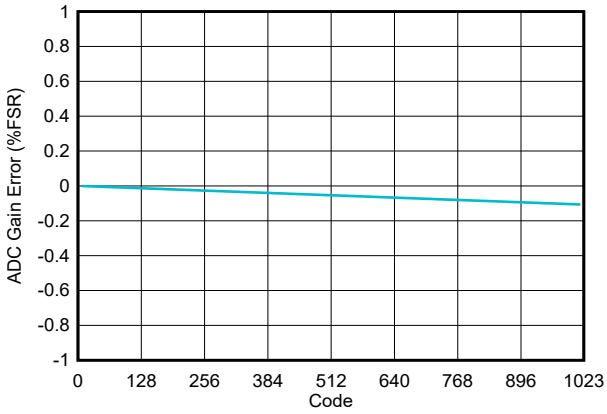


図 6-35. ADC Gain Error vs Digital Output Code

6.17 Typical Characteristics: ADC (continued)

at T_A = 25°C, V_{DD} = 5.5 V, external reference = 5.5 V, gain = 1 ×, (unless otherwise noted)

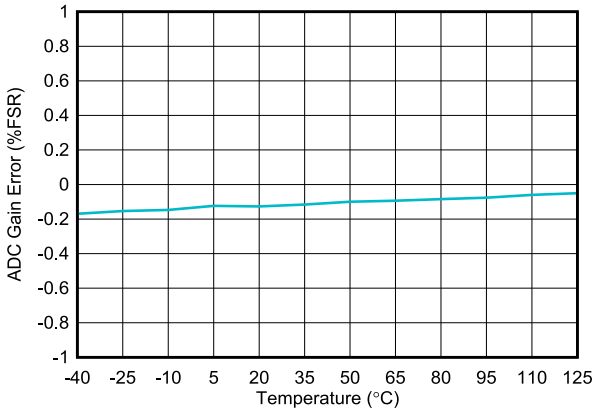


図 6-36. ADC Gain Error vs Temperature

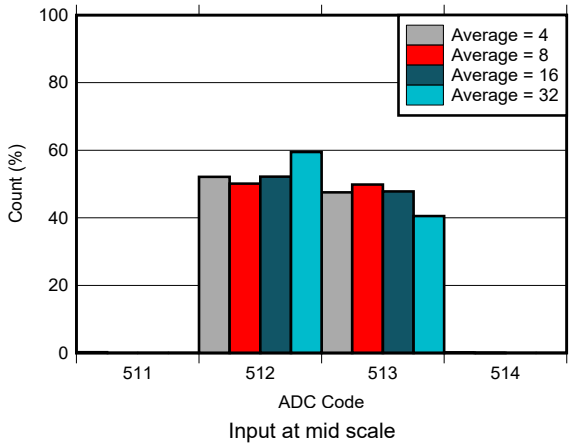


図 6-37. ADC Count vs Digital Output Code

6.18 Typical Characteristics: General

at T_A = 25°C, V_{DD} = 5.5 V, and DAC outputs unloaded (unless otherwise noted)

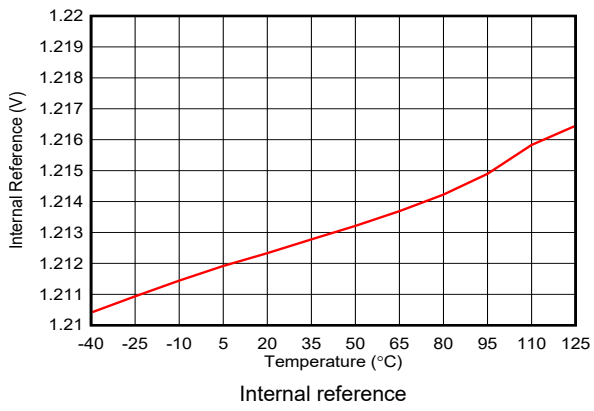


図 6-38. Internal Reference vs Temperature

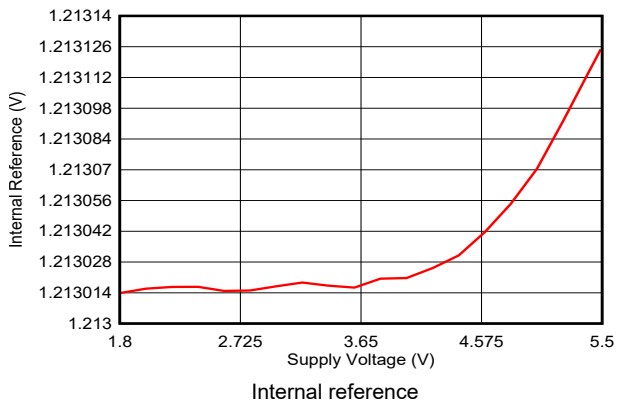


図 6-39. Internal Reference vs Supply Voltage

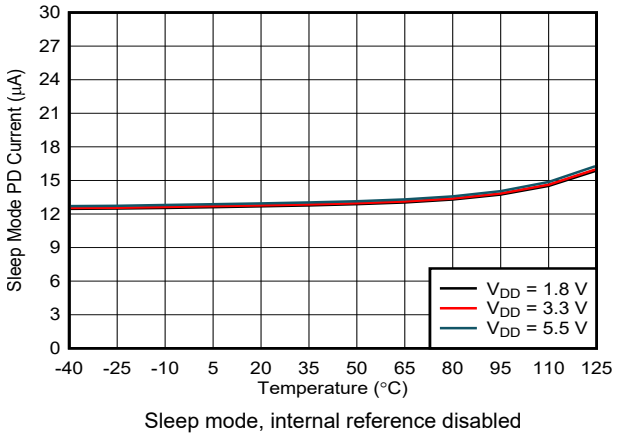


図 6-40. Power-Down Current vs Temperature

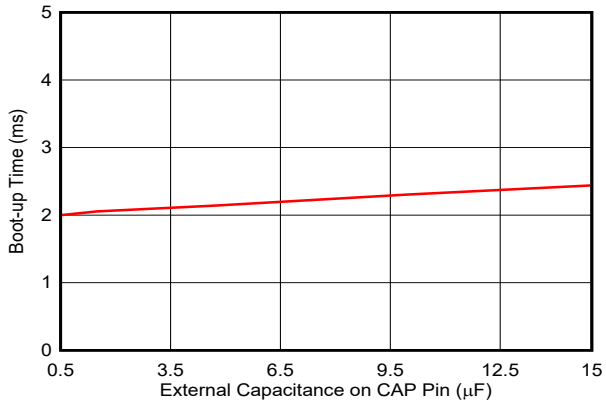


図 6-41. Boot-Up Time vs Capacitance on CAP pin

7 Detailed Description

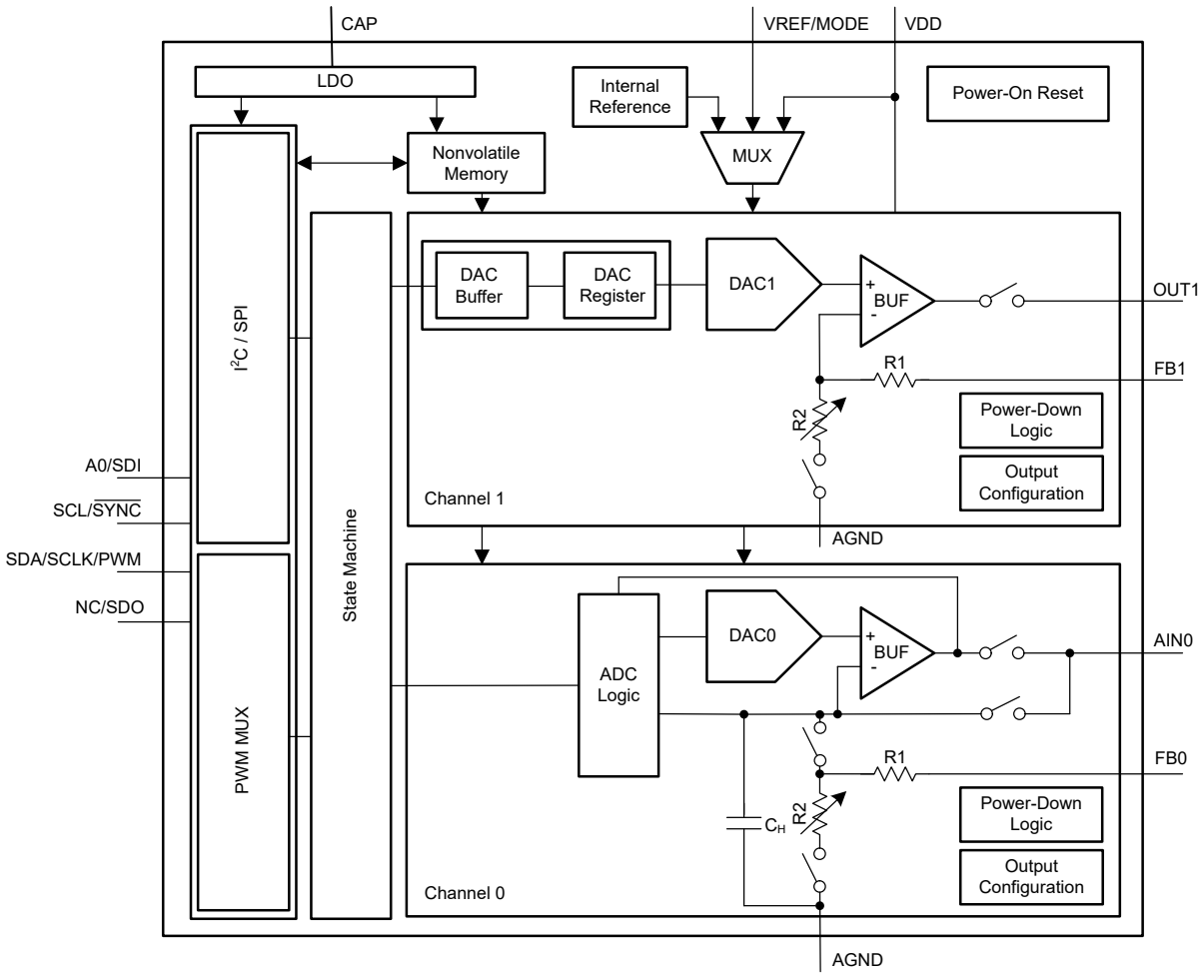
7.1 Overview

The 10-bit AFE53902-Q1 and the 8-bit AFE43902-Q1 devices (AFEx3902-Q1) are dual-channel smart analog front ends (AFE) with buffered voltage-output DAC, PWM, and ADC. The SDA/SCLK pin is repurposed as the PWM output when the VREF/MODE pin is held high.

The AFEx3902-Q1 provide a preprogrammed state machine that functions as a multislope thermal foldback controller. These devices contain nonvolatile memory (NVM), an internal reference and automatically detect I^2C and SPI. The devices support Hi-Z power-down modes by default, which can be configured to 10 kΩ-AGND or 100 kΩ-AGND using the NVM. The AFEx3902-Q1 have a power-on-reset (POR) circuit that makes sure all the registers start with default or user-programmed settings using NVM. The AFEx3902-Q1 operate with either an internal reference, external reference, or with power supply as the reference, and provide a full-scale output of 1.8 V to 5.5 V.

The AFEx3902-Q1 support I^2C standard mode (100Kbps), fast mode (400Kbps), and fast mode plus (1Mbps). The I^2C interface can be configured with four device addresses using the A0 pin. The SPI mode supports a three-wire interface by default, with up to a 25-MHz SCLK input. The NC/SDO pin can be configured as SDO in the NVM for SPI read capability. The AFEx3902-Q1 are designed for thermal foldback of LED lighting in automotive rear lights and headlights, horticulture lighting, and other lighting applications. The state machine and NVM enable *processor-less* operation. As a result of the *smart* feature set, the AFEx3902-Q1 is called a smart AFE.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Smart Analog Front End (AFE) Architecture

The AFEx3902-Q1 smart analog front end (AFE) consist of a 10-bit analog-to-digital converter (ADC) input, a 10-bit (AFE53902-Q1) or 8-bit (AFE43902-Q1) digital-to-analog converter (DAC) output, and a 7-bit pulse-width modulation (PWM) output. The ADC uses a successive-approximation register (SAR) architecture. The DAC uses a string architecture followed by a voltage-output amplifier. The PWM output is multiplexed with one of the digital interface pins. セクション 7.2 shows the smart AFE architecture within the block diagram, which operates from a 1.8-V to 5.5-V power supply. The device has an internal voltage reference of 1.21 V. There is an option to select an external reference on the VREF/MODE pin, or use the power supply as a reference. The ADC and DAC use one of these three reference options. Both the voltage-output and current-output modes support multiple programmable output ranges.

The AFEx3902-Q1 feature a preprogrammed state machine supporting multislope thermal foldback operation. 図 7-1 shows the digital architecture of the smart AFE with the interconnections between different functional blocks. This state machine allows the user to program the coefficients and input-output parameters. The state machine can be disabled by writing to the STATE-MACHINE-CONFIG0 register. The user configurations are stored in the NVM and the state machine can be operated in standalone mode without interfacing to a processor (*processor-less* operation)

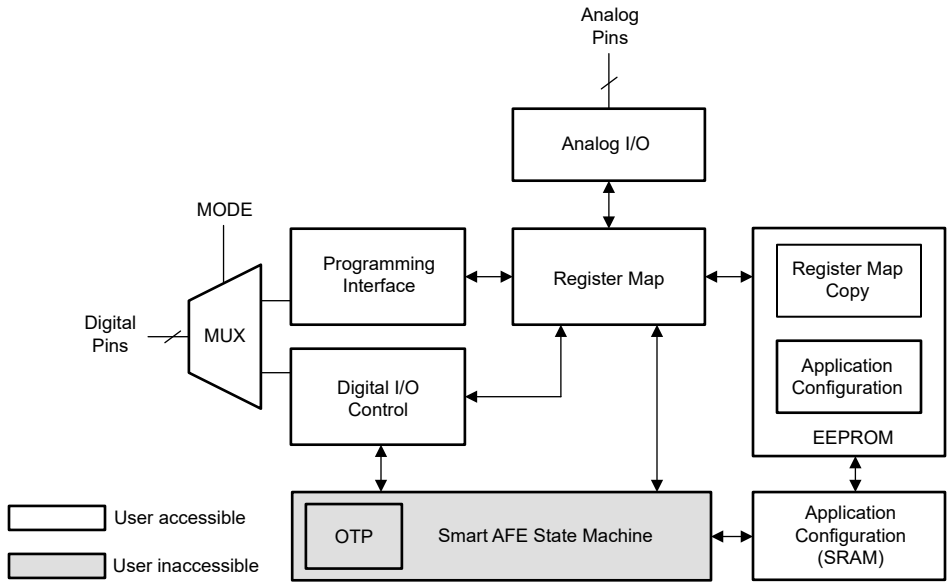


図 7-1. Smart AFE Architecture

7.3.2 Programming Interface

The AFEx3902-Q1 have five digital I/O pins that control I^2C, SPI, PWM, and mode selection. The VREF/MODE pin must be at logic low to enable the programming interface. These devices automatically detect I^2C and SPI protocols at the first successful communication after power-on, and then connect to the detected interface. After an interface protocol is connected, any change in the protocol is ignored. The I^2C interface uses the A0 pin to select from among four address options. The SPI is a three-wire interface by default. No readback capability is available in three-wire SPI mode. The NC/SDO pin can be configured as the SDO function in the register map and then programmed into the NVM. With the NC/SDO pin acting as SDO, the SPI works as a four-wire interface. The SPI readback mode is slower than the write mode. The programming interface pins are:

- I^2C: SCL, SDA, A0
- SPI: SCLK, SDI, $\overline{\text{SYNC}}$, NC/SDO

All the digital pins are open drain when used as outputs. Therefore, all the output pins must be pulled up to the desired I/O voltage using external resistors.

7.3.3 Nonvolatile Memory (NVM)

The AFEx3902-Q1 contain nonvolatile memory (NVM) bits. These memory bits are user programmable and erasable, and retain set values in the absence of a power supply. The highlighted gray cells in the *Register Map* show all the register bits that can be stored in the NVM by setting NVM-PROG = 1 in the COMMON-TRIGGER register. The NVM-PROG bit autoresets. The NVM-BUSY bit in the GENERAL-STATUS register is set to 1 by the device when an NVM write or reload operation is ongoing. During this time, the device blocks all read and write operations from and to the device. The NVM-BUSY bit is set to 0 after the write or reload operation is complete; at this point, all read and write operations from and to the device are allowed. The default value for all the registers in the AFEx3902-Q1 is loaded from NVM as soon as a POR event is issued.

The AFEx3902-Q1 also implements a NVM-RELOAD bit in the COMMON-TRIGGER register. Set this bit to 1 for the device to start an NVM-reload operation. The NVM-reload operation overwrites the register map with the stored data from the NVM. After completion, the device autoresets this bit to 0. During the NVM-RELOAD operation, the NVM-BUSY bit is set to 1.

7.3.3.1 NVM Cyclic Redundancy Check (CRC)

The AFEx3902-Q1 implements a cyclic redundancy check (CRC) feature for the NVM to make sure that the data stored in the NVM is uncorrupted. There are two types of CRC alarm bits implemented in the AFEx3902-Q1:

- NVM-CRC-FAIL-USER
- NVM-CRC-FAIL-INT

The NVM-CRC-FAIL-USER bit indicates the status of user-programmable NVM bits, and the NVM-CRC-FAIL-INT bit indicates the status of internal NVM bits. The CRC feature is implemented by storing a 16-bit CRC (CRC-16-CCITT) along with the NVM data each time the NVM program operation (write or reload) is performed and during the device boot up. The device reads the NVM data and validates the data with the stored CRC. The CRC alarm bits (NVM-CRC-FAIL-USER and NVM-CRC-FAIL-INT in the GENERAL-STATUS register) report any errors after the data are read from the device NVM. The alarm bits are set only at boot up.

7.3.3.1.1 NVM-CRC-FAIL-USER Bit

A logic 1 on NVM-CRC-FAIL-USER bit indicates that the user-programmable NVM data are corrupt. During this condition, all registers in the DAC are initialized with factory reset values, and any DAC registers can be written to or read from. To reset the alarm bits to 0, issue a software reset (see *セクション 7.3.5*) command, or cycle power to the DAC. A software reset or power-cycle also reloads the user-programmable NVM bits. In case the failure persists, reprogram the NVM.

7.3.3.1.2 NVM-CRC-FAIL-INT Bit

A logic 1 on NVM-CRC-FAIL-INT bit indicates that the internal NVM data are corrupt. During this condition, all registers in the DAC are initialized with factory reset values, and any DAC registers can be written to or read from. In case of a temporary failure, to reset the alarm bits to 0, issue a software reset (see *セクション 7.3.5*) command or cycle power to the DAC. A permanent failure in the NVM makes the device unusable.

7.3.4 Power-On Reset (POR)

The AFEx3902-Q1 family of devices includes a power-on reset (POR) function that controls the output voltage at power up. After the V_{DD} supply has been established, a POR event is issued. The POR causes all registers to initialize to default values, and communication with the device is valid only after a POR (boot-up) delay. The default value for all the registers in the AFEx3902-Q1 is loaded from NVM as soon as the POR event is issued.

When the device powers up, a POR circuit sets the device to the default mode. The POR circuit requires specific V_{DD} levels, as indicated in 図 7-2, to make sure that the internal capacitors discharge and reset the device at power up. To make sure that a POR occurs, V_{DD} must be less than 0.7 V for at least 1 ms. When V_{DD} drops to less than 1.65 V, but remains greater than 0.7 V (shown as the undefined region), the device may or may not reset under all specified temperature and power-supply conditions. In this case, initiate a POR. When V_{DD} remains greater than 1.65 V, a POR does not occur.

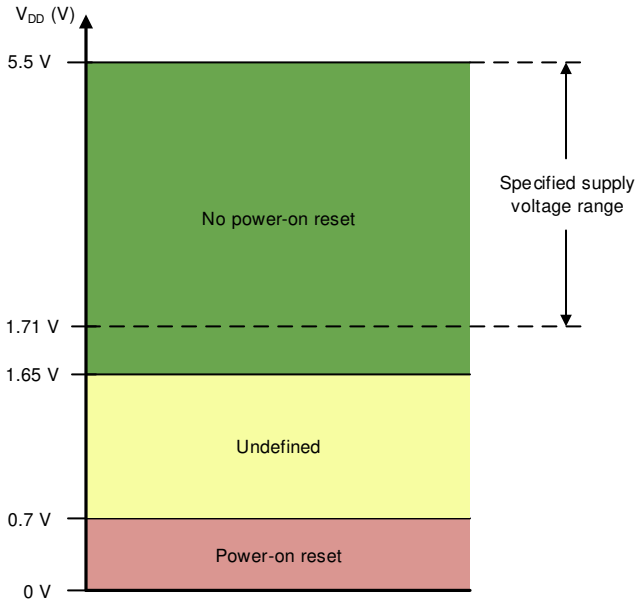


図 7-2. Threshold Levels for V_{DD} POR Circuit

7.3.5 External Reset

An external reset to the device can be triggered through the register map. To initiate a device software reset event, write the reserved code 1010b to the RESET field in the COMMON-TRIGGER register. A software reset initiates a POR event.

7.3.6 Register-Map Lock

The AFEx3902-Q1 implement a register-map lock feature that prevents an accidental or unintended write to the DAC registers. The device locks all the registers when the DEV-LOCK bit in the COMMON-CONFIG register is set to 1. However, the software reset function through the COMMON-TRIGGER register is not blocked when using I^2C interface. To bypass the DEV-LOCK setting, write 0101b to the DEV-UNLOCK bits in the COMMON-TRIGGER register.

7.4 Device Functional Modes

7.4.1 Digital-to-Analog Converter (DAC) Mode

The ADC and DAC channels can be enabled by selecting the power-up option in the VOUT-PDN-X or ADC-PDN-X fields in the COMMON-CONFIG register. Short the OUTx and FBx pins of the DAC channel externally for closed-loop amplifier output. An open FBx pin saturates the amplifier output for the DAC channel. To achieve the desired voltage output and ADC input ranges, select the correct reference option and select the amplifier gain.

7.4.1.1 Voltage Reference and DAC Transfer Function

図 7-3 shows the three possible voltage reference options with the AFEx3902-Q1: the power supply as reference, internal reference, or external reference (VREF/MODE pin). The DAC transfer function changes based on the voltage reference selection.

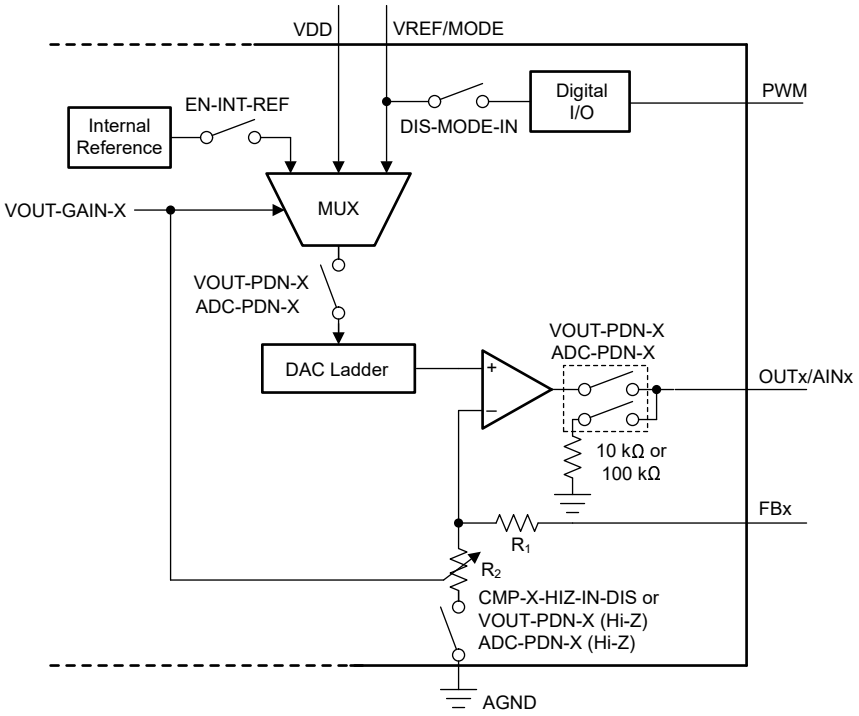


図 7-3. Voltage Reference Selection and Power-Down Logic

7.4.1.1.1 Power-Supply as Reference

By default, the AFEx3902-Q1 operate with the power-supply pin (VDD) as a reference. 式 1 shows DAC transfer function when the power-supply pin is used as reference. The gain at the output stage is always 1 ×.

$$V_{OUT} = \frac{DAC\_DATA}{2^N} \times V_{DD} \quad (1)$$

where:

- N is the resolution in bits, 10 bits for AFE53902-Q1 and 8 bits for AFE43902-Q1.
- DAC_DATA is the decimal equivalent of the binary code that is loaded to the DAC register.
- DAC_DATA ranges from 0 to $2^N - 1$.
- V_{DD} is used as the reference voltage.

7.4.1.1.2 Internal Reference

The AFEx3902-Q1 contain an internal reference that is disabled by default. To enable the internal reference, write 1 to the EN-INT-REF bit in the COMMON-CONFIG register. The internal reference generates a fixed 1.21-V voltage (typical). Use the VOUT-GAIN-x field in the DAC-x-VOUT-CMP-CONFIG register to achieve gains of 1.5 ×, 2 ×, 3 ×, or 4 × for the DAC output voltage (V_{OUT}). 式 2 shows DAC transfer function using the internal reference.

$$V_{OUT} = \frac{DAC\_DATA}{2^N} \times V_{REF} \times GAIN \quad (2)$$

where:

- N is the resolution in bits, 10 bits for AFE53902-Q1 or 8 bits for AFE43902-Q1.
- DAC_DATA is the decimal equivalent of the binary code that is loaded to the DAC register.
- DAC_DATA ranges from 0 to 2^N – 1.
- V_{REF} is the internal reference voltage = 1.21 V.
- GAIN = 1.5 ×, 2 ×, 3 ×, or 4 ×, based on VOUT-GAIN-x bits.

7.4.1.1.3 External Reference

The AFEx3902-Q1 provide an external reference input. Select the external reference option by configuring the VOUT-GAIN-x field in the DAC-x-VOUT-CMP-CONFIG register appropriately. The external reference can be between 1.8 V and VDD. 式 3 shows DAC transfer function when the external reference is used.

注

The external reference must be less than VDD in both transient and steady-state conditions. Therefore, the external reference must ramp up after VDD and ramp down before VDD.

$$V_{OUT} = \frac{DAC\_DATA}{2^N} \times V_{REF} \quad (3)$$

where:

- N is the resolution in bits, 10 bits for AFE53902-Q1 or 8 bits for AFE43902-Q1.
- DAC_DATA is the decimal equivalent of the binary code that is loaded to the DAC register.
- DAC_DATA ranges from 0 to 2^N – 1.
- V_{REF} is the external reference voltage.

7.4.2 Pulse-Width Modulation (PWM) Mode

The AFEx3902-Q1 provides the 7-bit PWM output on the SDA/SCLK/PWM pin. Pull the VREF/MODE pin high to enable PWM functionality. 表 7-1 lists all the possible PWM frequency configurations.

表 7-1. PWM Frequency Configuration

SRAM LOCATION	PWM-FREQ	PWM FREQUENCY (kHz)	DUTY CYCLE (%) FOR CODE 1	DUTY CYCLE (%) FOR CODE 126
0x2E [11:7]	0	Invalid	N/A	N/A
	1	48.828	4.88	95.12
	2	24.414	2.44	97.56
	3	16.276	1.63	98.37
	4	12.207	1.22	98.44
	5	8.138	0.81	98.44
	6	6.104	0.78	98.44
	7	3.052	0.78	98.44
	8	2.035	0.78	98.44
	9	1.526	0.78	98.44
	10	1.221	0.78	98.44
	11	1.017	0.78	98.44
	12	0.872	0.78	98.44
	13	0.763	0.78	98.44
	14	0.678	0.78	98.44
	15	0.610	0.78	98.44
	16	0.555	0.78	98.44
	17	0.509	0.78	98.44
	18	0.470	0.78	98.44
	19	0.436	0.78	98.44
	20	0.407	0.78	98.44
	21	0.381	0.78	98.44
	22	0.359	0.78	98.44
	23	0.339	0.78	98.44
	24	0.321	0.78	98.44
	25	0.305	0.78	98.44
	26	0.291	0.78	98.44
	27	0.277	0.78	98.44
	28	0.265	0.78	98.44
	29	0.254	0.78	98.44
	30	0.244	0.78	98.44
	31	0.218	0.78	98.44

The duty cycle of the PWM is proportional to the 7-bit code, 0d to 126d. 表 7-2 shows that code 127d corresponds to 100% duty cycle. The duty cycle 99.22% (127d/128d) is skipped to achieve 100% duty cycle using a 7-bit code.

表 7-2. PWM Duty Cycle Setting

CODE	DUTY-CYCLE	DESCRIPTION
0	0%	Always 0
1	0.78%	Minimum linear duty cycle
x	(x/128)%	*x* = code between 2d and 125d, both included
126	98.44%	Maximum linear duty cycle
127	100%	Always 1. The duty cycle of 99.22% (127d/128d) is skipped.

7.4.3 Analog-to-Digital Converter (ADC) Mode

Channel 0 of the AFEx3902-Q1 acts as an ADC. The ADC is controlled by the state-machine in this device. The transfer function of the ADC is given in 式 4.

$$\text{ADC\_DATA} = \left(\text{INTEGER}\right)\left(\frac{V_{IN}}{V_{FS}}\right) \times 2^{N} \tag{4}$$

where:

- ADC_DATA is the output of the ADC available to the state machine and is limited to (2^N–1).
- V_{IN} is the input voltage at the AIN0 pin.
- V_{FS} is the full-scale input voltage, as provided in 表 7-3.
- N is the number of ADC bits = 10.
- INTEGER denotes integer division.

表 7-3. Full Scale Analog Input (V_{FS})

REFERENCE (VREF)	GAIN	V_{FS}
Power supply	1 ×	VDD / 3
External	1 ×	VREF / 3
Internal	1.5 ×	(VREF × GAIN) / 3
	2 ×	(VREF × GAIN) / 3
	3 ×	(VREF × GAIN) / 6
	4 ×	(VREF × GAIN) / 6

7.4.4 Multislope Thermal Foldback Mode

AFEx3902-Q1 provide a multislope transfer function that is used in fine control of LED thermal foldback or similar other applications. The input to the transfer function are the (x, y) coordinates of the junction points. The x-axis (temperature input) and y-axis (voltage or PWM output) are normalized to the 10-bit straight binary code range. 図 7-4 shows the pictorial depiction of the multislope transfer function. 表 7-4 lists the SRAM locations to configure the multislope transfer function.

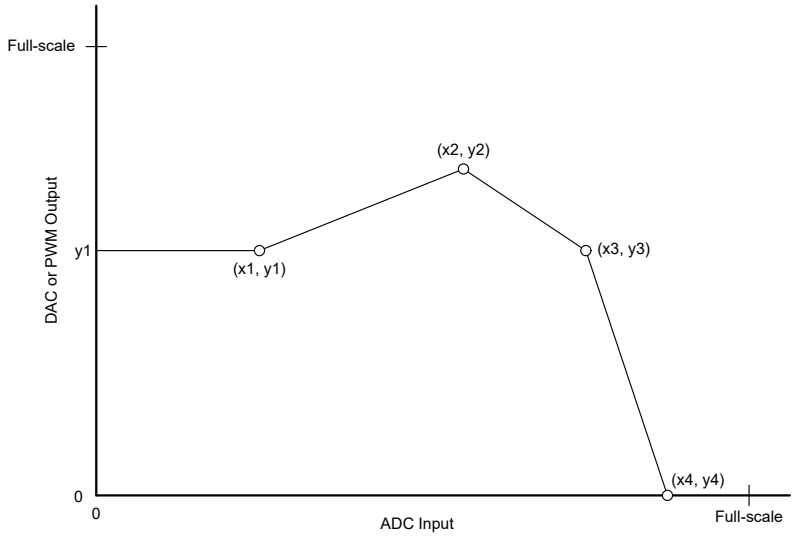


図 7-4. Multislope Transfer Function

表 7-4. Multislope Transfer Function Coordinates

COORDINATES	REGISTER NAME	SRAM ADDRESS (HEX)	DEFAULT VALUE (HEX)
x1	X1-OUTPUT	0x26	0x15
y1	X1-OUTPUT	0x27	0x200
x2	X2-OUTPUT	0x28	0x32
y2	Y2-OUTPUT	0x29	0x3FF
x3	X3-OUTPUT	0x2A	0x50
y3	Y3-OUTPUT	0x2B	0x00
x4	X4-OUTPUT	0x2C	0x68
y4	Y4-OUTPUT	0x2D	0x2BC

7.4.4.1 Thermistor Linearization

Thermistors, especially the negative temperature-coefficient (NTC) thermistors are used to measure LED temperature in front lights and rear lights of automotive vehicles. NTCs have a nonlinear temperature response. The AFEx3902-Q1 provide a three-segment, piecewise, linear method of linearizing the NTC before feeding the value to thermal foldback computation. 図 7-5 depicts how a NTC curve is linearized.

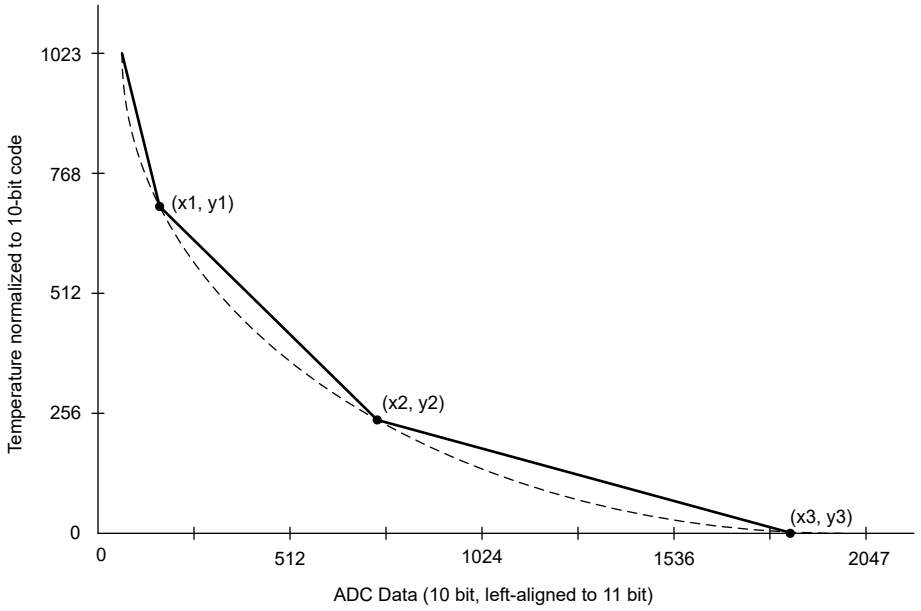


図 7-5. Thermistor Linearization

表 7-5 lists the SRAM locations for the linearization coordinates.

表 7-5. Thermistor Linearization Coordinates

COORDINATE	REGISTER NAME	SRAM ADDRESS (HEX)	DEFAULT VALUE (HEX)
x1	X1-TEMPERATURE	0x20	0x69
y1	Y1-TEMPERATURE	0x21	0x288
x2	X2-TEMPERATURE	0x22	0x46
y2	Y2-TEMPERATURE	0x23	0x634
x3	X3-TEMPERATURE	0x24	0x14
y3	Y3-TEMPERATURE	0x25	0x15

7.5 Programming

7.5.1 SPI Programming Mode

An SPI access cycle for the AFEx3902-Q1 is initiated by asserting the $\overline{\text{SYNC}}$ pin low. The serial clock, SCLK, can be continuous or gated. SDI data are clocked on the SCLK falling edges. The SPI frame for the AFEx3902-Q1 is 24 bits long. Therefore, the $\overline{\text{SYNC}}$ pin must stay low for at least 24 SCLK falling edges. The access cycle ends when the $\overline{\text{SYNC}}$ pin is deasserted high. If the access cycle contains less than the minimum clock edges, the communication is ignored. By default, the SDO pin is not enabled (three-wire SPI). In three-wire SPI mode, if the access cycle contains more than the minimum clock edges, only the first 24 bits are used by the device. When $\overline{\text{SYNC}}$ is high, the SCLK and SDI signals are blocked, and SDO becomes Hi-Z to allow data readback from other devices connected on the bus.

表 7-6 and 図 7-6 describe the format for the 24-bit SPI access cycle. The first byte input to SDI is the instruction cycle. The instruction cycle identifies the request as a read or write command and the 7-bit address that is to be accessed. The last 16 bits in the cycle form the data cycle.

表 7-6. SPI Read/Write Access Cycle

BIT	FIELD	DESCRIPTION
23	R/$\overline{\text{W}}$	Identifies the communication as a read or write command to the address register: R/$\overline{\text{W}}$ = 0 sets a write operation. R/$\overline{\text{W}}$ = 1 sets a read operation
22-16	A[6:0]	Register address: specifies the register to be accessed during the read or write operation
15-0	DI[15:0]	Data cycle bits: If a write command, the data cycle bits are the values to be written to the register with address A[6:0]. If a read command, the data cycle bits are *don't care* values.

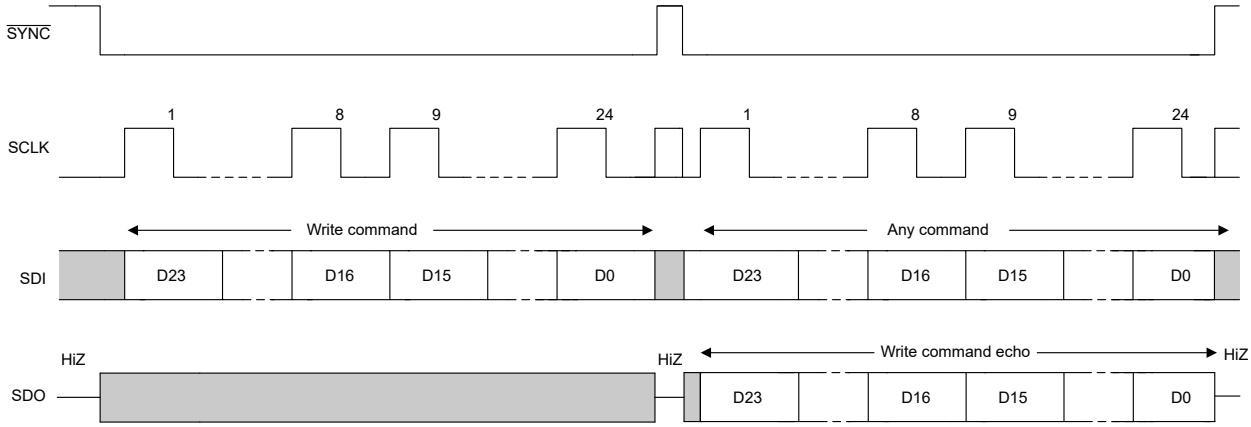


図 7-6. SPI Write Cycle

Read operations require that the SDO pin is first enabled by setting the SDO-EN bit in the INTERFACE-CONFIG register. This configuration is called four-wire SPI. A read operation is initiated by issuing a read command access cycle. After the read command, a second access cycle must be issued to get the requested data. 表 7-7 and 図 7-7 show the output data format. Data are clocked out on the SDO pin either on the falling edge or rising edge of SCLK according to the FSDO bit (see also 図 6-3).

表 7-7. SDO Output Access Cycle

BIT	FIELD	DESCRIPTION
23	R/$\overline{\text{W}}$	Echo R/$\overline{\text{W}}$ from previous access cycle
22-16	A[6:0]	Echo register address from previous access cycle
15-0	DI[15:0]	Readback data requested on previous access cycle

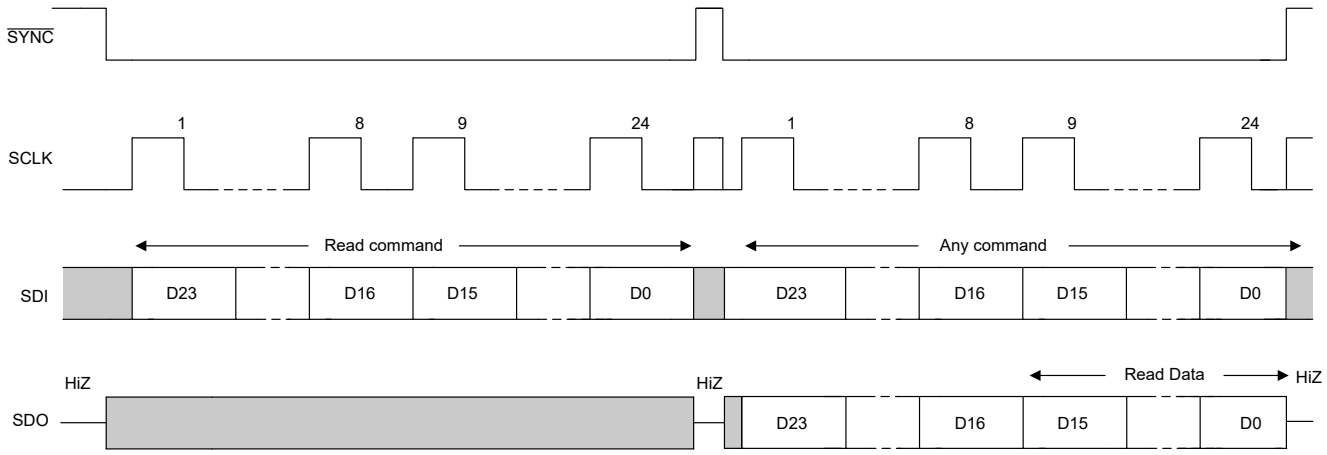


図 7-7. SPI Read Cycle

The daisy-chain operation is also enabled with the SDO pin. 図 7-8 shows that in daisy-chain mode, multiple devices are connected in a *chain* with the SDO pin of one device is connected to SDI pin of the following device. The SPI host drives the SDI pin of the first device in the chain. The SDO pin of the last device in the chain is connected to the POCI pin of the SPI host. In four-wire SPI mode, if the access cycle contains multiples of 24 clock edges, only the last 24 bits are used by the device first device in the chain. If the access cycle contains clock edges that are not in multiples of 24, the SPI packet is ignored by the device. 図 7-9 describes the packet format for the daisy-chain write cycle.

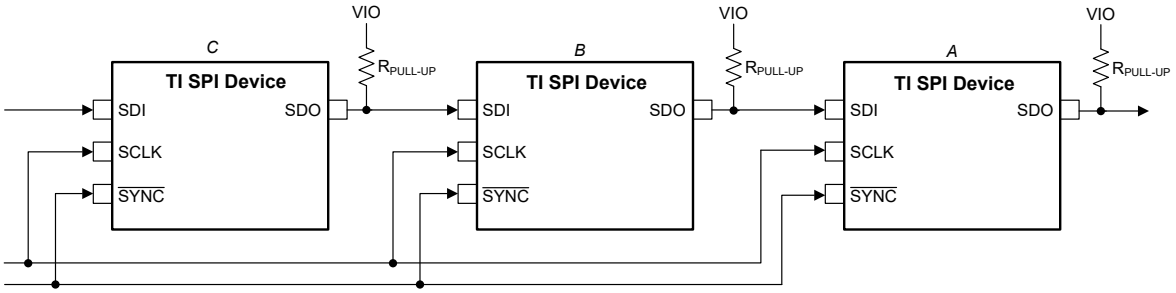


図 7-8. SPI Daisy-Chain Connection

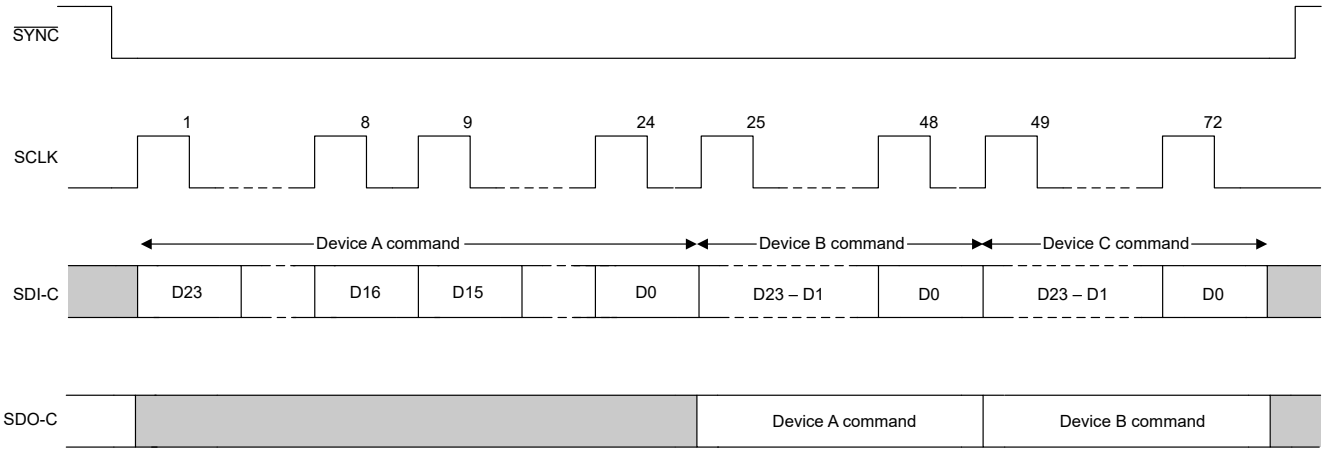


図 7-9. SPI Daisy-Chain Write Cycle

7.5.2 I²C Programming Mode

The AFEx3902-Q1 has a 2-wire serial interface (SCL and SDA), and one address pin (A0); see also 図 5-1. The I²C bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I²C-compatible devices connect to the I²C bus through the open drain I/O pins, SDA and SCL.

The I²C specification states that the device that controls communication is called a *controller*, and the devices that are controlled by the controller are called *targets*. The controller generates the SCL signal. The controller also generates special timing conditions (start condition, repeated start condition, and stop condition) on the bus to indicate the start or stop of a data transfer. Device addressing is completed by the controller. The controller on an I²C bus is typically a microcontroller or digital signal processor (DSP). The AFEx3902-Q1 operates as a target on the I²C bus. A target acknowledges controller commands, and upon controller control, receives or transmits data.

Typically, the AFEx3902-Q1 family operates as a target receiver. A controller writes to the AFEx3902-Q1, a target receiver. However, if a controller requires the AFEx3902-Q1 internal register data, the AFEx3902-Q1 operates as a target transmitter. In this case, the controller reads from the AFEx3902-Q1. According to I²C terminology, read and write refer to the controller.

The AFEx3902-Q1 supports the following data transfer modes:

- Standard mode (100Kbps)
- Fast mode (400Kbps)
- Fast mode plus (1.0Mbps)

The data transfer protocol for standard and fast modes is exactly the same; therefore, both modes are referred to as *F/S-mode* in this document. The fast mode plus protocol is supported in terms of data transfer speed, but not output current. The low-level output current is 3 mA; similar to the case of standard and fast modes. The AFEx3902-Q1 supports 7-bit addressing. The 10-bit addressing mode is not supported. The device supports the general call reset function. Sending the following sequence initiates a software reset within the device: start or repeated start, 0x00, 0x06, stop. The reset is asserted within the device on the rising edge of the ACK bit, following the second byte.

Other than specific timing signals, the I²C interface works with serial bytes. At the end of each byte, a ninth clock cycle generates and detects an acknowledge signal. An acknowledge is when the SDA line is pulled low during the high period of the ninth clock cycle. 図 7-10 depicts a not-acknowledge, when the SDA line is left high during the high period of the ninth clock cycle.

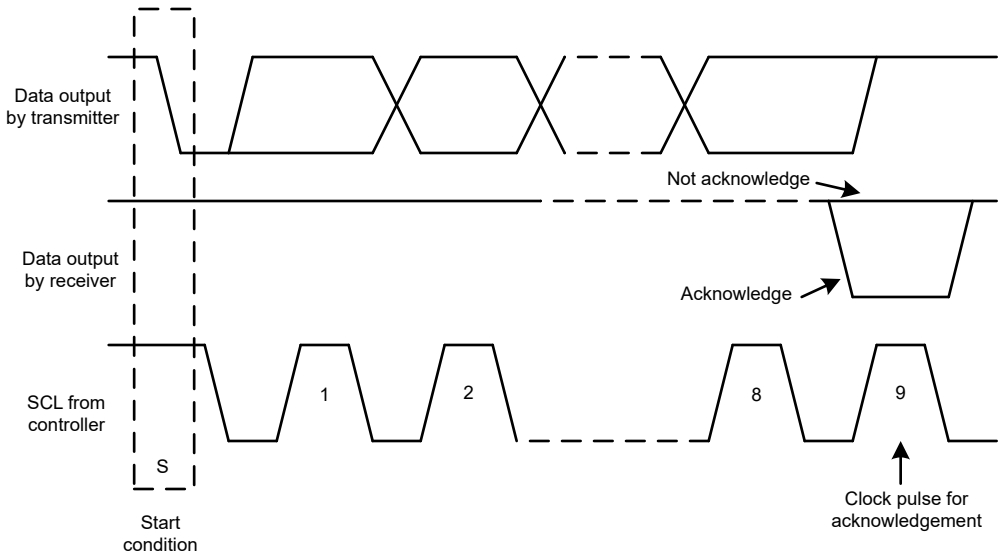


図 7-10. Acknowledge and Not Acknowledge on the I²C Bus

7.5.2.1 F/S Mode Protocol

The following steps explain a complete transaction in F/S mode.

1. The controller initiates data transfer by generating a start condition. 図 7-11 shows that the start condition is when a high-to-low transition occurs on the SDA line while SCL is high. All I^2C-compatible devices recognize a start condition.
2. The controller then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit (R/$\overline{W}$) on the SDA line. During all transmissions, the controller makes sure that data are valid. 図 7-12 shows that a valid data condition requires the SDA line to be stable during the entire high period of the clock pulse. All devices recognize the address sent by the controller and compare the address to the respective internal fixed address. Only the target device with a matching address generates an acknowledge by pulling the SDA line low during the entire high period of the 9th SCL cycle (see also 図 7-10). When the controller detects this acknowledge, the communication link with a target has been established.
3. The controller generates further SCL cycles to transmit (R/$\overline{W}$ bit 0) or receive (R/$\overline{W}$ bit 1) data to the target. In either case, the receiver must acknowledge the data sent by the transmitter. The acknowledge signal can be generated by the controller or by the target, depending on which is the receiver. The 9-bit valid data sequences consists of eight data bits and one acknowledge-bit, and can continue as long as necessary.
4. 図 7-11 shows that to signal the end of the data transfer, the controller generates a stop condition by pulling the SDA line from low-to-high while the SCL line is high. This action releases the bus and stops the communication link with the addressed target. All I^2C-compatible devices recognize the stop condition. Upon receipt of a stop condition, the bus is released, and all target devices then wait for a start condition followed by a matching address.

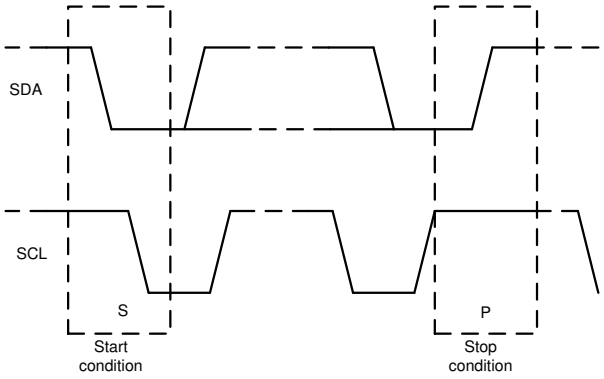


図 7-11. Start and Stop Conditions

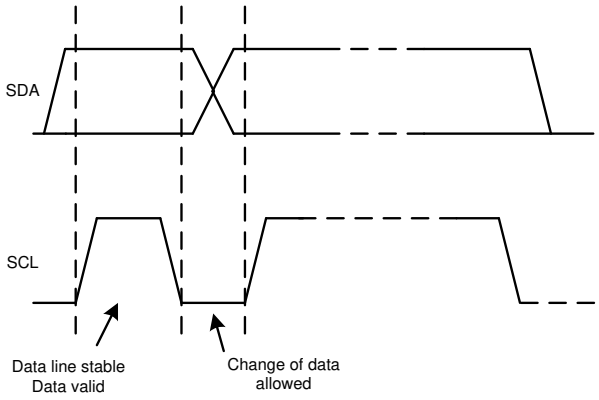


図 7-12. Bit Transfer on the I^2C Bus

7.5.2.2 I²C Update Sequence

表 7-8 shows that for a single update, the AFEx3902-Q1 requires a start condition, a valid I²C address byte, a command byte, and two data bytes.

表 7-8. Update Sequence

MSB	....	LSB	ACK	MSB	...	LSB	ACK	MSB	...	LSB	ACK	MSB	...	LSB	ACK
Address (A) byte セクション 7.5.2.2.1				Command byte セクション 7.5.2.2.2				Data byte - MSDB				Data byte - LSDB			
DB [31:24]				DB [23:16]				DB [15:8]				DB [7:0]			

図 7-13 shows that after each byte is received, the AFEx3902-Q1 acknowledges the byte by pulling the SDA line low during the high period of a single clock pulse. These four bytes and acknowledge cycles make up the 36 clock cycles required for a single update to occur. A valid I²C address byte selects the AFEx3902-Q1.

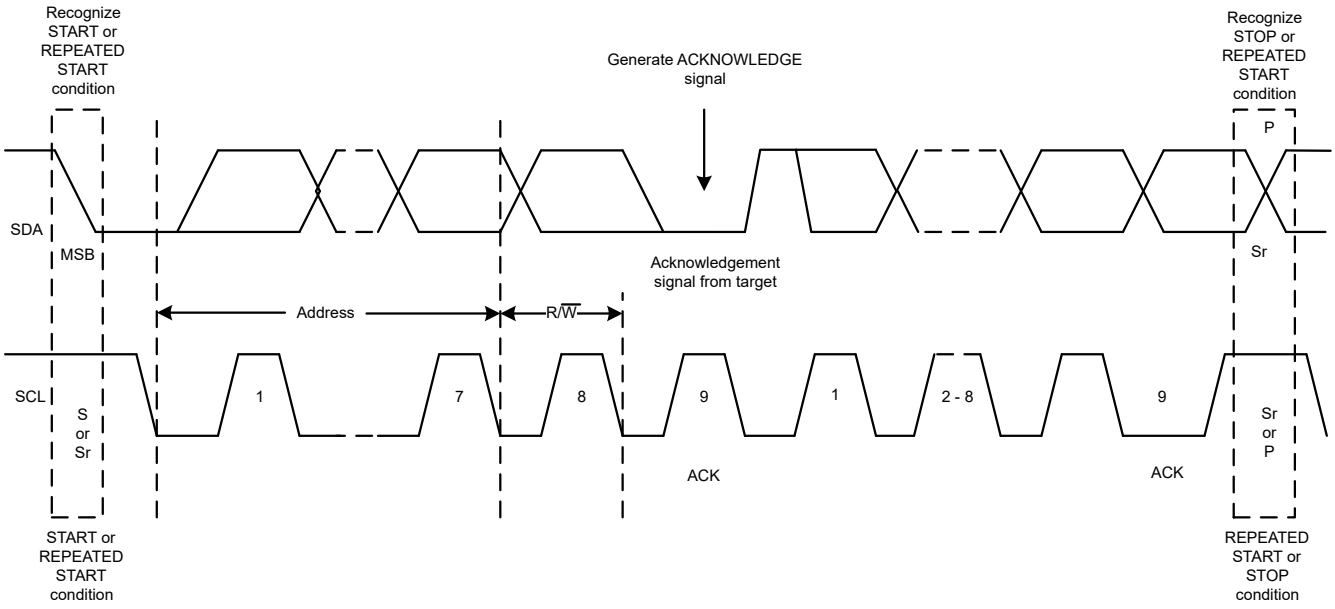


図 7-13. I²C Bus Protocol

The command byte sets the operating mode of the selected AFEx3902-Q1 device. For a data update to occur when the operating mode is selected by this byte, the AFEx3902-Q1 device must receive two data bytes: the most significant data byte (MSDB) and least significant data byte (LSDB). The AFEx3902-Q1 device performs an update on the falling edge of the acknowledge signal that follows the LSDB.

When using fast mode (clock = 400 kHz), the maximum DAC update rate is limited to 10 kSPS. Using fast mode plus (clock = 1 MHz), the maximum DAC update rate is limited to 25 kSPS. When a stop condition is received, the AFEx3902-Q1 device releases the I²C bus and awaits a new start condition.

7.5.2.2.1 Address Byte

表 7-9 depicts the address byte, the first byte received from the controller device following the start condition. The first four bits (MSBs) of the address are factory preset to 0b1001. The next three bits of the address are controlled by the A0 pin. The A0 pin input can be connected to VDD, AGND, SCL, or SDA. The A0 pin is sampled during the first byte of each data frame to determine the address. The device latches the value of the address pin, and consequently responds to that particular address according to 表 7-10.

表 7-9. Address Byte

COMMENT	MSB							LSB
—	AD6	AD5	AD4	AD3	AD2	AD1	AD0	R/$\overline{W}$
General address	1	0	0	1	See 表 7-10 (target address column)			0 or 1
Broadcast address	1	0	0	0	1	1	1	0

表 7-10. Address Format

TARGET ADDRESS	A0 PIN
000	AGND
001	VDD
010	SDA
011	SCL

The AFEx3902-Q1 supports broadcast addressing, which is used for synchronously updating or powering down multiple AFEx3902-Q1 devices. When the broadcast address is used, the AFEx3902-Q1 responds regardless of the address pin state. Broadcast is supported only in write mode.

7.5.2.2.2 Command Byte

表 7-13 lists the command byte in the ADDRESS column.

7.5.2.3 I^2C Read Sequence

To read any register the following command sequence must be used:

1. Send a start or repeated start command with a target address and the R/$\overline{W}$ bit set to 0 for writing. The device acknowledges this event.
2. Send a command byte for the register to be read. The device acknowledges this event again.
3. Send a repeated start with the target address and the R/$\overline{W}$ bit set to 1 for reading. The device acknowledges this event.
4. The device writes the MSDB byte of the addressed register. The controller must acknowledge this byte.
5. Finally, the device writes out the LSDB of the register.

The broadcast address cannot be used for reading.

表 7-11. Read Sequence

S	MSB	…	R/$\overline{W}$ (0)	ACK	MSB	…	LSB	ACK	Sr	MSB	…	R/$\overline{W}$ (1)	ACK	MSB	…	LSB	ACK	MSB	…	LSB	ACK
	Address byte セクション 7.5.2.2.1				Command byte セクション 7.5.2.2.2				Sr	Address byte セクション 7.5.2.2.1				MSDB				LSDB			
From controller				Target	From controller			Target	From controller				Target	From target			Controller	From target			Controller

7.6 Register Maps

表 7-12. Register Map

REGISTER	MOST SIGNIFICANT DATA BYTE (MSDB)								LEAST SIGNIFICANT DATA BYTE (LSDB)							
	BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
NOP	NOP															
DAC-0-VOUT-CMP-CONFIG	X			VOUT-GAIN-0			X					CMP-0-OD-EN	CMP-0-OUT-EN	CMP-0-HIZ-IN-DIS	CMP-0-INV-EN	CMP-0-EN
DAC-1-VOUT-CMP-CONFIG	X			VOUT-GAIN-1			X					CMP-1-OD-EN	CMP-1-OUT-EN	CMP-1-HIZ-IN-DIS	CMP-1-INV-EN	CMP-1-EN
COMMON-CONFIG	RESERVED	DEV-LOCK	RESERVED	EN-INT-REF	ADC-PDN-0		RESERVED							VOUT-PDN-1		RESERVED
COMMON-TRIGGER	DEV-UNLOCK				RESET				RESERVED						NVM-PROG	NVM-RELOAD
COMMON-PWM-TRIG	RESERVED															START-FUNCTION
GENERAL-STATUS	NVM-CRC-FAIL-INT	NVM-CRC-FAIL-USER	X	DAC-0-BUSY	X		DAC-1-BUSY	NVM-BUSY	DEVICE-ID							
DEVICE-MODE-CONFIG	RESERVED		DIS-MODE-IN	RESERVED						SM-IO-EN	RESERVED					
INTERFACE-CONFIG	X			TIMEOUT-EN	RESERVED									FSDO-EN	X	SDO-EN
STATE-MACHINE-CONFIG0	RESERVED													SM-ABORT	SM-START	SM-EN
SRAM-CONFIG	X								SRAM-ADDR							
SRAM-DATA	SRAM-DATA															
X1-TEMPERATURE	RESERVED						X1-TEMPERATURE									RESERVED
X2-TEMPERATURE	RESERVED						X2-TEMPERATURE									RESERVED
X3-TEMPERATURE	RESERVED						X3-TEMPERATURE									RESERVED
X4-TEMPERATURE	RESERVED						X4-TEMPERATURE									RESERVED
Y1-TEMPERATURE	RESERVED								Y1-TEMPERATURE							
Y2-TEMPERATURE	RESERVED								Y2-TEMPERATURE							
Y3-TEMPERATURE	RESERVED								Y3-TEMPERATURE							
Y4-TEMPERATURE	RESERVED								Y4-TEMPERATURE							
X1-OUTPUT	RESERVED								X1-OUTPUT							
X2-OUTPUT	RESERVED								X2-OUTPUT							
X3-OUTPUT	RESERVED								X3-OUTPUT							
X4-OUTPUT	RESERVED								X4-OUTPUT							
Y1-OUTPUT	RESERVED						Y1-OUTPUT									
Y2-OUTPUT	RESERVED						Y2-OUTPUT									
Y3-OUTPUT	RESERVED						Y3-OUTPUT									
Y4-OUTPUT	RESERVED						Y4-OUTPUT									
PWM-FREQUENCY	RESERVED				PWM-FREQUENCY				RESERVED							

Note: Shaded cells indicate the register bits or fields that are stored in NVM.

Note: X = Don't care.

表 7-13. Register Names

I²C/SPI ADDRESS	SRAM ADDR	REGISTER NAME	SECTION
00h	--	NOP	セクション 7.6.1
15h	--	DAC-0-VOUT-CMP-CONFIG	セクション 7.6.2
03h	--	DAC-1-VOUT-CMP-CONFIG	セクション 7.6.2
1Fh	--	COMMON-CONFIG	セクション 7.6.3
20h	--	COMMON-TRIGGER	セクション 7.6.4
21h	--	COMMON-PWM-TRIG	セクション 7.6.5
22h	--	GENERAL-STATUS	セクション 7.6.6
25h	--	DEVICE-MODE-CONFIG	セクション 7.6.7
26h	--	INTERFACE-CONFIG	セクション 7.6.8
27h	--	STATE-MACHINE-CONFIG0	セクション 7.6.9
2Bh	--	SRAM-CONFIG	セクション 7.6.10
2Ch	--	SRAM-DATA	セクション 7.6.11
--	20h	X1-TEMPERATURE	セクション 7.6.12
--	21h	Y1-TEMPERATURE	セクション 7.6.13
--	22h	X2-TEMPERATURE	セクション 7.6.12
--	23h	Y2-TEMPERATURE	セクション 7.6.13
--	24h	X3-TEMPERATURE	セクション 7.6.12
--	25h	Y3-TEMPERATURE	セクション 7.6.13
--	26h	X1-OUTPUT	セクション 7.6.14
--	27h	Y1-OUTPUT	セクション 7.6.15
--	28h	X2-OUTPUT	セクション 7.6.14
--	29h	Y2-OUTPUT	セクション 7.6.15
--	2Ah	X3-OUTPUT	セクション 7.6.14
--	2Bh	Y3-OUTPUT	セクション 7.6.15
--	2Ch	X4-OUTPUT	セクション 7.6.14
--	2Dh	Y4-OUTPUT	セクション 7.6.15
--	2Eh	PWM-FREQUENCY	セクション 7.6.16

7.6.1 NOP Register (address = 00h) [reset = 0000h]

図 7-14. NOP Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NOP															
R/W-0000h															

表 7-14. NOP Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	NOP	R/W	0000h	No operation

7.6.2 DAC-x-VOUT-CMP-CONFIG Register (address = 15h, 03h) [reset = 0400h]

図 7-15. DAC-x-VOUT-CMP-CONFIG Register (x = 0, 1)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X			VOUT-GAIN-x			X					CMP-x-OD-EN	CMP-x-OUT-EN	CMP-x-HIZ-IN-DIS	CMP-x-INV-EN	CMP-x-EN
X-0h			R/W-0h			X-00h					R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

表 7-15. DAC-x-VOUT-CMP-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	X	X	0h	Don't care.
12-10	VOUT-GAIN-x	R/W	001	001: Gain = 1 ×, VDD as reference. 010: Gain = 1.5 ×, internal reference. 011: Gain = 2 ×, internal reference. 100: Gain = 3 ×, internal reference. 101: Gain = 4 ×, internal reference. Others: NA.
9-5	X	X	0h	Don't care.
4	CMP-x-OD-EN	R/W	0	1: Set OUTx pin as open-drain in comparator mode (CMP-x-EN = 1 and CMP-x-OUT-EN = 1). 0: Set OUTx pin as push-pull.
3	CMP-x-OUT-EN	R/W	0	1: Bring comparator output to the respective OUTx pin. 0: Generate comparator output but consume internally.
2	CMP-x-HIZ-IN-DIS	R/W	0	0: FBx input has high-impedance. Input voltage range is limited. 1: FBx input is connected to resistor divider and has finite impedance. Input voltage range is same as full-scale.
1	CMP-x-INV-EN	R/W	0	1: Invert the comparator output. 0: Don't invert the comparator output.
0	CMP-x-EN	R/W	0	1: Enable comparator mode. 0: Disable comparator mode.

7.6.3 COMMON-CONFIG Register (address = 1Fh) [reset = 03F9h]

図 7-16. COMMON-CONFIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	DEV-LOCK	RESERVED	EN-INT-REF	ADC-PDN-0		RESERVED							VOUT-PDN-1		RESERVED
R/W-0	R/W-0	R/W-0	R/W-0	R/W-00		R/W-7Fh							R/W-00		R/W-1

表 7-16. COMMON-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0	Always write 0.
14	DEV-LOCK	R/W	0	0: Device not locked 1: Device locked, the device locks all the registers. To set this bit back to 0 (unlock device), write to the unlock code to the DEV-UNLOCK field in the COMMON-TRIGGER register first, followed by a write to the DEV-LOCK bit as 0.
13	RESERVED	R/W	0	Always write 0.
12	EN-INT-REF	R/W	0	0: Disable internal reference 1: Enable internal reference. This bit must be set before using internal reference gain settings.
11-10	ADC-PDN-0	R/W	00	00: Power-up ADC-0. 01: Power-down ADC-0 with 10 kΩ to AGND. 10: Power-down ADC-0 with 100 kΩ to AGND. 11: Power-down ADC-0 with Hi-Z to AGND.
9-3	RESERVED	R/W	7Fh	Always write 7Fh.
2-1	VOUT-PDN-1	R/W	00	00: Power-up VOUT-1. 01: Power-down VOUT-1 with 10 kΩ to AGND. 10: Power-down VOUT-1 with 100 kΩ to AGND. 11: Power-down VOUT-1 with Hi-Z to AGND.
0	RESERVED	R/W	1	Always write 1.

7.6.4 COMMON-TRIGGER Register (address = 20h) [reset = 0000h]

図 7-17. COMMON-TRIGGER Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEV-UNLOCK				RESET				RESERVED						NVM-PROG	NVM-RELOAD
R/W-0h				R/W-0h				R/W-00h						R/W-0h	R/W-0h

表 7-17. COMMON-TRIGGER Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	DEV-UNLOCK	R/W	0000	0101: Device unlocking password. Others: Don't care.
11-8	RESET	R/W	0000	1010: POR reset triggered. This field self-resets. Others: Don't care.
7-2	RESERVED	R/W	00h	Always write 00h.
1	NVM-PROG	R/W	0	0: NVM write not triggered. 1: NVM write triggered. This bit self-resets.
0	NVM-RELOAD	R/W	0	0: NVM reload not triggered. 1: Reload data from NVM to register map. This bit self-resets.

7.6.5 COMMON-PWM-TRIG Register (address = 21h) [reset = 0001h]

図 7-18. COMMON-PWM-TRIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															START-FUNCTION
R/W-0000h															R/W-0h

表 7-18. COMMON-PWM-TRIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-1	RESERVED	R/W	0000h	Always write 0000h.
0	START-FUNCTION	R/W	0	0: Stop PWM generation. 1: Invalid. This bit is automatically set by the state machine.

7.6.6 GENERAL-STATUS Register (address = 22h) [reset = 2068h]

図 7-19. GENERAL-STATUS Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NVM-CRC-FAIL-INT	NVM-CRC-FAIL-USER	X	DAC-0-BUSY	X		DAC-1-BUSY	NVM-BUSY	DEVICE-ID						VERSION-ID	
R-0h	R-0h	X-1h	R-0h	X-0h		R-0h	R-0h	AFE53902-Q1: R-10h AFE43902-Q1: R-11h						R-0h	

表 7-19. GENERAL-STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	NVM-CRC-FAIL-INT	R	0	0: No CRC error in OTP. 1: Indicates a failure in OTP loading. A software reset or power-cycle brings the device out of this condition in case of temporary failure.
14	NVM-CRC-FAIL-USER	R	0	0: No CRC error in NVM loading. 1: Indicates a failure in NVM loading. The register settings are corrupted. The device allows all operations during this error condition. Reprogram the NVM to get the original state. A software reset brings the device out of this error condition.
13	X	X	1	Don't care.
12	DAC-0-BUSY	R	0	0: DAC-0 channel accepts commands. 1: DAC-0 channel does not accept commands.
11-10	X	X	0	Don't care.
9	DAC-1-BUSY	R	0	0: DAC-1 channel accepts commands. 1: DAC-1 channel does not accept commands.
8	NVM-BUSY	R	0	0: NVM is available for read and write. 1: NVM is not available for read or write.
7-2	DEVICE-ID	R	AFE53902-Q1: 10h AFE43902-Q1: 11h	Device identifier.
1-0	VERSION-ID	R	00	Version identifier.

7.6.7 DEVICE-MODE-CONFIG Register (address = 25h) [reset = 8040h]

図 7-20. DEVICE-MODE-CONFIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		DIS-MODE-IN	RESERVED						SM-IO-EN	RESERVED					
R/W-10		R/W-0	R/W-00h						R/W-1	R/W-00h					

表 7-20. DEVICE-MODE-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R/W	10	Always write 10.
13	DIS-MODE-IN	R/W	0	0: MODE function enabled. 1: MODE function disabled.
12-7	RESERVED	R/W	00h	Always write 00h.
6	SM-IO-EN	R/W	1	0: The state machine does not have control over the digital input-output. 1: Digital input-output controlled by the state machine.
5-0	RESERVED	R/W	00h	Always write 00h.

7.6.8 INTERFACE-CONFIG Register (address = 26h) [reset = 0000h]

図 7-21. INTERFACE-CONFIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X			TIMEOUT-EN	X									FSDO-EN	X	SDO-EN
X-0h			R/W-0h	X-0h									R/W-0h	X-0h	R/W-0h

表 7-21. INTERFACE-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	X	X	0h	Don't care.
12	TIMEOUT-EN	R/W	0	0: I^2C timeout disabled. 1: I^2C timeout enabled.
11-3	X	X	0h	Don't care.
2	FSDO-EN	R/W	0	0: Fast SDO disabled. 1: Fast SDO enabled.
1	X	X	0	Don't care.
0	SDO-EN	R/W	0	0: SDO disabled. 1: SDO enabled.

7.6.9 STATE-MACHINE-CONFIG0 Register (address = 27h) [reset = 0003h]

図 7-22. STATE-MACHINE-CONFIG0 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													SM-ABORT	SM-START	SM-EN
R/W-0000h													R/W-0h	R/W-1	R/W-1

表 7-22. STATE-MACHINE-CONFIG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-3	RESERVED	R/W	0000h	Always write 0000h.
2	SM-ABORT	R/W	0	0: State machine not aborted. 1: State machine aborted.
1	SM-START	R/W	1	0: State machine stopped. 1: State machine started. The state machine must be enabled using the SM-EN bit.
0	SM-EN	R/W	1	0: State machine disabled. 1: State machine enabled.

7.6.10 SRAM-CONFIG Register (address = 2Bh) [reset = 0000h]

図 7-23. SRAM-CONFIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X								SRAM-ADDR							
X-00h								R/ W-00h							

表 7-23. SRAM-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	X	X	00h	Don't care.
7-0	SRAM-ADDR	R/W	00h	8-bit SRAM address. Writing to this register field configures the SRAM address to be accessed next. This address automatically increments after a read or write from the SRAM.

7.6.11 SRAM-DATA Register (address = 2Ch) [reset = 0000h]

図 7-24. SRAM-DATA Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRAM-DATA															
R/ W-0000h															

表 7-24. SRAM-DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	SRAM-DATA	R/W	0000h	16-bit SRAM data. This data is written to or read from the address configured in the SRAM-CONFIG register.

7.6.12 Xx-TEMPERATURE Register (SRAM address = 20h, 22h, 24h) [reset = 0000h]

注

This register address is mapped to SRAM. Use the SRAM-CONFIG and SRAM-DATA registers to read and write.

図 7-25. Xx-TEMPERATURE Register (X1, X2, X3)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					Xx-TEMPERATURE										RESERVED
W-00h					R/W-000h										W-0h

表 7-25. Xx-TEMPERATURE Register Field Descriptions (X1, X2, X3)

Bit	Field	Type	Reset	Description
15-11	RESERVED	X	00h	Always write 0.
10-1	Xx-TEMPERATURE	R/W	000h	10-bit X coordinate for NTC linearizer.
0	RESERVED	X	0	Always write 0.

7.6.13 Yx-TEMPERATURE Register (SRAM address = 21h, 23h, 25h) [reset = 0000h]

注

This register address is mapped to SRAM. Use the SRAM-CONFIG and SRAM-DATA registers to read and write.

図 7-26. Yx-TEMPERATURE Register (Y1, Y2, Y3)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								Yx-TEMPERATURE							
W-00h								R/W-00h							

表 7-26. Yx-TEMPERATURE Register Field Descriptions (Y1, Y2, Y3)

Bit	Field	Type	Reset	Description
15-8	RESERVED	W	00h	Always write 0.
7-0	Yx-TEMPERATURE	R/W	00h	8-bit Y coordinate for NTC linearizer.

7.6.14 Xx-OUTPUT Register (SRAM address = 26h, 28h, 2Ah, 2Ch) [reset = 0000h]

注

This register address is mapped to SRAM. Use the SRAM-CONFIG and SRAM-DATA registers to read and write.

図 7-27. Xx-OUTPUT Register (X1, X2, X3, X4)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								Xx-OUTPUT							
W-00h								R/W-00h							

表 7-27. Xx-OUTPUT Register Field Descriptions (X1, X2, X3, X4)

Bit	Field	Type	Reset	Description
15-8	RESERVED	W	00h	Always write 0.
7-0	Xx-OUTPUT	R/W	00h	8-bit X coordinate for multislope transfer function.

7.6.15 Yx-OUTPUT Register (SRAM address = 27h, 29h, 2Bh, 2Dh) [reset = 0000h]

注

This register address is mapped to SRAM. Use the SRAM-CONFIG and SRAM-DATA registers to read and write.

図 7-28. Yx-OUTPUT Register (Y1, Y2, Y3, Y4)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						Yx-OUTPUT									
W-00h						R/W-000h									

表 7-28. YX-OUTPUT Register Field Descriptions (Y1, Y2, Y3, Y4)

Bit	Field	Type	Reset	Description
15-10	RESERVED	W	00h	Always write 0.
9-0	Yx-OUTPUT	R/W	000h	10-bit Y coordinate for multislope transfer function.

7.6.16 PWM-FREQUENCY Register (SRAM address = 2Eh) [reset = 0000h]

注

This register address is mapped to SRAM. Use the SRAM-CONFIG and SRAM-DATA registers to read and write.

図 7-29. PWM-FREQUENCY Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X				PWM-FREQUENCY					X						
X-0h				R/W-00h					X-00h						

表 7-29. PWM-FREQUENCY Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	X	X	0h	Don't care.
11-7	PWM-FREQUENCY	R/W	00h	5-bit PWM frequency, as specified in 表 7-1.
6-0	X	X	00h	Don't care.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The AFEx3902-Q1 is a smart analog front end (AFE) that includes an ADC channel, PWM output, NVM, internal reference, and are available in a tiny 3-mm × 3-mm package. The AFEx3902-Q1 have an integrated state machine that is pre-programmed as a constant power output controller. The ADC has a full-scale of VDD/3. Use an external attenuator when the input exceeds this range. The PWM provides a 7-bit duty-cycle output on the SDA/SCLK/PWM pin. Pull the VREF/MODE pin high to enable the PWM output. Pulling the VREF/MODE pin low enables the I^2C or SPI programming mode. The application parameters are programmed in the device using I^2C or SPI and stored in the NVM.

8.2 Typical Applications

8.2.1 Multislope Thermal Foldback Using the AFE53902-Q1 and Voltage Output

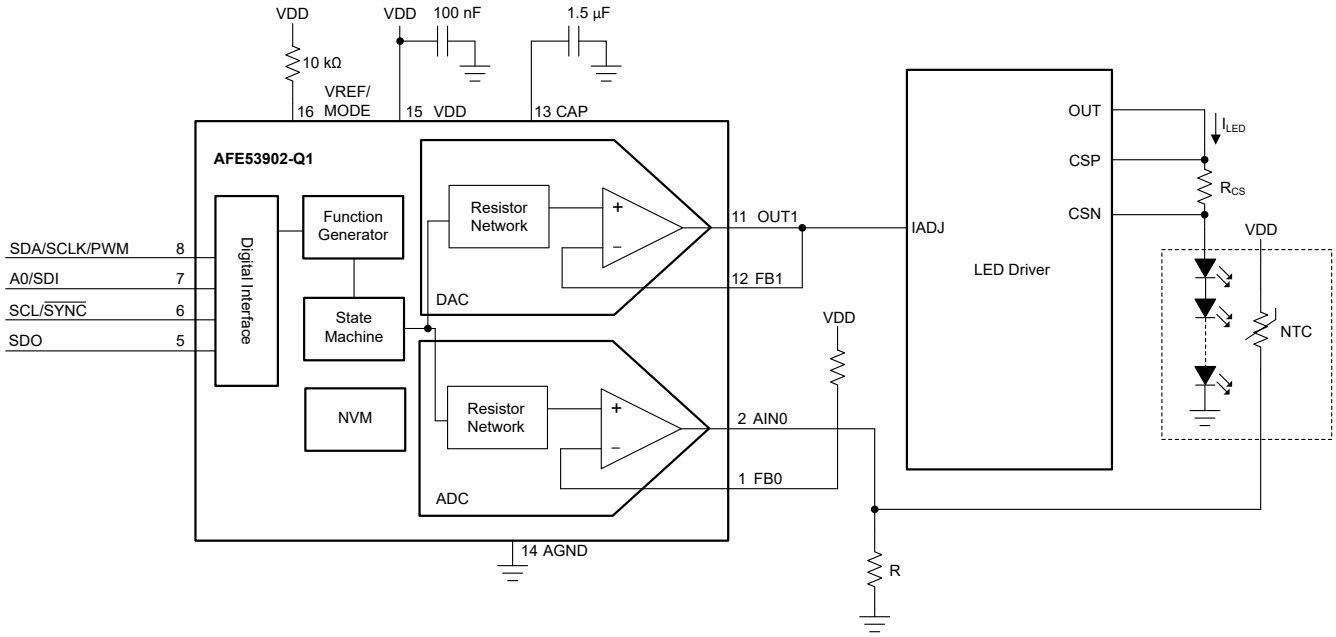


図 8-1. Multislope Thermal Foldback Using the AFE53902-Q1 and Voltage Output

図 8-1 shows how to connect the DAC output in voltage-output mode.

8.2.1.1 Design Requirements

表 8-1. AFE53902-Q1 With Voltage-Output Design Parameters

PARAMETER	VALUE
Voltage range	0 V to 5 V
Temperature range	0°C to 100°C

8.2.1.2 Detailed Design Procedure

The state machine converts a temperature input to a voltage output based on the values saved in the thermal foldback profile. The voltage output from the temperature sensor is read by the ADC and converted to an ADC code. There are three X and Y points available to map the ADC codes (X points) to a temperature (Y points). These points can be used to apply linearization to the temperature sensor output. The ADC is 10-bits, so the maximum code is 1023d. 式 5 calculates the ADC output code based on the voltage input.

$$ADC\_CODE = \frac{VIN \times 2^{10}}{VREF} \quad (5)$$

This application example uses the 5-V VDD as the ADC reference. 式 6 calculates the ADC code for a 2.5-V input.

$$ADC\_CODE = \frac{2.5\,V \times 2^{10}}{5\,V} = 512d \quad (6)$$

表 8-2 shows the ADC code to temperature mapping used in this application example. An NTC resistor is used as the temperature sensor. Higher ADC codes correspond to a lower temperature.

表 8-2. Thermal Foldback Profile: ADC to Temperature

ADC CODE	TEMPERATURE
0x000	100°C
0x200	50°C
0x3FF	0°C

There are four X and Y points available to map the temperature (X points) to an output voltage (Y points). The voltage output is configured by a 10-bit DAC code. The maximum code is 1023d. 式 7 calculates the DAC code for a desired voltage output.

$$DAC\_CODE = \frac{VOUT \times 2^{10}}{VREF} \quad (7)$$

This application example uses the 5-V VDD as the DAC reference. 式 8 calculates the DAC code for a 1-V output.

$$DAC\_CODE = \frac{VOUT \times 2^{10}}{VREF} \quad (8)$$

表 8-3 shows the temperature to output voltage mapping used in this application example. The profile can have both negative and positive slopes.

表 8-3. Thermal Foldback Profile: Temperature to VOUT

TEMPERATURE	OUTPUT VOLTAGE (CODE)
20°C	4 V (0x320)
50°C	5 V (0x3FF)
75°C	3.4 V (0x2BC)
100°C	0 V (0x00)

Follow these guidelines to setup the registers on the AFE53902-Q1:

- Set the VREF/MODE pin low to enable the digital pins for programming mode.
- Stop the state machine before updating the application parameters by writing 0 to the STATE-MACHINE-CONFIG0 register.
- Set all of the application parameters shown in 表 8-4. These locations must be used to save the settings in the NVM.
- Configure the reference for both channels in the DAC-x-VOUT-CMP-CONFIG registers.
  - Configure channel 0 as an ADC input by setting the CMP-x-EN bit to 1.
- Power on the DAC and ADC channels in voltage mode using the COMMON-CONFIG register.
- Set the DEVICE-MODE-CONFIG register to 0x9000.
- Start the state machine by writing 0x3 to the STATE-MACHINE-CONFIG0.
- Trigger an NVM write by setting the NVM-PROG bit in the COMMON-TRIGGER register (0x20) to 1.

表 8-4. Application Parameters

REGISTER FIELD NAME	ADDRESS[FIELD]	ADDRESS LOCATION
X1-TEMPERATURE	0x20[10:1]	SRAM
Y1-TEMPERATURE	0x21[7:0]	SRAM
X2-TEMPERATURE	0x22[10:1]	SRAM
Y2-TEMPERATURE	0x23[7:0]	SRAM
X3-TEMPERATURE	0x24[10:1]	SRAM
Y3-TEMPERATURE	0x25[7:0]	SRAM
X1-OUTPUT	0x26[7:0]	SRAM
Y1-OUTPUT	0x27[9:0]	SRAM
X2-OUTPUT	0x28[7:0]	SRAM
Y2-OUTPUT	0x29[9:0]	SRAM
X3-OUTPUT	0x2A[7:0]	SRAM
Y3-OUTPUT	0x2B[9:0]	SRAM
X4-OUTPUT	0x2C[7:0]	SRAM
Y4-OUTPUT	0x2D[9:0]	SRAM
PWM-FREQUENCY	0x2E[11:7]	SRAM
DAC-0-VOUT-CMP-CONFIG	0x15[12:10][4:0]	Register
DAC-1-VOUT-CMP-CONFIG	0x03[12:10][4:0]	Register
COMMON-CONFIG	0x1F[15:0]	Register
DEVICE-MODE-CONFIG	0x25[15:0]	Register
STATE-MACHINE-CONFIG0	0x27[2:0]	Register

Only the bits listed in the address column of 表 8-4 are saved in NVM and used in the state machine. For example, only bits 12 to 10 and 4 to 0 are saved in NVM for the DAC-x-VOUT-CMP-CONFIG registers.

The pseudocode for this application example is as follows:

```
//SYNTAX: WRITE <REGISTER NAME(Hex Code)>, <MSB DATA>, <LSB DATA>
//Stop the state machine
WRITE STATE-MACHINE-CONFIG0(0x27), 0x00, 0x03
//Set the thermal foldback profile values
//The voltage output is a 10-bit value
WRITE X1-TEMPERATURE(SRAM 0x20), 0x00, 0x00
WRITE Y1-TEMPERATURE(SRAM 0x21), 0x00, 0x64
WRITE X2-TEMPERATURE(SRAM 0x22), 0x04, 0x00
WRITE Y2-TEMPERATURE(SRAM 0x23), 0x00, 0x32
WRITE X3-TEMPERATURE(SRAM 0x24), 0x07, 0xFF
WRITE Y3-TEMPERATURE(SRAM 0x25), 0x00, 0x00
WRITE X1-OUTPUT(SRAM 0x26), 0x00, 0x14
WRITE Y1-OUTPUT(SRAM 0x27), 0x03, 0x20
WRITE X2-OUTPUT(SRAM 0x28), 0x00, 0x32
WRITE Y2-OUTPUT(SRAM 0x29), 0x03, 0xFF
WRITE X3-OUTPUT(SRAM 0x2A), 0x00, 0x4B
WRITE Y3-OUTPUT(SRAM 0x2B), 0x02, 0xBC
WRITE X4-OUTPUT(SRAM 0x2C), 0x00, 0x64
WRITE Y4-OUTPUT(SRAM 0x2D), 0x00, 0x00
//Set the channel 0 reference to VDD, enable the comparator for ADC mode (this is the device
default)
WRITE DAC-0-VOUT-CMP-CONFIG(0x15), 0x04, 0x01
//Set channel 1 reference to VDD (this is the device default)
WRITE DAC-1-VOUT-CMP-CONFIG(0x03), 0x04, 0x00
//Power on the DAC and ADC channel
WRITE COMMON-CONFIG(0x1F), 0x03, 0xF9
//Set the device mode (this is the device default)
WRITE DEVICE-MODE-CONFIG(0x25), 0x90, 0x00
//Start the state machine
WRITE STATE-MACHINE-CONFIG0(0x27), 0x00, 0x03
//Save settings to NVM
WRITE COMMON-TRIGGER(0x20), 0x00, 0x02
```

8.2.1.3 Application Performance Plots

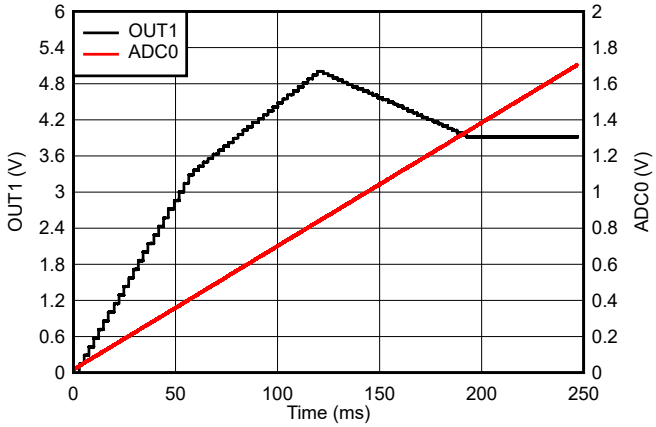
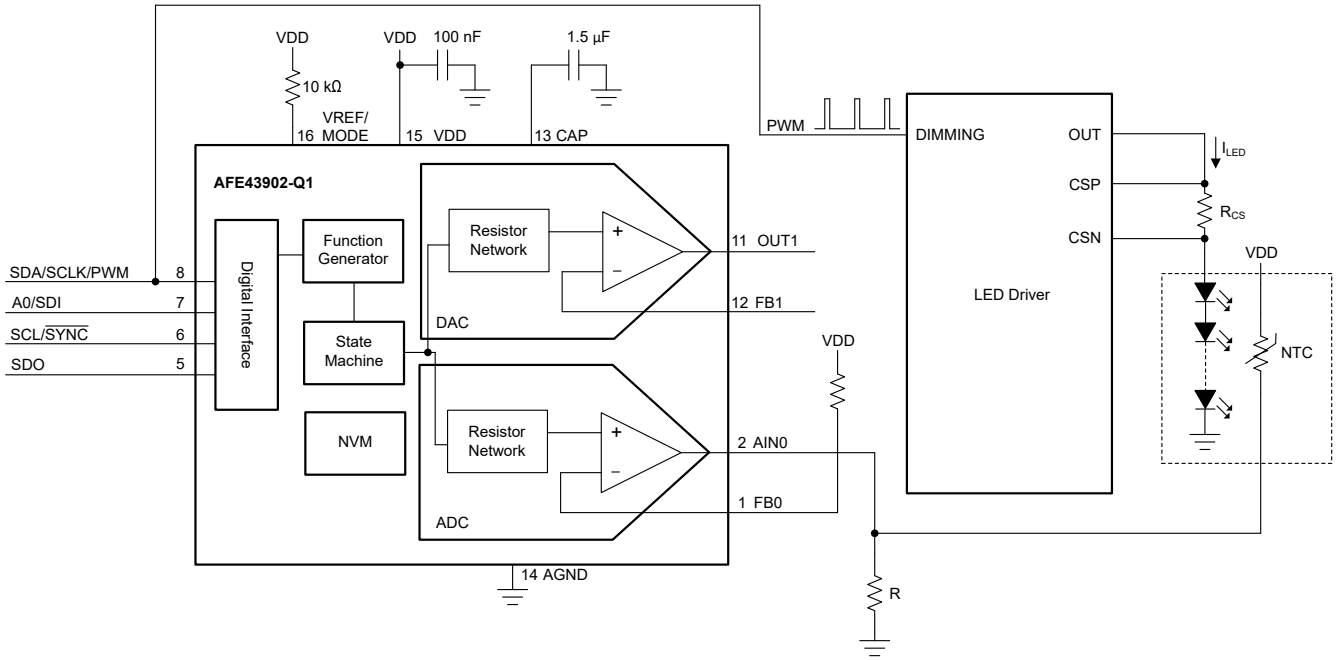


図 8-2. Voltage Output vs Temperature

8.2.2 Multislope Thermal Foldback Using the AFE43902-Q1 and PWM Output



Multislope Thermal Foldback Using the AFE43902-Q1 and PWM Output

図 8-3 shows how to connect the PWM output in PWM output mode.

8.2.2.1 Design Requirements

表 8-5. AFE43902-Q1 With PWM-Output Design Parameters

PARAMETER	VALUE
PWM frequency	1 kHz
Duty-cycle range	0% to 100%
Temperature range	0°C to 100°C

8.2.2.2 Detailed Design Procedure

The state machine converts a temperature input to a PWM output based on the values saved in the thermal foldback profile. The voltage output from the temperature sensor is read by the ADC and converted to an ADC code. There are three X and Y points available to map the ADC codes (X points) to a temperature (Y points). These points can be used to apply linearization to the temperature sensor output. The ADC is 10-bits, so the maximum code is 1023d. 式 9 calculates the ADC output code based on the voltage input.

$$ADC\_CODE = \frac{VIN \times 2^{10}}{VREF} \quad (9)$$

This application example uses the 5-V VDD as the ADC reference. 式 10 calculates the ADC code for a 2.5-V input.

$$ADC\_CODE = \frac{2.5\,V \times 2^{10}}{5\,V} = 512d \quad (10)$$

表 8-6 shows the ADC code to temperature mapping used in this application example. An NTC resistor is used as the temperature sensor. Higher ADC codes correspond to a lower temperature.

表 8-6. Thermal Foldback Profile: ADC to Temperature

ADC CODE	TEMPERATURE
0x000	100°C
0x200	50°C
0x3FF	0°C

The PWM frequency is set in the PWM-FREQUENCY SRAM location (SRAM: 0x2E). 表 7-1 defines the codes for each available frequency. There are four X and Y points available to map the temperature (X points) to an output duty cycle (Y points). The PWM duty-cycle output is configured by a 7-bit code. The maximum code is 127d. 式 11 calculates the duty-cycle:

$$DUTY\_CYCLE\_CODE = \frac{Duty\_Cycle\left(\%\right) \times 2^7}{100\%} \tag{11}$$

For a 50% duty cycle, 式 11 calculates the duty-cycle code as 64d.

注

A duty-cycle code of 127d sets the PWM duty cycle to 100% which does not follow 式 11. 表 7-2 provides the details of this exception.

表 8-7 shows the temperature to output duty cycle mapping used in this application example. The profile can have both negative and positive slopes.

表 8-7. Thermal Foldback Profile: Temperature to PWM

TEMPERATURE	OUTPUT DUTY CYCLE (CODE)
20°C	78% (0x64)
50°C	100% (0x7F)
75°C	63% (0x51)
100°C	0% (0x00)

Follow these guidelines to setup the registers on the AFE43902-Q1:

- Set the VREF/MODE pin low to enable the digital pins for programming mode.
- Stop the state machine before updating the application parameters by writing 0 to the STATE-MACHINE-CONFIG0 register.
- If the PWM generator is already running, the PWM generator needs to be stopped before any changes to the PWM frequency take effect. Write a 0 to the START-FUNCTION bit in the COMMON-PWM-TRIG register (0x21) to stop the PWM generator. The PWM generator is automatically started when the state machine is enabled.
- Set all of the application parameters shown in 表 8-8. These locations must be used to save the settings in the NVM. For example, the DAC register location for the PWM-FREQUENCY are not mapped to the NVM and is not saved when an NVM write is triggered.
- Configure the reference for both channels in the DAC-x-VOUT-CMP-CONFIG registers.
  - Configure channel 0 as an ADC input by setting the CMP-x-EN bit to 1.
- Power on the ADC channel using the COMMON-CONFIG register.
- Set the DEVICE-MODE-CONFIG register to 0x9000.
- Start the state machine by writing 0x3 to the STATE-MACHINE-CONFIG0.
- Trigger an NVM write by setting the NVM-PROG bit in the COMMON-TRIGGER register (0x20) to 1.
- Set the VREF/MODE pin high to enable the digital pins for standalone mode. This setting is required to see the PWM output on the digital pin.

表 8-8. Application Parameters

REGISTER FIELD NAME	ADDRESS[FIELD]	ADDRESS LOCATION
X1-TEMPERATURE	0x20[10:1]	SRAM
Y1-TEMPERATURE	0x21[7:0]	SRAM
X2-TEMPERATURE	0x22[10:1]	SRAM
Y2-TEMPERATURE	0x23[7:0]	SRAM
X3-TEMPERATURE	0x24[10:1]	SRAM
Y3-TEMPERATURE	0x25[7:0]	SRAM
X1-OUTPUT	0x26[7:0]	SRAM
Y1-OUTPUT	0x27[6:0]	SRAM
X2-OUTPUT	0x28[7:0]	SRAM
Y2-OUTPUT	0x29[6:0]	SRAM
X3-OUTPUT	0x2A[7:0]	SRAM
Y3-OUTPUT	0x2B[6:0]	SRAM
X4-OUTPUT	0x2C[7:0]	SRAM
Y4-OUTPUT	0x2D[6:0]	SRAM
PWM-FREQUENCY	0x2E[11:7]	SRAM
DAC-0-VOUT-CMP-CONFIG	0x15[12:10][4:0]	Register
DAC-1-VOUT-CMP-CONFIG	0x03[12:10][4:0]	Register
COMMON-CONFIG	0x1F[15:0]	Register
DEVICE-MODE-CONFIG	0x25[15:0]	Register
STATE-MACHINE-CONFIG0	0x27[2:0]	Register

Only the bits listed in the address column of 表 8-8 are saved in NVM and used in the state machine. For example, only bits 12 to 10 and 4 to 0 are saved in NVM for the DAC-x-VOUT-CMP-CONFIG registers.

The pseudocode for this application example is as follows:

```
//SYNTAX: WRITE <REGISTER NAME(Hex Code)>, <MSB DATA>, <LSB DATA>
//Stop the state machine
WRITE STATE-MACHINE-CONFIG0(0x27), 0x00, 0x03
//Stop the PWM generator
WRITE COMMON-PWM-TRIG(0x21), 0x00, 0x00
//Set the PWM frequncy (this is the device default)
WRITE PWM-FREQUENCY(SRAM 0x2E), 0x05, 0x80
//Set the thermal foldback profile values
//The PWM duty cycle is a 7-bit value
WRITE X1-TEMPERATURE(SRAM 0x20), 0x00, 0x00
WRITE Y1-TEMPERATURE(SRAM 0x21), 0x00, 0x64
WRITE X2-TEMPERATURE(SRAM 0x22), 0x04, 0x00
WRITE Y2-TEMPERATURE(SRAM 0x23), 0x00, 0x32
WRITE X3-TEMPERATURE(SRAM 0x24), 0x07, 0xFF
WRITE Y3-TEMPERATURE(SRAM 0x25), 0x00, 0x00
WRITE X1-OUTPUT(SRAM 0x26), 0x00, 0x14
WRITE Y1-OUTPUT(SRAM 0x27), 0x03, 0x64
WRITE X2-OUTPUT(SRAM 0x28), 0x00, 0x32
WRITE Y2-OUTPUT(SRAM 0x29), 0x03, 0x7F
WRITE X3-OUTPUT(SRAM 0x2A), 0x00, 0x4B
WRITE Y3-OUTPUT(SRAM 0x2B), 0x02, 0x51
WRITE X4-OUTPUT(SRAM 0x2C), 0x00, 0x64
WRITE Y4-OUTPUT(SRAM 0x2D), 0x00, 0x00
//Set the channel 0 reference to VDD, enable the comparator for ADC mode (this is the device
default)
WRITE DAC-0-VOUT-CMP-CONFIG(0x15), 0x04, 0x01
//Power on the ADC channel
WRITE COMMON-CONFIG(0x1F), 0x03, 0xFF
//Set the device mode (this is the device default)
WRITE DEVICE-MODE-CONFIG(0x25), 0x90, 0x00
//Start the state machine
WRITE STATE-MACHINE-CONFIG(0x27), 0x00, 0x03
//Save settings to NVM
WRITE COMMON-TRIGGER(0x20), 0x00, 0x02
```

8.2.2.3 Application Performance Plots

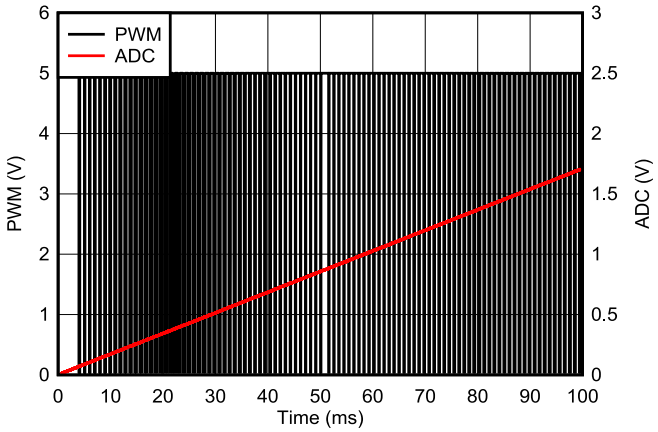


図 8-3. PWM Output vs Temperature

8.3 Power Supply Recommendations

The AFEx3902-Q1 do not require specific power-supply sequencing. These devices require a single power supply, V_{DD}. However, make sure the external voltage reference is applied after VDD powers on. Use a 0.1-µF decoupling capacitor for the V_{DD} pin. Use a bypass capacitor with a value approximately 1.5 µF for the CAP pin.

8.4 Layout

8.4.1 Layout Guidelines

The AFEx3902-Q1 pin configuration separates the analog, digital, and power pins for an optimized layout. For signal integrity, separate the digital and analog traces, and place decoupling capacitors close to the device pins.

8.4.2 Layout Example

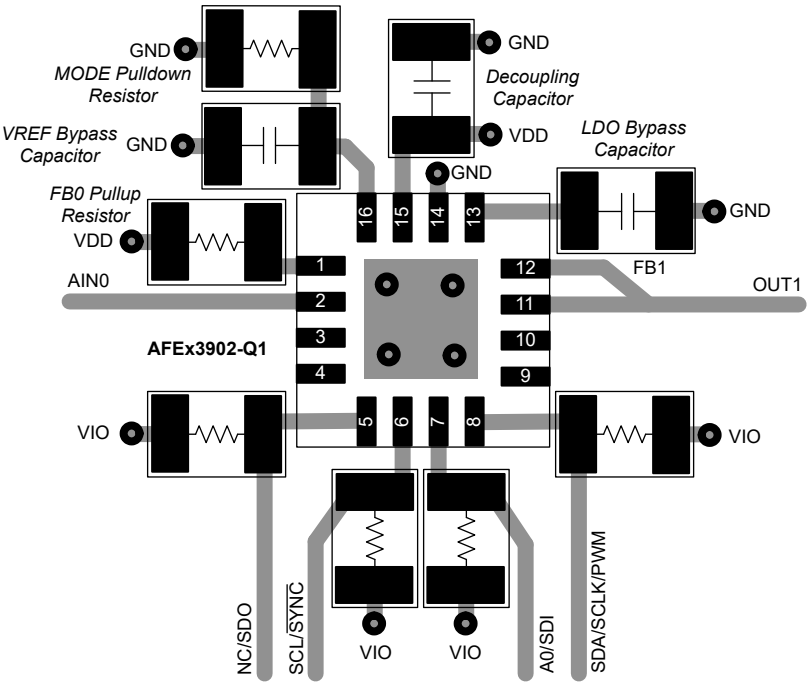


図 8-4. Layout Example

Note: The ground and power planes have been omitted for clarity. Connect the thermal pad to ground.

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

9.2 サポート・リソース

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9.3 Trademarks

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9.4 静電気放電に関する注意事項

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.5 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AFE43902RTERQ1	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A4902Q
AFE43902RTERQ1.A	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A4902Q
AFE53902RTERQ1	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A5902Q
AFE53902RTERQ1.A	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A5902Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

GENERIC PACKAGE VIEW

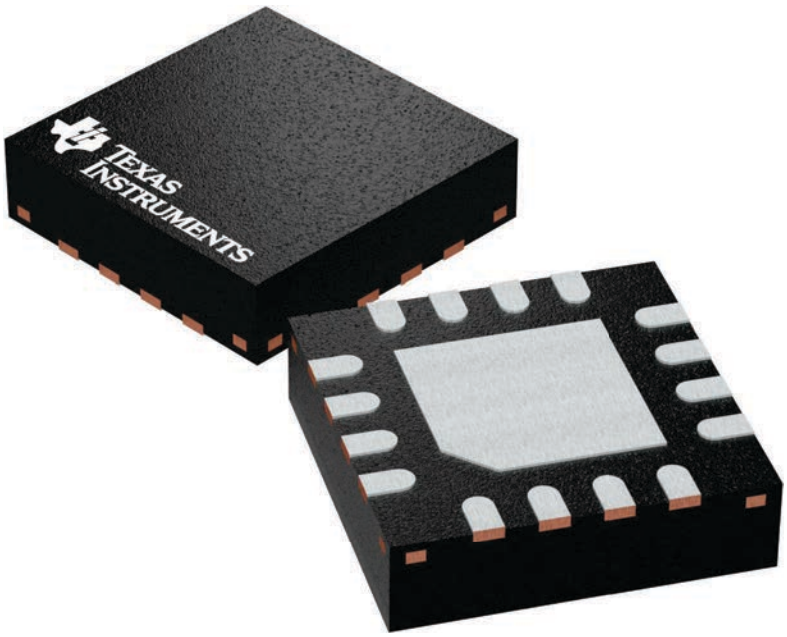
RTE 16

WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

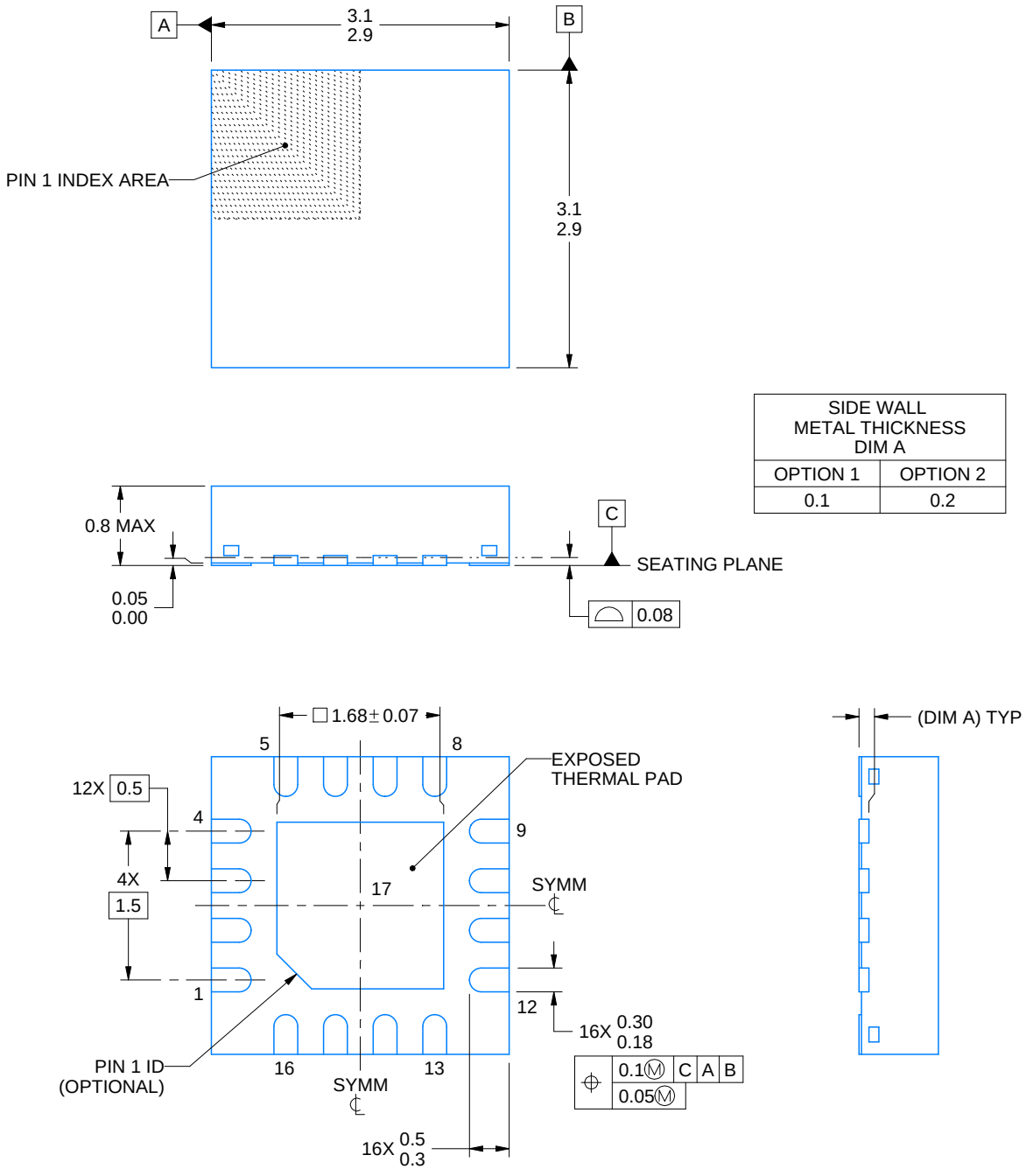


RTE0016C

PACKAGE OUTLINE

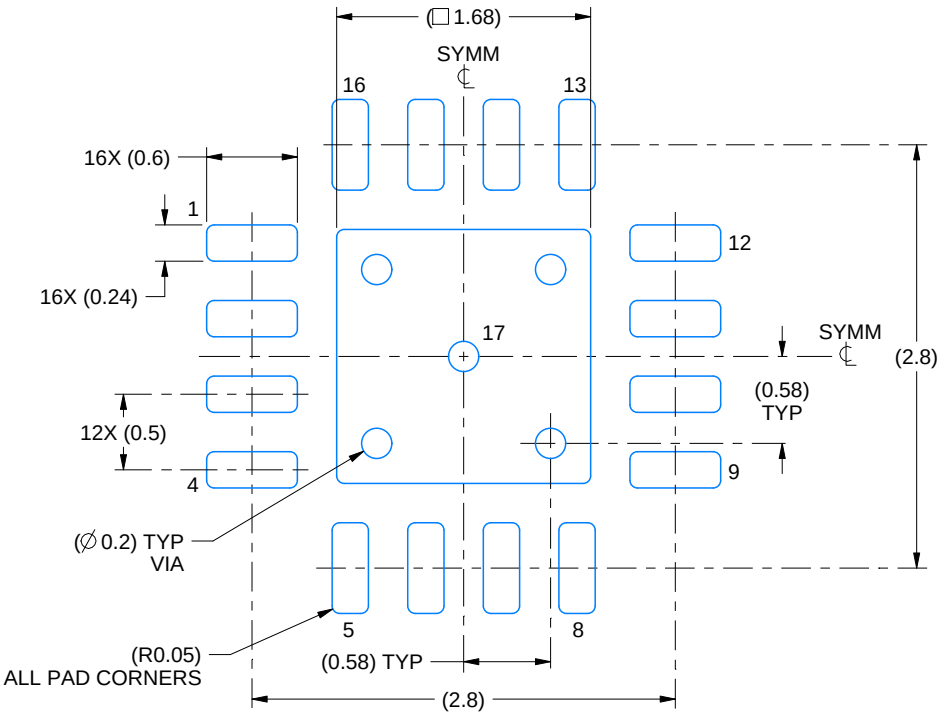
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

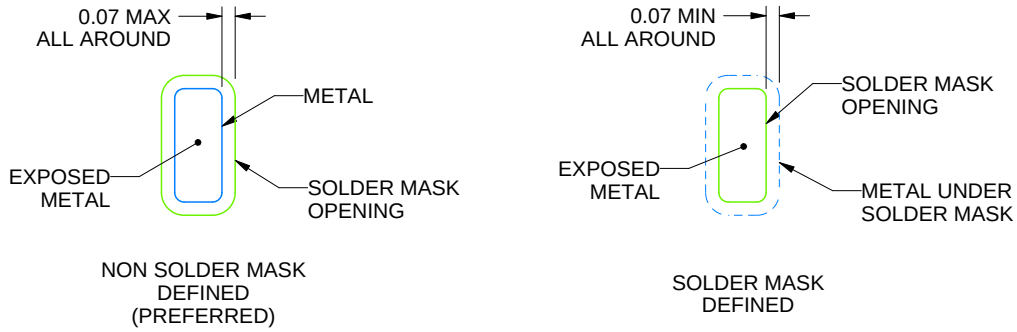


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

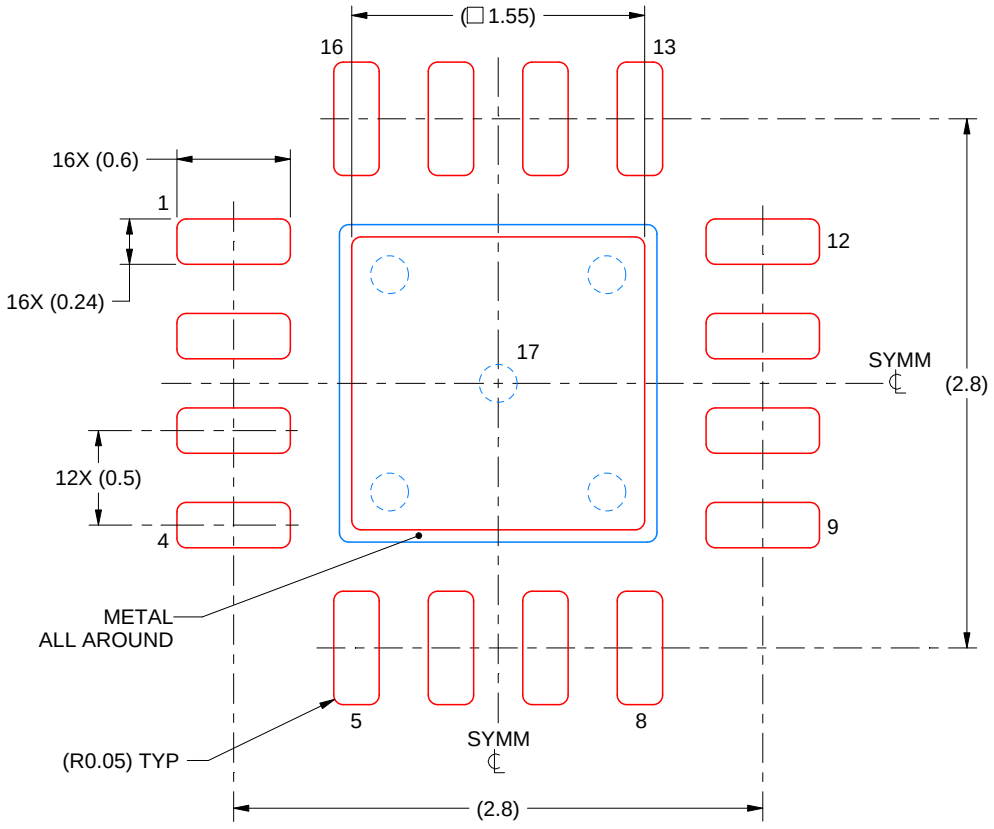


SOLDER MASK DETAILS

4219117/B 04/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219117/B 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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