TEXAS INSTRUMENTS
BQ25120, BQ25121
JAJSD89C – AUGUST 2015 – REVISED SEPTEMBER 2016

bq2512x ウェアラブルおよびIoT向け700nA低I_Q高度統合バッテリ充電管理ソリューション

1 特長

- **次の充電までのシステム動作時間が増大**
  - 300mAの可変降圧レギュレータ (デフォルト1.8V)
  - 降圧コンバータが有効な状態(無負荷)でのIq: 700nA (標準値)
  - 可変負荷スイッチまたは100mA LDO出力(デフォルトでは負荷スイッチ)
  - 最大300mAの充電電流により高速充電
  - 精度0.5%のバッテリ電圧レギュレーション(3.6V～4.65Vまで10mV刻みで設定可能)
  - 終了電流を最低500µAに設定可能
  - 単純な電圧ベースのバッテリ監視
- **占有面積の小さい、高度に統合されたソリューション**
  - 2.5mm×2.5mmのWCSPパッケージと6個の外付け部品により、最小のソリューションを構築可能
  - プッシュボタンによるウェークアップとリセット、タイマを設定可能
  - システム電源およびバッテリ充電用の電力パスの管理
  - 電力パス管理により50nA未満のシップ・モード・バッテリ静止電流を実現し、保管寿命を延長
  - バッテリ充電は3.4V～5.5V_{IN}で動作(5.5VのOVP / 20V耐圧)
  - 入力電流制限、充電電流、終了電流、およびステータス出力用の専用ピン
- **I^2C通信制御**
  - 充電電圧および電流
  - 終了スレッショルド
  - 入力電流制限
  - VINDPMスレッショルド
  - タイマ・オプション
  - 負荷スイッチ制御
  - フォルトおよびステータスの割り込みの制御
  - システム出力電圧の変更
  - LDO出力電圧の変更

2 アプリケーション

- **スマート・ウォッチ、その他ウェアラブル・デバイス**
- **フィットネス用アクセサリ**
- **健康監視用医療アクセサリ**
- **充電可能な玩具**

3 概要

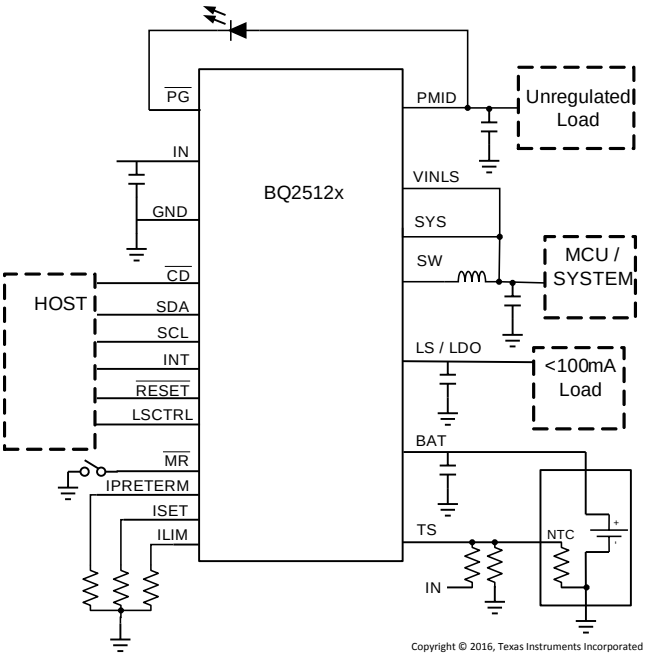
bq2512xは高度に統合されたバッテリ充電管理ICであり、ウェアラブル・デバイスでよく使われるリニア充電器、レギュレートされた出力、負荷スイッチ、タイマ付きマニュアル・リセット、バッテリ電圧モニタといった機能を内蔵しています。内蔵の降圧コンバータは高効率の低I_Qスイッチャーで、DCS制御を使用して、最小10µAの負荷電流まで軽負荷時の効率を維持します。動作時およびシャットダウン時の静止電流が小さいため、最大のバッテリ駆動時間が得られます。このデバイスは、5mA～300mAの充電電流をサポートします。入力電流制限、充電電流、降圧コンバータの出力電圧、LDO出力電圧、その他のパラメータは、I^2Cインターフェイスからプログラム可能です。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
BQ2512x	DSBGA (25)	2.50mm×2.50mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

概略回路図



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

5 概要（続き）

バッテリは、標準のリチウムイオン充電プロファイルを使用して、プリチャージ、定電流、定電圧の3つのフェーズで充電されます。電圧ベースのJEITA互換バッテリパック・サーミスタ監視入力(TS)が含まれており、バッテリの温度を監視し、バッテリが充電中に安全な温度範囲を逸脱しないよう、充電パラメータを自動的に変更します。充電器は5V USB入力に最適化されており、20V耐圧で、ライン過渡電圧に耐えられます。降圧コンバータは入力またはバッテリから駆動されます。バッテリのみのモードでは、デバイスは最高4.65Vのバッテリから駆動できます。

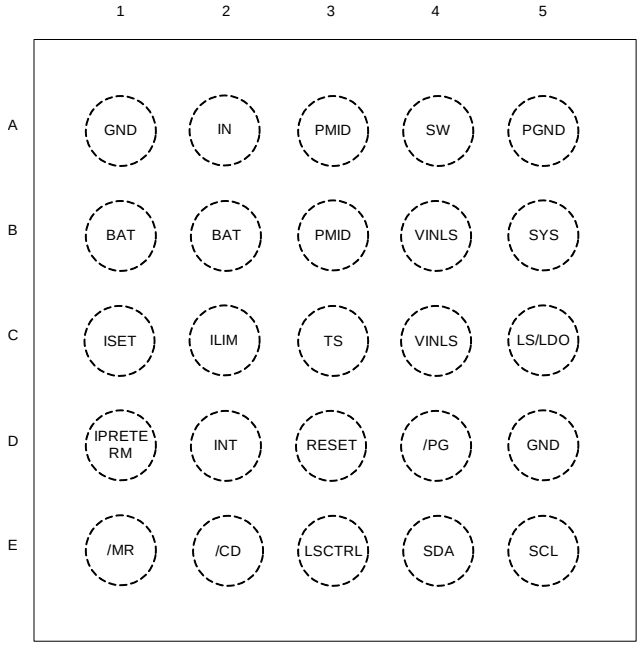
可変の負荷スイッチにより、使用頻度の低いデバイスを切断し、システムを最適化できます。タイマ付きのマニュアル・リセットにより、ウェークアップおよびリセットを最適化する各種の構成オプションを使用できます。単純な電圧ベースのモニタから、バッテリ・レベル情報がプログラミングした$V_{(BATREG)}$の60%から100%まで2%刻みでホストに提供されます。

6 Device Comparison Table

PART NUMBER	VINDPM	DEFAULT SYS OUTPUT	DEFAULT LDO OUTPUT	DEFAULT VBERG	DEFAULT CHARGE CURRENT	DEFAULT TERMINATION CURRENT	DEFAULT SHIP MODE
BQ25120	Enabled	1.8 V	Load Switch	4.2 V	10 mA	2 mA	Off
BQ25121	Enabled	2.5 V	Load Switch	4.2 V	10 mA	2 mA	Off

7 Pin Configuration and Functions

YFP Package
25-Pin (DSBGA)
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
IN	A2	I	DC Input Power Supply. IN is connected to the external DC supply. Bypass IN to GND with at least 1 µF of capacitance using a ceramic capacitor.
PMID	A3, B3	I/O	High Side Bypass Connection. Connect at least 3µF of ceramic capacitance with DC bias derating from PMID to GND as close to the PMID and GND pins as possible.
GND	A1, D5		Ground connection. Connect to the ground plane of the circuit.
PGND	A5		Power ground connection. Connect to the ground plane of the circuit. Connect the output filter cap from the buck converter to this ground as shown in the layout example.
$\overline{CD}$	E2	I	Chip Disable. Drive $\overline{CD}$ low to place the part in High-Z mode with battery only present, or enable charging when V_{IN} is valid. Drive $\overline{CD}$ high for Active Battery mode when battery only is present, and disable charge when V_{IN} is present. $\overline{CD}$ is pulled low internally with 900 kΩ.
SDA	E4	I/O	I^2C Interface Data. Connect SDA to the logic rail through a 10-kΩ resistor.
SCL	E5	I	I^2C Interface Clock. Connect SCL to the logic rail through a 10-kΩ resistor.
ILIM	C2	I	Adjustable Input Current Limit Programming. Connect a resistor from ILIM to GND to program the input current limit. The input current includes the system load and the battery charge current. Connect ILIM to GND to set the input current limit to the internal default threshold. ILIM can also be updated through I^2C.
LSCTRL	E3	I	Load Switch and LDO Control Input. Pull high to enable the LS/LDO output, pull low to disable the LS/LDO output.
ISET	C1	I	Fast-Charge Current Programming Input. Connect a resistor from ISET to GND to program the fast-charge current level. Connect a resistor from ISET to GND to set the charge current to the internal default. ISET can also be updated through I^2C. While charging, the voltage at ISET reflects the actual charging current and can be used to monitor charge current if an ISET resistor is present and the device is not in host mode.
IPRETERM	D1	I	Termination current programming input. Connect a 0-Ω to 10-kΩ resistor from IPRETERM to GND to program the termination current between 5% and 20% of the charge current. The pre-charge current is the same as the termination current setting. Connect IPRETERM to GND to set the termination current to the internal default threshold. IPRETERM can also be updated through I^2C.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
INT	D2	O	Status Output. INT is an open-drain output that signals charging status and fault interrupts. INT pulls low during charging. INT is high impedance when charging is complete, disabled, or the charger is in high impedance mode. When a fault occurs, a 128µs pulse is sent out as an interrupt for the host. INT charge indicator function is enabled/disabled using the EN_INT bit in the control register. Connect INT to a logic rail using an LED for visual indication of charge status or through a 100kΩ resistor to communicate with the host processor.
$\overline{PG}$	D4	O	Open-drain Power Good status indication output. $\overline{PG}$ pulls to GND when V_{IN} is above $V_{(BAT)}$ + V_{SLP} and less that V_{OVP}. $\overline{PG}$ is high-impedance when the input power is not within specified limits. Connect $\overline{PG}$ to the desired logic voltage rail using a 1kΩ to 100kΩ resistor, or use with an LED for visual indication. $\overline{PG}$ can also be configured as a push-button voltage shifted output (MRS) in the registers, where the output of the $\overline{PG}$ pin reflects the status of the $\overline{MR}$ input, but pulled up to the desired logic voltage rail using a 1kΩ to 100kΩ resistor.
$\overline{RESET}$	D3	O	Reset Output. $\overline{RESET}$ is an open drain active low output that goes low when $\overline{MR}$ is held low for longer than t_{RESET}, which is configurable by the MRRESET registers. $\overline{RESET}$ is deasserted after the t_{RESET_D}, typically 400ms.
$\overline{MR}$	E1	I	Manual Reset Input. $\overline{MR}$ is a push-button input that must be held low for greater than t_{RESET} to assert the reset output. If $\overline{MR}$ is pressed for a shorter period, there are two programmable timer events, t_{WAKE1} and t_{WAKE2}, that trigger an interrupt to the host. The $\overline{MR}$ input can also be used to bring the device out of Ship mode.
SW	A4	O	Inductor Connection. Connect to the switched side of the external inductor.
SYS	B5	I	System Voltage Sense Connection. Connect SYS to the system output at the output bulk capacitors. Bypass SYS locally with at least 4.7 µF of effective ceramic capacitance.
LS/LDO	C5	O	Load Switch or LDO output. Connect 1 µF of effective ceramic capacitance to this pin to assure stability. Be sure to account for capacitance bias voltage derating when selecting the capacitor.
VINLS	B4, C4	I	Input to the Load Switch / LDO output. Connect 1 µF of effective ceramic capacitance from this pin to GND.
BAT	B1, B2	I/O	Battery Connection. Connect to the positive terminal of the battery. Bypass BAT to GND with at least 1 µF of ceramic capacitance.
TS	C3	I	Battery Pack NTC Monitor. Connect TS to the center tap of a resistor divider from VIN to GND. The NTC is connected from TS to GND. The TS function provides four thresholds for JEITA compatibility. TS faults are reported by the I^2C interface during charge mode.

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
Input voltage	IN	wrt GND	–0.3	20	V
	PMID, VINLS	wrt GND	–0.3	7.7	V
	$\overline{CD}$, SDA, SCL, ILIM, ISET, IPRETERM, LSCTRL, INT, $\overline{RESET}$, TS	wrt GND	–0.3	5.5	V
Output voltage	SYS			3.6	V
Input current	IN			400	mA
Sink current	INT			10	mA
Sink/Source Current	$\overline{RESET}$			10	mA
Output Voltage Continuos	SW		–0.7	7.7	V
Output Current Continuous	SW			400	mA
	SYS, BAT			300	mA
Current	LS/LDO			150	mA
BAT Operating Voltage	VBAT, MR,			6.6	V
Junction Temperature			–40	125	°C
Storage Temperature, T_{stg}				300	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	IN voltage range	3.4	5	20	V
	IN operating voltage range, recommended	3.4	5	5.5	
$V_{(BAT)}$	$V_{(BAT)}$ operating voltage range			5.5 (1)	V
$V_{(VINLS)}$	VINLS voltage range for Load Switch	0.8		5.5 (2)	V
$V_{(VINLS)}$	VINLS voltage range for LDO	2.2		5.5	V
I_{IN}	Input Current, IN input			400	mA
$I_{(SW)}$	Output Current from SW, DC			300	mA
$I_{(PMID)}$	Output Current from PMID, DC			300	mA
ILS/LDO	Output Current from LS/LDO			100	mA
$I_{(BAT)}$, $I_{(SYS)}$	Charging and discharging using internal battery FET			300	mA
T_J	Operating junction temperature range	–40		125	°C

(1) Any voltage greater than shown should be a transient event.
(2) These inputs will support 6.6 V for less than 10% of the lifetime at $V_{(BAT)}$ or VIN, with a reduced current and/or performance.

8.4 Thermal Information

THERMAL METRIC[1]		bq2512x YFP (DSBGA) 25 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	60	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	12.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	12.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

8.5 Electrical Characteristics

Circuit of 図 1, $V_{(UVLO)} < V_{IN} < V_{(OVP)}$ and $V_{IN} > V_{(BAT)} + V_{(SLP)}$, T_J = –40°C to 85°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CURRENTS						
I_{IN}	Supply Current for Control	$V_{(UVLO)} < V_{IN} < V_{(OVP)}$ and $V_{IN} > V_{(BAT)} + V_{(SLP)}$ PWM Switching, –40°C < T_J < 85°C		1		mA
		$V_{(UVLO)} < V_{IN} < V_{(OVP)}$ and $V_{IN} > V_{(BAT)} + V_{(SLP)}$ PWM NOT Switching			3	mA
		0°C < T_J < 85°C, V_{IN} = 5 V, Charge Disabled			1.5	mA
$I_{(BAT\_HIZ)}$	Battery discharge current in High Impedance Mode	0°C < T_J < 60°C, V_{IN} = 0 V, High-Z Mode, PWM Not Switching, $V_{(BUVLO)} < V_{(BAT)}$ < 4.65 V		0.7	1.2	µA
		0°C < T_J < 60°C, V_{IN} = 0 V, High-Z Mode, PWM Not Switching, $V_{(BUVLO)} < V_{(BAT)}$ < 6.6 V		0.9	1.5	µA
		0°C < T_J < 60°C, V_{IN} = 0 V or floating, High-Z Mode, PWM Switching, No Load		0.75	3.5	µA
		0°C < T_J < 85°C, V_{IN} = 0 V, High-Z Mode, PWM Switching, LSLDO enabled		1.35	4.25	µA
$I_{(BAT\_ACTIVE)}$	Battery discharge current in Active Battery Mode	0°C < T_J < 85°C, V_{IN} = 0 V, Active Battery Mode, PWM Switching, LSLDO enabled, I2C Enabled, $V_{(BUVLO)} < V_{(BAT)}$ < 4.65 V		6.8	12	µA
		0°C < T_J < 85°C, 0 < V_{IN} < $V_{IN(UVLO)}$, Active Battery Mode, PWM Switching, LSLDO disabled, I2C Enabled, $\overline{CD}$ = Low, $V_{(BUVLO)} < V_{(BAT)}$ < 4.65 V		6.2	11	µA
$I_{(BAT\_SHIP)}$	Battery discharge current in Ship Mode	0°C < T_J < 85°C, V_{IN} = 0 V, Ship Mode		2	150	nA
POWER-PATH MANAGEMENT and INPUT CURRENT LIMIT						
$V_{DO(IN-PMID)}$	$V_{IN} – V_{(PMID)}$	V_{IN} = 5 V, I_{IN} = 300 mA		125	170	mV
$V_{DO(BAT-PMID)}$	$V_{(BAT)} – V_{(PMID)}$	V_{IN} = 0 V, $V_{(BAT)}$ > 3 V, I_{ff} = 400 mA		120	160	mV
$V_{(BSUP1)}$	Enter supplement mode threshold	$V_{(BAT)} > V_{(BUVLO)}$		$V_{(PMID)} < V_{(BAT)} – 25$ mV		V
$V_{(BSUP2)}$	Exit supplement mode threshold	$V_{(BAT)} > V_{(BUVLO)}$		$V_{(PMID)} < V_{(BAT)} –$ 5mV		V
$I_{(BAT\_OCP)}$	Current Limit, Discharge Mode	$V_{(BAT)} > V_{(BUVLO)}$	0.85	1.15	1.35	A
$I_{(ILIM)}$	Input Current Limit	Programmable Range, 50-mA steps	50		400	mA
	Maximum Input Current using ILIM			$K_{(ILIM)} / R_{(ILIM)}$		
	I_{ILIM} accuracy I_{ILIM} accuracy	50 mA to 100 mA	–12%		12%	
		100 mA to 400 mA	–5%		5%	
$K_{(ILIM)}$	Maximum input current factor	$I_{(ILIM)}$ = 50 mA to 100 mA	175	200	225	AΩ
		$I_{(ILIM)}$ = 100 mA to 400 mA	190	200	210	AΩ
$V_{IN(DPM)}$	Input voltage threshold when input current is reduced	Programmable Range using $V_{IN(DPM)}$ Registers. Can be disabled using $V_{IN(DPM\_ON)}$	4.2		4.9	V
	V_{IN_DPM} threshold accuracy		–3%		3%	
BATTERY CHARGER						
$V_{D(PPM)}$	PMID voltage threshold when charge current is reduced	Above $V_{(BATREG)}$		0.2		V
$R_{ON(BAT-PMID)}$	Internal Battery Charger MOSFET on-resistance	Measured from BAT to PMID, $V_{(BAT)}$ = 4.35 V, High-Z mode		300	400	mΩ
$V_{(BATREG)}$	Charge Voltage	Operating in voltage regulation, Programmable Range, 10-mV steps	3.6		4.65	V
	Voltage Regulation Accuracy	T_J = 25°C	–0.5%		0.5%	
		T_J = 0°C to 85°C	–0.5%		0.5%	

Electrical Characteristics (continued)

Circuit of 図 1, $V_{(UVLO)} < V_{IN} < V_{(OVP)}$ and $V_{IN} > V_{(BAT)} + V_{(SLP)}$, T_J = –40°C to 85°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(CHARGE)}$	Fast Charge Current Range	$V_{(BATUVLO)} < V_{(BAT)} < V_{(BATREG)}$	5		300	mA
	Fast Charge Current using ISET			$K_{(ISET)}$ / $R_{(ISET)}$		A
	Fast Charge Current Accuracy		–5%		5%	
$K_{(ISET)}$	Fast Charge Current Factor	5 mA > $I_{(CHARGE)}$ > 300 mA	190	200	210	AΩ
$I_{(TERM)}$	Termination charge current	Termination current programmable range over I^2C	0.5		37	mA
	Termination Current using IPRETERM	$I_{(CHARGE)}$ < 300 mA, $R_{(ITERM)}$ = 15 kΩ		5		% of I_{SET}
		$I_{(CHARGE)}$ < 300 mA, $R_{(ITERM)}$ = 4.99 kΩ		10		% of I_{SET}
		$I_{(CHARGE)}$ < 300 mA, $R_{(ITERM)}$ = 1.65 kΩ		15		% of I_{SET}
		$I_{(CHARGE)}$ < 300 mA, $R_{(ITERM)}$ = 549 Ω		20		% of I_{SET}
	Accuracy	$I_{(TERM)}$ > 4 mA	–10%		10%	
$t_{DGL(TERM)}$	TERM deglitch time	Both rising and falling, 2-mV over-drive, t_{RISE}, t_{FALL} = 100 ns		64		ms
$I_{(PRE\_CHARGE)}$	Pre-charge current	Pre-charge current programmable range over I^2C	0.5		37	mA
	Pre-charge Current using $I_{PRETERM}$			$I_{(TERM)}$		A
	Accuracy		–10%		10%	
$V_{(RCH)}$	Recharge threshold voltage	Below $V_{(BATREG)}$	100	120	140	mV
$t_{DGL(RCHG)}$	Recharge threshold deglitch time	t_{FALL} = 100 ns typ, $V_{(RCH)}$ falling		32		ms
SYS OUTPUT						
$R_{DS(ON\_HS)}$		PMID = 3.6 V, $I_{(SYS)}$ = 50 mA		675	850	mΩ
$R_{DS(ON\_LS)}$		PMID = 3.6 V, $I_{(SYS)}$ = 50 mA		300	475	mΩ
$R_{DS(CH\_SYS)}$	MOSFET on-resistance for SYS discharge	V_IN = 3.6 V, I_{OUT} = –10 mA into V_{OUT} pin		22	40	Ω
$I_{(LIMF)}$	SW Current limit HS	2.2 V < $V_{(PMID)}$ < 5.5 V	525	600	675	mA
	SW Current limit LS	2.2 V < $V_{(PMID)}$ < 5.5 V	525	700	850	mA
$I_{(LIM\_SS)}$	PMOS switch current limit during softstart	Current limit is reduced during softstart	80	130	200	mA
V_{SYS}	SYS Output Voltage Range	Programmable range, 100 mV Steps	1.1		3.3	V
	Output Voltage Accuracy	V_{IN} = 5 V, PFM mode, I_{OUT} = 10 mA, $V_{(SYS)}$ = 1.8 V	–2.5%	0	2.5%	
	DC Output Voltage Load Regulation in PWM mode	V_{OUT} = 2 V, over load range		0.01		%/mA
	DC Output Voltage Line Regulation in PWM mode	V_{OUT} = 2 V, I_{OUT} = 100 mA, over V_{IN} range		0.01		%/V
LS/LDO OUTPUT						
$V_{IN(LS)}$	Input voltage range for LS/LDO	Load Switch Mode	0.8		6.6	V
	Input voltage range for LS/LDO	LDO Mode	2.2		6.6	V
V_{OUT}	DC output accuracy	T_J = 25°C	–2%	±1%	2%	
		Over V_{IN}, I_{OUT}, temperature	–3%	±2%	3%	
V_{LDO}	Output range for LS/LDO	Programmable Range, 0.1 V steps	0.8		3.3	V
ΔV_{OUT} / ΔV_{IN}	DC Line regulation	$V_{OUT(NOM)}$ + 0.5 V < V_{IN} < 6.6 V, I_{OUT} = 5 mA	–1%		1%	
	DC Load regulation	0 mA < I_{OUT} < 100 mA	–1%		1%	
	Load Transient	2 µA to 100 mA, VOUT = 1. 8 V	–120		60	mV
$R_{DS(ON\_LDO)}$	FET Rdson	$V_{(VINLS)}$ = 3.6 V		460	600	mΩ
$R_{(DSCH\_LSLDO)}$	MOSFET on-resistance for LS/LDO discharge	1.7 V < $V_{(VINLS)}$ < 6.6 V, I_{LOAD} = –10 mA		30		Ω

Electrical Characteristics (continued)

Circuit of 図 1, $V_{(UVLO)} < V_{IN} < V_{(OVP)}$ and $V_{IN} > V_{(BAT)} + V_{(SLP)}$, T_J = –40°C to 85°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETERS		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{(OCL\_LDO)}$	Output Current Limit – LDO	$V_{LS/LDO}$ = 0.9 x $V_{LS/LDO(NOM)}$		275	365	450	mA
$I_{(LS/LDO)}$	Output Current	$V_{(VINLS)}$ = 3.6 V, V_{LSLDO} = 3.3 V				100	mA
		$V_{(VINLS)}$ = 3.3 V, V_{LSLDO} = 0.8 V				100	mA
		$V_{(VINLS)}$ = 2.2 V, V_{LSLDO} = 0.8 V				10	mA
$I_{IN(LDO)}$	Quiescent current for VINLS in LDO mode				0.9		µA
	OFF-state supply current				0.25		µA
$V_{IH(LSCTRL)}$	High-level input voltage for LSCTRL	1.15 V > $V_{(VINLS)}$ > 6.6 V		0.75 x $V_{(SYS)}$		6.6	V
$V_{IL(LSCTRL)}$	Low-level input voltage for LSCTRL	1.15 V > $V_{(VINLS)}$ > 6.6 V				0.25 x $V_{(SYS)}$	V
PUSHBUTTON TIMER ($\overline{MR}$)							
V_{IL}	Low-level input voltage	V_{BAT} > V_{BUVLO}				0.3	V
R_{PU}	Internal pull-up resistance				120		kΩ
VBAT MONITOR							
V_{BMON}	Battery Voltage Monitor Accuracy	$V_{(BAT)}$ Falling - Including 2% increment		–3.5		3.5	%$V_{(BATREG)}$
BATTERY-PACK NTC MONITOR							
V_{HOT}	High temperature threshold	V_{TS} falling, 1% V_{IN} Hysteresis	bq25120	14.5	15	15.2	%V_{IN}
			bq25121				
V_{WARM}	Warm temperature threshold	V_{TS} falling, 1% V_{IN} Hysteresis	bq25120	20.1	20.5	20.8	%V_{IN}
			bq25121	20.2	20.6	20.9	
V_{COOL}	Cool temperature threshold	V_{TS} rising, 1% V_{IN} Hysteresis	bq25120	35.4	36	36.4	%V_{IN}
			bq25121	35.5	36.1	36.5	
V_{COLD}	Low temperature threshold	V_{TS} rising, 1% V_{IN} Hysteresis	bq25120	39.3	39.8	40.2	%V_{IN}
			bq25121	39.5	40	40.3	
TS_{OFF}	TS Disable threshold	V_{TS} rising, 2% V_{IN} Hysteresis	bq25120	55		60	%V_{IN}
			bq25121				
PROTECTION							
$V_{(UVLO)}$	IC active threshold voltage	V_{IN} rising		3.4	3.6	3.8	V
$V_{UVLO(HYS)}$	IC active hysteresis	V_{IN} falling from above V_{UVLO}			150		mV
$V_{(BUVLO)}$	Battery Undervoltage Lockout threshold Range	Programmable Range for $V_{(BUVLO)}$ VBAT falling, 150 mV Hysteresis		2.2		3.0	V
	Default Battery Undervoltage Lockout Accuracy	$V_{(BAT)}$ falling		–2.5%		2.5%	
$V_{(BATSHORT)}$	Battery short circuit threshold	Battery voltage falling			2		V
$V_{(BATSHORT\_HYS)}$	Hysteresis for $V_{(BATSHORT)}$				100		mV
$I_{(BATSHORT)}$	Battery short circuit charge current				$I_{(PRETERM)}$		mA
$V_{(SLP)}$	Sleep entry threshold, V_{IN} – $V_{(BAT)}$	2 V < V_{BAT} < $V_{(BATREG)}$, V_{IN} falling			65	120	mV
$V_{(SLP\_HYS)}$	Sleep-mode exit hysteresis	V_{IN} rising above $V_{(SLP)}$		40	65	100	mV
V_{OVP}	Maximum Input Supply OVP threshold voltage	V_{IN} rising, 100 mV hysteresis		5.35	5.55	5.75	V
t_{DGL_OVP}	Deglitch time, VIN OVP falling	V_{IN} falling below V_{OVP}, 1V/us			32		ms
T_{SHTDWN}	Thermal trip	V_{IN} > V_{UVLO}			114		°C
T_{HYS}	Thermal hysteresis	V_{IN} > V_{UVLO}			11		°C

Electrical Characteristics (continued)

Circuit of 図 1, $V_{(UVLO)} < V_{IN} < V_{(OVP)}$ and $V_{IN} > V_{(BAT)} + V_{(SLP)}$, T_J = –40°C to 85°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DGL_SHTDWN}	Deglitch time, Thermal shutdown	T_J rising above T_{SHTDWN}		4		µs

Electrical Characteristics (continued)

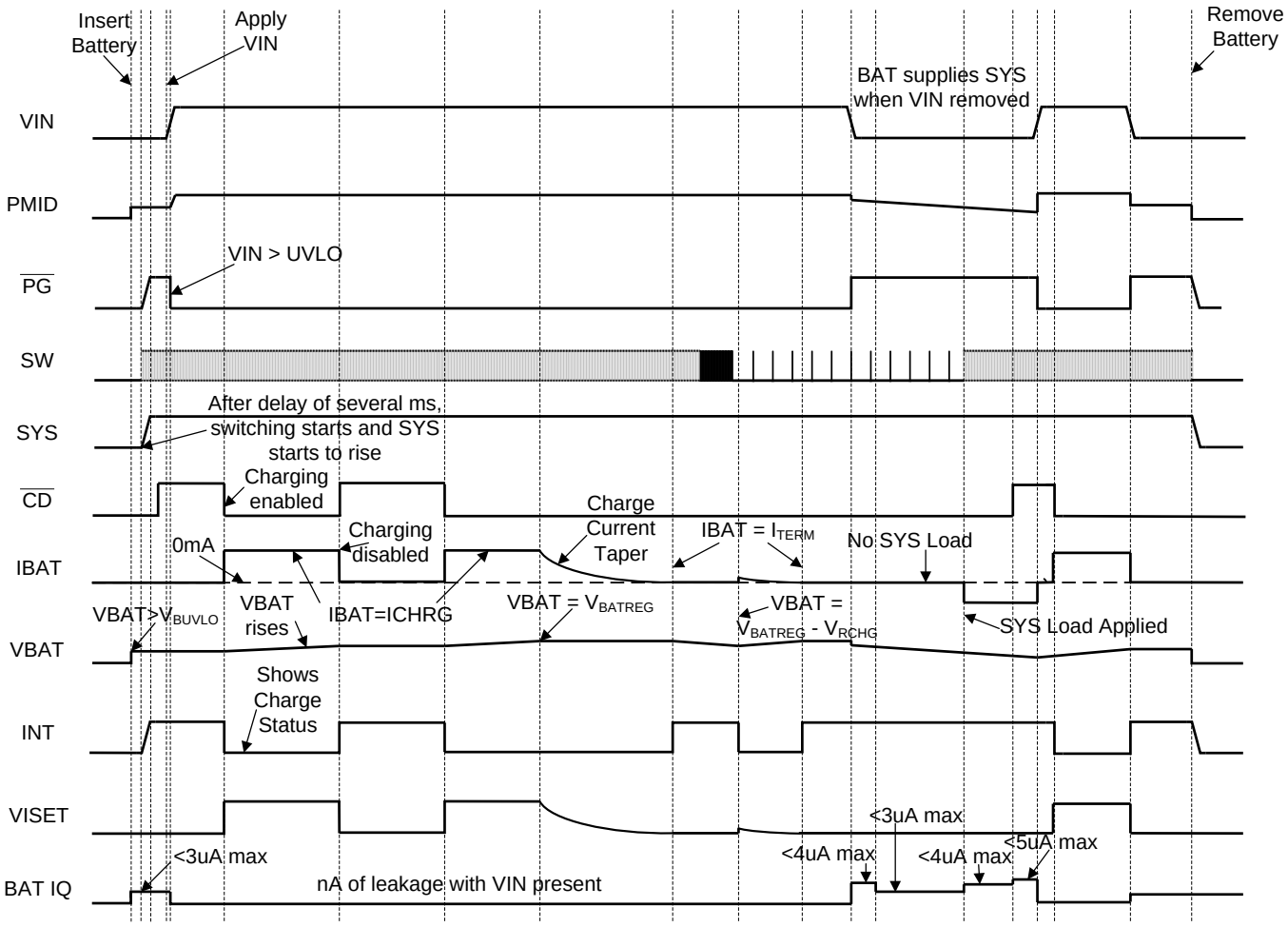
Circuit of 図 1, $V_{(UVLO)} < V_{IN} < V_{(OVP)}$ and $V_{IN} > V_{(BAT)} + V_{(SLP)}$, T_J = –40°C to 85°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I2C INTERFACE						
	I^2C Bus Specification standard and fast mode frequency support		100		400	kHz
V_{IL}	Input low threshold level	V_{PULLUP} = 1.1 V, SDA and SCL			0.275	V
V_{IH}	Input high threshold level	V_{PULLUP} = 1.1 V, SDA and SCL	0.825			V
V_{IH}	Input high threshold level	V_{PULLUP} = 3.3 V, SDA and SCL	2.475			V
V_{OL}	Output low threshold level	IL = 5 mA, sink current, V_{PULLUP} = 1.1 V			0.275	V
I_{BIAS}	High-Level leakage current	V_{PULLUP} = 1.8 V, SDA and SCL			1	µA
INT, $\overline{PG}$, and $\overline{RESET}$ OUTPUT (Open Drain)						
V_{OL}	Low level output threshold	Sinking current = 5 mA			0.25 x $V_{(SYS)}$	V
I_{IN}	Bias current into pin	Pin is high impedance, I_{OUT} = 0 mA; T_J = –40°C to 60°C			12	nA
$V_{IN(BAT\_DELTA)}$	Input voltage above VBAT where $\overline{PG}$ sends two 128 µs pulses each minute to signal the host of the input voltage status	$V_{UVLO} < V_{IN} < V_{OVP}$	0.825	1	1.15	V
INPUT PIN ($\overline{CD}$ LSCTRL)						
$V_{IL(/CD\_LSCTRL)}$	Input low threshold	$V_{(PULLUP)} = V_{SYS}$ = 3.3 V			0.25 * V_{SYS}	V
$V_{IH(/CD\_LSCTRL)}$	Input high threshold	$V_{(PULLUP)} = V_{SYS}$ = 3.3 V	0.75 * V_{SYS}			V
$R_{PULLDOWN/CD}$	Internal pull-down resistance			900		kΩ
$R_{(LSCTRL)}$	Internal pull-down resistance			2		MΩ

8.6 Timing Requirements

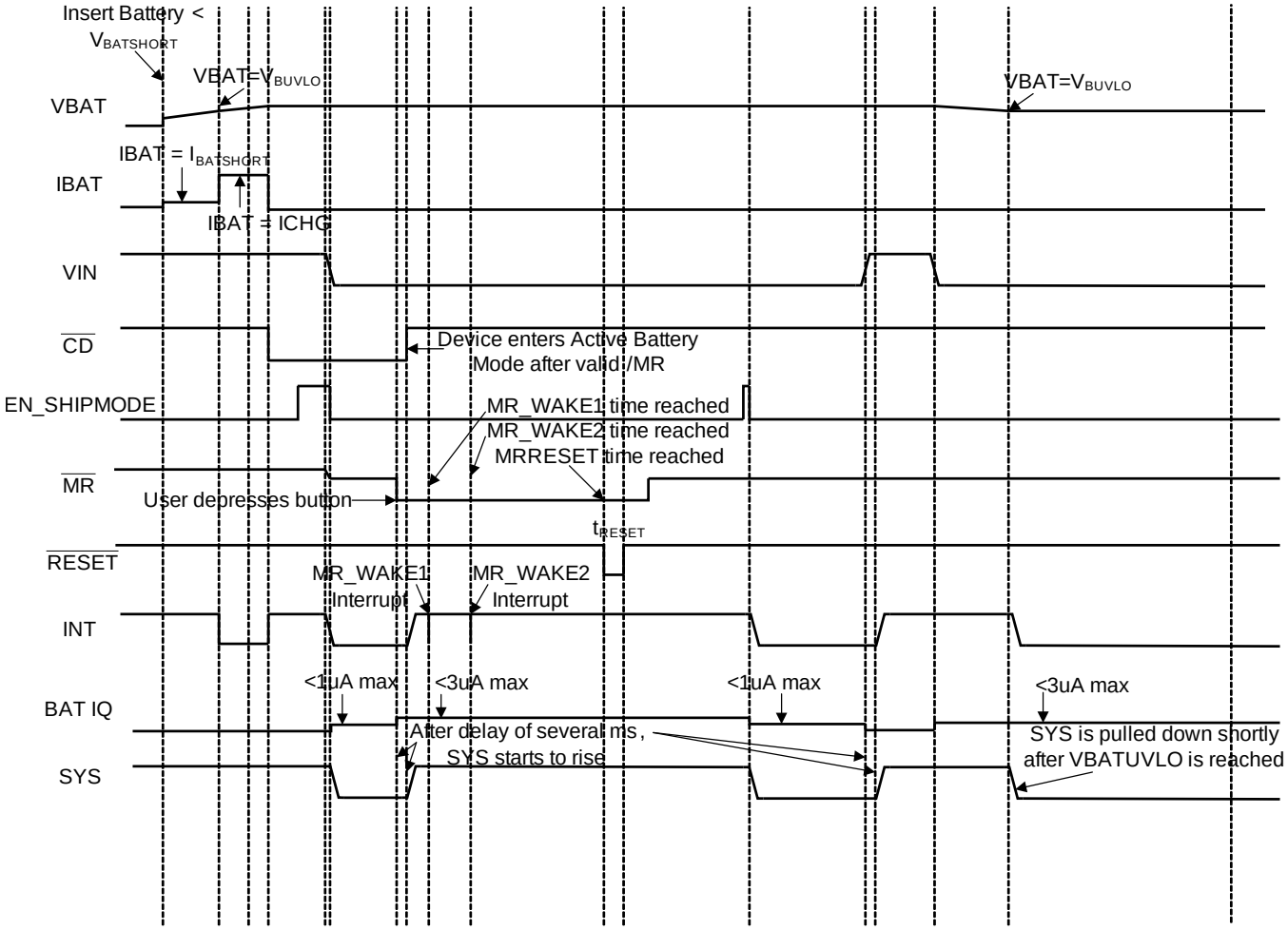
			MIN	TYP	MAX	UNIT
POWER-PATH MANAGEMENT AND INPUT CURRENT LIMIT						
t_{DGL_SC}	Deglitch Time, PMID or SW Short Circuit during Discharge Mode			250		µs
t_{REC_SC}	Recovery time, OUT Short Circuit during Discharge Mode			2		s
BATTERY CHARGER						
t_{DGL_SHORT}	Deglitch time transition from ISET short to $I_{(CHARGE)}$ disable	Clear fault by disconnecting VIN		1		ms
BATTERY CHARGING TIMERS						
t_{MAXCHG}	Charge safety timer	Programmable range	2		540	min
t_{PRECHG}	Precharge safety timer			0.1 x t_{MAXCHG}		
SYS OUTPUT						
t_{ONMIN}	Minimum ON time	V_{IN} = 3.6 V, V_{OUT} = 2 V, I_{OUT} = 0 mA		225		ns
t_{OFFMIN}	Minimum OFF time	V_{IN} = 4.2 V		50		ns
t_{START_SW}	SW start up time	V_{IN} = 5 V, from write on EN_SW_OUT until output starts to rise		5	25	ms
t_{START_SYS}	SYS output time to start switching	From insertion of BAT > $V_{(BUVLO)}$ or V_{IN} > $V_{(UVLO)}$		350		µs
$t_{SOFTSTART}$	Softstart time with reduced current limit			400	1200	µs
LS/LDO OUTPUT						
t_{ON_LDO}	Turn ON time	100-mA load		500		µs
t_{OFF_LDO}	Turn OFF time	100-mA load		5		µs
PUSHBUTTON TIMER						
t_{WAKE1}	Push button timer wake 1	Programmable Range for wake1 function	0.08		1	s
t_{WAKE2}	Push button timer wake 2	Programmable Range for wake2 function	1		2	s
t_{RESET}	Push button timer reset	Programmable Range for reset function	5		15	s
t_{RESET_D}	Reset pulse duration			400		ms
t_{DD}	Detection delay (from MR, input to RESET)	For 0s condition		6		µs
BATTERY-PACK NTC MONITOR						
$t_{DGL(TS)}$	Deglitch time on TS change	Applies to $V_{(HOT)}$, $V_{(WARM)}$, $V_{(COOL)}$, and $V_{(COLD)}$		50		ms
I2C INTERFACE						
$t_{WATCHDOG}$	I^2C interface reset timer for host			50		s
$t_{I2CRESET}$	I^2C interface inactive reset timer			700		ms
$t_{HIZ\_ACTIVEBAT}$	Transition time required to enable the I^2C interface from HiZ to Active BAT				1	ms
INPUT PIN						
$t_{/CD\_DGL}$	Deglitch for $\overline{CD}$	$\overline{CD}$ rising/falling		100		µs

Typical Start-Up Timing and Operation



Conditions: PGB_MRS = 0, TE = 1, SW_LDO = 1, VINDPM_ON = 0, $\overline{PG}$ and INT pulled up to SYS, EN_INT = 1

図 1. Typical Start-Up Timing and Operation



Conditions: SW_LDO = 1, MRREC = 1, $\overline{PG}$ and INT pulled up to SYS, ISYS = 10 µA, EN_INT = 1

図 2. Battery Operation and Sleep Mode

8.7 Typical Characteristics

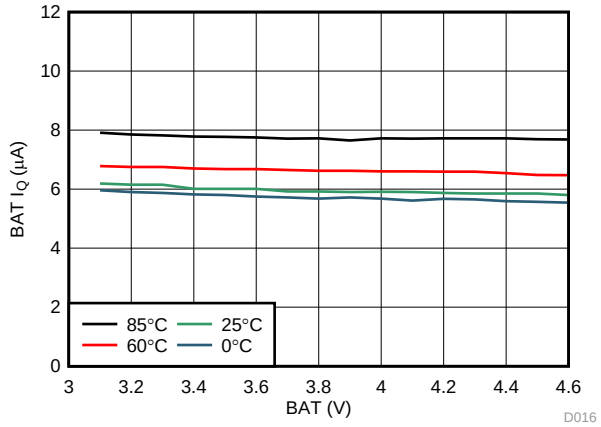
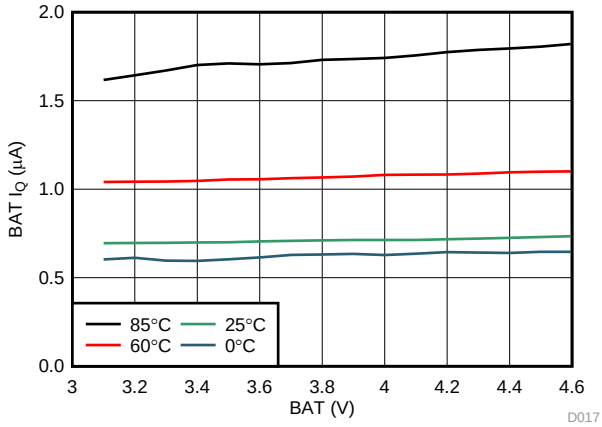


図 3. Active BAT, I_Q



1.8 V System Enabled (No Load)

図 4. Hi-Z BAT, I_Q

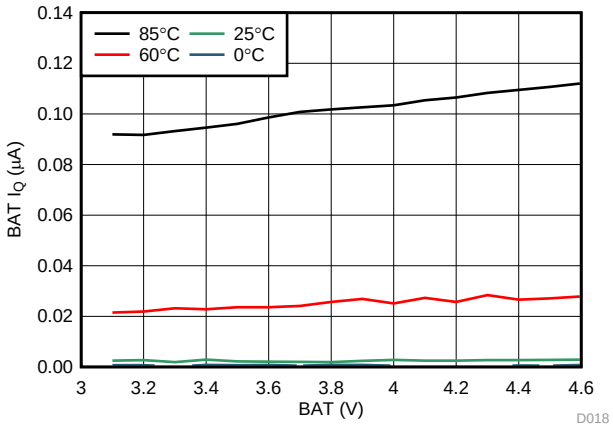


図 5. Ship Mode BAT, I_Q

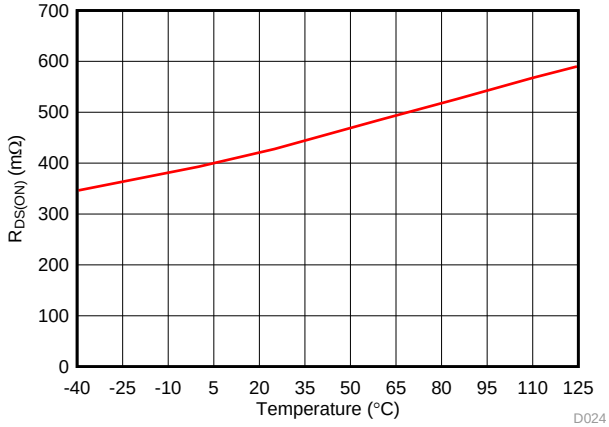


図 6. Blocking FET $R_{DS(ON)}$ vs Temperature

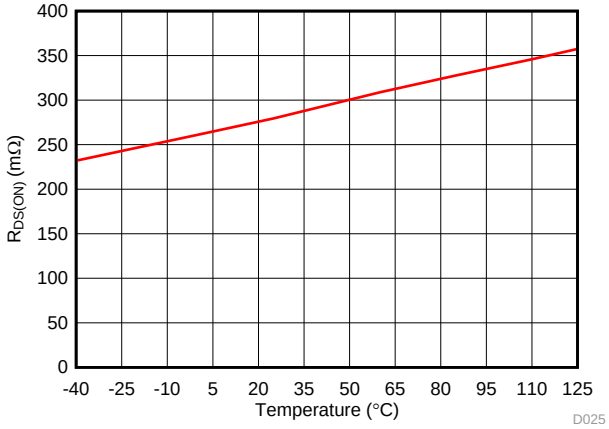


図 7. Battery Discharge FET $R_{DS(ON)}$ vs Temperature

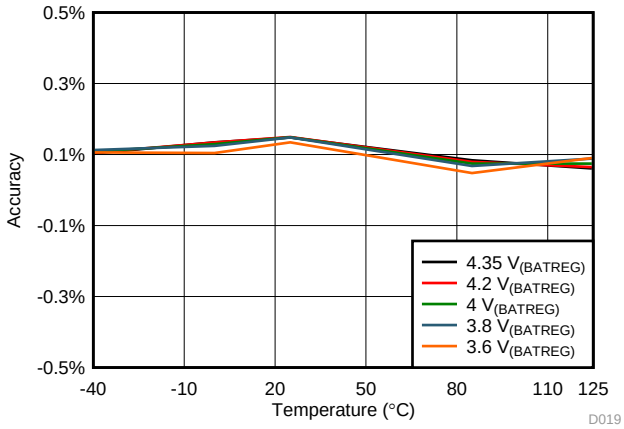


図 8. $V_{(BATREG)}$ Accuracy vs Temperature

Typical Characteristics (continued)

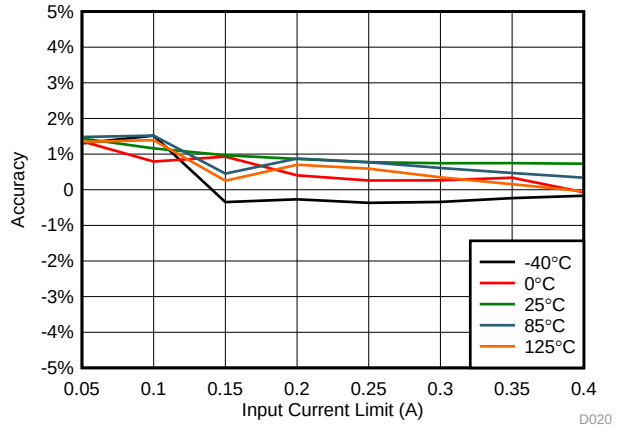


図 9. ILIM Accuracy vs Input Current

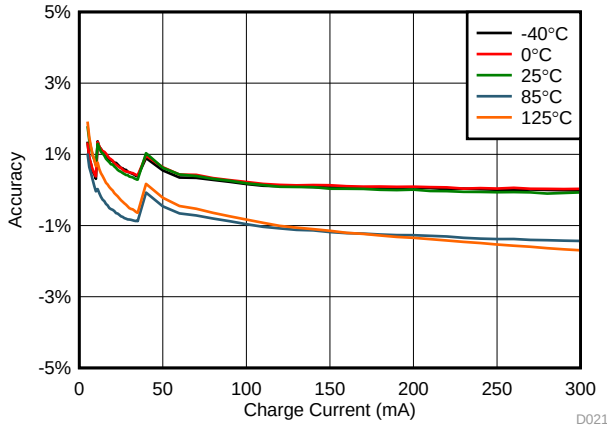


図 10. Charge Current Accuracy vs Charge Current

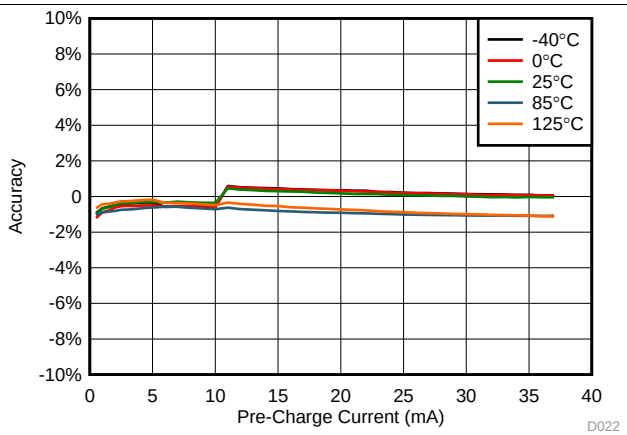
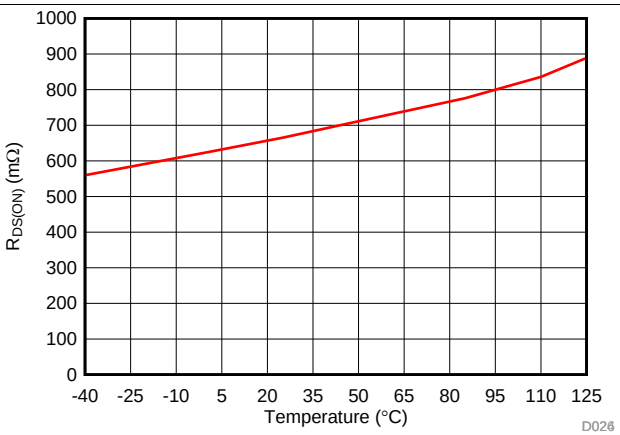
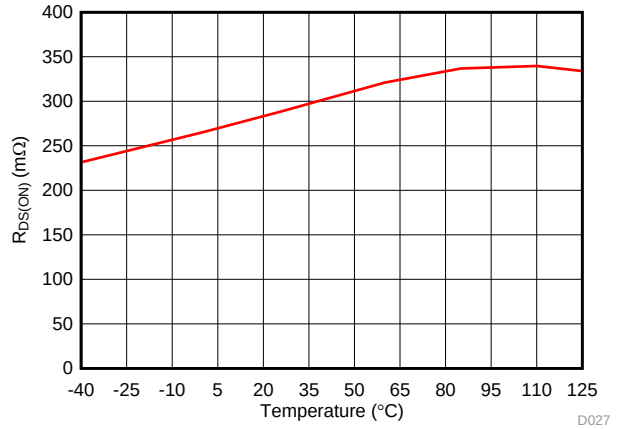


図 11. Pre-Charge Accuracy vs Pre-Charge Current



V_{IN} = 5 V

図 12. $R_{DS(ON)}$ of High Side MOSFET vs Temperature



V_{IN} = 5 V

図 13. $R_{DS(ON)}$ of Low Side MOSFET vs Temperature

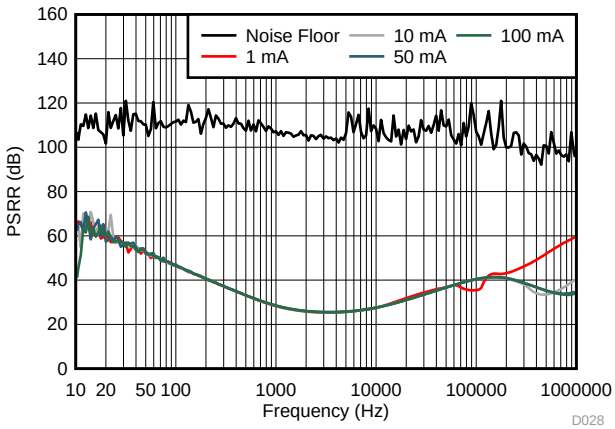


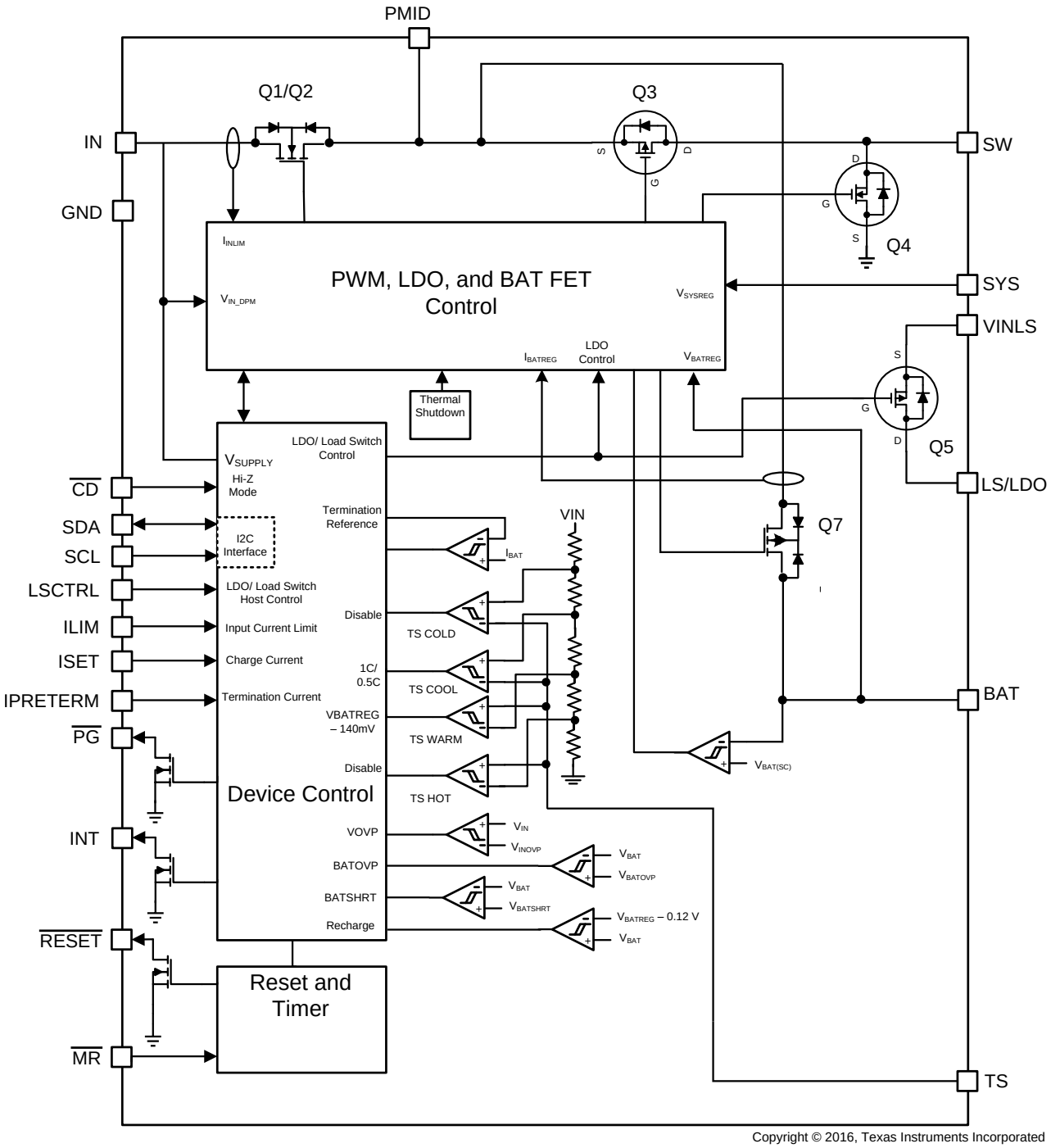
図 14. LS/LDO PSRR vs Frequency

9 Detailed Description

9.1 Overview

The following sections describe in detail the functions provided by the BQ25120. These include linear charger, PWM output, configurable LS/LDO output, Push-button input, reset timer, functional modes, battery monitor, I^2C configurability and functions, and safety features.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Ship Mode

Ship Mode is the lowest quiescent current state for the device. Ship Mode latches off the device and BAT FET until $V_{IN} > V_{UVLO}$ or the $\overline{MR}$ button is depressed for t_{WAKE1} and released. To enter Ship Mode, $\overline{CD}$ must be pulled high. If the EN_SHIPMODE is written to a 1 while the input is connected, it must first be removed to enter ship mode. This allows the end product with minimal load on the battery, and the end user can enable the device by plugging it into the adapter or by toggling the $\overline{MR}$ button. The battery voltage must be above the maximum programmable BUVLO threshold in order to exit Ship mode with a $\overline{MR}$ button press when V_{IN} is not present.. The EN_SHIPMODE bit can be cleared using the I^2C interface as well while the input is valid. The following list shows the events that are active during Ship Mode:

1. VIN_UV Comparator
2. $\overline{MR}$ Input (No clock or delay in this mode for lowest power consumption)

9.3.2 High Impedance Mode

High Impedance mode is the lowest quiescent current state while operating from the battery. During Hi-Z mode the SYS output is powered by BAT, the $\overline{MR}$ input is active, and the LSCTRL input is active. All other circuits are in a low power or sleep state.The LS/LDO output can be enabled in Hi-Z mode with the LSCTRL input. If the LS/LDO output has been enabled through I^2C prior to entering Hi-Z mode, it will stay enabled. The $\overline{CD}$ pin is used to put the device in a high-impedance mode when battery is present and $V_{IN} < V_{UVLO}$. Drive $\overline{CD}$ high to enable the device and enter active battery operation when V_{IN} is not valid. When the HZ_MODE bit is written by the host, the I^2C interface is disabled if only battery is present. To resume I^2C, the $\overline{CD}$ pin must be toggled. The functionality is shown in 表 1.

表 1. CD, State Table

CD, State	$V_{IN} < V_{UVLO}$	$V_{IN} > V_{UVLO}$
L	Hi-Z	Charge Enabled
H	Active Battery	Charge Disabled

9.3.3 Active Battery Only Connected

When the battery above $V_{BATUVLO}$ is connected with no input source, the battery discharge FET is turned on. After the battery rises above $V_{BATUVLO}$ and the deglitch time is reached, the SYS output starts to rise. The current from PMID and SYS is not regulated, but is protected by a short circuit current limit. If the short circuit limit is reached for the deglitch time (t_{DGL_SC}), the battery discharge FET is turned off for the recovery time (t_{REC_SC}). After the recovery time, the battery FET is turned on to test if the short has been removed. If it has not, the FET turns off and the process repeats until the short is removed. This process protects the internal FET from over current. During this event PMID will likely droop and cause SYS to go out of regulation.

To provide designers the most flexibility in optimizing their system, an adjustable BATUVLO is provided. When the voltage drops below the $V_{BATUVLO}$ threshold, the battery discharge FET is turned off. Deeper discharge of the battery enables longer times between charging, but may shorten the battery life. The BATUVLO is adjustable with a fixed 100-mV hysteresis.

If a valid V_{IN} is connected during active battery mode, $V_{IN} > V_{UVLO}$, the supplement and battery discharge FET is turned on when the battery voltage is above the minimum $V_{BATUVLO}$.

Drive $\overline{CD}$ high or write the CE register to disable charge when $V_{IN} > V_{UVLO}$ is present. $\overline{CD}$ is internally pulled down. When exiting this mode, charging resumes if V_{IN} is present, $\overline{CD}$ is low and charging is enabled.

All HOST interfaces ($\overline{CD}$, SDA/SCL, INT, $\overline{RESET}$ and LSCTRL) are active no later than 5 ms after SYS reaches the programmed level.

9.3.4 Voltage Based Battery Monitor

The device implements a simple voltage battery monitor which can be used to determine the depth of discharge. Prior to entering High-Z mode, the device will initiate a VBMON reading. The host can read the latched value for the no-load battery voltage, or initiate a reading using VBMON_READ to see the battery voltage under a known load. The register will be updated and can be read 2ms after a read is initiated. The VBMON voltage threshold is readable with 2% increments with ±1.5% accuracy between 60% and 100% of VBATREG using the VBMON_TH registers. Reading the value during charge is possible, but for the most accurate battery voltage indication, it is recommended to disable charge, initiate a read, and then re-enable charge.

A typical discharge profile for a Li-Ion battery is shown in 表 2. The specific battery to be used in the application should be fully characterized to determine the thresholds that will indicate the appropriate battery status to the user. Two typical examples are shown below, assuming the VBMON reading is taken with no load on the battery.

This function enables a simple 5-bar status indicator with the following typical performance with different VBATREG settings:

表 2. Discharge Profile for a Li-Ion Battery

VBATREG	BATTERY FULL	95% to 65% REMAINING CAPACITY	65% to 35% REMAINING CAPACITY	35% to 5% REMAINING CAPACITY	BATTERY EMPTY
4.35 V	VBMON > 90%	VBMON = 88%	VBMON = 86%	VBMON = 84%	VBMON < 82%
4.2 V	VBMON > 98%	VBMON = 94% or 96%	VBMON = 90% or 92%	VBMON = 86% or 88%	VBMON < 84%

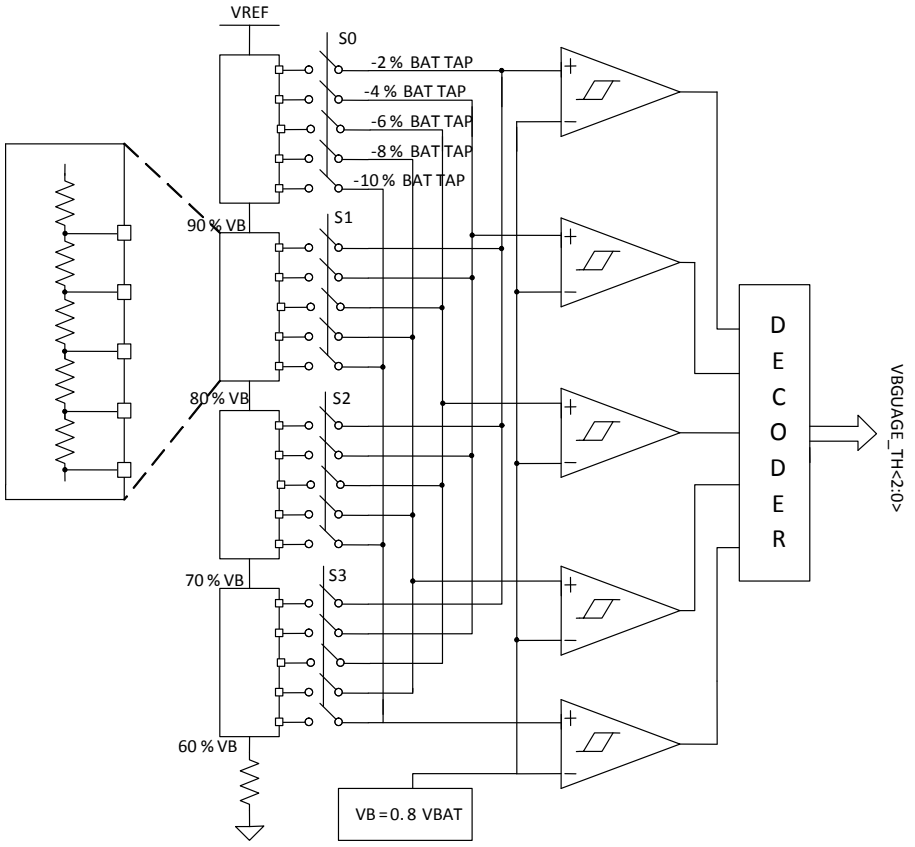


図 15. Voltage Battery Monitor

9.3.5 Sleep Mode

The device enters the low-power sleep mode if the voltage IN falls below the sleep-mode entry threshold and V_{IN} is higher than the undervoltage lockout threshold. In sleep mode, the input is isolated from the battery. This feature prevents draining the battery during the absence of V_{IN}. When $V_{IN} < V_{(BAT)} + V_{SLP}$, the device turns the battery discharge FET on, sends a 128-µs pulse on the INT output, and the FAULT bits of the register are update over I^2C. Once $V_{IN} > V_{(BAT)} + V_{SLP}$, the device initiates a new charge cycle. The FAULT bits are not cleared until they are read over I^2C and the sleep condition no longer exists.

9.3.6 Input Voltage Based Dynamic Power Management ($V_{IN(DPM)}$)

During the normal charging process, if the input power source is not able to support the programmed or default charging current and System load, the supply voltage decreases. Once the supply drops to $V_{IN(DPM)}$, the input DPM current and voltage loops will reduce the input current through the blocking FETs, to prevent the further drop of the supply. The $V_{IN(DPM)}$ threshold is programmable through the I^2C register from 4.2 V to 4.9 V in 100-mV steps. It can be disabled completely as well. When the device enters this mode, the charge current may be lower than the set value and the VINDPM_STAT bit is set. If the 2X timer is set, the safety timer is extended while $V_{IN(DPM)}$ is active. Additionally, termination is disabled.

9.3.7 Input Overvoltage Protection and Undervoltage Status Indication

The input overvoltage protection protects the device and downstream components connected to PMID, SYS, and BAT against damage from overvoltage on the input supply. When $V_{IN} > V_{OVP}$ an OVP fault is determined to exist. During the OVP fault, the device turns the battery discharge FET on, sends a single 128-µs pulse on INT, and the FAULT bits are updated over I^2C. Once the OVP fault is removed, after the deglitch time, t_{DGL_OVP}, STAT and FAULT bits are cleared and the device returns to normal operation. The FAULT bits are not cleared until they are read in from I^2C after the OVP condition no longer exists. The OVP threshold for the device is set to operate from standard USB sources.

The input under-voltage status indication is used to notify the host or other device when the input voltage falls below a desired threshold. When $V_{IN} < V_{UVLO}$, after the deglitch time t_{DGL_UVLO}, a UVLO fault is determined to exist. During the V_{IN} UVLO fault, the device sends a single 128-µs pulse on INT, and the STAT and FAULT bits are updated over I^2C. The FAULT bits are not cleared until they are read in from I^2C after the UVLO condition no longer exists.

9.3.8 Battery Charging Process and Charge Profile

When a valid input source is connected ($V_{IN} > V_{UVLO}$ and $V_{(BAT)} + V_{SLP} < V_{IN} < V_{OVP}$), the $\overline{CE}$ bit in the control register determines whether a charge cycle is initiated. When the $\overline{CE}$ bit is 1 and a valid input source is connected, the battery discharge FET is turned off, and the output at SYS is regulated depending on the output configuration. A charge cycle is initiated when the $\overline{CE}$ bit is written to a 0. Alternatively, the $\overline{CD}$ input can be used to enable and disable charge.

The device supports multiple battery chemistries for single-cell applications. Charging is done through the internal battery MOSFET. There are several loops that influence the charge current: constant current loop (CC), constant voltage loop (CV), input current limit, V_{DPPM}, and $V_{IN(DPM)}$. During the charging process, all loops are enabled and the one that is dominant takes control.

The charge current is regulated to I_{CHARGE} until the voltage between BAT and GND reaches the regulation voltage. The voltage between BAT and GND is regulated to V_{BATREG} (CV Mode) while the charge current naturally tapers down. When termination is enabled, the device monitors the charging current during the CV mode, and once the charge current tapers down to the termination threshold, I_{TERM}, and the battery voltage is above the recharge threshold, the device terminates charge, and turns off the battery charging FET. Termination is disabled when any loop is active other than CV.

9.3.9 Dynamic Power Path Management Mode

With a valid input source connected, the power-path management circuitry monitors the input voltage and current continuously. The current into IN is shared at PMID between charging the battery and powering the system load at PMID, SYS, and LS/LDO. If the sum of the charging and load currents exceeds the preset maximum input current, the input DPM loop reduces input current. If PMID drops below the DPPM voltage threshold, the charging current is reduced by the DPPM loop through the BATFET. If PMID continues to drop after BATFET charging current is reduced to zero, the part enters supplement mode when PMID falls below the supplement mode threshold. Battery termination is disabled while in DPPM mode.

9.3.10 Battery Supplement Mode

While in DPPM mode, if the charging current falls to zero and the system load current increases beyond the programmed input current limit, the voltage at PMID reduces further. When the PMID voltage drops below the battery voltage by $V_{(BSUP1)}$, the battery supplements the system load. The battery stops supplementing the system load when the voltage on the PMID pin rises above the battery voltage by $V_{(BSUP2)}$. During supplement mode, the battery supplement current is not regulated, however, the short-circuit protection circuit is active. Battery termination is disabled while in supplement mode.

9.3.11 Default Mode

The default mode is used when there is no host, or I^2C communication is not available. If the externally programmable pins, ILIM, ISET, and ITERM have resistors connected, that is considered the default mode. If they are tied to GND, the default register settings are used. The default mode can be entered by connecting a valid power source to V_{IN} or the RESET bit is written. Default mode is exited by writing to the I^2C interface.

9.3.12 Termination and Pre-Charge Current Programming by External Components (IPRETERM)

The termination current threshold is user programmable through an external resistor or through registers over I^2C. Set the termination current using the IPRETERM pin by connecting a resistor from IPRETERM to GND. The termination can be set between 5% and 20% of the programmed output current set by ISET, using 表 3 for guidance:

表 3. IPRETERM Resistor Settings

IPRE_CHARGE and ITERM			KKIPRETERM			RIPRETERM (STANDARD 1% VALUES)	UNIT
MIN	TYP (% of ISET)	MAX	MIN	TYP	MAX	RECOMMENDED RIPRETERM	
	5		180	200	220	15000	Ω
	10		180	200	220	4990	Ω
	15		180	200	220	1650	Ω
	20		180	200	220	549	Ω

Using the I^2C register, the termination current can be programmed with a minimum of 500 µA and a maximum of 37 mA.

The pre-charge current is not independently programmable through the external resistor, and is set at the termination current. The pre-charge and termination currents are programmable using the IPRETERM registers. If no IPRETERM resistor is connected and the pin is tied to GND, the default values in the IPRETERM registers are used. The external value can be used in host mode by configuring the IPRETERM registers. If the external ICHG setting will be used after being in Host mode, the IPRETERM registers should be set to match the desired external threshold for the highest ICHG accuracy.

Termination is disabled when any loop other than CV is active.

9.3.13 Input Current Limit Programming by External Components (ILIM)

The input current limit threshold is user programmable through an external resistor or through registers over I^2C. Set the input current limit using the ILIM pin by connecting a resistor from ILIM to GND using 表 4 for guidance. If no ILIM resistor is connected and the pin is tied to GND, the default ILIM register value is used. The external value is not valid once the device enters host mode.

表 4. ILIM Resistor Settings

ILIM			KILIM			RILIM (STANDARD 1% VALUES)	UNIT
MIN	TYP	MAX	MIN	TYP	MAX		
0.048469388	0.051020408	0.053571429	190	200	210	3920	Ω
0.09047619	0.095238095	0.1	190	200	210	2100	Ω
0.146153846	0.153846154	0.161538462	190	200	210	1300	Ω
0.19	0.2	0.21	190	200	210	1000	Ω
0.285714286	0.30075188	0.315789474	190	200	210	665	Ω
0.380761523	0.400801603	0.420841683	190	200	210	499	Ω

The device has register programmable input current limits from 50 mA to 400 mA in 50-mA steps. The device is USB-IF compliant for inrush current testing, assuming that the input capacitance to the device is selected to be small enough to prevent a violation (<10 µF), as this current is not limited.

9.3.14 Charge Current Programming by External Components (ISET)

The fast charge current is user programmable through an external resistor or through registers over I^2C. Set the fast charge current by connecting a resistor from ISET to GND. If no ISET resistor is connected and the pin is tied to GND, the default ISET register value is used. While charging, if the charge current is using the externally programmed value, the voltage at ISET reflects the actual charging current and can be used to monitor charge current. The current out of ISET is 1/100 (±10%) of the charge current. The charge current can be calculated by using 表 5 for guidance:

表 5. ISET Resistor Settings

ISET			KISET			RISET (STANDARD 1% VALUES)	UNIT
MIN	TYP	MAX	MIN	TYP	MAX		
0.285714286	0.30075188	0.315789474	190	200	210	665	Ω
0.19	0.2	0.21	190	200	210	1000	Ω
0.126666667	0.133333333	0.14	190	200	210	1500	Ω
0.095	0.1	0.105	190	200	210	2000	Ω
0.06462585	0.068027211	0.071428571	190	200	210	2940	Ω
0.048469388	0.051020408	0.053571429	190	200	210	3920	Ω
0.038076152	0.04008016	0.042084168	190	200	210	4990	Ω
0.031456954	0.033112583	0.034768212	190	200	210	6040	Ω
0.025956284	0.027322404	0.028688525	190	200	210	7320	Ω
0.019	0.02	0.021	190	200	210	10000	Ω
0.012666667	0.013333333	0.014	190	200	210	15000	Ω
0.0095	0.01	0.0105	190	200	210	20000	Ω
0.006462585	0.006802721	0.007142857	190	200	210	29400	Ω
0.004846939	0.005102041	0.005357143	190	200	210	39200	Ω

9.3.15 Safety Timer and Watchdog Timer

At the beginning of the charge cycle, the device starts the safety timer. If charging has not terminated before the programmed safety time, t_{MAXCHG}, expires, the device enters idle mode and charging is disabled. The pre-charge safety time, t_{PRECHG}, is 10% of t_{MAXCHG}. When a safety timer fault occurs, a single 128 µs pulse is sent on the INT pin and the STAT and FAULT bits of the status registers are updated over I^2C. The $\overline{CD}$ pin or power must be toggled in order to clear the safety timer fault. The safety timer duration is programmable using the TMR bits. When the safety timer is active, changing the safety timer duration resets the safety timer. The device also contains a 2X_TIMER bit that enables the 2X timer function to prevent premature safety timer expiration when the charge current is reduced by a load on PMID, SYS, LS/LDO or a NTC condition. When t_{2X_TIMER} function is enabled, the timer is allowed to run at half speed when any loop is active other than CC or CV.

In addition to the safety timer, the device contains a 50-second watchdog timer that monitors the host through the I^2C interface. Once any I^2C transaction is performed on the I^2C interface, a watchdog timer is started. The watchdog timer is reset by any transaction by the host using the I^2C interface. If the watchdog timer expires without a reset from the I^2C interface, all registers except MRRESET_VIN and MRREC are reset to the default values.

9.3.16 External NTC Monitoring (TS)

The I^2C interface allows the user to easily implement the JEITA standard for systems where the battery pack thermistor is monitored by the host. Additionally, the device provides a flexible voltage based TS input for monitoring the battery pack NTC thermistor. The voltage at TS is monitored to determine that the battery is at a safe temperature during charging.

To satisfy the JEITA requirements, four temperature thresholds are monitored: the cold battery threshold, the cool battery threshold, the warm battery threshold, and the hot battery threshold. These temperatures correspond to the $V_{(COLD)}$, $V_{(COOL)}$, $V_{(WARM)}$, and $V_{(HOT)}$ threshold in the *Electrical Characteristics*. Charging and timers are suspended when $V_{(TS)} < V_{(HOT)}$ or $> V_{(COLD)}$. When $V_{(COOL)} < V_{(TS)} < V_{(COLD)}$, the charging current is reduced to half of the programmed charge current. When $V_{(HOT)} < V_{(TS)} < V_{(WARM)}$, the battery regulation voltage is reduced by 140 mV the programmed charge current.

The TS function is voltage based for maximum flexibility. Connect a resistor divider from V_{IN} to GND with TS connected to the center tap to set the threshold. The connections are shown in 図 16. The resistor values are calculated using 式 1 and 式 2. To disable the TS function, pull TS above TS_{OFF} threshold.

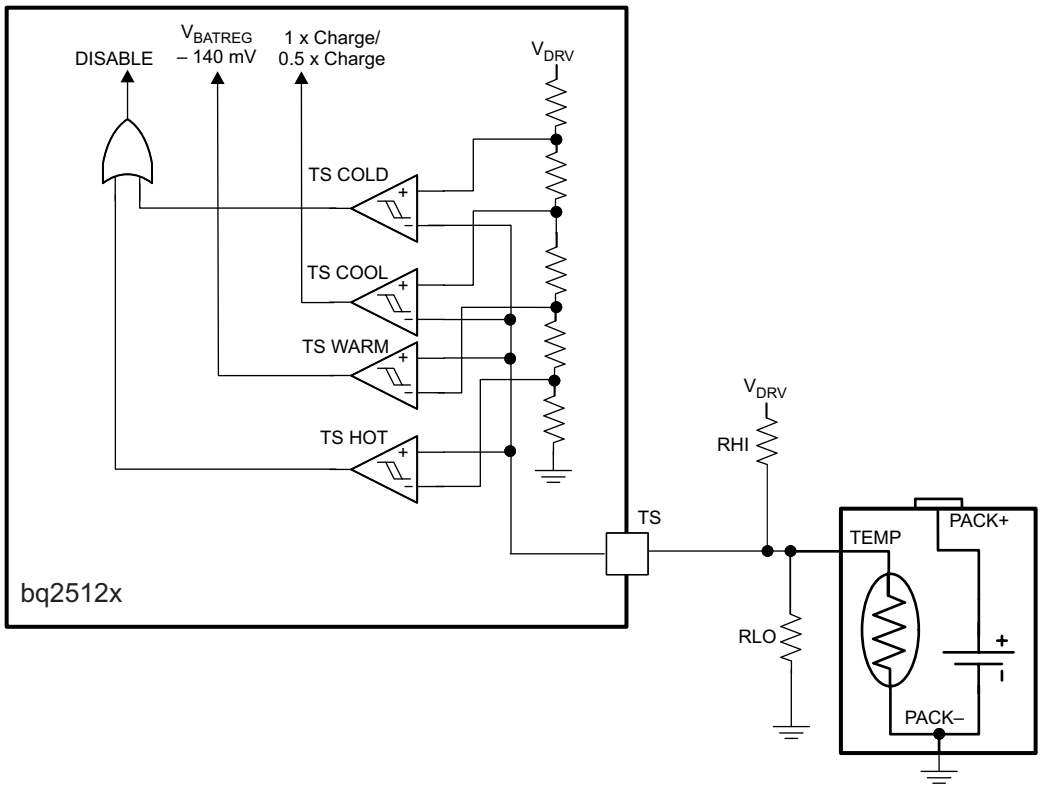


図 16. TS Circuit

$$R_{(LO)} = \frac{V_{IN} \times R_{(COLD)} \times R_{(HOT)} \times \left(\frac{1}{V_{(COLD)}} - \frac{1}{V_{(HOT)}}\right)}{R_{(HOT)} \times \left(\frac{V_{IN}}{V_{(HOT)}} - 1\right) - R_{(COLD)} \times \left(\frac{V_{IN}}{V_{(COLD)}} - 1\right)} \quad (1)$$

$$R_{(HI)} = \frac{\left(\frac{V_{IN}}{V_{(COLD)}} - 1\right)}{\left(\frac{1}{R_{(LO)}} + \frac{1}{R_{(COLD)}}\right)} \quad (2)$$

Where

- $R_{(HOT)}$ = the NTC resistance at the hot temperature
- $R_{(COLD)}$ = the NTC resistance at the cold temperature

The warm and cool thresholds are not independently programmable. The cool and warm NTC resistances for a selected resistor devider are calculated using 式 3 and 式 4.

$$R_{(COOL)} = \frac{R_{(LO)} \times R_{(HI)} \times V_{COOL}\%}{R_{(LO)} - R_{(LO)} \times V_{COOL}\% - R_{(HI)} \times V_{COOL}\%} \quad (3)$$

$$R_{(WARM)} = \frac{R_{(LO)} \times R_{(HI)} \times V_{WARM}\%}{R_{(LO)}} - \left(R_{(LO)} \times V_{WARM}\% - R_{(HI)} \times V_{WARM}\%\right) \quad (4)$$

9.3.17 Thermal Protection

During the charging process, to prevent overheating in the device, the juntion temperature of the die, T_J, is monitored. When T_J reaches $T_{(SHUTDOWN)}$ the device stops charging, disables the PMID output, disables the SYS output, and disables the LS/LDO output. During the time that $T_{(SHUTDOWN)}$ is exceeded, the safety timer is reset and the watchdog timer continues to operate if in host mode. The charge cycle resumes when T_J falls below $T_{(SHUTDOWN)}$ by $T_{(HYS)}$.

To avoid reaching thremal shutdown, ensure that the system power dissipation is under the limits of the device. The power dissipated by the device can be calculated using 式 5.

$$P_{DISS} = P_{(BLOCK)} + P_{(SYS)} + P_{(LS/LDO)} + P_{(BAT)} \quad (5)$$

Where

- $P_{(BLOCK)} = (V_{IN} – V_{(PMID)}) \times I_{IN}$
- $P_{(SYS)} = I_{SYS}^2 \times R_{DS(ON\_HS)}$
- $P_{(LS/LDO)} = (V_{(INLS)} – V_{(LS/LDO)}) \times I_{(LS/LDO)}$
- $P_{(BAT)} = (V_{(PMID)} – V_{(BAT)}) \times I_{(BAT)}$

9.3.18 Typical Application Power Dissipation

The die junction temperature, T_J, can be estimated based on the expected board performance using 式 6.

$$T_J = T_A + \theta_{JA} \times P_{DISS} \quad (6)$$

The θ_{JA} is largely driven by the board layout. For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report SPRA953. Under typical conditions, the time spent in this state is short.

9.3.19 Status Indicators ($\overline{PG}$ and INT)

The device contains two open-drain outputs that signal its status and are valid only after the device has completed start-up into a valid state. If the part starts into a fault, interrupts will not be sent. The $\overline{PG}$ output signals when a valid input source is connected. $\overline{PG}$ pulls to GND when V_{IN} is above V_{UVLO}. $\overline{PG}$ is high-impedance when the input power is not within specified limits. Connect $\overline{PG}$ to the desired logic voltage rail using a 1-kΩ to 100-kΩ resistor, or use with an LED for visual indication.

The $\overline{PG}$ pin can be configured as a $\overline{MR}$ shifted (MRS) output when the PGB_MRS bit is set to 1. $\overline{PG}$ is high-impedance when the $\overline{MR}$ input is not low, and $\overline{PG}$ pulls to GND when the $\overline{MR}$ input is below $V_{OL(TH\_MRS)}$. Connect $\overline{PG}$ to the desired logic voltage rail using a 1-kΩ to 100-kΩ resistor.

When enabled through OTP, the $\overline{PG}$ pin also functions as an OVP/UVP indicator. When the device is below V_{SLP} or $V_{IN(DPM)}$ (if enabled), a single 128us pulse is sent on $\overline{PG}$ to notify the host, repeating once per minute. When the device has an input voltage greater than $V_{(BAT)}$ +1 V and V_{IN} is less than V_{OVP}, two consecutive 128us pulses are sent on $\overline{PG}$, to notify the host, repeating once per minute. The $\overline{PG}$ pin does not function as an input power good indicator in this mode.

The INT pin is pulled low during charging when the EN_INT bit is set to 1 and interrupts are pulled high. When EN_INT is set to 0, charging status is not indicated on the INT pin. When charge is complete or disabled, INT is high impedance. The charge status is valid whether it is the first charge or recharge. When a fault occurs, a 128 µs pulse (interrupt) is sent on INT to notify the host.

9.3.20 Chip Disable ($\overline{CD}$)

The device contains a $\overline{CD}$ input that is used to disable the device and place it into a high impedance mode when only battery is present. In this case, when $\overline{CD}$ is low, PMID and SYS remain active, and the battery discharge FET is turned on. If the LS/LDO output has been enabled prior to pulling $\overline{CD}$ low, it will stay on. The LSCTRL pin can also enable/disable the LS/LDO output when the $\overline{CD}$ pin is pulled low. The $\overline{CD}$ pin has an internal pull-down.

If V_{IN} is present and the $\overline{CD}$ input is pulled low, charge is enabled and all other functions remain active. If V_{IN} is present and the $\overline{CD}$ input is pulled high, charge is disabled.

9.3.21 Buck (PWM) Output

The device integrates a low quiscent current switching regulator with DCS control allowing high efficiency down to 10-µA load currents. DCS control combines the advantages of hysteretic and voltage mode control. The internally compensated regulation network achieves fast and stable operation with small external components and low ESR capacitors. During PWM mode, it operates in continuous conduction mode, with a frequency up to 2 MHz. If the load current decreases, the converter enters a power save mode to maintain high efficiency down to light loads. In this mode, the device generates a single switching pulse to ramp up the inductor current and recharge the output capacitor, followed by a sleep period where most of the internal circuits are shut down to achieve a low quiescent current. The duration of the sleep period depends on the load current and the inductor peak current.

The output voltage is programmable using the SYS_SEL and SYS_VOUT bits in the SYS VOUT control register.

The SW output is enabled using the EN_SYS_OUT bit in the register. This bit is for testing and debug only and not intended to be used in the final system. When the device is enabled, the internal reference is powered up and the device enters softstart, starts switching, and ramps up the output voltage. When SW is disabled, the output is in shutdown mode in a low quiescent state. The device provides automatic output voltage discharge so the output voltage will ramp up from zero once the device in enabled again. Once SYS has been disabled, either V_{IN} needs to be connected or the $\overline{MR}$ button must be held low for the t_{RESET} duration to re-enable SYS.

The output is optimized for operation with a 2.2-µH inductor and 10-µF output capacitor. 表 6 shows the recommended LC output filter combinations.

表 6. Recommended Output Filter

INDUCTOR VALUE (µH)	OUTPUT CAPACITOR VALUE (µF)		
	4.7	10	22
2.2	Possible	Recommended	Possible

The inductor value affects the peak-to-peak ripple current, the PWM-to-PFM transition point where the part enters and exits Pulse Frequency Modulation to lower the power consumed at low loads, the output voltage ripple and the efficiency. The selected inductor must be selected for its DC resistance and saturation current. The inductor ripple current (ΔI_L) can be estimated according to 式 7.

$$\Delta I_L = V_{OUT} \times (1-(V_{OUT}/V_{IN}))/(L \times f) \quad (7)$$

Use 式 8 to calculate the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current. As the size of the inductor decreases, the saturation “knee” must be carefully considered to ensure that the inductance does not decrease during higher load condition or transient. This is recommended because during a heavy load transient the inductor current rises above the calculated value. A more conservative way is to select the inductor saturation current above the high-side MOSFET switch current.

$$I_L(max) = I_{OUT}(max) + \Delta I_L / 2 \quad (8)$$

Where

- F = Switching Frequency
- L = Inductor Value
- ΔI_L = Peak to Peak inductor ripple current
- $I_L(max)$ = Maximum Inductor current

In DC/DC converter applications, the efficiency is affected by the inductor AC resistance and by the inductor DCR value.

表 7 shows recommended inductor series from different suppliers.

表 7. Inductor Series

INDUCTANCE (µH)	DCR (Ω)	DIMENSIONS (mm^3)	INDUCTOR TYPE	SUPPLIER (1)	COMMENT
2.2	0.300	1.6 x 0.8 x 0.8	MDT1608CH2R2N	TOKO	Smallest size, 75mA max
2.2	0.170	1 .6 x 0.8 x 0.8	GLFR1608T2R2M	TDK	Smallest size, 150mA max

(1) See *Third-party Products Disclaimer*

表 7. Inductor Series (continued)

INDUCTANCE (µH)	DCR (Ω)	DIMENSIONS (mm^3)	INDUCTOR TYPE	SUPPLIER (1)	COMMENT
2.2	0.245	2.0 x 1.2 x 1.0	MDT2012CH2R2N	TOKO	Small size, high efficiency
2.2	0.23	2.0 x 1.2 x 1.0	MIPSZ2012 2R2	TDK	
2.2	0.225	2.0 x 1.6 x 1.0	74438343022	Wurth	
2.2	0.12	2.5 x 2.0 x 1.2	MIPSA2520 2R2	TDK	
2.2	0.145	3.3 x 3.3 x 1.4	LPS3314	Coicraft	

The PWM allows the use of small ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. At light load currents, the converter operates in Power Save Mode and the output voltage ripple is dependent on the output capacitor value and the PFM peak inductor current. Because the PWM converter has a pulsating input current, a low ESR input capacitor is required on PMID for the best voltage filtering to ensure proper function of the device and to minimize input voltage spikes. For most applications a 10-µF capacitor value is sufficient. The PMID capacitor can be increased to 22 µF for better input voltage filtering.

表 8 shows the recommended input/output capacitors.

表 8. Capacitors

CAPACITANCE (µF)	SIZE	CAPACITOR TYPE	SUPPLIER(1)	COMMENT
10	0603	GRM188R60J106ME84	Murata	Recommended
10	0402	CL05A106MP5NUNC	Samsung EMA	Smallest size

(1) See *Third-party Products Disclaimer*

9.3.22 Load Switch / LDO Output and Control

The device integrates a low Iq load switch which can also be used as a regulated output. The LSCTRL pin can be used to turn the load on or off. Activating LSCTRL continuously holds the switch in the on state so long as there is not a fault. The signal is active HI and has a low threshold making it capable of interfacing with low voltage signals. To limit voltage drop or voltage transients, a small ceramic capacitor must be placed close to VINLS. Due to the body diode of the PMOS switch, it is recommended to have the capacitor on VINLS ten times larger than the output capacitor on LS/LDO.

The output voltage is programmable using the LS_LDO bits in the register. The LS/LDO voltage is calculated using 式 9.

$$LS/LDO = 0.8\ V + LS\_LDOCODE \times 100\ mV \quad (9)$$

If a value greater than 3.3 V is written, the setting goes to pass-through mode where LS/LDO = VINLS - $V_{(DROPOUT)}$. 表 9 summarizes the control of the LS/LDO output based on the I^2C or LSCTRL pin setting:

表 9. LS/LDO Output Control

I^2C LS_LDO_EN	PIN LSCTRL	I^2C V_{LDO} > 3.3	LS/LDO Output
0	0	0	Pulldown
0	0	1	Pulldown
0	1	0	V_{LDO}
0	1	1	LSW
1	0	0	V_{LDO}
1	0	1	LSW
1	1	0	V_{LDO}
1	1	1	LSW

If the output of the LDO is less than the programmed $V_{(SYS)}$ voltage, connect VINLS to SYS. If the output of the LDO is greater than the programmed V_{SYS} voltage, connect VINLS to PMID.

The current capability of the LDO depends on the VINLS input voltage and the programmed output voltage. The full 100-mA output current for 0.8-V output voltage can be achieved when $V_{(VINLS)}$ > 3.25 V. The full 100-mA output current for 3.3-V output voltage can be achieved when $V_{(VINLS)}$ > 3.6 V.

When the LSLDO output is disabled with LSCTRL or through the register, an internal pull-down discharges the output.

9.3.23 Manual Reset Timer and Reset Output ($\overline{MR}$ and $\overline{RESET}$)

The $\overline{MR}$ input has an internal pull-up to BAT, and $\overline{MR}$ is functional only when BAT is present or when VIN is valid, stable, and charge is enabled. If $\overline{MR}$ input is asserted during a transient condition while VIN ramps up the IC may incorrectly turn off the SYS buck output, therefore $\overline{MR}$ should not be asserted during this condition in order to avoid unwanted shutdown of SYS output rail. The input conditions can be adjusted by using MRWAKE bits for the wake conditions and MRRESET bits for the reset conditions. When a wake condition is met, a 128-µs pulse is sent on INT to notify the host, and the WAKE1 and/or WAKE2 bits are updated on I^2C. The MR_WAKE bits and RESET FAULT bits are not cleared until the Push-button Control Register is read from I^2C.

When a $\overline{MR}$ reset condition is met, a 128us pulse is sent on INT to notify the host and a $\overline{RESET}$ signal is asserted. A reset pulse occurs with duration of t_{RESET_D} only one time after each valid MR$\overline{RESET}$ condition. The $\overline{MR}$ pin must be released (go high) and then driven low for the MRWAKE period before $\overline{RESET}$ asserts again. After $\overline{RESET}$ is asserted with battery only present, the device enters either Ship mode or Hi-Z mode depending on MRREC register settings. After $\overline{RESET}$ is asserted with a valid V_{IN} present, the device resumes operation prior to the $\overline{MR}$ button press. If SYS was disabled prior to $\overline{RESET}$, the SYS output is re-enabled if recovering into Hi-Z or Active Battery.

The MRRESET_VIN register can be configured to have $\overline{RESET}$ asserted by a button press only, or by a button press and V_{IN} present ($V_{UVLO} + V_{SLP} < V_{IN} < V_{OVP}$).

9.4 Device Functional Modes

表 10. Modes and Functions

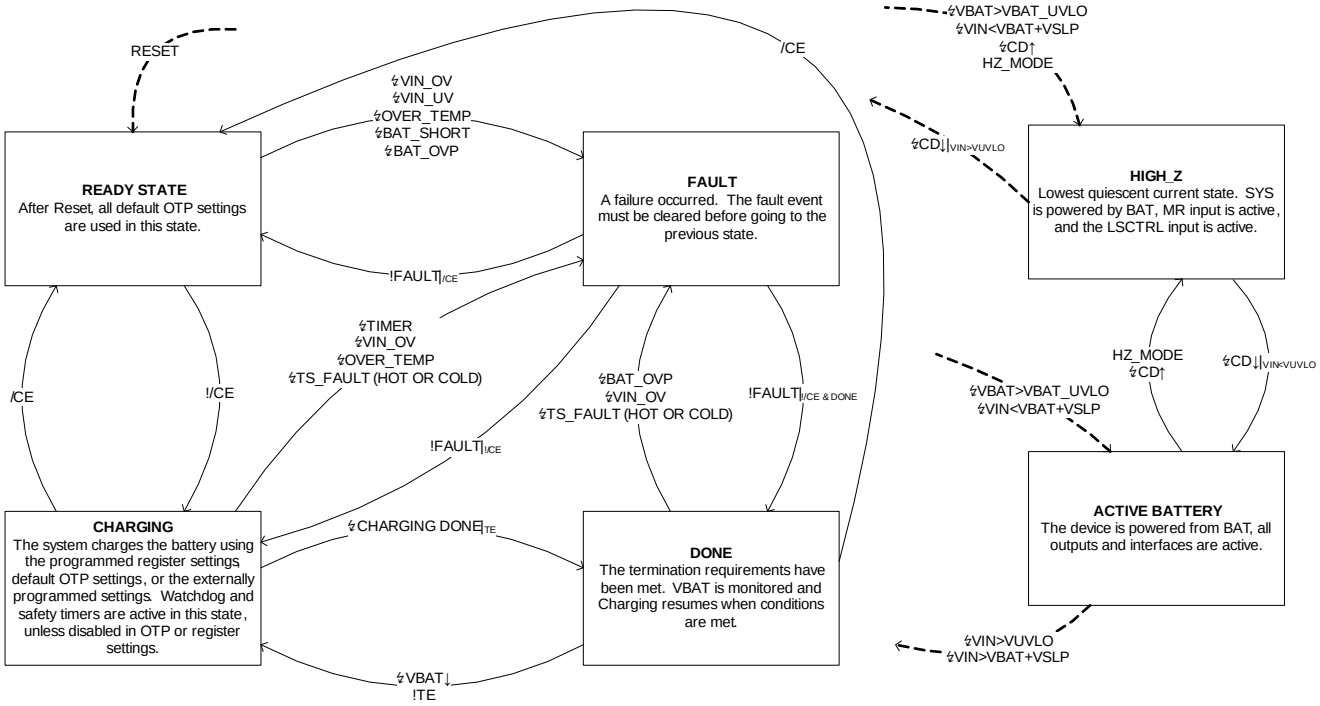
FUNCTION	READY (PRIOR TO I²C) AND AFTER RESET	HOST MODE READY (AFTER I²C)	CHARGE	SHIP MODE	HIGH_Z	ACTIVE BATTERY
VOVP	Yes	Yes	Yes	No	No	No
VUVLO	Yes	Yes	Yes	Yes	Yes	Yes
VBATUVLO	Yes	Yes	Yes	No	Yes	Yes
VINDPM	OTP or registers	OTP or registers	If enabled	No	No	No
SYS	OTP or registers	OTP or registers	If enabled	No	If enabled	If enabled
LS/LDO	OTP or registers	OTP or registers	If enabled	No	If enabled	If enabled
BATFET	Yes	Yes	Yes	No	Yes	Yes
TS	Yes (VIN Valid)	Yes (VIN Valid)	Yes	No	No	No
IPRETERM	External	OTP, registers, or external	OTP, registers, or external	No	No	No
ISET	External	OTP, registers, or external	OTP, registers, or external	No	No	No
ILIM	External	OTP, registers, or external	OTP, registers, or external	No	No	No
$\overline{MR}$ input	Yes	Yes	Yes	Yes	Yes	Yes
LSCTRL input	Yes	Yes	Yes	No	Yes	Yes
RESET output	Yes	Yes	Yes	No	Yes	Yes
INT output	Yes	Yes	Yes	No	No	Yes
I²C interface	Yes	Yes	Yes	No	No	Yes
$\overline{CD}$ input	Yes	Yes	Yes	No	Yes	Yes
$\overline{PG}$ output	Yes	Yes	Yes	No	No	If enabled
VBMON	No	Yes	No	No	No	Yes

表 11. Fault and Status Condition Responses

FAULT or STATUS	ACTIONS	CHARGER BEHAVIOR	SYS BEHAVIOR	LS/LDO BEHAVIOR	TS BEHAVIOR
VIN_OV	Update VIN_OV status, Update STAT to fault, interrupt on INT, $\overline{PG}$ shown not good	Disabled	Enabled through BAT	Enabled through BAT	Disabled
VIN_UV	Update VIN_UV status, Update STAT to fault, interrupt on INT, $\overline{PG}$ shown not good	Disabled	Enabled through BAT	Enabled through BAT	Disabled
VIN_ILIM	Update charge in progress status, interrupt on INT, input current is limited	Enabled, input current limited	Enabled (if enabled)	Enabled (if enabled)	Enabled
OVER_TEMP		Disabled	Disabled	Disabled	Disabled
BAT_UVLO	Update BAT_UVLO status, Update STAT to fault, interrupt on INT	Pre-charge	Enabled (if enabled) and VIN Valid	Enabled (if enabled) and VIN Valid	Enabled if VIN Valid
SW_SYS_SHORT		Enabled	Current Limit	Enabled (if enabled)	Enabled
LS_LDO_OCP		Enabled	Enabled (if enabled)	Current Limit	Enabled
TIMER fault	Update TIMER, Update STAT to fault, interrupt on INT	Disabled	Enabled (if enabled)	Enabled (if enabled)	Disabled
VINDPM	Update VINDPM_STAT, Update STAT to fault, interrupt on INT	Enabled, input current reduced	Enabled (if enabled)	Enabled (if enabled)	Enabled

表 11. Fault and Status Condition Responses (continued)

FAULT or STATUS	ACTIONS	CHARGER BEHAVIOR	SYS BEHAVIOR	LS/LDO BEHAVIOR	TS BEHAVIOR
TS_FAULT COLD or HOT	Update TS_FAULT to COLD OR HOT, Update STAT to fault, interrupt on INT	Disabled	Enabled (if enabled)	Enabled (if enabled)	Enabled
TS_FAULT COOL	Update TS_FAULT to COOL, Update STAT to fault, interrupt on INT	Reduce ICHG to ½	Enabled (if enabled)	Enabled (if enabled)	Enabled
TS_FAULT WARM	Update TS_FAULT to WARM, Update STAT to fault, interrupt on INT	Reduce VBATREG by 140 mV	Enabled (if enabled)	Enabled (if enabled)	Enabled
Charge Done	Update STAT to Charge Done, interrupt on INT	Disabled, monitor for VBAT falling below VRCHG	Enabled (if enabled)	Enabled (if enabled)	Enabled



Comments about naming convention

"/CE" or "HZ_MODE" -> Register name: event caused by user / configuration
"!" -> Not
"↯" -> Event caused by external influence
"Event|$_{condition}$" -> describes the event with a specific condition

図 17. State Diagram

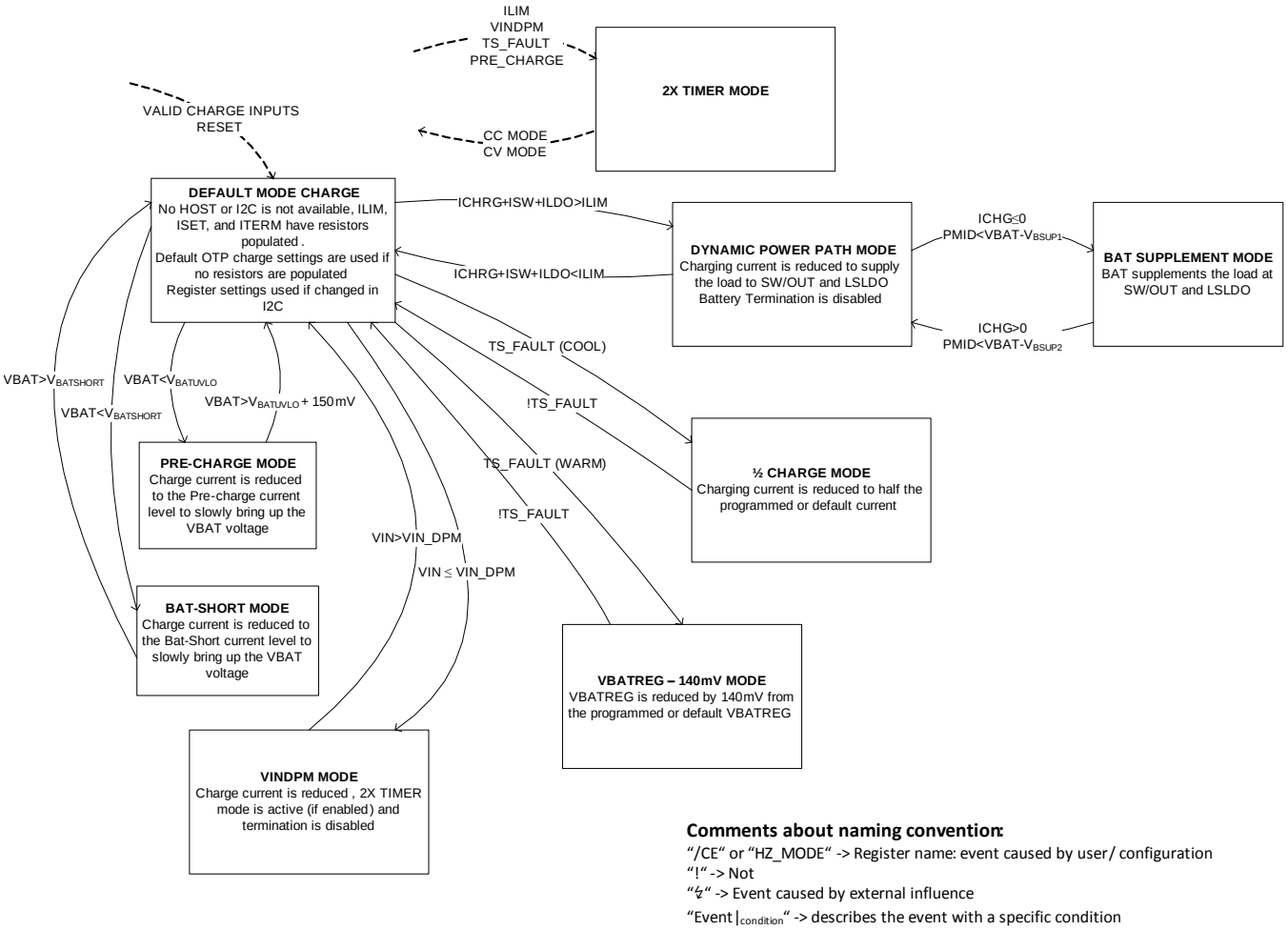


図 18. Change State Diagram

9.5 Programming

9.5.1 Serial Interface Description

The device uses an I^2C compatible interface to program and read many parameters. I^2C is a 2-wire serial interface developed by NXP. The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I^2C compatible devices connect to the I^2C bus through open drain I/O terminals, SDA and SCL. A master device, usually a microcontroller or digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and/or transmits data on the bus under control of the master device.

The device works as a slave and supports the following data transfer modes, as defined in the I^2C BUS Specification: standard mode (100 kbps) and fast mode (400kbps). The interface adds flexibility to the battery management solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. The I^2C circuitry is powered from the battery in active battery mode. The battery voltage must stay above $V_{(BATUVLO)}$ when no V_{IN} is present to maintain proper operation.

The data transfer protocol for standard and fast modes is exactly the same; therefore, they are referred to as the F/S-mode in this document. The device only supports 7-bit addressing. The device 7-bit address is 6A (8-bit shifted address is D4).

Programming (continued)

To avoid I^2C hang-ups, a timer ($t_{I2CRESET}$) runs duringI^2C transactions. If the SDA line is held low longer than $t_{I2CRESET}$, any additional commands are ignored and the I^2C engine is reset. The timeout is reset with START and repeated START conditions and stops when a valid STOP condition is sent.

9.5.2 F/S Mode Protocol

The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in 図 19. All I^2C-compatible devices should recognize a start condition.

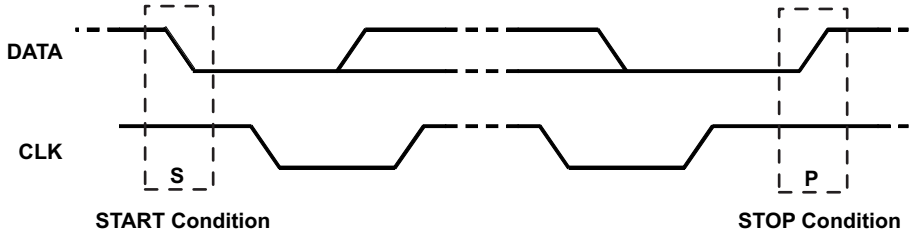


図 19. Start Stop Condition

The master then generates the SCL pulses, and transmits the address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see 図 20). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates and acknowledge (see 図 21) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting the acknowledge, the master knows that communication link with a slave has been established.

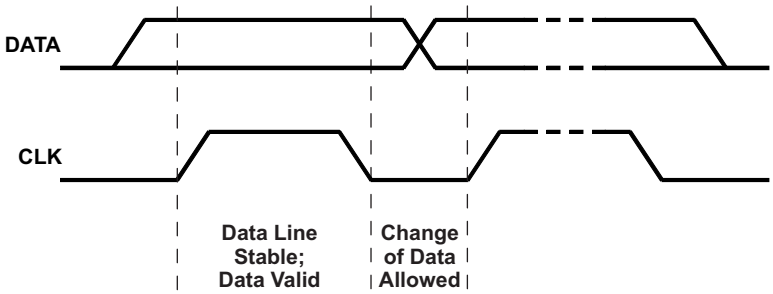


図 20. Bit Transfer on the Serial Interface

Programming (continued)

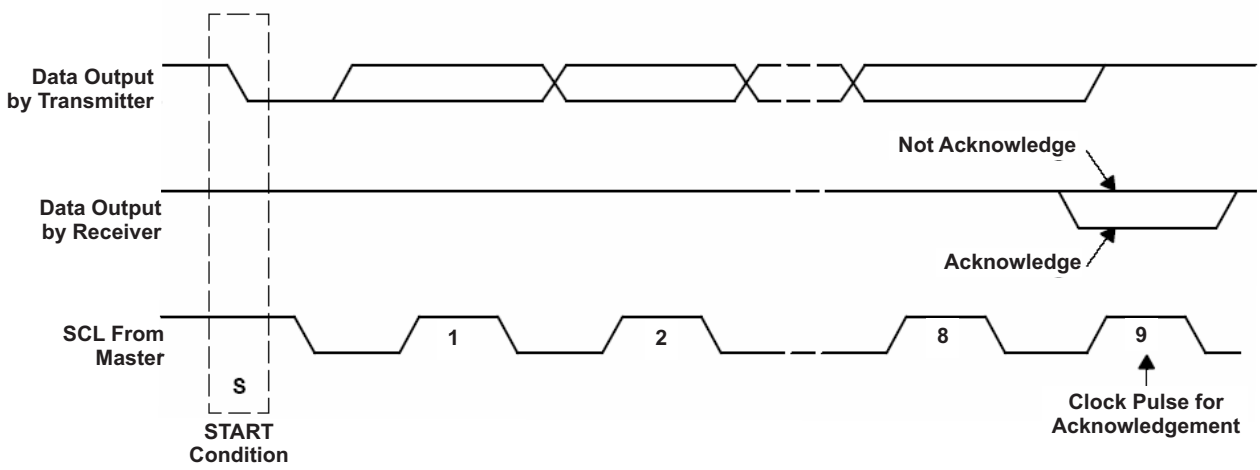


図 21. Acknowledge on the I²C Bus

The master generates further SCL cycles to either transmit data to the slave (R/W bit 0) or receive data from the slave (R/W bit 1). In either case, the receiver needs to acknowledge the data sent by the transmitter. An acknowledge signal can either be generated by the master or by the slave, depending on which on is the receiver. The 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary. To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see 図 22). This releases the bus and stops the communication link with the addressed slave. All I²C compatible devices must recognize the STOP condition. Upon the receipt of a STOP condition, all devices know that the bus is released, and wait for a START condition followed by a matching address. If a transaction is terminated prematurely, the master needs to send a STOP condition to prevent the slave I²C logic from remaining in an incorrect state. Attempting to read data from register addresses not listed in this section results in 0xFFh being read out.

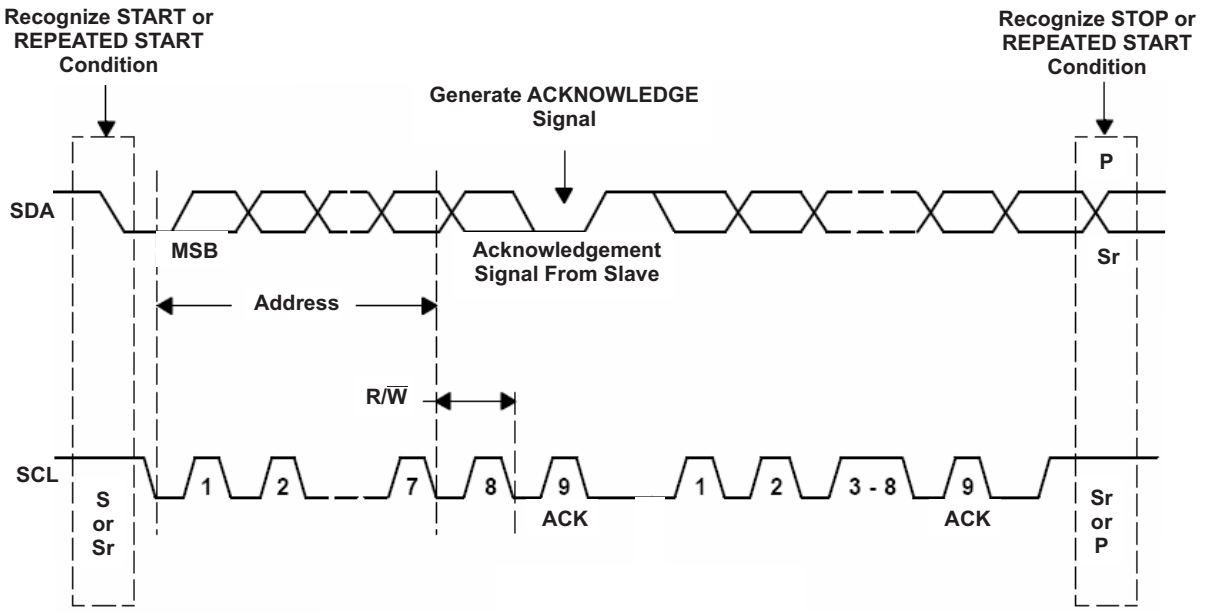


図 22. Bus Protocol

9.6 Register Maps

9.6.1 Status and Ship Mode Control Register

Memory location 0x00h, Reset State: xx0x xxx1 (bq25120)

図 23. Status and Ship Mode Control Register

7 (MSB)	6	5	4	3	2	1	0 (LSB)
x	x	0	x	x	x	x	1
R	R	Write Only	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 12. Status and Ship Mode Control Register

Bit	Field	Type	Reset	Description
B7 (MSB)	STAT_1	R	x	00 - Ready 01 - Charge in Progress 10 - Charge done 11 - Fault Status is current status only.
B6	STAT_0	R	x	
B5	EN_SHIPMODE	Write Only	0	0 – Normal Operation 1 – Ship Mode Enabled
B4	RESET_FAULT	R	x	1 – RESET fault. Indicates when the device meets the RESET conditions, and is cleared after I^2C read.
B3	TIMER	R	x	1 – Safety timer fault. Continues to show fault after an I^2C read unless the $\overline{CD}$ pin or power have been toggled.
B2	VINDPM_STAT	R	x	0 – VIN_DPM is not active 1 – VIN_DPM is active
B1	$\overline{CD}$_STAT	R	x	0 – $\overline{CD}$ low, IC enabled 1 – $\overline{CD}$ high, IC disabled
B0 (LSB)	SYS_EN_STAT	R	x	1 – SW enabled 0 – SW disabled

9.6.2 Faults and Faults Mask Register

Memory location 0x01h, Reset State: xxxx 0000 (bq25120)

図 24. Faults and Faults Mask Register

7 (MSB)	6	5	4	3	2	1	0 (LSB)
x	x	x	x	0	0	0	0
R	R	R	R	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 13. Faults and Faults Mask Register

Bit	Field	Type	Reset	Description
B7 (MSB)	VIN_OV	R	x	1 - V_{IN} overvoltage fault. VIN_OV continues to show fault after an I^2C read as long as OV exists
B6	VIN_UV	R	x	1 - V_{IN} undervoltage fault. VIN_UV is set when the input falls below V_{SLP}. VIN_UV fault shows only one time. Once read, VIN_UV clears until the the UVLO event occurs.
B5	BAT_UVLO	R	x	1 – BAT_UVLO fault. BAT_UVLO continues to show fault after an I^2C read as long as BAT_UVLO conditions exist.
B4	BAT_OCP	R	x	1 – BAT_OCP fault. BAT_OCP is cleared after I^2C read.
B3	VIN_OV_M	R/W	0	1 – Mask V_{IN} overvoltage fault
B2	VIN_UV_M	R/W	0	1 – Mask V_{IN} undervoltage fault
B1	BAT_UVLO_M	R/W	0	1 – Mask BAT UVLO fault
B0 (LSB)	BAT_OCP_M	R/W	0	1 – Mask BAT_OCP fault

9.6.3 TS Control and Faults Masks Register

Memory location 0x02h, Reset State: 1xxx 1000 (bq25120)

図 25. TS Control and Faults Masks Register (02)

7 (MSB)	6	5	4	3	2	1	0 (LSB)
1	x	x	x	1	0	0	0
R/W	R	R	R	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 14. TS Control and Faults Masks Register, Memory Location 0010

Bit	Field	Type	Reset	Description
B7 (MSB)	TS_EN	R/W	1	0 – TS function disabled 1 – TS function enabled
B6	TS_FAULT1	R	x	TS Fault mode: 00 – Normal, No TS fault 01 – TS temp < T_{COLD} or TS temp > T_{HOT} (Charging suspended) 10 – T_{COOL} > TS temp > T_{COLD} (Charging current reduced by half) 11 – T_{WARM} < TS temp < T_{HOT} (Charging voltage reduced by 140 mV)
B5	TS_FAULT0	R	x	
B4	TS_FAULT_OPEN	R	x	0 – No TS OFF fault 1 – TS OFF fault indicated, and charge has stopped (if enabled in OTP_EN_TS_OPEN)
B3	EN_INT	R/W	1	0 – Disable INT function (INT only shows faults and does not show charge status) 1 – Enable INT function (INT shows faults and charge status)
B2	WAKE_M	R/W	0	1 – Mask Wake Condition from $\overline{MR}$
B1	RESET_M	R/W	0	1 – Mask RESET condition from $\overline{MR}$
B0 (LSB)	TIMER_M	R/W	0	1 – Mask Timer fault (safety)

9.6.4 Fast Charge Control Register

Memory location 0x03h, Reset State: 0001 0100 (bq25120)

図 26. Fast Charge Control Register

7 (MSB)	6	5	4	3	2	1	0 (LSB)
0	0	0	1	0	1	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 15. Fast Charge Control Register

Bit	Field	Type	Reset	Description
B7 (MSB)	ICHRG_RANGE	R/W	0	0 – to select charge range from 5 mA to 35 mA, ICHRG bits are 1-mA steps 1 – to select charge range from 40 mA to 300 mA, ICHRG bits are 10-mA steps
B6	ICHRG_4	R/W	0	Charge current 16 mA or 160 mA
B5	ICHRG_3	R/W	0	Charge current 8 mA or 80 mA
B4	ICHRG_2	R/W	1	Charge current 4 mA or 40 mA
B3	ICHRG_1	R/W	0	Charge current 2 mA or 20 mA
B2	ICHRG_0	R/W	1	Charge current 1 mA or 10 mA
B1	$\overline{CE}$	R/W	0	0 – Charger enabled 1 – Charger is disabled
B0 (LSB)	HZ_MODE	R/W	0	0 – Not high impedance mode 1 – High impedance mode
ICHRG_RANGE and ICHRG bits are used to set the charge current. The I_{CHRG} is calculated using the following equation: If ICHRG_RANGE is 0, then I_{CHRG} = 5 mA + I_{CHRG}CODE x 1 mA. If ICHRG_RANGE is 1, then I_{CHRG} = 40 mA + I_{CHRG}CODE x 10 mA. If a value greater than 35 mA (ICHRG_RANGE = 0) or 300 mA (ICHRG_RANGE = 1) is written, the setting goes to 35 mA or 300 mA respectively except if the ICHRG bits are all 1 (that is, 11111), then the externally programmed value is used. The PRETERM bits must also be set prior to writing all 1s to ensure the external ISET current is used as well as the proper termination and pre-charge values are used. For IPRETERM = 5%, set the IPRETERM bits to 000001, for IPRETERM = 10%, set the IPRETERM bits to 000010, for IPRETERM = 15%, set the IPRETERM bits to 000100, and for IPRETERM = 20%, set the iPRETERM bits to 001000. The default is programmed by the external resistor on ISET, or if not populated and tied to GND, by OTP.				

9.6.5 Termination/Pre-Charge and I²C Address Register

Memory location 0x04h, Reset State: 0000 1110 (bq25120)

図 27. Termination/Pre-Charge and I²C Address Register

7 (MSB)	6	5	4	3	2	1	0 (LSB)
0	0	0	0	1	1	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 16. Termination/Pre-Charge and I²C Address Register

Bit	Field	Type	Reset	Description
B7 (MSB)	IPRETERM_RANGE	R/W	0	0 – to select termination range from 500 µA to 5 mA, IPRETERM bits are 500-µA steps 1 – to select charge range from 6 mA to 37 mA, IPRETERM bits are 1-mA steps
B6	IPRETERM_4	R/W	0	Termination current 8 mA or 16 mA
B5	IPRETERM_3	R/W	0	Termination current 4 mA or 8 mA
B4	IPRETERM_2	R/W	0	Termination current 2 mA or 4 mA
B3	IPRETERM_1	R/W	1	Termination current 1 mA or 2 mA
B2	IPRETERM_0	R/W	1	Termination current 500 µA or 1 mA
B1	TE	R/W	1	0 – Disable charge current termination 1 – Enable charge current termination
B0 (LSB)		R/W	0	
IPRETERM_RANGE and IPRETERM bits are used to set the termination and pre-charge current. The I_{TERM} is calculated using the following equation: If IPRETERM_RANGE is 0, then I_{TERM} = 500 µA + I_{TERM}CODE x 500 µA. If IPRETERM_RANGE is 1, then I_{TERM} = 6 mA + I_{TERM}CODE x 1 mA. If a value greater than 5 mA (IPRETERM_RANGE = 0) is written, the setting goes to 5 mA. Termination is disabled if any loop other than CC or DV in control, such as VINDPM, and TS/Cool. The default is programmed by the external resistor on IPRETERM, or if not populated and tied to GND, by OTP.				

9.6.6 Battery Voltage Control Register

Memory location 0x05h, Reset State: 0111 1000 (bq25120)

図 28. Battery Voltage Control Register

7 (MSB)	6	5	4	3	2	1	0 (LSB)
0	1	1	1	1	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 17. Battery Voltage Control Register

Bit	Field	Type	Reset	Description
B7 (MSB)	VBREG_6	R/W	0	Battery Regulation Voltage: 640 mV
B6	VBREG_5	R/W	1	Battery Regulation Voltage: 320 mV
B5	VBREG_4	R/W	1	Battery Regulation Voltage: 160 mV
B4	VBREG_3	R/W	1	Battery Regulation Voltage: 80 mV
B3	VBREG_2	R/W	1	Battery Regulation Voltage: 40 mV
B2	VBREG_1	R/W	0	Battery Regulation Voltage: 20 mV
B1	VBREG_0	R/W	0	Battery Regulation Voltage: 10 mV
B0 (LSB)		R/W	0	
VBREG Bits: Use VBREG bits to set the battery regulation threshold. The V_{BATREG} is calcuated using the following equation: V_{BATREG} = 3.6 V + V_{BREG}CODE x 10 mV. The charge voltage range is from 3.6 V to 4.65 V. If a value greater than 4.65 V is written, the setting goes to 4.65 V. Default is programmed by OTP.				

9.6.7 SYS VOUT Control Register

Memory location 0x06h, Reset State: 1010 1010 (bq25120)

図 29. SYS VOUT Control Register

7 (MSB)	6	5	4	3	2	1	0 (LSB)
1	0	1	0	1	0	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 18. SYS VOUT Control Register

Bit	Field	Type	Reset	Description
B7 (MSB)	EN_SYS_OUT	R/W	1	0 – Disable SW 1 – Enable SW (When disabled, output is pulled low)
B6	SYS_SEL1	R/W	0	00 – 1.1 V and 1.2 V selection 01 – 1.3 V through 2.8 V selection, 10 – Not Valid 11 – 1.8 V through 3.3 V selection
B5	SYS_SEL0	R/W	1	
B4	SYS_VOUT_3	R/W	0	OUT Voltage: 800 mV step if SYS_SEL is 01 or 11
B3	SYS_VOUT_2	R/W	1	OUT Voltage: 400 mV step if SYS_SEL is 01 or 11
B2	SYS_VOUT_1	R/W	0	OUT Voltage: 200 mV step if SYS_SEL is 01 or 11
B1	SYS_VOUT_0	R/W	1	OUT Voltage: 100 mV step if SYS_SEL is 01 or 11
B0 (LSB)			0	
SW_VOUT Bits: Use SYS_SEL and SYS_VOUT bits to set the output on SYS. The SYS voltage is calculated using the following equation: See table below for all VOUT values that can be programmed through SYS_SEL and SYS_VOUT. If SYS_SEL = 01, then SYS = 1.30 V + SYS_VOUTCODE x 100 mV. If SYS_SEL = 11, then SYS = 1.80 V + SYS_VOUTCODE x 100 mV.				

表 19. SYS_SEL Codes

SYS_SEL	SYS_VOUT	TYP	UNIT
00	0000	1.1	V
00	0001	1.2	V
00	0010	1.25	V
00	0011	1.333	V
00	0100	1.417	V
00	0101	1.5	V
00	0110	1.583	V
00	0111	1.667	V
00	1000	1.75	V
00	1001	1.833	V
00	1010	1.917	V
00	1011	2	V
00	1100	2.083	V
00	1101	2.167	V
00	1110	2.25	V
00	1111	2.333	V
01	0000	1.3	V
01	0001	1.4	V
01	0010	1.5	V
01	0011	1.6	V
01	0100	1.7	V
01	0101	1.8	V
01	0110	1.9	V

表 19. SYS_SEL Codes (continued)

SYS_SEL	SYS_VOUT	TYP	UNIT
01	0111	2	V
01	1000	2.1	V
01	1001	2.2	V
01	1010	2.3	V
01	1011	2.4	V
01	1100	2.5	V
01	1101	2.6	V
01	1110	2.7	V
01	1111	2.8	V
10	0000	1.5	V
10	0001	1.583	V
10	0010	1.667	V
10	0011	1.75	V
10	0100	1.833	V
10	0101	1.917	V
10	0110	2	V
10	0111	2.083	V
10	1000	2.167	V
10	1001	2.25	V
10	1010	2.333	V
10	1011	2.417	V
10	1100	2.5	V
10	1101	2.583	V
10	1110	2.667	V
10	1111	2.75	V
11	0000	1.8	V
11	0001	1.9	V
11	0010	2	V
11	0011	2.1	V
11	0100	2.2	V
11	0101	2.3	V
11	0110	2.4	V
11	0111	2.5	V
11	1000	2.6	V
11	1001	2.7	V
11	1010	2.8	V
11	1011	2.9	V
11	1100	3	V
11	1101	3.1	V
11	1110	3.2	V
11	1111	3.3	V

9.6.8 Load Switch and LDO Control Register

Memory location 0x07h, Reset State: 0111 110x (bq25120)

図 30. Load Switch and LDO Control Register

7 (MSB)	6	5	4	3	2	1	0 (LSB)
0	1	1	1	1	1	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 20. Load Switch and LDO Control Register

Bit	Field	Type	Reset	Description
B7 (MSB)	EN_LS_LDO	R/W	0	0 – Disable LS/LDO 1 – Enable LS/LDO
B6	LS_LDO_4	R/W	1	LS/LDO Voltage: 1600 mV
B5	LS_LDO_3	R/W	1	LS/LDO Voltage: 800 mV
B4	LS_LDO_2	R/W	1	LS/LDO Voltage: 400 mV
B3	LS_LDO_1	R/W	1	LS/LDO Voltage: 200 mV
B2	LS_LDO_0	R/W	1	LS/LDO Voltage: 100 mV
B1			0	
B0 (LSB)	MRRESET_VIN	R/W	x	0 – Reset sent when $\overline{MR}$ Reset time is met 1 – Reset sent when $\overline{MR}$ Reset time is met and V_{UVLO} + V_{SLP} < VIN < V_{OVP}
LS_LDO Bits: Use LS_LDO bits to set the LS/LDO output. The LS/LDO voltage is calculated using the following equation: LS/LDO = 0.8 V + LS_LDOCODE x 100 mV. If a value greater than 3.3 V is written, the setting goes to pass-through mode where LS/LDO = VINLS - $V_{DROPOUT}$. The LS_LDO output can only be changed when the EN_LS_LDO and LSCTRL pin has disabled the output.				

9.6.9 Push-button Control Register

Memory location 0x08h, Reset State: 0110 10xx (bq25120)

図 31. Push-button Control Register

7 (MSB)	6	5	4	3	2	1	0 (LSB)
0	1	1	0	1	0	x	x
R/W	R/W	R/W	R/W	R/W	R/W	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 21. Push-button Control Register

Bit	Field	Type	Reset	Description
B7 (MSB)	MRWAKE1	R/W	0	$\overline{MR}$ Timer adjustment for WAKE1: 0 – 50 ms < $\overline{MR}$ 1 – 500 ms < $\overline{MR}$
B6	MRWAKE2	R/W	1	$\overline{MR}$ Timer adjustment for WAKE2: 0 –1000 ms < $\overline{MR}$ 1 – 1500 ms < $\overline{MR}$
B5	MRREC	R/W	1	0 – After Reset, device enters Ship mode 1 – After Reset, device enters Hi-Z Mode
B4	MRRESET_1	R/W	0	$\overline{MR}$ Timer adjustment for reset: 00 – 4 s ± 10% 01 - 8 s ± 10% 10 - 10 s ± 10% 11 - 14 s ± 10%
B3	MRRESET_0	R/W	1	
B2	PGB_MR	R/W	0	0 – Output functions as $\overline{PG}$ 1 – Output functions as voltage shifted push-button ($\overline{MR}$) input
B1	WAKE1	R	x	1 – WAKE1 status. Indicates when the device meets the WAKE1 conditions, and is cleared after I^2C read.
B0 (LSB)	WAKE2	R	x	1 – WAKE2 status. Indicates when the device meets the WAKE2 conditions, and is cleared after I^2C read.

9.6.10 ILIM and Battery UVLO Control Register

Memory location 0x09h, Reset State: 0000 1010 (bq25120)

図 32. ILIM and Battery UVLO Control Register

7 (MSB)	6	5	4	3	2	1	0 (LSB)
0	0	0	0	1	0	1	0
Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 22. ILIM and Battery UVLO Control Register, Memory Location 1001

Bit	Field	Type	Reset	Description
B7 (MSB)	RESET	Write only	0	Write: 1- Reset all registers to default values 0 – No effect Read: Always get 0
B6		R/W	0	N/A
B5	INLIM_2	R/W	0	Input Current Limit: 200 mA
B4	INLIM_1	R/W	0	Input Current Limit: 100 mA
B3	INLIM_0	R/W	1	Input Current Limit: 50 mA
B2	BUVLO_2	R/W	0	000, 001, 010: BUVLO = 3 V 011: BUVLO = 2.8 V 100: BUVLO = 2.6 V 101: BULVO = 2.4 V 110: BUVLO = 2.2 V 111: BUVLO = Disabled
B1	BUVLO_1	R/W	1	
B0 (LSB)	BUVLO_0	R/W	0	
INLIM Bits: Use INLIM bits to set the input current limit. The $I_{(INLIM)}$ is calculated using the following equation: $I_{(INLIM)}$ = 50 mA + $I_{(INLIM)}$CODE x 50 mA. The default is programmed by the external resistor on ILIM, or if not populated and tied to GND, by OTP.				

9.6.11 Voltage Based Battery Monitor Register

Memory location 0x0Ah, Reset State: 0xxx xxxx (bq25120)

図 33. Voltage Based Battery Monitor Register

7 (MSB)	6	5	4	3	2	1	0 (LSB)
0	x	x	x	x	x	x	x
R/W	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 23. Voltage Based Battery Monitor Register, Memory Location 1010

Bit	Field	Type	Reset	Description
B7 (MSB)	VBMON_READ	R/W	0	Write 1 to initiate a new VBATREG reading. Read always 0.
B6	VBMON_RANGE_1	R	x	11 – 90% to 100% of VBATREG 10 – 80% to 90% of VBATREG 01 – 70% to 80% of VBATREG 00 – 60% to 70% of VBATREG
B5	VBMON_RANGE_0	R	x	
B4	VBMON_TH_2	R	x	111 – Above 8% of VBMON_RANGE 110 – Above 6% of VBMON_RANGE 011 – Above 4% of VBMON_RANGE 010 – Above 2% of VBMON_RANGE 001 – Above 0% of VBMON_RANGE
B3	VBMON_TH_1	R	x	
B2	VBMON_TH_0	R	x	
B1		R	x	N/A
B0 (LSB)		R	x	N/A
The VBMON registers are used to determine the battery voltage. Before entering a low power state, the device will determine the voltage level by starting at VBMON_RANGE 11 (90% to 100%), and if VBMON_TH of 000 is read, then it will move to VBMON_RANGE 10 (80% to 90%) and continue until a non 000 value of VBMON_TH is found. If this does not happen, then VBMON_RANGE and VBMON_TH will be written with 00 000. The VBMON_READ bit can be used to initiate a new reading by writing a 1 to it. Example: A reading of 10 011 indicated a VBAT voltage of between 84% and 86% of the VBATREG setting.				

9.6.12 VIN_DPM and Timers Register

Memory location 0x0Bh, Reset State: 0100 1010 (bq25120)

図 34. VIN_DPM and Timers Register

7 (MSB)	6	5	4	3	2	1	0 (LSB)
0	1	0	0	1	0	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 24. VIN_DPM and Timers Register

Bit	Field	Type	Reset	Description
B7 (MSB)	VINDPM_ON	R/W	0	0 - enable VINDPM 1 - disable VINDPM
B6	VINDPM_2	R/W	1	Input $V_{(IN\_DPM)}$ voltage: 400 mV
B5	VINDPM_1	R/W	0	Input $V_{(IN\_DPM)}$ voltage: 200 mV
B4	VINDPM_0	R/W	0	Input $V_{(IN\_DPM)}$ voltage: 100 mV
B3	2XTMR_EN	R/W	1	0 – Timer is not slowed at any time 1 – Timer is slowed by 2x when in any control other than CC or CV
B2	TMR_1	R/W	0	Safety Timer Time Limit 00 – 30 minute fast charge 01 – 3 hour fast charge 10 – 9 hour fast charge 11 – Disable safety timers
B1	TMR_0	R/W	1	
B0 (LSB)			0	
The VINDPM threshold is set using the following equation: VINDPM = 4.2 + VINDPM_CODE x 100 mV				

10 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

A typical design is shown in 図 35. This design uses the BQ25120 with external resistors for ILIM, IPRETERM, and ISET. These are not needed if these values are set with a host controller through I^2C commands. This design also shows the TS resistors, which is also optional.

When powering up in default mode the battery voltage is the default for the part (4.2 V), the SYS output is the default (1.8 V). External resistors set the charge current to 40 mA, the termination current to 10% (4 mA), and the input current limit to 100 mA. If the I^2C interface is used the part goes to the internal default settings until changed by the host.

10.2 Typical Application

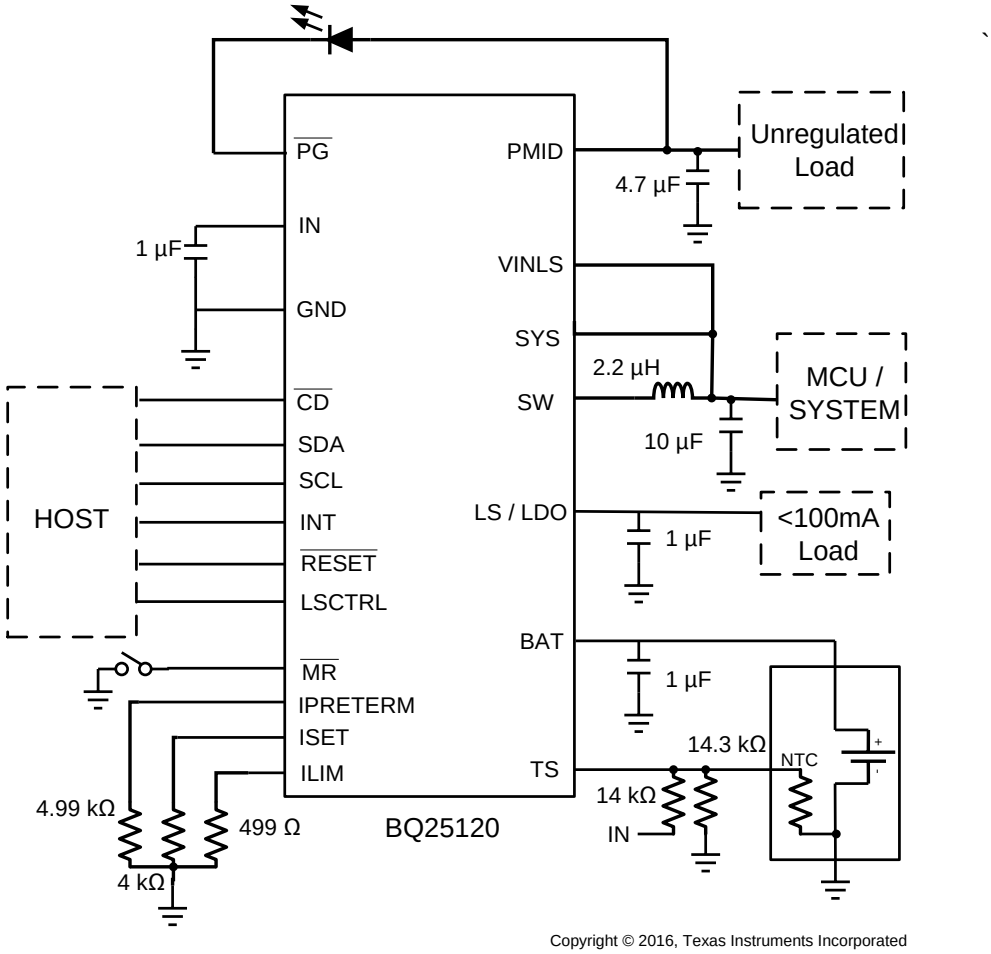


図 35. Typical Application Circuit

Typical Application (continued)

10.2.1 Design Requirements

This application is for a low power system that has varying loads from less than 10 mA up to 300 mA. It must work with a valid adaptor or USB power input. Below are some of the key components that are needed in normal operation. For this example, the fast charge current is 50 mA, input current limit is 400 mA and the pre-charge and termination current is 10% of the fast charge current.

- Supply voltage = 3.4 V to 20 V
- Fast charge current is default to 10 mA with ISET pin shorted to ground. To program the fast charge current, connect an external resistor from ISET to ground.
- Input current limit is default to 100 mA with ILIM pin shorted to ground. To program the input current limit, connect an external resistor from ILIM to ground.
- Termination current threshold is default to 2 mA with IPRETERM pin shorted to ground. To program the input current limit, connect an external resistor from IPRETERM to ground.
- A 2.2-µH inductor is needed between SW pin and SYS pin for PWM output.
- TS- Battery temperature sense needs a NTC connected on TS pin.

10.2.2 Detailed Design Procedure

See 図 35 for an example of the application diagram.

10.2.2.1 Default Settings

- • Connect ISET, ILIM and IPRETERM pins to ground to program fast charge current to 10mA, input current limit to 100mA and pre-charge/termination current to 2 mA.
- BAT_UVLO = 3 V.
- VSYS = 1.8 V
- LS/LDO is LS
- VBREG = 4.2 V
- VIN_DPM is enabled and VIN_DPM Threshold = 4.6 V.
- Safety Timer = 3 hr
- If the function is not needed, connect TS to the center tab of the resistor divider between V_{IN} and the ground. (pull up resistor = 14 kΩ, pull down resistor = 14.3 kΩ)

10.2.2.2 Choose the Correct Inductance and Capacitance

Refer to the *Buck (PWM) Output* section for the detailed procedure to determine the optimal inductance and capacitance for the buck output.

10.2.2.3 Calculations

10.2.2.3.1 Program the Fast Charge Current (ISET)

$$R_{ISET} = K_{ISET}/ICHG \quad (10)$$

K_{ISET} = 200 AΩ from the *Specifications* table

$$R_{ISET} = 200\ A\Omega / 0.05A = 4\ k\Omega \quad (11)$$

Select the closest standard value, which in this case is 4.99 kΩ. Connect this resistor between ISET pin and GND.

10.2.2.3.2 Program the Input Current Limit (ILIM)

$$R_{ILIM} = K_{ILIM}/I_{I\_MAX} \quad (12)$$

K_{ILIM} = 200 AΩ from the *Specifications* table

$$R_{ILIM} = 200\ A\Omega / 0.4A = 500\ \Omega \quad (13)$$

Select the closest standard value, which in this case is 499 Ω. Connect this resistor between ILIM pin and GND.

Typical Application (continued)

10.2.2.3.3 Program the Pre-charge/termination Threshold (IPRETERM)

According to 表 3, the RIPRETERM is 4990 Ω for 10% termination threshold. Therefore, connect a 4.99 kΩ resistor between IPRETERM pin and GND.

10.2.2.3.4 TS Resistors (TS)

The voltage at TS is monitored to determine that the battery is at a safe temperature during charging. This device uses JEITA temperature profile which has four temperature thresholds. Refer to *Specifications* for the detailed thresholds number.

The TS circuit is shown in 図 16. The resistor values can be calculated using 式 1 and 式 2.

Typical Application (continued)

10.2.3 Application Performance Curves

10.2.3.1 Charger Curves

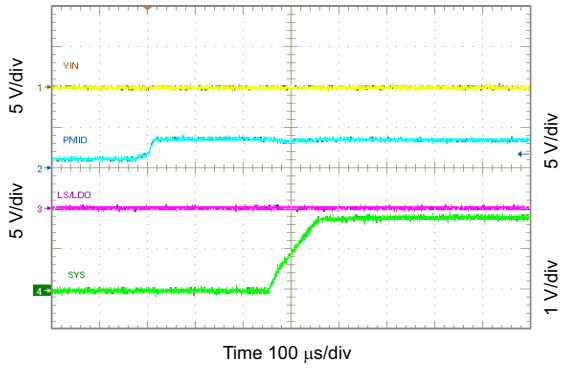


図 36. Battery Connected to $V_{(BAT)}$

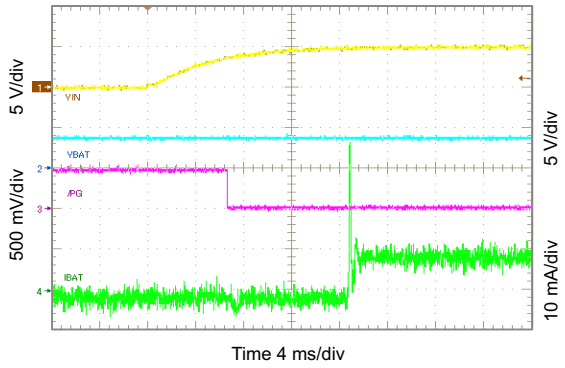


図 37. Power Supply Connected to V_{IN}

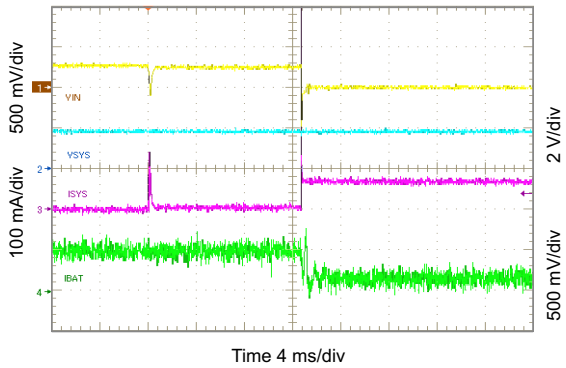


図 38. Entering DPPM Mode

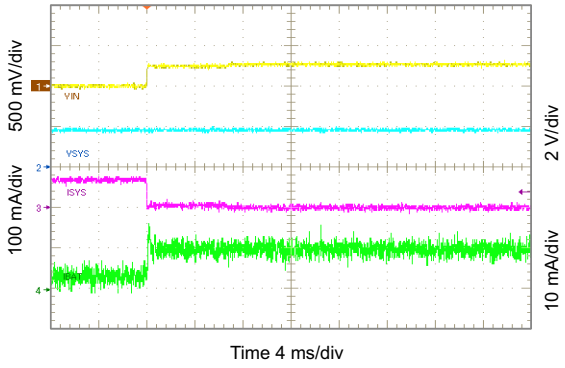


図 39. Exiting DPPM Mode

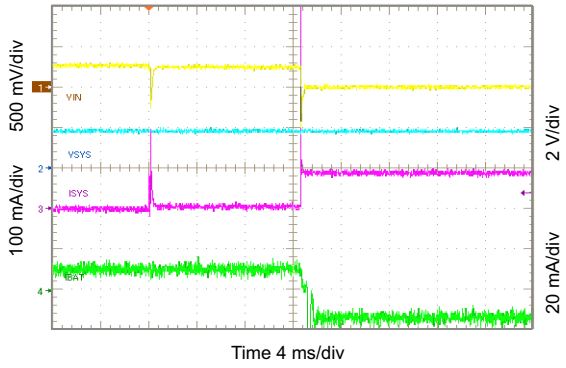


図 40. Entering Battery Supplement Mode

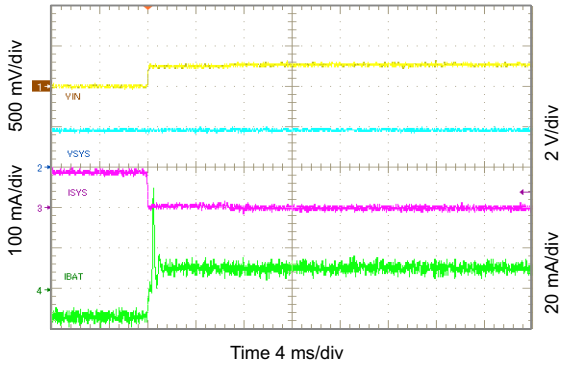


図 41. Exiting Battery Supplement Mode

Typical Application (continued)

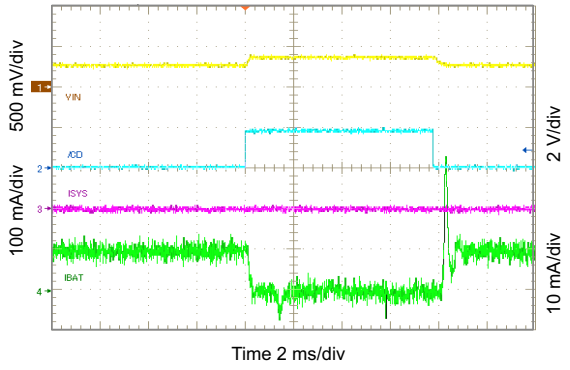


図 42. Charger On/Off Using $\overline{CD}$

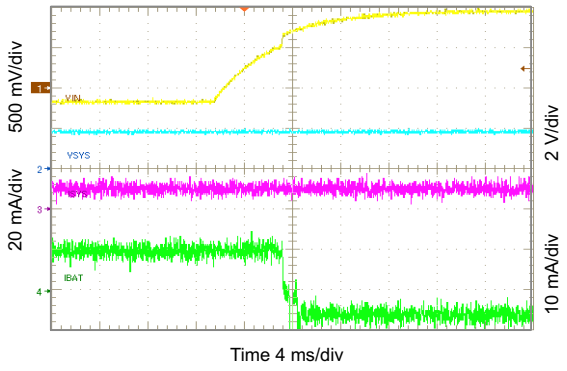
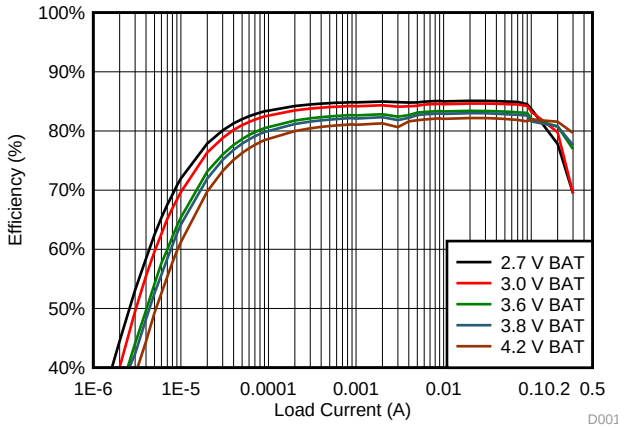


図 43. OVP Fault

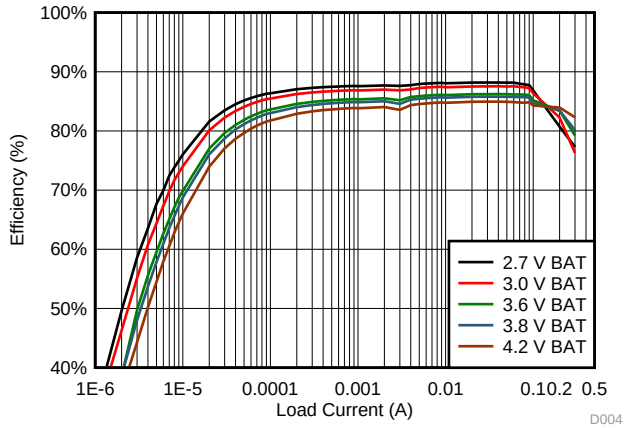
Typical Application (continued)

10.2.3.2 SYS Output Curves



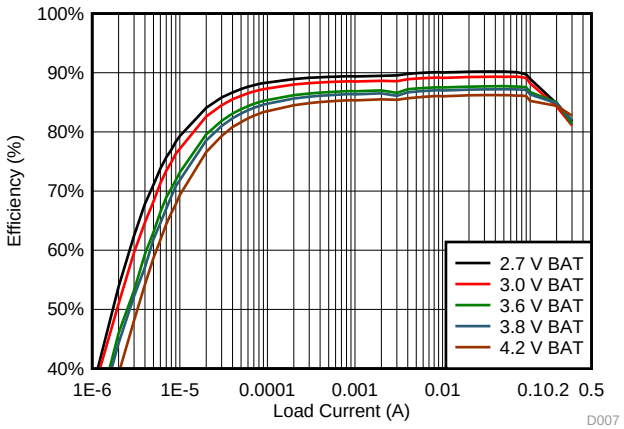
T_A = 25°C V_{SYS} = 1.2 V

図 44. 1.2 V_{SYS} System Efficiency



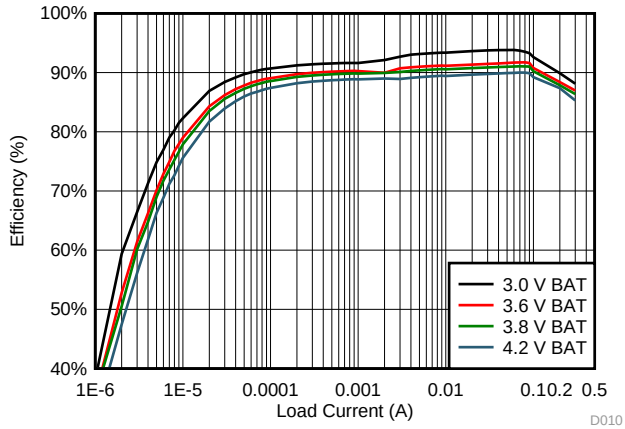
T_A = 25°C V_{SYS} = 1.5 V

図 45. 1.5 V_{SYS} System Efficiency



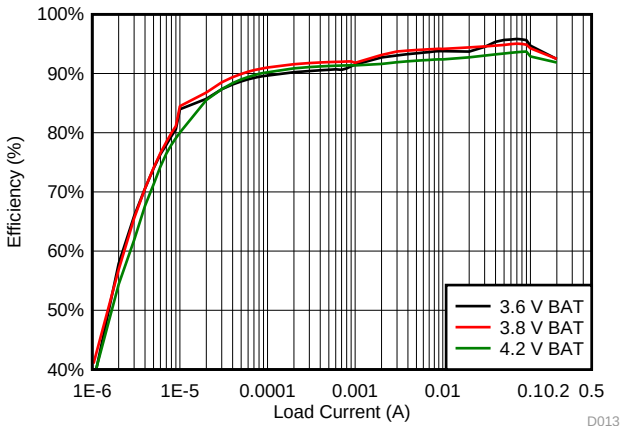
T_A = 25°C V_{SYS} = 1.8 V

図 46. 1.8 V_{SYS} System Efficiency



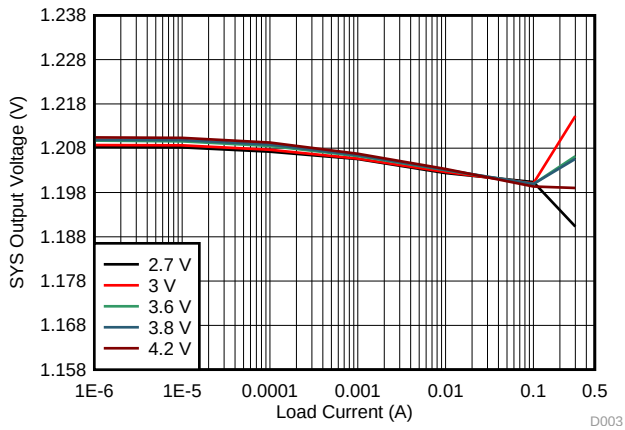
T_A = 25°C V_{SYS} = 2.5 V

図 47. 2.5 V_{SYS} System Efficiency



T_A = 25°C V_{SYS} = 3.3 V

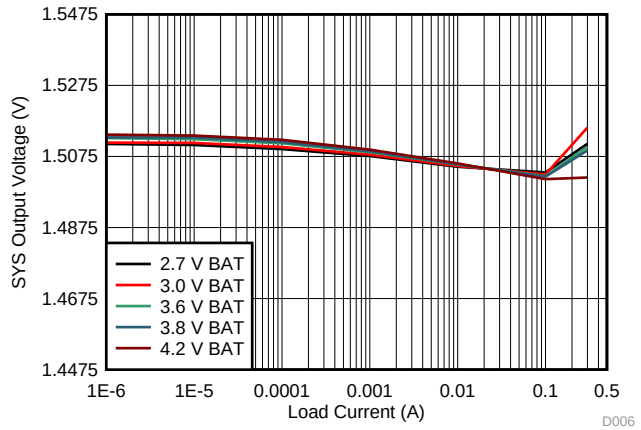
図 48. 3.3 V_{SYS} System Efficiency



T_A = 25°C V_{SYS} = 1.2 V

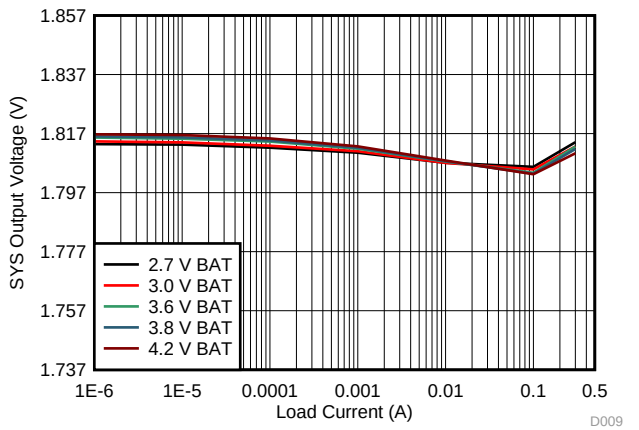
図 49. 1.2 V_{SYS} Load Regulation

Typical Application (continued)



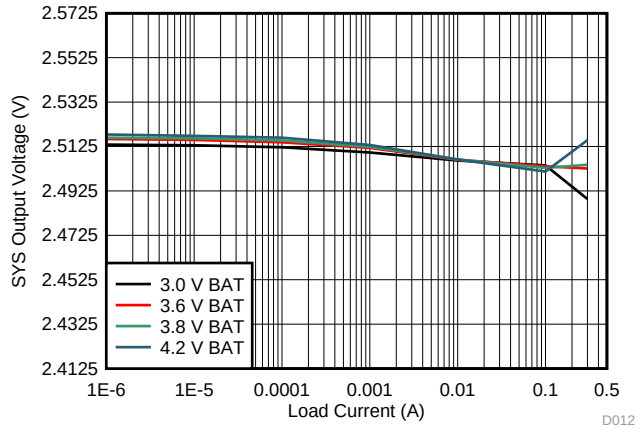
T_A = 25°C V_{SYS} = 1.5 V

図 50. 1.5 V_{SYS} Load Regulation



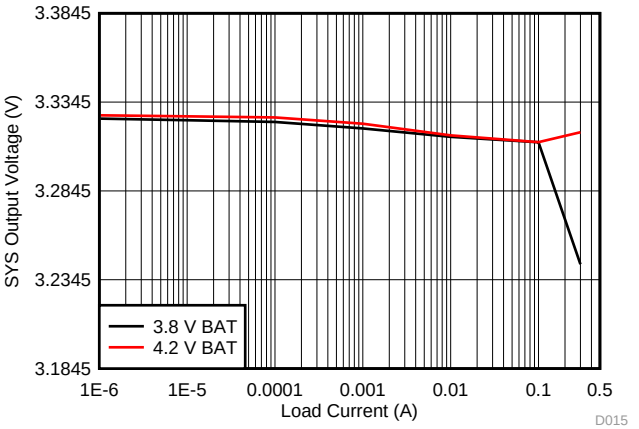
T_A = 25°C V_{SYS} = 1.8 V

図 51. 1.8 V_{SYS} Load Regulation



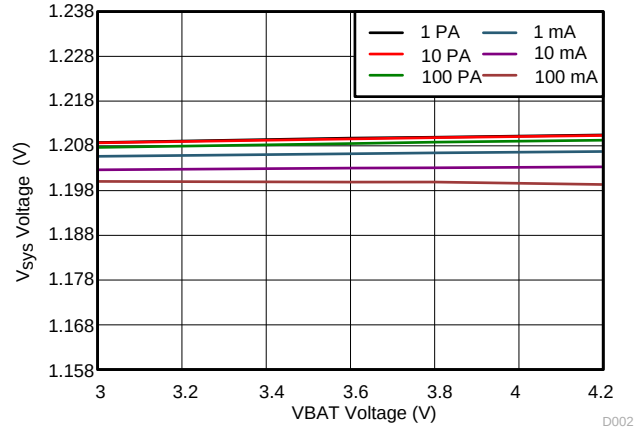
T_A = 25°C V_{SYS} = 2.5 V

図 52. 2.5 V_{SYS} Load Regulation



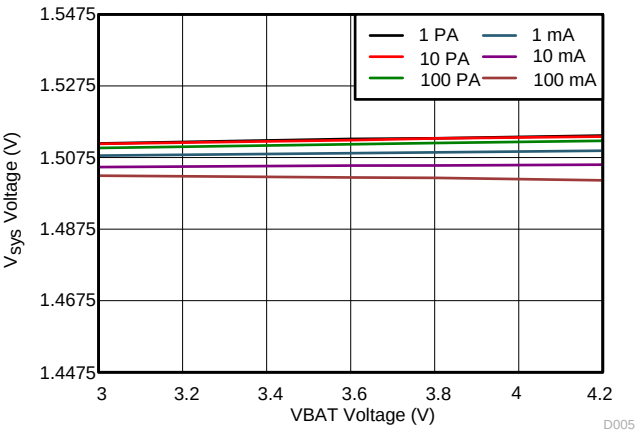
T_A = 25°C V_{SYS} = 3.3 V

図 53. 3.3 V_{SYS} Load Regulation



T_A = 25°C V_{SYS} = 1.2 V

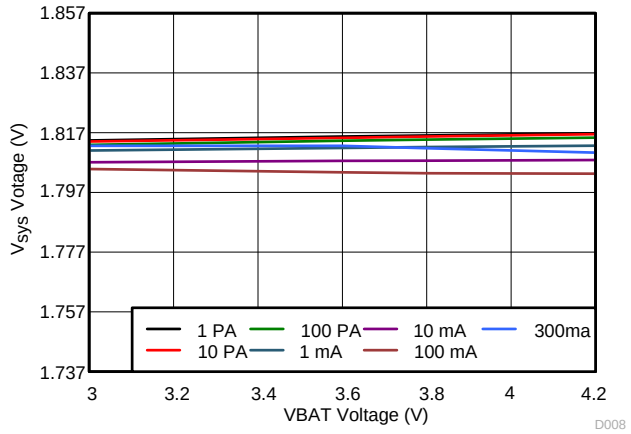
図 54. 1.2 V_{SYS} Line Regulation



T_A = 25°C V_{SYS} = 1.5 V

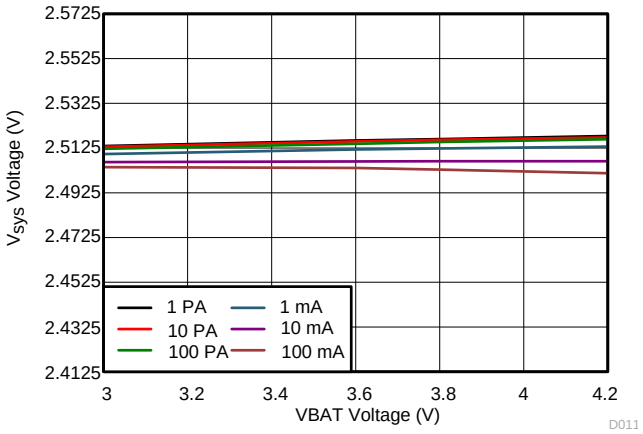
図 55. 1.5 V_{SYS} Line Regulation

Typical Application (continued)



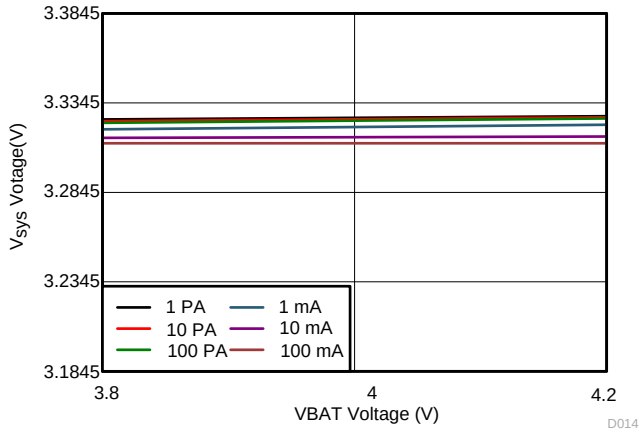
T_A = 25°C V_{SYS} = 1.8 V

図 56. 1.8 V_{SYS} Line Regulation



T_A = 25°C V_{SYS} = 2.1 V

図 57. 2.1 V_{SYS} Line Regulation



T_A = 25°C V_{SYS} = 3.3 V

図 58. 3.3 V_{SYS} Line Regulation

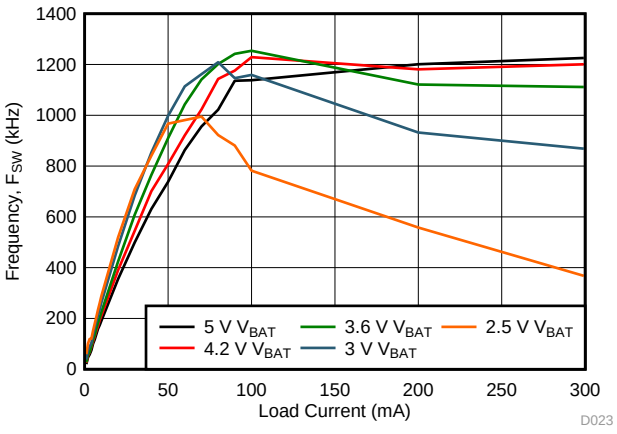
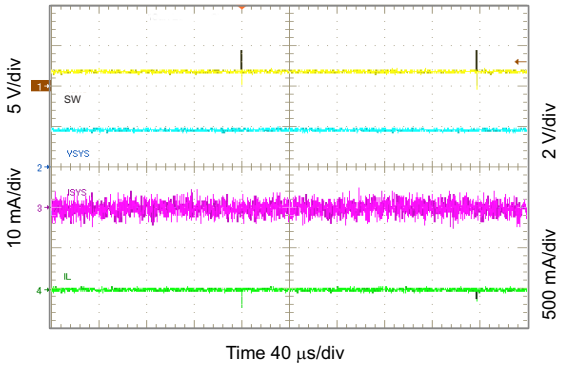
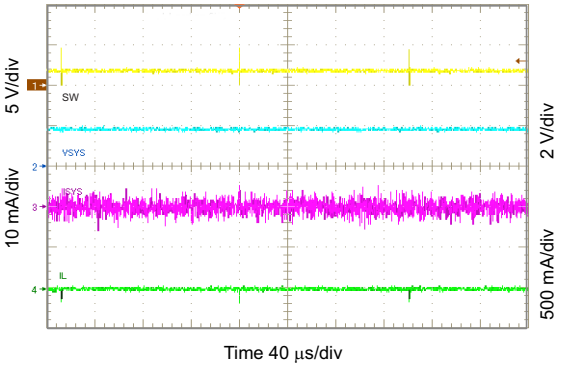


図 59. 1.8 V_{SYS} Switching Frequency vs Load Current



I_{LOAD} = 10 µA

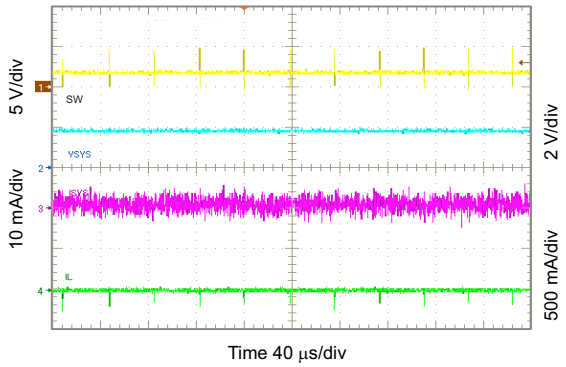
図 60. Light Load Operation Showing SW



I_{LOAD} = 100 mA

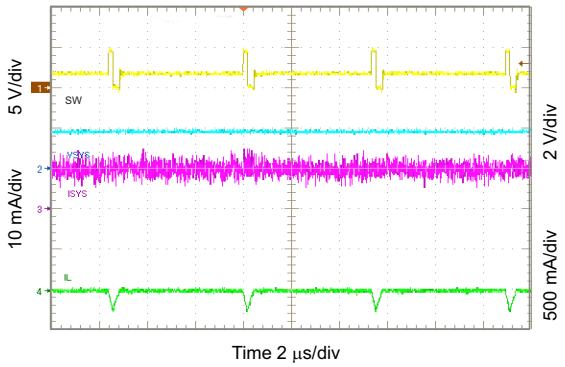
図 61. Light Load Operation Showing SW

Typical Application (continued)



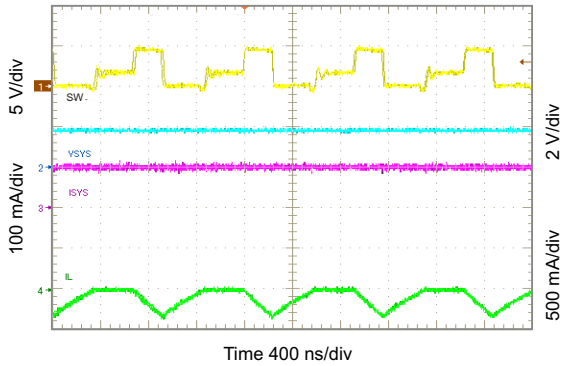
I_{LOAD} = 1 mA

図 62. Light Load Operation Showing SW



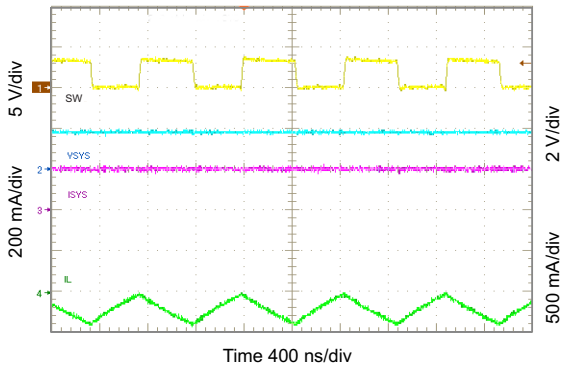
I_{LOAD} = 10 mA

図 63. Light Load Operation Showing SW



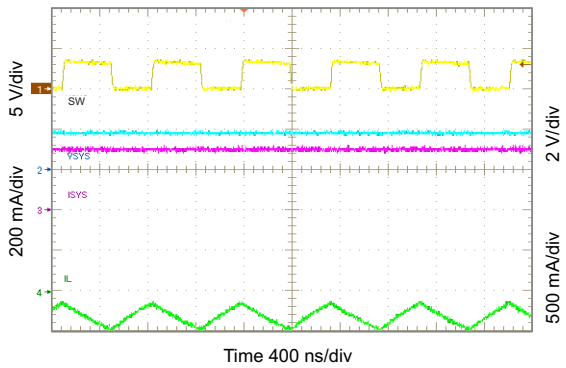
I_{LOAD} = 100 mA

図 64. Light Load Operation Showing SW



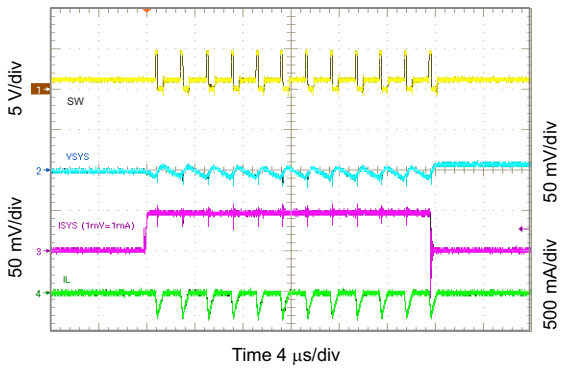
I_{LOAD} = 200 mA

図 65. Light Load Operation Showing SW



I_{LOAD} = 300 mA

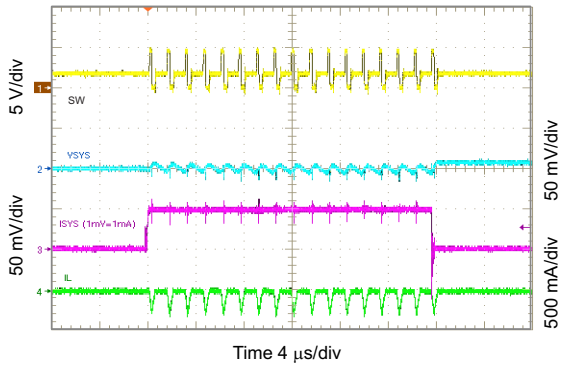
図 66. Light Load Operation Showing SW



V_{SYS} = 1.2 V

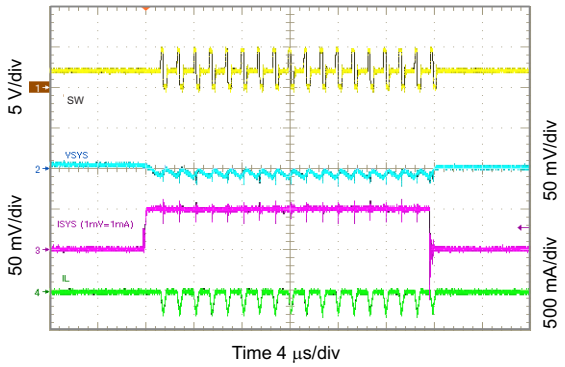
図 67. 1.2 V_{SYS} Load Transient, 0 to 50 mA

Typical Application (continued)



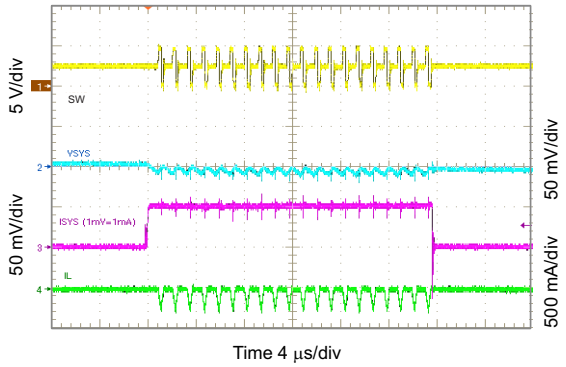
V_{SYS} = 1.8 V

図 68. 1.8 V_{SYS} Load Transient, 0 to 50 mA



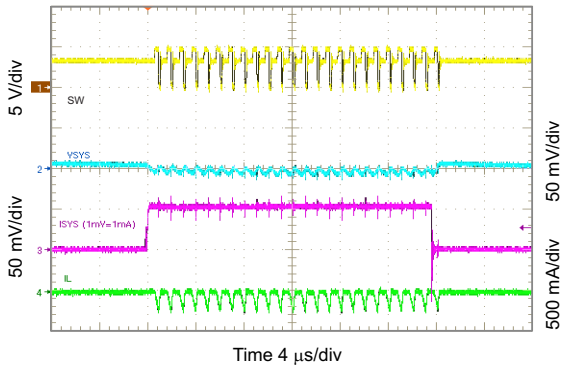
V_{SYS} = 2.1 V

図 69. 2.1 V_{SYS} Load Transient, 0 to 50 mA



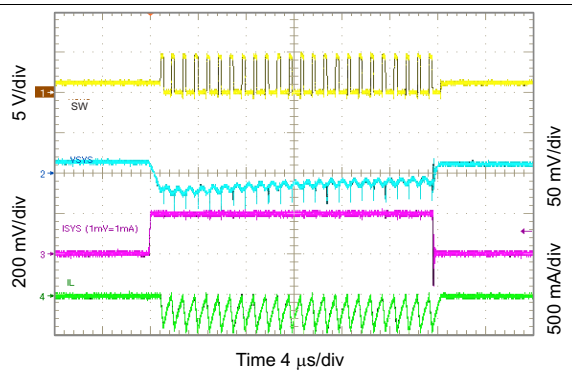
V_{SYS} = 2.5 V

図 70. 2.5 V_{SYS} Load Transient, 0 to 50 mA



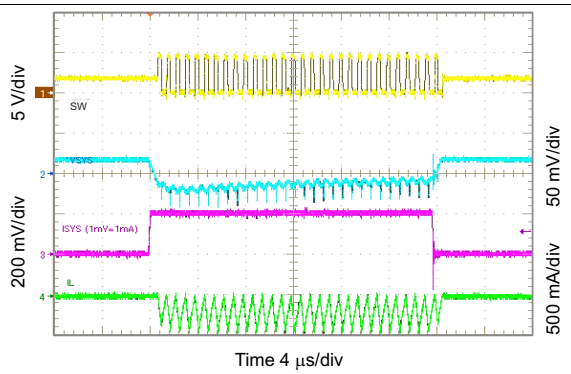
V_{SYS} = 3.3 V

図 71. 3.3 V_{SYS} Load Transient, 0 to 50 mA



V_{SYS} = 1.2 V

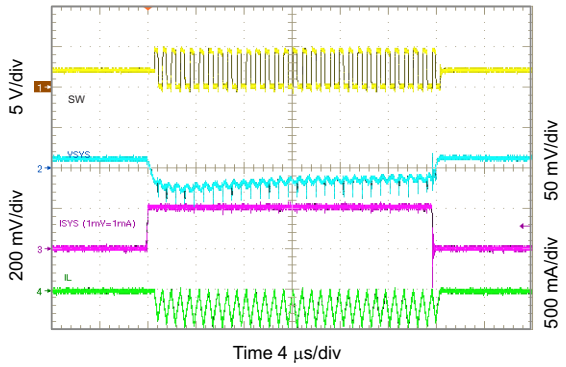
図 72. 1.2 V_{SYS} Load Transient, 0 to 200 mA



V_{SYS} = 1.8 V

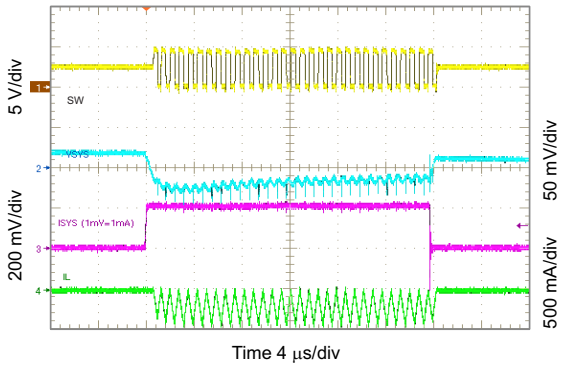
図 73. 1.8 V_{SYS} Load Transient, 0 to 200 mA

Typical Application (continued)



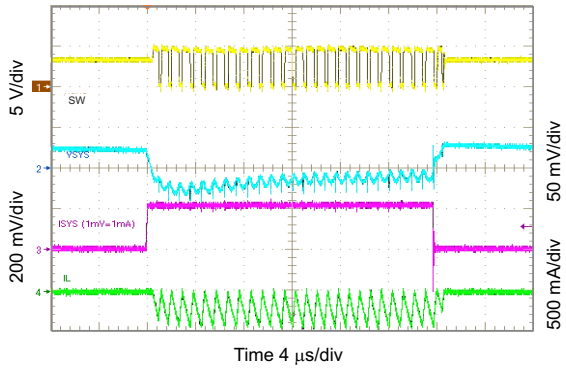
V_{SYS} = 2.1 V

図 74. 2.1 V_{SYS} Load Transient, 0 to 200 mA



V_{SYS} = 2.5 V

図 75. 2.5 V_{SYS} Load Transient, 0 to 200 mA



V_{SYS} = 3.3 V

図 76. 3.3 V_{SYS} Load Transient, 0 to 200 mA

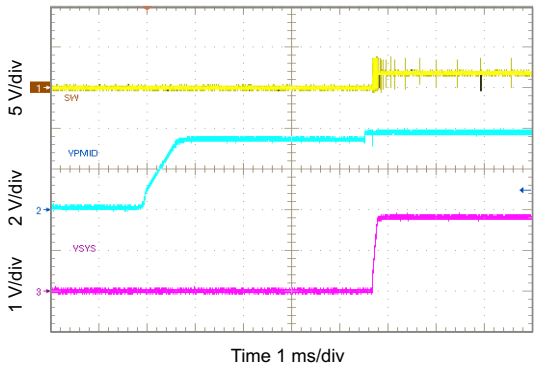


図 77. Startup Showing SS on SYS in PWM Mode

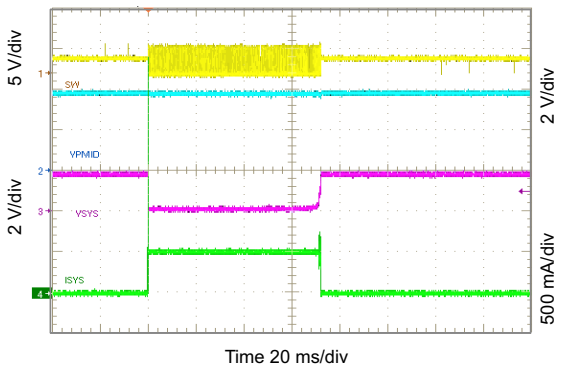


図 78. Short Circuit and Recovery for SYS

Typical Application (continued)

10.2.3.3 Load Switch and LDO Curves

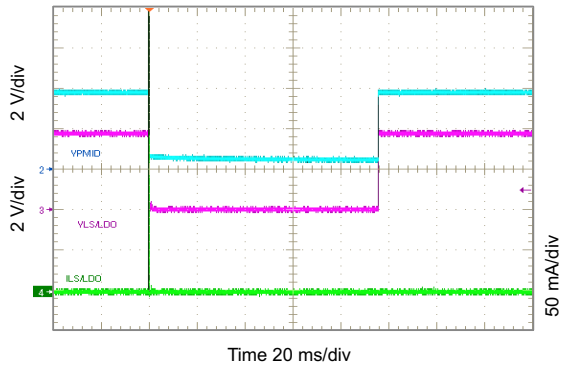


図 79. Short Circuit and Recovery for LS

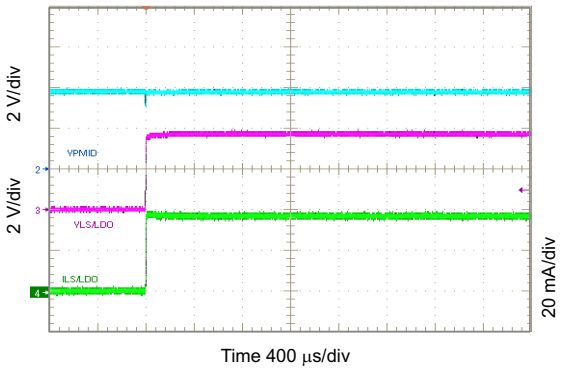
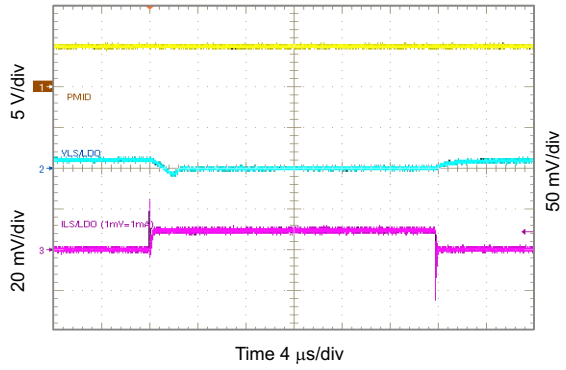
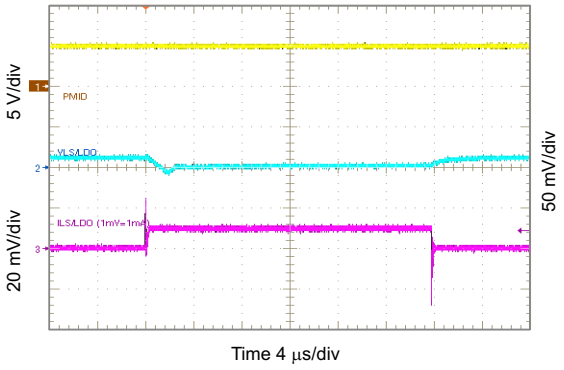


図 80. Startup Showing SS on LS/LDO Output



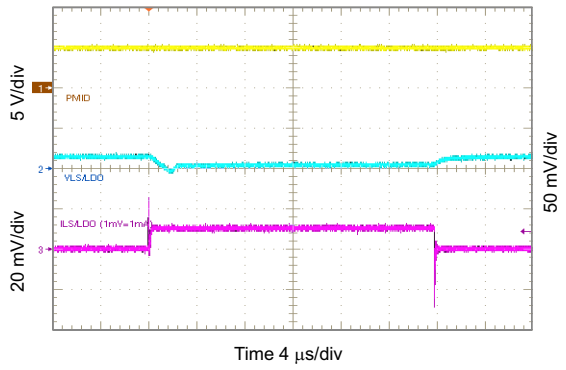
V_{SLSDO} = 0.8 V

図 81. 0.8 V_{LSLDO} Load Transient, 0 to 10 mA



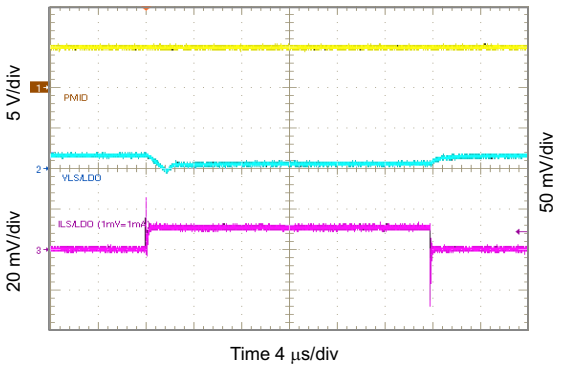
V_{SLSDO} = 1.2 V

図 82. 1.2 V_{LSLDO} Load Transient, 0 to 10 mA



V_{SLSDO} = 1.8 V

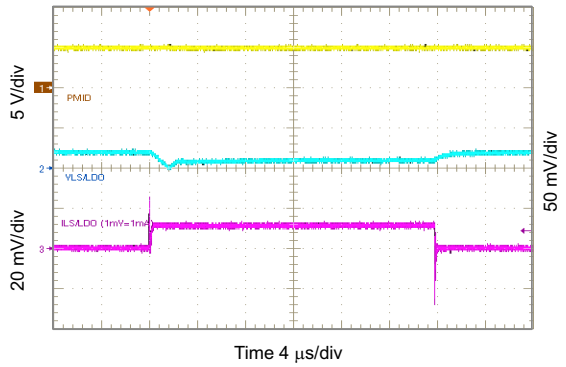
図 83. 1.8 V_{LSLDO} Load Transient, 0 to 10 mA



V_{SLSDO} = 2.5 V

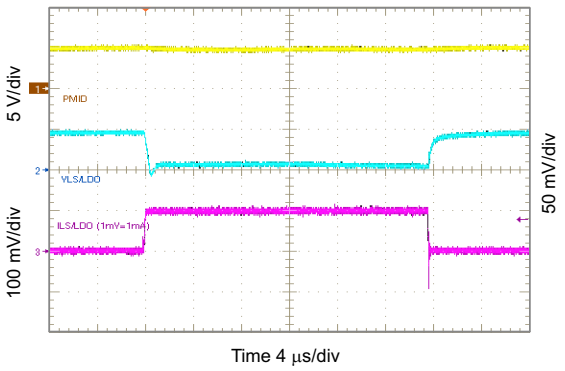
図 84. 2.5 V_{LSLDO} Load Transient, 0 to 10 mA

Typical Application (continued)



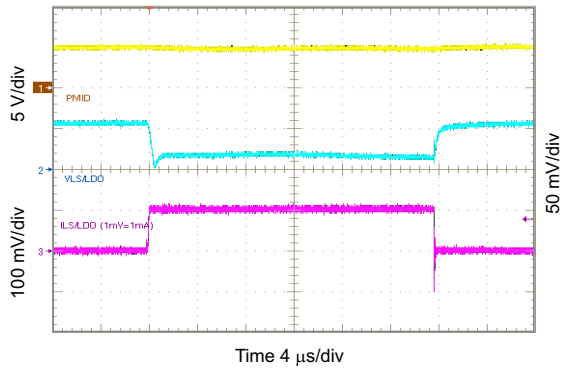
V_{SLSDO} = 3.3 V

図 85. 3.3 V_{LSLDO} Load Transient, 0 to 10 mA



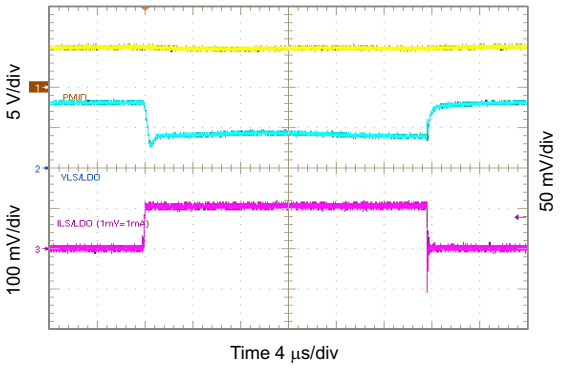
V_{SLSDO} = 0.8 V

図 86. 0.8 V_{LSLDO} Load Transient, 0 to 100 mA



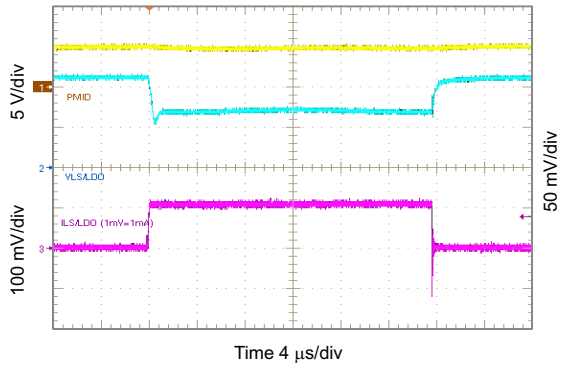
V_{SLSDO} = 1.2 V

図 87. 1.2 V_{LSLDO} Load Transient, 0 to 100 mA



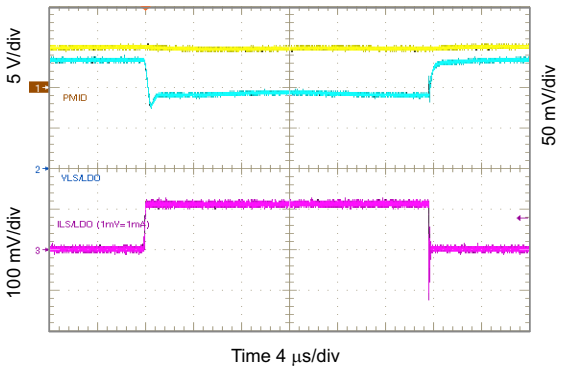
V_{SLSDO} = 1.8 V

図 88. 1.8 V_{LSLDO} Load Transient, 0 to 100 mA



V_{SLSDO} = 2.5 V

図 89. 2.5 V_{LSLDO} Load Transient, 0 to 100 mA



V_{SLSDO} = 3.3 V

図 90. 3.3 V_{LSLDO} Load Transient, 0 to 100 mA

Typical Application (continued)

10.2.3.4 LS/LDO Output Curves

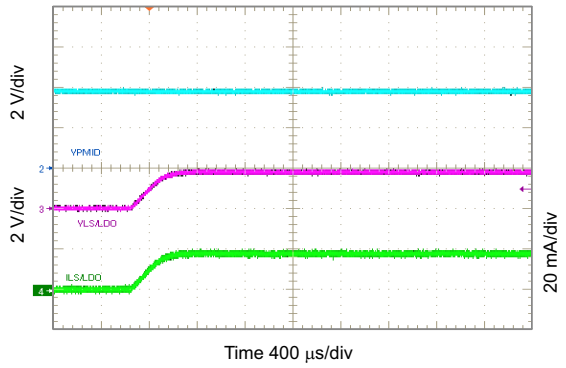


図 91. Startup Showing SS on LS/LDO in LDO Mode

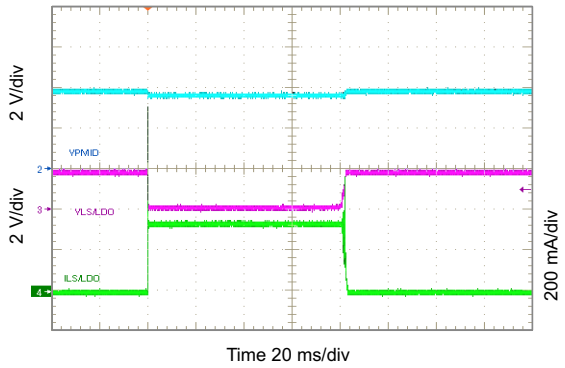


図 92. Short Circuit and Recovery for LDO

Typical Application (continued)

10.2.3.5 Timing Waveforms Curves

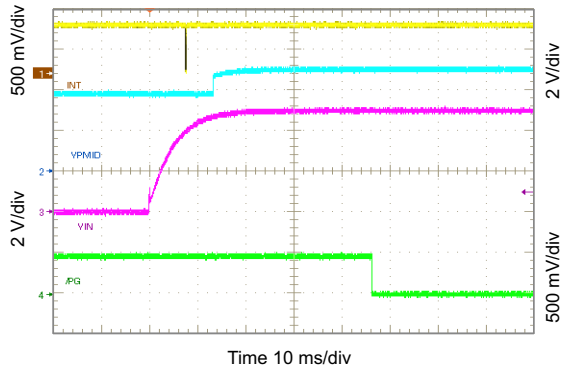


図 93. Show $\overline{PG}$ and $\overline{INT}$ Timing (VI_N Insertion)

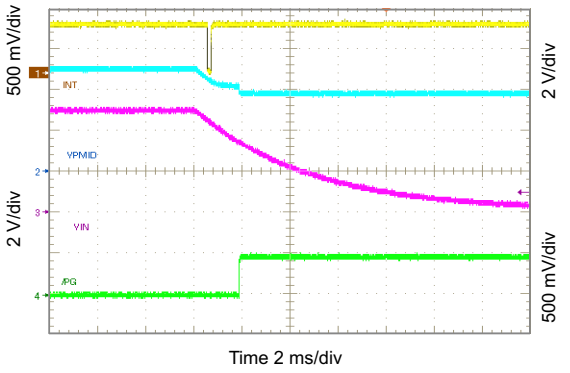


図 94. Show $\overline{PG}$ and $\overline{INT}$ Timing (V_{IN} Removal)

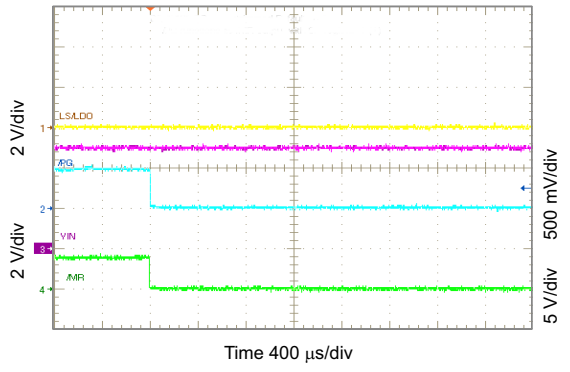


図 95. $\overline{PG}$ Functions as Shifted $\overline{MR}$ Output

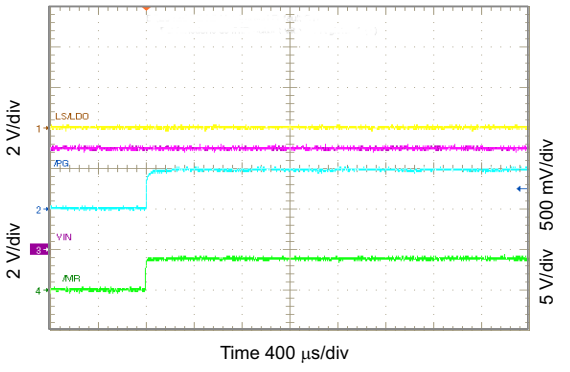


図 96. $\overline{PG}$ Functions as Shifted $\overline{MR}$ Output

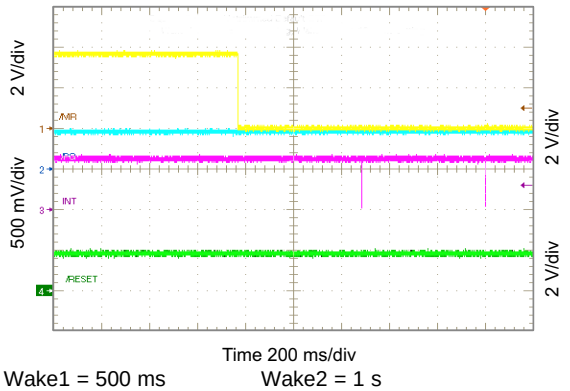


図 97. Show $\overline{MR}$ Timing

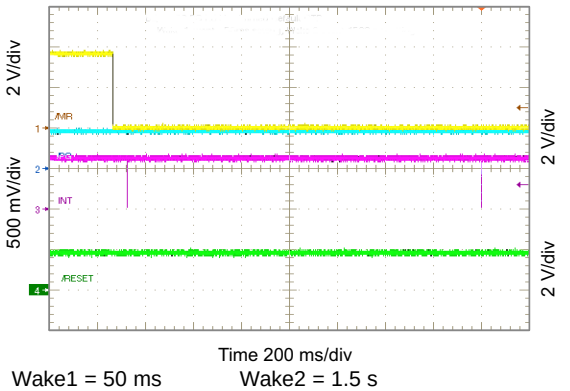
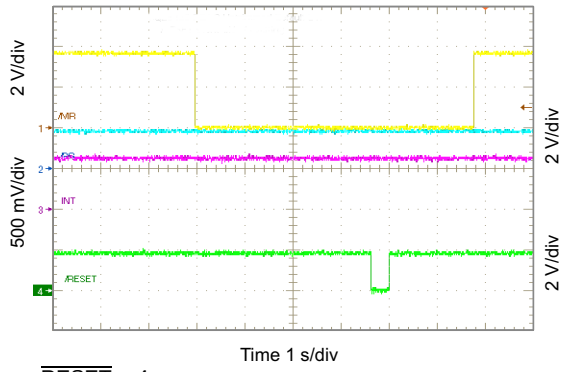


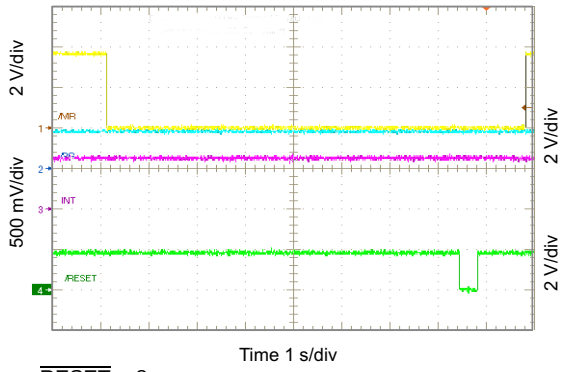
図 98. Show $\overline{MR}$ Timing

Typical Application (continued)



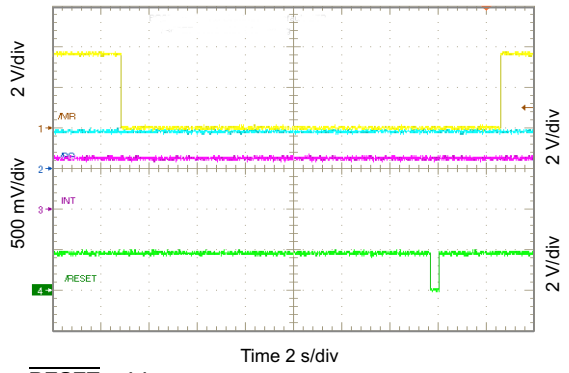
RESET = 4 s

図 99. RESET Timing



RESET = 8 s

図 100. RESET Timing



RESET = 14 s

図 101. RESET Timing

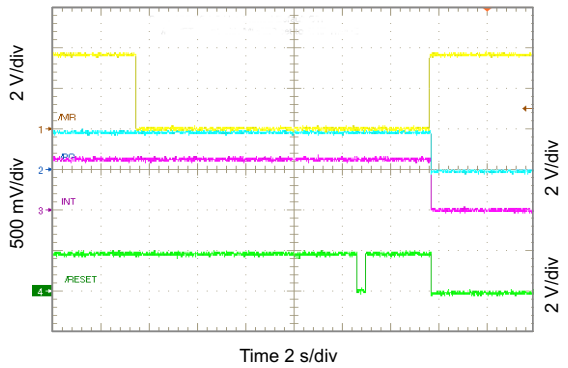


図 102. RESET Timing and Enter Ship Mode

11 Power Supply Recommendations

It is recommended to use a power supply that is capable of delivering 5 V at the input current limit set by the BQ25120.

12 Layout

12.1 Layout Guidelines

- Keep the core components of the system close to each other and the device.
- Keep the PMID, IN, and SYS caps as close to their respective pins as possible. Place the bypass caps for PMID, SYS, and LSLDO close to the pins.
- Place the GNDs of the PMID and IN caps close to each other.
- Don't route so the power planes are interrupted.

12.2 Layout Example

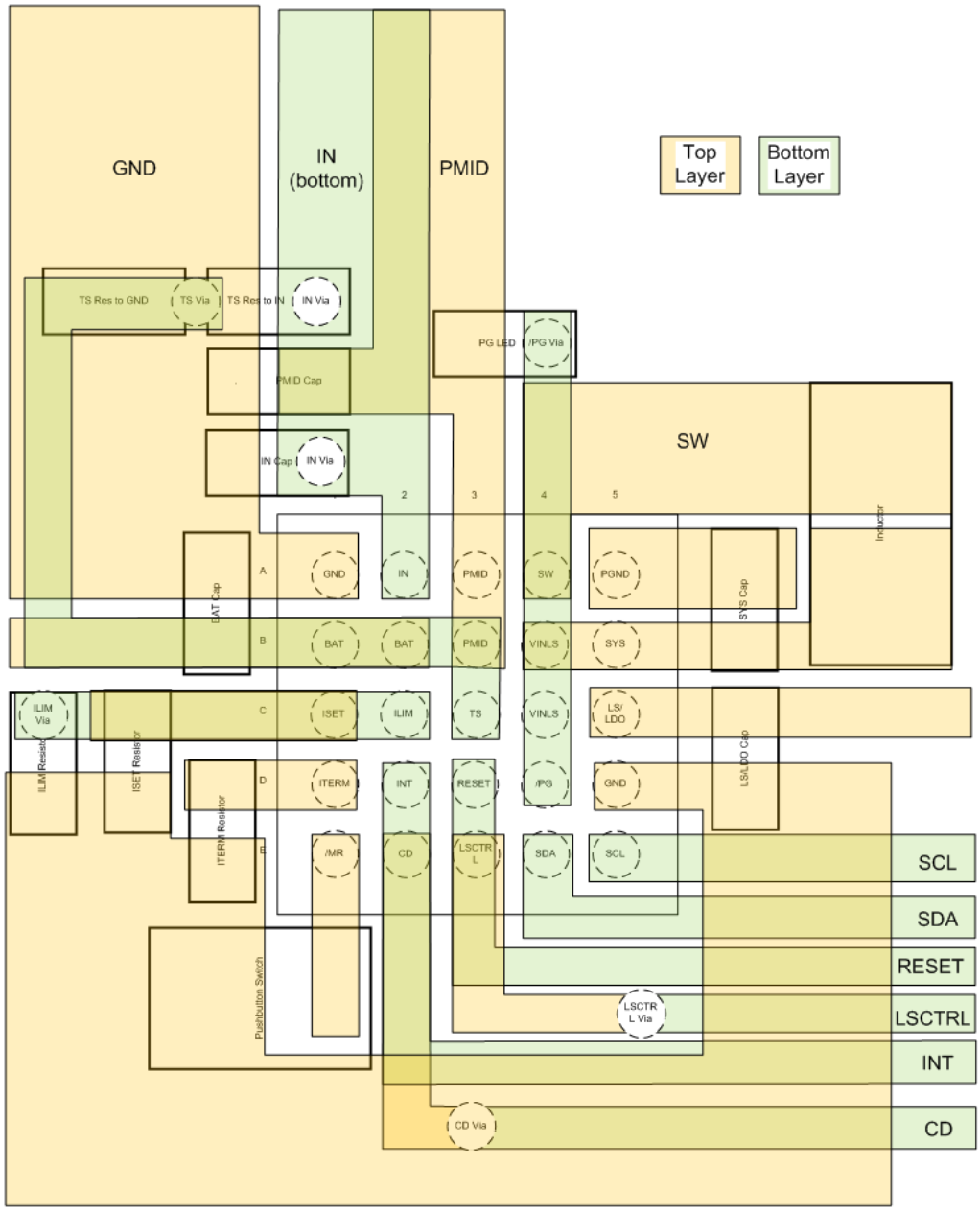


図 103. bq25120 Layout

13 デバイスおよびドキュメントのサポート

13.1 デバイス・サポート

13.1.1 デベロッパー・ネットワークの製品に関する免責事項

デベロッパー・ネットワークの製品またはサービスに関するTIの出版物は、単独またはTIの製品、サービスと一緒に提供される場合に関係なく、デベロッパー・ネットワークの製品またはサービスの適合性に関する是認、デベロッパー・ネットワークの製品またはサービスの是認の表明を意味するものではありません。

13.2 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 25. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
BQ25120	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
BQ25121	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

13.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

13.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™オンライン・コミュニティ ***TIのE2E (Engineer-to-Engineer) コミュニティ。エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。***

設計サポート ***TIの設計サポート*** **役に立つE2Eフォーラムや、設計サポート・ ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。**

13.5 商標

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.6 静電気放電に関する注意事項

これらのデバイスは、限定的なESD（静電破壊）保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ25120YFPR	NRND	DSBGA	YFP	25	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ25120	
BQ25120YFPT	NRND	DSBGA	YFP	25	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ25120	
BQ25121YFPR	NRND	DSBGA	YFP	25	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ25121	
BQ25121YFPT	NRND	DSBGA	YFP	25	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ25121	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

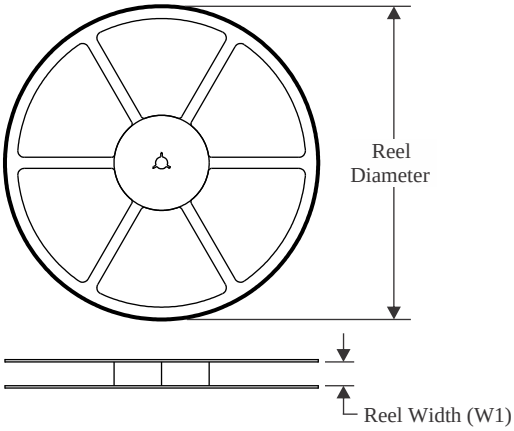
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

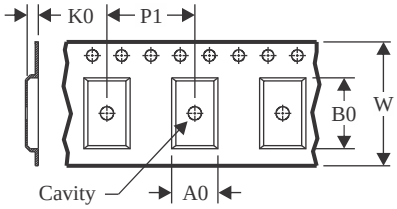
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

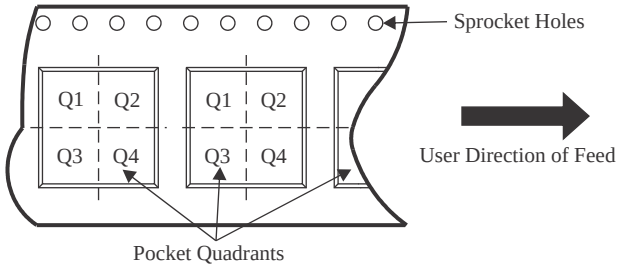


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

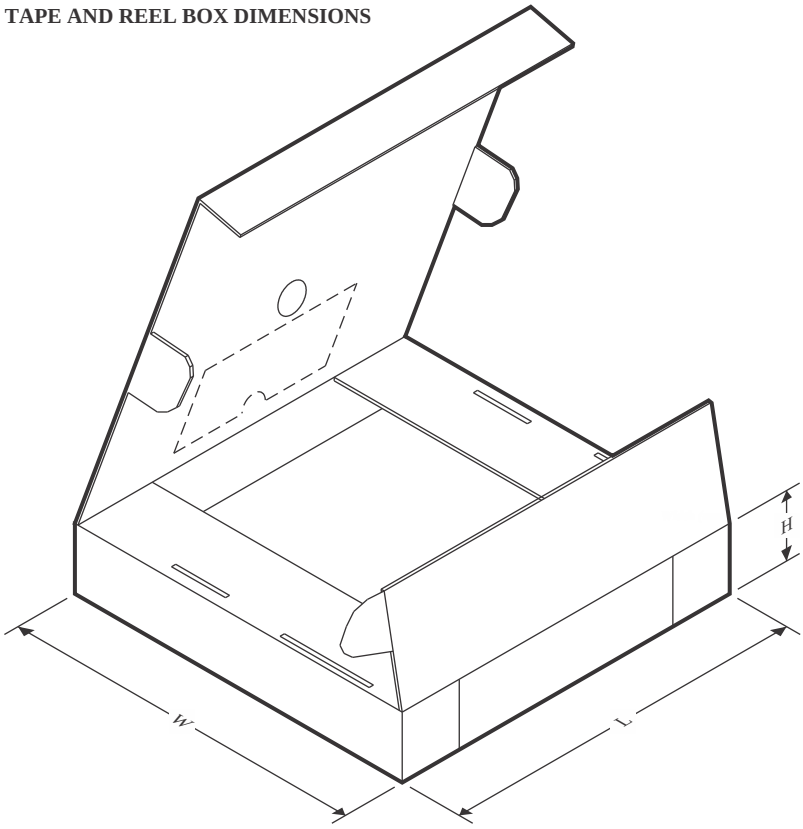
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ25120YFPR	DSBGA	YFP	25	3000	180.0	8.4	2.65	2.65	0.69	4.0	8.0	Q1
BQ25120YFPT	DSBGA	YFP	25	250	180.0	8.4	2.65	2.65	0.69	4.0	8.0	Q1
BQ25121YFPR	DSBGA	YFP	25	3000	180.0	8.4	2.65	2.65	0.69	4.0	8.0	Q1
BQ25121YFPT	DSBGA	YFP	25	250	180.0	8.4	2.65	2.65	0.69	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

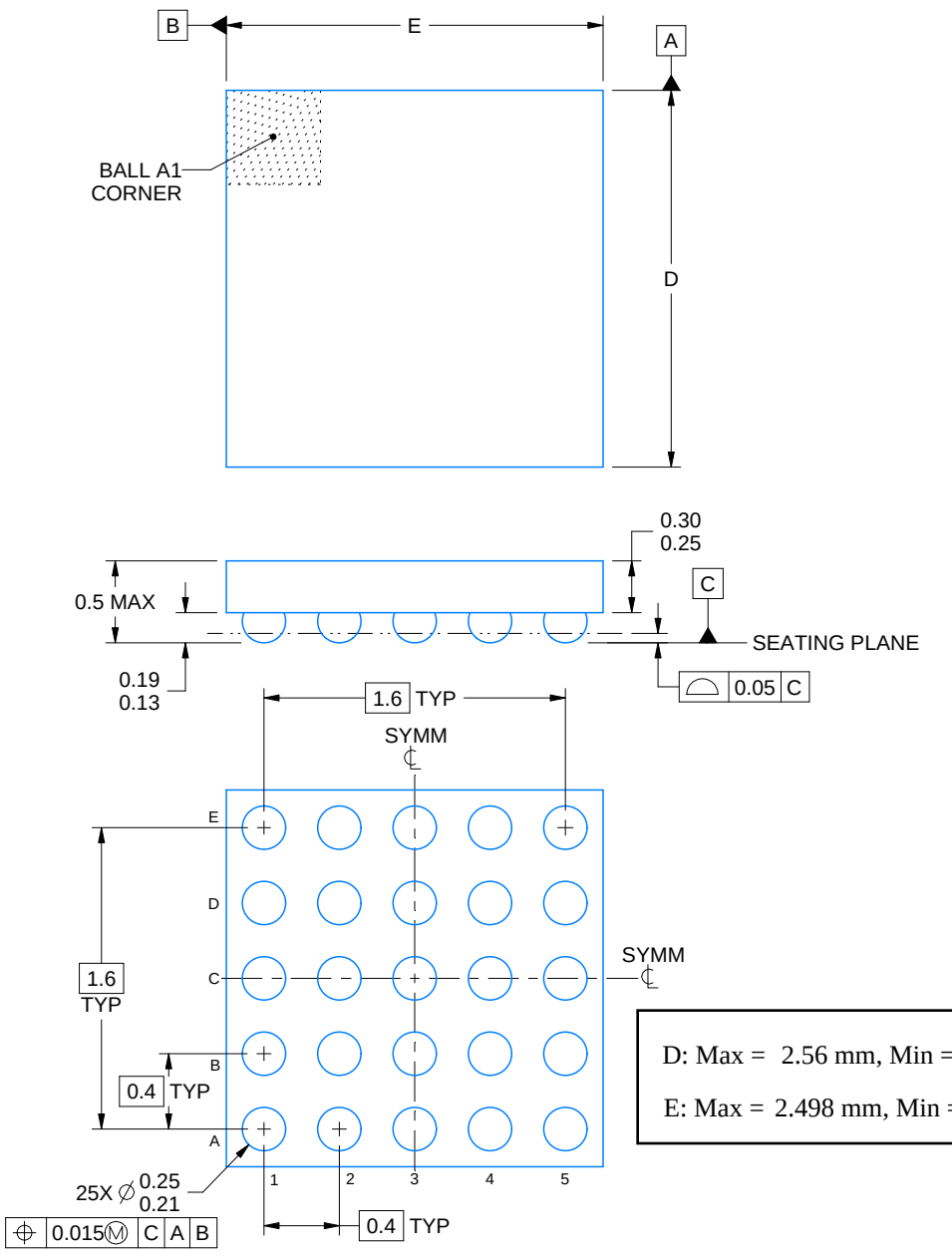
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ25120YFPR	DSBGA	YFP	25	3000	182.0	182.0	20.0
BQ25120YFPT	DSBGA	YFP	25	250	182.0	182.0	20.0
BQ25121YFPR	DSBGA	YFP	25	3000	182.0	182.0	20.0
BQ25121YFPT	DSBGA	YFP	25	250	182.0	182.0	20.0

PACKAGE OUTLINE

YFP0025

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



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NOTES:

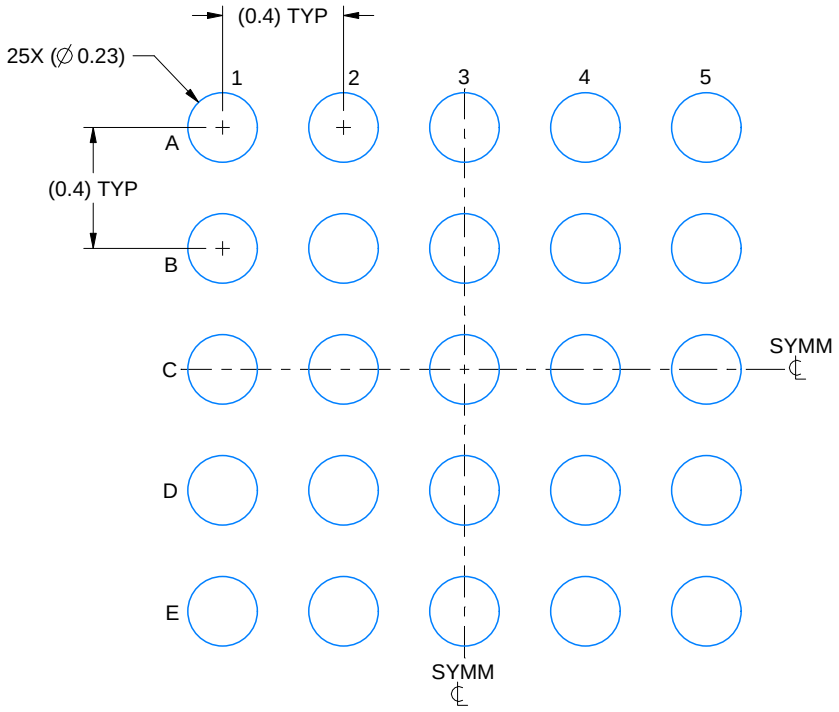
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

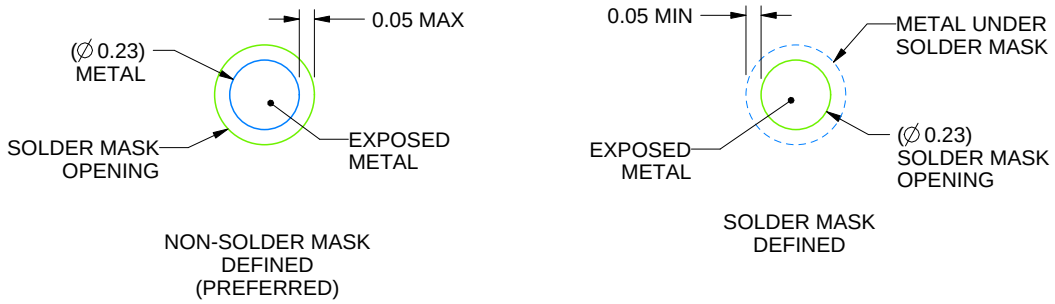
YFP0025

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 40X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

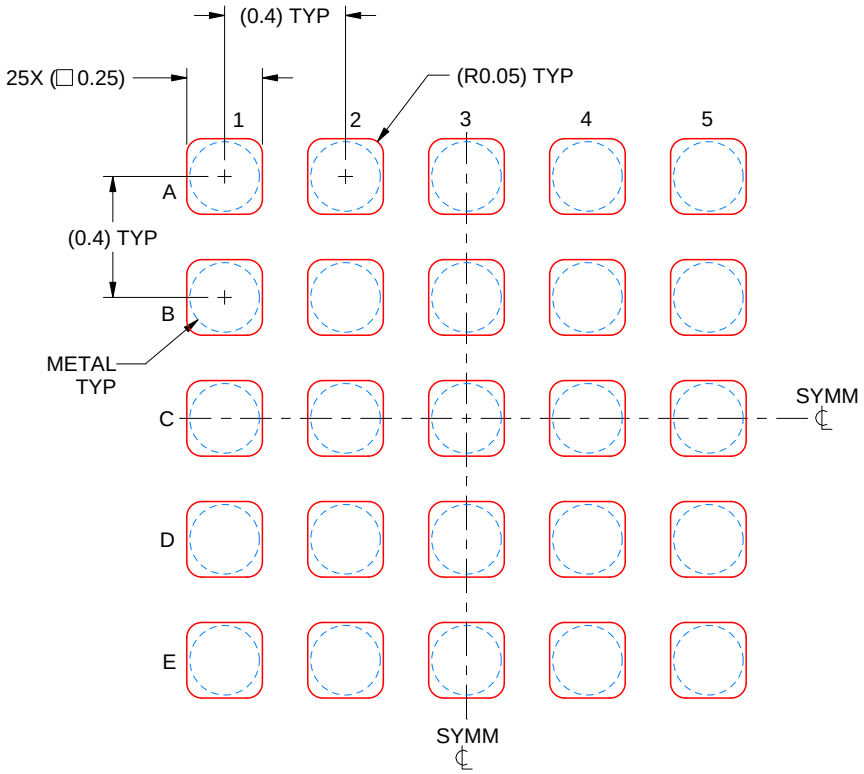
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YFP0025

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 40X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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