BQ25190 昇降圧、DVS 降圧、LDO、ADC、パワー パスを内蔵した I²C 制御の 1 セル、1A リニア バッテリ チャージャ

1 特長

- 統合型の 1A パワー パス リニア バッテリ チャージャ
  - 3.0V～18.0V の動作入力電圧範囲
  - 最大 25V の入力電圧に対応
  - 精度 ±0.5% のバッテリ レギュレーション電圧を 3.5V～4.65V の間で 10mV 刻みに設定可能
  - 5mA～1A に設定可能な高速充電電流
  - 55mΩ BATFET のオン抵抗
  - 最大 2.5A の放電電流で高いシステム負荷に対応
  - 完全にプログラマブルな JEITA プロファイルにより、温度範囲全体にわたって安全に充電
- システム電源およびバッテリ充電用のパワー パス管理
  - バッテリ電圧トラッキングと入力パススルーのオプションに加えて、4.4V～4.9V の範囲でレギュレートされたシステム電圧
  - 設定可能な入力電流制限
  - 動的なパワー パス管理により、弱いアダプタからの充電を最適化
  - システム電源にアダプタとバッテリのどちらかを選択可能
  - 高度なシステム リセット機構
- 超低静止電流モード
  - バッテリ モードで 2μA のバッテリ静止電流
  - 出荷モードで 15nA のバッテリ静止電流
- I²C および GPIO プログラマブル DVS 出力付きの内蔵降圧コンバータ
  - システムからの静止電流 0.36μA
  - 0.4V～1.575V の出力電圧 (12.5mV 刻み)、または 0.4V～3.6V の出力電圧 (25mV/50mV 刻み)
  - 最大 600mA の出力電流
- I²C プログラム可能な DVS 出力付きの内蔵昇降圧コンバータ
  - システムからの静止電流 0.1μA
  - 1.7V～5.2V の出力電圧 (50mV 刻み)
  - V_{SYS} ≧ 3.0V、V_{BBOUT} = 3.3V で最大 600mA の出力電流
- I²C プログラマブル LDO を内蔵 (LDO1 および LDO2)
  - 静止電流：25nA
  - 0.8V～3.6V の出力電圧 (50mV 刻み)
  - 最大 200mA の出力電流
  - LDO1 は出荷モードで常時オンに維持可能
  - LDO またはバイパス モードを構成可能
  - 専用の入力ピン
- 安全性を実現する統合フォルト保護機能
  - 入力電流制限および過電圧保護
  - バッテリ、内蔵レール過電流保護
  - バッテリ過放電保護
  - サーマル レギュレーションおよびサーマル シャットダウン
- 入力電流、BATFET 電流、入力電圧、バッテリ電圧、バッテリ温度、外部電圧信号を監視するための内蔵 12 ビット ADC

2 アプリケーション

- スマート ウォッチ、その他のウェアラブル デバイス
- 携帯医療機器
- スマート追跡機能
- リテール オートメーションおよびペイメント

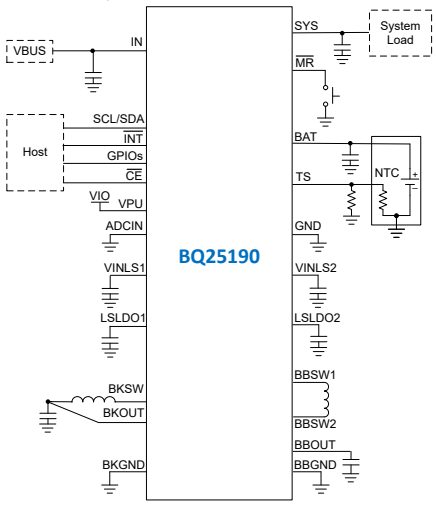
3 概要

BQ25190 は、ウェアラブル デバイス向けに最も一般的に使用される機能として、パワー パス付きのリニア チャージャ、1 つの降圧スイッチング コンバータ (Buck)、1 つの昇降圧スイッチング コンバータ (Buck-boost)、2 つの LDO (LDO1 および LDO2)、タイマ付きマニュアル リセット ($\overline{MR}$)、マルチチャネルのアナログ / デジタル コンバータ (ADC)、4 つの多機能汎用入出力 (GPIO) を搭載した、高度に統合されたバッテリ管理ユニットです。

製品情報

部品番号	パッケージ (1)	本体サイズ (公称)
BQ25190	YBG (WCSP 30)	2.25 mm × 2.75mm

(1) 供給されているすべてのパッケージについては、セクション 13 を参照してください。



概略回路図

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4 概要 (続き)

内蔵チャージャは 5mA～1A の充電電流をサポートしており、高速かつ正確な充電を可能にするとともに、レギュレートされた電圧をシステムに供給します。レギュレートされたシステム電圧 (V_{SYS}) は、下流のシステム負荷の推奨動作条件に基づいて I^2C で設定できます。入力電流制限、充電電流、降圧コンバータの出力電圧、昇降圧コンバータの出力電圧、LDO 出力電圧など他の動作パラメータも、I^2C インターフェイス経由でプログラムできます。

BQ25190 は、動作時とシャットダウン時の静止電流が小さいため、バッテリ駆動時間を延長できます。

5 Pin Configuration and Functions

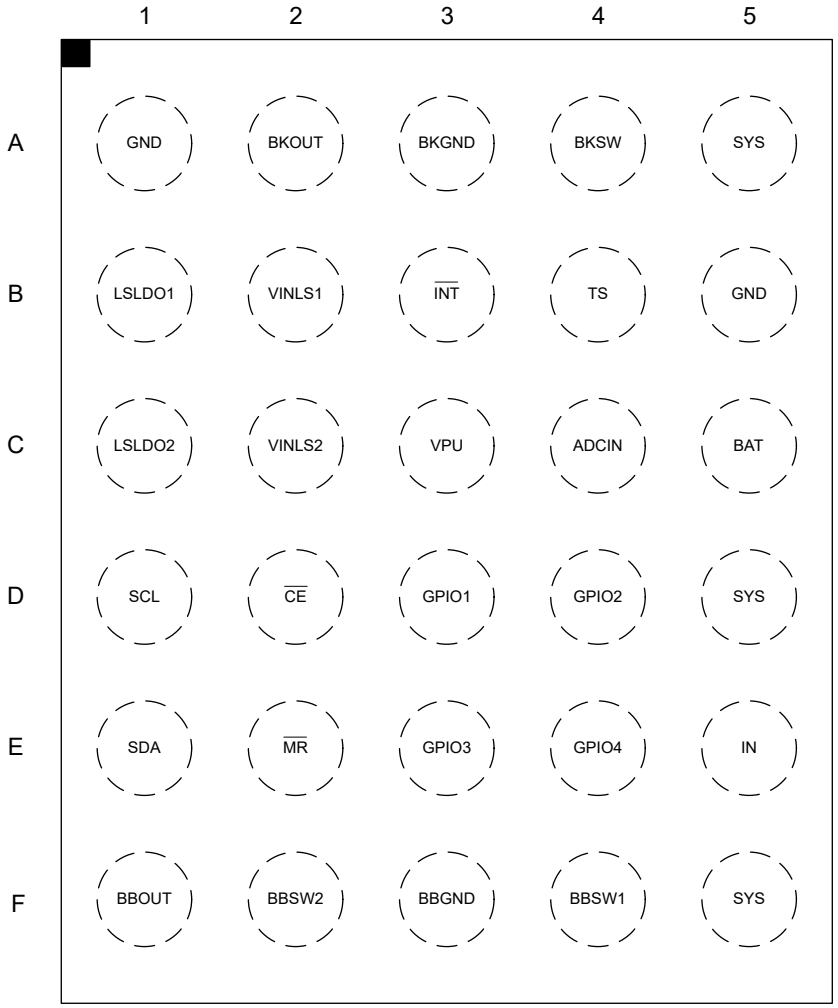


図 5-1. BQ25190 YBG Package 30-Pin WCSP (Top View)

表 5-1. Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
IN	E5	P	DC input power supply. IN is connected to the external DC supply. Bypass IN to GND with at least 1 µF of capacitance using a ceramic capacitor.
SYS	A5, D5, F5	P	Regulated system output. Connect ceramic capatitors respectivelly as suggested in セクション 8.2.2.2 as close to the SYS and GND pins as possible.
BAT	C5	P	Battery Connection. Connect to the positive terminal of the battery. Bypass BAT to GND with at least 1 µF of ceramic capacitance
GND	A1, B5	G	Ground connection. Connect to the ground plane of the circuit
$\overline{CE}$	D2	I	Charge enable. Drive $\overline{CE}$ low or leave floating to enable charging when VIN is valid. Drive $\overline{CE}$ high to disable charge. $\overline{CE}$ has no effect when VIN is not present.
SCL	D1	I	I^2C interface clock. Connect SCL to the logic rail through a 10 kΩ resistor.
SDA	E1	I/O	I^2C interface data. Connect SDA to the logic rail through a 10 kΩ resistor.

表 5-1. Pin Functions (続き)

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
$\overline{INT}$	B3	O	$\overline{INT}$ is an open-drain output that signals fault interrupts. When a fault occurs, a 128 µs active low pulse is sent out as an interrupt for the host. $\overline{INT}$ is enabled/disabled using the MASK_INT bit in the control register. Can be pulled up to 1- 20 kΩ resistor. Typical pull up voltage = 1.8V.
VPU	C3	I	GPIO push-pull mode Pull-up Voltage Pin. Connect VPU to the voltage to be used for the GPIO pins' push-pull mode functions. The pin can be left floating if GPIO pins' push-pull mode functions are not used.
GPIO1	D3	I/O	General-purpose input/output pin 1
GPIO2	D4	I/O	General-purpose input/output pin 2
GPIO3	E3	I/O	General-purpose input/output pin 3
GPIO4	E4	I/O	General-purpose input/output pin 4
BKOUT	A2	I	Output voltage sense pin for the internal feedback divider network of Buck. It also connects the output discharge circuit. Connect this pin to the Buck output capacitor with a short trace.
BBOUT	F1	P	Output voltage sense pin for the internal feedback divider network of Buck-boost. It also connects the output discharge circuit. Connect this pin to the Buck-boost output capacitor with a short trace.
BKSW	A4	P	Buck switch node. Connect the power inductor to this pin.
BBSW1	F4	P	Buck-boost switch node. Connect the power inductor to this pin.
BBSW2	F2	P	Buck-boost switch node. Connect the power inductor to this pin.
BKGND	A3	G	Power ground of Buck. Connect this pin to the ground plane.
BBGND	F3	G	Power ground of Buck-boost. Connect this pin to the ground plane.
$\overline{MR}$	E2	I	Manual reset input. $\overline{MR}$ is a push-button input that must be held low for greater than t_{RESET} to assert the reset output. If $\overline{MR}$ is pressed for a shorter period, there are two programmable timer events, t_{WAKE1} and t_{WAKE2}, that trigger an interrupt to the host. The $\overline{MR}$ input can also be used to bring the device out of Ship mode.
TS	B4	I	Battery pack NTC monitor. Connect TS to a 10-kΩ NTC thermistor in parallel to a 10-kΩ resistor. If TS function is not to be used, connect a 5-kΩ resistor from TS to ground.
LSLDO1	B1	P	Output pin of LDO1. Connect the output capacitor from this pin to the ground plain.
LSLDO2	C1	P	Output pin of LDO2. Connect the output capacitor from this pin to the ground plain.
ADCIN	C4	I	Input channel to the ADC.
VINLS1	B2	P	Input pin of LDO1. Connect the intput capacitor from this pin to the ground plain.
VINLS2	C2	P	Input pin of LDO2. Connect the intput capacitor from this pin to the ground plain.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input Voltage	IN	-0.3	25	V
Buck/Buck-boost Switch Node Voltage (converter not switching)	BKSW, BBSW1, BBSW2	-0.3	V_{SYS} + 0.3 or 5.5(2)	V
Buck/Buck-boost Output Voltage	BKOUT	-0.3	5	V
	BBOUT	-0.3	5.9	V
LDO1/LDO2 Input Voltages	VINLS1, VINLS2	-0.3	6.5	V
LDO1 Output Voltage	LSLDO1	-0.3	V_{VINLS1} + 0.3 or 5.5(2)	V
LDO2 Output Voltage	LSLDO2	-0.3	V_{VINLS2} + 0.3 or 5.5(2)	V
Output Sink Current	GPIO1, GPIO2, GPIO3, GPIO4		20	mA
	/INT		6	mA
Voltage	All other pins	-0.3	5.5	V
T_J	Junction temperature	-40	150	°C
T_{stg}	Storage temperature	-55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Whichever is smaller

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Thermal Information

THERMAL METRIC		BQ25190 YBG (DSBGA) 30 PIN	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (JEDEC(1))	59.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	12.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input Voltage Range	3		18	V
V_{BAT}	Battery Voltage Range			4.65	V
I_{IN}	Input Current Range (IN to SYS)			1.05	A
I_{BAT}	Fast Charging Current			1	A
	RMS Discharge Current (continuously)			1.5	A
	Peak Discharge Current (up to 50ms)			2.5	A
V_{VINLS1}/ V_{VINLS2}	LDO1/LDO2 Input Voltage Range	1.5		6	V
I_{OUT_BUCK}	Buck Output Current			600	mA
I_{OUT_BUBO}	Buck-boost Output Current (V_{SYS} ≥ 3.0V, V_{BBOUT} = 3.3V)			600	mA
I_{OUT_LDO1}/ I_{OUT_LDO2}	LDO1/LDO2 Output Current			200	mA
T_A	Operating Ambient Temperature Range	-40		85	°C
T_J	Operating Junction Temperature Range	-40		125	°C

6.5 Electrical Characteristics

V_{IN} = 5V, V_{BAT} = 3.6V, V_{BBOUT} = 2.5V, V_{VINLS1}/V_{VINLS2} = V_{LSLDO1}/V_{LSLDO2} + 0.5V or 2V (whichever is greater), I_{LSLDO1}/ I_{LSLDO2} = 1mA, -40°C < T_J < 125°C and T_J = 30°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CURRENTS						
I_{Q_BAT}	Battery quiescent current in battery mode, ADC disabled	V_{IN} = 0V, V_{BAT} = 3.6V, Buck disabled, Buck-boost disabled, LDO1 disabled, LDO2 disabled, ADC disabled, watchdog disabled, T_J =30°C		2	2.5	µA
		V_{IN} = 0V, V_{BAT} = 3.6V, Buck disabled, Buck-boost disabled, LDO1 disabled, LDO2 disabled, ADC disabled, watchdog disabled, 0°C<T_J<85°C		2	4	µA
$I_{Q\_BAT\_ADC}$	Battery quiescent current in battery mode, ADC enabled	V_{IN} = 0V, V_{BAT} = 3.6V, Buck disabled, Buck-boost disabled, LDO1 disabled, LDO2 disabled, ADC enabled, watchdog enabled, 0°C<T_J<85°C		350		µA
$I_{Q\_BAT\_SHIP}$	Battery quiescent current in ship mode	V_{IN} = 0V, always-on LDO1 disabled, V_{BAT} = 3.6V, 0°C<T_J<85°C		15	100	nA
I_{Q_IN}	Input supply quiescent current	V_{IN} = 5V, V_{BAT} = 3.6V, Buck disabled, Buck-boost disabled, LDO1 disabled, LDO2 disabled, charge disabled, ADC disabled, SYSREG = 4.5V, TS_FAULT_VIN_EN = 0		0.68	1	mA
		V_{IN} = 5V, V_{BAT} = 3.6V, Buck disabled, Buck-boost disabled, LDO1 disabled, LDO2 disabled, charge disabled, ADC disabled, SYS in pass-through mode, TS_FAULT_VIN_EN = 0		0.45	0.85	mA
I_{SLEEP_IN}	Sleep mode input current	V_{IN} = 3.6V, V_{BAT} = 3.7V, Buck disabled, Buck-boost disabled, LDO1 disabled, LDO2 disabled, ADC disabled		25		µA
I_{SYS_SD}	SYS shutdown current	Buck disabled, Buck-boost disabled, LDO1 disabled, LDO2 disabled, BATFET OFF, input FETs OFF, V_{SYS} = 3.6V, -40°C< T_J<85°C		90	800	nA

6.5 Electrical Characteristics (続き)

V_{IN} = 5V, V_{BAT} = 3.6V, V_{BBOUT} = 2.5V, V_{VINLS1}/V_{VINLS2} = V_{LSLDO1}/V_{LSLDO2} + 0.5V or 2V (whichever is greater), I_{LSLDO1}/I_{LSLDO2} = 1mA, -40°C < T_J < 125°C and T_J = 30°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER-PATH MANAGEMENT AND INPUT						
V_{IN_OP}	IN operating range		3		18	V
V_{IN_UVLOZ}	Exit IN undervoltage lock-out	IN rising			3	V
V_{IN_UVLO}	Enter IN undervoltage lock-out	IN falling			2.7	V
V_{IN_PORZ}	IN voltage threshold to enter ship mode	IN falling	1.09	1.3	1.66	V
V_{SLEEPZ_HYST}	Exit Sleep mode threshold	IN rising, V_{IN} – V_{BAT}, V_{BAT}=4V	175	225	295	mV
V_{SLEEP_HYST}	Enter Sleep mode threshold	IN falling, V_{IN} – V_{BAT}, V_{BAT}=4V	60	90	125	mV
V_{IN_OVP}	IN overvoltage rising threshold	IN rising, VIN_OVP = 0	5.5	5.7	5.9	V
$V_{IN\_OV\_HYST}$	IN overvoltage hysteresis	IN falling, VIN_OVP = 0		125		mV
V_{IN_OVP}	IN overvoltage rising threshold	IN rising, VIN_OVP = 1	18.2	18.5	18.8	V
V_{IN_OVPZ}	IN overvoltage falling threshold	IN falling, VIN_OVP = 1	17.7	18.0	18.3	V
I_{BAT_OCP}	BAT_OCP(Reverse OCP only)	V_{BAT}=3.6V, IBAT_OCP=b00		0.5		A
		V_{BAT}=3.6V, IBAT_OCP=b01		1		A
		V_{BAT}=3.6V, IBAT_OCP=b10		1.5		A
		V_{BAT}=3.6V, IBAT_OCP=b11		3.25		A
V_{BSUP1}	Enter supplement mode threshold	V_{BAT} =3.6V, V_{BAT}>$V_{BATDEPL}$, V_{SYS}<V_{BAT} – V_{BSUP1}		40		mV
V_{BSUP2}	Exit supplement mode threshold	V_{BAT} =3.6V, V_{BAT}>$V_{BATDEPL}$, V_{SYS}>V_{BAT} – V_{BSUP2}		20		mV
I_{LIM}	Input Current Limit	V_{IN}=5V, I_{LIM}=90mA	80	90	98	mA
		V_{IN}=5V, I_{LIM}=475mA	450	475	498	mA
		V_{IN}=5V, I_{LIM}=1050mA	1005	1050	1100	mA
V_{INDPM}	Input voltage threshold when input current is reduced	VINDPM=b00		4.2		V
		VINDPM=b01		4.5		V
		VINDPM=b10		4.7		V
V_{DPPM}	SYS voltage threshold when charge current is reduced	V_{BAT}=3.6V, V_{SYS}=V_{DPPM}+V_{BAT} before charge current is reduced.		0.1		V
$V_{SYS\_REG\_ACCURACY}$	DC SYS regulation accuracy	VIN = 5V, VBAT = 3.6V, I_{SYS} = 100mA, SYS regulation target = 4.5V	–2		2	%
V_{MINSYS}	Minimum SYS voltage when in battery tracking mode	V_{BAT}<3.6V		3.8		V
V_{SYS_TRACK}	Voltage regulation threshold for SYS when VBAT >3.6V	V_{BAT}=4V, V_{SYS}=V_{BAT}+V_{SYS_TRACK}		225		mV
R_{SYS_PD}	SYS pull down resistance	V_{SYS} = 3.6V		20		Ω
V_{SYS_SHORT}	Falling voltage threshold for triggering SYS_SHORT protection			840		mV
V_{SYS_SHORTZ}	Rising voltage threshold for recovering from SYS_SHORT protection			1.08		V
V_{SEQ_UVLOZ}	Exit sequence undervoltage lock-out	SYS rising, when power sequence is used	1.8	1.95	2.1	V
V_{SEQ_UVLO}	Enter sequence undervoltage lock-out	SYS falling, when power sequence is used	1.7	1.85	2	V

6.5 Electrical Characteristics (続き)

V_{IN} = 5V, V_{BAT} = 3.6V, V_{BBOUT} = 2.5V, V_{VINLS1}/V_{VINLS2} = V_{LSLDO1}/V_{LSLDO2} + 0.5V or 2V (whichever is greater), I_{LSLDO1}/I_{LSLDO2} = 1mA, -40°C < T_J < 125°C and T_J = 30°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BATTERY CHARGER						
R_{ON_BAT}	BATFET on-resistance	V_{BAT} = 4.5V, I_{BAT} = 500mA		55	90	mΩ
R_{ON_IN}	Input FET on-resistance	V_{IN} = 5V, I_{IN} = 1A		270	470	mΩ
V_{DO}	Dropout voltage (V_{SYS} - V_{BAT})	V_{BAT} = 4.2V, ICHG = 500mA			300	mV
V_{REG_RANGE}	Typical BAT charge voltage regulation range	10mV steps, programmabe through I^2C	3.5		4.65	V
V_{REG_ACC}	Charge voltage accuracy		–0.5		0.5	%
I_{CHG_RANGE}	Typical charge current regulation range	V_{OUT} > V_{LOWV}	5		1000	mA
I_{CHG_ACC}	Charge current accuracy	ICHG = 40mA	36	40	44	mA
		ICHG = 90mA	81	90	99	mA
		ICHG = 90 mA, 0°C< T_J < 85°C	85.5	90	94.5	mA
		ICHG = 900mA	810	900	990	mA
I_{PRECHG_ACC}	Precharge current accuracy	ICHG = 90 mA, IPRECHG = 20% ICHG	16.2	18	19.8	mA
I_{TERM_ACC}	Termination current accuracy	ITERM = 30 mA, ITERM = 10% ICHG, T_J = 30°C	2.6	3	3.3	mA
V_{LOWV}	Pre-charge to fast-charge transition threshold	VLOWVSEL = 3.0V, VBAT rising	2.9	3	3.1	V
		VLOWVSEL = 2.8V, VBAT rising	2.7	2.8	2.9	V
V_{LOWV_HYST}	Battery LOWV hysteresis			100		mV
$V_{BATDEPLZ}$	Battery depletion threshold, VBAT rising	BATDEPL = b000, VIN = 0V	3.05	3.15	3.25	V
$V_{BATDEPL}$	Battery depletion threshold, VBAT falling	BATDEPL = b000, VIN = 0V	2.9	3	3.1	V
$V_{BATDEPL\_HYST}$	Battery depletion threshold hysteresis, VBAT rising			150		mV
V_{BUVLOZ}	Battery UVLO, VBAT rising		2.4	2.5	2.6	V
V_{BUVLO}	Battery UVLO, VBAT falling		2.0	2.1	2.2	V
$V_{BAT\_ADC\_LOWVZ}$	Minimum battery voltage for ADC operation in battery mode			2.4		V
V_{RECHG}	Battery recharge threshold below regulation voltage	BAT falling, VRECHG = 0		100		mV
		BAT falling, VRECHG = 1		200		mV
V_{BATSC}	Short on battery threshold for trickle charge, VBAT rising			1.8		V
V_{BATSC_HYST}	Battery short circuit voltage hysteresis			200		mV
I_{BATSC}	Trickle charge current	V_{BAT}<V_{BATSC}, IBATSC = 0		8		mA
		V_{BAT}<V_{BATSC}, IBATSC = 1		1		mA
BUCK						
V_{OUT_BUCK}	Buck output voltage range	BUCK_HI_RANGE = 0	0.4		1.575	V
		BUCK_HI_RANGE = 1	0.4		3.6	V
V_{BUCK_UVLOZ}	Buck exit undervoltage lock-out	V_{SYS} rising		1.75	1.8	V
V_{BUCK_UVLO}	Buck enter undervoltage lock-out	V_{SYS} falling		1.65	1.7	V

6.5 Electrical Characteristics (続き)

V_{IN} = 5V, V_{BAT} = 3.6V, V_{BBOUT} = 2.5V, V_{VINLS1}/V_{VINLS2} = V_{LSLDO1}/V_{LSLDO2} + 0.5V or 2V (whichever is greater), I_{LSLDO1}/I_{LSLDO2} = 1mA, -40°C < T_J < 125°C and T_J = 30°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{Q\_BUCK\_ON}$	SYS current when only Buck is enabled	Non-switching, Buck enabled, I_{LOAD_BUCK} = 0 A, V_{OUT_BUCK} = 0.7V, Buck-boost disabled, LDO1 disabled, LDO2 disabled, BATFET OFF, input FETs OFF, Buck PGOOD function disabled, V_{SYS} = 3.6V, –40℃ ≤ T_J ≤ 85℃		360	3200	nA
		Switching, Buck1 enabled, I_{LOAD_BUCK} = 0 A, V_{OUT_BUCK} = 0.7V, Buck-boost disabled, LDO1 disabled, LDO2 disabled, BATFET OFF, input FETs OFF, Buck PGOOD function disabled, V_{SYS} = 3.6V		435		nA
$V_{OUT\_ACC\_BUCK}$	DC output voltage accuracy	PWM operation, –40℃ ≤ T_J ≤ 125℃	-1.5		+1.5	%
$R_{DSON\_HS\_BUCK}$	High-side MOSFET on-resistance	I_{BKOUT} = 300 mA, V_{SYS} = 3.6V		170		mΩ
$R_{DSON\_LS\_BUCK}$	Low-side MOSFET on-resistance	I_{BKOUT} = 300 mA, V_{SYS} = 3.6V		70		mΩ
I_{HSOC_BUCK}	High-side peak current limit	Peak current limit on HS FET	0.9	1.1	1.3	A
I_{LSOC_BUCK}	Low-side valley current limit	Valley current limit on LS FET	0.8	1.0	1.1	A
R_{PD_BUCK}	Output discharge resistor on BKOUT pin	Buck disabled, I_{OUT_BUCK} = -10mA		7		Ω
V_{BUCK_PGTH}	Buck power good threshold	V_{BKOUT} rising		93% V_{target}		
V_{BUCK_PGTHZ}	Buck power good threshold	V_{BKOUT} falling		90% V_{target}		
BUCK-BOOST						
V_{OUT_BB}	Buck-boost output voltage range		1.7		5.2	V
$I_{Q\_IN\_BB\_ON}$	SYS current when only Buck-boost is enabled	Buck-boost enabled, no load, not switching, "unlimited" current setting, Buck disabled, LDO1 disabled, LDO2 disabled, BATFET OFF, input FETs OFF, Buck-boost PGOOD function disabled, V_{SYS} = 3.6V, -40°C< T_J<85°C		105	2050	nA
V_{BB_UVLOZ}	Buck-boost exit undervoltage lock-out	V_{SYS} rising	1.70	1.75	1.80	V
$V_{BB\_UVLO\_HYST}$	UVLO threshold voltage hysteresis		90	100	110	mV
$V_{OUT\_ACC\_BB}$	Buck-boost output voltage DC accuracy	I_{BBOUT} = 1 mA	-1.5		1.5	%
$R_{DSON\_BBBK\_HS}$	Buck-boost buck bridge high-side MOSFET on resistance	V_{SYS} = 3V, V_{BBOUT} = 5V, test current = 1A		155		mΩ
$R_{DSON\_BBBK\_LS}$	Buck-boost buck bridge low-side MOSFET on resistance	V_{SYS} = 3V, V_{BBOUT} = 3V, test current = 1A		110		mΩ
$R_{DSON\_BBBST\_LS}$	Buck-boost boost bridge low-side MOSFET on resistance	V_{SYS} = 3V, V_{BBOUT} = 3V, test current = 1A		110		mΩ
$R_{DSON\_BBBST\_HS}$	Buck-boost boost bridge high-side MOSFET on resistance	V_{SYS} = 5V, V_{BBOUT} = 3V, test current = 1A		155		mΩ
$I_{OC\_SS\_BB}$	Peak current limit during startup	V_{SYS} = 3.6V, unlimited curent limit setting		0.6		A

6.5 Electrical Characteristics (続き)

V_{IN} = 5V, V_{BAT} = 3.6V, V_{BBOUT} = 2.5V, V_{VINLS1}/V_{VINLS2} = V_{LSLDO1}/V_{LSLDO2} + 0.5V or 2V (whichever is greater), I_{LSLDO1}/I_{LSLDO2} = 1mA, -40°C < T_J < 125°C and T_J = 30°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OC_BB}	Peak current limit	V_{SYS} = 1.8V, V_{BBOUT} = 3.6V, unlimited current limit setting	1.43	1.55	1.7	A
		V_{SYS} = 1.8V, V_{BBOUT} = 3.6V, 100mA current limit setting	0.15	0.29	0.51	A
R_{PD_BB}	Output discharge resistor on BBOUT pin	Buck-boost disabled, I_{OUT_BB} = -10mA		7		Ω
V_{BB_PGTH}	Buck-boost power good threshold	V_{BBOUT} rising		93% V_{target}		
V_{BB_PGTHZ}	Buck-boost power good threshold	V_{BBOUT} falling		90% V_{target}		
LDO1						
V_{IN_LDO1}	LDO1 input voltage range		1.5		6	V
V_{OUT_LDO1}	LDO1 output voltage range in LDO mode		0.8		3.6	V
I_{Q_LDO1}	LDO1 quiescent current	T_J = 30°C, I_{LSLDO1} = 0 mA, LDO1 PGOOD function disabled, LDO1 in LDO mode, V_{VINLS1} = 3.6V		25	46	nA
		–40°C ≤ T_J ≤ 85°C, I_{LSLDO1} = 0 mA, LDO1 PGOOD function disabled, LDO1 in LDO mode, V_{VINLS1} = 3.6V			60	nA
I_{SD_LDO1}	Shutdown current	LDO1 disabled, 1.5V ≤ V_{VINLS1} ≤ 5.0V, T_J = 30°C		3	10	nA
$\Delta V_{OUT\_LDO1}(\Delta V_{IN\_LDO1})$	Line regulation	$V_{LSLDO1\ (nom)}$ + 0.5V ≤ V_{VINLS1} ≤ 6V[1]			5	mV
$V_{OUT\_ACC\_LDO1}$	Output voltage accuracy over temperature	V_{LSLDO1} ≥ 1.5V	-2		2	%
		V_{LSLDO1} < 1.5V	-30		30	mV
$\Delta V_{OUT\_LDO1}(\Delta I_{OUT\_LDO1})$	Load regulation[2]	–40°C ≤ T_J ≤ 85°C, 1 mA ≤ I_{LSLDO1} ≤ 200 mA, V_{VINLS1} = $V_{LSLDO1\ (nom)}$ + 0.5V[1]		20	38	mV
		–40°C ≤ T_J ≤ 125°C, 1 mA ≤ I_{LSDO1} ≤ 200 mA, V_{VINLS1} = $V_{LSLDO1\ (nom)}$ + 0.5V[1]			50	mV
I_{CL_LDO1}	Output current limit	V_{LSLDO1} = 90% × $V_{LSLDO1(nom)}$, V_{LSLDO1} < 2.5V, V_{VINLS1} = $V_{LSLDO1(nom)}$ + $V_{DO\_LDO1(max)}$ + 1V	340	550	850	mA
		V_{LSLDO1} = 90% × $V_{LSLDO1(nom)}$, V_{LSLDO1} ≥ 2.5V, V_{VINLS1} = $V_{LSLDO1(nom)}$ + $V_{DO\_LDO1(max)}$ + 0.5V	340	550	850	mA
I_{SC_LDO1}	Short-circuit current limit	V_{LSLDO1} = 0V		80		mA
V_{DO_LDO1}	Dropout voltage[3]	–40°C ≤ T_J ≤ 125°C, 1.8V ≤ V_{LSLDO1} < 2.5V			450	mV
		–40°C ≤ T_J ≤ 125°C, 3.3V ≤ V_{LSLDO1} ≤ 3.6V			310	mV
V_{LDO1_UVLOZ}	LDO1 exit undervoltage lock-out	V_{VINLS1} rising	1	1.35	1.7	V
V_{LDO1_UVLO}	LDO1 enter undervoltage lock-out	V_{VINLS1} falling	0.85	1.19	1.35	V
R_{PD_LDO1}	Output pulldown resistance	V_{LSLDO1} = 3.3V, LDO1 disabled		60		Ω
V_{LDO1_PGTH}	LDO1 power good threshold	V_{LSLDO1} rising		93% V_{target}		

6.5 Electrical Characteristics (続き)

V_{IN} = 5V, V_{BAT} = 3.6V, V_{BBOUT} = 2.5V, V_{VINLS1}/V_{VINLS2} = V_{LSLDO1}/V_{LSLDO2} + 0.5V or 2V (whichever is greater), I_{LSLDO1}/I_{LSLDO2} = 1mA, -40°C < T_J < 125°C and T_J = 30°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{LDO1_PGTHZ}	LDO1 power good threshold	V_{LSLDO1} falling		90% V_{target}		
LDO2						
V_{IN_LDO2}	LDO2 input voltage range		1.5		6	V
V_{OUT_LDO2}	LDO2 output voltage range		0.8		3.6	V
I_{Q_LDO2}	LDO2 quiescent current	T_J = 30°C, I_{LSLDO2} = 0 mA, LDO2 PGOOD function disabled, LDO2 in LDO mode, V_{VINLS2} = 3.6V		25	46	nA
		–40°C ≤ T_J ≤ 85°C, I_{LSLDO2} = 0 mA, LDO2 PGOOD function disabled, LDO2 in LDO mode, V_{VINLS2} = 3.6V			60	nA
I_{SD_LDO2}	Shutdown current	LDO2 disabled, 1.5V ≤ V_{VINLS2} ≤ 5.0V, T_J = 30°C		3	10	nA
$\Delta V_{OUT\_LDO2}(\Delta V_{IN\_LDO2})$	Line regulation	$V_{LSLDO2(nom)}$ + 0.5V ≤ V_{VINLS2} ≤ 6V(4)			5	mV
$V_{OUT\_ACC\_LDO2}$	Output voltage accuracy over temperature	V_{LSLDO2} ≥ 1.5V	-2		2	%
		V_{LSLDO2} < 1.5V	-30		30	mV
$\Delta V_{OUT\_LDO2}(\Delta I_{OUT\_LDO2})$	Load regulation(5)	–40°C ≤ T_J ≤ 85°C, 1 mA ≤ I_{LSLDO2} ≤ 200 mA, V_{VINLS2} = $V_{LSLDO2(nom)}$ + 0.5V(4)		20	38	mV
		–40°C ≤ T_J ≤ 125°C, 1 mA ≤ I_{LSDO2} ≤ 200 mA, V_{VINLS2} = $V_{LSLDO2(nom)}$ + 0.5V(4)			50	mV
I_{CL_LDO2}	Output current limit	V_{LSLDO2} = 90% × $V_{LSLDO2(nom)}$, V_{LSLDO2} < 2.5V, V_{VINLS2} = $V_{LSLDO2(nom)}$ + $V_{DO\_LDO2(max)}$ + 1V	340	550	850	mA
		V_{LSLDO2} = 90% × $V_{LSLDO2(nom)}$, V_{LSLDO2} ≥ 2.5V, V_{VINLS2} = $V_{LSLDO2(nom)}$ + $V_{DO\_LDO2(max)}$ + 0.5V	340	550	850	mA
I_{SC_LDO2}	Short-circuit current limit	V_{LSLDO2} = 0V		80		mA
V_{DO_LDO2}	Dropout voltage(6)	–40°C ≤ T_J ≤ 125°C, 1.8V ≤ V_{LSLDO2} < 2.5V			450	mV
		–40°C ≤ T_J ≤ 125°C, 3.3V ≤ V_{LSLDO2} ≤ 3.6V			310	mV
V_{LDO2_UVLOZ}	LDO2 exit undervoltage lock-out	V_{VINLS2} rising	1	1.35	1.7	V
V_{LDO2_UVLO}	LDO2 enter undervoltage lock-out	V_{VINLS2} falling	0.85	1.19	1.35	V
R_{PD_LDO2}	Output pulldown resistance	V_{LSLDO2} = 3.3V, LDO2 disabled		60		Ω
V_{LDO2_PGTH}	LDO2 power good threshold	V_{LSLDO2} rising		93% V_{target}		
V_{LDO2_PGTHZ}	LDO2 power good threshold	V_{LSLDO2} falling		90% V_{target}		
TERMPERATURE REGULATION AND TEMPERATURE SHUTDOWN						
T_{REG}	Typical junction temperature regulation	THERM_REG = b00		100		°C
		THERM_REG = b01		80		°C
		THERM_REG = b10		60		°C
T_{SHUT_RISING}	Charger thermal shutdown rising threshold	Temperature rising		150		°C

6.5 Electrical Characteristics (続き)

V_{IN} = 5V, V_{BAT} = 3.6V, V_{BBOUT} = 2.5V, V_{VINLS1}/V_{VINLS2} = V_{LSLDO1}/V_{LSLDO2} + 0.5V or 2V (whichever is greater), I_{LSLDO1}/I_{LSLDO2} = 1mA, -40°C < T_J < 125°C and T_J = 30°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_{SHUT\_FALLING}$	Charger thermal shutdown falling threshold	Temperature falling		135		°C
$T_{SHUT\_RISING\_LDO1}$	LDO1 thermal shutdown rising threshold	Temperature rising		170		°C
$T_{SHUT\_FALLING\_LDO1}$	LDO1 thermal shutdown falling threshold	Temperature falling		145		°C
$T_{SHUT\_RISING\_LDO2}$	LDO2 thermal shutdown rising threshold	Temperature rising		170		°C
$T_{SHUT\_RISING\_BUCK}$	Buck thermal shutdown rising threshold	Temperature rising		160		°C
$T_{SHUT\_RISING\_BB}$	Buck-boost thermal shutdown rising threshold	Temperature rising		150		°C
BATTERY NTC MONITOR						
V_{HOT}	High temperature threshold (43°C)	V_{TS} falling, 0°C < T_J < 85°C	0.272(7)	0.276	0.280(7)	V
V_{COLD}	Cold temperature threshold (0°C)	V_{TS} rising, 0°C < T_J < 85°C	0.576(7)	0.580	0.584(7)	V
V_{NTC_HYST}	Threshold hysteresis			20		mV
V_{TS_OPEN}	TS open threshold	V_{TS} rising, 0°C < T_J < 85°C		0.9		V
I_{TS_BIAS}	TS bias current		76.8	80	83.2	µA
V_{TS_CLAMP}	TS clamp voltage	TS open-circuit (float), V_{IN} = 5V	1.2	1.5	1.8	V
PUSH BUTTON TIMERS						
t_{WAKE1}	WAKE1 timer. Time from /MR falling edge to INT being asserted.	WAKE1_TMR = 0		125		ms
		WAKE1_TMR = 1		500		ms
t_{WAKE2}	WAKE2 timer. Time from /MR falling edge to INT being asserted.	WAKE2_TMR = 0		1		s
		WAKE2_TMR = 1		2		s
t_{LPRESS_WARN}	RESET_WARN timer. Time prior to long press action			1		s
t_{LPRESS}	Long press timer. Time from /MR falling edge to long press action	MR_LPRESS = b00		5		s
		MR_LPRESS = b01		10		s
		MR_LPRESS = b10		15		s
		MR_LPRESS = b11		20		s
$t_{RESTART(AUTOWAKE)}$	RESTART timer. Time from HW Reset to SYS power up	AUTOWAKE = b00		0.5		s
		AUTOWAKE = b01		1		s
		AUTOWAKE = b10		2		s
		AUTOWAKE = b11		4		s
$t_{SHIPWAKE}$	Wake timer to count for ship mode exit			1		s
BATTERY CHARGING TIMERS						
t_{MAXCHG}	Charge safety timer	Programmable range	180		720	min
t_{SFTMR_ACC}	Safety timer accuracy		–10		10	%
t_{PRECHG}	Precharge safety timer			0.25 * t_{MAXCHG}		
ADC MEASUREMENT ACCURACY AND PERFORMANCE						

6.5 Electrical Characteristics (続き)

V_{IN} = 5V, V_{BAT} = 3.6V, V_{BBOUT} = 2.5V, V_{VINLS1}/V_{VINLS2} = V_{LSLDO1}/V_{LSLDO2} + 0.5V or 2V (whichever is greater), I_{LSLDO1}/I_{LSLDO2} = 1mA, -40°C < T_J < 125°C and T_J = 30°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ADC_CONV}	Conversion-time, each measurement	ADC_SAMPLE = b00		24		ms
		ADC_SAMPLE = b01		12		ms
		ADC_SAMPLE = b10		6		ms
		ADC_SAMPLE = b11		6		ms
ADC_RES	Effective resolution	ADC_SAMPLE = b00	11	12		bits
		ADC_SAMPLE = b01	10	11		bits
		ADC_SAMPLE = b10	9	10		bits
		ADC_SAMPLE = b11	9	10		bits
ADC MEASUREMENT RANGE AND LSB						
IIN_ADC	ADC IIN reading	Range	0		1.1	A
		LSB		0.5		mA
VIN_ADC	ADC VIN reading (VIN_OVP=0)	Range	0		6	V
		LSB		1.5		mV
	ADC VIN reading (VIN_OVP=1)	Range	0		20	V
		LSB		5		mV
VBAT_ADC	ADC VBAT reading	Range	0		5	V
		LSB		1.25		mV
VSYS_ADC	ADC VSYS reading	Range	0		5	V
		LSB		1.25		mV
IBAT_ADC	ADC IBAT reading	Range	-3		1	A
		LSB		1		mA
TS_ADC	ADC VTS reading	Range	0		1	V
		LSB		0.25		mV
TDIE_ADC	ADC TDIE reading	Range	–40		125	°C
		LSB		0.5		°C
ADCIN_ADC	ADC ADCIN voltage reading, ADCIN_MODE = 0	Range	0		5	V
		LSB		1.25		mV
	ADC ADCIN voltage reading, ADCIN_MODE = 1	Range	0		1	V
		LSB		0.25		mV
I²C INTERFACE						
$V_{IL\_SDA\_SCL}$	Input low threshold level, SDA and SCL				0.42	V
$V_{IH\_SDA\_SCL}$	Input high threshold level, SDA and SCL		0.78			V
V_{OL_SDA}	Output low threshold level, SDA	5 mA sink current, 1.2V V_{PULLUP}			0.3	V
$I_{LKG\_SDA\_SCL}$	High-level leakage current, SDA and SCL	V_{PULLUP} = 1.8V			1	µA
C_{BUS}	Capacitive load for each bus line				550	pF
$\overline{MR}$ INPUT PIN						
R_{PU_MR}	Internal pull up resistance			140		kΩ
V_{IL_MR}	$\overline{MR}$ input low threshold level				0.3	V
$\overline{INT}$ OUTPUT PIN						
V_{OL_INT}	Output low threshold level	5mA sink current			0.3	V
I_{LKG_INT}	High-level leakage current	V_{PULLUP} = 1.8V			1	µA

6.5 Electrical Characteristics (続き)

V_{IN} = 5V, V_{BAT} = 3.6V, V_{BBOUT} = 2.5V, V_{VINLS1}/V_{VINLS2} = V_{LSLDO1}/V_{LSLDO2} + 0.5V or 2V (whichever is greater), I_{LSLDO1}/I_{LSLDO2} = 1mA, -40°C < T_J < 125°C and T_J = 30°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\overline{CE}$ INPUT PIN						
R_{PD_CE}	Internal pull-down resistance, $\overline{CE}$			5		MΩ
V_{IL_CE}	Input low threshold level, $\overline{CE}$				0.4	V
V_{IH_CE}	Input high threshold level, $\overline{CE}$		0.78			V
$I_{IN\_BIAS\_CE}$	High-level leakage current, $\overline{CE}$	V_{PULLUP} = 1.8V			1	µA
GPIO1/GPIO2/GPIO3/GPIO4						
V_{IL_GPIO}	Input low threshold level, GPIO1/GPIO2/GPIO3/GPIO4				0.4	V
V_{IH_GPIO}	Input high threshold level, GPIO1/GPIO2/GPIO3/GPIO4		0.78			V
V_{OL_GPIO}	Output low threshold level, GPIO1/GPIO2/GPIO3/GPIO4	5 mA sink current			0.3	V
$V_{OH\_GPIO\_PP}$	Output high level in push-pull mode, GPIO1/GPIO2/GPIO3/GPIO4	0.5 mA output current, V_{VPU} =1.8V	0.8×V_{VPU}			V
f_{GPIO4_PWM}	GPIO4 frequency in PWM output mode			1		kHz
I_{LKG_GPIO}	High-level leakage current, GPIO1/GPIO2/GPIO3/GPIO4	GPIO1/GPIO2/GPIO3/GPIO4 in forced open-drain high mode, V_{PULLUP} = 1.8V			1	µA

(1) V_{VINLS1} = 2.0 V for V_{LSLDO1} ≤ 1.5 V
(2) Load Regulation is normalized to the output voltage at I_{LDOLS1} = 1 mA.
(3) Dropout is measured by ramping V_{VINLS1} down until V_{LSLDO1} = V_{LSLDO1} (nom) x 95%, with I_{LSLDO1} = 200 mA
(4) V_{VINLS2} = 2.0 V for V_{LSLDO2} ≤ 1.5 V
(5) Load Regulation is normalized to the output voltage at I_{LDOLS2} = 1 mA.
(6) Dropout is measured by ramping V_{VINLS2} down until V_{LSLDO2} = V_{LSLDO2} (nom) x 95%, with I_{LSLDO2} = 200 mA
(7) Based on Characterization Data

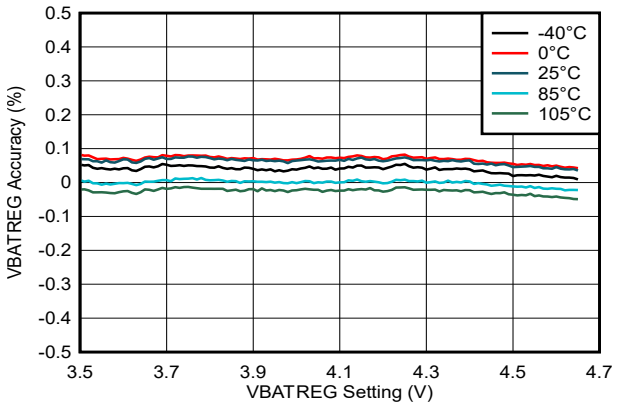
6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
INPUT					
$t_{VIN\_OVPZ\_DGL}$	VIN_OVP deglitch, VIN falling		30		ms
BATTERY CHARGER					
t_{REC_SC}	BAT_OCP retry hiccup time		250		ms
t_{RETRY_SC}	Retry window for BAT_OCP		2		s
t_{TSHUT_DGLZ}	TSHUT recovery deglitch time		100		ms
POWER SEQUENCING					
t_{SEQ_DELAY}	Delay time between power sequence time instances, SEQUENCE_DELAY_TIME = b00		1		ms
	Delay time between power sequence time instances, SEQUENCE_DELAY_TIME = b01		4		ms
	Delay time between power sequence time instances, SEQUENCE_DELAY_TIME = b10		16		ms
	Delay time between power sequence time instances, SEQUENCE_DELAY_TIME = b11		64		ms
$t_{SEQ\_PG\_DELAY}$	Delay time from time instance d to power sequence power good being evaluated		4		ms
I^2C CLOCK					

6.6 Timing Requirements (続き)

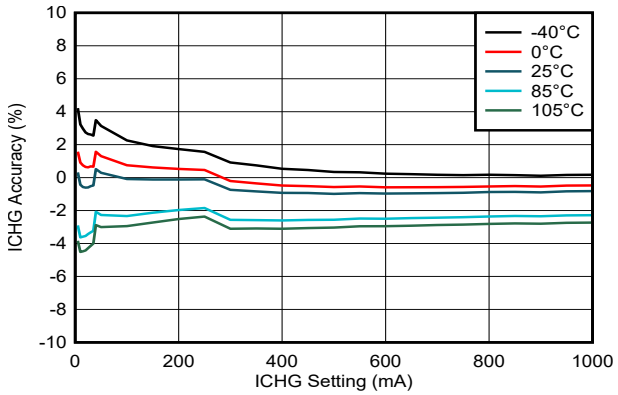
		MIN	NOM	MAX	UNIT
F_{I2C_CLK}	SCL clock frequency			1000	KHz

6.7 Typical Characteristics



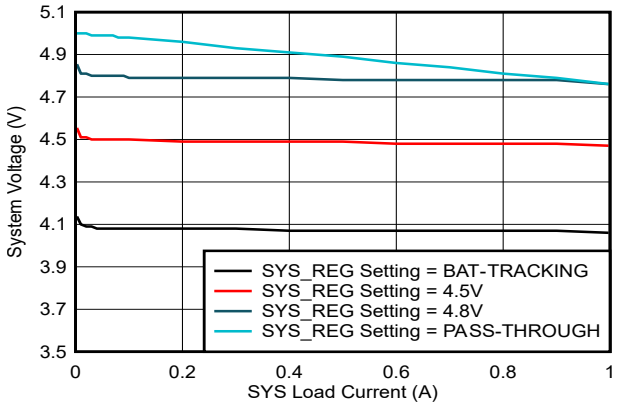
V_{IN} = 5V I_{CHG} = 5mA

図 6-1. Charge Voltage Accuracy vs VBATREG Setting



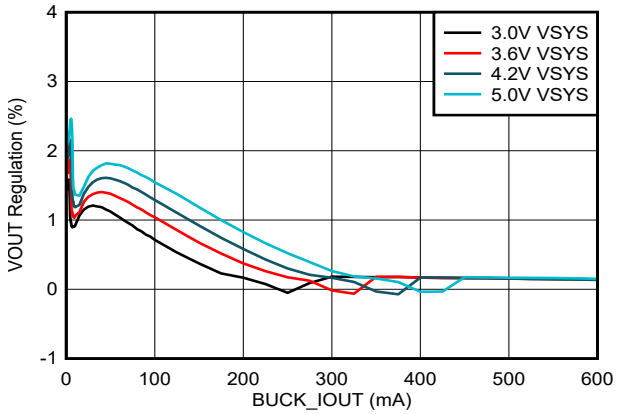
V_{IN} = 5V V_{BAT} = 3.8V

図 6-2. Charge Current Accuracy vs ICHG Setting



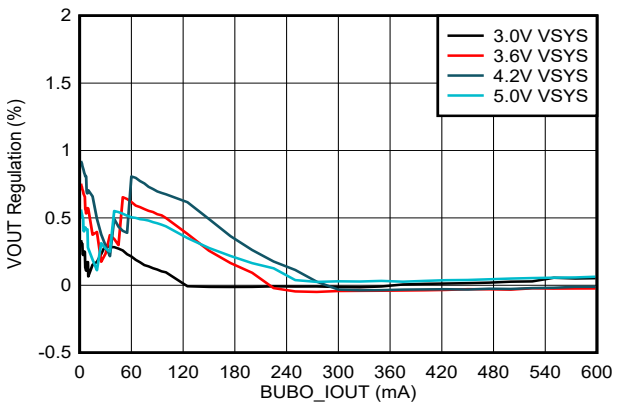
V_{IN} = 5V V_{BAT} = 3.8V T_A = 25°C

図 6-3. System Load Regulation



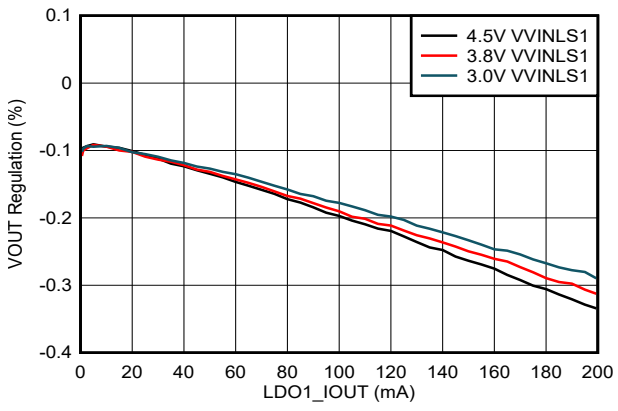
V_{BKOUT} = 1.8V T_A = 25°C

図 6-4. Buck Load Regulation



V_{BBOUT} = 3.3V T_A = 25°C

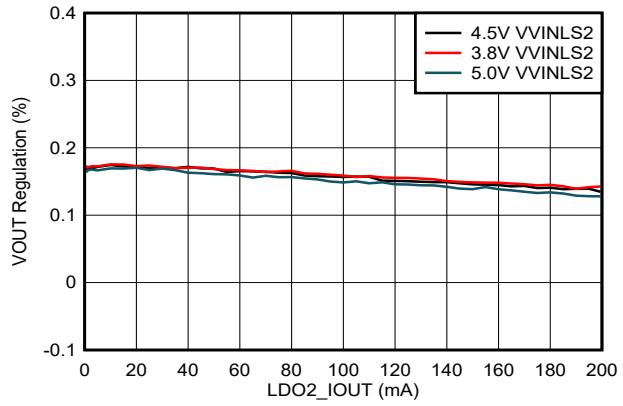
図 6-5. Buck-Boost Load Regulation



V_{LSLDO1} = 1.8V T_A = 25°C

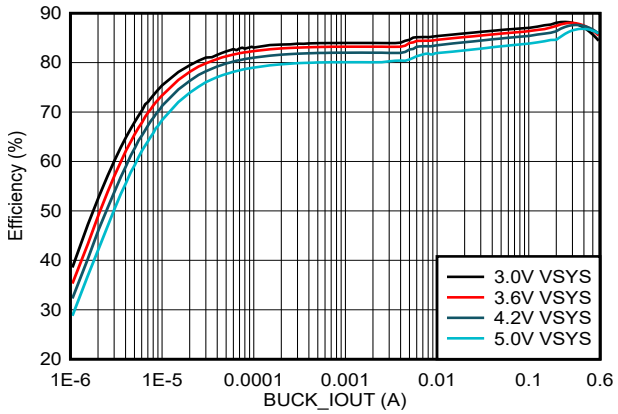
図 6-6. LDO1 Load Regulation

6.7 Typical Characteristics (continued)



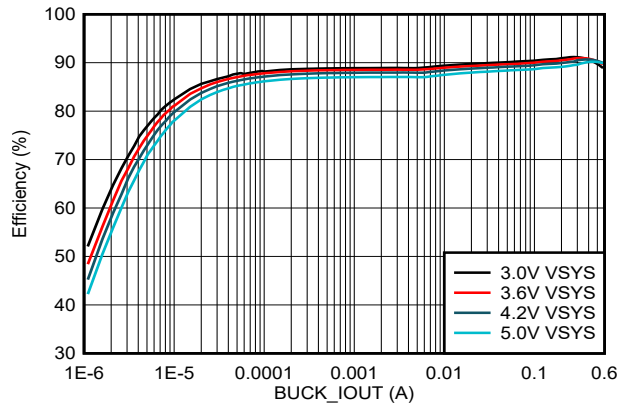
V_{LSLDO2} = 3.3V T_A = 25°C

図 6-7. LDO2 Load Regulation



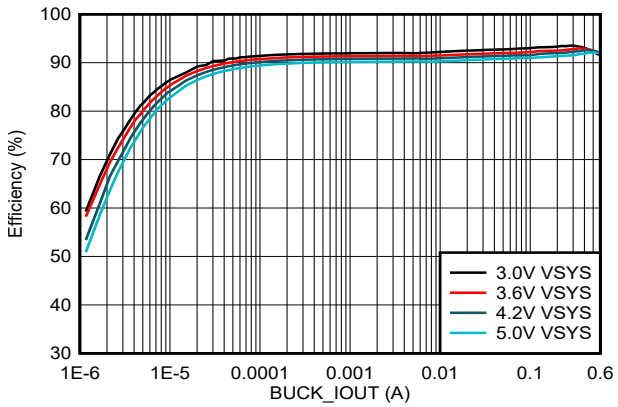
V_{BKOUT} = 0.7V T_A = 25°C

図 6-8. Buck Efficiency



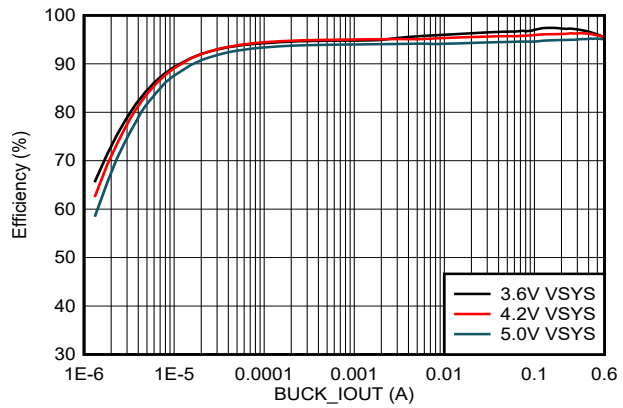
V_{BKOUT} = 1.2V T_A = 25°C

図 6-9. Buck Efficiency



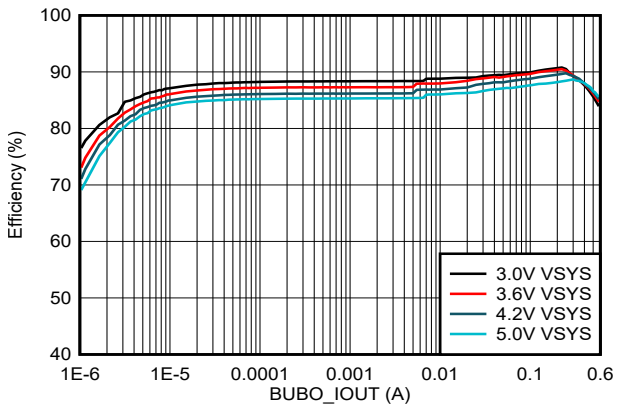
V_{BKOUT} = 1.8V T_A = 25°C

図 6-10. Buck Efficiency



V_{BKOUT} = 3.3V T_A = 25°C

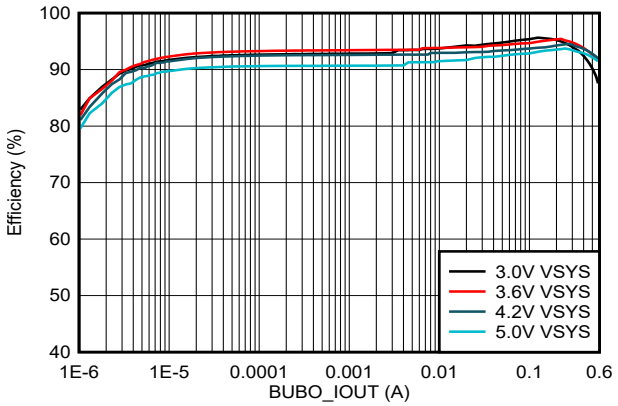
図 6-11. Buck Efficiency



V_{BBOUT} = 1.7V T_A = 25°C

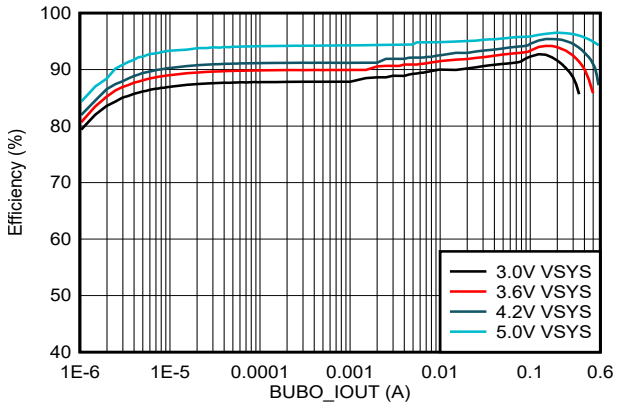
図 6-12. Buck-Boost Efficiency

6.7 Typical Characteristics (continued)



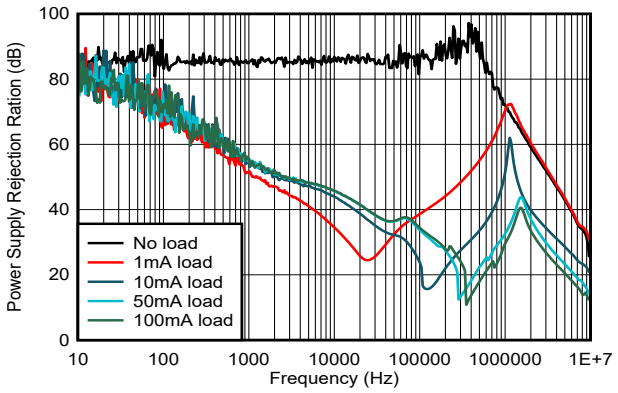
V_{BBOUT} = 3.3V T_A = 25°C

図 6-13. Buck-Boost Efficiency



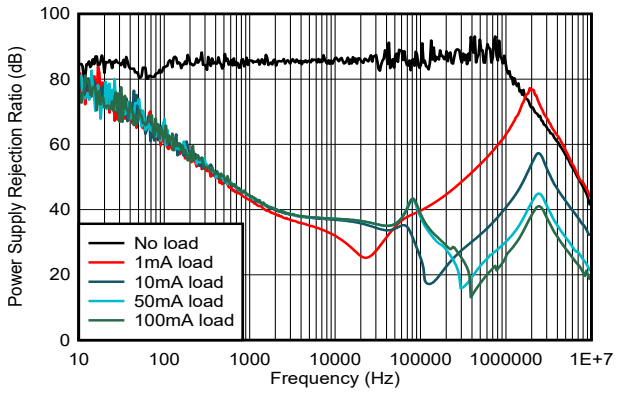
V_{BBOUT} = 5.0V T_A = 25°C

図 6-14. Buck-Boost Efficiency



V_{VINLS1} = 3.6V T_A = 25°C

図 6-15. LDO1 PSRR vs Frequency and Load



V_{VINLS2} = 3.6V T_A = 25°C

図 6-16. LDO2 PSRR vs Frequency and Load

7 Detailed Description

7.1 Overview

The BQ25190 is a battery management unit (BMU) with integrated linear charger, voltage regulators, 12-bit ADC,and multifunction GPIOs. The ultra-low quiescent current of inegarted linear charger and voltage regulators ensures the low power consumption. The flexibility offered by ADC and multifucntion GPIOs enables the easy system monitoring and control.

The device integrates a linear charger that allows the battery to be charged with a programmable charge current. In addition to the charge current, other charging parameters can be programmed through I^2C such as the pre-charge, termination and input current limit currents.

The power path allows the system to be powered from a regulated output, SYS, even when the battery is depleted or charging, by drawing power from IN pin. It also prioritizes the system load in SYS, reducing the charging current, if necessary, in order support the load when input power is limited. If the input supply is removed and the battery voltage level is above V_{BUVLO}, SYS will automatically and seamlessly switch to battery power.

There are two major subsystems in the charger and power path system, the BATSYS and ILIMSYS. The BATSYS consists of the Battery FET (BATFET) and analog and digital control circuitry that control the BATFET operation. There are several loops that influence the charge current: constant current loop (CC), constant voltage loop (CV), input current limit, DPPM, and VINDPM. During the charging process, all loops are enabled and the one that is dominant takes control. The ILIMSYS block consists of back-to-back blocking FETs to prevent reverse currents from SYS to IN as well as the control circuitry to regulate the input current and prevent excessive current from being drawn from the IN power supply for more reliable operation.

The device supports multiple battery chemistries for single-cell applications, hence the need to support multiple battery regulation voltage (V_{REG}) and charge current (I_{CHG}) options.

The device integrates one high efficiency step-down Buck converter with ultra-low operating quiescent current. It employs DCS-control archeture with low ouput voltage ripple and excellent load transient performance. It supports dynamic voltage scaling (DVS) with its output voltage being adjusted through I^2C or GPIO pins. The input of Buck converters is internally connected to SYS.

In addition to the integreated Buck, a Buck-boost converter is also integarted to support a wide range of output voltage from 1.7V to 5.2V, which is programmable through I^2C.

The device also integrates two ultra-low quiescent current LDOs. The output voltages of these LDOs can be programmed through I^2C. With input pins available, they can be used to connect or disconnet system load when configured to be operate in bypass mode.

A 12-bit ADC enables battery and system monitoring. It can also be used to measure the battery temperature using a thermistor connected to the TS pin as well as external system signals through the ADCIN pin.

In addition to functioning as MCU GPIO expanders, the four integrated multi-function GPIOs can also be used as enable signals for internal or external voltage regulator power rails, sequence power good indicator, or VSEL pins.

7.1.1 Battery Charging Process

When a valid input source is connected (V_{IN} > V_{UVLO} and V_{BAT}+V_{SLEEP_HYST} < V_{IN} < V_{IN_OVP}), the state of the CHG_DIS bit, the $\overline{CE}$ pin, and the TS pin determine whether a charge cycle is initiated. If either CHG_DIS bit or $\overline{CE}$ pin is set to disable charging, even if V_{HOT} < V_{TS} < V_{COLD} and a valid input source is connected, the BATFET is turned off, preventing any kind of charging of the battery. A charge cycle is initiated when CHG_DIS bit is written to 0 and $\overline{CE}$ pin is low. If either the CHG_DIS bit is set to disable charging or the $\overline{CE}$ pin is high, the device will shut off charging to the battery. Both $\overline{CE}$ and CHG_DIS have to be enabled for charging to occur. The following table shows the $\overline{CE}$ pin and CHG_DIS bit priority to enable/disable charging.

表 7-1. Charge Enable Function Through $\overline{CE}$ Pin and CHG_DIS Bit

/CE PIN	CHG_DIS BIT	CHARGING
LOW	0	Enabled
LOW	1	Disabled
HIGH	0	Disabled
HIGH	1	Disabled

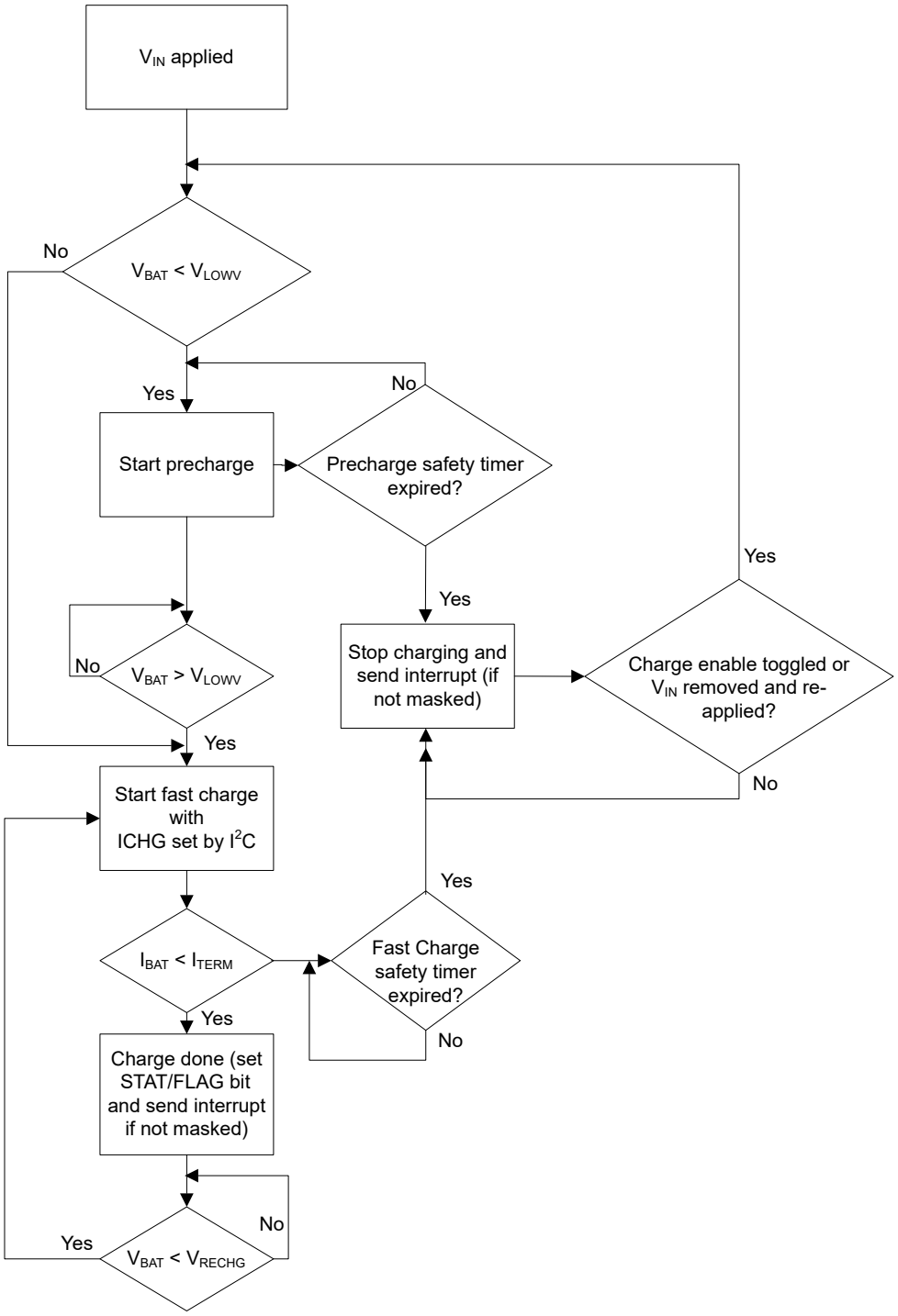


図 7-1. Charger Flow Diagram

The following figure illustrates a typical charge cycle.

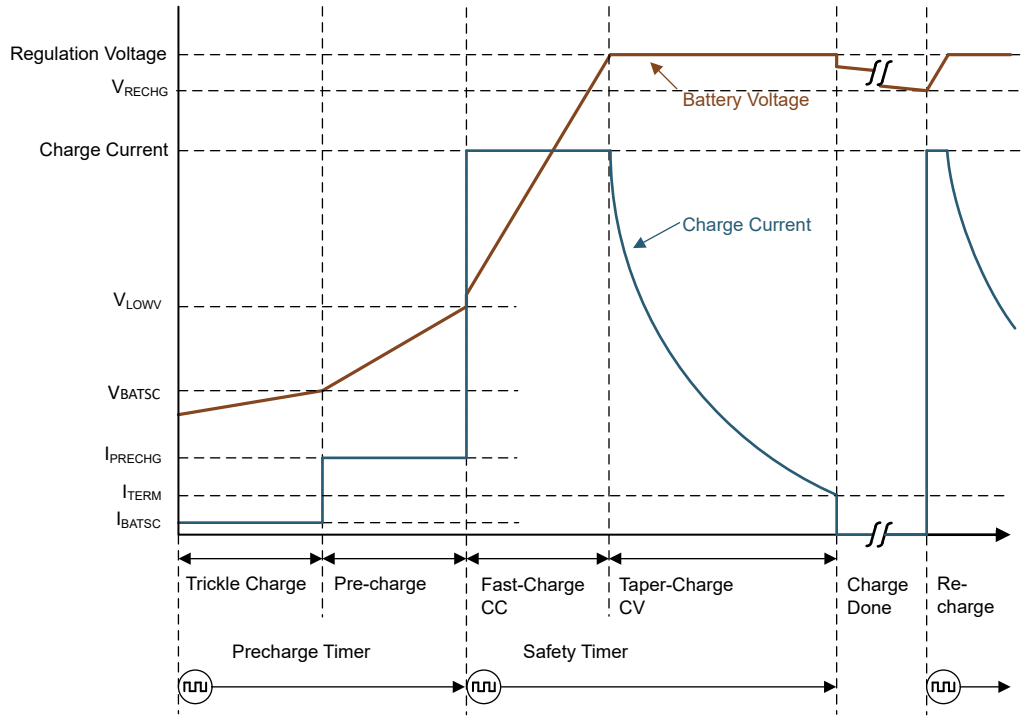


図 7-2. Battery Charging Profile

7.1.1.1 Trickle Charge

In order to prevent damage to the battery, the device will charge the battery at a much lower current level (I_{BATSC}) when the battery voltage is below the V_{BATSC}. During trickle charge, the device still counts against the precharge safety timer. The trickle charge and precharge are counting against the safety timer, for which the duration is 25% of the fast charge timer. The IBATSC bit determines if the trickle charge current is 8mA or 1mA.

7.1.1.2 Precharge

When battery voltage is above the V_{BATSC} but lower than V_{LOWV} threshold, the battery is charged with the precharge current level. The precharge current (I_{PRECHG}) can be programmed through I^2C and can be adjusted by the host with IPRECHG bit. Once the battery voltage reaches V_{LOWV}, the charger will then operate in the fast charge mode, charging the battery at ICHG.

During precharge, the safety timer is set to 25% of the safety timer value during fast charge. In the case where termination is disabled , precharge current is set to 20% of fast charge current setting.

7.1.1.3 Fast Charge

The charger has two main control loops that control charging when $V_{BAT} > V_{LOWV}$: the Constant Current (CC) and Constant Voltage (CV) loops. When the CC loop is active, the battery is charged at the maximum charge current level I_{CHG}, unless there is a TS fault condition (or JEITA condition), VINDPM is active, thermal regulation or DPPM is active. Once V_{BAT} reaches the V_{REG} level, the CV loop becomes active and the charging current starts tapering off. Once the charging current reaches the termination current (I_{TERM}), the charge is done and CHG_STAT is set to b11. If V_{REG} is set higher than 4.65 V by the I^2C, the battery regulation voltage is still maintained at 4.65 V. The device will switch to fast charge based on V_{LOWV} setting.

The fast charge current is programmable through I^2C with ICHG bits in ICHG_CTRL register.

7.1.1.4 Termination

The device will automatically terminate charging once the charge current reaches I_{TERM}, which is programmable through I^2C. After termination the charger will operate in high impedance mode, disabling the BATFET to disconnect the battery. Power is provided to the system (SYS) by IN supply as long as $V_{IN} > V_{UVLO}$, $V_{IN} > V_{BAT} + V_{SLEEPZ}$ and $V_{IN} < V_{IN\_OVP}$.

Termination is only enabled when the charger CV loop is active. Termination is disabled if the charge current reaches I_{TERM} while the VINDPM, DPPM, ILIM, or thermal regulation loops are active. The charger will only go into the termination when the current drops to I_{TERM} due to the battery reaching the target voltage and not due to the charge current limitation imposed by the previously mentioned controlled loops.

Post termination, the BATFET is disabled and the voltage on BAT pin is monitored to check if it drops to V_{RECHG} threshold. If it does, a new charge cycle is established. The safety timers are reset. During charging or even when charge done, a higher SYS load will be supported through the supplement operation.

7.2 Functional Block Diagram

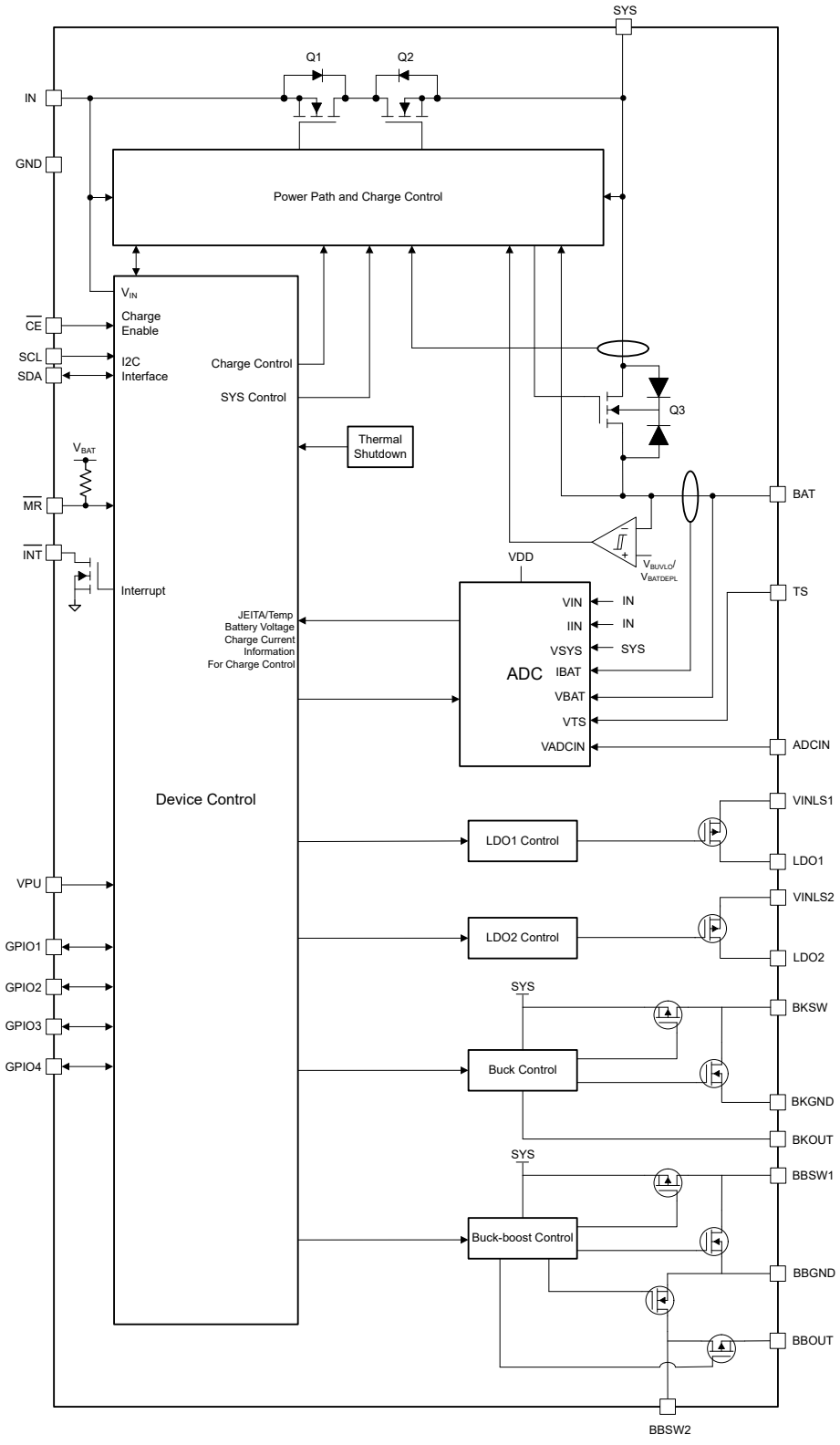


図 7-3. Functional Block Diagram

7.3 Feature Description

7.3.1 Input Voltage Based Dynamic Power Management (VINDPM)

The VINDPM prevents the input voltage from collapsing to a point where SYS would drop. This is done by reducing the current drawn by charger enough to keep V_{IN} regulated at a certain voltage (V_{INDPM}).

During the normal charging process, if the adapter power connected at IN is not sufficient to support both charging current and system load current, V_{IN} decreases. Once the supply drops to V_{INDPM}, I_{IN} is reduced to the current level which the adapter can provide through the blocking FETs to prevent the further reduce of V_{IN}. The V_{INDPM} is programmable through the I^2C register VINDPM and it can also be disabled. VINDPM_ACTIVE_STAT bit is set when VINDPM is active. The safety timer is doubled when VINDPM is active if TMR2X_EN bit is set to 1. Additionally, termination is disabled when VINDPM is active.

7.3.2 Dynamic Power Path Management Mode (DPPM)

With a valid input source connected, the power-path management circuitry monitors the input voltage and current continuously. The current into IN is shared between charge current and system load current. If the sum of the charge current and system load current exceeds I_{LIM} set by ILIM or the input current level reduced to by the VINDPM (whichever is lower), V_{SYS} can drop to the DPPM voltage threshold. In the case, the charge current is reduced by the DPPM loop through the BATFET so that V_{SYS} is regulated at V_{BAT} + V_{DPPM}. If V_{SYS} drops to supplement mode threshold after BATFET charging current is reduced to zero, the part enters supplement mode. Termination is disabled when the DPPM loop is active.

The DPPM can be disabled by setting VDPPM_DIS to 1 which may allow smaller voltage difference between V_{SYS} and V_{BAT}.

The DPPM cannot be disabled when the device is in BATDEPL.

7.3.3 Battery Supplement Mode

When V_{SYS} drops to V_{BAT} - V_{BSUP1}, the device enters supplement mode in which the the battery supplements the system load. The battery stops supplementing the system load when V_{SYS} rises to V_{BAT} + V_{BSUP2}. In supplement mode, the battery supplement current is not regulated. Termination is disabled in supplement mode. V_{BAT} needs to be higher than battery depletion threshold ($V_{BATDEPL}$) for the device to be able to enter supplement mode.

7.3.4 Sleep Mode

The device is in low-power sleep mode if V_{IN} is blow sleep mode threshold and higher than the undervoltage lockout threshold. In sleep mode, the input is isolated from the battery. This feature prevents draining the battery during the absence of V_{IN}. When the device enters the sleep mode, VIN_PGOOD_STAT is set to 0.

7.3.5 SYS Power Control

The device also offers the option to control SYS through the SYS_MODE bits. SYS_MODE can force SYS to be supplied by BAT instead of IN (even if V_{IN} > V_{BAT} + V_{SLEEP_HYST}), leave SYS floating or pull SYS to ground. The table below show the device behavior based on SYS_MODE setting:

表 7-2. SYS_MODE Bit Settings

SYS_MODE	DESCRIPTION	SYS SUPPLY	SYS PULLDOWN
b00	Normal Operation	IN or BAT	Off except in SYS pulldown states shown in 表 7-3
b01	Force BAT power (IN disconnected)	BAT	Off except in SYS pulldown states shown in 表 7-3
b10	SYS Off –Floating	None	Off
b11	SYS Off – Pulled Down	None	On

SYS_MODE = b00

SYS will be powered from IN if V_{IN} > V_{IN_UVLO}, V_{IN} > V_{BAT} + V_{SLEEPZ_HYST}, and V_{IN} < V_{IN_OVP} (VIN_PGOOD). SYS will powered by BAT if these conditions are not met. SYS will be disconnected from IN or BAT and pulled down when a hardware reset (HW_RESET) occurs, the device goes into ship mode, or SYS_MODE is set to b11.

SYS_MODE = b01

When this configuration is set, SYS will be powered by BAT if V_{BAT} > $V_{BATDEPL}$ regardless of V_{IN} state. This allows the host to minimize the current draw from the adapter while it is still connected as needed in the system. If SYS_MODE = b01 is set while V_{BAT} < $V_{BATDEPL}$, the SYS_MODE = b01 setting will be ignored and the device will go to the default SYS mode. When the device is in the forced battery power mode (SYS_MODE = b01), if V_{BAT} < $V_{BATDEPL}$, the device will go to the default SYS mode.

If the adapter is toggled (V_{IN}<V_{IN_UVLO}) , the device will switch to the default SYS mode. This prevents the device from needing a POR in order to restore power to the system thereby allowing battery charging. If SYS_MODE = b01 is set during charging, charging will be stopped and the battery will start to power SYS as needed. The behavior is similar to that when the input adapter is disconnected.

SYS_MODE = b10

When this configuration is set, SYS will be disconnected and left float. The device remains on and active.Toggling V_{IN} will reset the SYS_MODE to the default SYS mode.

SYS_MODE = b11

When this configuration is set, SYS will be disconnected from both IN and BAT and pulled to ground by R_{SYS_PD}. Toggling V_{IN} (V_{IN} <V_{IN_UVLO}) will reset the SYS_MODE to the default SYS mode. Power-down sequence is implemented when setting SYS_MODE to b11.

7.3.5.1 SYS Pulldown Control

The device has an internal pulldown on the SYS pin which is enabled in the following cases:

表 7-3. SYS Pulldown States

STATE	NOTES
ship mode	Pulldown on SYS is enabled with power-down sequence. Then the device enters the ship mode.
HW_RESET	Pulldown on SYS is enabled with power-down sequence. The SYS pull-down is retained until the autowake timer expires.
SYS_MODE = b11 (SYS pulldown mode)	Pulldown on SYS is enabled with power-down sequence. The SYS pull-down is retained until SYS_MODE is changed to b00/b01/b10 or VIN is toggled.

7.3.6 SYS Regulation

The device includes a SYS voltage regulation loop. By regulating the SYS voltage, the device prevents downstream devices connected to SYS from being exposed to voltages as high as VIN_OVP. SYS regulation is only active when V_{IN} > V_{IN_UVLO}, V_{IN} > V_{BAT} + V_{SLEEPZ_HYST} and V_{IN} < V_{IN_OVP} (VIN_PGOOD).

SYS voltage regulation target can be controlled through the SYS_REG_CTRL bits on the SYS_REG register to either track the battery, set to a fixed voltage, or enable pass-through modes.

In battery tracking mode, the minimum voltage is at V_{MINSYS} value for battery < 3.6 V. As battery voltage increases, V_{SYS} is regulated to typically 225 mV above battery. If V_{IN} <V_{MINSYS} and VIN_PGOOD is still active, then the SYS will be in dropout.

In the fixed voltage mode, the SYS voltage is regulated to a target set by the host ranging from 4.4 V to 4.9 V. If V_{IN} voltage is less than the SYS target voltage, then the device will be in dropout mode.

In pass-through mode, the SYS path is unregulated and the V_{SYS} voltage is equal to V_{IN}. SYS can only be set to pass-through mode if VIN_OVP bit is set to 0 for 5.7V V_{IN_OVP}. If VIN_OVP bit is already set to 1 for 18.5V V_{IN_OVP}, SYS cannot be set to pass-through mode (SYS_REG_CTRL = 111) through I^2C transaction. Likewise, if SYS is already in pass-through mode, the V_{IN_OVP} cannot be set to 18.5V (VIN_OVP = 1) through I^2C transaction.

Sufficient SYS capacitance should be used so that V_{SYS} does not exceed maximum ratings of the system loads.

表 7-4. SYS Voltage Regulation Settings

SYS_REG_CTRL	VSYS TARGET
b000	VBAT + 225 mV (3.8 V minimum)
b001	4.4
b010 (default)	4.5
b011	4.6
b100	4.7
b101	4.8
b110	4.9
b111	Pass-through

7.3.7 ILIM Control

The input current limit can be controlled by the ILIM bits through I^2C.

If the ILIM regulation loop is active, ILIM_ACTIVE_STAT bit is set after the input current limit deglitch t_{ILIM}. When the ILIM regulation loop is active, termination is suspended.

The ILIM_ACTIVE_MASK will prevent interrupt from being issued but does not override the ILIM behavior itself. ILIM value can be programmed dynamically through the I^2C by the host. The ILIM settings of 100mA and 500mA are designed to be the maximum value to support standard systems.

7.3.8 Protection Mechanisms

7.3.8.1 Input Overvoltage Protection

Input overvoltage protection protects the device and downstream components connected to SYS, and BAT against damage from overvoltage on the input supply. The input overvoltage protection thresholds are dependend on VIN_OVP bit.When VIN > V_{IN_OVP}, a VIN overvoltage condition is determined to exist. During the VIN overvoltage condition, the device turns the input FET OFF, battery discharge FET ON, sends a single 128-µs pulse on INT unless VIN_OVP_FAULT_MASK is set to be 1, and the fault bit (VIN_OVP_FAULT_FLAG) is updated over I^2C. The VIN_PGOOD_STAT bit also is affected by the VIN overvoltage condition as the VIN power good (VIN_PGOOD) condition will fail. Once the VIN overvoltage condition is removed ($V_{IN} \leq V_{IN\_OVP}$ - $V_{IN\_OV\_HYST}$), the VIN_OVP_STAT bit is cleared and the device returns to normal operation. Thereafter, a VIN power good (VIN_PGOOD) condition is determined if $V_{IN} > V_{BAT} + V_{SLEEPZ\_HYST}$ and $V_{IN} > V_{IN\_UVLO}$.

7.3.8.2 System Short Protection

When a valid adapter is connected to the device, the device detects if the SYS pin is shorted. If $V_{SYS} < V_{SYS\_SHORT}$, SYS short fault protection is implemented to turn off the input FET for ~200µs and turn it back ON for 5 ms for SYS to rise above V_{SYS_SHORTZ}. If after 10 tries, the SYS short still persists, the device will not turn on input FETs for 2s and 10-retry counter is reset while BATFET is turned on (if $V_{BAT} > V_{BATDEPL}$) to power SYS. SYS_SHORT_FAULT_STAT and SYS_SHORT_FAULT_FLAG are set to 1 with interrupt signal being sent if not

masked by SYS_SHORT_FAULT_MASK. After 2s, SYS_SHORT_FAULT_STAT is reset to 0 and the device will turn on the input FET for 5 ms and retry 10 times if necessary until the SYS rises above V_{SYS_SHORTZ}.

7.3.8.3 Battery Depletion Protection

To prevent deep discharge of the battery, the device integrates a battery depletion protection feature which disengages the BAT to SYS path when voltage at the battery drops below $V_{BATDEPL}$ programmed by BATDEPL bits in the CHARGECTRL1 register.

In battery only mode, the BATFET is turned on if V_{BAT} rises to be higher than $V_{BATDEPLZ}$. The BATFET is turned off if V_{BAT} falls to be lower than $V_{BATDEPL}$.

BATDEPL status is reported by BATDEPL_FAULT_STAT bit. BATDEPL_FAULT_FLAG is set to 1 if battery depletion is detected. a 128-µs pulse ($\overline{INT}$ pin pulled down) is sent on $\overline{INT}$ to notify the host if not masked by BATDEPL_FAULT_MASK.

7.3.8.3.1 Battery Undervoltage Lockout

If VIN is not present (V_{IN}<V_{IN_UVLO}), V_{BAT} needs to be higher than V_{BUVLO} for the device to be powered up.

In battery mode and ship mode (including LDO1-ON ship mode), the device is turned off if V_{BAT} falls below V_{BUVLO}.

7.3.8.4 Battery Overcurrent Protection

In order to protect the device from overcurrent and prevent excessive battery discharge current, the device detects if the discharge current on the BATFET exceeds I_{BAT_OCP}. If the I_{BAT_OCP} is reached, the BATFET is turned off and the device starts operating in hiccup mode, re-enabling the BATFET t_{REC_SC} (250 ms) after being turned OFF by the overcurrent condition. If the overcurrent condition is triggered upon retry for 4 to 7 consecutive times in a 2-s window, the BATFET remains off until a valid VIN is connected (VIN_PGOOD). If the overcurrent condition and hiccup operation occur while in supplement mode where VIN is already present, VIN must be toggled in order for the BATFET to be enabled and start another detection cycle.

7.3.8.5 Safety Timer and Watchdog Timer

At the beginning of each charge cycle mode (Precharge or Fast Charge), the device starts the respective mode safety timer. If charging has not terminated before the programmed safety timer, t_{MAXCHG}, expires or the device does not exit the precharge mode before t_{PRECHG} expires, charging is disabled. The precharge safety timer, t_{PRECHG}, is 25% of t_{MAXCHG}. When a safety timer fault occurs, a single 128-µs pulse is sent on the $\overline{INT}$ pin and the SAFETY_TMR_FAULT_FLAG is set to 1 in the I^2C register.

If the safety timer has expired, the device will produce an interrupt and update the SAFETY_TMR_FAULT_FLAG bit on the register map. The safety timer duration is programmable using the SAFETY_TIMER bits. When the safety timer is active, changing the safety timer duration resets the safety timer. The device also contains a 2XTMR_EN bit that doubles the fast charge safety timer duration to prevent premature safety timer expiration when the charge current is reduced by a high load on SYS (DPM operation- causing VDPPM to be enabled), VINDPM, ILIM, thermal regulation, or a NTC (JEITA) condition. When 2XTMR_EN bit is set, the fast charge timer is allowed to run at half speed when any loop is active other than CC or CV. In the event where during CC mode the battery voltage drops to push the charger into precharge mode, (due to a large load on battery, thermal events, and so forth) the safety timer will reset counting through precharge and then resetting the fast charge safety timer. If the device entered battery supplement mode while in precharge, CC or CV mode, while the charger is not disabled, the device will suspend the safety timer till the charging can resume back again. This prevents the safety timer from resetting when a supplement condition is caused.

In addition to the safety timer, the device contains a watchdog timer that monitors the host through the I^2C interface. The watchdog timer is enabled by default and may be disabled by the host through an I^2C transaction. Once the initial transaction is received, the watchdog timer is started. The watchdog timer is reset by any transaction by the host using the I^2C interface. If the watchdog timer expires without a reset from the I^2C interface, selected registers are reset to the default values. The watchdog timer can be set through the WATCHDOG_SEL bits.

表 7-5. Watchdog Settings

WATCHDOG_SEL	ACTION
b00	Device only performs a reset for selected register bits after 160s of the last I²C transaction
b01	Device issues a HW_RESET after 160s of last I²C transation
b10	Device sissue a HW_RESET after 40s of the last I²C transaction
b11	Watchdog function is disabled

7.3.8.6 Buck Overcurrent Protection

The Buck rail integrates a current limit on the high-side and low-side MOSFETs to protect the rail against overloading or short circuit conditions. The current in the switches is monitored cycle by cycle. If the high-side MOSFET current limit trips, the high-side MOSFET is turned off and the low-side MOSFET is turned on to ramp down the inductor current. Once the inductor current through the low-side switch decreases below the low-side MOSFET current limit, the low-side MOSFET is turned off and the high-side MOSFET turns on again.

7.3.8.7 LDO Overcurrent Protection

LDO1/LDO2 has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brickwall-foldback scheme. The current limit transitions from a brickwall scheme to a foldback scheme at the foldback voltage ($V_{FOLDBACK}$). In a high-load current fault with the output voltage above $V_{FOLDBACK}$, the brickwall scheme limits the output current to the current limit (I_{CL}). When the voltage drops below $V_{FOLDBACK}$, a foldback current limit activates that scales back the current as the output voltage approaches GND. When the output is shorted, the device supplies a typical current called the short-circuit current limit (I_{SC}). I_{CL} and I_{SC} are listed in the *Electrical Characteristics* table.

For this device, $V_{FOLDBACK}$ = 0.5 V.

図 7-4 shows a diagram of the foldback current limit.

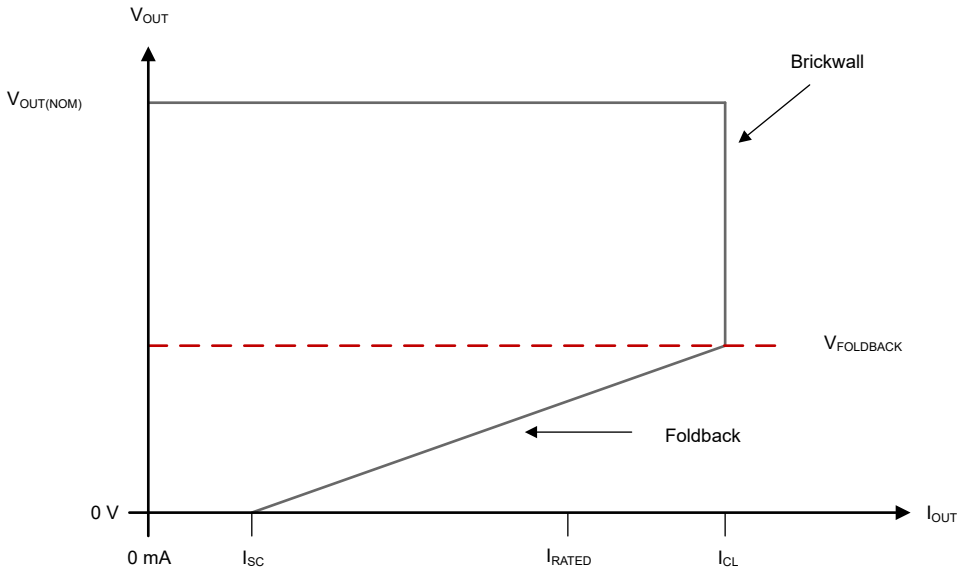


図 7-4. Foldback Current Limit

7.3.8.8 Buck-Boost Overcurrent Protection

The Buck-boost has a inbuilt short circuit protection function to limit the current through its buck bridge high-side MOSFET. The maximum current that flows is limited by the peak current limit, I_{OC_BB}. The typical current limit is 1.55 A for the"unlimited" input current limit setting and 0.29 A for 100 mA input current limit setting. During

startup, the typical current limit is 0.6 A typically to prevent inrush current. The output voltage decreases if the load is higher than the peak current limit.

7.3.8.9 Buck-Boost Output Short-Circuit Protection

The Buck-boost rail integrates the output short-circuit protection to limit the power dissipation in case the output is shorted. If the Buck-boost output voltage falls below 1.25V typical, the Buck-boost rail input current is limited to below 30mA typically.

7.3.8.10 Buck/Buck-Boost/LDO Undervoltage Lockout

Buck/Buck-boost/LDO1/LDO2 has an independent undervoltage lockout (UVLO) circuit that monitors the input voltage, allowing a controlled and consistent on and off of the output voltage. The UVLO comparator shuts down the device when the input voltage is less than UVLO falling threshold and enables the rail when the input voltage exceeds UVLO rising threshold. The LDO's UVLO thresholds are still active if it is configured to be operating in the bypass mode.

7.3.8.11 Sequence Undervoltage Lockout

If power sequence is used, the sequence UVLO (SEQ_UVLO) condition needs to be met in order for any sequence power rail to be enabled, which is that V_{SYS} needs to be higher than the SEQ_UVLO thresdholds (V_{SEQ_UVLO} and V_{SEQ_UVLOZ}). SEQ_UVLO disables all the sequence power rails at the same time.

7.3.8.12 Thermal Protection and Thermal Regulation

During operation, to protect the device from damage due to overheating, the junction temperature of the die is monitored.

In adapter mode, the TSHUT fault is triggered when T_J reaches T_{SHUT_RISING}, or T_{J_BUCK} reaches $T_{SHUT\_RISING\_BUCK}$ if Buck is enabled, or T_{J_BB} reaches $T_{SHUT\_RISING\_BB}$ if Buck-boost is enabled, or T_{J_LDO1} reaches $T_{SHUT\_RISING\_LDO1}$ if LDO1 is enabled, or T_{J_LDO2} reaches $T_{SHUT\_RISING\_LDO2}$ if LDO2 is enabled. In this case, the device stops charging, disables all the operating power rails, and then turns off input FETs and BATFET. After t_{TSHUT_DGLZ}, if T_J is below $T_{SHUT\_FALLING}$, the input FETs and BATFET are turned on to power SYS and charging can be restarted. The integrated power rails are reenabled when TSHUT fault recovers. The power-up sequence is implemented if power sequence is used with V_{SYS}>V_{SEQ_UVLOZ}.

In battery mode with ADC disabled (ADC_EN = 0), the TSHUT fault is triggered when T_{J_BUCK} reaches $T_{SHUT\_RISING\_BUCK}$ if Buck is enabled, or T_{J_BB} reaches $T_{SHUT\_RISING\_BB}$ if Buck-boost is enabled, or T_{J_LDO1} reaches $T_{SHUT\_RISING\_LDO1}$ if LDO1 is enabled, or T_{J_LDO2} reaches $T_{SHUT\_RISING\_LDO2}$ if LDO2 is enabled. In this case, the device disables all the operating power rails. After t_{TSHUT_DGLZ}, the BATFET is turned on to power SYS. The integrated power rails are reenabled when TSHUT fault recovers. The power-up sequence is implemented if power sequence is used with V_{SYS}>V_{SEQ_UVLOZ}.

In battery only mode with ADC disabled (ADC_EN = 1), the TSHUT fault is triggered when T_J reaches T_{SHUT_RISING} , or T_{J_BUCK} reaches $T_{SHUT\_RISING\_BUCK}$ if Buck is enabled, or T_{J_BB} reaches $T_{SHUT\_RISING\_BB}$ if Buck-boost is enabled, or T_{J_LDO1} reaches $T_{SHUT\_RISING\_LDO1}$ if LDO1 is enabled, or T_{J_LDO2} reaches $T_{SHUT\_RISING\_LDO2}$ if LDO2 is enabled. In this case, the device disables all the operating power rails, and then turns off the BATFET. After t_{TSHUT_DGLZ}, if T_J is below $T_{SHUT\_FALLING}$, the BATFET is turned on to power SYS. The integrated power rails are reenabled when TSHUT fault recovers. The power-up sequence is implemented if power sequence is used with V_{SYS}>V_{SEQ_UVLOZ}.

The Buck thermal shutdown protection is not active in PFM mode and LDO1/LDO2 thermal shutdown is not active with load less than 1 mA.

When TSHUT fault is triggered, TSHUT_STAT/TSHUT_FLAG is set to 1 with interrupt signal sent from $\overline{INT}$ pin if TSHUT_MASK is not set to 1.

If TSHUT_LOCKOUT_EN is set to 1, the device is locked out in TSHUT protection (input FETs off, BATFET off, rails disabled) if TSHUT fault is triggered 7 to 13 times in the 2s window. Once the device is locked out in TSHUT protection, VIN needs to be toggled to bring the device out of the lock-out state after t_{TSHUT_DGLZ}. After t_{TSHUT_DGLZ}, if T_J is below $T_{SHUT\_FALLING}$, the input FETs or BATFET are able to be turned on to power SYS and

charging can be restarted. The integrated power rails are reenabled when TSHUT fault recovers. The power-up sequence is implemented if power sequence is used with V_{SYS}>V_{SEQ_UVLOZ}.

When LDO1 is in always on mode (LDO1_EN_SET = b111) and LDO1_SHIP_AO is set to 1, the LDO1 is disabled only when T_J T_J reaches $T_{SHUT\_RISING\_LOD1}$ and resumes operation when T_J falls below $T_{SHUT\_FALLING\_LOD1}$. In LDO1-ON Ship mode, TSHUT_STAT/TSHUT_FLAG is not updated if the fault is triggered.

During the charging process, to prevent overheating in the device, the device monitors the junction temperature of the die and reduces the charging current once T_J reaches the thermal regulation threshold (T_{REG}) based on bits set by THERM_REG setting. If the charge current is reduced to 0, the battery supplies the current needed to supply the SYS output. Thermal regulation can be disabled through I^2C.

Four temperature settings are selectable in I^2C and shown in セクション 7.6.

The die junction temperature, T_J, can be estimated based on the expected board performance using the following equation:

$T_J = T_A + \theta_{JA} * P_{DISS}$

The θ_{JA} is largely driven by the board layout. For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics Application Report*.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed operational specifications. Although the thermal protection of the device is designed to protect against overheat conditions, it is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

7.3.9 Integrated 12-Bit ADC for Monitoring

The device provides an integrated 12-bit ADC for the host to monitor various system parameters. The ADC_RATE bits allow continuous conversion, conversion every 1 second, conversion every 1 minute, and one-shot behavior.

To enable the ADC, the ADC_EN bit must be set to '1'. The ADC is disabled by default (ADC_EN=0) to conserve power. The ADC is allowed to operate if either V_{IN}>V_{IN_UVLO} or V_{BAT}>$V_{BAT\_ADC\_LOWVZ}$. In battery mode, if ADC_EN is written to '1' by the host with V_{BAT} < $V_{BAT\_LOWVZ\_ADC}$, it will then be automatically cleared. ADC_EN should not be set to 1 when no channel is enabled.

The ADC range for VIN is dependent on the VIN_OVP bit.

The ADC supports averaging by setting ADC_AVG = 1. In averaging mode, each new sample is averaged with the previous value of that channel's output register. When ADC_AVG_INIT = 1, the first converted value is stored without averaging, and each subsequent value is averaged. In this mode, the first stored value is X_0, the second value is (½ X_1 + ½ X_0) and the third stored value is (½ X_2 + ¼ X_1 + ¼ X_0), where X0, X1 and X2 are the sequential values measured by the ADC. When ADC_AVG = 1 and ADC_AVG_INIT = 1 in one-shot mode, two samples are taken and averaged.

The ADC_DONE_STAT and ADC_DONE_FLAG bits will be set when a conversion is complete in one-shot mode, every 1 second mode, and every 1 minute mode. During continuous conversion mode, the ADC_DONE_STAT and ADC_DONE_FLAG bits have no meaning and will remain at 0. In one-shot mode, the ADC_EN bit will be set to 0 at the completion of the conversion, at the same time as the ADC_DONE_FLAG bit is set and a 128-µs pulse is sent on $\overline{INT}$ pin to notify the host. In continuous mode, the ADC_EN bit remains at 1 until the user disables the ADC by setting it to 0. In conversion every 1 second mode and conversion every 1 minute mode mode, the ADC_IN bit stays high in the waiting period in between measurements, but the digital signal will turn off the ADC in the background to save power. After an one-shot ADC cycle is done, the user should wait for at least 25ms before setting ADC_RATE to continuous and enable ADC by setting ADC_EN to 1.

ADC conversion operates independently of the faults present in the device. ADC conversion will continue even when a fault has occurred, with the exception of the TSHUT fault, which disables the ADC until the fault clears.

The device has an ADCIN input to monitor the value of an external voltage signal up to 5V or support another NTC thermister measurement without the need of an external biasing circuit by setting ADCIN_MODE bit to '1'. In this mode, the ADCIN pin is biased with 80µA bias current, same as TS pin, and V_{ADCIN} is monitored up to 1V.

The TDIE and IBAT ADC channel registers report in 2's compliment format in order to represent positive and negative current. 16-bit registers in 2's compliment represent positive numbers using the range 0x0000 - 0x7FFF, with 0x0 representing 0 and 0x7FFF representing the maximum positive value of 32,767. The negative numbers are represented in the range 0x8000-0xFFFF with 0x8000 representing the most negative value of -32,768 and 0xFFFF representing -1. Note that these are the raw integer values of the register. To convert into the current reading of the ADC, multiply this integer by the scaling factor of the register.

7.3.9.1 ADC Programmable Comparators

The device has three programmable ADC comparators that may be used to monitor any of the ADC channels as configured through the ADCCTRL1 and ADCCTRL2 registers. The comparators will send an interrupt (if not masked) and set the flags (COMP1_ALARM_FLAG/COMP2_ALARM_FLAG/COMP3_ALARM_FLAG) whenever the corresponding channel's ADC measurement result crosses the threshold programmed in their respective ADCALARM1/ADCALARM2/ADCALARM3 bits in the direction indicated by the ADCALARM1_ABOVE/ ADCALARM2_ABOVE/ADCALARM3_ABOVE bit. Note that the interrupts are masked by default and must be unmasked by the host to use this function.

For all the ADC channels except for the IBAT channel, the LSB of ADCALARM1/ADCALARM2/ADCALARM3 bits is corresponding to the same value as the channel's ADC result's LSB. For the IBAT channel, the ADCALARM1/ADCALARM2/ADCALARM3 bits' LSB is corresponding to 2mA instead of 1mA as in ADC_DATA_IBAT. Also, when the comparators are used to monitor TDIE and IBAT channels, the MSB of ADCALARM1/ADCALARM2/ADCALARM3 bits is the sign bit.

7.3.10 Pushbutton Wake and Reset Input

$\overline{MR}$ pin is internally pulled up such that it can work as a pushbutton to detect if it's being pulled low. The pushbutton function implemented through the $\overline{MR}$ pin has three main functions. First, it serves as a means to wake the device from ultra-low power modes like ship mode ($\overline{MR}$ pin pressed for $t_{SHIPWAKE}$). Second, it serves as a short button press detector, sending an interrupt to the host when the button driving the $\overline{MR}$ pin has been pressed for t_{WAKE1}, t_{WAKE2} durations. This allows the implementation of different functions in the end application such as menu selection and control. Finally it serves as a means to get the device into ship mode or reset the system (Hardware Reset) by performing a power cycle/ hardware reset (shut down SYS and automatically power it back on) after detecting a long button press ($\overline{MR}$ pin pressed for t_{LPRESS}). t_{LPRESS_WARN} before $\overline{MR}$ pin being pulled low for t_{LPRESS}, the device also sends an interrupt to warn the host the long press action is imminent. The timings of t_{WAKE1}, t_{WAKE2}, and t_{LPRESS} are programmable through I^2C for added flexibility and allows system designers to customize the end user experience of a specific application. Note that if a specific timer duration is changed through I^2C while that timer is active and has not expired, the new programmed value will be ignored until the timer expires and/or is reset by new push button action. If a button press is registered, the device will begin counting against t_{WAKE1}, t_{WAKE2} or t_{LPRESS}.

7.3.10.1 Pushbutton Short Button Press or Wake Functions

There are two programmable short button press timers, t_{WAKE1} and t_{WAKE2}. There are no specific actions taken by the t_{WAKE1} or t_{WAKE2} durations other than issuing an interrupt (if not masked) and updating the WAKE1_FLAG or WAKE2_FLAG registers. For a wake from ship mode event, the push button ($\overline{MR}$ pin) has to be low for $t_{SHIPWAKE}$ with $V_{BAT}>V_{BUVLO}$ before it can turn ON the SYS rail.

In the case where an input source ($V_{IN} > V_{IN\_UVLO}$) is connected prior to $t_{SHIPWAKE}$ timer expiring, the device will exit the Ship mode regardless of the $\overline{MR}$ pin or wake timer state.

7.3.10.2 Pushbutton Long Button Press Functions

Depending on the configuration set on pushbutton long press action register bits (PB_LPRESS_ACTION_1:0), the device will perform a ship mode entry or Hardware Reset or completely ignore the long button press action. If HOST_HW_RESET_VIN_REQ bit is set to 1, the Hardware Reset can only start with $V_{IN} > V_{IN\_UVLO}$.

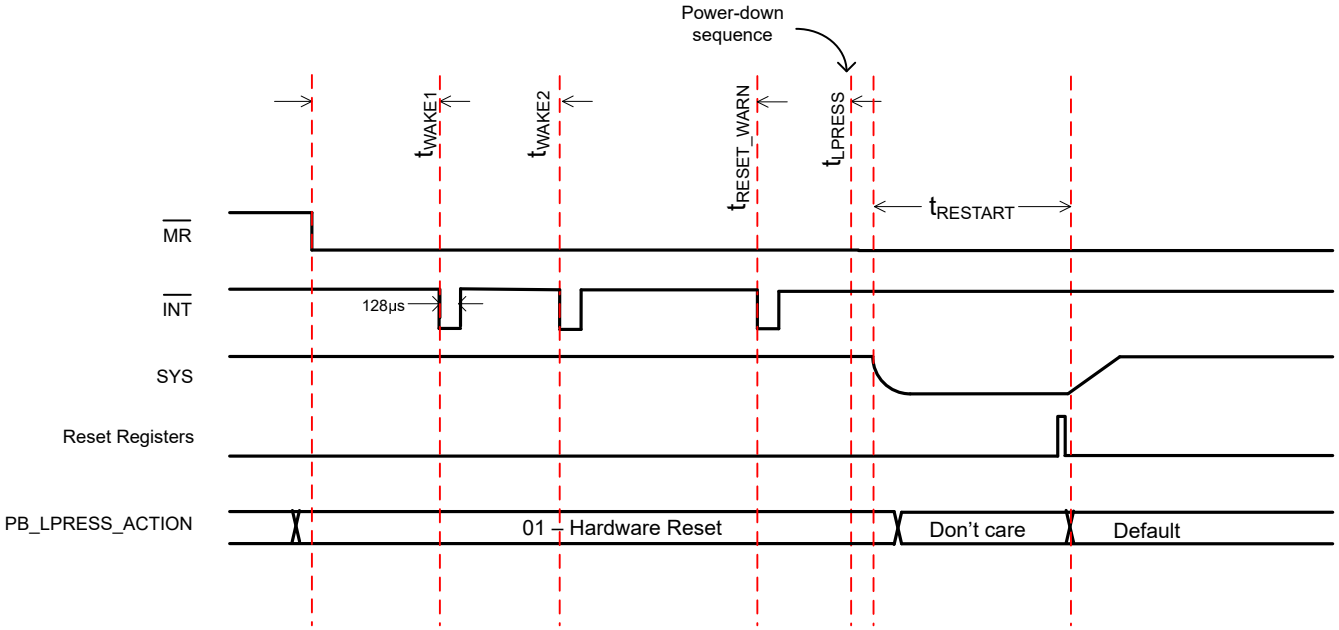


図 7-5. Pushbutton Long Press for Hardware Reset

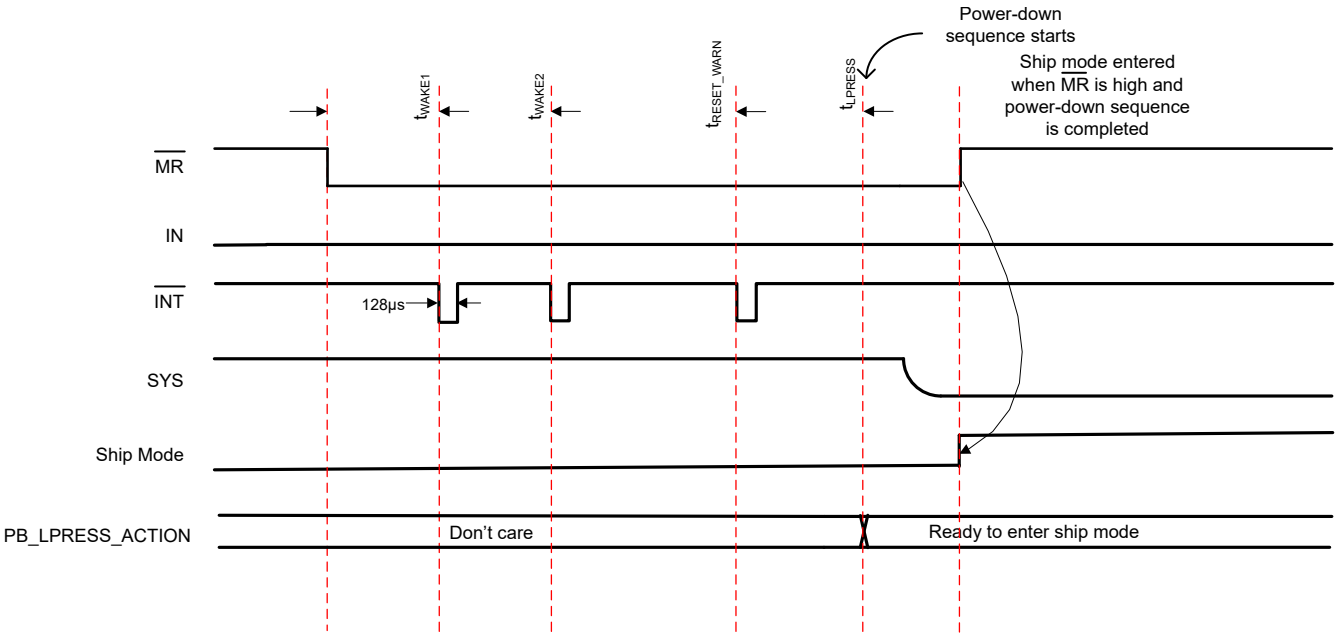


図 7-6. Pushbutton Long Press for Ship Mode Entry

7.3.11 VIN Pulse Detection for Hardware Reset

For applications with no pushbutton to implement the Hardware Reset, the device offers an function which detects a sequence of pulses at IN pin that would trigger the Hardware Reset. The device detects 3 pulses with

width of at least 500ms in an 8-second window. Less than or more than 3 pulses would not generate a HW reset. Once the 8-second window expires and the 3 pulses have been detected, the Hardware Reset is implemented.

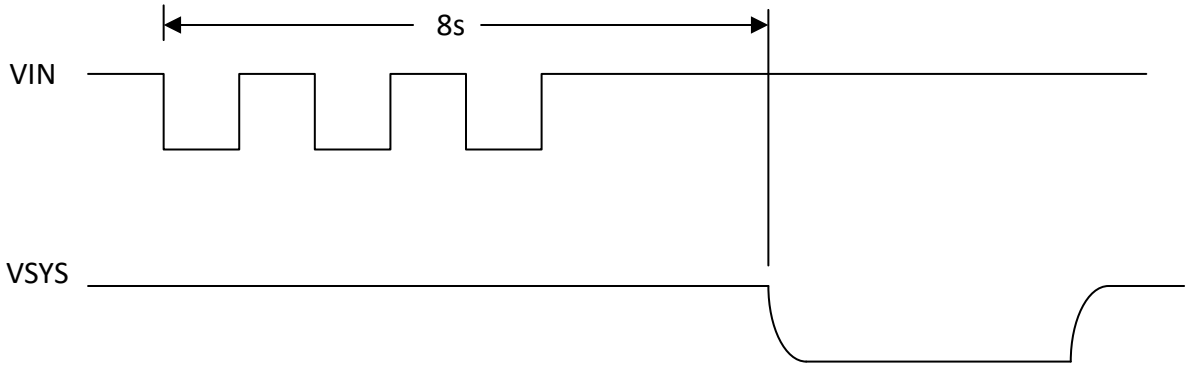


図 7-7. VIN Pulse Detection for Hardware Reset

7.3.12 15-Second VIN Watchdog for Hardware Reset

The 15-second watchdog can be enabled/disabled through I^2C by the WATCHDOG_15S_ENABLE bit. When the function is enabled, the device implements the Hardware Reset if the host does not respond 15 seconds after the adapter is connected with VIN_PGOOD_STAT being set.If the adapter is connected and the host responds before the 15-second watchdog expires, the part continues operating normally.

7.3.13 Hardware Reset

The device is capable of implementing the Hardware Reset (HW_RESET) to powercycle the system. This is partcularly useful when a software reset on the host side fails to work. Below is a sequence of events during a Haredware Reset:

1. Implement power-down sequence
2. Start the autowake timer (t_{RESATR})
3. Once the autowake timer expires, disconnect the pulldown on SYS
4. Reset all the register bits to default values
5. Turn on the BATFET (without BATDEPL fault) and input FETs (with VIN_PGOOD) to power the system.
6. Enable integrated power rails based on corresponding enable settings.

7.3.14 Software Reset

When a software reset is issued by the REG_RST bit, the device resets selected register bits to default values. The selected register bits are shown in the register map.

7.3.15 Interrupt to Host ($\overline{INT}$)

The device contains an open-drain output ($\overline{INT}$) to notify the host if a certain status has changed.

The $\overline{INT}$ pin is normally in high impedance and is pulled low for 128µs when an interrupt condition occurs.

Interrupts can be masked through I^2C. If the interrupt condition occurs while the interrupt is masked, the interrupt pulse will not be sent. If the interrupt is unmasked while the fault condition is still present, an interrupt pulse will not be sent until the interrupt triggering condition occurs while it is not unmasked.

7.3.16 External NTC Monitoring (TS)

The I^2C interface allows the user to easily implement the JEITA standard for systems where the battery pack thermistor is monitored by the host. The NTC thermistor is biased by the device with I_{TS_BIAS} and the resulting voltage at TS is monitored to determine that the battery is at a safe temperature during charging. The TS fault monitoring is enabled by TS_FAULT_BAT_EN bit in battery mode and TS_FAULT_VIN_EN in adapter mode. I_{TS_BIAS} is turned off when TS fault monitoring is disabled in both battery mode and adapter mode.

The part can be configured to meet JEITA requirements or a simpler HOT/COLD function only. Additionally, the TS charging control function can be disabled through the TS_ACTION_EN bit. This bit only disables the TS charge action but the faults are still reported. To satisfy the JEITA requirements, four temperature thresholds are monitored: the cold battery threshold, the cool battery threshold, the warm battery threshold, and the hot battery threshold which are all fully programmable with TS_COLD/TS_COOL/TS_WARM/TS_HOT register bits.

Charging and safety timers are suspended when $V_{TS} < V_{HOT}$ or $V_{TS} > V_{COLD}$. When $V_{COOL} < V_{TS} < V_{COLD}$, the charging current is reduced to the value programmed by the TS_ICHG bit. When $V_{HOT} < V_{TS} < V_{WARM}$, the battery regulation voltage is reduced to the value programmed by the TS_VREG bit.

When a TS fault is confirmed, the corresponding TS fault status is reported by TS_STAT bits and TS_FLAG bit set to 1 to reflect that a change to TS_STAT was detected. If not masked by TS_MASK, a 128-µs pulse is sent on /INT pin to notify the host about the TS_STAT change.

In battery mode (with $V_{BAT}>V_{BAT\_ADC\_LOWVZ}$), the TS faults can still be reported through I^2C when TS fault monitoring is enabled (TS_FAULT_BAT_EN=1). If TS fault monitoring is enabled, V_{TS} is monitored at the rate following the ADC_RATE bits (even with ADC_EN = 0), which can be in continuous conversion mode, one-shot conversion mode, every 1 second mode, or every 1 minite mode. The every-1-second and every-1-minute modes can be used to monitor V_{TS} periodically in an efficient way as the battery current consumption is low during the wait time with I_{TS_BIAS} also disabled.

7.3.16.1 TS Thresholds

The device monitors the TS voltage and sends an interrupt (if not masked) to the host whenever it crosses the V_{HOT}, V_{WARM}, V_{COOL} and V_{COLD} thresholds which correspond to different temperature thresholds based on the NTC resistance and biasing. Each threshold can be programmed via I^2C through the TS_COLD, TS_COOL, TS_WARM and TS_HOT registers. V_{COOL} threshold is disabled if TS_COOL is set to 0 and V_{WARM} threshold is disabled if TS_WARM is set to 0. This allows the device to either meet flexible JEITA requirements or implement a simpler HOT/COLD function only. To avoid unexpected behaviors, the thresholds should not be programmed overlapping each other. The device will also disable charging if TS pin exceeds the V_{TS_OPEN} threshold.

The device supports the following TS_HOT and TS_COLD thresholds for a typical 10-KΩ NTC thermister. The TS_COOL and TS_WARM thresholds are disabled by default.

表 7-6. TS Thresholds for 10-kΩ Thermistor

THRESHOLD	TEMPERATURE (°C)	VTS (V)
Open	--	>0.9
Cold	0	0.58
Hot	43	0.276

The TS biasing circuit is shown in 図 7-8. Note that the respective V_{TS} and hence ADC reading for T_{COLD}, T_{COOL}, T_{WARM} and T_{HOT} changes for every NTC, therefore the threshold values may need to be adjusted through I^2C based on the supported NTC type.

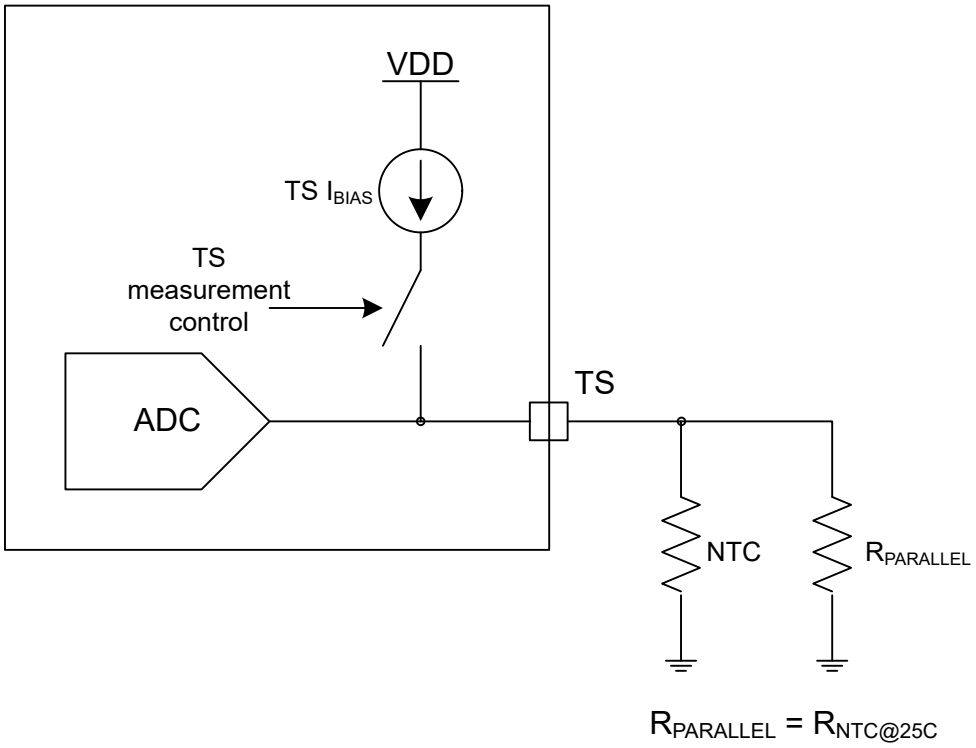


図 7-8. TS Bias Functional Diagram

For accurate temperature thresholds, a 10-kΩ NTC with a 3380 B-constant should be used (Murata NCP03XH103F05RL for example) with a parallel 10-kΩ resistor. For devices where TS function is not needed, tie a 5-kΩ resistor from the TS pin to ground.

7.3.17 Power Rail Power Sequence

The integrated power rails can be configured to be power up or power down in a programmable sequence. In addition, the GPIO pins can be configured to be push-pull power sequencer output which can enable or disable external power rails in the sequence. If at least one of the integrated power rail is configured to be in the sequence or at least one of the GPIO pins is configured to be sequencer output, it means that the power sequence is used. Otherwise, it means that the power sequence is not used. An integrated power rail is a sequence power rail if it is configured to be in the sequence. For Buck or Buck-boost, it can be individually enabled or disabled by I^2C or GPIO if it's not a sequence power rail. Therefore, Buck or Buck-boost can be in sequence mode or individual mode. For LDO1 or LDO2, it can be individually enabled or disabled by $I^2$2 or GPIO, or always on if it is not a sequence power rail. Therefore, the LDO1 and LDO2 can be in sequence mode, individual mode, or always-on mode.

7.3.17.1 Power-Up Sequence

Power-up sequence is implemented when V_{SYS} ramps up exceeding V_{SEQ_UVLOZ} with a SYS power-up condition while $T_J<T_{SHUT\_RISING}$ or during TSHUT recovery while $V_{SYS}>V_{SEQ\_UVLO}$ and power sequence is used. 図 7-9 shows the power-up sequence timing.

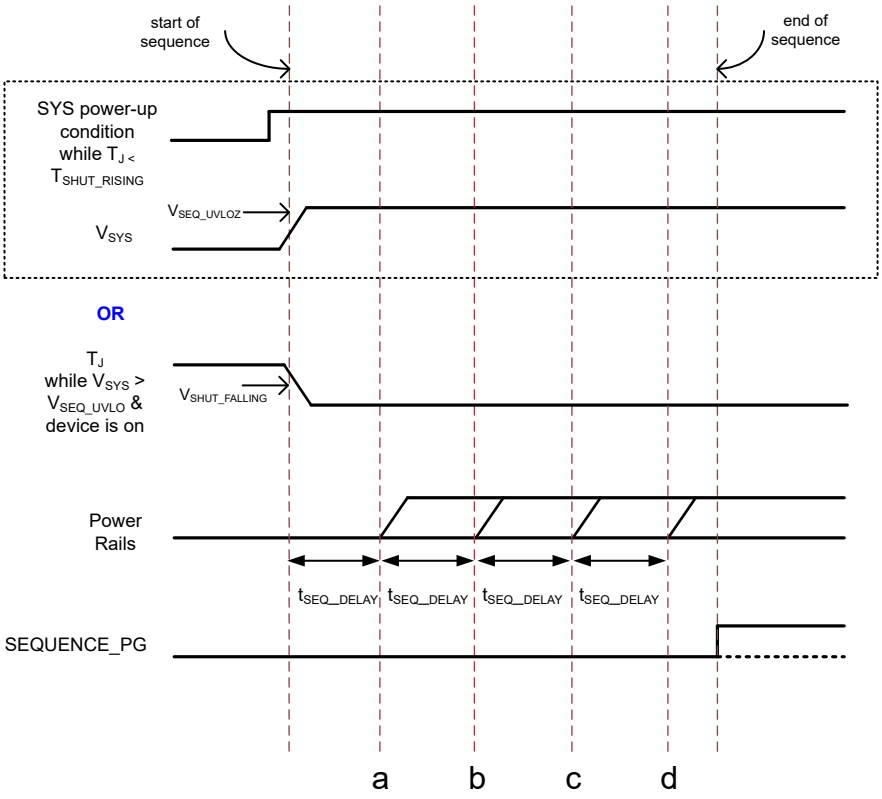


図 7-9. Power-Up Sequence Timing

t_{SEQ_DELAY} after power-up sequence is started, the power rails are enabled at four points, in the order of "a", "b", "c", "d", determined by each power rail's configuration, with t_{SEQ_DELAY} in between. t_{SEQ_DELAY} can be configured by SEQUENCE_DELAY_TIME bits from 1 ms to 64 ms. If GPIOs are configured to be sequencer outputs, they are pulled high at "a", "b", "c", or "d" to enable external loads or power rails.

After "a", "b", "c", and "d", the sequence power rail output voltages are evaluated $t_{SEQ\_PG\_DELAY}$ after "d" to determine the sequence power good status. If all of the sequence power rails are in power good status, SEQUENCE_PG bit is set to 1, indicating that the sequence is in power good status. Otherwise, SEQUENCE_PG bit remains 0.

If power sequence is not used, the device does not wait for four t_{SEQ_DELAY} and one $t_{SEQ\_PG\_DELAY}$ to pass to service individual mode power rail enable or disable request. In this case, the individual mode power rail's enable or disable request can be serviced directly after exiting individual UVLO.

7.3.17.2 Power-Down Sequence

Power-down sequence is implemented when SYS powers down due to a SYS power down condition, which can be Ship mode entry, HW_RESET, or SYS set to pulldown mode (SYS_MODE set to 11). 図 7-10 shows the power-down sequence timing. The power-down sequence is from SYS power down condition being met to SYS being powered down.

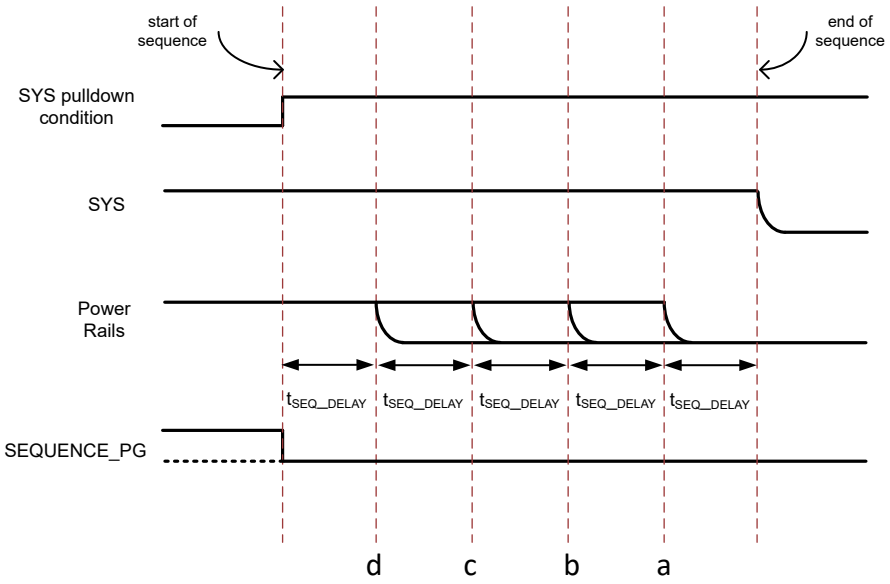


図 7-10. Power-Down Sequence Timing

With a SYS power down condition, SEQUENCE_PG bit is set to 0 immediately. t_{SEQ_DELAY} after SEQUENCE_PG set to 0, the sequence power rails are disabled in the order of "d", "c", "b", "a". If GPIOs are configured to be sequencer outputs, they will apply the corresponding pull-low at "d", "c", "b", or "a" to disable external loads or power rails. The individual mode power rails are disabled all at "d" (if not already disabled). t_{SEQ_DELAY} after "a", the input FET and battery FET are turned off and then, SYS is pulled to GND. If no integrated power rail is in sequence mode and no GPIO is configured as sequencer output, when a SYS power down request is received, then all individual mode power rails are disabled at "d". After "a", the input FET and battery FET are turned off. Then, SYS is pulled to GND.

7.3.18 Integrated Buck Converter (Buck)

The device integrates a synchronous step-down converter (Buck) with ultra low quiescent current consumption. It supports DVS by either I^2C or GPIO3/GPIO4. If BUCK_HI_RANGE is 0, the DVS range is from 0.4V to 1.575V in 12.5mV steps. If BUCK_HI_RANGE is 1, the DVS range is from 0.4V to 3.6V, with 25mV steps from 0.4V to 3.175V and 50mV steps from 3.2V to 3.6V. Note that the change to the BUCK_HI_RANGE takes effect the next time when the user programs the Buck output voltage with I^2C command or GPIO3/GPIO4. GPIO3_CONFIG bits determine if DVS is controlled by I^2C only or both I^2C and GPIO. If GPIO3_CONFIG is set to b0010, DVS is controlled by both I^2C and GPIO. Otherwiser, DVS is controlled by I^2C only. If GPIO3_CONFIG is set to b0010 but GPIO4_CONFIG is not set to b0010, GPIO3 is configured to be VSEL pin to toggle between two output voltage settings. If GPIO3_CONFIG and GPIO4_CONFIG are both set to b0010, GPIO3 and GPIO4 are configured to be VSEL1 pin and VSEL2 pin to toggle between four output voltage settings. If DVS is configured to be controlled by I^2C only, Buck output voltage is set by BUCK_VOUT_SET register. If GPIO3 is configured to be VSEL pin, the output voltage is determined by output voltage mode selection 1 and 2 which are set by BUCK_VOUT1_SET and BUCK_VOUT2_SET, depending on the state of GPIO3 pin as shown in 表 7-7. If

GPIO3 and GPIO4 are configured to be VSEL1 pin and VSEL2 pin, the output voltage is determined by output voltage mode selection 1, 2, 3, and 4 which are programmed by BUCK_VOUT1_SET, BUCK_VOUT2_SET, BUCK_VOUT3_SET, or BUCK_VOUT4_SET repectively, depending on the state of GPIO3 pin and GPIO4 pin combination as shown in 表 7-8. When Buck DVS is controlled by both I^{2}C and GPIO, the BUCK_VOUT1_SET/ BUCK_VOUT2_SET/BUCK_VOUT3_SET/BUCK_VOUT4_SET bits are programmable by I^{2}C to set the Buck output voltage while BUCK_VOUT_SET is automatically updated to match the active output voltage setting.

表 7-7. Buck Output Voltage Setting by VSEL

VSEL (GPIO3)	OUTPUT VOLTAGE MODE SELECTION
LOW	1
HIGH	2

表 7-8. Buck Output Voltage Setting by VSEL1 and VSEL2

VSEL2 (GPIO4)	VSEL1 (GPIO3)	OUTPUT VOLTAGE MODE SELECTION
LOW	LOW	1
LOW	HIGH	2
HIGH	LOW	3
HIGH	HIGH	4

Buck has the output discharge function when it is being disabled. The purpose of this function is to ensure a defined down-ramp of the output voltage when it is disabled and to keep the output voltage close to 0V. The discharge function is only active when Buck is disabled.

7.3.19 Integrated Buck-Boost Converter (Buck-boost)

The device integrates a high-efficiency synchronous buck-boost converter with ultra-low quiescent current. It supports programmable output voltage by I^{2}C from 1.7V to 5.2V in 50mV steps with BUBO_VOUT_SET bits. The Buck-boost does not actively discharge the output capacitor if the actual VOUT is higher than the target. The Buck-boost stops switching until the actual VOUT reaches the target. Therefore, the actual VOUT slew rate is dependent on the load at the output in this case.

Buck-boost has the output discharge function when it is being disabled. The purpose of this function is to ensure a defined down-ramp of the output voltage when it's disabled and to keep the output voltage close to 0V. The discharge function is only active when Buck-boost is disabled.

Buck-boost has an average input current limit function which are configurable by I^{2}C with BUBO_ILIMIT bit, with "unlimited" and 100mA setttings. This function is active during normal operation and at start-up to prevent inrush current.

7.3.20 Integrated LDOs (LDO1/LDO2)

The device integrates two ultra-low quiescent current LDOs, LDO1 and LDO2, which can also be configured to bypass mode to operate as a switch. Therefore, they can provide either a regulated output or gate power to external loads. LDO1 and LDO2 have dedicated input pins VINLS1 and VINLS2 and can support up to 200 mA load current.

The output of voltage of LDO1/LDO2 is programmable using LDO1_VOUT_SET/LDO2_VOUT_SET bits from 0.8V to 3.6V in 50mV steps. The LDO1/LDO2 does not actively discharge the output capacitor if the actual VOUT is higher than the target. The LDO1/LDO2 turns off the internal FET until the actual VOUT reaches the target. Therefore, the actual VOUT slew rate is dependent on the load at the output in this case.

Setting the LDO1_LDO_SWITCH_CONFG/LDO2_LDO_SWITCH_CONFG will configure LDO1/LDO2 to operate in either LDO mode or bypass (switch) mode. Note that in order to change the configuration, LDO1/LDO2 must be disabled first, then the LDO1_LDO_SWITCH_CONFG/LDO2_LDO_SWITCH_CONFG takes effect.

Whether always-on LDO1 is operating in LDO1-ON Ship mode is dependent on the LDO1_SHIP_AO bit setting.If LDO1_SHIP_AO is 1 when power-down sequence is started to enter the Ship mode, the LDO1 VOUT

is set by LDO1_VOUT_SET if LDO1 was in LDO mode and LDO1's ON/OFF status is latched if LDO1 was in bypass mode. For LDO1_SHIP_AO to be effective, LDO1_EN_SET needs to be set to b111.

LDO1/LDO2 has the output discharge function. The purpose of this function is to ensure a defined down-ramp of the output voltage when LDO1/LDO2 is disabled and to keep the output voltage close to 0V. The discharge function is only active when LDO1/LDO2 is disabled. Do not rely on the active discharge circuit for discharging a large amount of output capacitance after the input supply has collapsed because reverse current can possibly flow from the output to the input. This reverse current flow can cause damage to the device. Limit reverse current to no more than 5% of the device rated current for a short period of time.

When LDO1/LDO2 does not have valid input power at VINLS1/VINLS2, it should be disabled.

7.3.21 Multi-Function GPIOs

The device integrates 4 multi-function GPIOs which can be used as individual enable signals for internal power rails, sequencer outputs for external power rails/loads, sequence power good signal, level-shifted $\overline{MR}$ signal, or VSEL pins for Buck rail. The GPIOs can also be used as MCU GPIO expanders since they can be configured to operate in level-sensitive input mode, positive-edge/negative-edge trigger mode, forced push-pull output mode, or open-drain output mode.

7.3.21.1 GPIO1 Functions

GPIO1 can be configured to function as LDO2 EN pin, open-drain output, push-pull output, sequencer output, level-sensitive input, positive-edge/negative-edge trigger input based on different I^2C settings.

To set GPIO1 as the LDO2 EN pin, LDO2_EN_SET should be set to b110 and GPIO1_CONFIG needs to be set to b1000.

If GPIO1_CONFIG = b0010, GPIO1 is set to be in level shifted $\overline{MR}$ output mode. If GPIO1 is set to be the level shifeted $\overline{MR}$, it is pulled up to VPU when $\overline{MR}$ input state is high and it is pulled down to GND when $\overline{MR}$ input state is low.

If GPIO1 is set to be in forced open-drain high state, it is in a HIGH-Z state. If GPIO1 is set to be in forced low state, it is pulled down to GND. If GPIO1 is set to be in forced push-pull high state, it is pulled up to VPU.

If GPIO1 is set to operate as a sequencer output, it is pulled up to VPU or pulled down to GND at the corresponding time instances during power-up/power-down sequence.

If GPIO1 is configured to be in input mode, its current state is readable with the GPIO1_STAT bit. As a positive-edge/negative-edge trigger input, the GPIO1_FLAG will be set when a trigger event happens and a 128µs pulse is sent through the $\overline{INT}$ pin to notify the host.

7.3.21.2 GPIO2 Functions

GPIO2 can be configured to function as Buck-boost EN pin, open-drain output, push-pull output, sequencer output, level-sensitive input, positive-edge/negative-edge trigger input based on different I^2C settings.

To set GPIO2 as the Buck-boost EN pin, BUBO_EN_SET should be set to b110 and GPIO2_CONFIG needs to be set to b1000.

If GPIO_CONFIG = b0010, GPIO2 is set as the sequence PG pin to reflect the sequence PG status, same as the SEQUENCE_PG bit. GPIO2 is pulled up to VPU if SEQUENCE_PG bit is 1 and pulled down to GND if SEQUENCE_PG bit is 0.

If GPIO2 is set to be in forced open-drain high state, it is in a HIGH-Z state. If GPIO2 is set to be in forced low state, it is pulled down to GND. If GPIO2 is set to be in forced push-pull high state, it is pulled up to VPU.

If GPIO2 is set to operate as a sequencer output, it is pulled up to VPU or pulled down to GND at the corresponding time instances during power-up/power-down sequence.

If GPIO2 is configured to be in input mode, its current state is readable with the GPIO2_STAT bit. As a positive-edge/negative-edge trigger input, the GPIO2_FLAG will be set when a trigger event happens and a 128µs pulse is sent through the $\overline{INT}$ pin to notify the host.

7.3.21.3 GPIO3 Functions

GPIO3 can be configured to function as Buck EN pin, open-drain output, push-pull output, sequencer output, level-sensitive input, positive-edge/negative-edge trigger input based on different I^2C settings.

To set GPIO3 as the Buck EN pin, BUCK_EN_SET should be set to b110 and GPIO3_CONFIG needs to be set to b1000.

If GPIO3_CONFIG = b0010, GPIO3 is configured as the VSEL/VSEL1 pin to support Buck GPIO DVS function. When GPIO3 is configured to be VSEL pin or VSEL1 pin, it's High/Low state is read to determine the which voltage setting to be used for Buck.

If GPIO3 is set to be in forced open-drain high state, it is in a HIGH-Z state. If GPIO3 is set to be in forced low state, it is pulled down to GND. If GPIO3 is set to be in forced push-pull high state, it is pulled up to VPU.

If GPIO3 is set to operate as a sequencer output, it is pulled up to VPU or pulled down to GND at the corresponding time instances during power-up/power-down sequence.

If GPIO3 is configured to be in input mode, its current state is readable with the GPIO3_STAT bit. As a positive-edge/negative-edge trigger input, the GPIO3_FLAG will be set when a trigger event happens and a 128µs pulse is sent through the $\overline{INT}$ pin to notify the host.

7.3.21.4 GPIO4 Functions

GPIO4 can be configured to function as LDO1 EN pin, open-drain output, push-pull output, sequencer output, level-sensitive input, positive-edge/negative-edge trigger input based on different I^2C settings.

To set GPIO4 as the LDO1 EN pin, LDO1_EN_SET should be set to b110 and GPIO4_CONFIG needs to be set to b1000.

When GPIO4 is configured to be VSEL2 pin when GPIO3 isconfigured to be VSEL1 pin, both GPIO3 and GPIO4's High/Low states are read to determine the which voltage setting to be used for Buck.

If GPIO4 is set to be in forced open-drain high state, it is in a HIGH-Z state. If GPIO4 is set to be in forced low state, it is pulled down to GND. If GPIO4 is set to be in forced push-pull high state, it is pulled up to VPU.

If GPIO4 is set to operate as a sequencer output, it is pulled up to VPU or pulled down to GND at the corresponding time instances during power-up/power-down sequence.

If GPIO4 is configured to be in input mode, its current state is readable with the GPIO4_STAT bit. As a positive-edge/negative-edge trigger input, the GPIO4_FLAG will be set when a trigger event happens and a 128µs pulse is sent through the $\overline{INT}$ pin to notify the host.

If GPIO4_CONFIG is set to b1100/b1101/b1110/b1111, GPIO4 is operating as a open-drain PWM output which is pulled low for 20%/40%/60%/80% duty ratio at f_{GPIO4_PWM}.

7.4 Device Functional Modes

The device has three main modes of operation: battery mode, ship mode, and adapter mode. LDO1-ON Ship mode is a special type of Ship mode in which always-on LDO1 remains on.

7.4.1 Ship Mode

Ship mode is the lowest quiescent current state for the device with BATFET being turned off.

Ship mode can be initiated by writing b10 to the EN_RST_SHIP register bits. If the ship mode setting is set, the device will wait until the input source is removed to enter ship mode. When an I^2C command is given to set the device to enter ship mode, the device waits for 1 second before the implementation.

Ship mode can also be initiated with $\overline{MR}$ pulled low for t_{LPRESS} when PB_LPRESS_ACTION is writen to b10. 図 7-6 shows this behavior. The power-down sequence starts when $\overline{MR}$ pin is pulled low for t_{LPRESS}. The ship mode is entered after SYS pulldown with power-down sequence completion and $\overline{MR}$ pin is above the low threshold.

The device can exit ship mode by adapter insertion (V_{IN} > V_{IN_UVLOZ}) or $\overline{MR}$ pin is pulled low for $t_{SHIPWAKE}$ with V_{BAT}>V_{BUVLO}.For the device to reliably exit ship mode by adapter insertion, V_{IN} needs to be higher than V_{IN_UVLOZ} for at least 30ms.

7.4.1.1 LDO1-ON Ship Mode

If LDO1 is configured to be in always-on mode and LDO1_SHIP_AO is set to 1, LDO1-ON ship mode is enterted with ship mode entry condtions. To enter this mode, LDO1 remains enabled in power-down sequence during ship mode entry.

Exiting the LDO1-ON ship mode is the same as exiting the regular ship mode.

7.4.2 Battery Mode

When V_{BAT} rises above V_{BUVLOZ}, the device is powered on when adapter is not present and the device is in battery mode.With V_{BAT} > $V_{BATDEPLZ}$, the BATFET is turned on. The system is powered by the battery and BATFET is protected by the battery overcurrent protection (see セクション 7.3.8.4 for details).

In battery mode, if the battery voltage falls below $V_{BATDEPL}$, the BATFET is turned off. If V_{BAT} falls below V_{BUVLO}, the device is turned off with no adapter.

7.4.3 Adapter Mode

The device is in adapter mode with adapter being connected (V_{IN} > V_{IN_UVLO}). If the adater supply is valid (VIN_PGOOD) and above the V_{INDPM} level, the system is powered by the adapter and the charging can start if it is enabled and there is no fault that prevents charging.

7.5 Programming

7.5.1 Serial Interface

The device uses I^{2}C compatible interface for flexible charging parameter programming and instantaneous device status reporting. I^{2}C is a bi-directional 2-wire serial interface. Only two open-drain bus lines are required: a serial data line (SDA), and a serial clock line (SCL).

The device has 7-bit I^{2}C address 0x6C, receiving control inputs from a host device such as a micro-controller or digital signal processor through register addresses defined in the Register Map. The host device initiates all transfers and the charger responds. Register reads outside of these adresses return 0xFF. When the bus is free, both SDA and SCL lines are HIGH.

The I^{2}C interface supports standard mode (up to 100 kbits/s), fast mode (up to 400 kbits/s) and fast mode plus (up to 1 Mbits/s.) These lines are pulled up to a reference voltage via pull-up resistor. The device I^{2}C detection thresholds support a communication reference voltage between 1.2V - 5V.

- Standard mode (100 kbits/s):
  - No additional requirements
- Fast mode (400 kbits/s):
  - Increase I^{2}C t_{buf} to at least 80 µs
  - If using repeated start commands, ensure I^{2}C tsu:STA is at least 80 µs
- Fast mode plus (1 Mbits/s):
  - Increase I^{2}C t_{buf} to at least 120 µs
  - If using repeated start commands, ensure I^{2}C tsu:STA is at least 120 µs

7.5.1.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

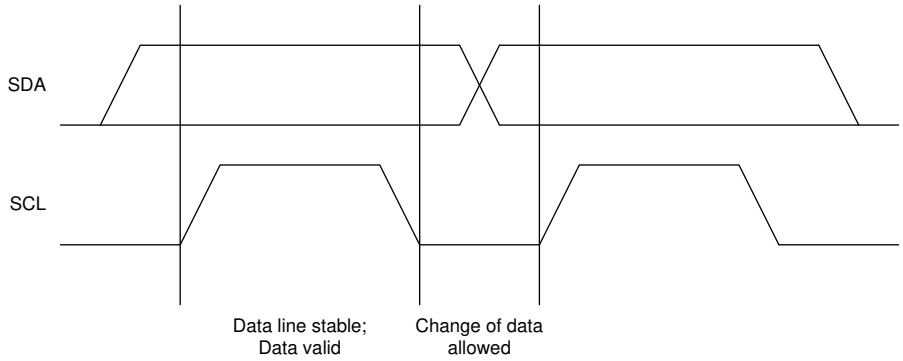


図 7-11. Bit Transfer on the I^{2}C Bus

7.5.1.2 START and STOP Conditions

All transactions begin with a START (S) and are terminated with a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the host. The bus is considered busy after the START condition, and free after the STOP condition.

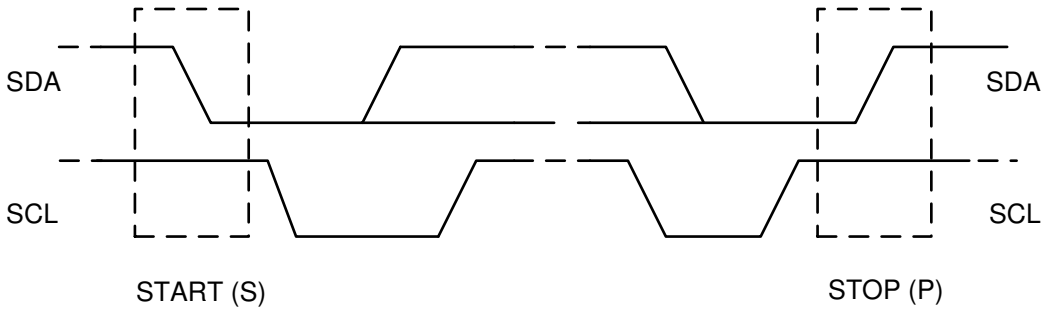


図 7-12. START and STOP Conditions on the I²C Bus

7.5.1.3 Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an ACKNOWLEDGE (ACK) bit. Data is transferred with the Most Significant Bit (MSB) first. If a target cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the SCL line low to force the host into a wait state (clock stretching). Data transfer then continues when the target is ready for another byte of data and releases the SCL line.

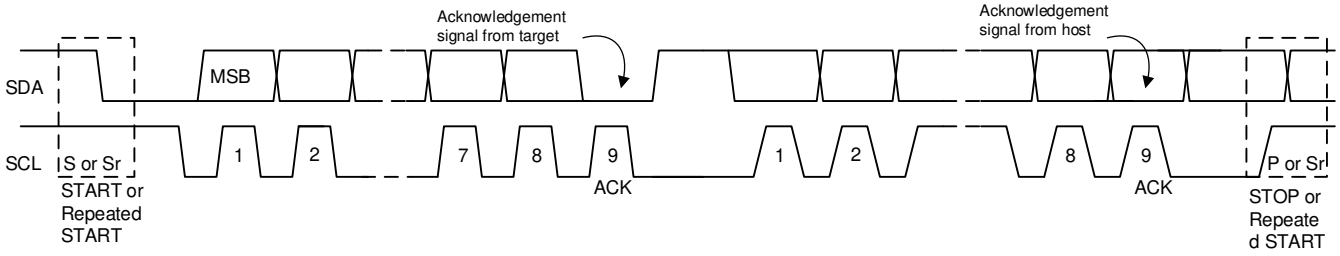


図 7-13. Data Transfer on the I²C Bus

7.5.1.4 Acknowledge (ACK) and Not Acknowledge (NACK)

The ACK signaling takes place after each transmitted byte. The ACK bit allows the host to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the host.

The transmitter releases the SDA line during the acknowledge clock pulse so the host can pull the SDA line LOW and it remains stable LOW during the HIGH period of this 9th clock pulse.

A NACK is signaled when the SDA line remains HIGH during the 9th clock pulse. The host can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

7.5.1.5 Target Address and Data Direction Bit

After the START signal, a target address is sent. This address is 7 bits long, followed by the 8 bit as a data direction bit (bit R/ $\overline{W}$). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ). The device 7-bit address is defined as 1101 100' (0x6C). The address bit arrangement is shown below.

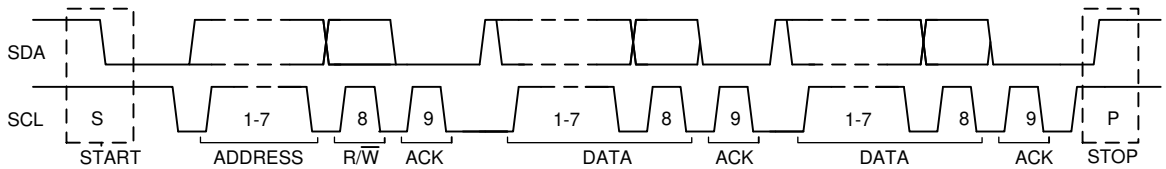


図 7-14. Complete Data Transfer on the I²C Bus

7.5.1.6 Single Write and Read

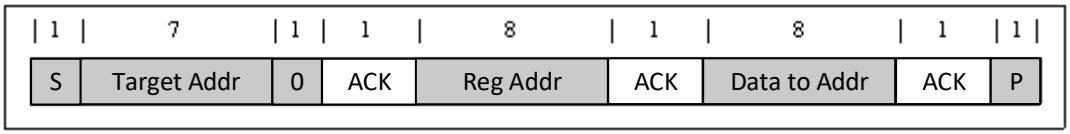


図 7-15. Single Write

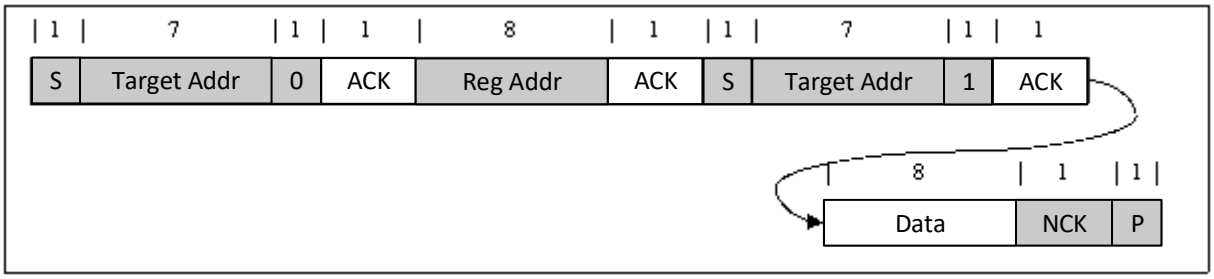


図 7-16. Single Read

If the register address is not defined, the charger IC sends back NACK and returns to the idle state.

7.5.1.7 Multi-Write and Multi-Read

The charger device supports multi-byte read and multi-byte write of all registers. These multi-byte operations are allowed to cross register boundaries. For instance, the entire register map may be read in a single operation with a 39-byte read that starts at register address 0x01.

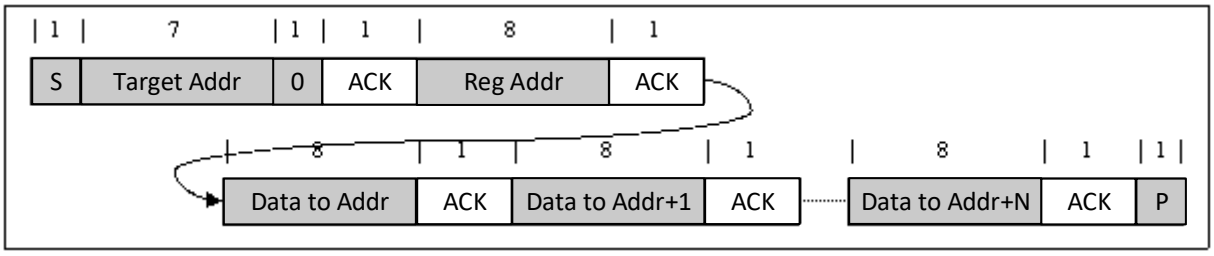


図 7-17. Multi-Write

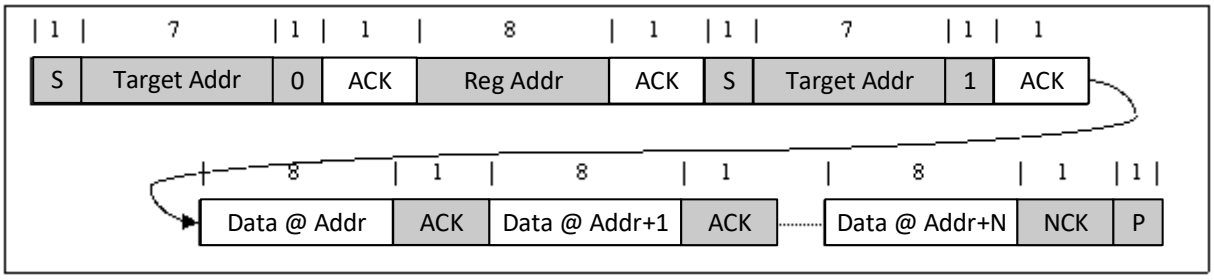


図 7-18. Multi-Read

7.6 Register Maps

7.6.1 BQ25190 Registers

表 7-9 lists the memory-mapped registers for the BQ25190 registers. All register offset addresses not listed in 表 7-9 should be considered as reserved locations and the register contents should not be modified.

表 7-9. BQ25190 Registers

Offset	Acronym	Register Name	Section
0h	REG0x00_STAT0	STAT0	セクション 7.6.1.1
1h	REG0x01_STAT1	STAT1	セクション 7.6.1.2
2h	REG0x02_STAT2	STAT2	セクション 7.6.1.3
3h	REG0x03_STAT3	STAT3	セクション 7.6.1.4
4h	REG0x04_FLAG0	FLAG0	セクション 7.6.1.5
5h	REG0x05_FLAG1	FLAG1	セクション 7.6.1.6
6h	REG0x06_FLAG2	FLAG2	セクション 7.6.1.7
7h	REG0x07_FLAG3	FLAG3	セクション 7.6.1.8
8h	REG0x08_MASK0	MASK0	セクション 7.6.1.9
9h	REG0x09_MASK1	MASK1	セクション 7.6.1.10
Ah	REG0x0A_MASK2	MASK2	セクション 7.6.1.11
Bh	REG0x0B_MASK3	MASK3	セクション 7.6.1.12
Ch	REG0x0C_VBAT	VBAT	セクション 7.6.1.13
Dh	REG0x0D_ICHG_CTRL	ICHG_CTRL	セクション 7.6.1.14
Eh	REG0x0E_CHARGECTRL0	CHARGECTRL0	セクション 7.6.1.15
Fh	REG0x0F_CHARGECTRL1	CHARGECTRL1	セクション 7.6.1.16
10h	REG0x10_IC_CTRL	IC_CTRL	セクション 7.6.1.17
11h	REG0x11_TMR_ILIM	TMR_ILIM	セクション 7.6.1.18
12h	REG0x12_SHIP_RST	SHIP_RST	セクション 7.6.1.19
13h	REG0x13_SYS_REG	SYS_REG	セクション 7.6.1.20
14h	REG0x14_TS_COLD	TS_COLD	セクション 7.6.1.21
15h	REG0x15_TS_COOL	TS_COOL	セクション 7.6.1.22
16h	REG0x16_TS_WARM	TS_WARM	セクション 7.6.1.23
17h	REG0x17_TS_HOT	TS_HOT	セクション 7.6.1.24
18h	REG0x18_ADCCTRL0	ADCCTRL0	セクション 7.6.1.25
19h	REG0x19_ADCCTRL1	ADCCTRL1	セクション 7.6.1.26
1Ah	REG0x1A_ADCCTRL2	ADCCTRL2	セクション 7.6.1.27
1Bh	REG0x1B_ADC_DATA_VBAT	ADC_DATA_VBAT	セクション 7.6.1.28
1Dh	REG0x1D_ADC_DATA_TS	ADC_DATA_TS	セクション 7.6.1.29
1Fh	REG0x1F_ADC_DATA_IBAT	ADC_DATA_IBAT	セクション 7.6.1.30
21h	REG0x21_ADC_DATA_ADCIN	ADC_DATA_ADCIN	セクション 7.6.1.31
23h	REG0x23_ADC_DATA_VIN	ADC_DATA_VIN	セクション 7.6.1.32
25h	REG0x25_ADC_DATA_VSYS	ADC_DATA_VSYS	セクション 7.6.1.33
27h	REG0x27_ADC_DATA_IIN	ADC_DATA_IIN	セクション 7.6.1.34
29h	REG0x29_ADC_DATA_TDIE	ADC_DATA_TDIE	セクション 7.6.1.35
2Bh	REG0x2B_ADCALARM_COMP1	ADCALARM_COMP1	セクション 7.6.1.36
2Dh	REG0x2D_ADCALARM_COMP2	ADCALARM_COMP2	セクション 7.6.1.37

表 7-9. BQ25190 Registers (続き)

Offset	Acronym	Register Name	Section
2Fh	REG0x2F_ADCALARM_COMP3	ADCALARM_COMP3	セクション 7.6.1.38
31h	REG0x31_ADC_CHANNEL_DISABLE	ADC_CHANNEL_DISABLE	セクション 7.6.1.39
32h	REG0x32_BUCK_VOUT	BUCK_VOUT	セクション 7.6.1.40
33h	REG0x33_BUCK_VOUT1	BUCK_VOUT1	セクション 7.6.1.41
34h	REG0x34_BUCK_VOUT2	BUCK_VOUT2	セクション 7.6.1.42
35h	REG0x35_BUCK_VOUT3	BUCK VOUT3	セクション 7.6.1.43
36h	REG0x36_BUCK_VOUT4	BUCK_VOUT4	セクション 7.6.1.44
37h	REG0x37_BUCK_CTRL0	BUCK_CTRL0	セクション 7.6.1.45
38h	REG0x38_BUCK_CTRL1	BUCK_CTRL1	セクション 7.6.1.46
39h	REG0x39_BUBO_CTRL0	BUBO_CTRL0	セクション 7.6.1.47
3Ah	REG0x3A_BUBO_CTRL1	BUBO_CTRL1	セクション 7.6.1.48
3Bh	REG0x3B_LDO1_CTRL0	LDO1_CTRL0	セクション 7.6.1.49
3Ch	REG0x3C_LDO1_CTRL1	LDO1_CTRL1	セクション 7.6.1.50
3Dh	REG0x3D_LDO2_CTRL0	LDO2_CTRL0	セクション 7.6.1.51
3Eh	REG0x3E_LDO2_CTRL1	LDO2_CTRL1	セクション 7.6.1.52
3Fh	REG0x3F_NTC_CTRL	NTC_CTRL	セクション 7.6.1.53
40h	REG0x40_GPIO1_CTRL	GPIO1_CTRL	セクション 7.6.1.54
41h	REG0x41_GPIO2_CTRL	GPIO2_CTRL	セクション 7.6.1.55
42h	REG0x42_GPIO3_CTRL	GPIO3_CTRL	セクション 7.6.1.56
43h	REG0x43_GPIO4_CTRL	GPIO4_CTRL	セクション 7.6.1.57
44h	REG0x44_PART_INFORMATION	PART_INFORMATION	セクション 7.6.1.58

Complex bit access types are encoded to fit into small table cells. 表 7-10 shows the codes that are used for access types in this section.

表 7-10. BQ25190 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.6.1.1 REG0x00_STAT0 Register (Offset = 0h) [Reset = XXh]

REG0x00_STAT0 is shown in 図 7-19 and described in 表 7-11.

Return to the Summary Table.

Charger Status 0

図 7-19. REG0x00_STAT0 Register

7	6	5	4	3	2	1	0
TS_OPEN_STAT	TS_STAT			RESERVED	ILIM_ACTIVE_STAT	VDPPM_ACTIVE_STAT	VINDPM_ACTIVE_STAT

図 7-19. REG0x00_STAT0 Register (続き)

R-Xh	R-Xh	R-0h	R-Xh	R-Xh	R-Xh

表 7-11. REG0x00_STAT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	TS_OPEN_STAT	R	X	TS Open Status (Clamp is active) 0b = TS is not Open 1b = TS is Open
6-4	TS_STAT	R	X	TS Status 000b = TS_NORMAL (VWARM < VTS < VCOOL) 001b = TS_COLD (VTS > VCOLD) 010b = TS_HOT (VTS < VHOT) 011b = TS_COOL (VCOOL < VTS < VCOLD) 100b = TS_WARM (VHOT < VTS < VWARM) 101b = Reserved 110b = Reserved 111b = Reserved
3	RESERVED	R	X	Reserved
2	ILIM_ACTIVE_STAT	R	X	Input Curent Limit Active 0b = Not Active 1b = Active
1	VDPPM_ACTIVE_STAT	R	X	VDPPM Mode Active 0b = Not Active 1b = Active
0	VINDPM_ACTIVE_STAT	R	X	VINDPM Mode Active 0b = Not Active 1b = Active

7.6.1.2 REG0x01_STAT1 Register (Offset = 1h) [Reset = XXh]

REG0x01_STAT1 is shown in 図 7-20 and described in 表 7-12.

Return to the Summary Table.

Charger Status 1

図 7-20. REG0x01_STAT1 Register

7	6	5	4	3	2	1	0
THERMREG_ACTIVE_STAT	RESERVED			ADC_DONE_STAT	COMP1_ALARM_STAT	COMP2_ALARM_STAT	COMP3_ALARM_STAT
R-Xh	R-0h			R-Xh	R-Xh	R-Xh	R-Xh

表 7-12. REG0x01_STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	THERMREG_ACTIVE_STAT	R	X	Thermal Regulation Active 0b = Not Active 1b = Active
6-4	RESERVED	R	X	Reserved
3	ADC_DONE_STAT	R	X	ADC Conversion Status (in one-shot mode only) Note: Always reads 0 in continous mode 0b = Conversion not complete 1b = Conversion complete

表 7-12. REG0x01_STAT1 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
2	COMP1_ALARM_STAT	R	X	COMP1 Status 0b = Selected ADC measreument does not meet condition set by 1_ADCALARM_ABOVE bit 1b = Selected ADC measurement meets condition set by 1_ADCALARM_ABOVE bit
1	COMP2_ALARM_STAT	R	X	COMP2 Status 0b = Selected ADC measreument does not meet condition set by 2_ADCALARM_ABOVE bit 1b = Selected ADC measurement meets condition set by 2_ADCALARM_ABOVE bit
0	COMP3_ALARM_STAT	R	X	COMP3 Status 0b = Selected ADC measreument does not meet condition set by 3_ADCALARM_ABOVE bit 1b = Selected ADC measurement meets condition set by 3_ADCALARM_ABOVE bit

7.6.1.3 REG0x02_STAT2 Register (Offset = 2h) [Reset = XXh]

REG0x02_STAT2 is shown in 図 7-21 and described in 表 7-13.

Return to the Summary Table.

Charger Status 2

図 7-21. REG0x02_STAT2 Register

7	6	5	4	3	2	1	0
CHG_STAT		SEQUENCE_PG_STAT	RESERVED			VIN_PGOOD_STAT	VIN_OVP_STAT
R-Xh		R-Xh	R-0h			R-Xh	R-Xh

表 7-13. REG0x02_STAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	CHG_STAT	R	X	Charging Status Indicator 00b = When charging is enabled but device is not charging 01b = When charger is in constant current charging (Trickle Charge, Precharge or Fast charge) 10b = When charger is in constant voltage operation 11b = When charging is done or disabled by the host
5	SEQUENCE_PG_STAT	R	X	Sequence Power Good 0b = Sequence Power Not Good 1b = Sequence Power Good
4-2	RESERVED	R	0h	Reserved
1	VIN_PGOOD_STAT	R	X	VIN Power Good 0b = VIN Power Not Good 1b = VIN Power Good
0	VIN_OVP_STAT	R	X	VIN OVP Fault 0b = Not Active 1b = Active

7.6.1.4 REG0x03_STAT3 Register (Offset = 3h) [Reset = XXh]

REG0x03_STAT3 is shown in 図 7-22 and described in 表 7-14.

Return to the Summary Table.

Charger Status 3

図 7-22. REG0x03_STAT3 Register

7	6	5	4	3	2	1	0
GPIO1_STAT	GPIO2_STAT	GPIO3_STAT	GPIO4_STAT	RESERVED		BATDEPL_FAULT_STAT	TSHUT_STAT
R-Xh	R-Xh	R-Xh	R-Xh	R-0h		R-Xh	R-Xh

表 7-14. REG0x03_STAT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO1_STAT	R	X	GPIO1 Status 0b = GPIO1 is low 1b = GPIO1 is high in input modes
6	GPIO2_STAT	R	X	GPIO2 Status 0b = GPIO2 is low 1b = GPIO2 is high in input modes
5	GPIO3_STAT	R	X	GPIO3 Status 0b = GPIO3 is low 1b = GPIO3 is high in input modes
4	GPIO4_STAT	R	X	GPIO4 Status 0b = GPIO1 is low 1b = GPIO4 is high in input modes
3-2	RESERVED	R	0h	Reserved
1	BATDEPL_FAULT_STAT	R	X	BATDEPL 0b = Not Active 1b = Active
0	TSHUT_STAT	R	X	Thermal Shutdown 0b = Not Active 1b = Active

7.6.1.5 REG0x04_FLAG0 Register (Offset = 4h) [Reset = 00h]

REG0x04_FLAG0 is shown in 図 7-23 and described in 表 7-15.

Return to the Summary Table.

Flags 0

図 7-23. REG0x04_FLAG0 Register

7	6	5	4	3	2	1	0
TS_OPEN_FLAG	TS_FLAG	RESERVED			ILIM_ACTIVE_FLAG	VDPPM_ACTIVE_FLAG	VINDPM_ACTIVE_FLAG
R-0h	R-0h	R-0h			R-0h	R-0h	R-0h

表 7-15. REG0x04_FLAG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	TS_OPEN_FLAG	R	0h	TS Open Flag Access: R (ClearOnRead) 0b = No TS Open fault detected 1b = TS Open fault detected
6	TS_FLAG	R	0h	TS status Flag Access: R (ClearOnRead) 0b = No change to TS status (TS_STAT) was detected 1b = A change to TS status (TS_STAT) was detected
5-3	RESERVED	R	0h	Reserved
2	ILIM_ACTIVE_FLAG	R	0h	ILIM Active Access: R (ClearOnRead) 0b = ILIM not detected 1b = ILIM detected
1	VDPPM_ACTIVE_FLAG	R	0h	VDPPM Flag Access: R (ClearOnRead) 0b = VDPPM regulation not detected 1b = VDPPM regulation detected
0	VINDPM_ACTIVE_FLAG	R	0h	VINDPM Flag Access: R (ClearOnRead) 0b = VINDPM regulation not detected 1b = VINDPM regulation detected

7.6.1.6 REG0x05_FLAG1 Register (Offset = 5h) [Reset = 00h]

REG0x05_FLAG1 is shown in 図 7-24 and described in 表 7-16.

Return to the Summary Table.

Flags 1

図 7-24. REG0x05_FLAG1 Register

7	6	5	4	3	2	1	0
THERMREG_ACTIVE_FLAG	SAFETY_TMR_FAULT_FLAG	WAKE1_FLAG	WAKE2_FLAG	ADC_DONE_FLAG	COMP1_ALARM_FLAG	COMP2_ALARM_FLAG	COMP3_ALARM_FLAG
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

表 7-16. REG0x05_FLAG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	THERMREG_ACTIVE_FLAG	R	0h	Thermal regulation Flag Access: R (ClearOnRead) 0b = No thermal regulation detected 1b = Thermal regulation has occurred
6	SAFETY_TMR_FAULT_FLAG	R	0h	Safety Timer Expired Flag Access: R (ClearOnRead) 0b = Not Active 1b = Active
5	WAKE1_FLAG	R	0h	Wake 1 Timer Flag Access: R (ClearOnRead) 0b = Does not meet Wake 1 Condition 1b = Met Wake 1 Condition

表 7-16. REG0x05_FLAG1 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
4	WAKE2_FLAG	R	0h	Wake 2 Timer Flag Access: R (ClearOnRead) 0b = Does not meet Wake 2 Condition 1b = Met Wake 2 Condition
3	ADC_DONE_FLAG	R	0h	ADC Conversion Flag (only in one-shot mode) Access: R (ClearOnRead) 0b = Conversion not completed 1b = Conversion completed
2	COMP1_ALARM_FLAG	R	0h	ADC COMP1 Threshold Flag Access: R (ClearOnRead) 0b = No threshold crossing detected 1b = Selected ADC measurement crossed condition set by 1_ADCALARM_ABOVE bit
1	COMP2_ALARM_FLAG	R	0h	ADC COMP2 Threshold Flag Access: R (ClearOnRead) 0b = No threshold crossing detected 1b = Selected ADC measurement crossed condition set by 2_ADCALARM_ABOVE bit
0	COMP3_ALARM_FLAG	R	0h	ADC COMP3 Threshold Flag Access: R (ClearOnRead) 0b = No threshold crossing detected 1b = Selected ADC measurement crossed condition set by 3_ADCALARM_ABOVE bit

7.6.1.7 REG0x06_FLAG2 Register (Offset = 6h) [Reset = 00h]

REG0x06_FLAG2 is shown in 図 7-25 and described in 表 7-17.

Return to the Summary Table.

Flags 2

図 7-25. REG0x06_FLAG2 Register

7	6	5	4	3	2	1	0
CHG_FLAG	SEQUENCE_PG_FLAG	BUCK_PG_FLAG	BUBO_PG_FLAG	LDO1_PG_FLAG	LDO2_PG_FLAG	VIN_PGOOD_FLAG	VIN_OVP_FAULT_FLAG
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

表 7-17. REG0x06_FLAG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CHG_FLAG	R	0h	Charge Status Flag Access: R (ClearOnRead) 0b = No change in charge status 1b = Charge status changed
6	SEQUENCE_PG_FLAG	R	0h	Sequence Power Good Flag Access: R (ClearOnRead) 0b = No change in sequence power good status detected 1b = Change in sequence power good status detected
5	BUCK_PG_FLAG	R	0h	Buck Power Good Flag Access: R (ClearOnRead) 0b = Buck power not good event not detected 1b = Buck power not good event detected

表 7-17. REG0x06_FLAG2 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
4	BUBO_PG_FLAG	R	0h	Buck-boost Power Good Flag Access: R (ClearOnRead) 0b = Buck-boost power not good event not detected 1b = Buck-boost power not good event detected
3	LDO1_PG_FLAG	R	0h	LDO1 Power Good Flag Access: R (ClearOnRead) 0b = LDO1 power not good event not detected 1b = LDO1 power not good event detected
2	LDO2_PG_FLAG	R	0h	LDO2 Power Good Flag Access: R (ClearOnRead) 0b = LDO2 power not good event not detected 1b = LDO2 power not good event detected
1	VIN_PGOOD_FLAG	R	0h	VIN Power Good Flag Access: R (ClearOnRead) 0b = No change in VIN power good status 1b = Change in VIN power good status detected.
0	VIN_OVP_FAULT_FLAG	R	0h	VIN_OVP Flag Access: R (ClearOnRead) 0b = VIN_OVP fault not detected 1b = VIN_OVP fault detected

7.6.1.8 REG0x07_FLAG3 Register (Offset = 7h) [Reset = 00h]

REG0x07_FLAG3 is shown in 図 7-26 and described in 表 7-18.

Return to the Summary Table.

Flags 3

図 7-26. REG0x07_FLAG3 Register

7	6	5	4	3	2	1	0
GPIO1_FLAG	GPIO2_FLAG	GPIO3_FLAG	GPIO4_FLAG	SYS_SHORT_FAULT_FLAG	BATDEPL_FAULT_FLAG	BAT_OCP_FAULT_FLAG	TSHUT_FLAG
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

表 7-18. REG0x07_FLAG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO1_FLAG	R	0h	GPIO1 Flag 0b = GPIO1 interrupt not triggered 1b = GPIO1 interrupt triggered
6	GPIO2_FLAG	R	0h	GPIO2 Flag Access: R (ClearOnRead) 0b = GPIO2 interrupt not triggered 1b = GPIO2 interrupt triggered
5	GPIO3_FLAG	R	0h	GPIO3 Flag Access: R (ClearOnRead) 0b = GPIO3 interrupt not triggered 1b = GPIO3 interrupt triggered
4	GPIO4_FLAG	R	0h	GPIO4 Flag Access: R (ClearOnRead) 0b = GPIO4 interrupt not triggered 1b = GPIO4 interrupt triggered

表 7-18. REG0x07_FLAG3 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
3	SYS_SHORT_FAULT_FLAG	R	0h	SYS Short Fault Access: R (ClearOnRead) 0b = SYS short fault not detected 1b = SYS short fault detected
2	BATDEPL_FAULT_FLAG	R	0h	Battery depletion Flag Access: R (ClearOnRead) 0b = Battery depletion fault not detected 1b = Battery depletion fault detected
1	BAT_OCP_FAULT_FLAG	R	0h	Battery overcurrent protection Access: R (ClearOnRead) 0b = Battery overcurrent condition not detected 1b = Battery overcurrent condition detected
0	TSHUT_FLAG	R	0h	TSHUT Flag Access: R (ClearOnRead) 0b = TSHUT not detected 1b = TSHUT detected

7.6.1.9 REG0x08_MASK0 Register (Offset = 8h) [Reset = 84h]

REG0x08_MASK0 is shown in 図 7-27 and described in 表 7-19.

Return to the Summary Table.

Interrupt Masks 0

図 7-27. REG0x08_MASK0 Register

7	6	5	4	3	2	1	0
TS_OPEN_MASK	TS_MASK	RESERVED			ILIM_ACTIVE_MASK	VDPPM_ACTIVE_MASK	VINDPM_ACTIVE_MASK
R/W-1h	R/W-0h	R-0h			R/W-1h	R/W-0h	R/W-0h

表 7-19. REG0x08_MASK0 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	TS_OPEN_MASK	R/W	1h	Reset by: REG_RESET	Mask for TS_OPEN interrupt 0b = Interrupt Not Masked 1b = Interrupt Masked
6	TS_MASK	R/W	0h	Reset by: REG_RESET	Mask for TS interrupt 0b = Interrupt Not Masked 1b = Interrupt Masked
5-3	RESERVED	R	0h		Reserved
2	ILIM_ACTIVE_MASK	R/W	1h	Reset by: REG_RESET	Mask for TS_IINLIM_ACTIVEinterrupt 0b = Interrupt Not Masked 1b = Interrupt Masked
1	VDPPM_ACTIVE_MASK	R/W	0h	Reset by: REG_RESET	Mask for VINDPM_ACTIVE interrupt 0b = Interrupt Not Masked 1b = Interrupt Masked
0	VINDPM_ACTIVE_MASK	R/W	0h	Reset by: REG_RESET	Mask for VDPPM_ACTIVE interrupt 0b = Interrupt Not Masked 1b = Interrupt Masked

7.6.1.10 REG0x09_MASK1 Register (Offset = 9h) [Reset = 07h]

REG0x09_MASK1 is shown in 図 7-28 and described in 表 7-20.

Return to the Summary Table.

Interrupt Masks 1

図 7-28. REG0x09_MASK1 Register

7	6	5	4	3	2	1	0
TREG_INT_MASK	SAFETY_TMR_FAULT_MASK	WAKE1_MASK	WAKE2_MASK	ADC_DONE_MASK	COMP1_ALARM_MASK	COMP2_ALARM_MASK	COMP3_ALARM_MASK
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-1h	R/W-1h

表 7-20. REG0x09_MASK1 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	TREG_INT_MASK	R/W	0h	Reset by: REG_RESET	Mask for THERMREG_ACTIVE interrupt 0b = Interrupt Not Masked 1b = Interrupt Masked
6	SAFETY_TMR_FAULT_MASK	R/W	0h	Reset by: REG_RESET	Mask for SAFETY_TIMER_FAULT interrupt 0b = Interrupt Not Masked 1b = Interrupt Masked
5	WAKE1_MASK	R/W	0h	Reset by: REG_RESET	Mask for Wake 1 timer interrupt 0b = Interrupt Not Masked 1b = Interrupt Masked
4	WAKE2_MASK	R/W	0h	Reset by: REG_RESET	Mask for Wake 2 timer interrupt 0b = Interrupt Not Masked 1b = Interrupt Masked
3	ADC_DONE_MASK	R/W	0h	Reset by: REG_RESET	Mask for ADC_DONE interrupt (only in one-shot mode) 0b = Interrupt Not Masked 1b = Interrupt Masked
2	COMP1_ALARM_MASK	R/W	1h	Reset by: REG_RESET	Mask for COMP1_ALARM interrupt 0b = Interrupt Not Masked 1b = Interrupt Masked
1	COMP2_ALARM_MASK	R/W	1h	Reset by: REG_RESET	Mask for COMP2_ALARM interrupt 0b = Interrupt Not Masked 1b = Interrupt Masked
0	COMP3_ALARM_MASK	R/W	1h	Reset by: REG_RESET	Mask for COMP3_ALARM interrupt 0b = Interrupt Not Masked 1b = Interrupt Masked

7.6.1.11 REG0x0A_MASK2 Register (Offset = Ah) [Reset = C0h]

REG0x0A_MASK2 is shown in 図 7-29 and described in 表 7-21.

Return to the Summary Table.

Interrupt Masks 2

図 7-29. REG0x0A_MASK2 Register

7	6	5	4	3	2	1	0
CHG_STATUS_INT_MASK	SEQUENCE_PG_MASK	BUCK_PG_MASK	BUBO_PG_MASK	LDO1_PG_MASK	LDO2_PG_MASK	VIN_PGOOD_MASK	VIN_OVP_FAULT_MASK
R/W-1h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

図 7-29. REG0x0A_MASK2 Register (続き)

表 7-21. REG0x0A_MASK2 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	CHG_STATUS_INT_MASK	R/W	1h	Reset by: REG_RESET	Mask Charging Status Interrupt 0b = Enable Charging Status Interrupt anytime there is a charging status change. (this is disabled by default as when the battery is not present, the device will switch between CC and CV which can drive the MCU to keep servicing it's ISR) 1b = Mask Charging Status Interrupt
6	SEQUENCE_PG_MASK	R/W	1h	Reset by: REG_RESET	Mask for sequence power good status change interrupt 0b = Interrupt Not Masked 1b = Interrupt Masked
5	BUCK_PG_MASK	R/W	0h	Reset by: REG_RESET	Mask for BUCK_PG interrupt 0b = Interrupt Not Masked 1b = Interrupt Masked
4	BUBO_PG_MASK	R/W	0h	Reset by: REG_RESET	Mask for BUBO_PG interrupt 0b = Interrupt Not Masked 1b = Interrupt Masked
3	LDO1_PG_MASK	R/W	0h	Reset by: REG_RESET	Mask for LDO1_PG interrupt 0b = Interrupt Not Masked 1b = Interrupt Masked
2	LDO2_PG_MASK	R/W	0h	Reset by: REG_RESET	Mask for LDO2_PG interrupt 0b = Interrupt Not Masked 1b = Interrupt Masked
1	VIN_PGOOD_MASK	R/W	0h	Reset by: REG_RESET	Mask for VIN_PGOOD interrupt 0b = Interrupt Not Masked 1b = Interrupt Masked
0	VIN_OVP_FAULT_MASK	R/W	0h	Reset by: REG_RESET	Mask for VIN_OVP interrupt 0b = Interrupt Not Masked 1b = Interrupt Masked

7.6.1.12 REG0x0B_MASK3 Register (Offset = Bh) [Reset = 00h]

REG0x0B_MASK3 is shown in 図 7-30 and described in 表 7-22.

Return to the Summary Table.

Interrupt Masks 3

図 7-30. REG0x0B_MASK3 Register

7	6	5	4	3	2	1	0
RESERVED				SYS_SHORT_FAULT_MASK	BAT_OCP_FAULT_MASK	BATDEPL_FAULT_MASK	TSHUT_MASK
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

表 7-22. REG0x0B_MASK3 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7-4	RESERVED	R	0h		Reserved

表 7-22. REG0x0B_MASK3 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Notes	Description
3	SYS_SHORT_FAULT_MASK	R/W	0h	Reset by: REG_RESET	Mask for SYS_SHORT_FAULT interrupt 0b = Interrupt Not Masked 1b = Interrupt Masked
2	BAT_OCP_FAULT_MASK	R/W	0h	Reset by: REG_RESET	Mask for BAT_OCP_FAULT interrupt 0b = Interrupt Not Masked 1b = Interrupt Masked
1	BATDEPL_FAULT_MASK	R/W	0h	Reset by: REG_RESET	Mask for BATDEPL_FAULT interrupt 0b = Interrupt Not Masked 1b = Interrupt Masked
0	TSHUT_MASK	R/W	0h	Reset by: REG_RESET	Mask for TSHUT interrupt 0b = Interrupt Not Masked 1b = Interrupt Masked

7.6.1.13 REG0x0C_VBAT Register (Offset = Ch) [Reset = 46h]

REG0x0C_VBAT is shown in 図 7-31 and described in 表 7-23.

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Battery Voltage and Fast Charge Current Control

図 7-31. REG0x0C_VBAT Register

7	6	5	4	3	2	1	0
RESERVED	VBATREG						
R-0h	R/W-46h						

表 7-23. REG0x0C_VBAT Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	RESERVED	R	0h		Reserved
6-0	VBATREG	R/W	46h	Reset by: REG_RESET	Battery Regulation Voltage POR: 4200mV (46h) Range: 3500mV-4650mV (0h-73h) Clamped High Bit Step: 10mV Offset: 3500mV

7.6.1.14 REG0x0D_ICHG_CTRL Register (Offset = Dh) [Reset = 05h]

REG0x0D_ICHG_CTRL is shown in 図 7-32 and described in 表 7-24.

Return to the Summary Table.

Fast Charge Current Control

図 7-32. REG0x0D_ICHG_CTRL Register

7	6	5	4	3	2	1	0
CHG_DIS	ICHG						
R/W-0h	R/W-5h						

表 7-24. REG0x0D_ICHG_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	CHG_DIS	R/W	0h	Reset by: REG_RESET WATCHDOG	Charge Disable 0b = Battery Charging Enabled 1b = Battery Charging Disabled
6-0	ICHG	R/W	5h	Reset by: REG_RESET WATCHDOG	For ICHG <= 35mA ICHG = ICHGCODE +5mA For ICHG > 35mA ICHG = 40+(ICHGCODE-31) x 10 mA

7.6.1.15 REG0x0E_CHARGECTRL0 Register (Offset = Eh) [Reset = 70h]

REG0x0E_CHARGECTRL0 is shown in 図 7-33 and described in 表 7-25.

Return to the Summary Table.

Charger Control 0

図 7-33. REG0x0E_CHARGECTRL0 Register

7	6	5	4	3	2	1	0
VDPPM_DIS	IPRECHG	ITERM		VINDPM		THERM_REG	
R/W-0h	R/W-1h	R/W-3h		R/W-0h		R/W-0h	

表 7-25. REG0x0E_CHARGECTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	VDPPM_DIS	R/W	0h	Reset by: REG_RESET	Disable Vin DPPM 0b = enable DPPM 1b = diable DPPM
6	IPRECHG	R/W	1h	Reset by: REG_RESET	Precharge current = x times of term 0b = Precharge is 2 x Term 1b = Precharge is Term
5-4	ITERM	R/W	3h	Reset by: REG_RESET WATCHDOG	Termination current = % of Icharge 00b = Disable 01b = 5% of ICHG 10b = 10% of ICHG 11b = 20% of ICHG
3-2	VINDPM	R/W	0h	Reset by: REG_RESET	VINDPM Level Selection 00b = 4.2V 01b = 4.5V 10b = 4.7V 11b = Disabled
1-0	THERM_REG	R/W	0h	Reset by: REG_RESET	Thermal Regulation Threshold 00b = 100degC 01b = 80degC 10b = 60degC 11b = Disabled

7.6.1.16 REG0x0F_CHARGECTRL1 Register (Offset = Fh) [Reset = 45h]

REG0x0F_CHARGECTRL1 is shown in 図 7-34 and described in 表 7-26.

Return to the Summary Table.

Charger Control 1

図 7-34. REG0x0F_CHARGECTRL1 Register

7	6	5	4	3	2	1	0
IBAT_OCP_ILIM		BATDEPL			IBATSC	SEQUENCE_DELAY_TIME	
R/W-1h		R/W-0h			R/W-1h	R/W-1h	

表 7-26. REG0x0F_CHARGECTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7-6	IBAT_OCP_ILIM	R/W	1h	Reset by: REG_RESET	Battery Discharge Current Limit 00b = 500mA 01b = 1000mA 10b = 1500mA 11b = 3250mA
5-3	BATDEPL	R/W	0h	Reset by: REG_RESET	Battery Depletion Threshold Falling (150mV Hyst). 000b = 3.0V 001b = 2.8V 010b = 2.7V 011b = 2.5V 100b = 2.4V 101b = 2.3V 110b = 2.2V 111b = 2.1V
2	IBATSC	R/W	1h	Reset by: REG_RESET	Set battery short trickle charging current 0b = 8mA 1b = 1mA
1-0	SEQUENCE_DELAY_TIME	R/W	1h	Reset by: REG_RESET	Delay Time In Sequence 00b = 1ms 01b = 4ms 10b = 16ms 11b = 64ms

7.6.1.17 REG0x10_IC_CTRL Register (Offset = 10h) [Reset = 10h]

REG0x10_IC_CTRL is shown in 図 7-35 and described in 表 7-27.

Return to the Summary Table.

IC Control

図 7-35. REG0x10_IC_CTRL Register

7	6	5	4	3	2	1	0
RESERVED	VLOWV_SEL	VRECHG	TMR2X_EN	SAFETY_TIMER		WATCHDOG_SEL	
R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	

表 7-27. REG0x10_IC_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	RESERVED	R	0h		Reserved
6	VLOWV_SEL	R/W	0h		Precharge Voltage Threshold (VLOWV) 0b = 3V(default) 1b = 2.8V
5	VRECHG	R/W	0h	Reset by: REG_RESET	Recharge Voltage Threshold 0b = 100mV 1b = 200mV

表 7-27. REG0x10_IC_CTRL Register Field Descriptions (続き)

Bit	Field	Type	Reset	Notes	Description
4	TMR2X_EN	R/W	1h	Reset by: REG_RESET	Timer Slow 0b = The timer is not slowed at any time 1b = The timer is slowed by 2x when in any control other than CC or CV
3-2	SAFETY_TIMER	R/W	0h	Reset by: REG_RESET WATCHDOG	Fast Charge Timer 00b = 3 hour fast charge 01b = 6 hour fast charge 10b = 12 hour fast charge 11b = Disabled Safety timer
1-0	WATCHDOG_SEL	R/W	0h	Reset by: REG_RESET	Watchdog Selection 00b = 160s software reset 01b = 160s HW_RESET 10b = 40s HW_RESET 11b = Disabled watchdog function

7.6.1.18 REG0x11_TMR_ILIM Register (Offset = 11h) [Reset = 55h]

REG0x11_TMR_ILIM is shown in 図 7-36 and described in 表 7-28.

Return to the Summary Table.

Timer and Input Current Limit Control

図 7-36. REG0x11_TMR_ILIM Register

7	6	5	4	3	2	1	0
MR_LPRESS		HOST_HW_RESET_VIN_REQ	AUTOWAKE		ILIM		
R/W-1h		R/W-0h	R/W-2h		R/W-5h		

表 7-28. REG0x11_TMR_ILIM Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7-6	MR_LPRESS	R/W	1h	Reset by: REG_RESET	Push button Long Press duration timer 00b = 5s 01b = 10s 10b = 15s 11b = 20s
5	HOST_HW_RESET_VIN_REQ	R/W	0h		Host Initiated Hardware Reset VIN_UVLO Requirement 0b = Host initiated hardware reset not requiring VIN > VIN_UVLO 1b = Host initiated hardware reset requiring VIN > VIN_UVLO
4-3	AUTOWAKE	R/W	2h	Reset by: REG_RESET	Auto Wake UP Timer Restart 00b = 0.5s 01b = 1s 10b = 2s 11b = 4s

表 7-28. REG0x11_TMR_ILIM Register Field Descriptions (続き)

Bit	Field	Type	Reset	Notes	Description
2-0	ILIM	R/W	5h	Reset by: REG_RESET	Input Current Limit Setting 000b = 25mA 001b = 50mA 010b = 90mA 011b = 200mA 100b = 300mA 101b = 475mA 110b = 665mA 111b = 1050mA

7.6.1.19 REG0x12_SHIP_RST Register (Offset = 12h) [Reset = 0Ah]

REG0x12_SHIP_RST is shown in 図 7-37 and described in 表 7-29.

Return to the Summary Table.

Shipmode, Reset and Pushbutton Control

図 7-37. REG0x12_SHIP_RST Register

7	6	5	4	3	2	1	0
REG_RST	EN_RST_SHIP		PB_LPRESS_ACTION		WAKE1_TMR	WAKE2_TMR	RESERVED
R/W-0h	R/W-0h		R/W-1h		R/W-0h	R/W-1h	R-0h

表 7-29. REG0x12_SHIP_RST Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	REG_RST	R/W	0h		Software Reset 0b = Do nothing 1b = Software Reset
6-5	EN_RST_SHIP	R/W	0h	Reset by: REG_RESET	Ship Mode Enable and Hardware Reset 00b = Do nothing 01b = Hardware reset 10b = Enable ship mode 11b = Reserved
4-3	PB_LPRESS_ACTION	R/W	1h	Reset by: REG_RESET	Pushbutton Long Press Action (taken when /MR is pressed for tLPRESS) 00b = Do nothing 01b = Hardware reset 10b = Enable ship mode 11b = Reserved
2	WAKE1_TMR	R/W	0h	Reset by: REG_RESET	Wake 1 Timer Set 0b = 125ms 1b = 500ms
1	WAKE2_TMR	R/W	1h	Reset by: REG_RESET	Wake 2 Timer Set 0b = 1s 1b = 2s
0	RESERVED	R	0h		Reserved

7.6.1.20 REG0x13_SYS_REG Register (Offset = 13h) [Reset = 44h]

REG0x13_SYS_REG is shown in 図 7-38 and described in 表 7-30.

Return to the Summary Table.

SYS Regulation Voltage Control

図 7-38. REG0x13_SYS_REG Register

7	6	5	4	3	2	1	0
SYS_REG_CTRL			WATCHDOG_15S_ENABLE	RESERVED	VIN_OVP	SYS_MODE	
R/W-2h			R/W-0h	R-0h	R/W-1h	R/W-0h	

表 7-30. REG0x13_SYS_REG Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7-5	SYS_REG_CTRL	R/W	2h	Reset by: REG_RESET	SYS Regulation Voltgage 000b = VBAT + 225mV 001b = 4.4V 010b = 4.5V 011b = 4.6V 100b = 4.7V 101b = 4.8V 110b = 4.9V 111b = Pass Through
4	WATCHDOG_15S_ENABLE	R/W	0h	Reset by: REG_RESET	I2C Watchdog 0b = Mode Disabled 1b = Do a HW reset after 15s if no I2C transaction after VIN plugged
3	RESERVED	R	0h		Reserved
2	VIN_OVP	R/W	1h	Reset by: REG_RESET	Sets VIN Overvoltage Protection Threshold 0b = 5.7V 1b = 18.5V
1-0	SYS_MODE	R/W	0h	Reset by: REG_RESET WATCHDOG	Sets System Power Mode 00b = SYS powered from VIN if present or VBAT 01b = SYS powered from VBAT only, even if VIN present 10b = SYS disconnected and left floating 11b = SYS disconnected with pulldown

7.6.1.21 REG0x14_TS_COLD Register (Offset = 14h) [Reset = 91h]

REG0x14_TS_COLD is shown in 図 7-39 and described in 表 7-31.

Return to the Summary Table.

TS_COLD Threshold

図 7-39. REG0x14_TS_COLD Register

7	6	5	4	3	2	1	0
TS_COLD							
R/W-91h							

表 7-31. REG0x14_TS_COLD Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7-0	TS_COLD	R/W	91h	Reset by: REG_RESET	TS Cold Threshold POR: 580mV (91h) Range: 0mV-1020mV (0h-FFh) Bit Step: 4mV

7.6.1.22 REG0x15_TS_COOL Register (Offset = 15h) [Reset = 00h]

REG0x15_TS_COOL is shown in 図 7-40 and described in 表 7-32.

Return to the Summary Table.

TS_COOL Threshold

図 7-40. REG0x15_TS_COOL Register

7	6	5	4	3	2	1	0
TS_COOL							
R/W-0h							

表 7-32. REG0x15_TS_COOL Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7-0	TS_COOL	R/W	0h	Setting of 0 is disable TS_COOL threshold. Lower limit is really 4mV. Reset by: REG_RESET	TS Cool Threshold POR: 0mV (0h) Range: 0mV-1020mV (0h-FFh) Bit Step: 4mV

7.6.1.23 REG0x16_TS_WARM Register (Offset = 16h) [Reset = 00h]

REG0x16_TS_WARM is shown in 図 7-41 and described in 表 7-33.

Return to the Summary Table.

TS_WARM Threshold

図 7-41. REG0x16_TS_WARM Register

7	6	5	4	3	2	1	0
TS_WARM							
R/W-0h							

表 7-33. REG0x16_TS_WARM Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7-0	TS_WARM	R/W	0h	Setting of 0 is disable TS_WARM threshold. Lower limit is really 4mv. Reset by: REG_RESET	TS Warm Threshold POR: 0mV (0h) Range: 0mV-1020mV (0h-FFh) Bit Step: 4mV

7.6.1.24 REG0x17_TS_HOT Register (Offset = 17h) [Reset = 45h]

REG0x17_TS_HOT is shown in 図 7-42 and described in 表 7-34.

Return to the Summary Table.

TS_HOT Threshold

図 7-42. REG0x17_TS_HOT Register

7	6	5	4	3	2	1	0
TS_HOT							
R/W-45h							

表 7-34. REG0x17_TS_HOT Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7-0	TS_HOT	R/W	45h	Reset by: REG_RESET	TS Hot Threshold POR: 276mV (45h) Range: 0mV-1020mV (0h-FFh) Bit Step: 4mV

7.6.1.25 REG0x18_ADCCTRL0 Register (Offset = 18h) [Reset = 10h]

REG0x18_ADCCTRL0 is shown in 図 7-43 and described in 表 7-35.

Return to the Summary Table.

ADC Control 0

図 7-43. REG0x18_ADCCTRL0 Register

7	6	5	4	3	2	1	0
ADC_EN	ADC_RATE		ADC_SAMPLE		ADC_AVG	ADC_AVG_INIT	RESERVED
R/W-0h	R/W-0h		R/W-2h		R/W-0h	R/W-0h	R-0h

表 7-35. REG0x18_ADCCTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	ADC_EN	R/W	0h	Reset by: REG_RESET WATCHDOG	ADC control 0b = Disable (deafult) 1b = Enabled
6-5	ADC_RATE	R/W	0h	Reset by: REG_RESET	ADC conversion rate control 00b = Continuous conversion (default) 01b = One-shot conversion 10b = Every 1 second 11b = Every 1 minute
4-3	ADC_SAMPLE	R/W	2h	Reset by: REG_RESET	ADC sample speed 00b = 11 bit effective resolution 01b = 10 bit effective resolution 10b = 9 bit effective resolution (default) 11b = 9 bit effective resolution
2	ADC_AVG	R/W	0h	Reset by: REG_RESET	ADC average control 0b = Single value (default) 1b = Running average
1	ADC_AVG_INIT	R/W	0h	Reset by: REG_RESET	ADC average initial value control 0b = Start average using the existing register value 1b = Start average using a new ADC conversion
0	RESERVED	R	0h		Reserved

7.6.1.26 REG0x19_ADCCTRL1 Register (Offset = 19h) [Reset = C8h]

REG0x19_ADCCTRL1 is shown in 図 7-44 and described in 表 7-36.

Return to the Summary Table.

ADC Control 1

図 7-44. REG0x19_ADCCTRL1 Register

7	6	5	4	3	2	1	0
ADC_COMP1_EN	ADC_COMP2_EN	ADC_COMP3_EN	ADC_COMP1			ADCIN_MODE	RESERVED

図 7-44. REG0x19_ADCCTRL1 Register (続き)

R/W-1h	R/W-1h	R/W-0h	R/W-2h	R/W-0h	R-0h

表 7-36. REG0x19_ADCCTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	ADC_COMP1_EN	R/W	1h	Reset by: REG_RESET	ADC comparator 1 control 0b = ADC comparator 1 disabled 1b = ADC comparator 1 enabled
6	ADC_COMP2_EN	R/W	1h	Reset by: REG_RESET	ADC comparator 2 control 0b = ADC comparator 2 disabled 1b = ADC comparator 2 enabled
5	ADC_COMP3_EN	R/W	0h	Reset by: REG_RESET	ADC comparator 3 control 0b = ADC comparator 3 disabled 1b = ADC comparator 3 enabled
4-2	ADC_COMP1	R/W	2h	Reset by: REG_RESET	ADC Channel for Comparator 1 000b = TDIE 001b = ADCIN 010b = TS 011b = VBAT 100b = IBAT 101b = VIN 110b = VSYS 111b = IIN
1	ADCIN_MODE	R/W	0h	Reset by: REG_RESET	ADCIN Pin Mode of Operation 0b = General Purpose ADC input (no internal biasing) 1b = NTC ADC input (80 uA biasing)
0	RESERVED	R	0h		

7.6.1.27 REG0x1A_ADCCTRL2 Register (Offset = 1Ah) [Reset = 40h]

REG0x1A_ADCCTRL2 is shown in 図 7-45 and described in 表 7-37.

Return to the Summary Table.

ADC Control 2

図 7-45. REG0x1A_ADCCTRL2 Register

7	6	5	4	3	2	1	0
ADC_COMP2				ADC_COMP3		RESERVED	
R/W-2h				R/W-0h		R-0h	

表 7-37. REG0x1A_ADCCTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7-5	ADC_COMP2	R/W	2h	Reset by: REG_RESET	ADC Channel for Comparator 2 000b = TDIE 001b = ADCIN 010b = TS 011b = VBAT 100b = IBAT 101b = VIN 110b = VSYS 111b = IIN

表 7-37. REG0x1A_ADCCTRL2 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Notes	Description
4-2	ADC_COMP3	R/W	0h	Reset by: REG_RESET	ADC Channel for Comparator 3 000b = TDIE 001b = ADCIN 010b = TS 011b = VBAT 100b = IBAT 101b = VIN 110b = VSYS 111b = IIN
1-0	RESERVED	R	0h		Reserved

7.6.1.28 REG0x1B_ADC_DATA_VBAT Register (Offset = 1Bh) [Reset = 0000h]

REG0x1B_ADC_DATA_VBAT is shown in 図 7-46 and described in 表 7-38.

Return to the Summary Table.

VBAT ADC Measurement

図 7-46. REG0x1B_ADC_DATA_VBAT Register

15	14	13	12	11	10	9	8
ADC_DATA_VBAT							
R-0h							
7	6	5	4	3	2	1	0
ADC_DATA_VBAT							
R-0h							

表 7-38. REG0x1B_ADC_DATA_VBAT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	ADC_DATA_VBAT	R	0h	VBAT ADC Measurement POR: 0mV(0h) Range: 0mV - 5000mV (0h-FA0h) Clamped High Bit Step: 1.25mV

7.6.1.29 REG0x1D_ADC_DATA_TS Register (Offset = 1Dh) [Reset = 0000h]

REG0x1D_ADC_DATA_TS is shown in 図 7-47 and described in 表 7-39.

Return to the Summary Table.

TS ADC Measurement

図 7-47. REG0x1D_ADC_DATA_TS Register

15	14	13	12	11	10	9	8
ADC_DATA_TS							
R-0h							
7	6	5	4	3	2	1	0
ADC_DATA_TS							
R-0h							

表 7-39. REG0x1D_ADC_DATA_TS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	ADC_DATA_TS	R	0h	TS ADC Measurement POR: 0mV(0h) Range: 0mV - 1000mV (0h-FA0h) Clamped High Bit Step: 0.25mV

7.6.1.30 REG0x1F_ADC_DATA_IBAT Register (Offset = 1Fh) [Reset = 0000h]

REG0x1F_ADC_DATA_IBAT is shown in 図 7-48 and described in 表 7-40.

Return to the Summary Table.

IBAT ADC Measurement

図 7-48. REG0x1F_ADC_DATA_IBAT Register

15	14	13	12	11	10	9	8
ADC_DATA_IBAT							
R-0h							
7	6	5	4	3	2	1	0
ADC_DATA_IBAT							
R-0h							

表 7-40. REG0x1F_ADC_DATA_IBAT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	ADC_DATA_IBAT	R	0h	IBAT ADC Measurement POR: 0mA (0h) Format: 2s Complement Range: -3000mA-1000mA (F448h-3E8h) Clamped Low Clamped High Bit Step: 1mA

7.6.1.31 REG0x21_ADC_DATA_ADCIN Register (Offset = 21h) [Reset = 0000h]

REG0x21_ADC_DATA_ADCIN is shown in 図 7-49 and described in 表 7-41.

Return to the Summary Table.

ADCIN ADC Measurement

図 7-49. REG0x21_ADC_DATA_ADCIN Register

15	14	13	12	11	10	9	8
ADC_DATA_ADCIN							
R-0h							
7	6	5	4	3	2	1	0
ADC_DATA_ADCIN							
R-0h							

表 7-41. REG0x21_ADC_DATA_ADCIN Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15-0	ADC_DATA_ADCIN	R	0h	Bit Step is 0.25mV if ADCIN_MODE = 1	ADCIN ADC Measurement POR: 0mV(0h) Range: 0mV - 5000mV (0h-FA0h) Clamped High Bit Step: 1.25mV

7.6.1.32 REG0x23_ADC_DATA_VIN Register (Offset = 23h) [Reset = 0000h]

REG0x23_ADC_DATA_VIN is shown in 図 7-50 and described in 表 7-42.

Return to the Summary Table.

VIN ADC Measurement

図 7-50. REG0x23_ADC_DATA_VIN Register

15	14	13	12	11	10	9	8
ADC_DATA_VIN							
R-0h							
7	6	5	4	3	2	1	0
ADC_DATA_VIN							
R-0h							

表 7-42. REG0x23_ADC_DATA_VIN Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	ADC_DATA_VIN	R	0h	VIN ADC Measurement Range: 0mV-6000mV if VIN_OVP = 0 or 0mV-20000mV if VIN_OVP = 1 Clamped High Bit Step: 1.5mV if VIN_OVP = 0 or 5mV if VIN_OVP = 1

7.6.1.33 REG0x25_ADC_DATA_VSYS Register (Offset = 25h) [Reset = 0000h]

REG0x25_ADC_DATA_VSYS is shown in 図 7-51 and described in 表 7-43.

Return to the Summary Table.

VSYS ADC Measurement

図 7-51. REG0x25_ADC_DATA_VSYS Register

15	14	13	12	11	10	9	8
ADC_DATA_VSYS							
R-0h							
7	6	5	4	3	2	1	0
ADC_DATA_VSYS							
R-0h							

表 7-43. REG0x25_ADC_DATA_VSYS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	ADC_DATA_VSYS	R	0h	VSYS ADC Measurement POR: 0mV(0h) Range: 0mV - 5000mV (0h-FA0h) Clamped High Bit Step: 1.25mV

7.6.1.34 REG0x27_ADC_DATA_IIN Register (Offset = 27h) [Reset = 0000h]

REG0x27_ADC_DATA_IIN is shown in 図 7-52 and described in 表 7-44.

Return to the Summary Table.

IIN ADC Measurement

図 7-52. REG0x27_ADC_DATA_IIN Register

15	14	13	12	11	10	9	8
ADC_DATA_IIN							
R-0h							
7	6	5	4	3	2	1	0
ADC_DATA_IIN							
R-0h							

表 7-44. REG0x27_ADC_DATA_IIN Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	ADC_DATA_IIN	R	0h	IIN ADC Measurement POR: 0mA(0h) Range: 0mA - 1100mA (0h-898h) Clamped High Bit Step: 0.5mA

7.6.1.35 REG0x29_ADC_DATA_TDIE Register (Offset = 29h) [Reset = 0000h]

REG0x29_ADC_DATA_TDIE is shown in 図 7-53 and described in 表 7-45.

Return to the Summary Table.

TDIE ADC Measurement

図 7-53. REG0x29_ADC_DATA_TDIE Register

15	14	13	12	11	10	9	8
ADC_DATA_TDIE							
R-0h							
7	6	5	4	3	2	1	0
ADC_DATA_TDIE							
R-0h							

表 7-45. REG0x29_ADC_DATA_TDIE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	ADC_DATA_TDIE	R	0h	TDIE ADC Measurement POR: 0deg.C(0h) Format: 2s Complement Range: -16384deg.C - 16383.5deg.C (8000h-7FFFh) Bit Step: 0.5deg.C

7.6.1.36 REG0x2B_ADCALARM_COMP1 Register (Offset = 2Bh) [Reset = 2900h]

REG0x2B_ADCALARM_COMP1 is shown in 図 7-54 and described in 表 7-46.

Return to the Summary Table.

COMP1 ADC Measurement

図 7-54. REG0x2B_ADCALARM_COMP1 Register

15	14	13	12	11	10	9	8
ADCALARM1							
R/W-290h							
7	6	5	4	3	2	1	0
ADCALARM1				ADCALARM1_ABOVE	RESERVED		
R/W-290h				R/W-0h	R-0h		

表 7-46. REG0x2B_ADCALARM_COMP1 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15-4	ADCALARM1	R/W	290h	Reset by: REG_RESET	ADC Comparator 1 Threshold
3	ADCALARM1_ABOVE	R/W	0h	Reset by: REG_RESET	ADC Comparator1 Polarity 0b = Set Flag and send interrupt if ADC measurement becomes lower than comparator threshold 1b = Set Flag and send interrupt if ADC measurement becomes greater than, or equal to comparator threshold
2-0	RESERVED	R	0h		Reserved

7.6.1.37 REG0x2D_ADCALARM_COMP2 Register (Offset = 2Dh) [Reset = 41C0h]

REG0x2D_ADCALARM_COMP2 is shown in 図 7-55 and described in 表 7-47.

Return to the Summary Table.

COMP2 ADC Measurement

図 7-55. REG0x2D_ADCALARM_COMP2 Register

15	14	13	12	11	10	9	8
ADCALARM2							
R/W-41Ch							
7	6	5	4	3	2	1	0
ADCALARM2				ADCALARM2_ABOVE	RESERVED		
R/W-41Ch				R/W-0h	R-0h		

表 7-47. REG0x2D_ADCALARM_COMP2 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15-4	ADCALARM2	R/W	41Ch	Reset by: REG_RESET	ADC Comparator 2 Threshold
3	ADCALARM2_ABOVE	R/W	0h	Reset by: REG_RESET	ADC Comparator2 Polarity 0b = Set Flag and send interrupt if ADC measurement becomes lower than comparator threshold 1b = Set Flag and send interrupt if ADC measurement becomes greater than, or equal to comparator threshold
2-0	RESERVED	R	0h		Reserved

7.6.1.38 REG0x2F_ADCALARM_COMP3 Register (Offset = 2Fh) [Reset = 0000h]

REG0x2F_ADCALARM_COMP3 is shown in 図 7-56 and described in 表 7-48.

Return to the Summary Table.

COMP3 ADC Measurement

図 7-56. REG0x2F_ADCALARM_COMP3 Register

15	14	13	12	11	10	9	8
ADCALARM3							
R/W-0h							
7	6	5	4	3	2	1	0
ADCALARM3				ADCALARM3_ABOVE	RESERVED		
R/W-0h				R/W-0h	R-0h		

表 7-48. REG0x2F_ADCALARM_COMP3 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15-4	ADCALARM3	R/W	0h	Reset by: REG_RESET	ADC Comparator 3 Threshold
3	ADCALARM3_ABOVE	R/W	0h	Reset by: REG_RESET	ADC Comparator3 Polarity 0b = Set Flag and send interrupt if ADC measurement becomes lower than comparator threshold 1b = Set Flag and send interrupt if ADC measurement becomes greater than, or equal to comparator threshold
2-0	RESERVED	R	0h		Reserved

7.6.1.39 REG0x31_ADC_CHANNEL_DISABLE Register (Offset = 31h) [Reset = 00h]

REG0x31_ADC_CHANNEL_DISABLE is shown in 図 7-57 and described in 表 7-49.

Return to the Summary Table.

ADC Channel Disable

図 7-57. REG0x31_ADC_CHANNEL_DISABLE Register

7	6	5	4	3	2	1	0
IIN_ADC_DIS	VSYS_ADC_DIS	IBAT_ADC_DIS	VIN_ADC_DIS	VBAT_ADC_DIS	TS_ADC_DIS	ADCIN_ADC_DIS	TDIE_ADC_DIS
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

表 7-49. REG0x31_ADC_CHANNEL_DISABLE Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	IIN_ADC_DIS	R/W	0h	Reset by: REG_RESET	IIN ADC control 0b = ADC measurement enabled 1b = ADC measurement disabled
6	VSYS_ADC_DIS	R/W	0h	Reset by: REG_RESET	VSYS ADC control 0b = ADC measurement enabled 1b = ADC measurement disabled
5	IBAT_ADC_DIS	R/W	0h	Reset by: REG_RESET	IBAT ADC control 0b = ADC measurement enabled 1b = ADC measurement disabled

表 7-49. REG0x31_ADC_CHANNEL_DISABLE Register Field Descriptions (続き)

Bit	Field	Type	Reset	Notes	Description
4	VIN_ADC_DIS	R/W	0h	Reset by: REG_RESET	VIN ADC control 0b = ADC measurement enabled 1b = ADC measurement disabled
3	VBAT_ADC_DIS	R/W	0h	Reset by: REG_RESET	VBAT ADC control 0b = ADC measurement enabled 1b = ADC measurement disabled
2	TS_ADC_DIS	R/W	0h	Reset by: REG_RESET	TS ADC control 0b = ADC measurement enabled 1b = ADC measurement disabled
1	ADCIN_ADC_DIS	R/W	0h	Reset by: REG_RESET	ADCIN ADC control 0b = ADC measurement enabled 1b = ADC measurement disabled
0	TDIE_ADC_DIS	R/W	0h	Reset by: REG_RESET	TDIE ADC control 0b = ADC measurement enabled 1b = ADC measurement disabled

7.6.1.40 REG0x32_BUCK_VOUT Register (Offset = 32h) [Reset = 38h]

REG0x32_BUCK_VOUT is shown in 図 7-58 and described in 表 7-50.

Return to the Summary Table.

Buck VOUT Setting

図 7-58. REG0x32_BUCK_VOUT Register

7	6	5	4	3	2	1	0
RESERVED	BUCK_VOUT_SET						
R-0h	R/W-38h						

表 7-50. REG0x32_BUCK_VOUT Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	RESERVED	R	0h		Reserved
6-0	BUCK_VOUT_SET	R/W	38h	When GPIO DVS is used, this register is read only and matching the current voltage reference in BUCK_VOUTx_SET. When GPIO DVS is not used, this register sets the Buck output voltage. Reset by: REG_RESET	Buck Output Voltage Setting POR: 1.8V (38h) with BUCK_HI_RANGE = 1 Range: 0.4V-1.575V if BUCK_HI_RANGE = 0 or 0.4V-3.6V if BUCK_HI_RANGE = 1 Bit Step: 12.5 mV if BUCK_HI_RANGE = 0 or 25 mV for 0.4V-3.175V and 50 mV for 3.2V to 3.6V if BUCK_HI_RANGE = 1

7.6.1.41 REG0x33_BUCK_VOUT1 Register (Offset = 33h) [Reset = 38h]

REG0x33_BUCK_VOUT1 is shown in 図 7-59 and described in 表 7-51.

Return to the Summary Table.

Buck VOUT1 Setting

図 7-59. REG0x33_BUCK_VOUT1 Register

7	6	5	4	3	2	1	0

図 7-59. REG0x33_BUCK_VOUT1 Register (続き)

RESERVED	BUCK_VOUT1_SET
R-0h	R/W-38h

表 7-51. REG0x33_BUCK_VOUT1 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	RESERVED	R	0h		Reserved
6-0	BUCK_VOUT1_SET	R/W	38h	Reset by: REG_RESET	Buck Output Voltage Setting POR: 1.8V (38h) with BUCK_HI_RANGE = 1 Range: 0.4V-1.575V if BUCK_HI_RANGE = 0 or 0.4V-3.6V if BUCK_HI_RANGE = 1 Bit Step: 12.5 mV if BUCK_HI_RANGE = 0 or 25 mV for 0.4V-3.175V and 50 mV for 3.2V to 3.6V if BUCK_HI_RANGE = 1

7.6.1.42 REG0x34_BUCK_VOUT2 Register (Offset = 34h) [Reset = 72h]

REG0x34_BUCK_VOUT2 is shown in 図 7-60 and described in 表 7-52.

Return to the Summary Table.

Buck VOUT2 Setting

図 7-60. REG0x34_BUCK_VOUT2 Register

7	6	5	4	3	2	1	0
RESERVED	BUCK_VOUT2_SET						
R-0h	R/W-72h						

表 7-52. REG0x34_BUCK_VOUT2 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	RESERVED	R	0h		Reserved
6-0	BUCK_VOUT2_SET	R/W	72h	Reset by: REG_RESET	Buck Output Voltage Setting in Selection 2 POR: 3.3V (72h) with BUCK_HI_RANGE = 1 Range: 0.4V-1.575V if BUCK_HI_RANGE = 0 or 0.4V-3.6V if BUCK_HI_RANGE = 1 Bit Step: 12.5 mV if BUCK_HI_RANGE = 0 or 25 mV for 0.4V-3.175V and 50 mV for 3.2V to 3.6V if BUCK_HI_RANGE = 1

7.6.1.43 REG0x35_BUCK_VOUT3 Register (Offset = 35h) [Reset = 54h]

REG0x35_BUCK_VOUT3 is shown in 図 7-61 and described in 表 7-53.

Return to the Summary Table.

Buck VOUT3 Setting

図 7-61. REG0x35_BUCK_VOUT3 Register

7	6	5	4	3	2	1	0
RESERVED	BUCK_VOUT3_SET						
R-0h	R/W-54h						

表 7-53. REG0x35_BUCK_VOUT3 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	RESERVED	R	0h		Reserved
6-0	BUCK_VOUT3_SET	R/W	54h	Reset by: REG_RESET	Buck Output Voltage Setting in Selection 3 POR: 2.5V (54h) with BUCK_HI_RANGE = 1 Range: 0.4V-1.575V if BUCK_HI_RANGE = 0 or 0.4V-3.6V if BUCK_HI_RANGE = 1 Bit Step: 12.5 mV if BUCK_HI_RANGE = 0 or 25 mV for 0.4V-3.175V and 50 mV for 3.2V to 3.6V if BUCK_HI_RANGE = 1

7.6.1.44 REG0x36_BUCK_VOUT4 Register (Offset = 36h) [Reset = 20h]

REG0x36_BUCK_VOUT4 is shown in 図 7-62 and described in 表 7-54.

Return to the Summary Table.

Buck VOUT4 Setting

図 7-62. REG0x36_BUCK_VOUT4 Register

7	6	5	4	3	2	1	0
RESERVED	BUCK_VOUT4_SET						
R-0h	R/W-20h						

表 7-54. REG0x36_BUCK_VOUT4 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	RESERVED	R	0h		Reserved
6-0	BUCK_VOUT4_SET	R/W	20h	Reset by: REG_RESET	Buck Output Voltage Setting in Selection 4 POR: 1.2V (20h) with BUCK_HI_RANGE = 1 Range: 0.4V-1.575V if BUCK_HI_RANGE = 0 or 0.4V-3.6V if BUCK_HI_RANGE = 1 Bit Step: 12.5 mV if BUCK_HI_RANGE = 0 or 25 mV for 0.4V-3.175V and 50 mV for 3.2V to 3.6V if BUCK_HI_RANGE = 1

7.6.1.45 REG0x37_BUCK_CTRL0 Register (Offset = 37h) [Reset = 20h]

REG0x37_BUCK_CTRL0 is shown in 図 7-63 and described in 表 7-55.

Return to the Summary Table.

Buck Control 0

図 7-63. REG0x37_BUCK_CTRL0 Register

7	6	5	4	3	2	1	0
RESERVED		BUCK_HI_RANGE	BUCK_VRAMP_SPEED		RESERVED		
R-0h		R/W-1h	R/W-0h		R-0h		

表 7-55. REG0x37_BUCK_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7-6	RESERVED	R	0h		Reserved

表 7-55. REG0x37_BUCK_CTRL0 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Notes	Description
5	BUCK_HI_RANGE	R/W	1h	Reset by: REG_RESET	Buck VOUT Step 0b = Buck with 12.5 mV (0.4V to 1.575V) DVS steps 1b = Buck with 25 mV (0.4V to 3.175V) and 50 mV (3.2V to 3.6V) DVS steps
4-3	BUCK_VRAMP_SPEED	R/W	0h	Reset by: REG_RESET	Voltage Ramp Speed 00b = Instantaneous 01b = 5 mV/us 10b = 1 mV/us 11b = 0.1 mV/us
2-0	RESERVED	R	0h		Reserved

7.6.1.46 REG0x38_BUCK_CTRL1 Register (Offset = 38h) [Reset = 0Xh]

REG0x38_BUCK_CTRL1 is shown in 図 7-64 and described in 表 7-56.

Return to the Summary Table.

Buck Control 1

図 7-64. REG0x38_BUCK_CTRL1 Register

7	6	5	4	3	2	1	0
BUCK_EN_SET			RESERVED	BUCK_PG_EN	RESERVED	BUCK_PG	RESERVED
R/W-0h			R-0h	R/W-1h	R-0h	R-Xh	R-0h

表 7-56. REG0x38_BUCK_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7-5	BUCK_EN_SET	R/W	0h	Reset by: REG_RESET	Buck Enable Setting 000b = Buck in the sequence, enabled/disabled at a 001b = Buck in the sequence, enabled/disabled at b 010b = Buck in the sequence, enabled/disabled at c 011b = Buck in the sequence, enabled/disabled at d 100b = Buck not in the sequence, Buck disabled 101b = Buck not in the sequence, Buck enabled 110b = Buck not in sequence, Buck controlled by GPIO3 111b = Reserved
4	RESERVED	R	0h		Reserved
3	BUCK_PG_EN	R/W	1h	Reset by: REG_RESET	Enable Buck Power Good Feature 0b = Disable Buck power good feature 1b = Enable Buck power good feature
2	RESERVED	R	0h		Reserved
1	BUCK_PG	R	X		Buck Power Good 0b = Buck not power good 1b = Buck power good
0	RESERVED	R	0h		Reserved

7.6.1.47 REG0x39_BUBO_CTRL0 Register (Offset = 39h) [Reset = 3Eh]

REG0x39_BUBO_CTRL0 is shown in 図 7-65 and described in 表 7-57.

Return to the Summary Table.

Buck-boost Control 0

図 7-65. REG0x39_BUBO_CTRL0 Register

7	6	5	4	3	2	1	0
RESERVED	BUBO_VOUT_SET						
R-0h	R/W-3Eh						

表 7-57. REG0x39_BUBO_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	RESERVED	R	0h		Reserved
6-0	BUBO_VOUT_SET	R/W	3Eh	Reset by: REG_RESET	Buck-boost Output Voltage POR: 4800mV (3Eh) Range: 1700mV-5200mV (0h-46h) Clamped High Bit Step: 50mV Offset: 1700mV

7.6.1.48 REG0x3A_BUBO_CTRL1 Register (Offset = 3Ah) [Reset = 4Xh]

REG0x3A_BUBO_CTRL1 is shown in 図 7-66 and described in 表 7-58.

Return to the Summary Table.

Buck-boost Control 1

図 7-66. REG0x3A_BUBO_CTRL1 Register

7	6	5	4	3	2	1	0
BUBO_EN_SET			RESERVED	BUBO_PG_EN	RESERVED	BUBO_PG	BUBO_ILIMIT
R/W-2h			R-0h	R/W-1h	R-0h	R-Xh	R/W-0h

表 7-58. REG0x3A_BUBO_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7-5	BUBO_EN_SET	R/W	2h	Reset by: REG_RESET	Buck-boost Enable Setting 000b = Buck-boost in the sequence, enabled/disabled at a 001b = Buck-boost in the sequence, enabled/disabled at b 010b = Buck-boost in the sequence, enabled/disabled at c 011b = Buck-boost in the sequence, enabled/disabled at d 100b = Buck-boost not in the sequence, Buck-boost disabled 101b = Buck-boost not in the sequence, Buck-boost enabled 110b = Buck-boost not in sequence, Buck-boost controlled by GPIO2 111b = Reserved
4	RESERVED	R	0h		Reserved
3	BUBO_PG_EN	R/W	1h	Reset by: REG_RESET	Enable Buck-boost Power Good Feature 0b = Disable Buck-boost power good feature 1b = Enable Buck-boost power good feature

表 7-58. REG0x3A_BUBO_CTRL1 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Notes	Description
2	RESERVED	R	0h		Reserved
1	BUBO_PG	R	X		Buck-boost Power Good 0b = Buck-boost not power good 1b = Buck-boost power good
0	BUBO_ILIMIT	R/W	0h	Reset by: REG_RESET	Buck-boost Input Current Limit 0b = Unlimited 1b = 100 mA

7.6.1.49 REG0x3B_LDO1_CTRL0 Register (Offset = 3Bh) [Reset = 14h]

REG0x3B_LDO1_CTRL0 is shown in 図 7-67 and described in 表 7-59.

Return to the Summary Table.

LDO1 Control 0

図 7-67. REG0x3B_LDO1_CTRL0 Register

7	6	5	4	3	2	1	0
RESERVED	LDO1_LDO_SWITCH_CONFG	LDO1_VOUT_SET					
R-0h	R/W-0h	R/W-14h					

表 7-59. REG0x3B_LDO1_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	RESERVED	R	0h		Reserved
6	LDO1_LDO_SWITCH_CONFG	R/W	0h		LDO1 LDO/Bypass mode Selection 0b = LDO mode 1b = Bypass mode
5-0	LDO1_VOUT_SET	R/W	14h	Reset by: REG_RESET	LDO1 Output Voltage Setting POR: 1800mV (14h) Range: 800mV-3600mV (0h-38h) Clamped High Bit Step: 50mV Offset: 800mV

7.6.1.50 REG0x3C_LDO1_CTRL1 Register (Offset = 3Ch) [Reset = 2Xh]

REG0x3C_LDO1_CTRL1 is shown in 図 7-68 and described in 表 7-60.

Return to the Summary Table.

LDO1 Control 1

図 7-68. REG0x3C_LDO1_CTRL1 Register

7	6	5	4	3	2	1	0
LDO1_EN_SET			RESERVED	LDO1_PG_EN	RESERVED	LDO1_PG	LDO1_SHIP_AO
R/W-1h			R-0h	R/W-1h	R-0h	R-Xh	R/W-0h

表 7-60. REG0x3C_LDO1_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7-5	LDO1_EN_SET	R/W	1h	Reset by: REG_RESET	LDO1 Enable Setting 000b = LDO1 in the sequence, enabled/disabled at a 001b = LDO1 in the sequence, enabled/disabled at b 010b = LDO1 in the sequence, enabled/disabled at c 011b = LDO1 in the sequence, enabled/disabled at d 100b = LDO1 not in the sequence, LDO1 disabled 101b = LDO1 not in the sequence, LDO1 enabled 110b = LDO1 not in sequence, LDO1 controlled by GPIO4 111b = LDO1 always on
4	RESERVED	R	0h		Reserved
3	LDO1_PG_EN	R/W	1h	Reset by: REG_RESET	Enable LDO1 Power Good Feature 0b = Disable LDO1 power good feature 1b = Enable LDO1 power good feature
2	RESERVED	R	0h		Reserved
1	LDO1_PG	R	X		LDO1 Power Good 0b = LDO1 not power good 1b = LDO1 power good
0	LDO1_SHIP_AO	R/W	0h	Reset by: REG_RESET	LDO1 ON/OFF in LDO1-ON Ship Mode or Ship Mode 0b = LDO1 powering down in power-down sequence entering ship mode in always-on mode 1b = LDO1 not powering down in power-down sequence entering LDO1-ON ship mode in always-on mode

7.6.1.51 REG0x3D_LDO2_CTRL0 Register (Offset = 3Dh) [Reset = 32h]

REG0x3D_LDO2_CTRL0 is shown in 図 7-69 and described in 表 7-61.

Return to the Summary Table.

LDO2 Control 0

図 7-69. REG0x3D_LDO2_CTRL0 Register

7	6	5	4	3	2	1	0
RESERVED	LDO2_LDO_SWITCH_CONFG	LDO2_VOUT_SET					
R-0h	R/W-0h	R/W-32h					

表 7-61. REG0x3D_LDO2_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	RESERVED	R	0h		Reserved
6	LDO2_LDO_SWITCH_CONFG	R/W	0h		LDO2 LDO/Bypass mode Selection 0b = LDO mode 1b = Bypass mode
5-0	LDO2_VOUT_SET	R/W	32h	Reset by: REG_RESET	LDO2 Output Voltage Setting POR: 3300mV (32h) Range: 800mV-3600mV (0h-38h) Clamped High Bit Step: 50mV Offset: 800mV

7.6.1.52 REG0x3E_LDO2_CTRL1 Register (Offset = 3Eh) [Reset = 8Xh]

REG0x3E_LDO2_CTRL1 is shown in 図 7-70 and described in 表 7-62.

Return to the Summary Table.

LDO2 Control 1

図 7-70. REG0x3E_LDO2_CTRL1 Register

7	6	5	4	3	2	1	0
LDO2_EN_SET			RESERVED	LDO2_PG_EN	RESERVED	LDO2_PG	RESERVED
R/W-4h			R-0h	R/W-1h	R-0h	R-Xh	R-0h

表 7-62. REG0x3E_LDO2_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7-5	LDO2_EN_SET	R/W	4h	Reset by: REG_RESET	LDO2 Enable Setting 000b = LDO2 in the sequence, enabled/disabled at a 001b = LDO2 in the sequence, enabled/disabled at b 010b = LDO2 in the sequence, enabled/disabled at c 011b = LDO2 in the sequence, enabled/disabled at d 100b = LDO2 not in the sequence, LDO2 disabled 101b = LDO2 not in the sequence, LDO2 enabled 110b = LDO2 not in sequence, LDO2 controlled by GPIO1 111b = LDO2 always on
4	RESERVED	R	0h		Reserved
3	LDO2_PG_EN	R/W	1h	Reset by: REG_RESET	Enable LDO2 Power Good Feature 0b = Disable LDO2 power good feature 1b = Enable LDO2 power good feature
2	RESERVED	R	0h		Reserved
1	LDO2_PG	R	X		LDO2 Power Good 0b = LDO2 not power good 1b = LDO2 power good
0	RESERVED	R	0h		Reserved

7.6.1.53 REG0x3F_NTC_CTRL Register (Offset = 3Fh) [Reset = A0h]

REG0x3F_NTC_CTRL is shown in 図 7-71 and described in 表 7-63.

Return to the Summary Table.

NTC Control

図 7-71. REG0x3F_NTC_CTRL Register

7	6	5	4	3	2	1	0
TS_ACTION_EN	TS_FAULT_BAT_EN	TS_FAULT_VIN_EN	TS_ICHG	TS_VREG	TSHUT_LOCKOUT_EN	RESERVED	
R/W-1h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R-0h	

表 7-63. REG0x3F_NTC_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	TS_ACTION_EN	R/W	1h	Reset by: REG_RESET WATCHDOG	TS Action Enable 0b = TS action disabled 1b = TS action enabled

表 7-63. REG0x3F_NTC_CTRL Register Field Descriptions (続き)

Bit	Field	Type	Reset	Notes	Description
6	TS_FAULT_BAT_EN	R/W	0h	Reset by: REG_RESET WATCHDOG	TS Fault Monitoring Enable in Battery-only Mode 0b = TS fault monitoring disabled 1b = TS fault monitoring enabled and folloing ADC_RATE
5	TS_FAULT_VIN_EN	R/W	1h	Reset by: REG_RESET WATCHDOG	TS Fault Monitoring Enable in Adapter Mode 0b = TS fault monitoring disabled 1b = TS fault monitoring enabled at 30ms rate
4	TS_ICHG	R/W	0h	Reset by: REG_RESET	Fast charge current when decreased by TS function 0b = 0.5 x ICHG 1b = 0.2 x ICHG
3	TS_VREG	R/W	0h	Reset by: REG_RESET	Reduced target battery voltage during Warm 0b = VBATREG-100mV 1b = VBATREG-200mV
2	TSHUT_LOCKOUT_EN	R/W	0h	Reset by: REG_RESET	Lockout device in TSHUT protection after retries 0b = Do not lockout device in TSHUT protection 1b = Lockout device in TSHUT protection
1-0	RESERVED	R	0h		Reserved

7.6.1.54 REG0x40_GPIO1_CTRL Register (Offset = 40h) [Reset = 00h]

REG0x40_GPIO1_CTRL is shown in 図 7-72 and described in 表 7-64.

Return to the Summary Table.

GPIO1 Control

図 7-72. REG0x40_GPIO1_CTRL Register

7	6	5	4	3	2	1	0
GPIO1_CONFIG				RESERVED			
R/W-0h				R-0h			

表 7-64. REG0x40_GPIO1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7-4	GPIO1_CONFIG	R/W	0h	Reset by: REG_RESET	GPIO1 Configuration 0000b = GPIO1 forced open-drain high 0001b = GPIO1 forced low 0010b = GPIO1 configured as deglitched level shifted /MR 0011b = GPIO1 forced push-pull high 0100b = GPIO1 as sequencer output at a (push-pull) 0101b = GPIO1 as sequencer output at b (push-pull) 0110b = GPIO1 as sequencer output at c (push-pull) 0111b = GPIO1 as sequencer output at d (push-pull) 1000b = GPIO1 in level-sensitive input mode 1001b = Reserved 1010b = GPIO1 in positive-edge trigger input mode 1011b = GPIO1 in negative-edge trigger input mode 1100b = Reserved 1101b = Reserved 1110b = Reserved 1111b = Reserved
3-0	RESERVED	R	0h		Reserved

7.6.1.55 REG0x41_GPIO2_CTRL Register (Offset = 41h) [Reset = 00h]

REG0x41_GPIO2_CTRL is shown in 図 7-73 and described in 表 7-65.

Return to the Summary Table.

GPIO2 Control

図 7-73. REG0x41_GPIO2_CTRL Register

7	6	5	4	3	2	1	0
GPIO2_CONFIG				RESERVED			
R/W-0h				R-0h			

表 7-65. REG0x41_GPIO2_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7-4	GPIO2_CONFIG	R/W	0h	Reset by: REG_RESET	GPIO2 Configuration 0000b = GPIO2 forced open-drain high 0001b = GPIO2 forced low 0010b = GPIO2 configured as sequence PG pin (push-pull) 0011b = GPIO2 forced push-pull high 0100b = GPIO2 as sequencer output at a (push-pull) 0101b = GPIO2 as sequencer output at b (push-pull) 0110b = GPIO2 as sequencer output at c (push-pull) 0111b = GPIO2 as sequencer output at d (push-pull) 1000b = GPIO2 in level-sensitive input mode 1001b = Reserved 1010b = GPIO2 in positive-edge trigger input mode 1011b = GPIO2 in negative-edge trigger input mode 1100b = Reserved 1101b = Reserved 1110b = Reserved 1111b = Reserved
3-0	RESERVED	R	0h		Reserved

7.6.1.56 REG0x42_GPIO3_CTRL Register (Offset = 42h) [Reset = 20h]

REG0x42_GPIO3_CTRL is shown in 図 7-74 and described in 表 7-66.

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GPIO3 Control

図 7-74. REG0x42_GPIO3_CTRL Register

7	6	5	4	3	2	1	0
GPIO3_CONFIG				RESERVED			
R/W-2h				R-0h			

表 7-66. REG0x42_GPIO3_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7-4	GPIO3_CONFIG	R/W	2h	Reset by: REG_RESET	GPIO3 Configuration 0000b = GPIO3 forced open-drain high 0001b = GPIO3 forced low 0010b = Buck DVS controlled by GPIO3 0011b = GPIO3 forced push-pull high 0100b = GPIO3 as sequencer output at a (push-pull) 0101b = GPIO3 as sequencer output at b (push-pull) 0110b = GPIO3 as sequencer output at c (push-pull) 0111b = GPIO3 as sequencer output at d (push-pull) 1000b = GPIO3 in level-sensitive input mode 1001b = Reserved 1010b = GPIO3 in positive-edge trigger input mode 1011b = GPIO3 in negative-edge trigger input mode 1100b = Reserved 1101b = Reserved 1110b = Reserved 1111b = Reserved
3-0	RESERVED	R	0h		Reserved

7.6.1.57 REG0x43_GPIO4_CTRL Register (Offset = 43h) [Reset = 20h]

REG0x43_GPIO4_CTRL is shown in 図 7-75 and described in 表 7-67.

Return to the Summary Table.

GPIO4 Control

図 7-75. REG0x43_GPIO4_CTRL Register

7	6	5	4	3	2	1	0
GPIO4_CONFIG				RESERVED			
R/W-2h				R-0h			

表 7-67. REG0x43_GPIO4_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7-4	GPIO4_CONFIG	R/W	2h	Reset by: REG_RESET	GPIO4 Configuration 0000b = GPIO4 forced open-drain high 0001b = GPIO4 forced low 0010b = GPIO4 as VSEL2 pin (valid only if LDO1_EN_SET != 110 AND GPIO3_CONFIG = 0010) 0011b = GPIO4 forced push-pull high 0100b = GPIO4 as sequencer output at a (push-pull) 0101b = GPIO4 as sequencer output at b (push-pull) 0110b = GPIO4 as sequencer output at c (push-pull) 0111b = GPIO4 as sequencer output at d (push-pull) 1000b = GPIO4 in level-sensitive input mode 1001b = Reserved 1010b = GPIO4 in positive-edge trigger input mode 1011b = GPIO4 in negative-edge trigger input mode 1100b = GPIO4 in 20% duty ratio pull-low PWM mode (open-drain) 1101b = GPIO4 in 40% duty ratio pull-low PWM mode (open-drain) 1110b = GPIO4 in 60% duty ratio pull-low PWM mode (open-drain) 1111b = GPIO4 in 80% duty ratio pull-low PWM mode (open-drain)
3-0	RESERVED	R	0h		Reserved

7.6.1.58 REG0x44_PART_INFORMATION Register (Offset = 44h) [Reset = 01h]

REG0x44_PART_INFORMATION is shown in 図 7-76 and described in 表 7-68.

Return to the Summary Table.

Part information

図 7-76. REG0x44_PART_INFORMATION Register

7	6	5	4	3	2	1	0
DEVICE_ID				RESERVED	DEV_REV		
R-0h				R-0h	R-1h		

表 7-68. REG0x44_PART_INFORMATION Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DEVICE_ID	R	0h	Device part number
3	RESERVED	R	0h	Reserved
2-0	DEV_REV	R	1h	Device revision

8 Application and Implementation

注

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8.1 Application Information

A typical application consists of the device configured as an I^2C controlled single cell Li-Ion battery charger and power path management device for battery applications such as fitness trackers and other portable devices. It integrates an input reverse-block FET (Q1), LDO converter FET (Q2), and BATFET (Q3) between the system and battery. The device also integrates a Buck rail, a Buck-boost rail, two LDOs to power other system loads.

The system designer may connect the $\overline{MR}$ pin input to a push button to send interrupts to the host as a button is pressed or to allow the user to reset the system.

8.2 Typical Application

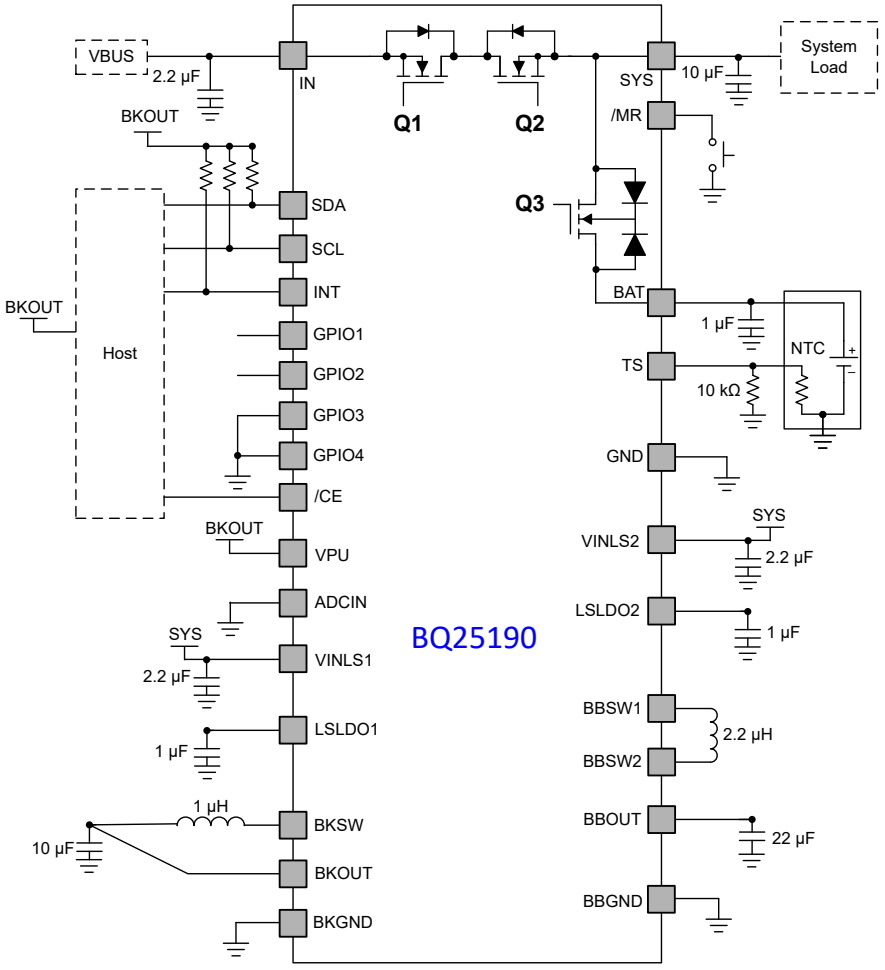


図 8-1. BQ25190 Typical Application Diagram

8.2.1 Design Requirements

表 8-1. Design Requirements

PARAMETER	VALUE
Input supply voltage	5 V
System regulation voltage	4.5 V
Battery regulation voltage	4.2 V
Buck output voltage	1.8 V
Buck-boost output voltage	4.8 V
LDO1 output voltage	1.8 V
LDO2 output voltage	3.3 V

8.2.2 Detailed Design Procedure

8.2.2.1 Input Capacitor Selection

Low ESR X5R or X7R ceramic capacitors are preferred for input capacitor to minimize transient currents from the battery or adapter.

For the integrated charger, a 2.2μF input decoupling capacitor (C_{IN}) is normally used for 5V V_{IN}. After derating, the effective capacitance needs to be at least 1μF.

For the integrated Buck rail, a 4.7μF input decoupling capacitor (C_{SYS_A5}) is normally used.

For the integrated Buck-boost rail, a 10μF input doucoupling capacitor (C_{SYS_F5}) is normally used.

For the integrated LDO rails, a 2.2μF input decoupling capacitor (C_{VINLS1}/C_{VINLS2}) is normally used.

8.2.2.2 Output Capacitor Selection

Low ESR X5R or X7R ceramic capacitors are preferred for output capacitors for optimized internal compensation loop stability, or output voltage ripple of integrated Buck or Buck-boost rails.

For the integrated charger, a 10μF output capacitor (C_{SYS_D5}) is normally used. After derating, the total effective capacitance on all the SYS pins needs to be higher than 1μF but less than 100μF.

For the integrated Buck rail, a 10μF output capacitor (C_{BKOUT}) is normally used. After derating, the effective capacitance needs to be at least 4μF but less than 25μF.

For the integrated Buck-boost rail, a 22μF output capacitor (C_{BKOUT}) is normally used. After derating, the effective capacitance needs to be at least 5μF.

For the integrated LDO rails, a 1μF output capacitor (C_{LSLDO1}/C_{LSLDO2}) is normally used. After defating, the effective capacitance needs to be at least 0.5μF at least but less than 22μF.

8.2.2.3 Inductor Selection

The inductor selection for the Buck rail and Buck-boost rail is mainly a trade off between size and efficiency as larger sized inductors normally have lower DC resistance, thus higher efficiency. It's also recommended to choose the inductor with saturation current at least 20% higher than peak inductor current under the highest load condition in the application.

For the integrated Buck rail, a 1μH inductor is recommended to be used.

For the integrated Buck-boost rail, a 2.2μH inductor is recommended to be used.

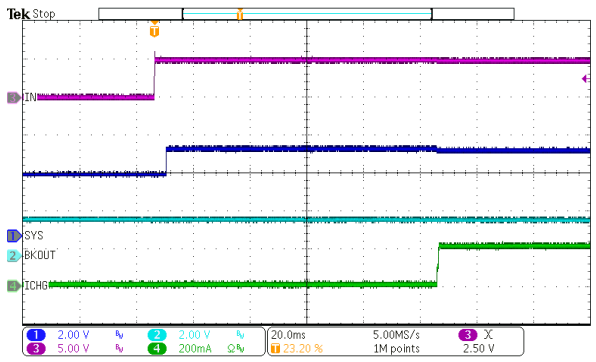
8.2.2.4 Recommended Passive Components

表 8-2 shows the list of recommended components for the typical application circuit.

表 8-2. Recommended Components for Typical Application Circuit

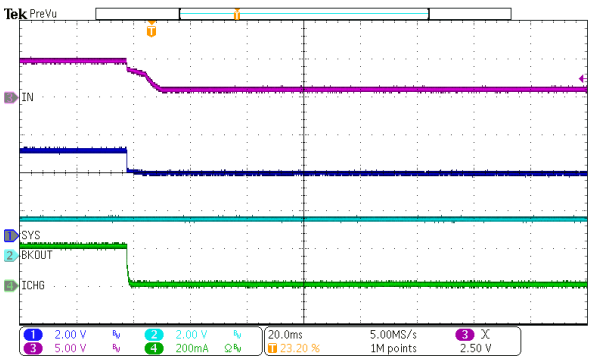
REFERENCE	DESCRIPTION	VALUE	SIZE CODE
C_{IN}	Ceramic capacitor C1005X5R1V225K050BC	2.2µF	0402
C_{SYS_D5}	Ceramic capacitor GRM155R61A106ME11	10µF	0402
C_{BAT}	Ceramic capacitor EMK105BJ105KVHF	1µF	0402
C_{VINLS1}	Ceramic capacitor GRM155R60J225ME15D	2.2µF	0402
C_{LSLDO1}	Ceramic capacitor GRM155R61C105MA12D	1µF	0402
C_{VINLS2}	Ceramic capacitor GRM155R60J225ME15D	2.2µF	0402
C_{LSLDO2}	Ceramic capacitor GRM155R61C105MA12D	1µF	0402
C_{SYS_A5}	Ceramic capacitor GRM155R60J475ME47D	4.7µF	0402
L_{BK}	Inductor DFE201610E-1R0M	1µH	0806
C_{BKOUT}	Ceramic capacitor GRM155R60J106ME15D	10µF	0402
C_{SYS_F5}	Ceramic capacitor GRM155R61A106ME11	10µF	0402
L_{BB}	Inductor DFE201610E-2R2M	2.2µH	0806
C_{BBOUT}	Ceramic capacitor GRM188R60J226MEA0D	22µF	0603

8.2.3 Application Performance Plots



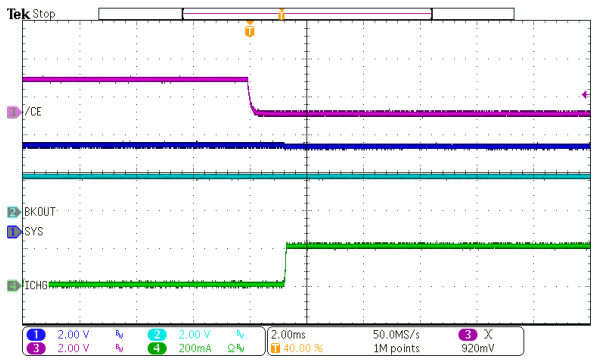
V_{BAT} = 3.2V I_{CHG} = 200mA

図 8-2. Adapter Plug-In with Charge Enabled



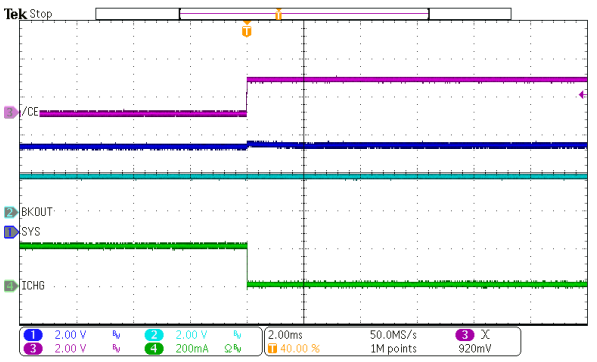
V_{BAT} = 3.2V I_{CHG} = 200mA

図 8-3. Adapter Unplug with Charge Enabled



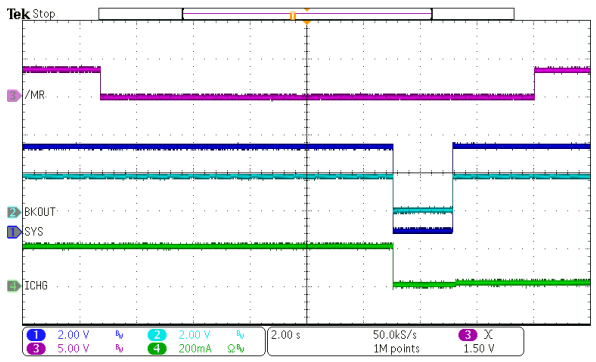
V_{BAT} = 3.2V I_{CHG} = 200mA

図 8-4. Charge Enable



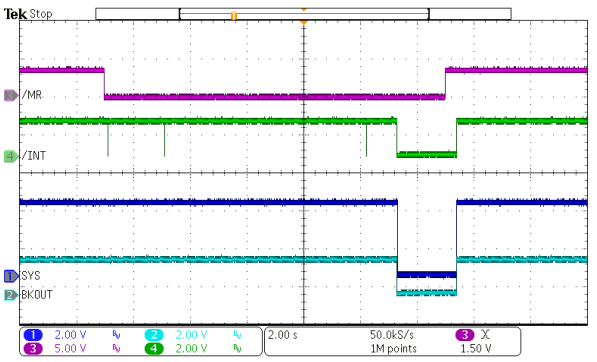
V_{BAT} = 3.2V I_{CHG} = 200mA

図 8-5. Charge Disable



V_{BAT} = 3.8V I_{CHG} = 200mA

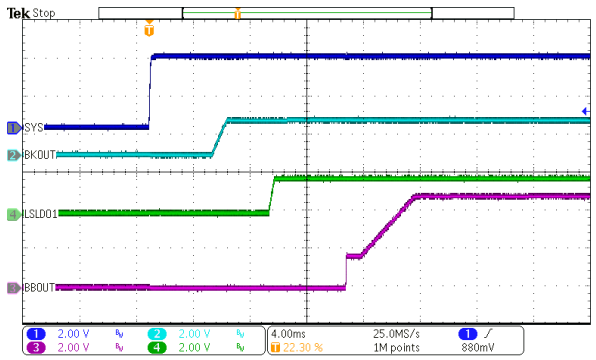
図 8-6. Hardware Reset by Push-Button ($\overline{MR}$) Press with Adapter



V_{BAT} = 3.8V

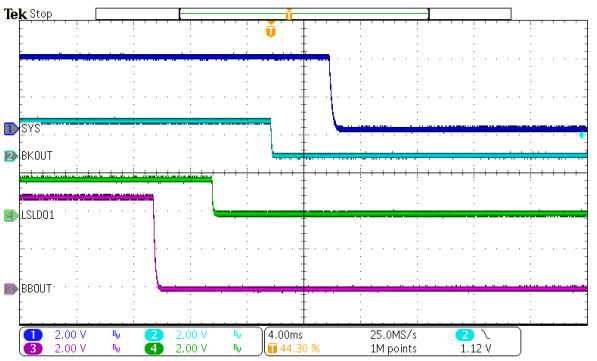
図 8-7. Hardware Reset by Push-Button ($\overline{MR}$) Press without Adapter

8.2.3 Application Performance Plots (continued)



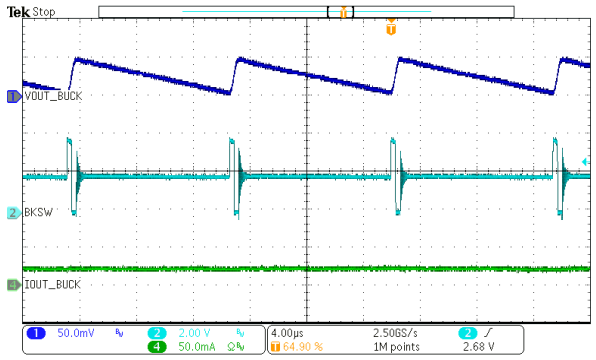
V_{BAT} = 3.8V V_{VINLS1} = V_{SYS}

図 8-8. Power-Up Sequence During Ship Mode Exit



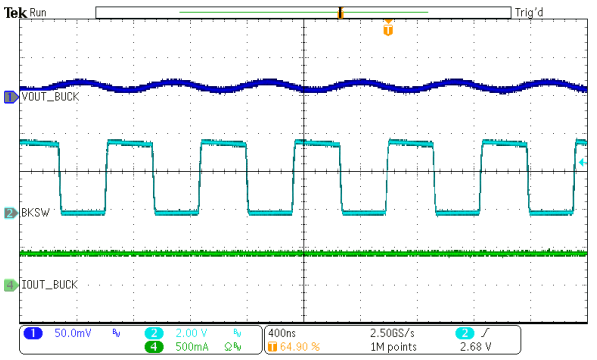
V_{BAT} = 3.8V

図 8-9. Power-Down Sequence (default) During Ship Mode Entry



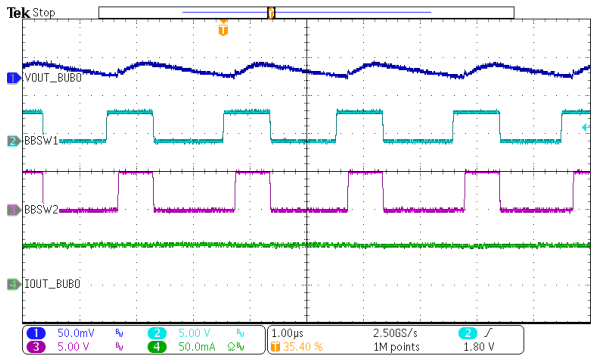
V_{BAT} = V_{SYS} = 3.8V V_{BKOUT} = 1.8V

図 8-10. Buck Typical Operation (Buck load = 20mA)



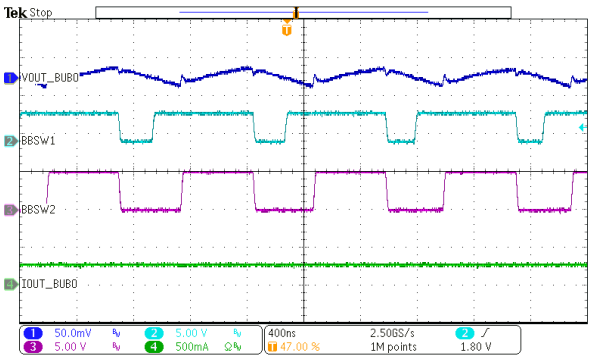
V_{BAT} = V_{SYS} = 3.8V V_{BKOUT} = 1.8V

図 8-11. Buck Typical Operation (Buck load = 400mA)



V_{BAT} = V_{SYS} = 3.8V V_{BBOUT} = 5V

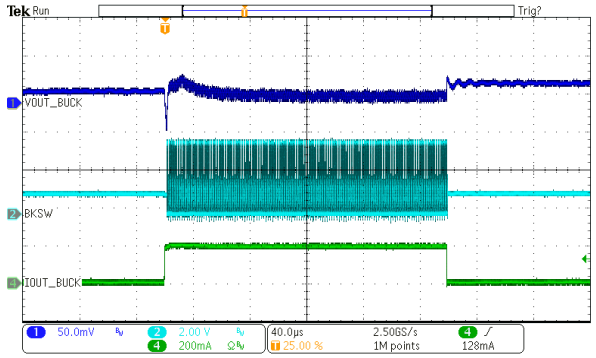
図 8-12. Buck-Boost Typical Operation (Buck-boost load = 50mA)



V_{BAT} = V_{SYS} = 3.8V V_{BBOUT} = 5V

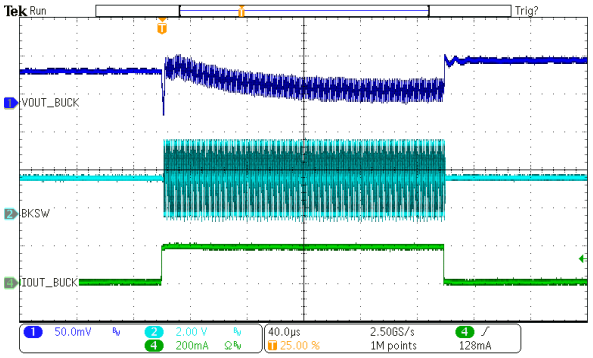
図 8-13. Buck-Boost Typical Operation (Buck-boost load = 250mA)

8.2.3 Application Performance Plots (continued)



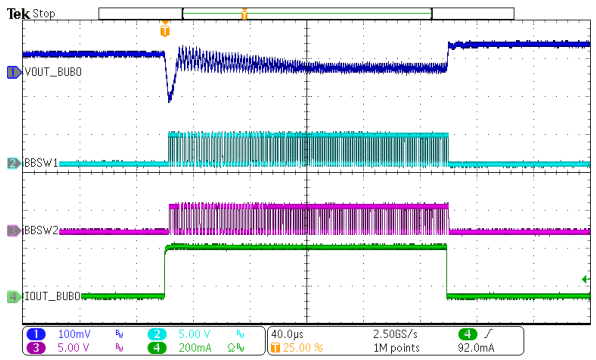
V_{BAT} = V_{SYS} = 3.8V V_{BKOUT} = 1V

図 8-14. Buck Load Transient (Buck load = 0 to 200mA)



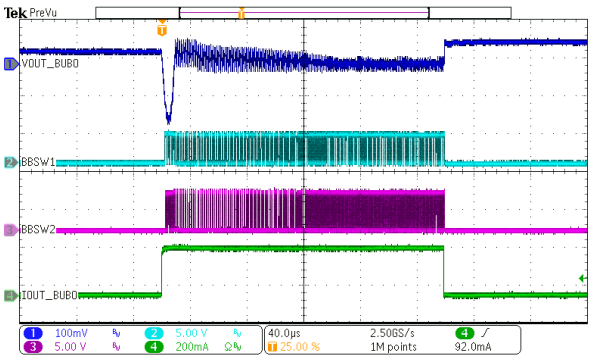
V_{BAT} = V_{SYS} = 3.8V V_{BKOUT} = 1.8V

図 8-15. Buck Load Transient (Buck load = 0 to 200mA)



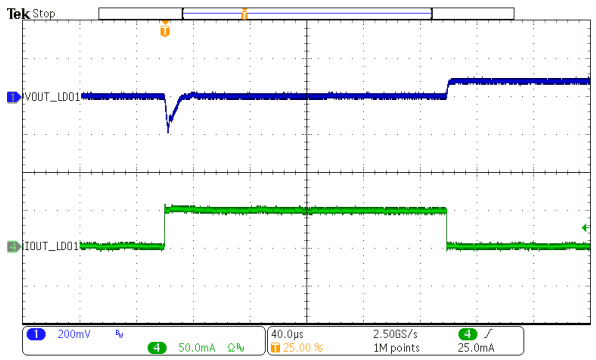
V_{BAT} = V_{SYS} = 3.8V V_{BBOUT} = 3.3V

図 8-16. Buck-Boost Load Transient (Buck-boost load = 0 to 250mA)



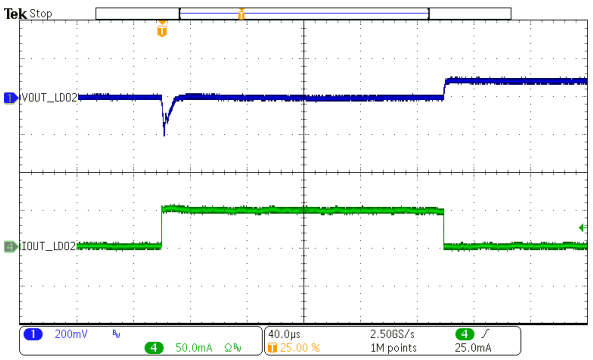
V_{BAT} = V_{SYS} = 3.8V V_{BBOUT} = 5V

図 8-17. Buck-Boost Load Transient (Buck-boost load = 0 to 250mA)



V_{BAT} = V_{SYS} = V_{VINLS1} = 3.8V V_{LSLDO1} = 1.8V

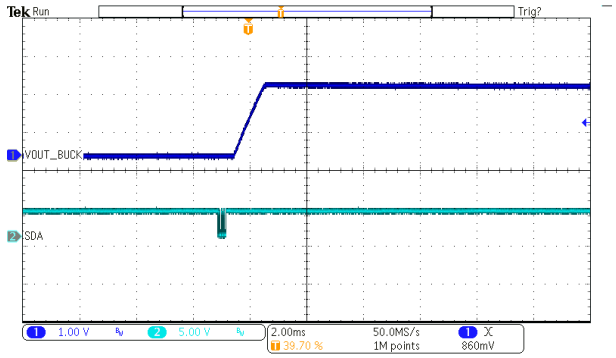
図 8-18. LDO1 Load Transient (LDO1 load = 0 to 50mA)



V_{BAT} = V_{SYS} = V_{VINLS2} = 3.8V V_{LSLDO2} = 3.3V

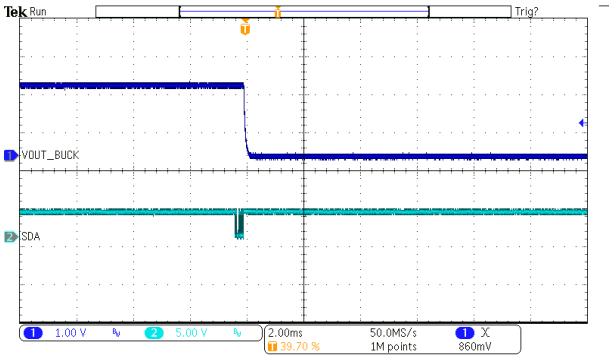
図 8-19. LDO2 Load Transient (LDO2 load = 0 to 50mA)

8.2.3 Application Performance Plots (continued)



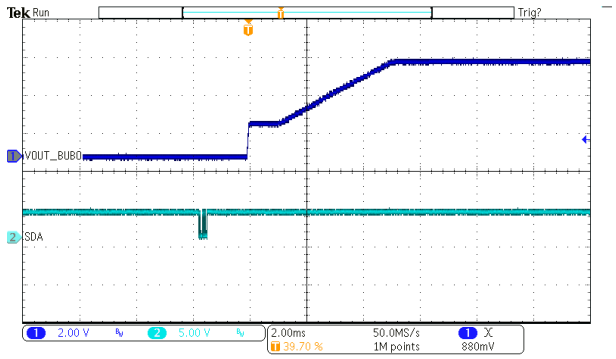
V_{BAT} = V_{SYS} = 3.8V V_{BKOUT} = 1.8V

図 8-20. Buck Enable (No load)



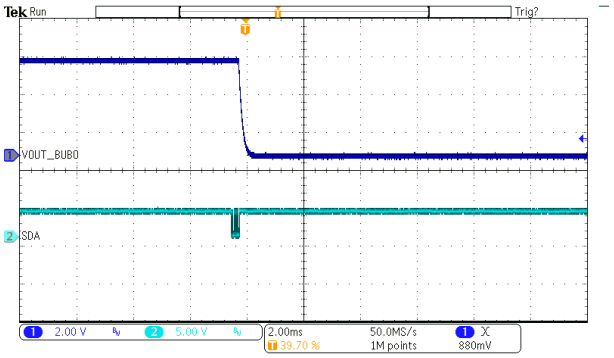
V_{BAT} = V_{SYS} = 3.8V V_{BKOUT} = 1.8V

図 8-21. Buck Disable (No load)



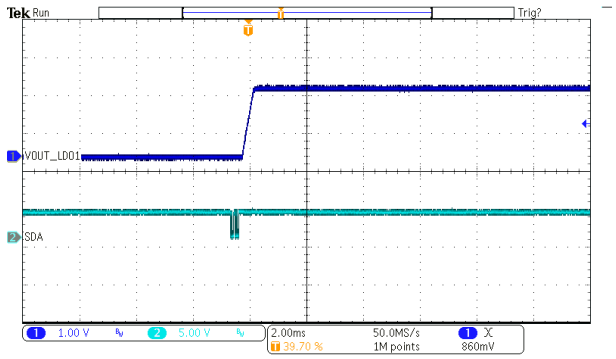
V_{BAT} = V_{SYS} = 3.8V V_{BBOUT} = 5V

図 8-22. Buck-Boost Enable (No load)



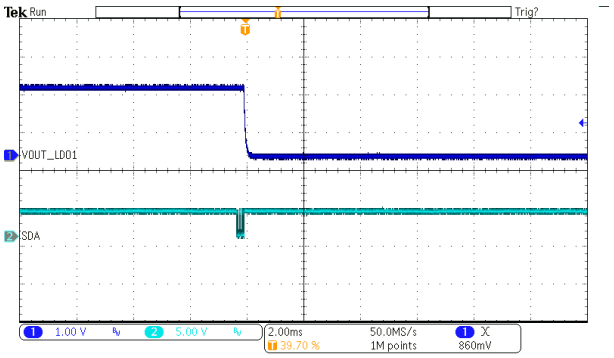
V_{BAT} = V_{SYS} = 3.8V V_{BBOUT} = 5V

図 8-23. Buck-Boost Disable (No load)



V_{BAT} = V_{SYS} = V_{VINLS1} = 3.8V V_{LSLDO1} = 1.8V

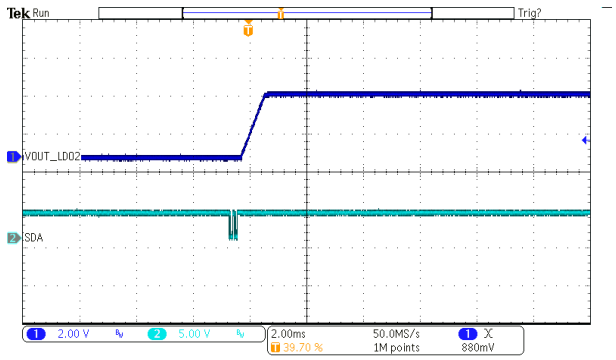
図 8-24. LDO1 Enable (No load)



V_{BAT} = V_{SYS} = V_{VINLS1} = 3.8V V_{LSLDO1} = 1.8V

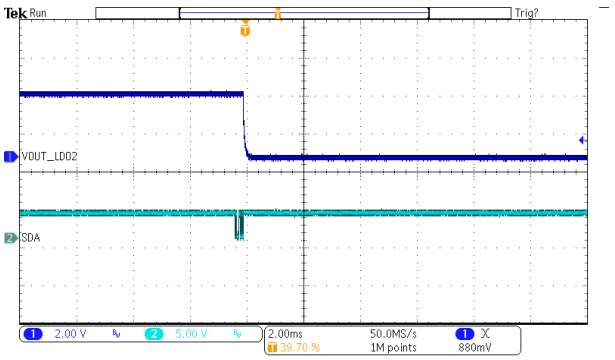
図 8-25. LDO1 Disable (No load)

8.2.3 Application Performance Plots (continued)



V_{BAT} = V_{SYS} = V_{VINLS2} = 3.8V V_{LSLDO2} = 3.3V

図 8-26. LDO2 Enable (No load)



V_{BAT} = V_{SYS} = V_{VINLS2} = 3.8V V_{LSLDO2} = 3.3V

図 8-27. LDO2 Disable (No load)

9 Power Supply Recommendations

In order to provide an output voltage on SYS, the device requires a power supply between 3V and 18V input connected to IN or a single-cell lithium battery with voltage > $V_{BATDEPLZ}$ connected to BAT.

10 Layout

10.1 Layout Guidelines

The following PCB layout design guidelines are recommended:

- Place the input decoupling caps from VIN to GND, SYS (A5) to GND, and SYS (F5) to GND close to the IC with wide and short traces. The input decoupling caps from SYS (A5) to GND and from SYS (F5) to GND are required.
- Place the output caps from BBOUT to GND, SYS to GND, BAT to GND, LSLDO1 to GND, and LSLDO2 to GND close to the IC with wide and short traces.
- All SYS pins must be connected with a wide trace for strong connection.
- 2nd layer should be the ground layer for strong ground connection with vias for all the GND connections, especially for BKGND, BBGND, and all the input/output caps' GND connections. Avoid routing which can intterupt or cut the ground planes.
- The Buck output voltage feedback from Buck output cap to BKOUT should be realized with an independent trace with no current flow. This feedback line is a sensitive, high impedance line and should be routed away from noisy components and traces (for example, switch nodes of Buck and Buck-boost) or other noise sources.
- The power (high current) paths traces must be sized appropriately for the maximum charge current in order to avoid large voltage drops on these traces.

10.2 Layout Example

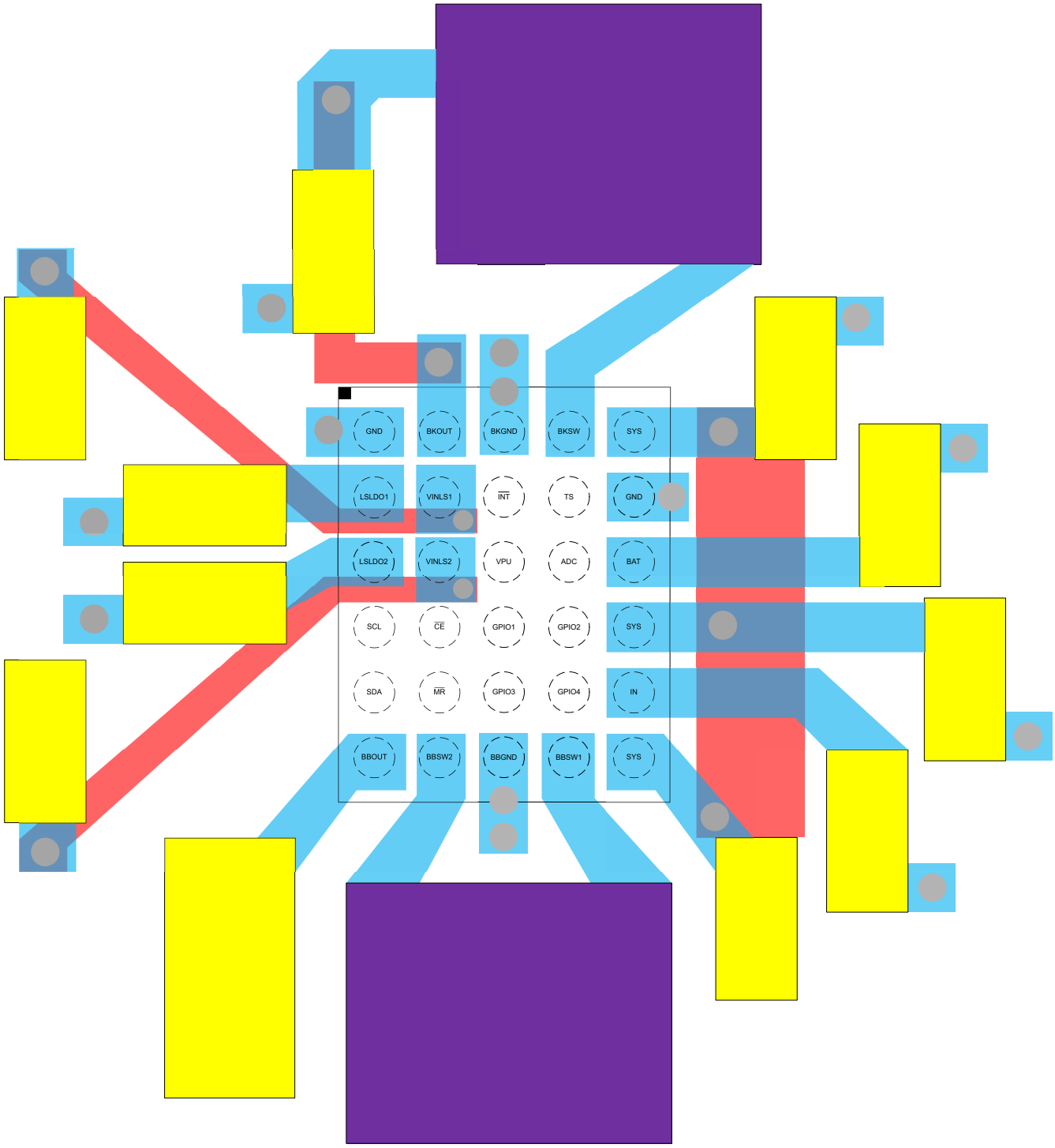


図 10-1. Layout Example (Top View)

11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

11.1 サード・パーティ製品に関する免責事項

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11.3 サポート・リソース

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11.4 Trademarks

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11.5 静電気放電に関する注意事項

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

12 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (October 2024) to Revision A (December 2024)	Page
• Deleted tSLEEP_DGL (deglitch time to enter sleep mode)	15
• Deleted tBATDEPL (deglitch time to open BATFET due to BATDEPL)	15

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ25190YBGR	Active	Production	DSBGA (YBG) | 30	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ25190
BQ25190YBGR.A	Active	Production	DSBGA (YBG) | 30	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ25190

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

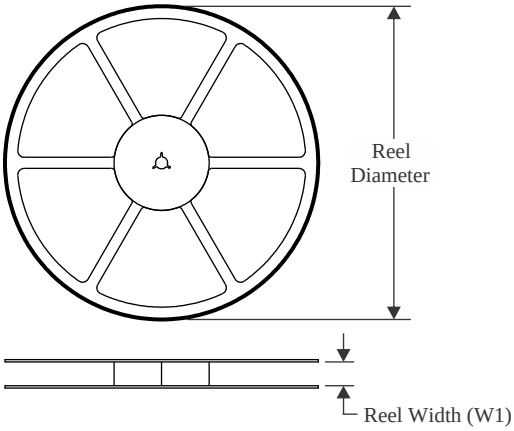
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

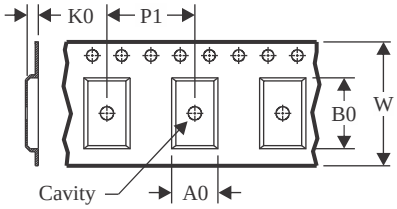
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

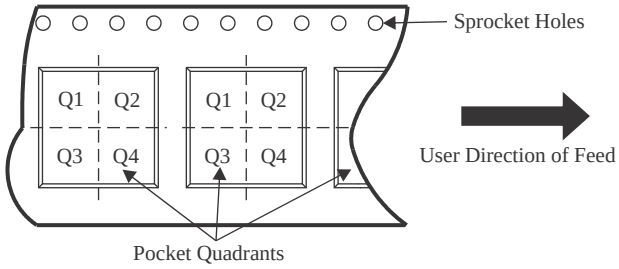


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

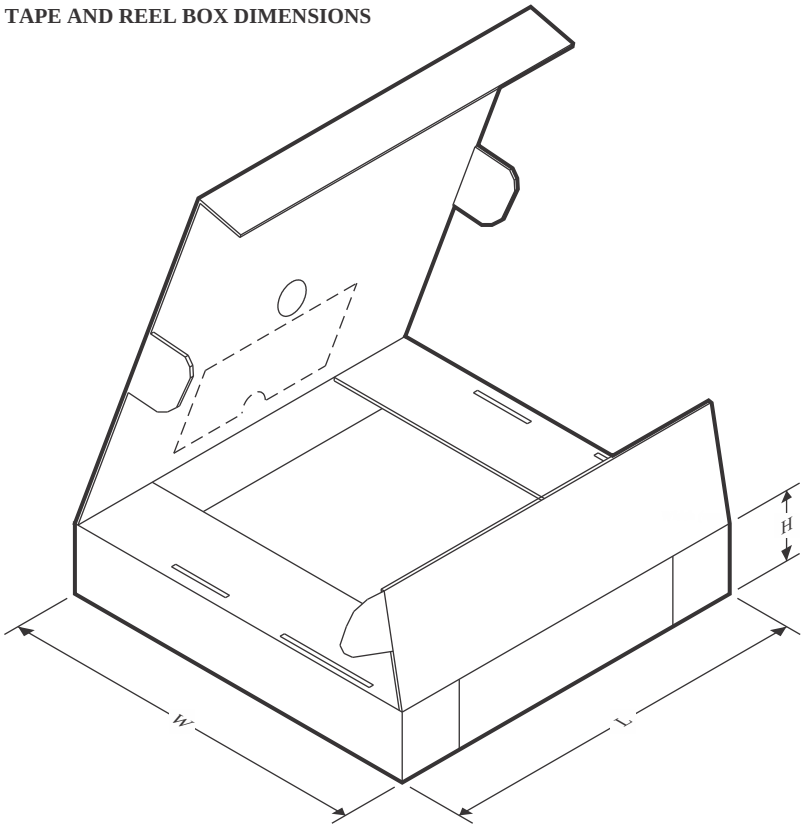
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ25190YBGR	DSBGA	YBG	30	3000	330.0	12.4	2.42	2.92	0.65	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

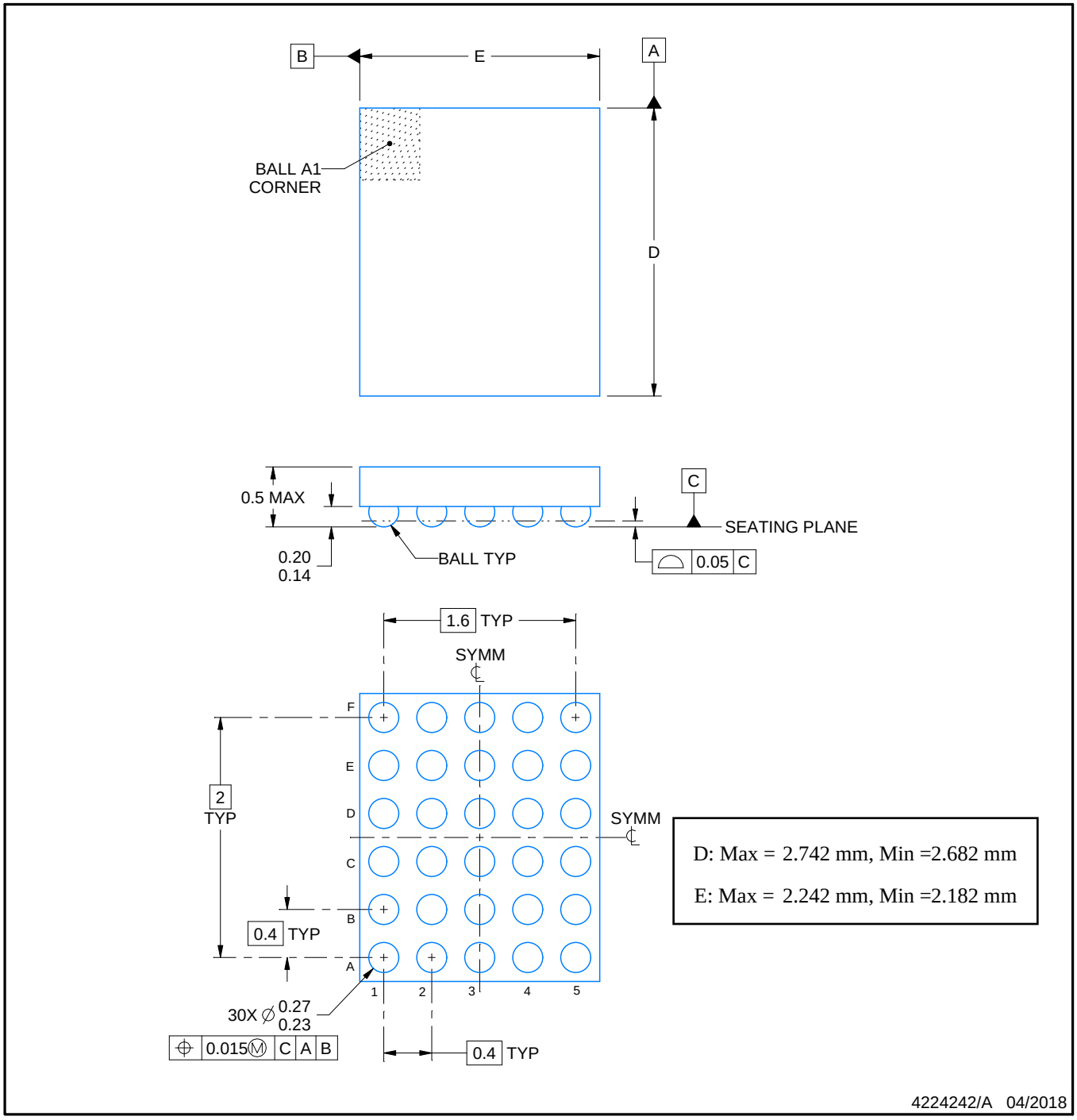
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ25190YBGR	DSBGA	YBG	30	3000	367.0	367.0	35.0

PACKAGE OUTLINE

YBG0030

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

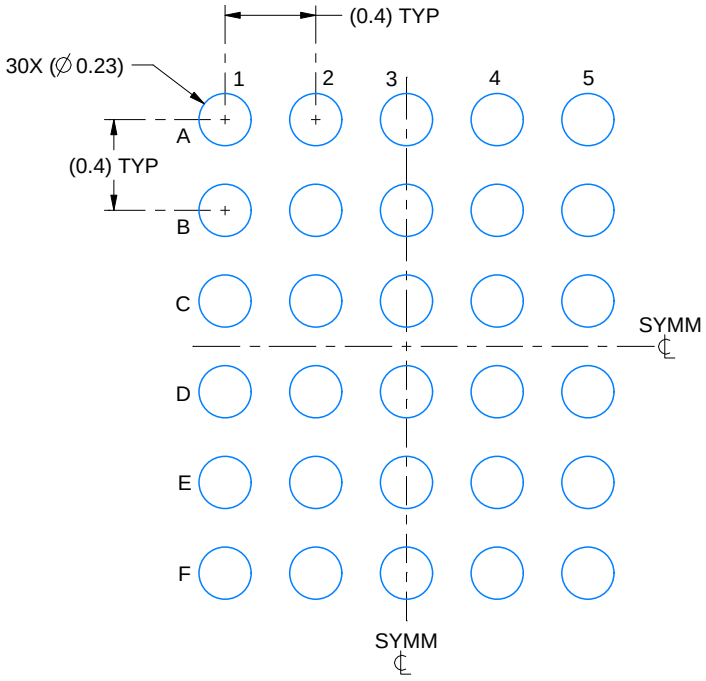
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

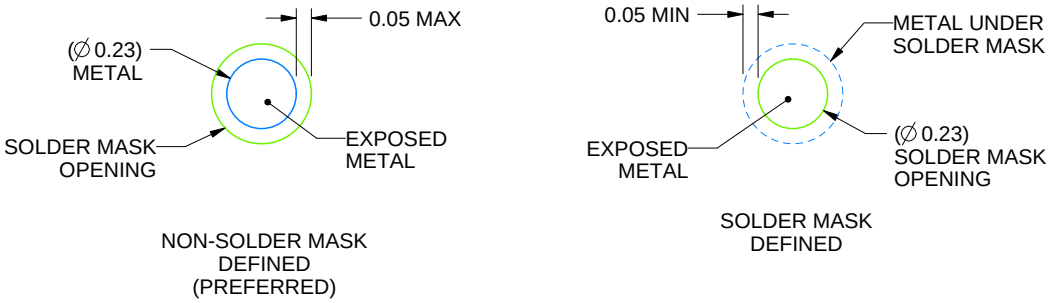
YBG0030

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X

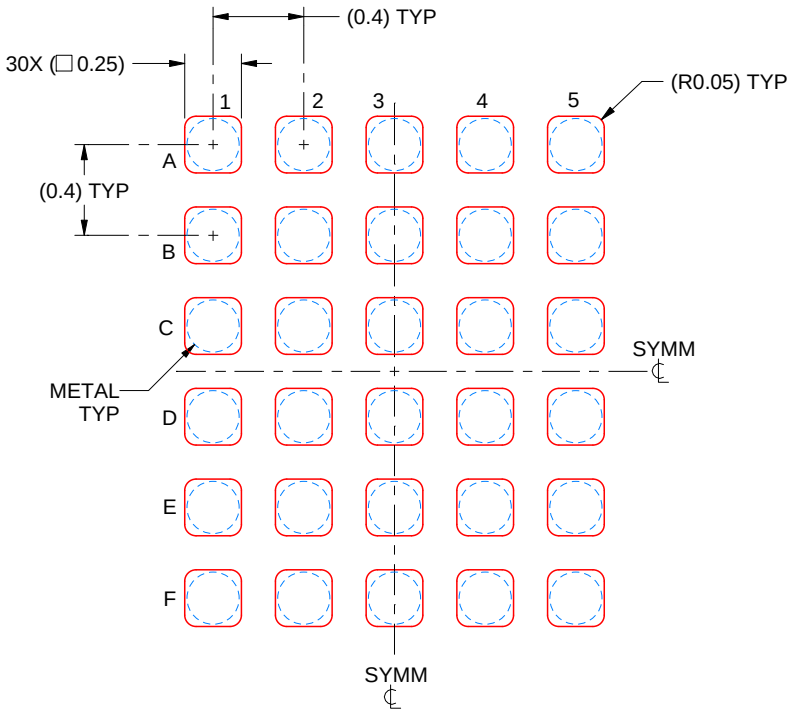


SOLDER MASK DETAILS
NOT TO SCALE

4224242/A 04/2018

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 30X

4224242/A 04/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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最終更新日：2025 年 10 月