BQ25601D I^{2}C 制御、3A シングルセル・バッテリ・チャージャ、高入力電圧およびナロー電圧 DC (NVDC) パワー・パス管理向け、USB チャージャ検出機能付き

1 特長

- 高効率 1.5MHz 同期整流スイッチモード降圧チャージャ
  - 5V 入力から 2A で 92% の充電効率
  - USB 電圧入力 (5V) 用に最適化
  - 軽負荷動作向けに、低消費電力のパルス周波数変調 (PFM) モードを選択可能
- USB On-The-Go (OTG) をサポート
  - 最大 1.2A を出力可能な昇圧コンバータ
  - 1A 出力で 92% の昇圧効率
  - 高精度定電流 (CC) 制限
  - 最大 500µF の容量性負荷に対するソフトスタート
  - 出力短絡保護
  - 軽負荷動作向けに、低消費電力の PFM モードを選択可能
- 1 つの入力で USB 入力および高電圧アダプタに対応
  - 3.9V～13.5V の入力電圧範囲に対応、入力電圧の絶対最大定格 22V
  - USB 2.0、USB 3.0 規格および高電圧アダプタに対応する、プログラム可能な入力電流制限 (100mA の分解能で 100mA～3.2A) (IINDPM)
  - 最高 5.4V までの入力電圧制限による最大電力トラッキング (VINDPM)
  - バッテリ電圧に自動的に追従する VINDPM スレッショルド
  - USB BC1.2、SDP、CDP、DCP および非標準アダプタの自動検出
- 19.5mΩ のバッテリ放電 MOSFET による高いバッテリ放電効率
- ナロー VDC (NVDC) パワー・パス管理
  - バッテリ未接続または深放電状態でも即時オン
  - バッテリ補助モードで理想ダイオード動作
- 出荷モード、ウェークアップ、全システム・リセットに対応する BATFET 制御
- 柔軟性の高い、自律モードおよび I^{2}C モードにより最適なシステム性能を実現
- すべての MOSFET、電流センシング、ループ補償を含む高度な統合
- 17µA の低いバッテリ・リーク電流
- 高い精度
  - ±0.5% の充電電圧レギュレーション
  - 1.5A で ±5% の充電電流レギュレーション
  - 0.9A で ±10% の入力電流レギュレーション
- 安全関連認証：
  - TUV IEC 62368 認証

2 アプリケーション

- スマートフォン
- 携帯型インターネット・デバイスおよびアクセサリ

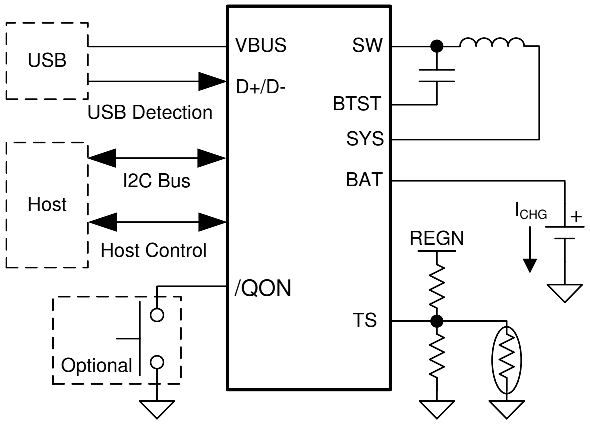
3 説明

BQ25601D デバイスは、シングル・セル・リチウムイオンおよびリチウムポリマー・バッテリ用の高度に統合された 3A スイッチモード・バッテリ充電管理およびシステム・パワー・パス管理デバイスです。パワー・パスのインピーダンスが低いため、スイッチ・モードの動作効率が最適化され、バッテリ充電時間の短縮と、放電フェーズにおけるバッテリ駆動時間の延長を実現できます。I^{2}C シリアル・インターフェイスを使って充電とシステムの設定ができるので、真に柔軟性の高いソリューションとなります。

デバイス情報(1)

部品番号	パッケージ	本体サイズ (公称)
BQ25601D	WQFN (24)	4.00mm × 4.00mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



アプリケーション概略

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (December 2020) to Revision B (February 2022)	Page
• Deleted MAX values for V_{REGN} in セクション 8.5	8

Changes from Revision * (July 2018) to Revision A (December 2020)	Page
• 安全関連認証の特長を追加	1
• データシート全体にわたって WEBENCH を削除	1
• Deleted OVPFET_DIS-1 from I_{BAT} and I_{VBUS_HIZ} test conditions	8
• Added text to the end of last paragraph in Converter Power-Up	19
• Added text to the end of third paragraph in JEITA Guideline Compliance During Charging Mode	23
• Added TS Resistor Network figure in JEITA Guideline Compliance During Charging Mode	23
• Changed fault to timer in fourth paragraph in Charging Safety Timer	25
• Changed 0111 to 0010 in PN[3:0] in REG0B Field Descriptions	45
• Changed >20μF to ≤20μF in last paragraph in Output Capacitor	48

5 概要 (続き)

BQ25601D は、シングル・セル・リチウムイオンおよびリチウムポリマー・バッテリ用の高度に統合された 3.0A スイッチモード・バッテリ充電管理およびシステム・パワー・パス管理デバイスです。広範囲にわたるスマートフォン、タブレットおよび携帯型デバイスについて、高い入力電圧をサポートし、高速な充電を行います。パワー・パスのインピーダンスが低いため、スイッチ・モードの動作効率が最適化され、バッテリ充電時間の短縮と、放電フェーズにおけるバッテリ駆動時間の延長を実現できます。入力電圧および電流レギュレーションにより、バッテリに最大限の充電電力を供給できます。このソリューションは、入力逆電流ブロック FET (RBFET、Q1)、ハイサイド・スイッチング FET (HSFET、Q2)、ローサイド・スイッチング FET (LSFET、Q3)、およびシステムとバッテリの間にあるバッテリ FET (BATFET、Q4) を高度に統合しています。また、ハイサイド・ゲート・ドライブ用のブートストラップ・ダイオードを内蔵し、システム設計の簡素化を実現しています。充電およびシステムの設定に I^{2}C シリアル・インターフェイスを使用できるため、真に柔軟なソリューションとなります。

このデバイスは、標準の USB ホスト・ポート、USB 充電ポート、USB 対応高電圧アダプタなど、幅広い入力ソースをサポートしています。また、内蔵された USB インターフェイスに基づき、デフォルトの入力電流制限を設定します。 デフォルトの入力電流制限を設定するために、デバイスは内蔵の USB インターフェイスを使用するか、または、USB PHY デバイスなどシステム内の検出回路の結果を使用します。このデバイスは、入力電流および電圧のレギュレーションにより、USB 2.0 および USB 3.0 の電力仕様に準拠しています。また、このデバイスは USB On-the-Go (OTG) の動作電力定格仕様にも合致しており、VBUS 上で最大 1.2A までの定電流制限により、5.15V を供給します。

パワー・パス管理により、システムは、バッテリ電圧より少し高い電圧で、最低システム電圧の 3.5V より低下しないようにレギュレートされます (プログラム可能)。この機能により、システムはバッテリが完全に消耗したとき、または取り除かれたときでも、動作を継続できます。入力電流制限または電圧制限に達すると、パワー・パス管理により、充電電流が自動的にゼロまで低下します。システム負荷が引き続き増大すると、パワー・パスはシステムの電力要件が満たされるまで、バッテリを放電します。この補助モードにより、入力ソースの過負荷を防止します。

このデバイスは、ソフトウェア制御なしで、充電サイクルの開始から完了までを実行できます。バッテリ電圧を感知し、プレコンディショニング、定電流、定電圧という 3 フェーズでバッテリを充電します。充電サイクルの終わりに、充電電流があらかじめ設定された制限値を下回り、バッテリ電圧が再充電スレッショルドを上回ると、チャージャは自動的に処理を終了します。十分に充電されたバッテリが再充電スレッショルドを下回ると、チャージャは自動的に次の充電サイクルを開始します。

このチャージャは、バッテリの負温度係数サーミスタ監視、充電安全タイマ、過電圧および過電流保護など、バッテリ充電とシステム運用のための多様な安全機能を備えています。サーマル・レギュレーションにより、接合部温度が 110℃ (プログラム可能) を超えると充電電流が低減されます。STAT 出力により、充電状態とフォルト状態を通知します。その他の安全機能として、充電および昇圧モードでのバッテリ温度センシング、サーマル・レギュレーションおよびサーマル・シャットダウン、入力 UVLO および過電圧保護があります。VBUS_GD ビットは、適切な電源が存在することを示します。フォルトが発生すると、$\overline{\text{INT}}$ 出力により即座にホストに通知します。

また、このデバイスには BATFET イネーブルおよびリセット制御用の $\overline{\text{QON}}$ ピンがあり、低消費電力の出荷モードの終了、または全システム・リセット機能を実行できます。

このデバイスは、24 ピン、4mm×4mm×0.75mm の薄型 WQFN パッケージで供給されます。

6 Device Comparison Table

	BQ25600(D)	**BQ25601(D)**	**BQ25606**
Number of Series Cells	1	1	1
Cell Chemistry	Li-Ion/Li-Polymer	Li-Ion/Li-Polymer	Li-Ion/Li-Polymer
Operation Input Voltage Range (V)	3.9 - 13.5	3.9 - 13.5	3.9 - 13.5
Absolute Max Rating, VBUS (V)	22	22	22
Charge Voltage (V)	3.85 - 4.62	3.85 - 4.62	4.2/4.35/4.4
Charge Current ICHG (A)	3	3	3
Power Path	Yes	Yes	Yes
Discharge Current Rating (A)	6	6	6
I2C / Standalone (I2C Address)	I2C (6BH)	I2C (6BH)	Standalone
USB Detection	BQ25600: PSEL; BQ25600D: D+/D-	BQ25601: PSEL; BQ25601D: D+/D-	D+/D-
BAT Remote Sense	Yes	No	No
Termination Current (A)	60 - 780	60 - 780	5% of ICHG
Precharge Current (A)	60 -780	60 -780	5% of ICHG
Package	WCSP30 - 2x2.4	QFN24 - 4x4	QFN24 - 4x4

7 Pin Configuration and Functions

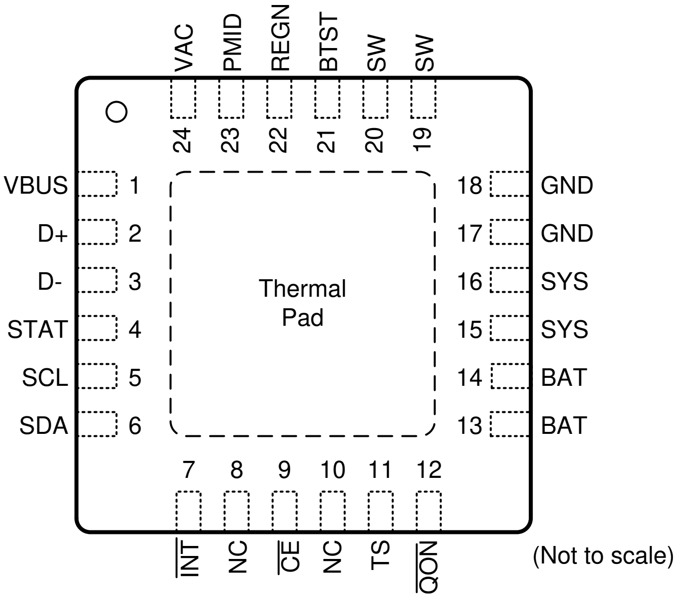


図 7-1. RTW Package 24-Pin WQFN Top View

表 7-1. Pin Functions

Pin		TYPE[1]	DESCRIPTION
NAME	NO.		
BAT	13 14	P	Battery connection point to the positive terminal of the battery pack. The internal BATFET and current sensing is connected between SYS and BAT. Connect a 10 µF close to the BAT pin.
BTST	21	P	PWM high side driver positive supply. Internally, the BTST pin is connected to the cathode of the boost-strap diode. Connect the 0.047-µF bootstrap capacitor from SW to BTST.
$\overline{\text{CE}}$	9	DI	Charge enable pin. When this pin is driven low, battery charging is enabled.
GND	17 18	—	Ground pins.
$\overline{\text{INT}}$	7	DO	Open-drain interrupt Output. Connect the INT to a logic rail through 10-kΩ resistor. The $\overline{\text{INT}}$ pin sends an active low, 256-µs pulse to host to report charger device status and fault.
NC	8 10	—	No Connect. Keep the pins float.
D–	3	AIO	Negative line of the USB data line pair. D+/D– based USB host/charging port detection. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2 and nonstandard adaptors
PMID	23	DO	Connected to the drain of the reverse blocking MOSFET (RBFET) and the drain of HSFET. Put 10 µF ceramic capacitor on PMID to GND.
D+	2	AIO	Positive line of the USB data line pair. D+/D– based USB host/charging port detection. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2 and nonstandard adaptors
$\overline{\text{QON}}$	12	DI	BATFET enable/reset control input. When BATFET is in ship mode, a logic low of $t_{SHIPMODE}$ duration turns on BATFET to exit shipping mode. When VBUS is not pluggeD–in, a logic low of t_{QON_RST} (minimum 8 s) duration resets SYS (system power) by turning BATFET off for t_{BATFET_RST} (minimum 250 ms) and then re-enable BATFET to provide full system power reset. The pin contains an internal pull-up to maintain default high logic.
REGN	22	P	LSFET driver and internal supply output. Internally, REGN is connected to the anode of the boost-strap diode. Connect a 4.7-µF (10-V rating) ceramic capacitor from REGN to GND. The capacitor should be placed close to the IC.
SCL	5	DI	I^2C interface clock. Connect SCL to the logic rail through a 10-kΩ resistor.
SDA	6	DIO	I^2C interface data. Connect SDA to the logic rail through a 10-kΩ resistor.
STAT	4	DO	Open-drain charge status output. Connect the STAT pin to a logic rail via 10-kΩ resistor. The STAT pin indicates charger status. Collect a current limit resister and a LED from a rail to this pin. Charge in progress: LOW Charge complete or charger in SLEEP mode: HIGH Charge suspend (fault response): 1-Hz, 50% duty cycle Pulses This pin can be disabled via EN_ICHG_MON[1:0] register bits.

表 7-1. Pin Functions (continued)

Pin		TYPE[1]	DESCRIPTION
NAME	**NO.**		
SW	19 20	P	Switching node output. Connected to output inductor. Connect the 0.047-μF bootstrap capacitor from SW to BTST.
SYS	15 16	P	Converter output connection point. The internal current sensing network is connected between SYS and BAT. Connect a 20 μF capacitor close to the SYS pin.
TS	11	AI	Temperature qualification voltage input to support JEITA profile. Connect a negative temperature coefficient thermistor. Program temperature window with a resistor divider from REGN to TS to GND. Charge suspends when TS pin is out of range. When TS pin is not used, connect a 10-kΩ resistor from REGN to TS and connect a 10-kΩ resistor from TS to GND. It is recommended to use a 103AT-2 thermistor.
VAC	24	AI	Charge input voltage sense. This pin must be connected to VBUS pin.
VBUS	1	P	Charger input. The internal n-channel reverse block MOSFET (RBFET) is connected between VBUS and PMID pins. Place a 1-uF ceramic capacitor from VBUS to GND close to device.
Thermal Pad	—	P	Thermal pad and ground reference. This pad is ground reference for the device and it is also the thermal pad used to conduct heat from the device. This pad should be tied externally to a ground plane through PCB vias under the pad.

(1) AI = Analog input, AO = Analog Output, AIO = Analog input Output, DI = Digital input, DO = Digital Output, DIO = Digital input Output, P = Power

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage Range (with respect to GND)	VAC, VBUS (converter not switching)(2)	–2	22	V
Voltage Range (with respect to GND)	BTST, PMID (converter not switching)(2)	–0.3	22	V
Voltage Range (with respect to GND)	SW	–2	16	V
Voltage Range (with respect to GND)	BTST to SW	–0.3	7	V
Voltage Range (with respect to GND)	D+, D–	–0.3	7	V
Voltage Range (with respect to GND)	REGN, TS, $\overline{\text{CE}}$, BAT, SYS (converter not switching)	–0.3	7	V
Output Sink Current	STAT		6	mA
Voltage Range (with respect to GND)	SDA, SCL, INT, /QON, STAT	–0.3	7	V
Voltage Range (with respect to GND)	PGND to GND (QFN package only)	–0.3	0.3	V
Output Sink Current	INT		6	mA
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under Absolute maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.

(2) VBUS is specified up to 22 V for a maximum of one hour at room temperature

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{BUS}	Input voltage	3.9		13.5 (1)	V
I_{in}	Input current (VBUS)			3.25	A
I_{SWOP}	Output current (SW)			3.25	A
V_{BATOP}	Battery voltage			4.615	V
I_{BATOP}	Fast charging current			3.0	A
I_{BATOP}	Discharging current (continuous)			6	A
T_A	Operating ambient temperature	–40		85	°C

(1) The inherent switching noise voltage spikes should not exceed the absolute maximum voltage rating on either the BTST or SW pins. A tight layout minimizes switching noise.

8.4 Thermal information

THERMAL METRIC[1]		BQ25601D	UNIT
		RTW (WQFN)	
		24 PinS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	35.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	22.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	12	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

8.5 Electrical Characteristics

$V_{VAC\_UVLOZ} < V_{VAC} < V_{VAC\_OV}$ and $V_{VAC} > V_{BAT} + V_{SLEEP}$, T_J = –40°C to 125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
QUIESCENT CURRENTS						
I_{BAT}	Battery discharge current (BAT, SW, SYS) in buck mode	V_{BAT} = 4.5 V, $V_{BUS} < V_{AC\text{-}UVLOZ}$, leakage between BAT and VBUS, T_J< 85°C			5	µA
I_{BAT}	Battery discharge current (BAT) in buck mode	V_{BAT} = 4.5 V, HIZ Mode and No VBUS, I2C disabled, BATFET Disabled. T_J < 85°C		17	33	µA
I_{BAT}	Battery discharge current (BAT, SW, SYS)	V_{BAT} = 4.5 V, HIZ Mode and No VBUS, I2C Disabled, BATFET Enabled. T_J < 85°C		58	85	µA
I_{VBUS_HIZ}	Input supply current (VBUS) in buck mode	V_{VBUS} = 5 V, High-Z Mode, No battery		37	55	µA
I_{VBUS_HIZ}	Input supply current (VBUS) in buck mode	V_{VBUS} = 12 V, High-Z Mode, No battery		68	93	µA
I_{VBUS}	Input supply current (VBUS) in buck mode	V_{VBUS} = 12 V, $V_{VBUS} > V_{VBAT}$, converter not switching		1.5	3	mA
I_{VBUS}	Input supply current (VBUS) in buck mode	V_{VBUS} > VUVLO, $V_{VBUS} > V_{VBAT}$, converter switching, VBAT = 3.8V, ISYS = 0A		3		mA
I_{BOOST}	Battery Discharge Current in boost mode	V_{BAT} = 4.2 V, boost mode, I_{VBUS} = 0 A, converter switching		3		mA
VBUS, VAC AND BAT PIN POWER-UP						
V_{BUS_OP}	VBUS operating range	V_{VBUS} rising	3.9		13.5	V
V_{VAC_UVLOZ}	VBUS for active I^2C, no battery Sense VAC pin voltage	V_{VAC} rising		3.3	3.6	V
$V_{VAC\_UVLOZ\_HYS}$	I^2C active hysteresis	V_{AC} falling from above V_{VAC_UVLOZ}		300		mV
$V_{VAC\_PRESENT}$	One of the conditions to turn on REGN	V_{VAC} rising		3.65	3.9	V
$V_{VAC\_PRESENT\_HYS}$	One of the conditions to turn on REGN	V_{VAC} falling		500		mV
V_{SLEEP}	Sleep mode falling threshold	$(V_{VAC}–V_{VBAT})$, $V_{BUSMIN\_FALL} \le V_{BAT} \le V_{REG}$, VAC falling	15	60	131	mV
V_{SLEEPZ}	Sleep mode rising threshold	$(V_{VAC}–V_{VBAT})$, $V_{BUSMIN\_FALL} \le V_{BAT} \le V_{REG}$, VAC rising	115	220	340	mV

8.5 Electrical Characteristics (continued)

$V_{VAC\_UVLOZ} < V_{VAC} < V_{VAC\_OV}$ and $V_{VAC} > V_{BAT} + V_{SLEEP}$, T_J = –40°C to 125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{VAC\_OV\_RISE}$	VAC 6.5-V Overvoltage rising threshold	VAC rising; OVP (REG06[7:6]) = '01'	6.1	6.4	6.7	V
$V_{VAC\_OV\_RISE}$	VAC 10.5-V Overvoltage rising threshold	VAC rising, OVP (REG06[7:6]) = '10'	10.35	10.9	11.5	V
$V_{VAC\_OV\_RISE}$	VAC 14-V Overvoltage rising threshold	VAC rising, OVP (REG06[7:6]) = '11'	13.5	14.2	14.85	V
$V_{VAC\_OV\_HYS}$	VAC 6.5-V Overvoltage hysteresis	VAC falling, OVP (REG06[7:6]) = '01'		320		mV
$V_{VAC\_OV\_HYS}$	VAC 10.5-V Overvoltage hysteresis	VAC falling, OVP (REG06[7:6]) = '10'		250		mV
$V_{VAC\_OV\_HYS}$	VAC 14-V Overvoltage hysteresis	VAC falling, OVP (REG06[7:6]) = '11'		300		mV
V_{BAT_UVLOZ}	BAT for active I^2C, no adapter	V_{BAT} rising	2.5			V
$V_{BAT\_DPL\_FALL}$	Battery Depletion Threshold	V_{BAT} falling	2.2		2.6	V
$V_{BAT\_DPL\_RISE}$	Battery Depletion Threshold	V_{BAT} rising	2.34		2.86	V
$V_{BAT\_DPL\_HYST}$	Battery Depletion rising hysteresis	V_{BAT} rising		180		mV
V_{BUSMIN_FALL}	Bad adapter detection falling threshold	V_{BUS} falling	3.75	3.9	4.0	V
V_{BUSMIN_HYST}	Bad adapter detection hysteresis			80		mV
I_{BADSRC}	Bad adapter detection current source	Sink current from VBUS to GND		30		mA
POWER-PATH						
V_{SYS_MIN}	System regulation voltage	V_{VBAT} < SYS_MIN[2:0] = 101, BATFET Disabled (REG07[5] = 1)	3.5	3.68		V
V_{SYS}	System Regulation Voltage	I_{SYS} = 0 A, $V_{VBAT} > V_{SYSMIN}$, V_{VBAT} = 4.400 V, BATFET disabled (REG07[5] = 1)		V_{BAT} + 50 mV		V
V_{SYS_MAX}	Maximum DC system voltage output	I_{SYS} = 0 A, , Q4 off, $V_{VBAT} \leq$ 4.400 V, $V_{VBAT} > V_{SYSMIN}$ = 3.5V	4.4	4.45	4.48	V
$R_{ON(RBFET)}$	Top reverse blocking MOSFET on-resistance between VBUS and PMID - Q1	-40°C≤ T_A ≤ 125°C		45		mΩ
$R_{ON(HSFET)}$	Top switching MOSFET on-resistance between PMID and SW - Q2	V_{REGN} = 5 V , -40°C≤ T_A ≤ 125°C		62		mΩ
$R_{ON(LSFET)}$	Bottom switching MOSFET on-resistance between SW and GND - Q3	V_{REGN} = 5 V , -40°C≤ T_A ≤ 125°C		71		mΩ
V_{FWD}	BATFET forward voltage in supplement mode			30		mV
$R_{ON(BAT\text{-}SYS)}$	SYS-BAT MOSFET on-resistance	QFN package, Measured from BAT to SYS, V_{BAT} = 4.2V, T_J = 25°C		19.5	24	mΩ
$R_{ON(BAT\text{-}SYS)}$	SYS-BAT MOSFET on-resistance	QFN package, Measured from BAT to SYS, V_{BAT} = 4.2V, T_J = –40 - 125°C		19.5	30	mΩ
BATTERY CHARGER						
V_{BATREG_RANGE}	Charge voltage program range		3.847		4.615	V
V_{BATREG_STEP}	Charge voltage step			32		mV

8.5 Electrical Characteristics (continued)

$V_{VAC\_UVLOZ} < V_{VAC} < V_{VAC\_OV}$ and $V_{VAC} > V_{BAT} + V_{SLEEP}$, T_J = –40°C to 125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BATREG}	Charge voltage setting	VREG (REG04[7:3]) = 4.20 V (01011), V, –40 ≤ T_J ≤ 85°C	4.178	4.200	4.220	
		VREG (REG04[7:3]) = 4.343 V (01111), V, –40 ≤ T_J ≤ 85°C	4.321	4.343	4.365	V
		VREG (REG04[7:3]) = 4.391 V (10001), V, –40 ≤ T_J ≤ 85°C	4.373	4.391	4.407	V
$I_{CHG\_REG\_RANGE}$	Charge current regulation range		0		3000	mA
$I_{CHG\_REG\_STEP}$	Charge current regulation step			60		mA
I_{CHG_REG}	Charge current regulation setting	I_{CHG} = 240 mA, V_{VBAT} = 3.1V or V_{VBAT} = 3.8 V	0.216	0.24	0.264	A
$I_{CHG\_REG\_ACC}$	Charge current regulation accuracy	I_{CHG} = 240 mA, V_{VBAT} = 3.1 V or V_{VBAT} = 3.8 V	–10%		10%	
I_{CHG_REG}	Charge current regulation setting	I_{CHG} = 720 mA, V_{VBAT} = 3.1 V or V_{VBAT} = 3.8 V	0.685	0.720	0.761	A
I_{CHG_REG}	Charge current regulation accuracy	I_{CHG_REG} = 720 mA, V_{BAT} = 3.1 V or V_{BAT} = 3.8 V	-5%		6%	
I_{CHG_REG}	Charge current regulation setting	I_{CHG} = 1.38 A, V_{VBAT} = 3.1 V or V_{VBAT} = 3.8 V	1.311	1.380	1.449	A
$I_{CHG\_REG\_ACC}$	Charge current regulation accuracy	I_{CHG} = 720 mA or I_{CHG} = 1.38 A, V_{VBAT} = 3.1 V or V_{VBAT} = 3.8 V	–5%		5%	
$V_{BATLOWV\_FALL}$	Battery LOWV falling threshold	I_{CHG} = 240 mA	2.7	2.8	2.9	V
$V_{BATLOWV\_RISE}$	Battery LOWV rising threshold	Pre-charge to fast charge	3.0	3.12	3.24	V
I_{PRECHG}	Precharge current regulation	IPRECHG[3:0] = '0010' = 180 mA	153	171	189	mA
I_{PRECHG_ACC}	Precharge current regulation accuracy	IPRECHG[3:0] = '0010' = 180 mA	–15%		5%	
I_{TERM}	Termination current regulation	I_{CHG} > 780 mA, ITERM[3:0] = '0010' = 180 mA, V_{VBAT} = 4.208 V	150	180	216	mA
I_{TERM_ACC}	Termination current regulation accuracy	I_{CHG} > 780 mA, , ITERM[3:0] = '0010' = 180 mA, V_{VBAT} = 4.208 V	-16.7%		20%	
I_{TERM}	Termination current regulation	I_{CHG} ≤ 780 mA, , ITERM[3:0] = '0010' = 180 mA	162	180	192	mA
I_{TERM_ACC}	Termination current regulation accuracy	I_{CHG} ≤ 780 mA, , ITERM[3:0] = '0010' = 180 mA	-10%		10%	
I_{TERM}	Termination current regulation	I_{CHG} = 600 mA, ITERM[3:0] = '0000' = 60 mA, V_{VBAT} = 4.208 V	45	60	85	mA
I_{TERM_ACC}	Termination current regulation accuracy	I_{CHG} = 600 mA, ITERM[3:0] = '0000' = 60 mA, V_{VBAT} = 4.208 V	-25%		42%	
V_{SHORT}	Battery short voltage	V_{VBAT} falling	1.85	2	2.15	V
V_{SHORTZ}	Battery short voltage	V_{VBAT} rising	2.15	2.25	2.35	V
I_{SHORT}	Battery short current	$V_{VBAT} < V_{SHORTZ}$	70	90	110	mA
V_{RECHG}	Recharge Threshold below V_{BAT_REG}	V_{BAT} falling, REG04[0] = 0	90	120	150	mV
V_{RECHG}	Recharge Threshold below V_{BAT_REG}	V_{BAT} falling, REG04[0] = 1	200	230	265	mV
$I_{SYSLOAD}$	System discharge load current	V_{SYS} = 4.2 V		30		mA
INPUT VOLTAGE AND CURRENT REGULATION						
V_{INDPM}	Input voltage regulation limit	V_{INDPM} (REG06[3:0] = 0000) = 3.9 V	3.78	3.95	4.1	V
V_{INDPM_ACC}	Input voltage regulation accuracy		–3%		5%	
V_{INDPM}	Input voltage regulation limit	V_{INDPM} (REG06[3:0] = 0110) = 4.4 V	4.268	4.4	4.532	V

8.5 Electrical Characteristics (continued)

$V_{VAC\_UVLOZ} < V_{VAC} < V_{VAC\_OV}$ and $V_{VAC} > V_{BAT} + V_{SLEEP}$, T_J = –40°C to 125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{INDPM_ACC}	Input voltage regulation accuracy		–3%		3%	
V_{DPM_VBAT}	Input voltage regulation limit tracking VBAT	VINDPM = 3.9V, VDPM_VBAT_TRACK = 300mV, VBAT = 4.0V	4.171	4.3	4.43	V
$V_{DPM\_VBAT\_ACC}$	Input voltage regulation accuracy tracking VBAT		–3%		3%	
I_{INDPM}	USB input current regulation limit	V_{VBUS} = 5 V, current pulled from SW, I_{INDPM} (REG[4:0] = 00100) = 500 mA, –40 ≤ T_J ≤ 85°C	450		500	mA
		V_{VBUS} = 5 V, current pulled from SW, IINDPM (REG[4:0] = 01000) = 900 mA, –40 ≤ T_J ≤ 85°C	750		900	mA
		V_{VBUS} = 5 V, current pulled from SW, IINDPM (REG[4:0] = 01110) = 1.5 A, –40 ≤ T_J ≤ 85°C	1.3		1.5	A
I_{IN_START}	Input current limit during system start-up sequence			200		mA
BAT PIN OVERVOLTAGE PROTECTION						
V_{BATOVP_RISE}	Battery overvoltage threshold	V_{BAT} rising, as percentage of V_{BAT_REG}	103%	104%	105%	
V_{BATOVP_FALL}	Battery overvoltage threshold	V_{BAT} falling, as percentage of V_{BAT_REG}	101%	102%	103%	
THERMAL REGULATION AND THERMAL SHUTDOWN						
$T_{JUNCTION\_REG}$	Junction Temperature Regulation Threshold	Temperature Increasing, TREG (REG05[1] = 1) = 110℃		110		°C
$T_{JUNCTION\_REG}$	Junction Temperature Regulation Threshold	Temperature Increasing, TREG (REG05[1] = 0) = 90℃		90		°C
T_{SHUT}	Thermal Shutdown Rising Temperature	Temperature Increasing		160		°C
T_{SHUT_HYST}	Thermal Shutdown Hysteresis			30		°C
JEITA Thermistor Comparator (BUCK MODE)						
V_{T1}	T1 (0°C) threshold, Charge suspended T1 below this temperature.	Charger suspends charge. As Percentage to V_{REGN}	72.4%	73.3%	74.2%	
V_{T1}	Falling	As Percentage to V_{REGN}	69%	71.5%	74%	
V_{T2}	T2 (10°C) threshold, Charge back to I_{CHG}/2 and 4.2 V below this temperature	As percentage of V_{REGN}	67.2%	68%	69%	
V_{T2}	Falling	As Percentage to V_{REGN}	66%	66.8%	67.7%	
V_{T3}	T3 (45°C) threshold, charge back to ICHG and 4.05V above this temperature.	Charger suspends charge. As Percentage to V_{REGN}	43.8%	44.7%	45.8%	
V_{T3}	Falling	As Percentage to V_{REGN}	45.1%	45.7%	46.3%	
V_{T5}	T5 (60°C) threshold, charge suspended above this temperature.	As Percentage to V_{REGN}	33.7%	34.2%	35.1%	
V_{T5}	Falling	As Percentage to V_{REGN}	34.5%	35.3%	36.3%	
COLD OR HOT THERMISTER COMPARATOR (BOOST MODE)						
V_{BCOLD}	Cold Temperature Threshold, TS pin Voltage Rising Threshold	As Percentage to V_{REGN} (Approx. -20°C w/ 103AT), T_J = –20°C - 125°C	79.5%	80%	80.5%	
V_{BCOLD}	Falling	T_J = –20°C - 125°C	78.3%	79%	79.7%	

8.5 Electrical Characteristics (continued)

$V_{VAC\_UVLOZ} < V_{VAC} < V_{VAC\_OV}$ and $V_{VAC} > V_{BAT} + V_{SLEEP}$, T_J = –40°C to 125°C and T_J = 25°C for typical values (unless otherwise noted)

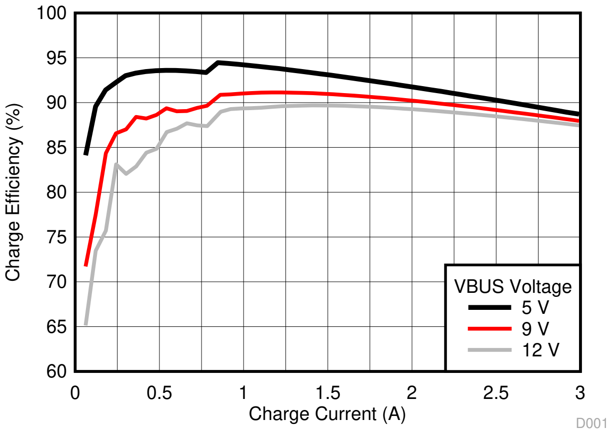
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BHOT}	Hot Temperature Threshold, TS pin Voltage falling Threshold	As Percentage to V_{REGN} (Approx. 60°C w/ 103AT), T_J = –20°C - 125°C	30.2%	31.2%	32.2%	
V_{BHOT}	Rising	T_J = –20°C - 125°C	33.8%	34.4%	34.9%	
CHARGE OVERCURRENT COMPARATOR (CYCLE-BY-CYCLE)						
I_{HSFET_OCP}	HSFET cycle-by-cycle over-current threshold		5.2		8.0	A
I_{BATFET_OCP}	System over load threshold		6.0			A
PWM						
f_{SW}	PWM switching frequency	Oscillator frequency, buck mode	1320	1500	1680	kHz
		Oscillator frequency, boost mode	1150	1412	1660	kHz
D_{MAX}	Maximum PWM duty cycle$^{(1)}$			97%		
BOOST MODE OPERATION						
V_{OTG_REG}	Boost mode regulation voltage	V_{VBAT} = 3.8 V, $I_{(PMID)}$ = 0 A, BOOSTV[1:0] = '10' = 5.15 V	4.97	5.126	5.280	V
$V_{OTG\_REG\_ACC}$	Boost mode regulation voltage accuracy	V_{VBAT} = 3.8 V, $I_{(PMID)}$ = 0 A, BOOSTV[1:0] = '10' = 5.15 V	-3%		3%	
$V_{BATLOWV\_OTG}$	Battery voltage exiting boost mode	V_{VBAT} falling, MIN_V_{BAT}_SEL (REG01[0]) = 0	2.6	2.8	2.93	V
		V_{VBAT} rising, MIN_V_{BAT}_SEL (REG01[0]) = 0	2.9	3.0	3.15	V
		V_{VBAT} falling, MIN_V_{BAT}_SEL (REG01[0]) = 1	2.38	2.5	2.6	V
		V_{VBAT} rising, MIN_V_{BAT}_SEL (REG01[0]) = 1	2.7	2.8	2.93	V
I_{OTG}	OTG mode output current	BOOST_LIM (REG02[7]) = 1	1.2	1.4	1.6	A
$I_{OTG\_OCP\_ACC}$	Boost mode RBFET over-current protection accuracy	BOOST_LIM = 0.5 A (REG02[7] = 0)	0.5		0.722	A
V_{OTG_OVP}	OTG overvoltage threshold	Rising threshold	5.55	5.8	6.15	V
REGN LDO						
V_{REGN}	REGN LDO output voltage	V_{VBUS} = 9V, I_{REGN} = 40mA	5.6	6		V
V_{REGN}	REGN LDO output voltage	V_{VBUS} = 5V, I_{REGN} = 20mA	4.6	4.7		V
LOGIC I/O PIN CHARACTERISTICS ($\overline{\text{CE}}$, $\overline{\text{INT}}$, STAT)						
V_{ILO}	Input low threshold				0.4	V
V_{IH}	Input high threshold		1.3			V
I_{BIAS}	High-level leakage current	Pull up rail 1.8 V			1	μA
I2C Interface (SCL, SDA)						
V_{IH}	Input high threshold level	Pull up rail 1.8 V	1.3			V
V_{IL}	Input t low threshold level	Pull up rail 1.8 V			0.4	V
V_{OL}	Output low threshold level	Sink current = 5 mA,			0.4	V

(1) Specified by design. Not production tested.

8.6 Timing Requirements

			MIN	NOM	MAX	UNIT
VBUS/BAT POWER UP						
t_{ACOV}	VAC OVP reaction time	VAC rising above ACOV threshold to turn off Q2		200		ns
t_{BADSRC}	Bad adapter detection duration			30		ms
BATTERY CHARGER						
t_{TERM_DGL}	Deglitch time for charge termination			250		ms
t_{RECHG_DGL}	Deglitch time for recharge			250		ms
$t_{SYSOVLD\_DGL}$	System over-current deglitch time to turn off Q4			100		µs
t_{BATOVP}	Battery over-voltage deglitch time to disable charge			1		µs
t_{SAFETY}	Typical Charge Safety Timer Range	CHG_TIMER = 1	8	10	12	hr
t_{TOP_OFF}	Typical Top-Off Timer Range	TOP_OFF_TIMER[1:0] = 10 (30 min)	24	30	36	min
$\overline{\text{QON}}$ TIMING						
$t_{SHIPMODE}$	/QON low time to turn on BATFET and exit ship mode	–10°C ≤ T_J ≤ 60°C	0.9		1.3	s
$t_{QON\_RST\_2}$	$\overline{\text{QON}}$ low time to reset BATFET	–10°C ≤ T_J ≤ 60°C	8		12	s
t_{BATFET_RST}	BATFET off time during full system reset	–10°C ≤ T_J ≤ 60°C	250		400	ms
t_{SM_DLY}	Enter ship mode delay	–10°C ≤ T_J ≤ 60°C	10		15	s
DIGITAL CLOCK AND WATCHDOG TIMER						
t_{WDT}	REG05[4]=1	REGN LDO disabled		40		s
f_{LPDIG}	Digital Low Power Clock	REGN LDO disabled		30		kHz
f_{DIG}	Digital Clock	REGN LDO enabled		500		kHz
f_{SCL}	SCL clock frequency				400	kHz

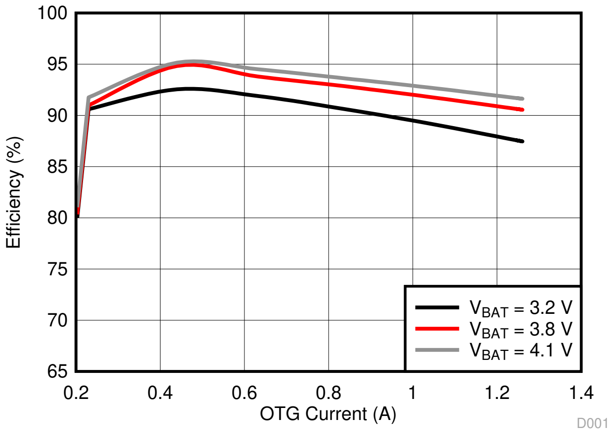
8.7 Typical Characteristics



f_{SW} = 1.5 MHz inductor DCR = 18 mΩ

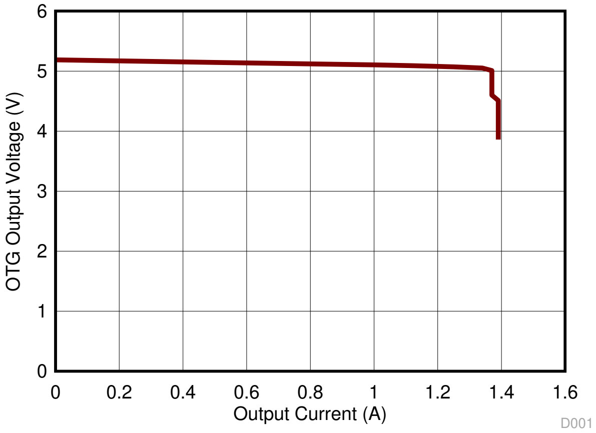
V_{BAT}=3.8V

図 8-1. Charge Efficiency vs. Charge Current



V_{OTG} = 5.15 V inductor DCR = 18 mΩ

図 8-2. Efficiency vs. OTG Current



I_{OTG} = 1.2 A V_{OTG} = 5.15 V

V_{VBAT} = 3.8 V

図 8-3. OTG Output Voltage vs. Output Current

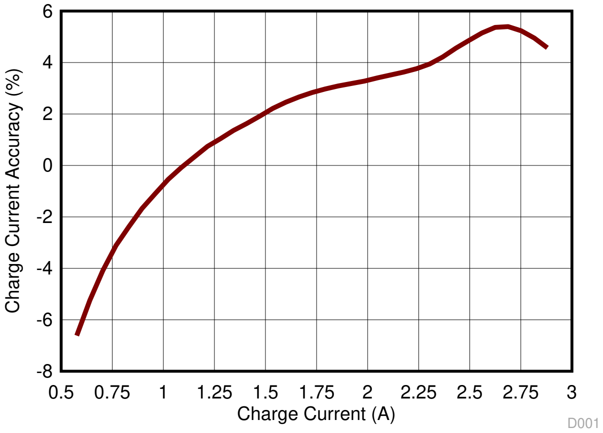


図 8-4. Charge Current Accuracy

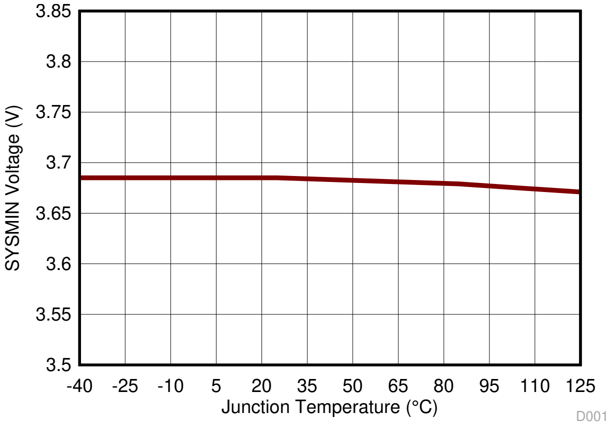


図 8-5. SYSMIN Voltage vs. Junction Temperature

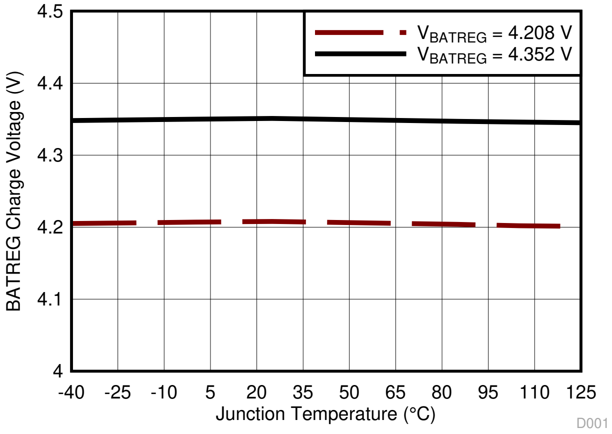


図 8-6. BATREG Charge Voltage vs. Junction Temperature

8.7 Typical Characteristics (continued)

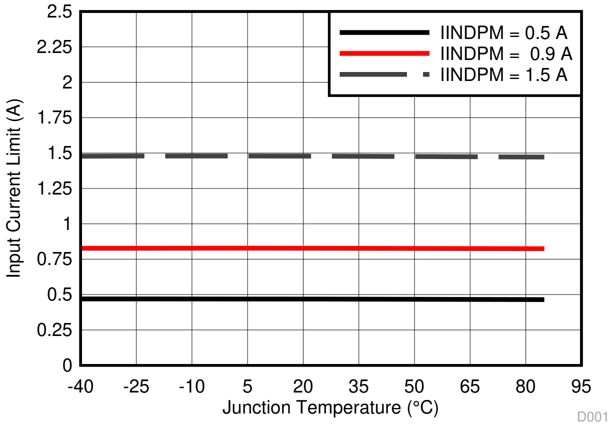


図 8-7. Input Current Limit vs. Junction Temperature

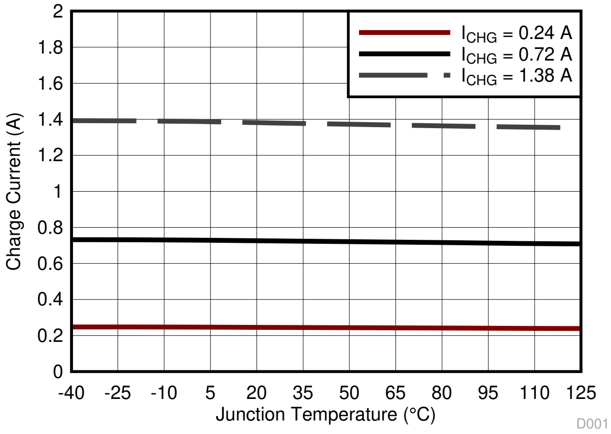


図 8-8. Charge Current vs. Junction Temperature

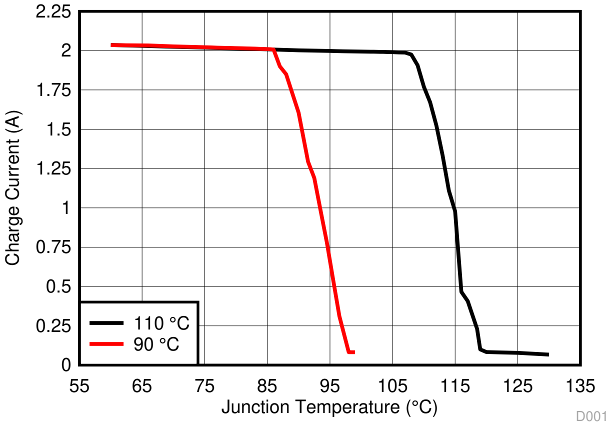


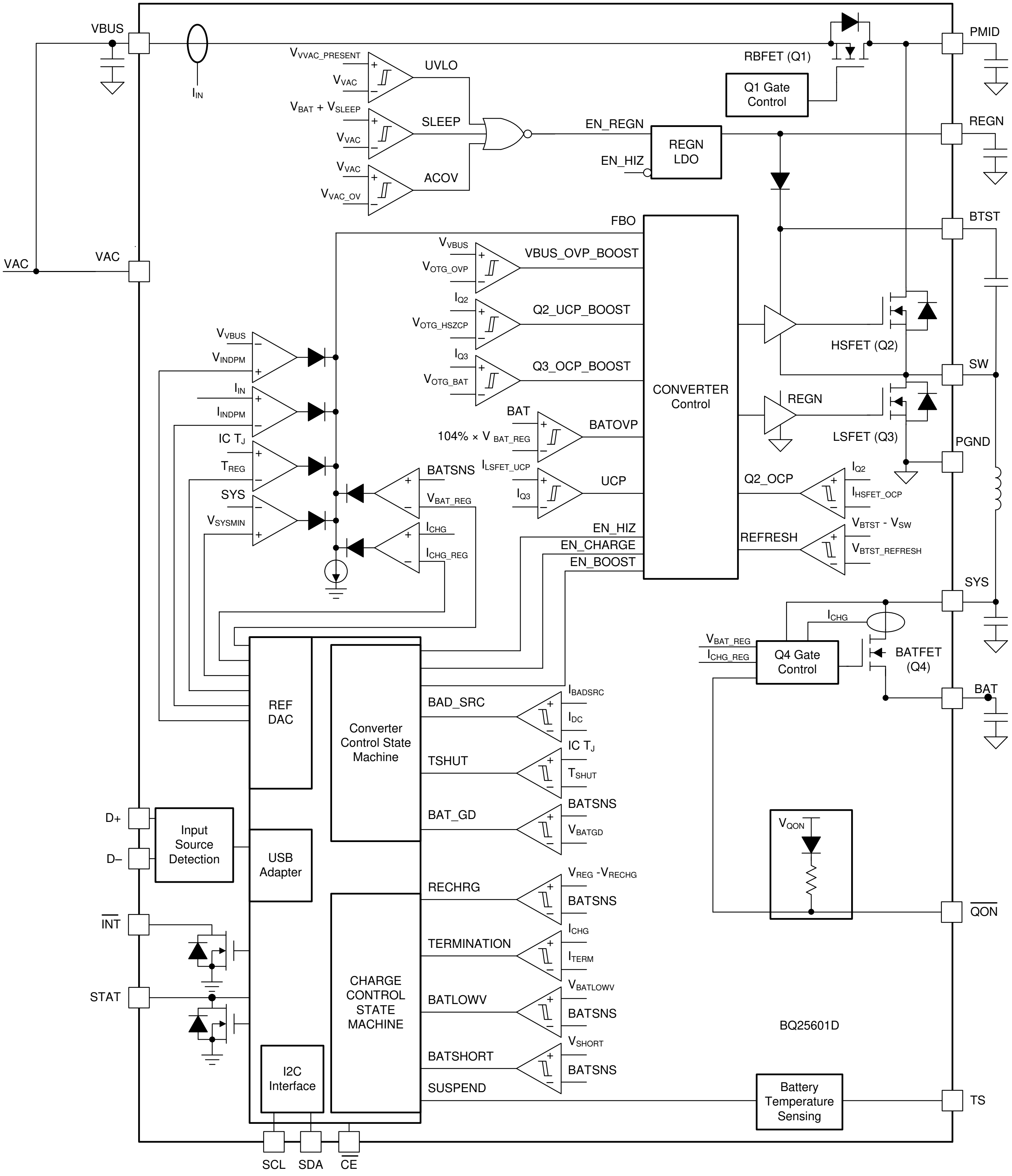
図 8-9. Charge Current vs. Junction Temperature

9 Detailed Description

9.1 Overview

The BQ25601D device is a highly integrated 3.0-A switch-mode battery charger for single cell Li-Ion and Li-polymer battery. It includes the input reverse-blocking FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and battery FET (BATFET, Q4), and bootstrap diode for the high-side gate drive.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Power-On-Reset (POR)

The device powers internal bias circuits from the higher voltage of VBUS and BAT. When VBUS rises above V_{VBUS_UVLOZ} or BAT rises above V_{BAT_UVLOZ} , the sleep comparator, battery depletion comparator and BATFET driver are active. I^2C interface is ready for communication and all the registers are reset to default value. The host can access all the registers after POR.

9.3.2 Device Power Up from Battery without Input Source

If only battery is present and the voltage is above depletion threshold ($V_{BAT\ \_DPL\_RISE}$), the BATFET turns on and connects battery to system. The REGN stays off to minimize the quiescent current. The low RDSON of BATFET and the low quiescent current on BAT minimize the conduction loss and maximize the battery run time.

The device always monitors the discharge current through BATFET (*Supplement Mode*). When the system is overloaded or shorted ($I_{BAT} > I_{BATFET\_OCP}$), the device turns off BATFET immediately and set BATFET_DIS bit to indicate BATFET is disabled until the input source plugs in again or one of the methods described in *BATFET Enable* (*Exit Shipping Mode*) is applied to re-enable BATFET.

9.3.3 Power Up from Input Source

When an input source is plugged in, the device checks the input source voltage to turn on REGN LDO and all the bias circuits. It detects and sets the input current limit before the buck converter is started. The power up sequence from input source is as listed:

1. Power Up REGN LDO
2. Poor Source Qualification
3. Input Source Type Detection is based on D+/D– to set default input current limit (IINDPM) register or input source type.
4. Input Voltage Limit Threshold Setting (VINDPM threshold)
5. Converter Power-up

9.3.3.1 Power Up REGN Regulation

The REGN LDO supplies internal bias circuits as well as the HSFET and LSFET gate drive. The REGN also provides bias rail to TS external resistors. The pull-up rail of STAT can be connected to REGN as well. The REGN is enabled when all the below conditions are valid:

- V_{VAC} above $V_{VAC\_PRESENT}$
- V_{VAC} above $V_{BAT} + V_{SLEEPZ}$ in buck mode or VBUS below $V_{BAT} + V_{SLEEP}$ in boost mode
- After 220-ms delay is completed

If any one of the above conditions is not valid, the device is in high impedance mode (HIZ) with REGN LDO off. The device draws less than IVBUS_HIZ from VBUS during HIZ state. The battery powers up the system when the device is in HIZ.

9.3.3.2 Poor Source Qualification

After REGN LDO powers up, the device confirms the current capability of the input source. The input source must meet both of the following requirements in order to start the buck converter.

- VBUS voltage below V_{VAC_OV}
- VBUS voltage above $V_{VBUSMIN}$ when pulling I_{BADSRC} (typical 30 mA)

Once the input source passes all the conditions above, the status register bit VBUS_GD is set high and the $\overline{\text{INT}}$ pin is pulsed to signal to the host. If the device fails the poor source detection, it repeats poor source qualification every 2 seconds.

9.3.3.3 Input Source Type Detection

After the VBUS_GD bit is set and REGN LDO is powered, the device runs input source detection through D+/D– lines. The BQ25601D follows the USB Battery Charging Specification 1.2 (BC1.2) to detect input source (SDP/DCP) and non-standard adapter through USB D+/D– lines.

After input source type detection is completed, an INT pulse is asserted to the host. in addition, the following registers and pin are changed:

1. Input Current Limit (IINDPM) register is changed to set current limit
2. PG_STAT bit is set
3. VBUS_STAT bit is updated to indicate USB or other input source

The host can over-write IINDPM register to change the input current limit if needed. The charger input current is always limited by the IINDPM register.

9.3.3.3.1 D+/D– Detection Sets Input Current Limit in BQ25601D

The BQ25601D contains a D+/D– based input source detection to set the input current limit at VBUS plug-in. The D+/D– detection includes standard USB BC1.2 and non-standard adapter. When input source is plugged in, the device starts standard USB BC1.2 detections. The USB BC1.2 is capable to identify Standard Downstream Port (SDP) and Dedicated Charging Port (DCP). When the Data Contact Detection (DCD) timer expires, the non-standard adapter detection is applied to set the input current limit. The non-standard detection is used to distinguish vendor specific adapters (Apple and Samsung) based on their unique dividers on the D+/D– pins. If an adapter is detected as DCP, the input current limit is set at 2.4 A. If an adapter is detected as unknown, the input current limit is set at 0.5 A.

表 9-1. Non-Standard Adapter Detection

NON-STANDARD ADAPTER	D+ THRESHOLD	D– THRESHOLD	INPUT CURRENT LIMIT (A)
Divider 1	V_{D+} within V_{2P7_VTH}	V_{D-} within V_{2P0_VTH}	2.1
Divider 2	V_{D+} within V_{1P2_VTH}	V_{D-} within V_{1P2_VTH}	2
Divider 3	V_{D+} within V_{2P0_VTH}	V_{D-} within V_{2P7_VTH}	1
Divider 4	V_{D+} within V_{2P7_VTH}	V_{D-} within V_{2P7_VTH}	2.4

表 9-2. Input Current Limit Setting from D+/D– Detection

D+/D– DETECTION	INPUT CURRENT LIMIT (IINLIM)
USB SDP (USB500)	500 mA
USB DCP	2.4 A
Divider 3	1 A
Divider 1	2.1 A
Divider 4	2.4 A
Divider 2	2 A
Unknown 5-V Adapter	

9.3.3.4 Input Voltage Limit Threshold Setting (VINDPM Threshold)

The device supports wide range of input voltage limit (3.9 V – 5.4V) for USBThe device's VINDPM is set at 4.5V. The device supports dynamic VINDPM trackingsettings which tracks the battery voltage. This function can be enabled via the VDPM_BAT_TRACK[1:0] register bits. When enabled, the actual input voltage limit will be the higher of the VINDPM register and VBAT + VDPM_BAT_TRACK offset.

9.3.3.5 Converter Power-Up

After the input current limit is set, the converter is enabled and the HSFET and LSFET start switching. If battery charging is disabled, BATFET turns off. Otherwise, BATFET stays on to charge the battery.

The device provides soft-start when system rail is ramped up. When the system rail is below 2.2 V, the input current is limited to is to the lower of 200 mA or IINDPM register setting. After the system rises above 2.2 V, the device limits input current to the value set by IINDPM register.

As a battery charger, the device deploys a highly efficient 1.5 MHz step-down switching regulator. The fixed frequency oscillator keeps tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current and temperature, simplifying output filter design.

The device switches to PFM control at light load or when battery is below minimum system voltage setting or charging is disabled. The PFM_DIS bit can be used to prevent PFM operation in either buck or boost configuration. The PFM mod is only enabled when IINDPM is set ≥500 mA. When IINDPM is set ≤400 mA, the PFM mode is disabled.

9.3.4 Boost Mode Operation From Battery

The device supports boost converter operation to deliver power from the battery to other portable devices through USB port. The boost mode output current rating meets the USB On-The-Go 500 mA output requirement. The maximum output current is up to 1.2 A. The boost operation can be enabled if the conditions are valid:

1. BAT above V_{OTG_BAT}
2. VBUS less than BAT+V_{SLEEP} (in sleep mode)
3. Boost mode operation is enabled (OTG_CONFIG bit = 1)
4. Voltage at TS (thermistor) pin is within acceptable range ($V_{BHOT} < V_{TS} < V_{BCOLD}$)
5. After 30-ms delay from boost mode enable

During boost mode, the status register VBUS_STAT bits is set to 111, the VBUS output is 5.15 V and the output current can reach up to 1.2 A , selected through I^2C (BOOST_LIM bit). The boost output is maintained when BAT is above V_{OTG_BAT} threshold.

When OTG is enabled, the device starts up with PFM and later transits to PWM to minimize the overshoot. The PFM_DIS bit can be used to prevent PFM operation in either buck or boost configuration.

9.3.5 Host Mode and Standalone Power Management

9.3.5.1 Host Mode and Default Mode in BQ25601D

The BQ25601D is a host controlled charger, but it can operate in default mode without host management. in default mode, the device can be used as an autonomous charger with no host or while host is in sleep mode. When the charger is in default mode, WATCHDOG_FAULT bit is HIGH. When the charger is in host mode, WATCHDOG_FAULT bit is LOW.

After power-on-reset, the device starts in default mode with watchdog timer expired, or default mode. All the registers are in the default settings.

in default mode, the device keeps charging the battery with default 10-hour fast charging safety timer. At the end of the 10-hour, the charging is stopped and the buck converter continues to operate to supply system load.

Writing a 1 to the WD_RST bit transitions the charger from default mode to host mode. All the device parameters can be programmed by the host. To keep the device in host mode, the host has to reset the watchdog timer by writing 1 to WD_RST bit before the watchdog timer expires (WATCHDOG_FAULT bit is set), or disable watchdog timer by setting WATCHDOG bits = 00.

When the watchdog timer expires (WATCHDOG_FAULT bit = 1), the device returns to default mode and all registers are reset to default values except IINDPM, VINDPM, BATFET_RST_EN, BATFET_DLY, and BATFET_DIS bits.

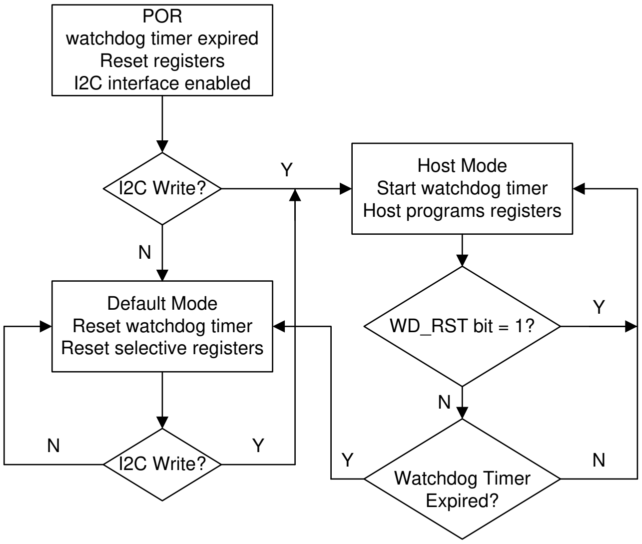


図 9-1. Watchdog Timer Flow Chart

9.3.6 Power Path Management

The device accommodates a wide range of input sources from USB, wall adapter, to car charger. The device provides automatic power path selection to supply the system (SYS) from input source (VBUS), battery (BAT), or both.

9.3.7 Battery Charging Management

The device charges 1-cell Li-Ion battery with up to 3.0-A charge current for high capacity tablet battery. The 19.5-mΩ BATFET improves charging efficiency and minimize the voltage drop during discharging.

9.3.7.1 Autonomous Charging Cycle

With battery charging is enabled (CHG_CONFIG bit = 1 and $\overline{CE}$ pin is LOW), the device autonomously completes a charging cycle without host involvement. The device default charging parameters are listed in 表 9-3. The host can always control the charging operations and optimize the charging parameters by writing to the corresponding registers through I^{2}C.

表 9-3. Charging Parameter Default Setting

DEFAULT MODE	BQ25601D
Charging voltage	4.208V
Charging current	2.048 A
Pre-charge current	180 mA
Termination current	180 mA
Temperature profile	JEITA
Safety timer	10 hours

A new charge cycle starts when the following conditions are valid:

- Converter starts
- Battery charging is enabled (CHG_CONFIG bit = 1 and I_{CHG} register is not 0 mA and $\overline{CE}$ is low)
- No thermistor fault on TS
- No safety timer fault
- BATFET is not forced to turn off (BATFET_DIS bit = 0)

The charger device automatically terminates the charging cycle when the charging current is below termination threshold, battery voltage is above recharge threshold, and device not is in DPM mode or thermal regulation. When a fully charged battery is discharged below recharge threshold (selectable through VRECHG bit), the device automatically starts a new charging cycle. After the charge is done, toggle $\overline{CE}$ pin or CHG_CONFIG bit can initiate a new charging cycle.

The STAT output indicates the charging status: charging (LOW), charging complete or charge disable (HIGH) or charging fault (Blinking). The STAT output can be disabled by setting EN_ICHG_MON bits = 11. in addition, the status register (CHRG_STAT) indicates the different charging phases: 00-charging disable, 01-precharge, 10-fast charge (constant current) and constant voltage mode, 11-charging done. Once a charging cycle is completed, an INT is asserted to notify the host.

9.3.7.2 Battery Charging Profile

The device charges the battery in five phases: battery short, preconditioning, constant current, constant voltage and top-off trickle charging (optional). At the beginning of a charging cycle, the device checks the battery voltage and regulates current and voltage accordingly.

表 9-4. Charging Current Setting

V_{BAT}	CHARGING CURRENT	REGISTER DEFAULT SETTING	CHRG_STAT
< 2.2 V	I_{SHORT}	100 mA	01
2.2 V to 3 V	I_{PRECHG}	180 mA	01
> 3 V	I_{CHG}	2.048 A	10

If the charger device is in DPM regulation or thermal regulation during charging, the actual charging current will be less than the programmed value. in this case, termination is temporarily disabled and the charging safety timer is counted at half the clock rate.

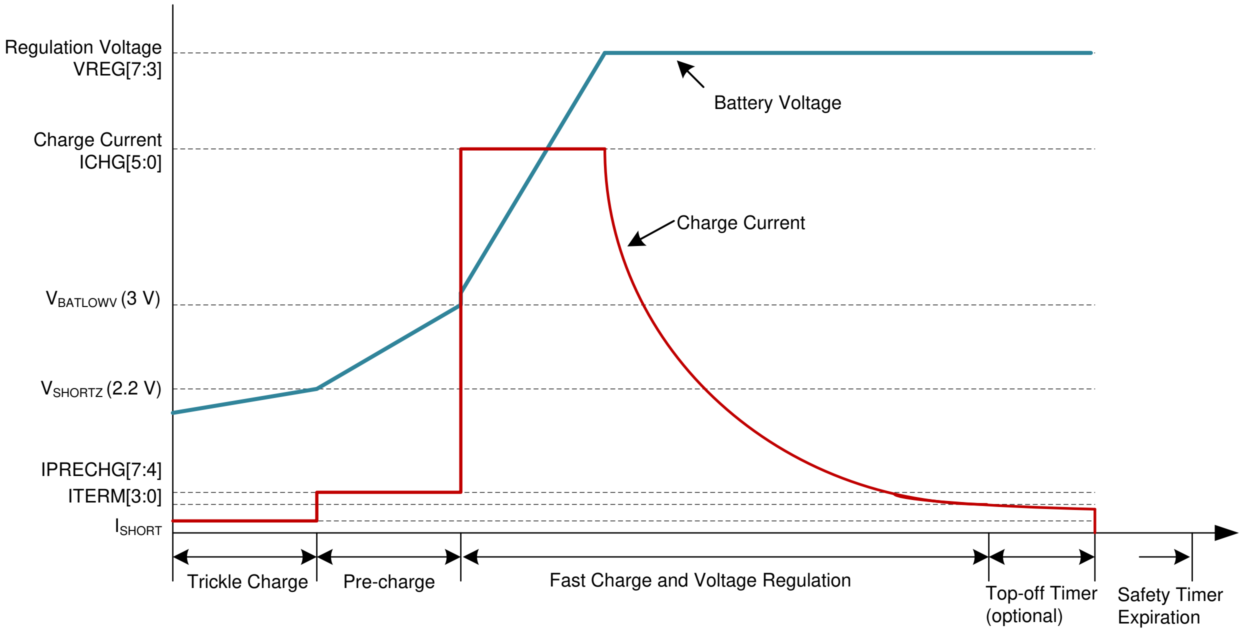


図 9-2. Battery Charging Profile

9.3.7.3 Charging Termination

The device terminates a charge cycle when the battery voltage is above recharge threshold, and the current is below termination current. After the charging cycle is completed, the BATFET turns off. The converter keeps running to power the system, and BATFET can turn on again to engage *Supplement Mode*.

When termination occurs, the status register CHRG_STAT is set to 11, and an INT pulse is asserted to the host. Termination is temporarily disabled when the charger device is in input current, voltage or thermal regulation. Termination can be disabled by writing 0 to EN_TERM bit prior to charge termination.

At low termination currents (25 mA-50 mA), due to the comparator offset, the actual termination current may be 10 mA-20 mA higher than the termination target. in order to compensate for comparator offset, a programmable top-off timer can be applied after termination is detected. The termination timer will follow safety timer constraints, such that if safety timer is suspended, so will the termination timer. Similarly, if safety timer is doubled, so will the termination timer. TOPOFF_ACTIVE bit reports whether the top off timer is active or not. The host can read CHRG_STAT and TOPOFF_ACTIVE to find out the termination status.

Top off timer gets reset at one of the following conditions:

1. Charge disable to enable
2. Termination status low to high
3. REG_RST register bit is set

The top-off timer settings are read in once termination is detected by the charger. Programming a top-off timer value after termination will have no effect unless a recharge cycle is initiated. An INT is asserted to the host when entering top-off timer segment as well as when top-off timer expires.

9.3.7.4 Thermistor Qualification

The charger device provides a single thermistor input for battery temperature monitor.

9.3.7.5 JEITA Guideline Compliance During Charging Mode

To improve the safety of charging Li-ion batteries, JEITA guideline was released on April 20, 2007. The guideline emphasized the importance of avoiding a high charge current and high charge voltage at certain low and high temperature ranges.

To initiate a charge cycle, the voltage on TS pin must be within the VT1 to VT5 thresholds. If TS voltage exceeds the T1-T5 range, the controller suspends charging and waits until the battery temperature is within the T1 to T5 range.

At cool temperature (T1-T2), JEITA recommends the charge current to be reduced to half of the charge current or lower. At warm temperature (T3-T5), JEITA recommends charge voltage less than 4.1 V charge termination is disabled for cool and warm conditions.

The charger provides flexible voltage/current settings beyond the JEITA requirement. The voltage setting at warm temperature (T3-T5) can be VREG or 4.1V (configured by JEITA_VSET). The current setting at cool temperature (T1-T2) can be further reduced to 20% of fast charge current (JEITA_ISET).

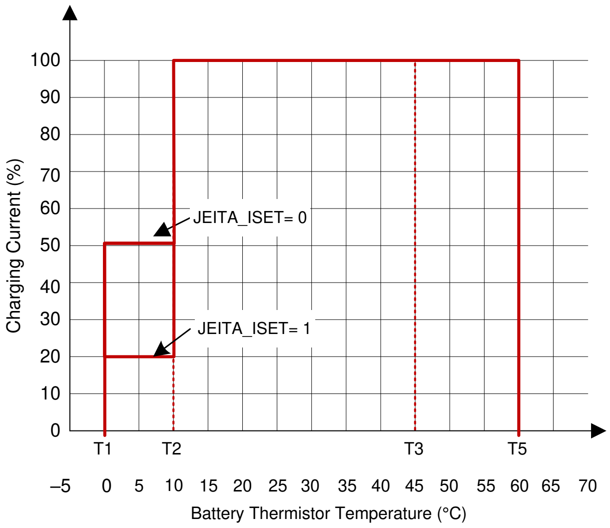


図 9-3. JEITA Profile: Charging Current

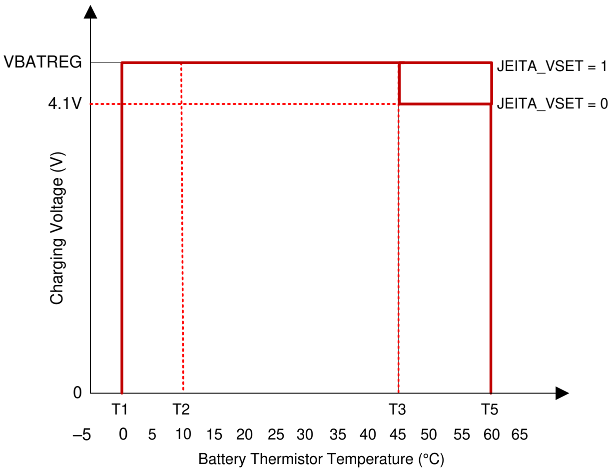


図 9-4. JEITA Profile: Charging Voltage

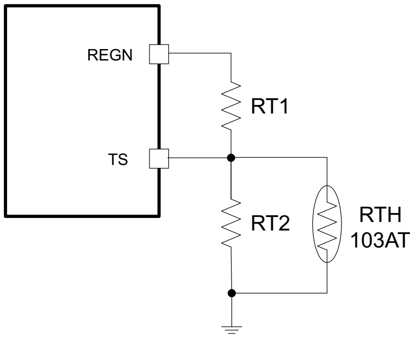


図 9-5. TS Resistor Network

式 1 through 式 2 describe updates to the resistor bias network.

$$RT2 = \frac{V_{REGN} \times RTH_{COLD} \times RTH_{HOT} \times \left(\frac{1}{VT1} - \frac{1}{VT5} \right)}{RTH_{HOT} \times \left(\frac{V_{REGN}}{VT5} - 1 \right) - RTH_{COLD} \times \left(\frac{V_{REGN}}{VT1} - 1 \right)} \quad (1)$$

$$RT1 = \frac{\left(\left(\frac{V_{REGN}}{VT1} \right) - 1 \right)}{\left(\frac{1}{RT2} \right) + \left(\frac{1}{RTH_{COLD}} \right)} \quad (2)$$

Select 0°C to 60°C range for Li-ion or Li-polymer battery:

- RTH_{COLD} = 27.28 KΩ
- RTH_{HOT} = 3.02 KΩ
- RT1 = 5.23 KΩ
- RT2 = 30.9 KΩ

9.3.7.6 Boost Mode Thermistor Monitor During Battery Discharge Mode

For battery protection during boost mode, the device monitors the battery temperature to be within the VBCOLD to VBHOTthresholds. When temperature is outside of the temperature thresholds, the boost mode is suspended. In additional, VBUS_STAT bits are set to 000 and NTC_FAULT is reported. Once temperature returns within thresholds, the boost mode is recovered and NTC_FAULT is cleared.

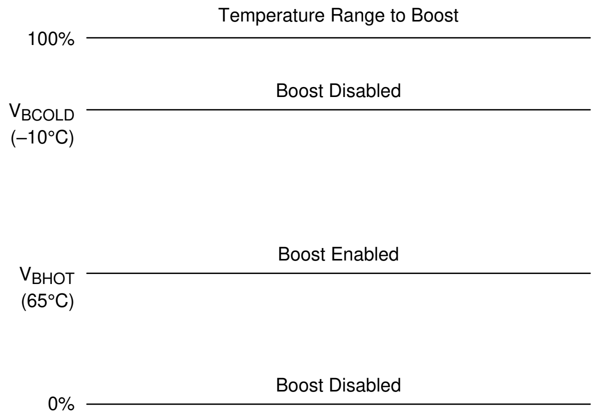


図 9-6. TS Pin Thermistor Sense Threshold in Boost Mode

9.3.7.7 Charging Safety Timer

The device has built-in safety timer to prevent extended charging cycle due to abnormal battery conditions. The safety timer is 2 hours when the battery is below $V_{BATLOWV}$ threshold and 10 hours when the battery is higher than $V_{BATLOWV}$ threshold.

The user can program fast charge safety timer through I^2C (CHG_TIMER bits). When safety timer expires, the fault register CHRG_FAULT bits are set to 11 and an INT is asserted to the host. The safety timer feature can be disabled through I^2C by setting EN_TIMER bit

During input voltage, current, JEITA cool or thermal regulation, the safety timer counts at half clock rate as the actual charge current is likely to be below the register setting. For example, if the charger is in input current regulation (IDPM_STAT = 1) throughout the whole charging cycle, and the safety time is set to 5 hours, the safety timer will expire in 10 hours. This half clock rate feature can be disabled by writing 0 to TMR2X_EN bit.

During the fault, timer is suspended. Once the fault goes away, timer resumes. If user stops the current charging cycle, and start again, timer gets reset (toggle CE pin or CHRG_CONFIG bit).

9.4 Device Functional Modes

9.4.1 Narrow VDC Architecture

The device deploys Narrow VDC architecture (NVDC) with BATFET separating system from battery. The minimum system voltage is set by SYS_Min bits. Even with a fully depleted battery, the system is regulated above the minimum system voltage.

When the battery is below minimum system voltage setting, the BATFET operates in linear mode (LDO mode), and the system is typically 180 mV above the minimum system voltage setting. As the battery voltage rises above the minimum system voltage, BATFET is fully on and the voltage difference between the system and battery is the VDS of BATFET.

When the battery charging is disabled and above minimum system voltage setting or charging is terminated, the system is always regulated at typically 50mV above battery voltage. The status register VSYS_STAT bit goes high when the system is in minimum system voltage regulation.

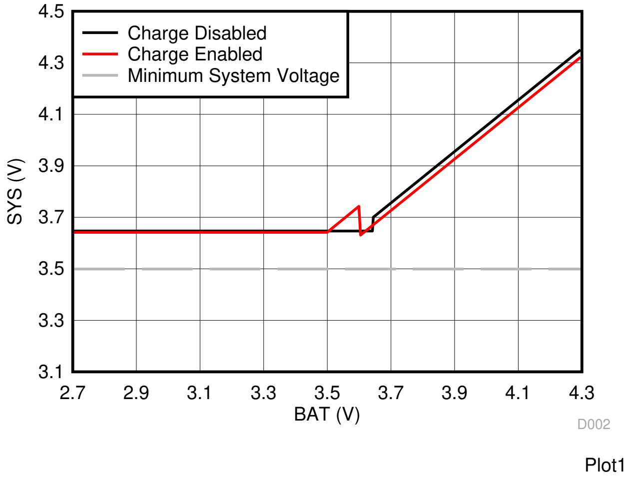


図 9-7. System Voltage vs Battery Voltage

9.4.2 Dynamic Power Management

To meet maximum current limit in USB spec and avoid over loading the adapter, the device features Dynamic Power management (DPM), which continuously monitors the input current and input voltage. When input source is over-loaded, either the current exceeds the input current limit (IIDPM) or the voltage falls below the input voltage limit (VINDPM). The device then reduces the charge current until the input current falls below the input current limit and the input voltage rises above the input voltage limit.

When the charge current is reduced to zero, but the input source is still overloaded, the system voltage starts to drop. Once the system voltage falls below the battery voltage, the device automatically enters the supplement mode where the BATFET turns on and battery starts discharging so that the system is supported from both the input source and battery.

During DPM mode, the status register bits VDPM_STAT (VINDPM) or IDPM_STAT (IINDPM) goes high. 図 9-8 shows the DPM response with 9-V/1.2-A adapter, 3.2-V battery, 2.8-A charge current and 3.5-V minimum system voltage setting.

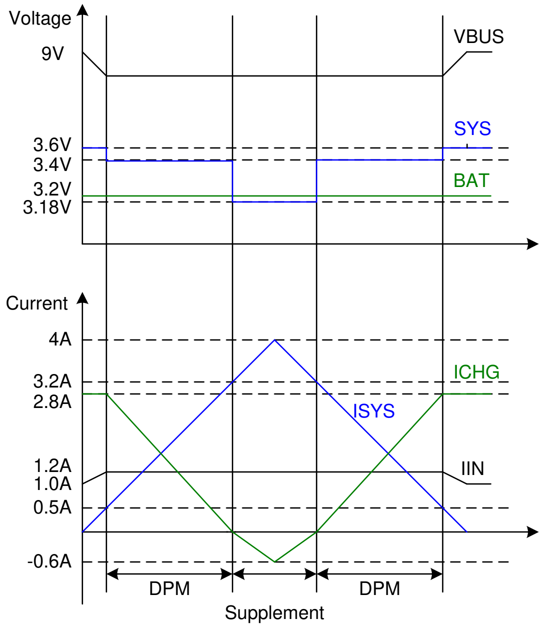


図 9-8. DPM Response

9.4.3 Supplement Mode

When the system voltage falls 180 mV (VBAT > VSYSMin) or 45 mV (VBAT < VSYSMin) below the battery voltage, the BATFET turns on and the BATFET gate is regulated the gate drive of BATFET so that the minimum BATFET VDS stays at 30 mV when the current is low. This prevents oscillation from entering and exiting the supplement mode.

As the discharge current increases, the BATFET gate is regulated with a higher voltage to reduce RDSON until the BATFET is in full conduction. At this point onwards, the BATFET VDS linearly increases with discharge current. 図 9-9 shows the V-I curve of the BATFET gate regulation operation. BATFET turns off to exit supplement mode when the battery is below battery depletion threshold.

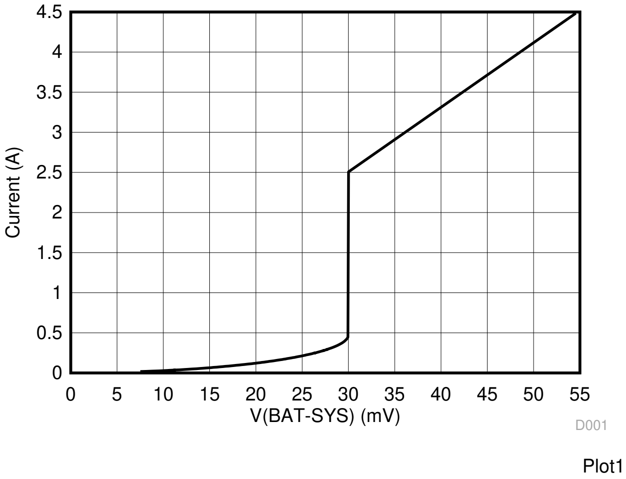


図 9-9. BAFET V-I Curve

9.4.4 Shipping Mode and $\overline{\text{QON}}$ Pin

9.4.4.1 BATFET Disable Mode (Shipping Mode)

To extend battery life and minimize power when system is powered off during system idle, shipping, or storage, the device can turn off BATFET so that the system voltage is zero to minimize the battery leakage current. When the host set BATFET_DIS bit, the charger can turn off BATFET immediately or delay by t_{SM_DLY} as configured by BATFET_DLY bit.

9.4.4.2 BATFET Enable (Exit Shipping Mode)

When the BATFET is disabled (in shipping mode) and indicated by setting BATFET_DIS, one of the following events can enable BATFET to restore system power:

1. Plug in adapter
2. Clear BATFET_DIS bit
3. Set REG_RST bit to reset all registers including BATFET_DIS bit to default (0)
4. A logic high to low transition on $\overline{\text{QON}}$ pin with $t_{SHIPMODE}$ deglitch time to enable BATFET to exit shipping mode

9.4.4.3 BATFET Full System Reset

The BATFET functions as a load switch between battery and system when input source is not pluggeD–in. By changing the state of BATFET from on to off, systems connected to SYS can be effectively forced to have a power-on-reset. The $\overline{\text{QON}}$ pin supports push-button interface to reset system power without host by changing the state of BATFET.

When the $\overline{\text{QON}}$ pin is driven to logic low for t_{QON_RST} while input source is not plugged in and BATFET is enabled (BATFET_DIS = 0), the BATFET is turned off for t_{BATFET_RST} and then it is re-enabled to reset system power. This function can be disabled by setting BATFET_RST_EN bit to 0.

9.4.4.4 $\overline{\text{QON}}$ Pin Operations

The $\overline{\text{QON}}$ pin incorporates two functions to control BATFET.

1. BATFET Enable: A $\overline{\text{QON}}$ logic transition from high to low with longer than $t_{SHIPMODE}$ deglitch turns on BATFET and exit shipping mode. When exiting shipping mode, HIZ is enabled (EN_HIZ = 1) as well. HIZ can be disabled (EN_HIZ = 0) by the host after exiting shipping mode. OTG cannot be enabled (OTG_CONFIG = 1) until HIZ is disabled.
2. BATFET Reset: When $\overline{\text{QON}}$ is driven to logic low by at least t_{QON_RST} while adapter is not plugged in (and BATFET_DIS = 0), the BATFET is turned off for t_{BATFET_RST}. The BATFET is re-enabled after t_{BATFET_RST} duration. This function allows systems connected to SYS to have power-on-reset. This function can be disabled by setting BATFET_RST_EN bit to 0.

図 9-10 shows the sample external configurations for each.

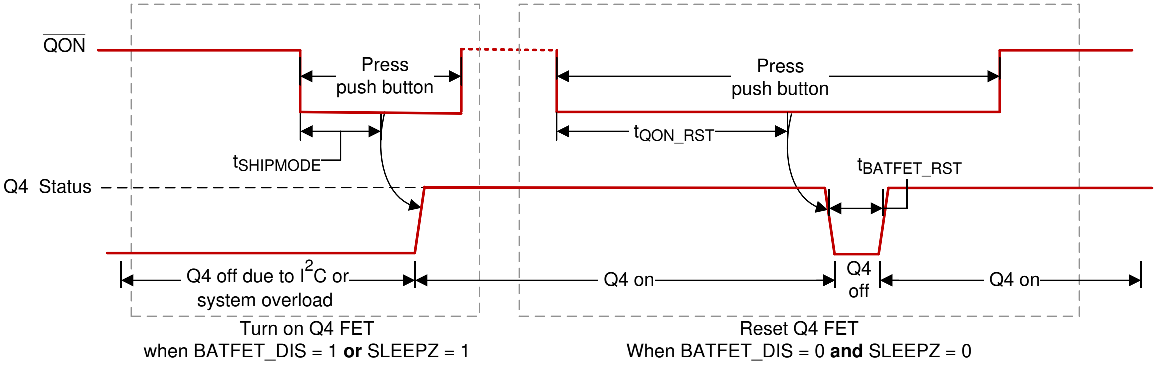


図 9-10. $\overline{\text{QON}}$ Timing

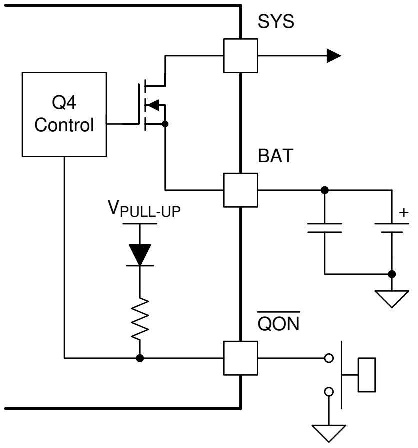


図 9-11. $\overline{\text{QON}}$ Circuit

9.4.5 Status Outputs ($\overline{\text{PG}}$, STAT, $\overline{\text{INT}}$)

9.4.5.1 Power Good Indicator ($\overline{\text{PG}}$Pin PG_STAT Bit)

The PG_STAT bit goes HIGH to indicate a good input source when:

- VBUS above V_{VBUS_UVLO}
- VBUS above battery (not in sleep)
- VBUS below V_{VAC_OV} threshold
- VBUS above $V_{VBUSMin}$ (typical 3.8 V) when I_{BADSRC} (typical 30 mA) current is applied (not a poor source)
- Completed *input Source Type Detection*

9.4.5.2 Charging Status indicator (STAT)

The device indicates charging state on the open drain STAT pin. The STAT pin can drive LED. The STAT pin function can be disabled by setting the EN_ICHG_MON bits = 11.

表 9-5. STAT Pin State

CHARGING STATE	STAT INDICATOR
Charging in progress (including recharge)	LOW
Charging complete	HIGH
Sleep mode, charge disable	HIGH
Charge suspend (input overvoltage, TS fault, timer fault or system overvoltage) Boost Mode suspend (due to TS fault)	Blinking at 1 Hz

9.4.5.3 Interrupt to Host ($\overline{\text{INT}}$)

In some applications, the host does not always monitor the charger operation. The INT pulse notifies the system on the device operation. The following events will generate 256-μs INT pulse.

- USB/adapter source identified (through DPDM detection)
- Good input source detected
  - VBUS above battery (not in sleep)
  - VBUS below V_{VAC_OV} threshold
  - VBUS above $V_{VBUSMin}$ (typical 3.8 V) when I_{BADSRC} (typical 30 mA) current is applied (not a poor source)
- input removed
- Charge Complete
- Any FAULT event in REG09
- VINDPM / IINDPM event detected (maskable)

When a fault occurs, the charger device sends out INT and keeps the fault state in REG09 until the host reads the fault register. Before the host reads REG09 and all the faults are cleared, the charger device would not send any INT upon new faults. To read the current fault status, the host has to read REG09 two times consecutively. The first read reports the pre-existing fault register status and the second read reports the current fault register status.

9.5 Protections

9.5.1 Voltage and Current Monitoring in Converter Operation

The device closely monitors the input and system voltage, as well as internal FET currents for safe buck and boost mode operation.

9.5.1.1 Voltage and Current Monitoring in Buck Mode

9.5.1.1.1 Input Overvoltage (ACOV)

If VBUS voltage exceeds V_{VAC_OV} (programmable via OVP[2:0] bits), the device stops switching immediately.

During input overvoltage event (ACOV), the fault register CHRG_FAULT bits are set to 01. An INT pulse is asserted to the host. The device will automatically resume normal operation once the input voltage drops back below the OVP threshold.

9.5.1.1.2 System Overvoltage Protection (SYSOVP)

The charger device clamps the system voltage during load transient so that the components connect to system would not be damaged due to high voltage. SYSOVP threshold is 350 mV above minimum system regulation voltage when the system is regulate at V_{SYSMIN}. Upon SYSOVP, converter stops switching immediately to clamp the overshoot. The charger provides 30 mA discharge current to bring down the system voltage.

9.5.2 Voltage and Current Monitoring in Boost Mode

The device closely monitors the VBUS voltage, as well as RBFET and LSFET current to ensure safe boost mode operation.

9.5.2.1 VBUS Soft Start

When the boost function is enabled, the device soft-starts boost mode to avoid inrush current.

9.5.2.2 VBUS Output Protection

The device monitors boost output voltage and other conditions to provide output short circuit and overvoltage protection. The Boost build in accurate constant current regulation to allow OTG to adaptive to various types of load. If short circuit is detected on VBUS, the Boost turns off and retry 7 times. If retries are not successful, OTG is disabled with OTG_CONFIG bit cleared. In addition, the BOOST_FAULT bit is set and $\overline{\text{INT}}$ pulse is generated. The BOOST_FAULT bit can be cleared by host by re-enabling boost mode.

9.5.2.3 Boost Mode Overvoltage Protection

When the VBUS voltage rises above regulation target and exceeds VOTG_OVP, the device enters overvoltage protection which stops switching, clears OTG_CONFIG bit and exits boost mode. At Boost overvoltage duration, the fault register bit (BOOST_FAULT) is set high to indicate fault in boost operation. An INT is also asserted to the host.

9.5.3 Thermal Regulation and Thermal Shutdown

9.5.3.1 Thermal Protection in Buck Mode

The BQ25601D monitors the internal junction temperature T_J to avoid overheat the chip and limits the IC surface temperature in buck mode. When the internal junction temperature exceeds thermal regulation limit (110°C), the device lowers down the charge current. During thermal regulation, the actual charging current is usually below the programmed battery charging current. Therefore, termination is disabled, the safety timer runs at half the clock rate, and the status register THERM_STAT bit goes high.

Additionally, the device has thermal shutdown to turn off the converter and BATFET when IC surface temperature exceeds T_{SHUT}(160°C). The fault register CHRG_FAULT is set to 1 and an $\overline{\text{INT}}$ is asserted to the host. The BATFET and converter is enabled to recover when IC temperature is T_{SHUT_HYS} (30°C) below T_{SHUT}(160°C).

9.5.3.2 Thermal Protection in Boost Mode

The device monitors the internal junction temperature to provide thermal shutdown during boost mode. When IC junction temperature exceeds T_{SHUT} (160°C), the boost mode is disabled by setting OTG_CONFIG bit low and BATFET is turned off. When IC junction temperature is below T_{SHUT}(160°C) - T_{SHUT_HYS} (30°C), the BATFET is enabled automatically to allow system to restore and the host can re-enable OTG_CONFIG bit to recover.

9.5.4 Battery Protection

9.5.4.1 Battery Overvoltage Protection (BATOVP)

The battery overvoltage limit is clamped at 4% above the battery regulation voltage. When battery over voltage occurs, the charger device immediately disables charging. The fault register BAT_FAULT bit goes high and an INT is asserted to the host.

9.5.4.2 Battery Over-Discharge Protection

When battery is discharged below $V_{BAT\_DPL\_FALL}$, the BATFET is turned off to protect battery from over discharge. To recover from over-discharge latch-off, an input source plug-in is required at VBUS. The battery is charged with I_{SHORT} (typically 100 mA) current when the VBAT < VSHORT, or precharge current as set in IPRECHG register when the battery voltage is between V_{SHORTZ} and V_{BAT_LOWV}.

9.5.4.3 System Over-Current Protection

When the system is shorted or significantly overloaded (IBAT > IBATOP) and the current exceeds BATFET overcurrent limit, the BATFET latches off. Section BATFET Enable (Exit Shipping Mode) can reset the latch-off condition and turn on BATFET.

9.6 Programming

9.6.1 Serial Interface

The device uses I^{2}C compatible interface for flexible charging parameter programming and instantaneous device status reporting. I^{2}CTM is a bi-directional 2-wire serial interface developed by Philips Semiconductor (now NXP Semiconductors). Only two bus lines are required: a serial data line (SDA) and a serial clock line (SCL). Devices can be considered as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

The device operates as a slave device with address 6BH, receiving control inputs from the master device like micro controller or a digital signal processor through REG00-REG0B. Register read beyond REG0B (0x0B) returns 0xFF. The I^{2}C interface supports both standard mode (up to 100 kbits), and fast mode (up to 400 kbits). connecting to the positive supply voltage via a current source or pull-up resistor. When the bus is free, both lines are HIGH. The SDA and SCL pins are open drain.

9.6.1.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

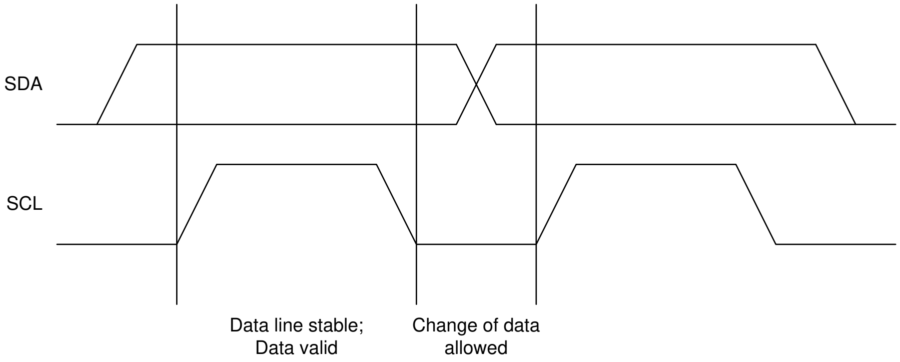


図 9-12. Bit Transfer on the I^{2}C Bus

9.6.1.2 START and STOP Conditions

All transactions begin with a START (S) and can be terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCl is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition. START and STOP conditions are always generated by the master. The bus is considered busy after the START condition, and free after the STOP condition.

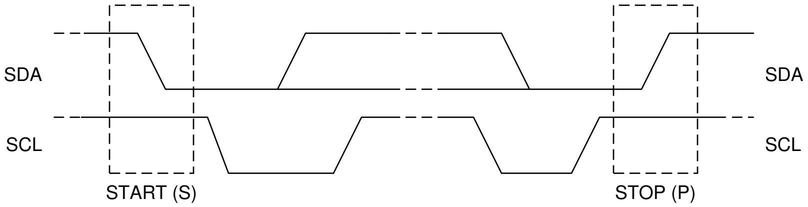


図 9-13. TS START and STOP Conditions

9.6.1.3 Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the mAster into a wait state (clock stretching). Data transfer then continues when the slave is ready for another byte of data and release the clock line SCL.

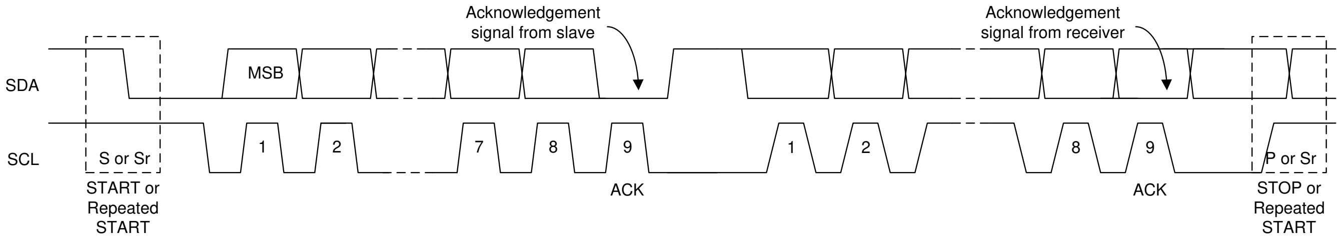


図 9-14. Data Transfer on the I^2C Bus

9.6.1.4 Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge ninth clock pulse, are generated by the master. The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during the ninth clock pulse, this is the Not Acknowledge signal. The master can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

9.6.1.5 Slave Address and Data Direction Bit

After the START, a slave address is sent. This address is 7 bits long followed by the eighth bit as a data direction bit (bit R/W). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ).

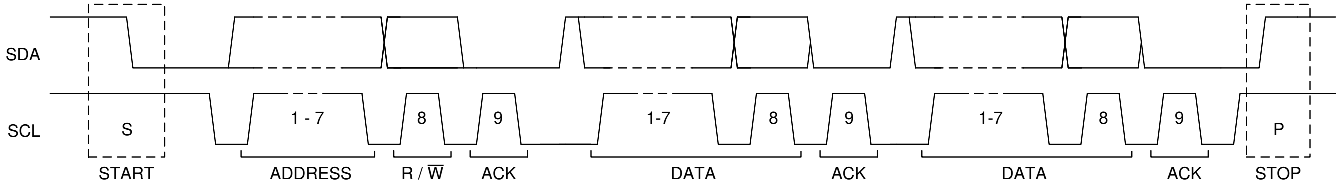


図 9-15. Complete Data Transfer

9.6.1.6 Single Read and Write

If the register address is not defined, the charger IC send back NACK and go back to the idle state.

1	7	1	1	8	1	8	1	1
S	Slave Address	0	ACK	Reg Addr	ACK	Data to Addr	ACK	P

図 9-16. Single Write

1	7	1	1	8	1	1	7	1	1
S	Slave Address	0	ACK	Reg Addr	ACK	S	Slave Addr	1	ACK

8	1	1
Data	NCK	P

図 9-17. Single Read

9.6.1.7 Multi-Read and Multi-Write

The charger device supports multi-read and multi-write on REG00 through REG0B.

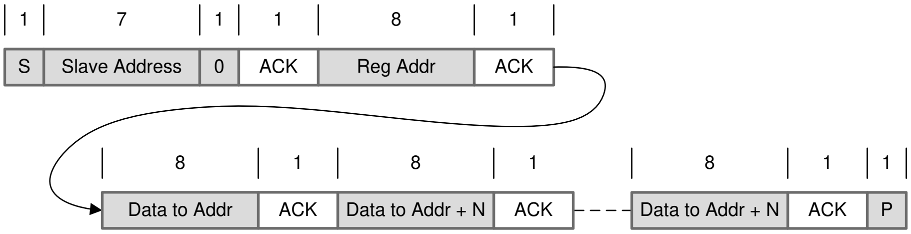


図 9-18. Multi-Write

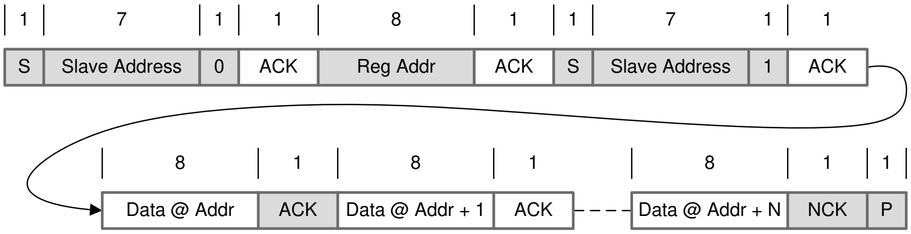


図 9-19. Multi-Read

REG09 is a fault register. It keeps all the fault information from last read until the host issues a new read. For example, if Charge Safety Timer Expiration fault occurs but recovers later, the fault register REG09 reports the fault when it is read the first time, but returns to normal when it is read the second time. in order to get the fault information at present, the host has to read REG09 for the second time. The only exception is NTC_FAULT which always reports the actual condition on the TS pin. in addition, REG09 does not support multi-read and multi-write.

9.7 Register Maps

I²C Slave Address: 6BH

9.7.1 REG00 (address = 00) [reset = 00010111]

図 9-20. REG00 Register

7	6	5	4	3	2	1	0
EN_HIZ	EN_ICHG_MON[1]	EN_ICHG_MON[0]	IINDPM[4]	IINDPM[3]	IINDPM[2]	IINDPM[1]	IINDPM[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

表 9-6. REG00 Field Descriptions

Bit	Field	POR	Type[1]	Reset	Description	Comment
7	EN_HIZ	0	R/W	by REG_RST by Watchdog	0 – Disable, 1 – Enable	Enable HIZ Mode 0 – Disable (default) 1 – Enable
6	EN_ICHG_MON[1]	0	R/W	by REG_RST	00 - Enable STAT pin function (default) 01 - Reserved 10 - Reserved 11 - Disable STAT pin function (float pin)	
5	EN_ICHG_MON[0]	0	R/W	by REG_RST		
4	IINDPM[4]	1	R/W	by REG_RST	1600 mA	Input Current Limit Offset: 100 mA Range: 100 mA (000000) – 3.2 A (11111) Default:2400 mA (10111), maximum input current limit, not typical. IINDPM bits are changed automatically after input source detection is completed Host can over-write IINDPM register bits after input source detection is completed.
3	IINDPM[3]	0	R/W	by REG_RST	800 mA	
2	IINDPM[2]	1	R/W	by REG_RST	400 mA	
1	IINDPM[1]	1	R/W	by REG_RST	200 mA	
0	IINDPM[0]	1	R/W	by REG_RST	100 mA	

(1) LEGEND: R/W = Read/Write; R = Read only

9.7.2 REG01 (address = 01) [reset = 00011010]

図 9-21. REG01 Register

7	6	5	4	3	2	1	0
PFM _DIS	WD_RST	OTG_CONFIG	CHG_CONFIG	SYS_Min[2]	SYS_Min[1]	SYS_Min[0]	Min_V_{BAT}_SEL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

表 9-7. REG01 Field Descriptions

Bit	Field	POR	Type(1)	Reset	Description	Comment
7	PFM _DIS	0	R/W	by REG_RST	0 – Enable PFM 1 – Disable PFM	Default: 0 - Enable
6	WD_RST	0	R/W	by REG_RST by Watchdog	I^2C Watchdog Timer Reset 0 – Normal ; 1 – Reset	Default: Normal (0) Back to 0 after watchdog timer reset
5	OTG_CONFIG	0	R/W	by REG_RST by Watchdog	0 – OTG Disable 1 – OTG Enable	Default: OTG disable (0) Note: 1. OTG_CONFIG would over-ride Charge Enable Function in CHG_CONFIG
4	CHG_CONFIG	1	R/W	by REG_RST by Watchdog	0 - Charge Disable 1- Charge Enable	Default: Charge Battery (1) Note: 1. Charge is enabled when both CE pin is pulled low AND CHG_CONFIG bit is 1.
3	SYS_Min[2]	1	R/W	by REG_RST	System Minimum Voltage	000: 2.6 V 001: 2.8 V 010: 3 V 011: 3.2 V 100: 3.4 V 101: 3.5 V 110: 3.6 V 111: 3.7 V Default: 3.5 V (101)
2	SYS_Min[1]	0	R/W	by REG_RST		
1	SYS_Min[0]	1	R/W	by REG_RST		
0	Min_V_{BAT}_SEL	0	R/W	by REG_RST	0 – 2.8 V BAT falling, 1 – 2.5 V BAT falling	Minimum battery voltage for OTG mode. Default falling 2.8 V (0); Rising threshold 3.0 V (0)

(1) LEGEND: R/W = Read/Write; R = Read only

9.7.3 REG02 (address = 02) [reset = 10100 010]

図 9-22. REG02 Register

7	6	5	4	3	2	1	0
BOOST_LIM	Q1_FULLON	ICHG[5]	ICHG[4]	ICHG[3]	ICHG[2]	ICHG[1]	ICHG[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

表 9-8. REG02 Field Descriptions

Bit	Field	POR	Type(1)	Reset	Description	Comment
7	BOOST_LIM	1	R/W	by REG_RST by Watchdog	0 = 0.5 A 1 = 1.2 A	Default: 1.2 A (1) Note: The current limit options listed are minimum current limit specs.
6	Q1_FULLON	0	R/W	by REG_RST	0 – Use higher Q1 RDSON when programmed IINDPM < 700mA (better accuracy) 1 – Use lower Q1 RDSON always (better efficiency)	In boost mode, full FET is always used and this bit has no effect
5	ICHG[5]	1	R/W	by REG_RST by Watchdog	1920 mA	Fast Charge Current Default: 2040mA (100010) Range: 0 mA (0000000) – 3000 mA (110010) Note: I_{CHG} = 0 mA disables charge. I_{CHG} > 3000 mA (110010 clamped to register value 3000 mA (110010))
4	ICHG[4]	0	R/W	by REG_RST by Watchdog	960 mA	
3	ICHG[3]	0	R/W	by REG_RST by Watchdog	480 mA	
2	ICHG[2]	0	R/W	by REG_RST by Watchdog	240 mA	
1	ICHG[1]	1	R/W	by REG_RST by Watchdog	120 mA	
0	ICHG[0]	0	R/W	by REG_RST by Watchdog	60 mA	

(1) LEGEND: R/W = Read/Write; R = Read only

9.7.4 REG03 (address = 03) [reset = 001 0001 0]

図 9-23. Register REG03

7	6	5	4	3	2	1	0
IPRECHG[3]	IPRECHG[2]	IPRECHG[1]	IPRECHG[0]	ITERM[3]	ITERM[2]	ITERM[1]	ITERM[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

表 9-9. REG03 Field Descriptions

Bit	Field	POR	Type(1)	Reset	Description	Comment
7	IPRECHG[3]	0	R/W	by REG_RST by Watchdog	480 mA	Precharge Current Default: 180 mA (0010) Offset: 60 mA Note: IPRECHG > 780 mA clamped to 780 mA (1100)
6	IPRECHG[2]	0	R/W	by REG_RST by Watchdog	240 mA	
5	IPRECHG[1]	1	R/W	by REG_RST by Watchdog	120 mA	
4	IPRECHG[0]	0	R/W	by REG_RST by Watchdog	60 mA	
3	ITERM[3]	0	R/W	by REG_RST by Watchdog	480 mA	Termination Current Default: 180 mA (0010) Offset: 60 mA
2	ITERM[2]	0	R/W	by REG_RST by Watchdog	240 mA	
1	ITERM[1]	1	R/W	by REG_RST by Watchdog	120 mA	
0	ITERM[0]	0	R/W	by REG_RST by Watchdog	60 mA	

(1) LEGEND: R/W = Read/Write; R = Read only

9.7.5 REG04 (address = 04) [reset = 01011000]

図 9-24. Register REG04

7	6	5	4	3	2	1	0
VREG[4]	VREG[3]	VREG[2]	VREG[1]	VREG[0]	TOPOFF_TIMER[1]	TOPOFF_TIMER[0]	VRECHG
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

表 9-10. REG04 Field Descriptions

Bit	Field	POR	Type[1]	Reset	Description	Comment
7	VREG[4]	0	R/W	by REG_RST by Watchdog	512 mV	Charge Voltage Offset: 3.847 V Range: 3.847 V to 4.615 V (11000) Default: 4.199 V (01011) Special Value: (01111): 4.343 V Note: Value above 11000 (4.615 V) is clamped to register value 11000 (4.615 V)
6	VREG[3]	1	R/W	by REG_RST by Watchdog	256 mV	
5	VREG[2]	0	R/W	by REG_RST by Watchdog	128 mV	
4	VREG[1]	1	R/W	by REG_RST by Watchdog	64 mV	
3	VREG[0]	1	R/W	by REG_RST by Watchdog	32 mV	
2	TOPOFF_TIMER[1]	0	R/W	by REG_RST by Watchdog	00 – Disabled (Default) 01 – 15 minutes 10 – 30 minutes 11 – 45 minutes	The extended time following the termination condition is met. When disabled, charge terminated when termination conditions are met
1	TOPOFF_TIMER[0]	0	R/W	by REG_RST by Watchdog		
0	VRECHG	0	R/W	by REG_RST by Watchdog	0 – 100 mV 1 – 200 mV	Recharge threshold Default: 100mV (0)

(1) LEGEND: R/W = Read/Write; R = Read only

9.7.6 REG05 (address = 05) [reset = 10011111]

図 9-25. Register REG05

7	6	5	4	3	2	1	0
EN_TERM	Reserved	WATCHDOG[1]	WATCHDOG[0]	EN_TIMER	CHG_TIMER	TREG	JEITA_ISET
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

表 9-11. REG05 Field Descriptions

Bit	Field	POR	Type(1)	Reset	Description	Comment
7	EN_TERM	1	R/W	by REG_RST by Watchdog	0 – Disable 1 – Enable	Default: Enable termination (1)
6	Reserved	0	R/W	by REG_RST by Watchdog	Reserved	Reserved
5	WATCHDOG[1]	0	R/W	by REG_RST by Watchdog	00 – Disable timer, 01 – 40 s, 10 – 80 s,11 – 160 s	Default: 40 s (01)
4	WATCHDOG[0]	1	R/W	by REG_RST by Watchdog		
3	EN_TIMER	1	R/W	by REG_RST by Watchdog	0 – Disable 1 – Enable both fast charge and precharge timer	Default: Enable (1)
2	CHG_TIMER	1	R/W	by REG_RST by Watchdog	0 – 5 hrs 1 – 10 hrs	Default: 10 hours (1)
1	TREG	1	R/W	by REG_RST by Watchdog	Thermal Regulation Threshold: 0 - 90°C 1 - 110°C	Default: 110°C (1)
0	JEITA_ISET (0C-10C)	1	R/W	by REG_RST by Watchdog	0 – 50% of ICHG 1 – 20% of ICHG	Default: 20% (1)

(1) LEGEND: R/W = Read/Write; R = Read only

9.7.7 REG06 (address = 06) [reset = 01100110]

図 9-26. Register REG06

7	6	5	4	3	2	1	0
OVP[1]	OVP[0]	BOOSTV[1]	BOOSTV[0]	VINDPM[3]	VINDPM[2]	VINDPM[1]	VINDPM[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

表 9-12. REG06 Field Descriptions

Bit	Field	POR	Type(1)	Reset	Description	Comment
7	OVP[1]	0	R/W	by REG_RST	Default: 6.5V (01)	VAC OVP threshold: 00 - 5.5 V 01 – 6.5 V (5-V input) 10 – 10.5 V (9-V input) 11 – 14 V (12-V input)
6	OVP[0]	1	R/W	by REG_RST		
5	BOOSTV[1]	1	R/W	by REG_RST		Boost Regulation Voltage: 00 - 4.85V 01 - 5.00V 10 - 5.15V 11 - 5.30V
4	BOOSTV[0]	0	R/W	by REG_RST		
3	VINDPM[3]	0	R/W	by REG_RST	800 mV	Absolute VINDPM Threshold Offset: 3.9 V Range: 3.9 V (0000) – 5.4 V (1111) Default: 4.5V (0110)
2	VINDPM[2]	1	R/W	by REG_RST	400 mV	
1	VINDPM[1]	1	R/W	by REG_RST	200 mV	
0	VINDPM[0]	0	R/W	by REG_RST	100 mV	

(1) LEGEND: R/W = Read/Write; R = Read only

9.7.8 REG07 (address = 07) [reset = 01001100]

図 9-27. Register REG07

7	6	5	4	3	2	1	0
IINDET_EN	TMR2X_EN	BATFET_DIS	JEITA_VSET	BATFET_DLY	BATFET_RST_EN	VDPM_BAT_TRACK[1]	VDPM_BAT_TRACK[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

表 9-13. REG07 Field Descriptions

Bit	Field	POR	Type(1)	Reset	Description	Comment
7	IINDET_EN	0	R/W	by REG_RST by Watchdog	0 - Not in input current limit detection 1 - Force input current limit detection when VBUS is present	Returns to 0 after input detection is complete
6	TMR2X_EN	1	R/W	by REG_RST by Watchdog	0 – Disable 1 – Safety timer slowed by 2X during input DPM (both V and I) or JEITA cool, or thermal regulation	
5	BATFET_DIS	0	R/W	by REG_RST	0 – Allow Q4 turn on, 1 – Turn off Q4 with t_{BATFET_DLY} delay time (REG07[3])	Default: Allow Q4 turn on(0)
4	JEITA_VSET (45C-60C)	0	R/W	by REG_RST by Watchdog	0 – Set Charge Voltage to 4.1V (max), 1 – Set Charge Voltage to VREG	
3	BATFET_DLY	1	R/W	by REG_RST	0 – Turn off BATFET immediately when BATFET_DIS bit is set 1 –Turn off BATFET after t_{BATFET_DLY} (typ. 10 s) when BATFET_DIS bit is set	Default: 1 Turn off BATFET after t_{BATFET_DLY} (typ. 10 s) when BATFET_DIS bit is set
2	BATFET_RST_EN	1	R/W	by REG_RST by Watchdog	0 – Disable BATFET reset function 1 – Enable BATFET reset function	Default: 1 Enable BATFET reset function
1	VDPM_BAT_TRACK[1]	0	R/W	by REG_RST	00 - Disable function (VINDPM set by register) 01 - VBAT + 200mV 10 - VBAT + 250mV 11 - VBAT + 300mV	Sets VINDPM to track BAT voltage. Actual VINDPM is higher of register value and VBAT + VDPM_BAT_TRACK
0	VDPM_BAT_TRACK[0]	0	R/W	by REG_RST		

(1) LEGEND: R/W = Read/Write; R = Read only

9.7.9 REG08 (address = 08) [reset = xxxxxxxx]

図 9-28. Register REG08

7	6	5	4	3	2	1	0
VBUS_STAT[2]	VBUS_STAT[1]	VBUS_STAT[0]	CHRG_STAT[1]	CHRG_STAT[0]	PG_STAT	THERM_STAT	VSYS_STAT
R	R	R	R	R	R	R	R

表 9-14. REG08 Field Descriptions

Bit	Field	POR	Type[(1)]	Reset	Description
7	VBUS_STAT[2]	x	R	NA	VBUS Status register BQ25601D 000: No input 001: USB Host SDP 010: USB CDP: (1.5A) 011: USB DCP (2.4 A) 101: Unknown Adapter (500 mA) 110: Non-Standard Adapter (1A/2A/2.1A/2.4A) 111: OTG Software current limit is reported in IINDPM register
6	VBUS_STAT[1]	x	R	NA	
5	VBUS_STAT[0]	x	R	NA	
4	CHRG_STAT[1]	x	R	NA	Charging status: 00 – Not Charging 01 – Pre-charge (< $V_{BATLOWV}$) 10 – Fast Charging 11 – Charge Termination
3	CHRG_STAT[0]	x	R	NA	
2	PG_STAT	x	R	NA	Power Good status: 0 – Power Not Good 1 – Power Good
1	THERM_STAT	x	R	NA	0 – Not in ther mAl regulation 1 – in ther mAl regulation
0	VSYS_STAT	x	R	NA	0 – Not in VSYSMin regulation (BAT > VSYSMin) 1 – in VSYSMin regulation (BAT < VSYSMin)

(1) LEGEND: R/W = Read/Write

9.7.10 REG09 (address = 09) [reset = xxxxxxxx]

図 9-29. Register REG09

7	6	5	4	3	2	1	0
WATCHDOG_FAULT	BOOST_FAULT	CHRG_FAULT[1]	CHRG_FAULT[0]	BAT_FAULT	NTC_FAULT[2]	NTC_FAULT[1]	NTC_FAULT[0]
R	R	R	R	R	R	R	R

表 9-15. REG09 Field Descriptions

Bit	Field	POR	Type(1)	Reset	Description
7	WATCHDOG_FAULT	x	R	NA	0 – Normal, 1- Watchdog timer expiration
6	BOOST_FAULT	x	R	NA	0 – Normal, 1 – VBUS overloaded in OTG, or VBUS OVP, or battery is too low (any conditions that we cannot start boost function)
5	CHRG_FAULT[1]	x	R	NA	00 – Normal, 01 – input fault (VAC OVP or VBAT < VBUS < 3.8 V), 10 - Thermal shutdown, 11 – Charge Safety Timer Expiration
4	CHRG_FAULT[0]	x	R	NA	
3	BAT_FAULT	x	R	NA	0 – Normal, 1 – BATOVP
2	NTC_FAULT[2]	x	R	NA	JEITA 000 – Normal, 010 – Warm, 011 – Cool, 101 – Cold, 110 – Hot (Buck mode) 000 – Normal, 101 – Cold, 110 – Hot (Boost mode)
1	NTC_FAULT[1]	x	R	NA	
0	NTC_FAULT[0]	x	R	NA	

(1) LEGEND: R/W = Read/Write; R = Read only

9.7.11 REG0A (address = 0A) [reset = xxxxxx00]

図 9-30. Register REG0A

7	6	5	4	3	2	1	0
VBUS_GD	VINDPM_STAT	IINDPM_STAT	Reserved	TOPOFF_ACTIVE	ACOV_STAT	VINDPM_INT_MASK	IINDPM_INT_MASK
R	R	R	R	R	R	R/W	R/W

表 9-16. REG0A Field Descriptions

Bit	Field	POR	Type[1]	Reset	Description
7	VBUS_GD	x	R	NA	0 – Not VBUS attached, 1 – VBUS Attached
6	VINDPM_STAT	x	R	NA	0 – Not in VINDPM, 1 – in VINDPM
5	IINDPM_STAT	x	R	NA	0 – Not in IINDPM, 1 – in IINDPM
4	Reserved	x	R	NA	
3	TOPOFF_ACTIVE	x	R	NA	0 – Top off timer not counting. 1 – Top off timer counting
2	ACOV_STAT	x	R	NA	0 – Device is NOT in ACOV 1 – Device is in ACOV
1	VINDPM_INT_ MASK	0	R/W	by REG_RST	0 - Allow VINDPM INT pulse 1 - Mask VINDPM INT pulse
0	IINDPM_INT_ MASK	0	R/W	by REG_RST	0 - Allow IINDPM INT pulse 1 - Mask IINDPM INT pulse

(1) LEGEND: R/W = Read/Write; R = Read only

9.7.12 REG0B (address = 0B) [reset = 00111xxx]

図 9-31. Register REG0B

7	6	5	4	3	2	1	0
REG_RST	PN[3]	PN[2]	PN[1]	PN[0]	Reserved	DEV_REV[1]	DEV_REV[0]
R/W	R	R	R	R	R	R	R

表 9-17. REG0B Field Descriptions

Bit	Field	POR	Type(1)	Reset	Description
7	REG_RST	0	R/W	NA	Register reset 0 – Keep current register setting 1 – Reset to default register value and reset safety timer Note: Bit resets to 0 after register reset is completed
6	PN[3]	0	R	NA	BQ25601D : 0010
5	PN[2]	1	R	NA	
4	PN[1]	1	R	NA	
3	PN[0]	1	R	NA	
2	Reserved	x	R	NA	
1	DEV_REV[1]	x	R	NA	
0	DEV_REV[0]	x	R	NA	

(1) LEGEND: R/W = Read/Write; R = Read only

Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

10.1 Application information

A typical application consists of the device configured as an I^2C controlled power path management device and a single cell battery charger for Li-Ion and Li-polymer batteries used in a wide range of smart phones and other portable devices. It integrates an input reverse-block FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and battery FET (BATFET Q4) between the system and battery. The device also integrates a bootstrap diode for the high-side gate drive.

10.2 Typical Application

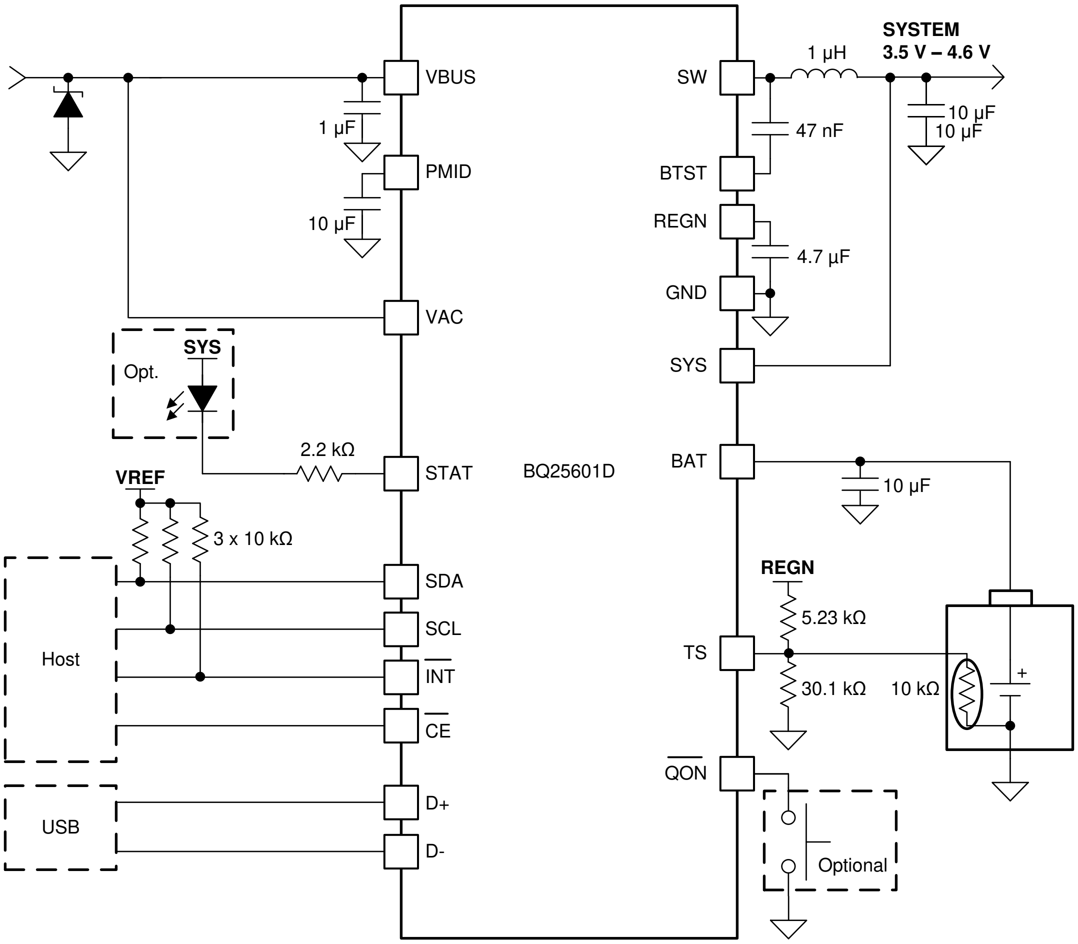


図 10-1. Power Path Management Application

10.2.1 Design Requirements

表 10-1. Design Requirements

PARAMETER	VALUE
Input Voltage	3.9V to 13.5V
Input Current	3.0A
Fast Charge Current	3.0A
Battery Regulation Voltage	4.2V

10.2.2 Detailed Design Procedure

10.2.2.1 Inductor Selection

The 1.5-MHz switching frequency allows the use of small inductor and capacitor values to maintain an inductor saturation current higher than the charging current (I_{CHG}) plus half the ripple current (I_{RIPPLE}):

$$I_{SAT} \geq I_{CHG} + (1/2)\, I_{RIPPLE} \tag{3}$$

The inductor ripple current depends on the input voltage (V_{VBUS}), the duty cycle ($D = V_{BAT}/V_{VBUS}$), the switching frequency (f_S) and the inductance (L).

$$I_{RIPPLE} = \frac{V_{IN} \times D \times (1 - D)}{fs \times L} \quad (4)$$

The maximum inductor ripple current occurs when the duty cycle (D) is 0.5 or approximately 0.5. Usually inductor ripple is designed in the range between 20% and 40% maximum charging current as a trade-off between inductor size and efficiency for a practical design.

10.2.2.2 Input Capacitor

Design input capacitance to provide enough ripple current rating to absorb input switching ripple current. The worst case RMS ripple current is half of the charging current when duty cycle is 0.5. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current I_{Cin} occurs where the duty cycle is closest to 50% and can be estimated using 式 5.

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1 - D)} \quad (5)$$

Low ESR ceramic capacitor such as X7R or X5R is preferred for input decoupling capacitor and should be placed to the drain of the high-side MOSFET and source of the low-side MOSFET as close as possible. Voltage rating of the capacitor must be higher than normal input voltage level. A rating of 25-V or higher capacitor is preferred for 15 V input voltage. Capacitance of 22-μF is suggested for typical of 3A charging current.

10.2.2.3 Output Capacitor

Ensure that the output capacitance has enough ripple current rating to absorb the output switching ripple current. 式 6 shows the output capacitor RMS current I_{COUT} calculation.

$$I_{COUT} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE} \quad (6)$$

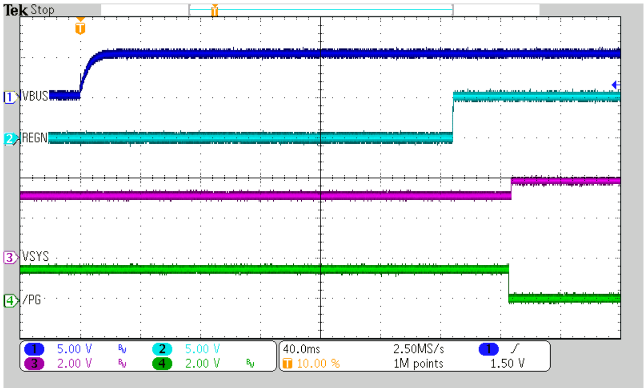
The output capacitor voltage ripple can be calculated as follows:

$$\Delta V_O = \frac{V_{OUT}}{8LCfs^2}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

At certain input and output voltage and switching frequency, the voltage ripple can be reduced by increasing the output filter LC.

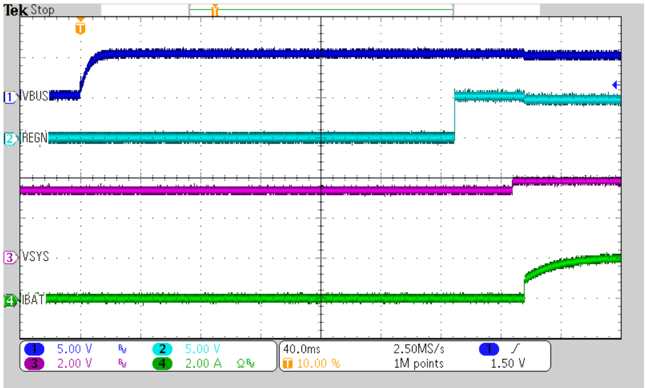
The charger device has internal loop compensation optimized for ≤20μF ceramic output capacitance. The preferred ceramic capacitor is 10V rating, X7R or X5R.

10.2.3 Application Curves



V_{VBUS} = 5 V V_{VBAT} = 3.2 V

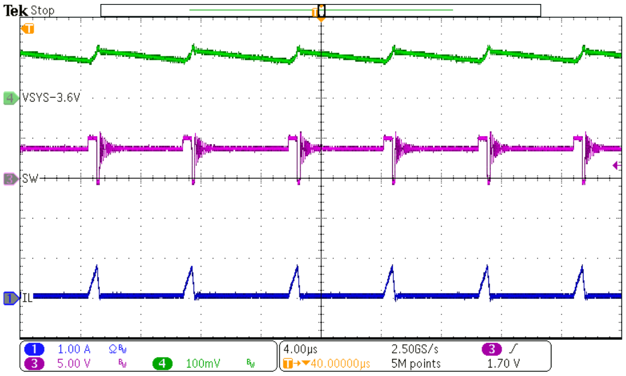
図 10-2. Power-Up with Charge Disabled



V_{VBUS} = 5 V V_{VBAT} = 3.2 V

I_{CHG} = 2 A

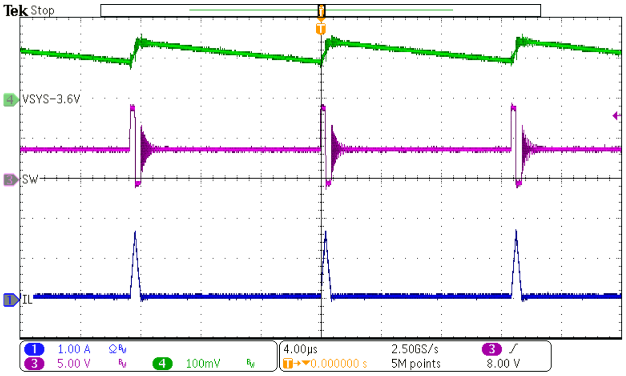
図 10-3. Power-Up with Charge Enabled



V_{VBUS} = 5 V

I_{SYS} = 50 mA Charge Disabled

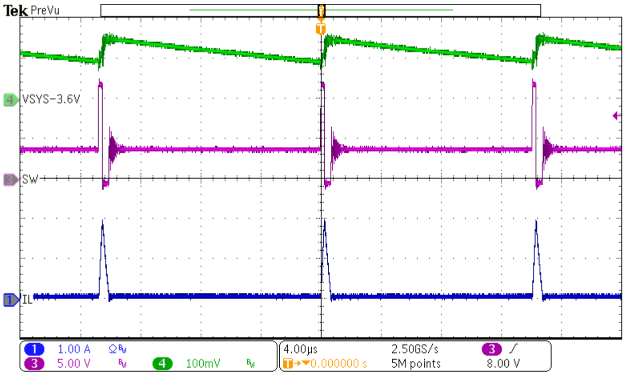
図 10-4. PFM Switching in Buck Mode



V_{VBUS} = 9 V

I_{SYS} = 50 mA Charge Disabled

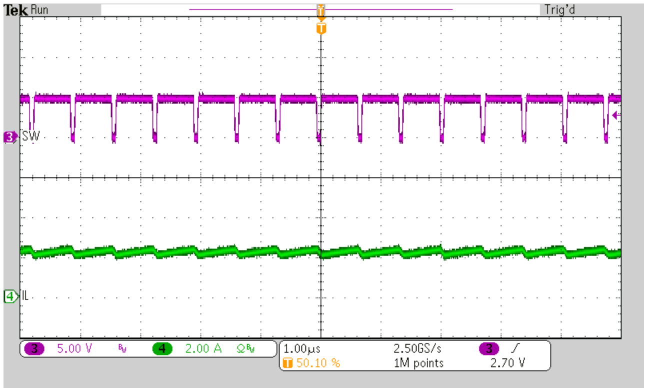
図 10-5. PFM Switching in Buck Mode



V_{VBUS} = 12 V

I_{SYS} = 50 mA Charge Disabled

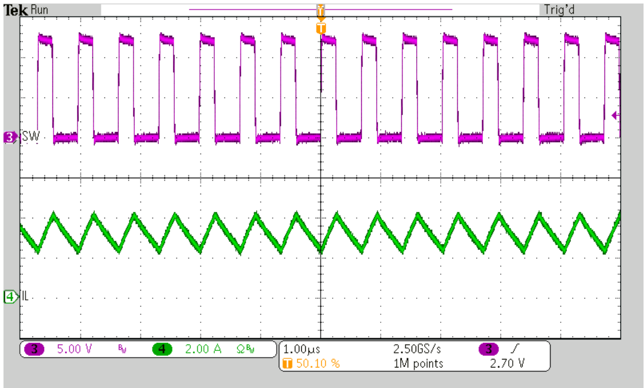
図 10-6. PFM Switching in Buck Mode



V_{VBUS} = 5 V V_{VBAT} = 3.8 V

I_{CHG} = 2 A

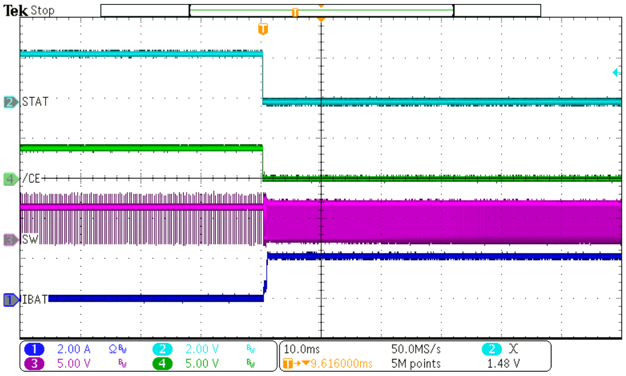
図 10-7. PWM Switching in Buck Mode



V_{VBUS} = 12 V V_{VBAT} = 3.8 V

I_{CHG} = 2 A

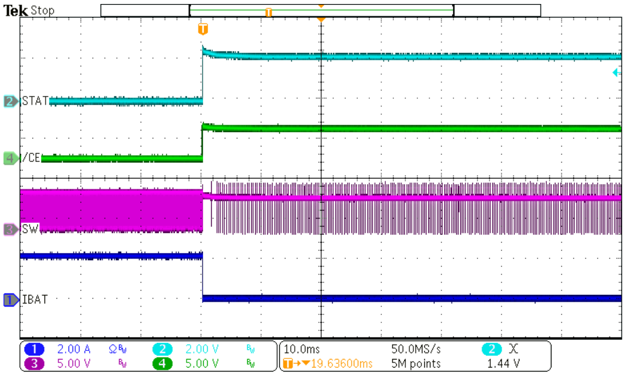
図 10-8. PWM Switching in Buck Mode



V_{VBUS} = 5 V V_{VBAT} = 3.2 V

I_{CHG} = 2 A

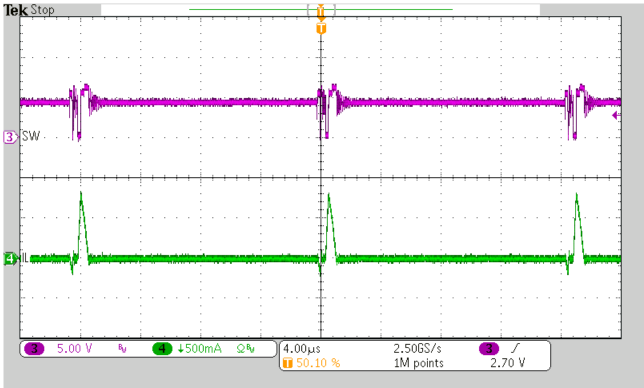
図 10-9. Charge Enable



V_{VBUS} = 5 V V_{VBAT} = 3.2 V

I_{CHG} = 2 A

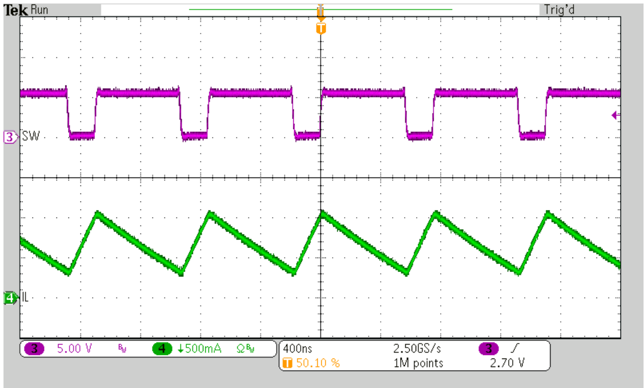
図 10-10. Charge Disable



V_{VBAT} = 4 V

I_{LOAD}= 50 mA PFM Enabled

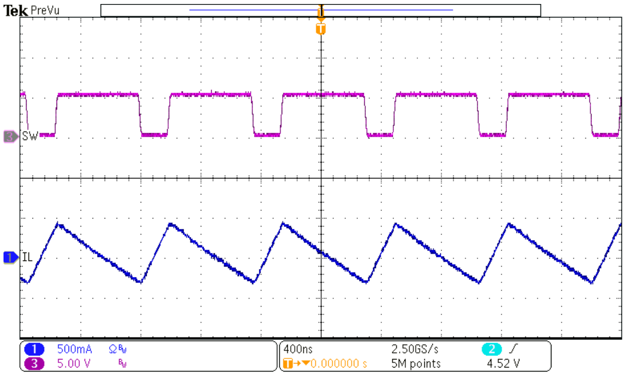
図 10-11. OTG Switching



V_{VBAT} = 4 V

I_{LOAD}= 1 A PFM Enabled

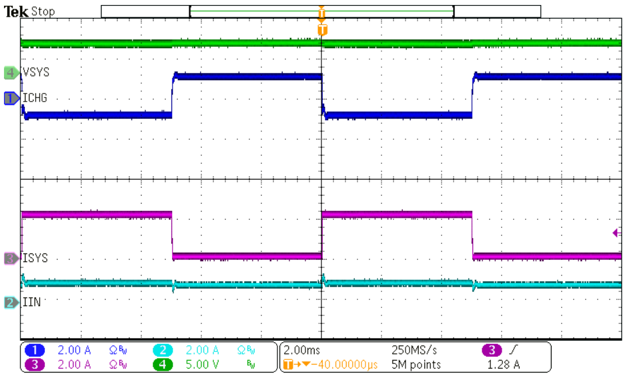
図 10-12. OTG Switching



V_{VBAT} = 4 V

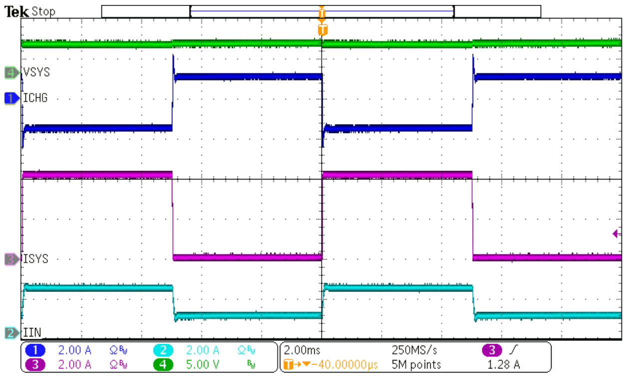
I_{LOAD}= 0 A PFM Disabled

図 10-13. OTG Switching



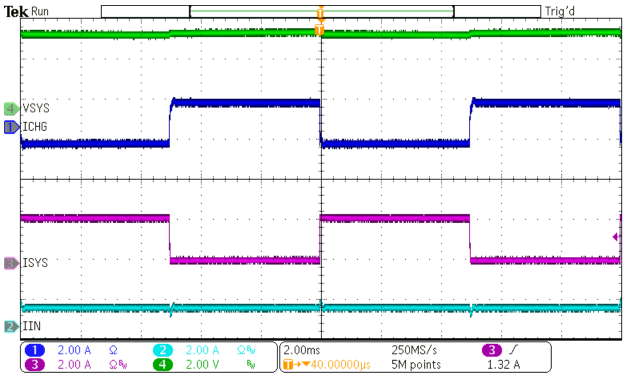
V_{VBUS} = 5 V
I_{SYS} from 0 A to 2 A
V_{BAT} = 3.7 V
I_{INDPM} = 1 A
I_{CHG} = 1 A

図 10-14. System Load Transient



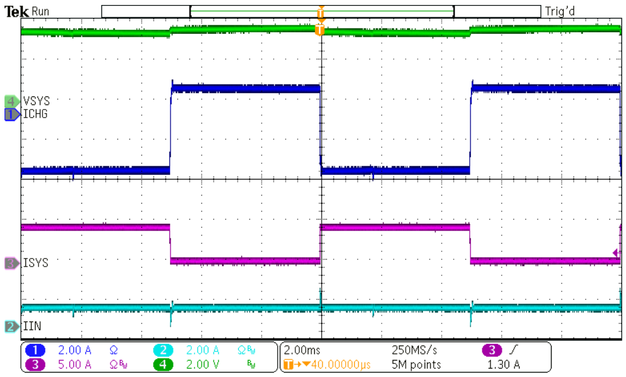
V_{VBUS} = 5 V
I_{SYS} from 0 A to 4 A
V_{BAT} = 3.7 V
I_{INDPM} = 2 A
I_{CHG} = 1 A

図 10-15. System Load Transient



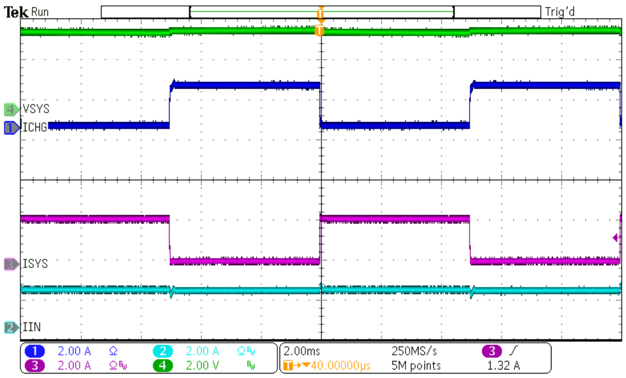
V_{VBUS} = 5 V
I_{SYS} from 0 A to 2 A
V_{BAT} = 3.7 V
I_{INDPM} = 1 A
I_{CHG} = 2 A

図 10-16. System Load Transient



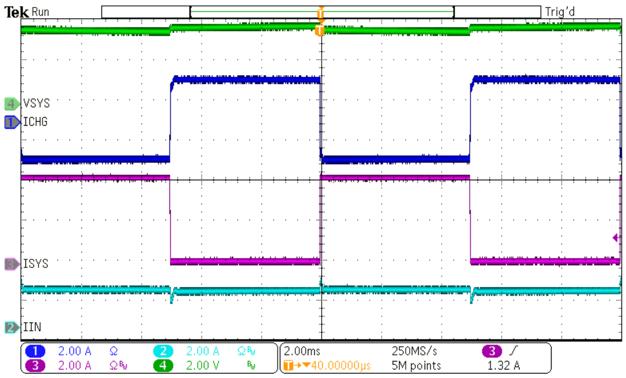
V_{VBUS} = 5 V
I_{SYS} from 0 A to 4 A
V_{BAT} = 3.7 V
I_{INDPM} = 1 A
I_{CHG} = 2 A

図 10-17. System Load Transient



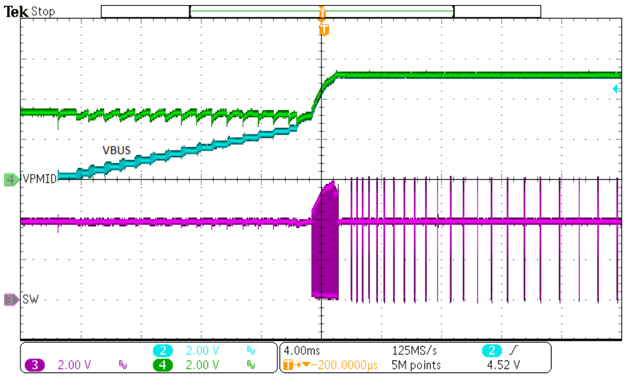
V_{VBUS} = 5 V
I_{SYS} from 0 A to 2 A
V_{BAT} = 3.7 V
I_{INDPM} = 2 A
I_{CHG} = 2 A

図 10-18. System Load Transient



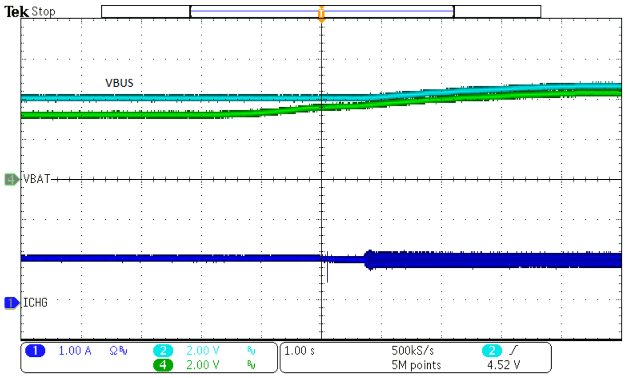
V_{VBUS} = 5 V
I_{SYS} from 0 A to 4 A
V_{BAT} = 3.7 V
I_{INDPM} = 2 A
I_{CHG} = 2 A

図 10-19. System Load Transient



V_{BAT} = 3.8 V C_{LOAD} = 470 µF

図 10-20. OTG Start-Up



Adaptor I_{LIM} = 1 A

図 10-21. VINDPM Tracking Battery Voltage

Power Supply Recommendations

in order to provide an output voltage on SYS, the BQ25601D device requires a power supply between 3.9 V and 14.2 V input with at least 100-mA current rating connected to VBUS and a single-cell Li-Ion battery with voltage > $V_{BATUVLO}$ connected to BAT. The source current rating needs to be at least 3 A in order for the buck converter of the charger to provide maximum output power to SYS.

10 Layout

10.1 Layout Guidelines

The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize high frequency current path loop (see 図 10-1) is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Follow this specific order carefully to achieve the proper layout.

1. Place input capacitor as close as possible to PMID pin and GND pin connections and use shortest copper trace connection or GND plane.
2. Place inductor input pin to SW pin as close as possible. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the charging current. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.
3. Put output capacitor near to the inductor and the device. Ground connections need to be tied to the IC ground with a short copper trace connection or GND plane.
4. Route analog ground separately from power ground. Connect analog ground and connect power ground separately. Connect analog ground and power ground together using thermal pad as the single ground connection point. Or using a 0-Ω resistor to tie analog ground to power ground.
5. Use single ground connection to tie charger power ground to charger analog ground. Just beneath the device. Use ground copper pour but avoid power pins to reduce inductive and capacitive noise coupling.
6. Place decoupling capacitors next to the IC pins and make trace connection as short as possible.
7. It is critical that the exposed thermal pad on the backside of the device package be soldered to the PCB ground. Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layers.
8. Ensure that the number and sizes of vias allow enough copper for a given current path.

See the EVM user's guide *BQ25601 and BQ25601D (PWR877) Evaluation Module User's Guide* for the recommended component placement with trace and via locations. For the VQFN information, refer to *Quad Flatpack No-Lead Logic Packages Application Report* and *QFN and SON PCB Attachment Application Report*.

10.2 Layout Example

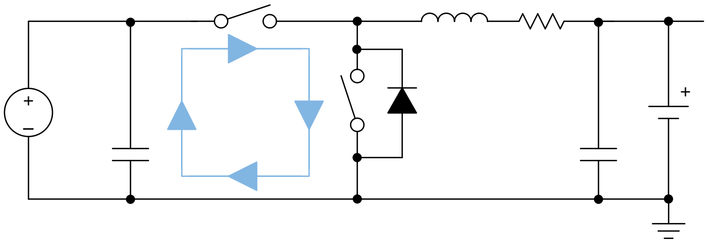


図 10-1. High Frequency Current Path

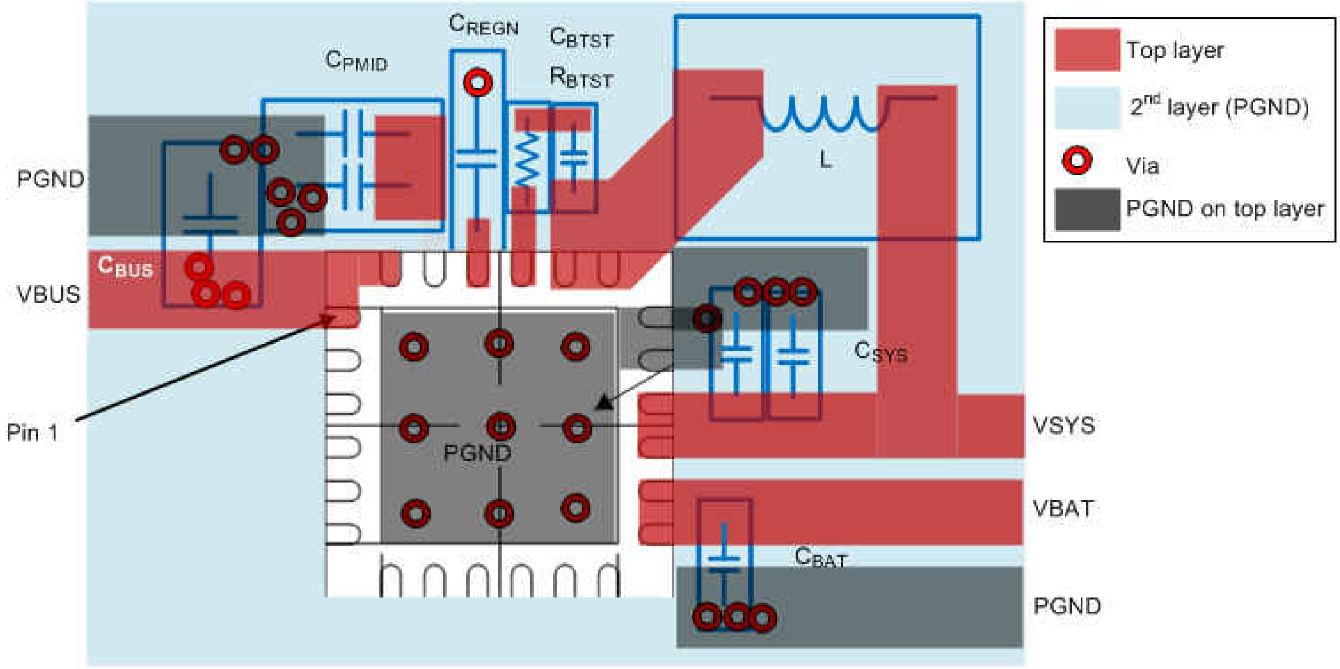


図 10-2. Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *BQ25601 and BQ25601D (PWR877) Evaluation Module User's Guide*

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 サポート・リソース

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11.5 Trademarks

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11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ25601DRTWR	Active	Production	WQFN (RTW) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BQ 25601D
BQ25601DRTWR.A	Active	Production	WQFN (RTW) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BQ 25601D
BQ25601DRTWR.B	Active	Production	WQFN (RTW) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BQ 25601D
BQ25601DRTWT	Active	Production	WQFN (RTW) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BQ 25601D
BQ25601DRTWT.A	Active	Production	WQFN (RTW) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BQ 25601D
BQ25601DRTWT.B	Active	Production	WQFN (RTW) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BQ 25601D

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

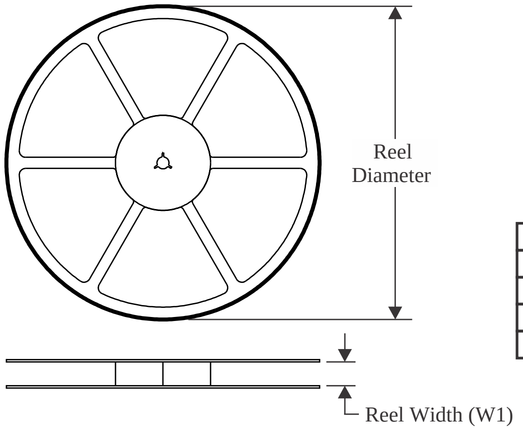
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

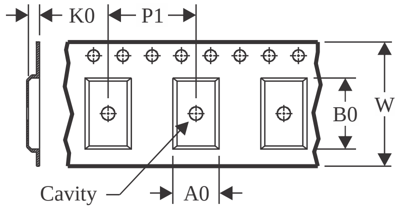
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

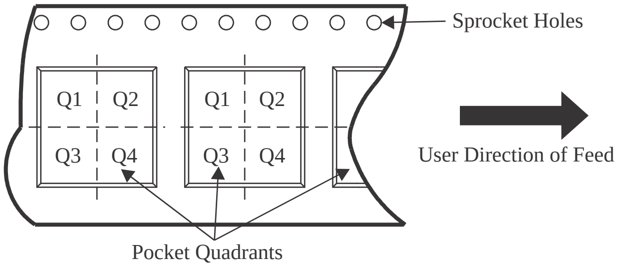


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

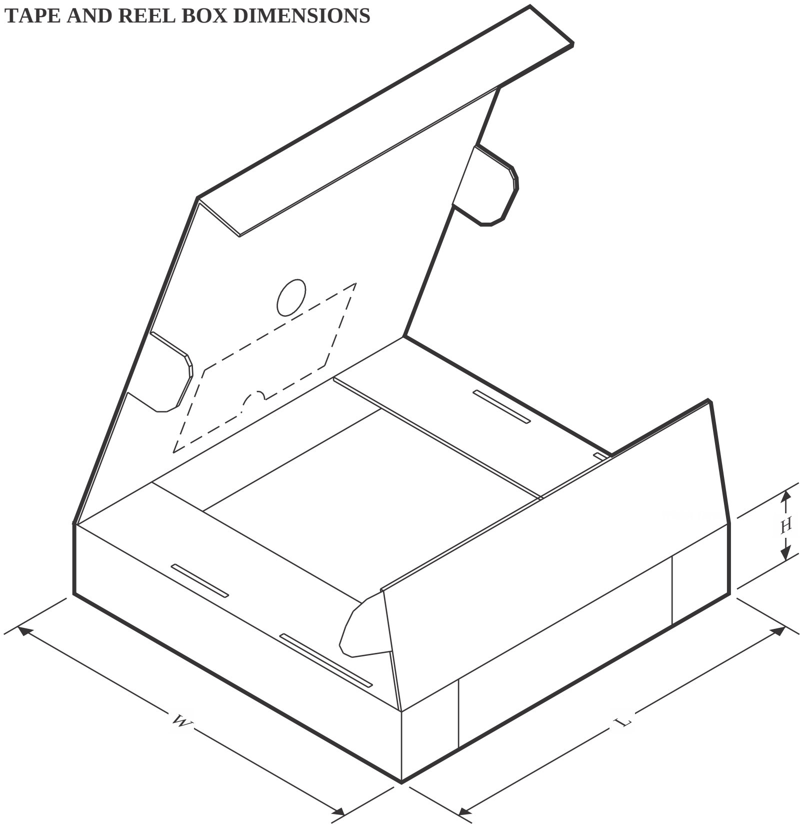
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ25601DRTWT	WQFN	RTW	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ25601DRTWT	WQFN	RTW	24	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

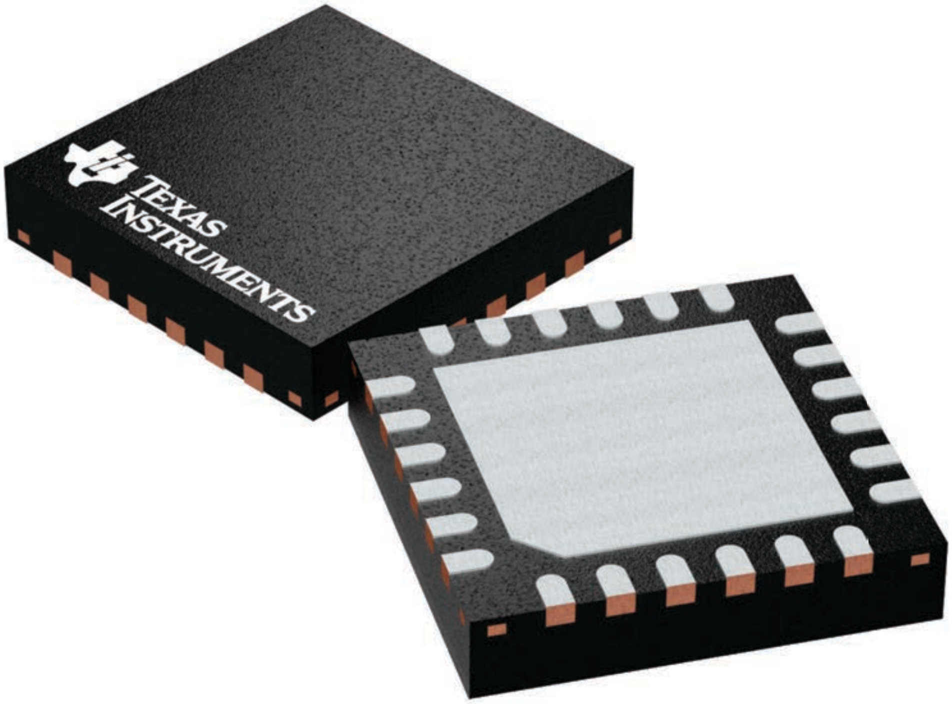
RTW 24

WQFN - 0.8 mm max height

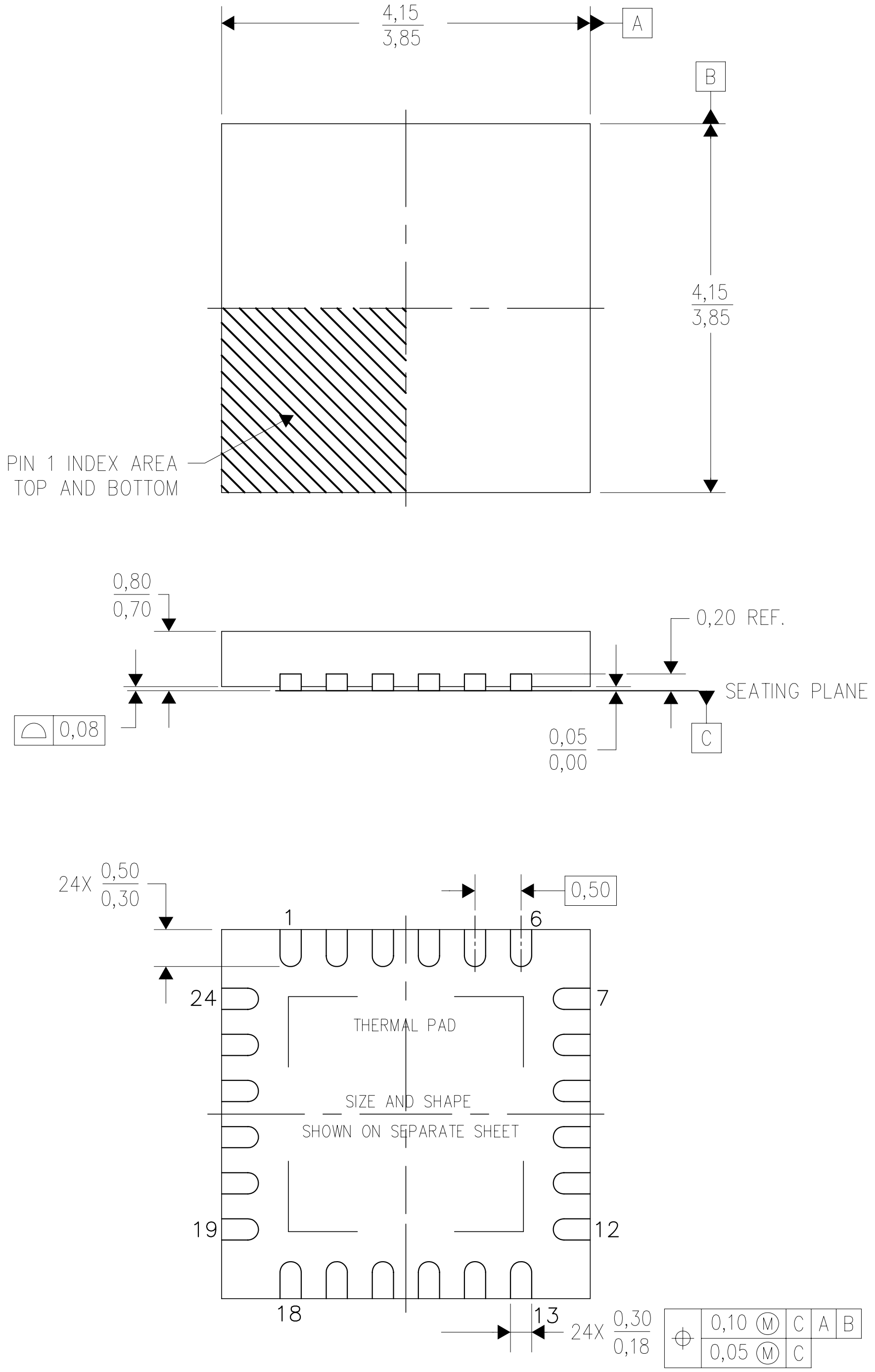
4 x 4, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



RTW (S-PWQFN-N24) PLASTIC QUAD FLATPACK NO-LEAD



4206244/C 07/11

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- C. Quad Flatpack, No—Leads (QFN) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO—220.

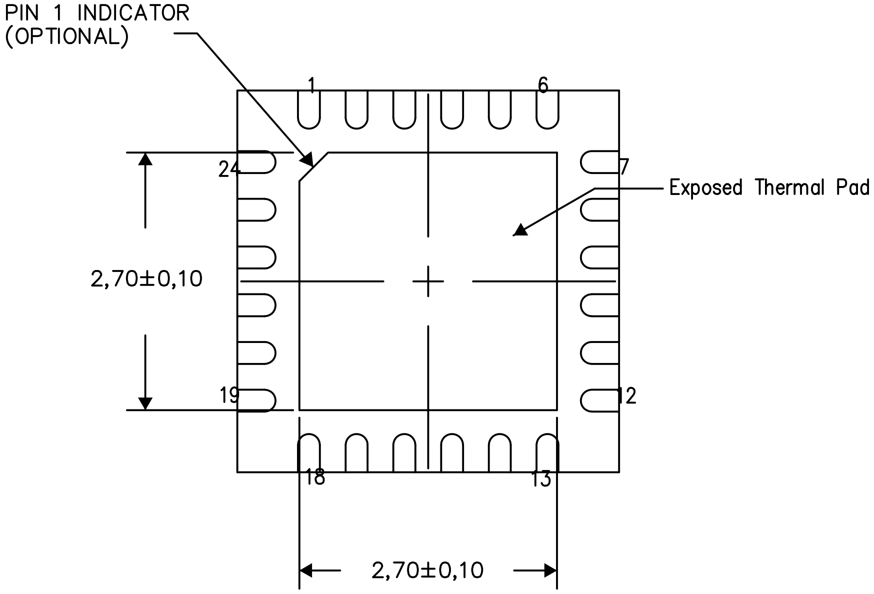
RTW (S-PWQFN-N24) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



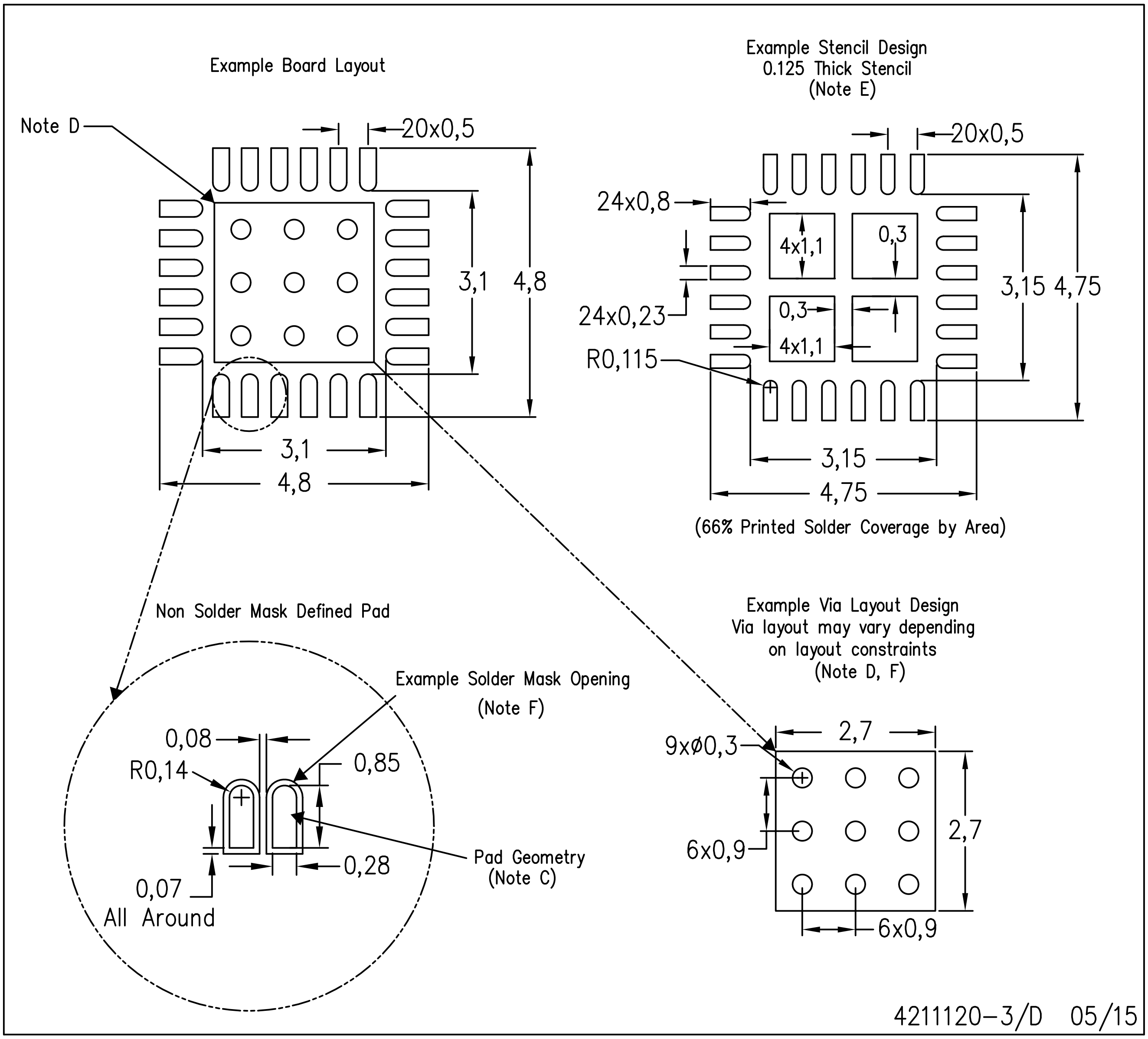
Bottom View

Exposed Thermal Pad Dimensions

4206249-5/P 05/15

NOTES: A. All linear dimensions are in millimeters

RTW (S-PWQFN-N24) PLASTIC QUAD FLATPACK NO-LEAD



4211120-3/D 05/15

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

重要なお知らせと免責事項

最終更新日：2025 年 10 月