BQ25758：I²C 制御、双方向昇降圧コントローラ (広電圧範囲対応)

1 特長

- 広い入力電圧動作範囲:4.2V～60V
- NFET ドライバ搭載の同期昇降圧 DC/DC コントローラ
  - 200kHz～600kHz の可変スイッチング周波数
  - 外部クロックへの周波数同期も可能
  - ソフト スタート付きループ補償機能を内蔵
  - 選択可能な PFM 動作で軽負荷時の効率を向上 (PFM または強制 PWM オプション)
  - 効率を最適化するオプションのゲートドライバ電源入力
- 順電力方向と逆電力方向の USB-PD 拡張電力範囲 (EPR) をサポート
  - 3.3V～60V の範囲で 20mV 刻みに調整可能な入出力電圧レギュレーション
  - 5mΩ の抵抗を使用して 400mA～20A の範囲で 50mA 刻みに調整可能な入出力電流レギュレーション (RAC_SNS、ROUT_SNS)
- VOUT = VAC で最高の効率を実現するバイパス モード
- 降圧専用モード
- 高い精度
  - ±2% の出力電圧レギュレーション
  - ±3% の出力電流レギュレーション
  - ±2% の入力電圧レギュレーション
  - ±3% の入力電流レギュレーション
- 最適なシステム性能を実現する I²C 制御、抵抗によりプログラム可能
  - ハードウェアで調整可能な入出力電流制限
- 電圧、電流、温度モニタリングのための 16 ビット ADC を内蔵
- 高度な安全機能内蔵
  - 可変入力過電圧および低電圧保護
  - 出力過電圧および過電流保護
  - サーマル シャットダウン
- ステータス出力
  - アダプタ存在ステータス ($\overline{PG}$)
  - スイッチャの動作ステータス (STAT)
- パッケージ
  - 36 ピン 5mm × 6mm QFN

2 アプリケーション

- ドッキング ステーション
- モニタ
- USB-PD EPR (拡張電力範囲)
- 昇降圧および降圧のみの動作

3 概要

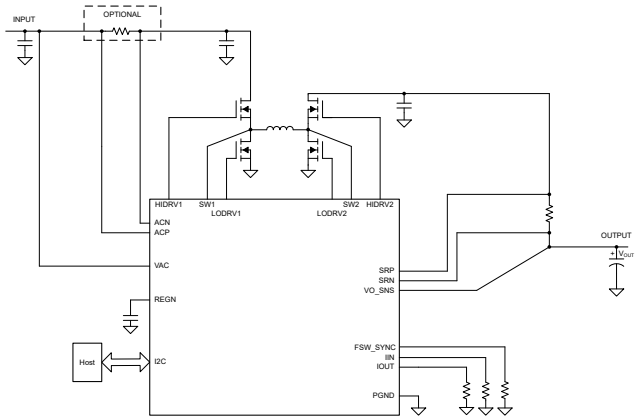
BQ25758 は、広い入力電圧に対応する 双方向のスイッチモード昇降圧コントローラです。このデバイスは、出力 CC/CV (定電流と定電圧) の各制御機能を搭載しており、広い電圧範囲にわたって高効率の電力変換を実現できます。このデバイスは、昇降圧コンバータのあらゆるループ補償機能を内蔵しているため、使いやすい高密度ソリューションを実現します。逆方向モードでは、このデバイスは出力電源から電力を取得し、保護のために追加された定電流ループによって入力端子の電圧をレギュレートします。

I²C ホスト制御モードに加えて、このデバイスは、プログラム可能なハードウェア制限もサポートしています。入力電流および出力電流のレギュレーション ターゲットは、それぞれ IIN および IOUT ピンの単一抵抗によって設定できます。デフォルトでは、このデバイスは 5V 出力を供給するようにプログラムされており、ターゲット出力電圧は VOUT_REG レジスタ ビットで調整できます。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ (2)	本体サイズ (公称)
BQ25758	RRV (VQFN 36)	6.0mm × 5.0mm	6.0mm × 5.0mm

(1) 供給されているすべてのパッケージについては、セクション 12 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



概略回路図

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4 Pin Configuration and Functions

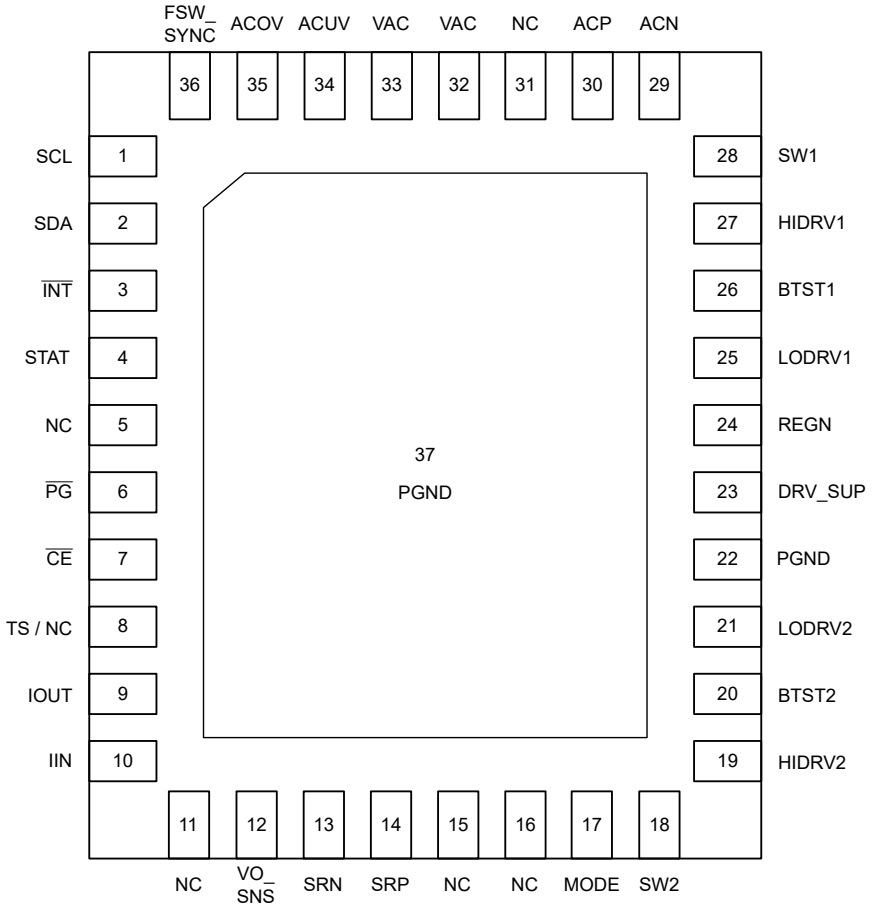


図 4-1. BQ25758, RRV Package 36-pin VQFN Top View

表 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
SCL	1	DI	**I²C Interface Clock –** Connect SCL to the logic rail through a 10-kΩ resistor.
SDA	2	DIO	**I²C Interface Data –** Connect SDA to the logic rail through a 10-kΩ resistor.
INT	3	DO	**Open Drain Interrupt Output –** Connect the INT pin to a logic rail via 10-kΩ resistor. The INT pin sends an active low, 256-µs pulse to host to report the controller device status and faults.
STAT	4	DO	**Open Drain Status Output –** Connect to the pull up rail via 10-kΩ resistor. The STAT pin function can be disabled when DIS_STAT_PIN bit is set to 1. When disabled, this pin can be used as a general purpose indicator via the FORCE_STAT_ON bit.
NC	5	-	**No Connect -** Leave this pin floating, do not tie to PGND
PG/STAT3	6	DO	**Open Drain Active Low Power Good Indicator –** Connect to the pull up rail via 10-kΩ resistor. LOW indicates a good input source if VAC is within the programmed ACUV / ACOV operating window. The PG pin function can be disabled when DIS_PG_PIN bit is set to 1. When disabled, this pin can be used as a general purpose indicator via the FORCE_STAT3_ON bit.
CE/STAT4	7	DIO	**Active Low Enable Pin –** Power conversion is enabled when EN_CHG bit is 1 and CE pin is LOW. CE pin must be pulled HIGH or LOW, do not leave floating. The CE pin function can be disabled when DIS_CE_PIN bit is set to 1. When disabled, this pin can be used as a general purpose indicator via the FORCE_STAT4_ON bit.

表 4-1. Pin Functions (続き)

PIN		I/O	DESCRIPTION
NAME	NO.		
TS / NC	8	AI	**Temperature Qualification Voltage Input –** This pin's function is normally disabled. If not needed, leave this pin floating. To enable pin functionality, set EN_TS register bit to 1. Connect a negative temperature coefficient thermistor. Program temperature window with a resistor divider from REGN to TS to PGND. Power conversion suspends when TS pin voltage is out of range. Recommend 103AT-2 10-kΩ thermistor.
IOUT	9	AI	**Output Current Limit Setting –** IOUT pin sets the maximum output current, and can be used to monitor the output current. A programming resistor to PGND is used to set the output current limit as $I_{IOUT} = K_{IOUT} / R_{IOUT}$. When the device is under output current regulation, the voltage at IOUT pin is V_{REF_IOUT}. When IOUT pin voltage is less than V_{REF_IOUT}, the actual output current can be calculated as: $IOUT = K_{IOUT} \times V_{IOUT} / (R_{IOUT} \times V_{REF\_IOUT})$. The actual output current limit is the lower of the limits set by IOUT pin or the IOUT_REG register bits. This pin function can be disabled when EN_IOUT_PIN bit is 0. If IOUT pin is not used, this pin should be pulled to PGND, do not leave floating.
IIN	10	AI	**Input Current Limit Setting –** IIN pin sets the maximum input current, and can be used to monitor the input current. A programming resistor to PGND is used to set the input current limit as $I_{LIM} = K_{ILIM} / R_{IIN}$. When the device is under input current regulation, the voltage at IIN pin is V_{REF_IILIM}. When IIN pin voltage is less than V_{REF_ILIM}, the actual input current can be calculated as: $IAC = K_{ILIM} \times V_{IIN} / (R_{IIN} \times V_{REF\_ILIM})$. The actual input current limit is the lower of the limits set by IIN pin or the IAC_DPM register bits. This pin function can be disabled when EN_IIN_PIN bit is 0. If IIN pin is not used, this pin should be pulled to PGND, do not leave floating.
NC	11	-	**No Connect -** Leave this pin floating , do not tie to PGND
VO_SNS	12	AI	**Output Voltage Sensing –** Kelvin connect directly to the output voltage regulation point.
SRN	13	AI	**Current-Sense Resistor, Negative Input –** A 0.47-µF ceramic capacitor is placed from SRN to SRP to provide differential-mode filtering. An optional 0.1-µF ceramic capacitor is placed from the SRN pin to PGND for common-mode filtering.
SRP	14	AI	**Current-Sense Resistor, Positive Input –** A 0.47-µF ceramic capacitor is placed from SRN to SRP to provide differential-mode filtering. A 0.1-µF ceramic capacitor is placed from the SRP pin to PGND for common-mode filtering.
NC	15	-	**No Connect -** Leave this pin floating, do not tie to PGND
NC	16	-	**No Connect -** Leave this pin floating, do not tie to PGND
MODE	17	AI	**Mode Programming resistor –** Connect a resistor from this pin to PGND to select between buck-boost or buck-only operation. Refer to MODE Pin Configuration section for more details.
SW2	18	AI	**Boost Side Half Bridge Switching Node –**
HIDRV2	19	AO	**Boost Side High-Side Gate Driver –** Connect to the boost high-side N-channel MOSFET gate.
BTST2	20	P	**Boost Side High-Side Power MOSFET Gate Driver Power Supply –** Connect a capacitor between BTST2 and SW2 to provide bias to the high-side MOSFET gate driver.
LODRV2	21	AO	**Boost Side Low-Side Gate Driver –** Connect to the boost low-side N-channel MOSFET gate.
PGND	22	-	**Power Ground Return –** The high current ground connection for the low-side gate drivers.
DRV_SUP	23	P	**Gate Drive Supply Input –** Voltage on this pin is used to drive the gates of buck-boost converter switching FET. Connect a 4.7-µF ceramic capacitor from DRV_SUP to power ground. REGN LDO voltage can be used as the gate driver supply for all switching FETs by connecting REGN to DRV_SUP pin. In high-voltage applications, it is possible to directly provide the DRV_SUP voltage with an external supply up to 12 V to achieve higher switching efficiency. See セクション 6.3.3.3 for more details.
REGN	24	P	**Internal Linear Regulator Output –** Connect a 4.7-µF ceramic capacitor from REGN to power ground. REGN LDO voltage can be used as the gate driver supply for all switching FETs by connecting REGN to DRV_SUP pin. In high-voltage applications, it is possible to directly provide the DRV_SUP voltage with an external supply up to 12 V to achieve higher switching efficiency. See セクション 6.3.3.3 for more details.
LODRV1	25	AO	**Buck Side Low-Side Gate Driver –** Connect to the buck low-side N-channel MOSFET gate.
BTST1	26	P	**Buck Side High-Side Power MOSFET Gate Driver Power Supply –** Connect a capacitor between BTST1 and SW1 to provide bias to the high-side MOSFET gate driver.
HIDRV1	27	AO	**Buck Side High-Side Gate Driver –** Connect to the buck high-side N-channel MOSFET gate.
SW1	28	AI	**Buck Side Half Bridge Switching Node –**

表 4-1. Pin Functions (続き)

PIN		I/O	DESCRIPTION
NAME	NO.		
ACN	29	AI	**Adapter Current-Sense Resistor, Negative Input** A 0.47-µF ceramic capacitor is placed from ACN to ACP to provide differential-mode filtering. An optional 0.1-µF ceramic capacitor is placed from the ACN pin to PGND for common-mode filtering.
ACP	30	AI	**Adapter Current-Sense Resistor, Positive Input** A 0.47-µF ceramic capacitor is placed from ACN to ACP to provide differential-mode filtering. A 0.1-µF ceramic capacitor is placed from the ACP pin to PGND for common-mode filtering
NC	31	-	**No Connect -** Leave this pin floating, do not tie to PGND
VAC	32	P	**Input Voltage Detection and Power** VAC is the input bias to power the IC. Connect a 1µF capacitor from pin to PGND. When Reverse Mode is enabled, pin 32 is regulated to VAC_REV.
	33		
ACUV	34	AI	**VAC Undervoltage Comparator Input –** Connect a resistor divider from VAC to PGND to program the undervoltage protection. When this pin falls below V_{REF_ACUV}, the device stops operation. The hardware limit for input voltage regulation reference is V_{ACUV_DPM}. The actual input voltage regulation setting is the higher of the pin-programmed value and the VAC_DPM register value. If ACUV programming is not used, pull this pin to VAC, do not leave floating.
ACOV	35	AI	**VAC Overvoltage Comparator Input –** Connect a resistor divider from VAC to PGND to program the overvoltage protection. When this pin rises above V_{REF_ACOV}, the device stops operation. If ACOV programming is not used, pull this pin to PGND, do not leave floating.
FSW_SYNC	36	DAI	**Switching Frequency and Synchronization Input –** An external resistor is connected to the FSW_SYNC pin and PGND to set the nominal switching frequency. This pin can also be used to synchronize the PWM controller to an external clock.
Thermal Pad	37	-	**Exposed pad beneath the IC –** Always solder the thermal pad to the board, and have vias on the thermal pad plane star-connecting to PGND and ground plane for high-current power converter. It also serves as a thermal pad to dissipate the heat.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	VAC, ACUV, ACOV, ACP, ACN,SRP, SRN, VO_SNS	–0.3	70	V
	SW1, SW2	–2	70	V
	SW1, SW2 (40ns transient)	–4	70	V
	$\overline{PG}$	–0.3	40	V
	BTST1, HIDRV1 with respect to SW1	–0.3	14	V
	BTST2, HIDRV2 with respect to SW2	–0.3	14	V
	DRV_SUP, LODRV1, LODRV2	–0.3	14	V
	ACP - ACN, SRP - SRN	–0.3	0.3	V
	$\overline{CE}$, FSW_SYNC, IOUT, IIN, $\overline{INT}$, REGN, SCL, SDA, MODE, STAT, TS	–0.3	6	V
Output Sink Current	$\overline{CE}$, $\overline{PG}$, STAT		5	mA
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{VAC}	Input voltage	4.2		60	V
V_{OUT}	Output voltage	0		60	V
V_{DRV_SUP}	DRV_SUP pin direct drive voltage range	4.0		12	V
F_{SW}	Switching Frequency	200		600	kHz
T_J	Junction temperature	–40		125	°C
T_A	Ambient temperature	–40		105	°C
C_{IN}	Buck-boost input capacitance	160			µF
C_{OUT}	Buck-boost output capacitance	160			µF
C_{REGN}	REGN capacitor	4.7			µF
C_{DRV_SUP}	DRV_SUP capacitor	4.7			µF
L	Switched Inductor	2.2		15	µH
R_{DCR}	Inductor DC Resistance	1.75		60	mΩ

5.3 Recommended Operating Conditions (続き)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
R_{AC_SNS}	Input current sense resistor	0[1]	5	10	mΩ
R_{OUT_SNS}	Output current sense resistor		5		mΩ
R_{IOUT}	IOUT programming pulldown resistor	0.0		100	kΩ
R_{IIN}	IIN programming pulldown resistor	0.0		50	kΩ

(1) When R_{AC_SNS} is 0mΩ, input current limit function is disabled

5.4 Thermal Information

THERMAL METRIC[1]		BQ25758 RRV 36 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (JEDEC[1])	29.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	18.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	9.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

VAC = ACP = ACN = SYS = SRP = SRN = 28V, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
QUIESCENT CURRENTS						
I_{Q_VAC}	Quiescent input current (I_{VAC})	Not switching		0.75	1	mA
I_{Q_REV}	Quiescent battery current in Reverse mode (I_{SRN} + I_{SRP})	Not switching		0.75	1	mA
VAC / BAT POWER UP						
V_{VAC_OP}	VAC operating range		4.2		60	V
V_{VAC_OK}	VAC converter enable threshold	VAC rising, no battery	4.2			V
V_{VAC_OKZ}	VAC converter disable threshold	VAC falling, no battery			3.5	V
V_{REF_ACUV}	ACUV comparator threshold to enter VAC_UVP	V_{ACUV} falling	1.095	1.1	1.106	V
$V_{REF\_ACUV\_HYS}$	ACUV comparator threshold hysteresis	V_{ACUV} rising		50		mV
$V_{VAC\_INT\_OV}$	VAC internal threshold to enter VAC_OVP	IN rising		66		V
$V_{VAC\_INT\_OVZ}$	VAC internal thresholds to exit VAC_OVP	IN falling		63		V
V_{REF_ACOV}	ACOV comparator threshold to enter VAC_OVP	V_{ACOV} rising	1.184	1.2	1.206	V
$V_{REF\_ACOV\_HYS}$	ACOV comparator threshold hysteresis	V_{ACOV} falling		50		mV
OUTPUT VOLTAGE REGULATION						
$V_{OUT\_REG\_RANGE}$	Output voltage regulation range		3.3		60	V
$V_{OUT\_REG\_ACC}$	I²C setting output voltage regulation accuracy	VOUT_REG = 0x0960		48		V
			-2		2	%
		VOUT_REG = 0x0578		28		V
			-2		2	%
$V_{OUT\_REG\_ACC}$	I²C setting output voltage regulation accuracy	VOUT_REG = 0x02EE		15		V
			-2		2	%
		VOUT_REG = 0x00FA		5		V
			-2		2	%
OUTPUT CURRENT REGULATION						
$I_{OUT\_REG\_RANGE}$	Output current regulation range		0.4		20	A
$I_{OUT\_REG\_ACC}$	I²C setting output current regulation accuracy	R_{OUT_SNS} = 5mΩ, VOUT = 12V, 36V, 55V. IOUT_REG = 0x012C		15		A
			–3		3	%
		R_{OUT_SNS} = 5mΩ, VOUT = 12V, 36V, 55V. IOUT_REG = 0x0064		5		A
			–3		3	%
		R_{OUT_SNS} = 5mΩ, VOUT = 12V, 36V, 55V. IOUT_REG = 0x0028		2		A
			–5		5	%
K_{IOUT}	Hardware output current limit set factor (Amperes of output current per kΩ on IOUT pin)	R_{OUT_SNS} = 5mΩ, R_{IOUT} = 10kΩ, 5kΩ, and 3.33kΩ	48	50	52	A x kΩ
V_{REF_IOUT}	IOUT pin voltage when IOUT pin is in regulation			2.0		V
INPUT CURRENT REGULATION						

5.5 Electrical Characteristics (続き)

VAC = ACP = ACN = SYS = SRP = SRN = 28V, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{IREG\_DPM\_ACC}$	I^2C setting input current regulation accuracy in forward mode	R_{AC_SNS} = 2mΩ, IAC_DPM = 0x00A0		20		A
			–3		3	%
		R_{AC_SNS} = 2mΩ, IAC_DPM = 0x0050		10		A
			–4		4	%
		R_{AC_SNS} = 2mΩ, IAC_DPM = 0x0028		5.0		A
			–7		7	%
K_{ILIM}	Hardware input current limit set factor (Amperes of input current per kΩ on ILIM_HIZ pin)	R_{AC_SNS} = 2mΩ, R_{ILIM} = 5kΩ, 2.5kΩ, and 1.67kΩ	48	50	52	A x kΩ
$V_{REF\_ILIM\_HIZ}$	ILIM_HIZ pin voltage when ILIM_HIZ pin is in regulation			2.0		V
$V_{IH\_ILIM\_HIZ}$	ILIM_HIZ input high threshold to enter HIZ mode	V_{ILIM_HIZ} rising	3.7			V
INPUT VOLTAGE REGULATION						
$V_{VREG\_DPM\_RANGE}$	Input voltage DPM regulation range		4.2		60	V
$V_{VREG\_DPM\_ACC}$	I^2C setting input voltage regulation accuracy	VAC_DPM = 0x076C		38		V
			–2		2	%
$V_{VREG\_DPM\_ACC}$	I^2C setting input voltage regulation accuracy in forward mode	VAC_DPM = 0x04E2		25		V
			–2		2	%
		VAC_DPM = 0x03B6		19		V
			–2		2	%
V_{ACUV_DPM}	ACUV pin voltage when in VDPM regulation		1.198	1.210	1.222	V
REVERSE MODE VOLTAGE REGULATION						
V_{REV_RANGE}	VAC Voltage regulation range in Reverse mode		3.3		60	V
V_{REV_ACC}	Voltage regulation accuracy in Reverse mode	VAC_REV = 0x0960		48		V
			–2		2	%
		VAC_REV = 0x0578		28		V
			–2		2	%
V_{REV_ACC}	VAC Voltage regulation accuracy in Reverse mode	VAC_REV = 0x02EE		15		V
			–2		2	%
		VAC_REV = 0x00FA		5		V
			–2		2	%
REVERSE MODE CURRENT REGULATION						
I_{IREV_ACC}	Input current regulation accuracy in Reverse mode	R_{AC_SNS} = 2mΩ, IAC_REV = 0x00A0		20		A
			–3.5		3.5	%
		R_{AC_SNS} = 2mΩ, IAC_REV = 0x0028		5.0		A
			–5.5		5.5	%
MULTI-LEVEL CURRENT LIMIT (OVERLOAD MODE)						
ILIM2	Temporary higher current limit for IIN or IOUT. Percentage above the IAC_REG or IOUT_REG register values. ILIM2 duration is t_{OVLD}	EN_OVLD = 1 and OVLD_ILIM2 = 0		150		%
		EN_OVLD = 1 and OVLD_ILIM2 = 1		200		%

5.5 Electrical Characteristics (続き)

VAC = ACP = ACN = SYS = SRP = SRN = 28V, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ILIM3	Maximum temporary current limit for IIN or IOUT. ILIM3 duration is t_{3L_OVLD}	Absolute maximum current limit across 5mΩ R_{AC_SNS} and/or 5mΩ R_{OUT_SNS}. EN_OVLD_3L = 1 and EN_OVLD = 1		20		A
ILIM2_IIN	Temporary higher current limit for IIN. Percentage above the IAC_REG register value	EN_OVLD = 1 and OVLD_ILIM2 = 0		150		%
		EN_OVLD = 1 and OVLD_ILIM2 = 1		200		%
ILIM2_IOUT	Temporary higher current limit for IOUT. Percentage above the IOUT_REG register value	EN_OVLD = 1 and OVLD_ILIM2 = 0		150		%
		EN_OVLD = 1 and OVLD_ILIM2 = 1		200		%
I_{BYPASS_OCP}	Bypass mode over-current threshold	R_{OUT_SNS} = 5mΩ, V_{SRP} - V_{SRN} rising, I_{OUT_REG} = 5A	4.5	5	5.5	A
THERMAL SHUTDOWN						
T_{SHUT}	Thermal shutdown rising threshold	Temperature increasing		150		°C
	Thermal shutdown falling threshold	Temperature decreasing		135		°C
REGN REGULATOR AND GATE DRIVE SUPPLY (DRV_SUP)						
V_{REGN}	REGN LDO output voltage	IREGN = 20mA	4.8	5	5.2	V
		VAC = 5V, IREGN = 20mA	4.35	4.6		V
I_{REGN}	REGN LDO current limit	VREGN = 4.5V	70			mA
V_{REGN_OK}	REGN OK threshold to allow switching	REGN rising		3.55		V
V_{DRV_UVPZ}	DRV_SUP under-voltage threshold to allow switching	DRV_SUP rising			3.7	V
V_{DRV_OVP}	DRV_SUP over-voltage threshold to disable switching	DRV_SUP rising	12.8	13.2	13.6	V
SWITCHING FREQUENCY AND SYNC						
f_{SW}	Switching Frequency	R_{FSW_SYNC} = 133kΩ	212	250	288	kHz
		R_{FSW_SYNC} = 50kΩ	425	500	575	kHz
V_{IH_SYNC}	FSW_SYNC input high threshold		1.3			V
V_{IL_SYNC}	FSW_SYNC input low threshold				0.4	V
PW_{SYNC}	FSW_SYNC input pulse width		80			ns
PWM DRIVERS						
R_{HIDRV1_ON}	Buck side high-side turnon resistance	V_{BTST1} - V_{SW1} = 5V		3.4		Ω
R_{HIDRV1_OFF}	Buck side high-side turnoff resistance	V_{BTST1} - V_{SW1} = 5V		1.0		Ω
$V_{BTST1\_REFRESH}$	Bootstrap refresh comparator threshold voltage	BTST1 falling, V_{BTST1} - V_{SW1} when low-side refresh pulse is requested	2.7	3.1	3.9	V
R_{LODRV1_ON}	Buck side low-side turnon resistance	VREGN = 5V		3.4		Ω
R_{LODRV1_OFF}	Buck side low-side turnoff resistance	VREGN = 5V		1.0		Ω
t_{DT1}	Buck side dead time, both edges			45		ns
R_{HIDRV2_ON}	Boost side high-side turnon resistance	V_{BTST2} - V_{SW2} = 5V		3.4		Ω
R_{HIDRV2_OFF}	Boost side high-side turnoff resistance	V_{BTST2} - V_{SW2} = 5V		1.0		Ω
$V_{BTST2\_REFRESH}$	Bootstrap refresh comparator threshold voltage	BTST2 falling, V_{BTST2} - V_{SW2} when low-side refresh pulse is requested	2.7	3.1	3.9	V
R_{LODRV2_ON}	Boost side low-side turnon resistance	VREGN = 5V		3.4		Ω
R_{LODRV2_OFF}	Boost side low-side turnoff resistance	VREGN = 5V		1.0		Ω

5.5 Electrical Characteristics (続き)

VAC = ACP = ACN = SYS = SRP = SRN = 28V, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

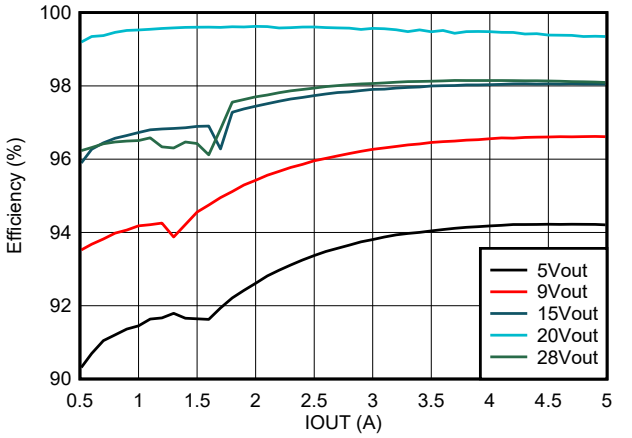
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DT2}	Boost side dead time, both edges			45		ns
ANALOG-TO-DIGITAL CONVERTER (ADC)						
t_{ADC_CONV}	Conversion-time, each measurement	ADC_SAMPLE[1:0] = 00		24		ms
		ADC_SAMPLE[1:0] = 01		12		ms
		ADC_SAMPLE[1:0] = 10		6		ms
ADC_{RES}	Effective resolution	ADC_SAMPLE[1:0] = 00	14	15		bits
		ADC_SAMPLE[1:0] = 01	13	14		bits
		ADC_SAMPLE[1:0] = 10	12	13		bits
ADC MEASUREMENT RANGE AND LSB						
I_{AC_ADC}	Input current ADC reading (positive or negative)	Range with 2mΩ R_{AC_SNS}	–50000		50000	mA
		LSB with 2mΩ R_{AC_SNS}		2		mA
I_{OUT_ADC}	Output current ADC reading (positive or negative)	Range with 5mΩ R_{BAT_SNS}	–20000		20000	mA
		LSB with 5mΩ R_{BAT_SNS}		2		mA
V_{AC_ADC}	Input voltage ADC reading	Range	0		65534	mV
		LSB		2		mV
V_{OUT_ADC}	VO_SNS voltage ADC reading	Range	0		65534	mV
		LSB		2		mV
TS_{ADC}	TS voltage ADC reading, as percentage of REGN	Range	0		99.9	%
		LSB		0.098		%
I^2C INTERFACE (SCL, SDA)						
V_{IH}	Input high threshold level		1.3			V
V_{IL}	Input low threshold level				0.4	V
V_{OL}	Output low threshold level	Sink current = 5mA			0.4	V
I_{IN_BIAS}	High-level leakage current	Pull up rail 3.3V			1	µA
LOGIC I/O PIN ($\overline{CE}$, $\overline{PG}$, STAT)						
V_{IH}	Input high threshold level ($\overline{CE}$)		1.3			V
V_{OL}	Output low threshold level ($\overline{CE}$, $\overline{PG}$, STAT)	Sink current = 5mA			0.4	V
V_{IL}	Input low threshold level ($\overline{CE}$)				0.4	V
I_{OUT_BIAS}	High-level leakage current ($\overline{CE}$, $\overline{PG}$, STAT)	Pull up rail 3.3V			1	µA

5.6 Timing Requirements

		MIN	NOM	MAX	UNIT
VAC / BAT POWER UP					
t_{ACOV_DGL}	Enter ACOV deglitch time, ACOV rising		100		µs
t_{ACOVZ_DGL}	Exit ACOV deglitch time, ACOV falling		12		ms
t_{ACUV_DGL}	Enter ACUV deglitch time, ACUV falling		100		µs
t_{ACUVZ_DGL}	Exit ACUV deglitch time, ACUV rising		12		ms
BATTERY-PACK NTC MONITOR					
t_{TS_DGL}	Deglitch time for TS threshold crossing		25		ms
MULTI-LEVEL CURRENT LIMIT (OVERLOAD MODE)					
t_{OVLD}	Overload time during which ILIM2 is allowed, TOVLD_SET = 0		25		ms
	Overload time during which ILIM2 is allowed, TOVLD_SET = 1		50		ms
t_{MAX}	Time required before a new overload event is allowed after an original overload event. EN_OVLD_TMAX = 1		100		ms
t_{OVLD_3L}	Deglitch time before engaging ILIM2, allowing maximum current for this time. EN_OVLD_3L = 1		1		ms
I²C INTERFACE					
f_{SCL}	SCL clock frequency			1000	kHZ
DIGITAL CLOCK AND WATCHDOG					
t_{LP_WDT}	I²C Watchdog reset time (EN_HIZ = 1, WATCHDOG[1:0] = 160s)	100	160		s
t_{WDT}	I²C Watchdog reset time (EN_HIZ = 0, WATCHDOG[1:0] = 160s)	130	160		s

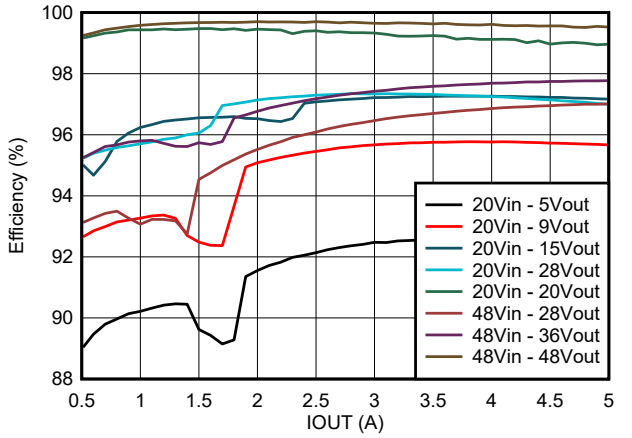
5.7 Typical Characteristics

C_{VAC} = 80 µF, C_{OUT}= 80 µF, f_{SW} = 250 kHz, L = 10 µH, T_A = 25°C (unless otherwise specified)



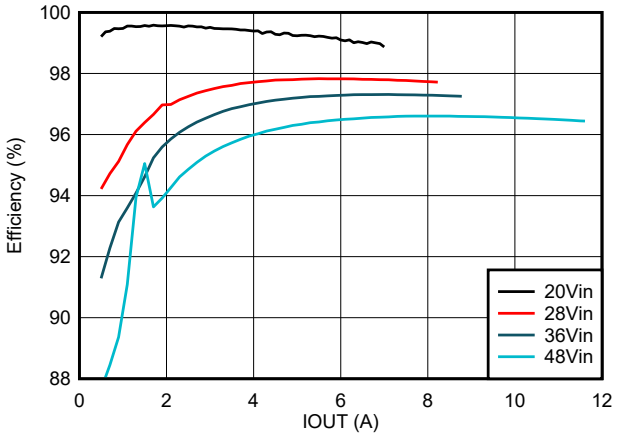
VAC = 20 V MOSFET = 40 V, 3.5 mΩ L = 4.7 µH, 17 mΩ f_{SW} = 450 kHz

図 5-1. 28-V USB-PD EPR Efficiency vs Output Current



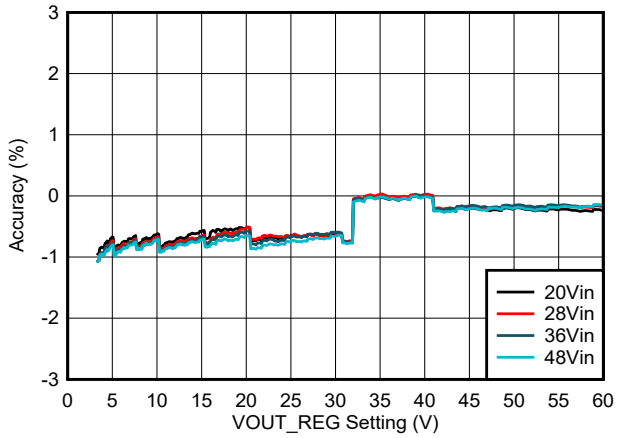
MOSFET = 80 V, 6.2 mΩ L = 10 µH, 19 mΩ f_{SW} = 450 kHz

図 5-2. 48-V USB-PD EPR Efficiency vs Output Current



VOUT = 20 V MOSFET = 80 V, 2.9 mΩ L = 10 µH, 12 mΩ

図 5-3. 48-V USB-PD EPR Efficiency vs Output Current with 20-V Fixed Output



IOUT = 3 A f_{SW} = 450 kHz

図 5-4. Output Voltage Accuracy vs VOUT Setting

6 Detailed Description

6.1 Overview

BQ25758 is a wide voltage, bidirectional switched-mode synchronous buck-boost controller. The device offers high-efficiency voltage conversion over a wide voltage range with output CC-CV control. The device integrates all the loop compensation and 5-V gate drivers for the buck-boost converter, thereby providing a high density solution with ease of use. The switching frequency of the device can be programmed or forced to follow an external clock frequency via the FSW_SYNC pin. While switching under light-load, the device offers an optional Pulse Frequency Modulation (PFM) scheme to increase efficiency. In reverse mode, the device draws power from the output supply and regulates the input terminal voltage with an added constant current loop for protection.

Besides the I^2C host-controlled mode, the device also supports programmable hardware limits. Input current, and output current regulation targets can be set with single resistor on the IIN, and IOUT pins, respectively. By default, the device is programmed to provide 5-V output, and the target output voltage can be adjusted via the VOUT_REG register bits. Forward switching function is controlled via the $\overline{CE}$ pin.

The input operating window is programmed via the ACUV and ACOV pins. When the input voltage is outside the programmed window, the device automatically stops switching, and the $\overline{PG}$ pin pulls HIGH.

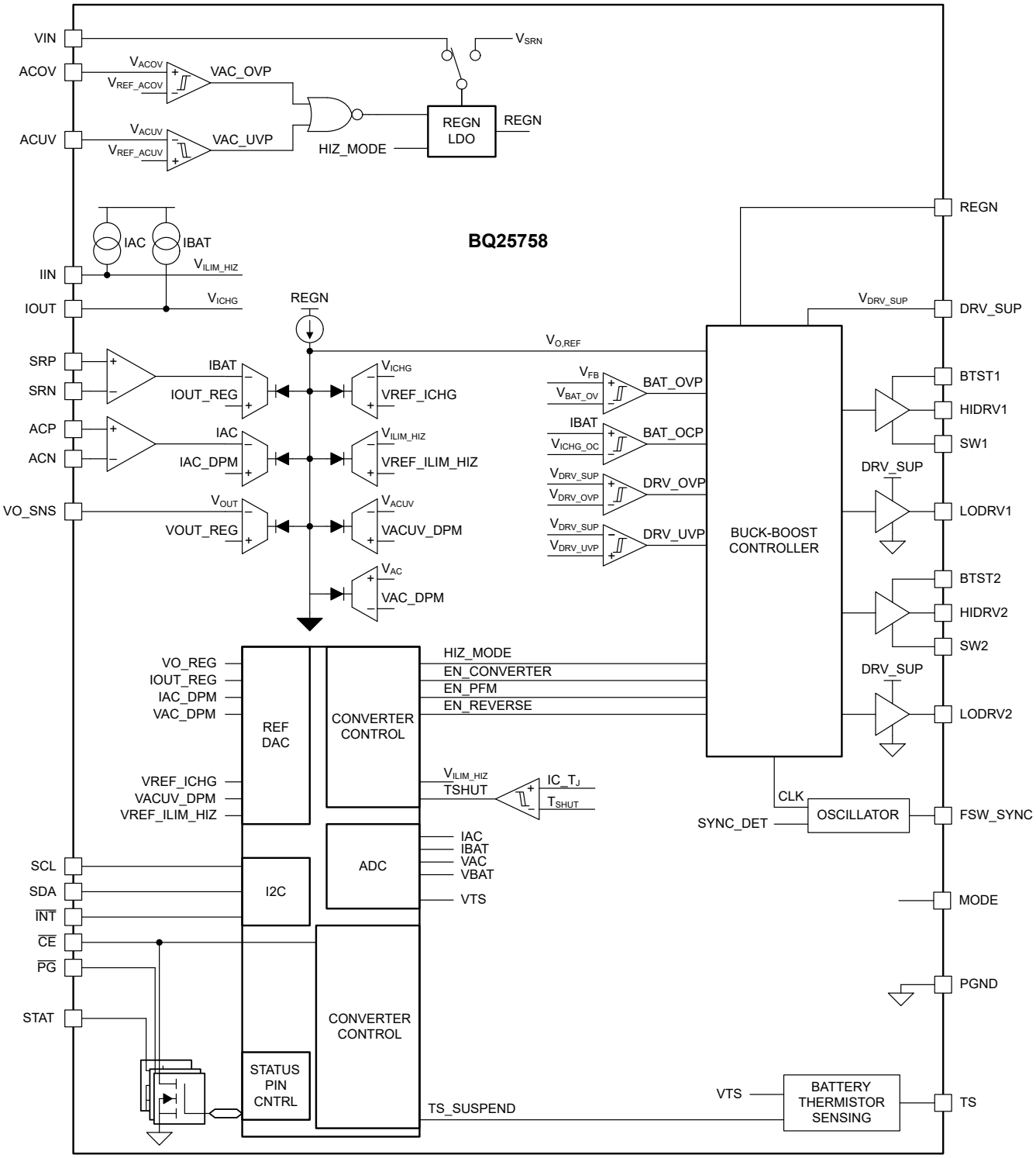
The BQ25758 provides various safety features including over-voltage and over-current protections on the input and the output. The thermal shutdown prevents operating when the junction temperature exceeds the T_{SHUT} limit.

The device has two status pins (STAT, and $\overline{PG}$) to indicate the switcher and input voltage status. These pins can be used to drive LEDs or communicate with a host processor. If needed, these pins can also be used as general purpose indicators and their status controlled directly by the I^2C interface. In addition, the $\overline{CE}$ pin can also be used as a general purpose indicator. The $\overline{INT}$ pin immediately notifies host when the device status changes, including faults.

The device also provides a 16-bit analog-to-digital converter (ADC) for monitoring input current, output current and input/output/thermistor voltages (IAC, IOUT, VAC, VOUT, TS).

The device comes with a 36-pin 5-mm × 6-mm QFN package with 0.5-mm pin pitch.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Device Power-On-Reset

The internal bias circuits are powered from either VAC or SRN. When VAC rises above V_{VAC_OK}, converter operation is allowed. When BAT rises above 3 V, reverse mode operation is allowed.

A POR occurs when one of these supplies rises above its corresponding V_{OK} level, while the other supply is below its corresponding V_{OK} level. After the POR, I^2C interface is ready for communication and all the registers are reset to default value. The host can access all the registers after POR.

6.3.2 Device Power-Up From Battery Without Input Source

If only battery is present and the voltage is above 3-V threshold, the device is ready for I^2C communication , and the converter is ready to start operation in reverse mode. The REGN LDO stays off to minimize the quiescent current. The ADC can be used to monitor all system parameters.

6.3.3 Device Power Up from Input Source

When a valid input source (V_{VAC_OK} < VAC and VAC within the ACUV and ACOV operating window) is detected, the $\overline{PG}$ pin pulls LOW. If converter operation is enabled, the device proceeds to enable the REGN LDO and power up the buck-boost converter.

6.3.3.1 VAC Operating Window Programming (ACUV and ACOV)

The VAC operating window can be programmed via the ACUV and ACOV pins using a three-resistor divider from VAC to PGND as shown in 図 6-1.

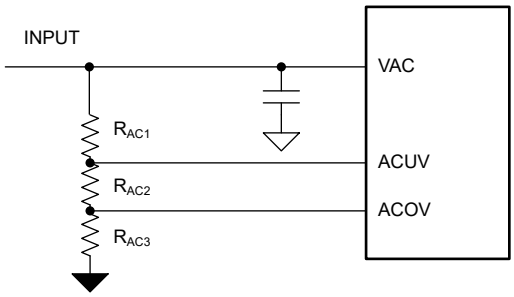


図 6-1. ACUV and ACOV Programming

When V_{ACUV} falls and reaches V_{ACUV_DPM}, the device enters input voltage regulation, thereby reducing the current. V_{ACUV} continues falling below V_{REF_ACUV}, the device automatically stops the converter and the $\overline{PG}$ pin pulls high.

System Note: if VAC_DPM register is programmed to a value higher than POR, the device regulates the VAC voltage to the higher of VAC_DPM register or V_{ACUV_DPM} pin voltage. Refer to セクション 6.3.4.3.2 for more information.

When V_{ACOV} rises above V_{REF_ACOV}, the device automatically stops the converter and the $\overline{PG}$ pin pulls high.

The following equations govern the relationship between the resistor divider and the target operating voltage window programmed by ACOV and ACUV pins:

$$V_{ACOV\_TARGET} = V_{REF\_ACOV} \times \frac{R_{AC1} + R_{AC2} + R_{AC3}}{R_{AC3}} \quad (1)$$

$$V_{ACUV\_TARGET} = V_{REF\_ACUV} \times \frac{R_{AC1} + R_{AC2} + R_{AC3}}{R_{AC2} + R_{AC3}} \quad (2)$$

If unused, tie ACUV to VAC and ACOV to PGND in order to apply the internal VAC operating window (V_{VAC_OP}).

6.3.3.2 MODE Pin Configuration

The MODE pin can be used to configure the device as either a buck-boost or buck-only configuration. When configured as buck-only typical inductor value used must be provided to appropriately compensate the converter. The closest inductor to the values presented below should be programmed via the MODE pin. When configured in buck-only mode, the device operates as a buck converter and MOSFETs Q3 and Q4 have to be removed. This is demonstrated in 図 7-25.

At POR, the device detects the MODE pin pull down resistance, then sets the device operating mode as shown below. The MODE pin resistance detection is only done one time at the device POR, after that, the converter will not sense the MODE pin voltage any more. Follow the resistance listed in the table below to set the desired operating mode. The surface mount resistor with ±1% or ±2% tolerance is recommended.

表 6-1. MODE Pin Resistance Configuration Options

OPERATION	L (nom)	R_{DCR} (min)	R_{DCR} (max)	TYPICAL RESISTANCE AT MODE PIN
Buck-Boost, device detects inductance automatically	2.2 µH - 15 µH	L/DCR = 1260 µs(1)	60 mΩ	≤3.0 kΩ
Buck-Only	3.3 µH	2.6 mΩ	60 mΩ	4.7 kΩ
Buck-Only	4.7 µH	3.7 mΩ	60 mΩ	6.04 kΩ
Buck-Only	5.6 µH	4.4 mΩ	60 mΩ	8.2 kΩ
Buck-Only	6.8 µH	5.4 mΩ	60 mΩ	10.5 kΩ
Buck-Only	8.2 µH	6.5 mΩ	60 mΩ	13.7 kΩ
Buck-Only	10 µH	7.9 mΩ	60 mΩ	17.4 kΩ
Buck-Only	15 µH	11.9 mΩ	60 mΩ	≥27.0 kΩ

(1) The minimum DCR varies as a function of selected inductor: for example, a 10-µH inductor supports 7.9 mΩ as the minimum DCR.

6.3.3.3 REGN Regulator (REGN LDO)

The REGN LDO regulator provides a regulated bias supply for the IC and the TS external resistors. Additionally, REGN voltage can be used to drive the buck-boost switching FETs directly by tying the DRV_SUP pin to REGN. The pull-up rail of $\overline{PG}$, STAT can be connected to REGN as well. The REGN LDO is enabled when below conditions are valid:

1. VAC voltage above V_{VAC_OK} and converter operation is enabled in forward mode.
2. BAT voltage above 3 V in Reverse mode and Reverse Mode is enabled (EN_REV = 1)

At high input voltages and/or large gate drive requirements, the power loss from gate driving via the REGN LDO can be excessive. This power for the gate drivers can be provided externally by directly driving the DRV_SUP pin with a high efficiency supply ranging from 4.5 V to 12 V. This supply should be able to provide at least 50 mA or more as required to drive the switching FET gate charge.

The power dissipation for driving the gates via the REGN LDO is: $P_{REGN} = (VAC - V_{REGN}) \times Q_{G(TOT)1,2,3,4} \times f_{SW}$, where $Q_{G(TOT)1,2,3,4}$ is the sum of the total gate charge for all switching FETs and f_{SW} is the programmed switching frequency. The Safe Operating Area (SOA) below is based on a 1-W power loss limit.

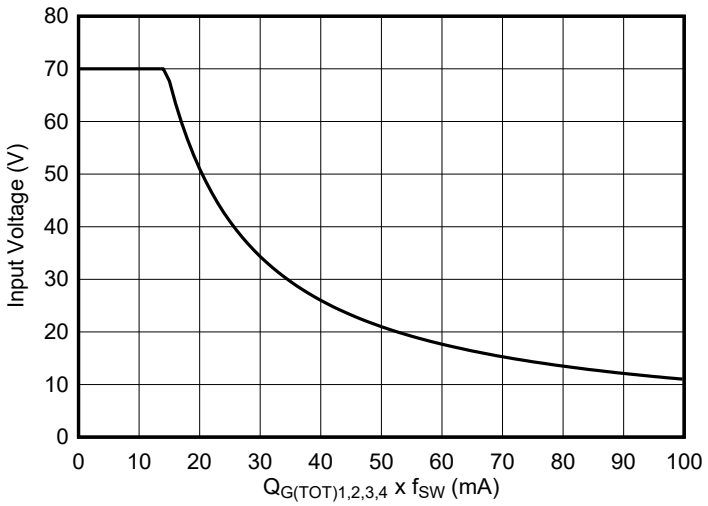


図 6-2. REGN LDO Safe Operating Area (SOA)

6.3.3.4 Compensation-Free Buck-Boost Converter Operation

The device integrates all the loop compensation, thereby providing a high density solution with ease of use.

The converter employs a synchronous buck-boost converter that allows conversion from a wide range of input voltage sources. The converter operates in buck, buck-boost or boost mode. The converter can operate uninterruptedly and continuously across the three operation modes. During buck-boost mode, the converter alternates a SW1 pulse with a SW2 pulse, with effective switching frequency interleaved among these pulses for highest efficiency operation.

During boost mode operation, the HS FET is forced to turn on for 225 ns in each switching cycle to ensure inductor energy is delivered to the output, effectively limiting the maximum boosting ratio. For example, when device is configured to switch at 500 kHz, the switching period is 2 µs, yielding a duty cycle limit of (1 - 0.225 µs/2 µs) = 88.75%. Given a 5-V input, this translates to a maximum 44-V output assuming 100% efficiency. The true output will be lower than this ideal limit. At lower switching frequencies, the maximum duty cycle increases, making the limitation less significant.

表 6-2. Switching MOSFET Operation

MODE	BUCK	BUCK-BOOST	BOOST
HS BUCK FET	Switching at f_{SW}	Switching (f_{SW} interleaved between SW1 and SW2)	ON
LS BUCK FET	Switching at f_{SW}	Switching (f_{SW} interleaved between SW1 and SW2)	OFF
LS BOOST FET	OFF	Switching (f_{SW} interleaved between SW1 and SW2)	Switching at f_{SW}
HS BOOST FET	ON	Switching (f_{SW} interleaved between SW1 and SW2)	Switching at f_{SW}

6.3.3.4.1 Light-Load Operation

In order to improve converter light-load efficiency, the device switches to Pulse Frequency Modulation (PFM) control at light load when the EN_PFM bit is set to 1. The effective switching frequency will decrease accordingly when output load decreases.

EN_PFM bit is automatically cleared to 0 every time the converter starts and a valid SYNC clock input is detected on the FSW_SYNC pin, thereby ensuring fixed frequency operation regardless of output current. The bit can be overwritten to 1 to allow PFM after startup even when SYNC signal is present.

Light-load PFM mode can be disabled by clearing the EN_PFM bit. In this case, the device switches in PWM mode at a fixed switching frequency.

6.3.3.5 Switching Frequency and Synchronization (FSW_SYNC)

The device switching frequency can be programmed between 200 kHz to 600 kHz using a resistor from the FSW_SYNC pin to PGND. The R_{FSW} resistor is related to the nominal switching frequency (f_{SW}) by the equation:

$$R_{FSW} = \frac{1}{10 \times \left(f_{SW} \times 5 \times 10^{-12} - 500 \times 10^{-9}\right)} \quad (3)$$

This pin must be pulled to PGND using a R_{FSW}, do not leave floating. In addition to programming the nominal switching frequency, the FSW_SYNC pin can also be used to synchronize the internal oscillator to an external clock signal. The synchronization feature works over the same range as the switching frequency: 200-kHz to 600-kHz range.

表 6-3. Common R_{FSW} and Switching Frequency Values

R_{FSW} (kΩ)	SWITCHING FREQUENCY (kHz)
200	200
133	250
100	300
80	350
66.67	400
57.1	450
50	500
44.4	550
40	600

6.3.3.6 Device HIZ Mode

When a valid input supply is present, it is possible to force the device into HIZ Mode which disables switching, disables REGN LDO. The system load is provided by the battery in this mode. The controller enters HIZ Mode when EN_HIZ bit is set to 1 or the IIN pin is pulled above $V_{IH\_ILIM\_HIZ}$ (refer to セクション 6.3.4.3.1.1).

If the device is operating in reverse mode with the converter turned on, and the device enters HIZ mode (EN_HIZ bit is set to 1 or IIN pin is pulled above $V_{IH\_ILIM\_HIZ}$), switching stops. Once HIZ mode condition is cleared by the host, the device resumes reverse mode operation.

The device exits HIZ Mode when the EN_HIZ bit is cleared to 0 and the IIN pin is pulled below 0.4 V.

6.3.4 Power Management

The device accommodates a wide range of input sources from 4.2 V up to 60 V.

6.3.4.1 Output Voltage Programming (VOUT_REG)

The output voltage at VO_SNS pin can be programmed via the I2C register setting (VOUT_REG). The output voltage range is from 3.3V to 60V with 20mV/step. The default VOUT_REG is set to 5V.

6.3.4.2 Output Current Programming (IOUT pin and IOUT_REG)

There are two distinct thresholds to limit the output current regulation point (if both are enabled, the lowest limit of these will apply):

1. IOUT pin pull down resistor (hardware control)
2. IOUT_REG register bits (host software control)

To set the maximum output current using the IOUT pin, a pull-down resistor to PGND is used. It is required to use a 5-mΩ R_{OUT_SNS} sense resistor. The output current limit is controlled by:

$$I_{OUT\_MAX} = \frac{K_{IOUT}}{R_{IOUT}} \quad (4)$$

The actual output current limit is the lower value between IOUT pin setting and I2C register setting (IOUT_REG). For example, if the register setting is 10A (0xC8), and ICHG pin has a 10-kΩ resistor (K_{ICHG} = 50 A-kΩ) to ground for 5A, the actual output current limit is 5A. The device regulates IOUT pin at 2V. If ICHG pin voltage exceeds 2V, the device enters output current regulation (CC mode).

The IOUT pin can also be used to monitor output current when device is not in output current regulation. The voltage on IOUT pin (V_{IOUT}) is proportional to the actual output current. IOUT pin can be used to monitor output current with the following relationship:

$$I_{OUT} = \frac{K_{IOUT} \times V_{IOUT}}{R_{IOUT} \times 2V} \quad (5)$$

For example, if IOUT pin is set with 10-kΩ resistor, and the IOUT voltage 1.0V, the actual output current is between 2.4A to 2.6A (based on K_{IOUT} specified).

If IOUT pin is shorted to PGND, the current limit is set by the IOUT_REG register. If hardware output current limit function is not needed, it is recommended to short this pin to PGND. The IOUT pin function can be disabled by setting the EN_IOUT_PIN bit to 0 (recommended when pin is shorted to PGND). When the pin is disabled, output current limit and monitoring functions via IOUT pin are not available.

To set the maximum output current using the IOUT_REG register bits, write to the IOUT_REG register bits. The current limit range is from 400mA to 20,000mA with 50mA/step. The default IOUT_REG is set to maximum code, allowing IOUT pin to limit the current in hardware.

6.3.4.3 Dynamic Power Management: Input Voltage and Input Current Regulation

The device features Dynamic Power Management (DPM), which continuously monitors the input current and input voltage. When input source is over-loaded, either the current exceeds the input current limit (lower of IAC_DPM or IIN pin setting), or the voltage falls below the input voltage limit (higher of VAC_DPM or ACUV pin setting, V_{ACUV_DPM}). The device then reduces the current until the input current falls below the input current limit and the input voltage rises above the input voltage limit.

When the current is reduced to zero, but the input source is still overloaded, the input voltage continues to drop. Once the input voltage drops below the ACUV limit ($V_{ACUV} < V_{REF\_ACUV}$), the controller stops switching.

6.3.4.3.1 Input Current Regulation

The total input current is a function of the system supply current and the current. System current normally fluctuates as portions of the systems are powered up or down. Without DPM, the source must be able to supply the maximum system current and the maximum input current simultaneously. By using DPM, the converter reduces the current when the input current exceeds the input current limit set by the lower of IAC_DPM register bits, or IIN pin. This allows the current capability of the input source to be lowered, reducing system cost.

There are two thresholds to limit the input current (if both are enabled, the lower limit of these two will apply):

1. IAC_DPM register bits (host software control)
2. IIN pull down resistor (hardware control)

To set the maximum current using the IAC_DPM register bits, write to the IAC_DPM register bits. When using a 2-mΩ resistor, the input current limit range is from 1 A to 50 A with 125 mA/step. The default IAC_DPM is set to maximum code, allowing IIN pin to limit the current in hardware.

To set the maximum current using the IIN pin, refer to セクション 6.3.4.3.1.1.

Although both limits are referenced to a 2-mΩ sense resistor, other values can also be used. A larger sense resistor provides a larger sense voltage and higher regulation accuracy, but at the expense of higher conduction loss. For example, using a 5-mΩ resistor yields programmability from 400 mA to 20 A with 50 mA/step.

6.3.4.3.1.1 IIN Pin

To set the maximum input current using the IIN pin, a pull-down resistor to PGND is used. When using a 2-mΩ R_{AC_SNS} resistor, the input current limit is controlled by: $I_{AC\_MAX} = K_{ILIM} / R_{IIN}$.

The actual input current limit is the lower value between IIN pin setting and register setting (IAC_DPM). For example, if the register setting is 20 A, and IIN pin has a 5-kΩ resistor (K_{ILIM} = 50 A-kΩ) to ground for 10 A, the actual input current limit is 10 A. IIN pin can be used to set the input current limit when EN_IIN_PIN bit is set to 1. The device regulates the pin at $V_{REF\_ILIM\_HIZ}$. If pin voltage exceeds $V_{REF\_ILIM\_HIZ}$, the device enters input current regulation. Entering input current regulation through the pin sets the IAC_DPM_STAT and FLAG bits, and produces an interrupt to host. The interrupt can be masked via the IAC_DPM_MASK bit.

The IIN pin can also be used to monitor input current. When not in input current regulation, the voltage on IIN pin (V_{IIN}) is proportional to the input current. Pin voltage can be used to monitor input current with the following relationship: $IAC = K_{ILIM} \times V_{IIN} / (R_{IIN} \times V_{REF\_ILIM\_HIZ})$.

For example, if the pin is set with 5-kΩ resistor, and the pin voltage is 1.0 V, the actual input current is between 4.8 A to 5.2 A (based on K_{ILIM} specified).

If IIN pin is shorted, the input current limit is set by the IAC_DPM register. If hardware input current limit function is not needed, it is recommended to short this pin to GND. If IIN pin is pulled above $V_{IH\_ILIM\_HIZ}$, the device enters HIZ mode (refer to セクション 6.3.3.6). The IIN pin function can be disabled by setting the EN_IIN_PIN bit to 0. When the pin is disabled, input current limit and monitoring functions as well as HIZ mode control via the pin are not available.

6.3.4.3.2 Input Voltage Regulation

In addition to input current regulation, the device also offers input voltage regulation to limit the input power. This is especially useful when dealing with input sources such as solar panels, where the operating voltage must be controlled to extract the maximum power. Alternatively, if the input source current limitation is not known, input voltage regulation can be used to limit the power draw from the input source. By using input voltage regulation, the converter reduces the current when the input voltage falls below the input voltage limit set by the higher of VAC_DPM register bits, or ACUV pin.

There are two thresholds to limit the input voltage (the higher limit of these will apply)

1. VAC_DPM register bits (host software control)
2. ACUV pin falling threshold (hardware control)

To set the minimum input voltage using the VAC_DPM register bits, write the desired value directly to the VAC_DPM register bits. The default VAC_DPM is set to minimum code, allowing ACUV pin to limit the input voltage in hardware.

To set the minimum input voltage using the ACUV pin, refer to セクション 6.3.3.1.

6.3.4.4 Bypass Mode

The device supports bypass mode to allow VOUT = VAC without regulation and highest efficiency. In this operating mode, the buck and boost high-side FETs (Q1 and Q4) are both turned on, while the Buck and Boost low-side FETs (Q2 and Q3) remain off. The input power is directly passed through the power stage to the output. The switching losses of MOSFETs and the inductor core loss are eliminated, thereby providing highest efficiency. The bypass mode can be enabled by setting the EN_BYPASS register bit to 1.

While device is in bypass mode, the current through R_{OUT_SNS} is monitored and compared against the IOUT_REG register setting. If the output current exceeds the register setting, the device automatically exits bypass mode and enters HIZ mode (completely disabling the power stage). The IBAT_OCP_STAT bit is set, and an INT pulse is asserted to signal the host. To recover from this fault, it is recommended to clear the EN_HIZ bit.

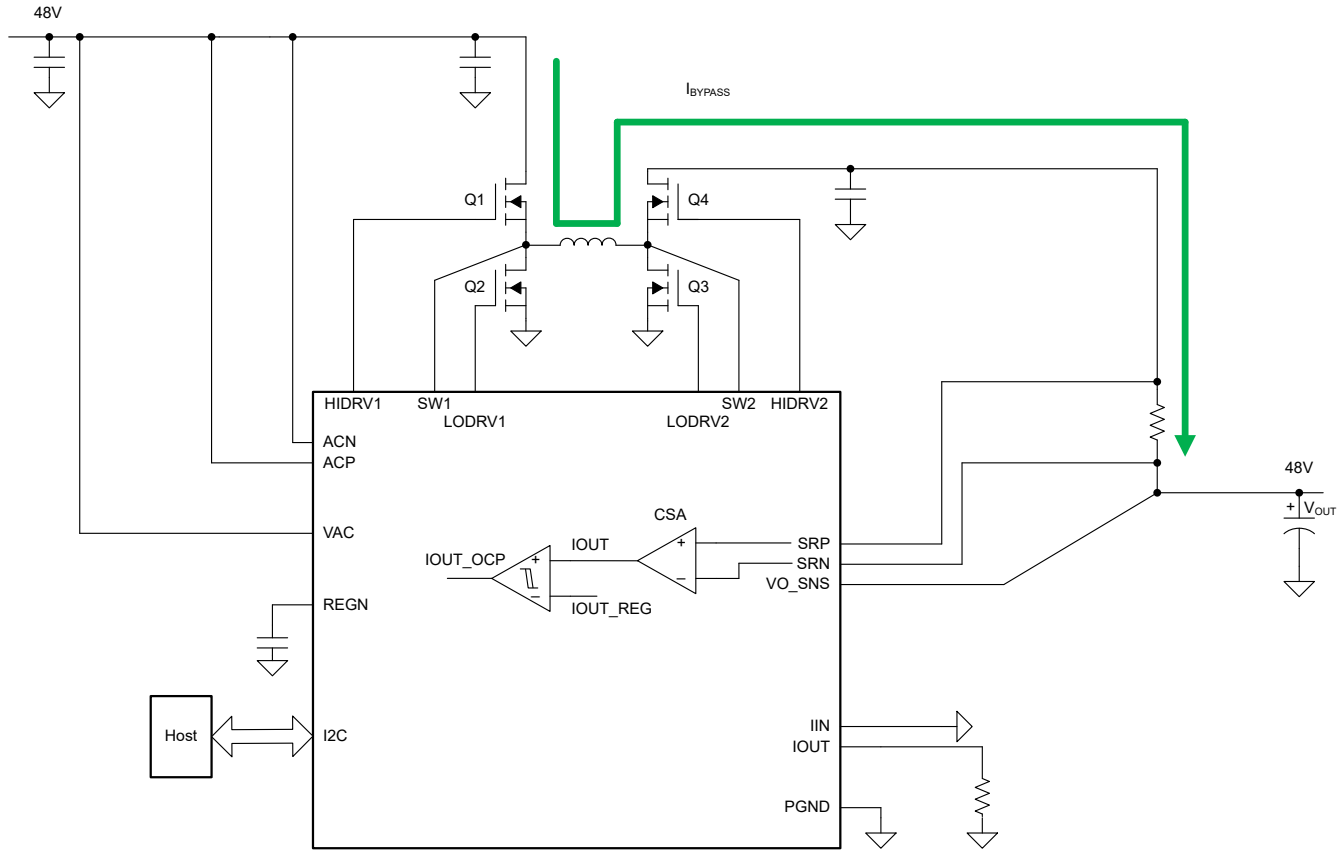


図 6-3. BQ25758 Bypass Mode Protection

6.3.5 Bidirectional Power Flow and Programmability

The device supports buck-boost bidirectional power flow with programmable parameters via the I2C.

In the forward direction, the power flows from INPUT to OUTPUT, and the device controls the output current, output voltage, as well as the input current and input voltage. The IOUT_REG register bits control the current across the sense resistor connected at SRP and SRN (R_{OUT_SNS}). The VOUT_REG register bits control the voltage regulation setpoint at VO_SNS pin. The IAC_DPM register bits control the input current across the sense resistor connected at ACP and ACN (R_{AC_SNS}). The VAC_DPM register bits control the input voltage at the VAC pin.

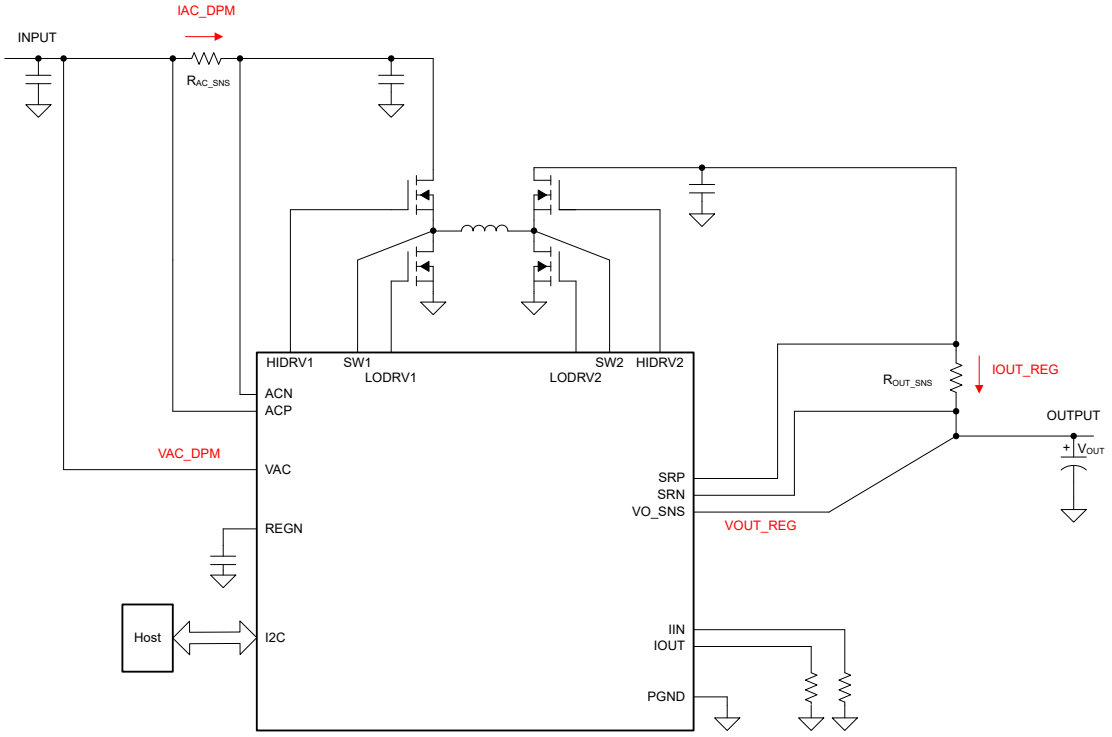


図 6-4. Programmability in Forward Mode

In the reverse direction, power flows from OUTPUT to INPUT, and the device control the input current as well as the input voltage. Reverse direction power flow can be enabled by setting the EN_REV bit to 1. The IAC_REV register bits control the reverse input current across the sense resistor connected at ACP and ACN (R_{AC_SNS}). The VAC_REV register bits control the reverse input voltage at the VAC pin.

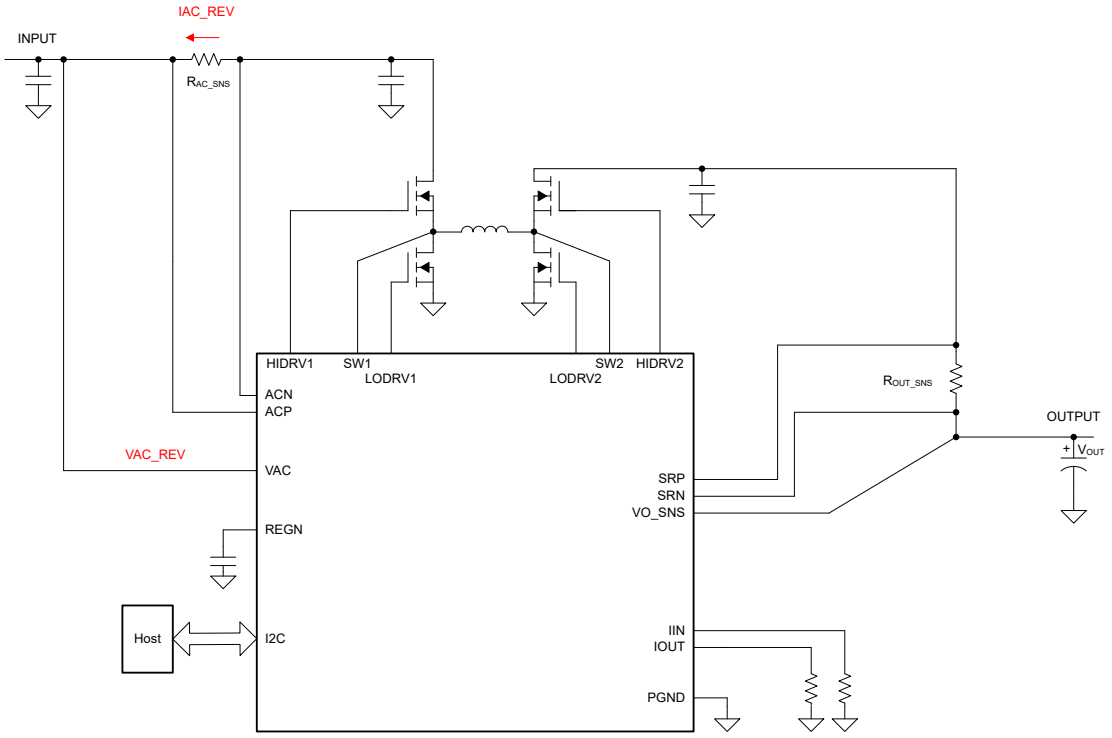


図 6-5. Programmability in Reverse Mode

The reverse mode operation can be stopped at any time by setting EN_REV bit to 0; this action disables the switching converter.

Note: When operating as buck-only configuration via the MODE pin, it is recommended to set EN_CHG = 0 before enabling reverse mode operation.

6.3.6 Integrated 16-Bit ADC for Monitoring

The device includes a 16-bit ADC to monitor critical system information based on the device's modes of operation. The ADC is allowed to operate if either the V_{VAC}>V_{VAC_OK} or VBAT>V_{REGN_OK} is valid. The ADC_EN bit provides the ability to enable and disable the ADC to conserve power. The ADC_RATE bit allows continuous conversion or one-shot behavior. After a one-shot conversion finishes, the ADC_EN bit is cleared, and must be re-asserted to start a new conversion.

The ADC_SAMPLE bits control the resolution and sample speed of the ADC. By default, ADC channels will be converted in one-shot or continuous conversion mode unless disabled in the ADC Function Disable register. If an ADC parameter is disabled by setting the corresponding bit, then the read-back value in the corresponding register will be from the last valid ADC conversion or the default POR value (all zeros if no conversions have taken place). If an ADC parameter is disabled in the middle of an ADC measurement cycle, the device will finish the conversion of that parameter, but will not convert the parameter starting the next conversion cycle. If all channels are disabled in one-shot conversion mode, the ADC_EN bit is cleared.

The ADC_DONE_STAT and ADC_DONE_FLAG bits signal when a conversion is complete in one-shot mode only. This event produces an INT pulse, which can be masked with ADC_DONE_MASK. During continuous conversion mode, the ADC_DONE_STAT bit has no meaning and will be '0'. The ADC_DONE_FLAG bit will remain unchanged in continuous conversion mode.

ADC conversion operates independently of the faults present in the device. ADC conversion will continue even after a fault has occurred (such as one that causes the power stage to be disabled), and the host must set ADC_EN = '0' to disable the ADC. ADC readings are only valid for DC states and not for transients. When host writes ADC_EN = 0, the ADC stops immediately, and ADC measurement values correspond to last valid ADC reading.

If the host wants to exit ADC more gracefully, it is possible to do either of the following:

1. Write ADC_RATE to one-shot, and the ADC will stop at the end of a complete cycle of conversions, or
2. Disable all ADC conversion channels, and the ADC will stop at the end of the current measurement.

When system load is powered from the battery (input source is removed, or device in HIZ mode), enabling the ADC automatically powers up REGN and increases the quiescent current. To keep the battery leakage low, it is recommended to duty cycle or completely disable the ADC.

6.3.7 Status Outputs ($\overline{PG}$, STAT and $\overline{INT}$)

6.3.7.1 Power Good Indicator ($\overline{PG}$)

The PG_STAT bit goes HIGH and the $\overline{PG}$ pin pulls LOW to indicate a good input source when a valid VAC voltage is detected. The $\overline{PG}$ pin can drive an LED. All conditions must be met to indicate power good:

1. V_{VAC_OK} < V_{VAC} < $V_{VAC\_INT\_OV}$
2. V_{ACUV} > V_{REF_ACUV}
3. V_{ACOV} < V_{REF_ACOV}
4. Device not in HIZ mode

The $\overline{PG}$ pin can be disabled via the DIS_PG_PIN bit. When disabled, this pin can be controlled to pull LOW using the FORCE_STAT3_ON bit.

6.3.7.2 Interrupt to Host ($\overline{INT}$)

In some applications, the host does not always monitor the controller operation. The $\overline{INT}$ pin notifies the system host on the device operation. By default, the following events will generate an active-low, 256-µs INT pulse.

1. Valid input source conditions detected (see conditions for $\overline{PG}$ pin)

2. Valid input source conditions removed (see conditions for $\overline{PG}$ pin)
3. Entering IAC_DPM regulation through register or IIN pin
4. Entering VAC_DPM regulation through register or ACUV pin
5. I^2C Watchdog timer expired
6. TS_STAT changes state (TS_STAT value change)
7. Junction temperature shutdown (TSHUT)
8. A rising edge on any of the *_STAT bits

Each one of these INT sources can be masked off to prevent INT pulses from being sent out when they occur. Three bits exist for each one of these events:

- The STAT bit holds the *current status* of each INT source
- The FLAG bit holds information on which source produced an INT, regardless of the current status
- The MASK bit is used to prevent the device from sending out INT for each particular event

When one of the above conditions occurs (a rising edge on any of the *_STAT bits), the device sends out an INT pulse and keeps track of which source generated the INT via the FLAG registers. The FLAG register bits are automatically reset to zero after the host reads them, and a new edge on STAT bit is required to re-assert the FLAG.

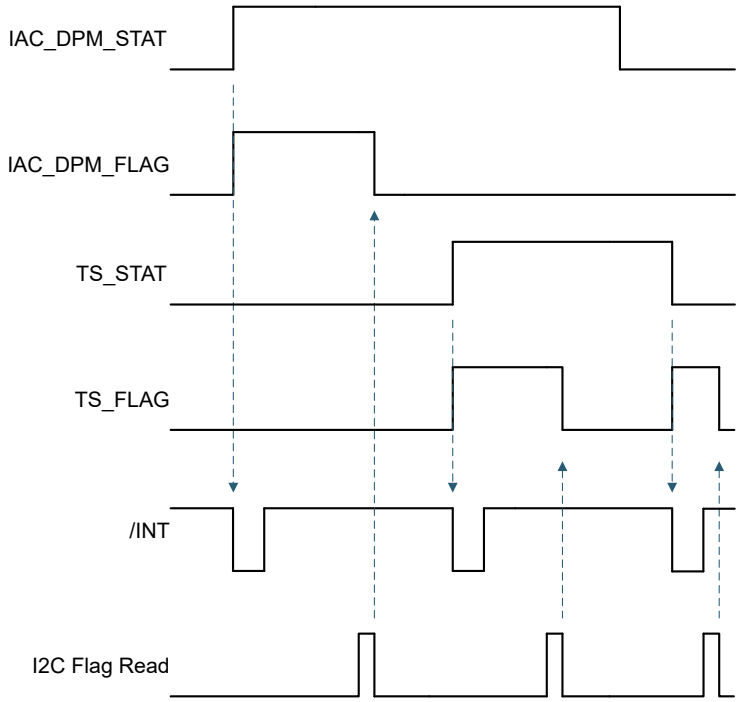


図 6-6. INT Generation Behavior Example

6.3.8 Protections

The device closely monitors the input and battery voltage, as well as switching FET currents for safe switch-mode operation.

6.3.8.1 Voltage and Current Monitoring

6.3.8.1.1 VAC Over-voltage Protection (VAC_OVP)

In order to protect downstream devices on the system rail, the input over-voltage threshold can be programed with the ACOV pin as $V_{VACOV} = V_{REF\_ACOV}$ (refer to セクション 6.3.3.1). The device also features an internal over-voltage protection preset at $V_{VAC\_INT\_OV}$. When the input voltage rises above the lower of these two thresholds, the device disables the controller. During input over-voltage, an INT pulse is asserted to signal the host, and the

VAC_OV_STAT, and _FLAG bits are set. Additionally, the PG_STAT bit is cleared and the $\overline{PG}$ pin pulls HIGH. The device automatically resumes operation when the over-voltage condition goes away.

6.3.8.1.2 VAC Under-voltage Protection (VAC_UVP)

In order to maintain a minimum operating voltage on the system rail, the input under-voltage threshold can be programed with the ACUV pin as V_{VACUV} = V_{REF_ACUV} (refer to セクション 6.3.3.1). The device also features an internal under-voltage protection preset at V_{VAC_OK}. When the input voltage falls below the higher of these two thresholds, the device disables the controller. During input under-voltage, an INT pulse is asserted to signal the host, and the VAC_UV_STAT, and _FLAG bits are set. Additionally, the PG_STAT bit is cleared and the $\overline{PG}$ pin pulls HIGH. The device automatically resumes operation when the under-voltage condition goes away.

6.3.8.1.3 Reverse Mode Over-voltage Protection (REV_OVP)

While operating the converter in reverse mode, the device monitors the reverse voltage, V_{VAC}. When V_{VAC} rises above regulation target and exceeds V_{REV_OVP}, the device stops switching, and waits for the voltage to fall below the threshold to resume switching. An INT pulse is asserted to the host.

6.3.8.1.4 Reverse Mode Under-voltage Protection (REV_UVP)

While operating the converter in reverse mode, the device monitors the reverse voltage, V_{VAC}. When V_{VAC} falls below the undervoltage threshold (programmable via SYSREV_UV register bit), the device stops switching, clears the EN_REV bit, and exits Reverse mode. During the over-voltage event duration, the REVERSE_STAT bit is cleared and the REVERSE_FLAG bit is set to indicate a fault in reverse mode. An INT pulse is also asserted to the host

6.3.8.1.5 DRV_SUP Under-voltage and Over-voltage Protection (DRV_OKZ)

The DRV_SUP pin must maintain a valid voltage between DRV_UVP and DRV_OVP for proper operation of the switching power converter stage. This is true both in forward mode and in reverse mode.

When DRV_SUP pin voltage falls below DRV_UVP threshold, the switching converter stops operation, an INT pulse is asserted to signal the host, the DRV_OKZ_STAT, and DRV_OKZ_FLAG bits are set to signal the fault.

When DRV_SUP pin voltage rises above DRV_OVP threshold, the switching converter stops operation, an INT pulse is asserted to signal the host, the DRV_OKZ_STAT, and DRV_OKZ_FLAG bit are set to signal the fault.

When the DRV pin returns to normal operating range, the device automatically resumes switching in either forward or reverse mode as configured before the fault.

6.3.8.1.6 REGN Under-voltage Protection (REGN_OKZ)

The REGN pin is driven by an internal regulator, and must maintain a voltage above REGN_OKZ for proper device operation. This is true both in forward mode and in reverse mode, and for the ADC to function in battery only mode.

If the internal regulator is overloaded externally, the pin voltage may drop. When REGN falls below REGN_OKZ threshold, the switching converter stops operation. When the fault is removed, the REGN voltage recovers automatically and switching resumes in either forward or reverse mode as configured before the fault.

6.3.8.2 Thermal Shutdown (TSHUT)

The device has thermal shutdown to turn off the converter when IC surface temperature exceeds TSHUT. The fault register bits TSHUT_STAT and TSHUT_FLAG are set and an INT pulse is asserted to the host. The converter turns back on when IC temperature is below TSHUT_HYS. Note that TSHUT protection is active both in forward and reverse mode of operation.

6.3.9 Serial Interface

The device uses I^2C compatible interface for flexible parameter programming and instantaneous device status reporting. I^2C is a bi-directional 2-wire serial interface. Only two open-drain bus lines are required: a serial data line (SDA), and a serial clock line (SCL). Devices can be considered as controllers or targets when performing

data transfers. A controller is a device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a target.

The device operates as a target device with address 0x6B, receiving control inputs from the controller device like a micro-controller or digital signal processor through the registers defined in the Register Map. Registers read outside those defined in the map, return 0xFF. The I^2C interface supports standard mode (up to 100 kbits/s), fast mode (up to 400 kbits/s), and fast mode plus (up to 1 Mbit/s). When the bus is free, both lines are HIGH. The SDA and SCL pins are open drain and must be connected to the positive supply voltage via a current source or pull-up resistor.

System Note: All 16-bit registers are defined as Little Endian, with the most-significant byte allocated to the higher address. 16-bit register writes must be done sequentially and are recommended to be programmed using multi-write approach described in the セクション 6.3.9.7.

6.3.9.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on SCL line is LOW. One clock pulse is generated for each data bit transferred.

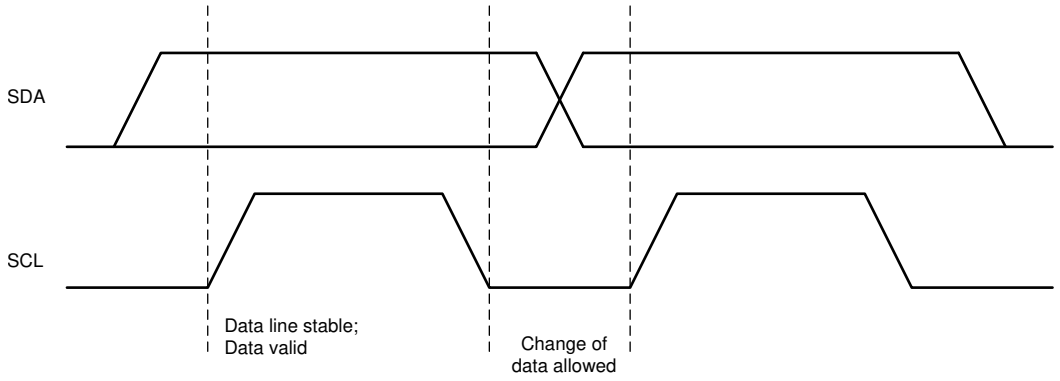


図 6-7. Bit Transfers on the I^2C Bus

6.3.9.2 START and STOP Conditions

All transactions begin with a START (S) and are terminated with a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the controller. The bus is considered busy after the START condition, and free after the STOP condition. When timeout condition is met, for example START condition is active for more than 2 seconds and there is no STOP condition triggered, the I^2C communication will automatically reset and communication lines are free for another transmission.

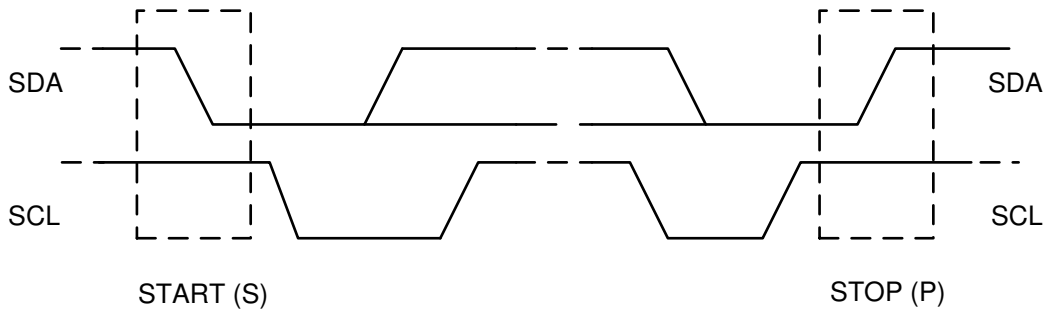


図 6-8. START and STOP Conditions on the I^2C Bus

6.3.9.3 Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an ACKNOWLEDGE (ACK) bit. Data is transferred with the Most Significant Bit (MSB) first. If a target cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the SCL line low to force the controller into a wait state (clock stretching). Data transfer then continues when the target is ready for another byte of data and releases the SCL line.

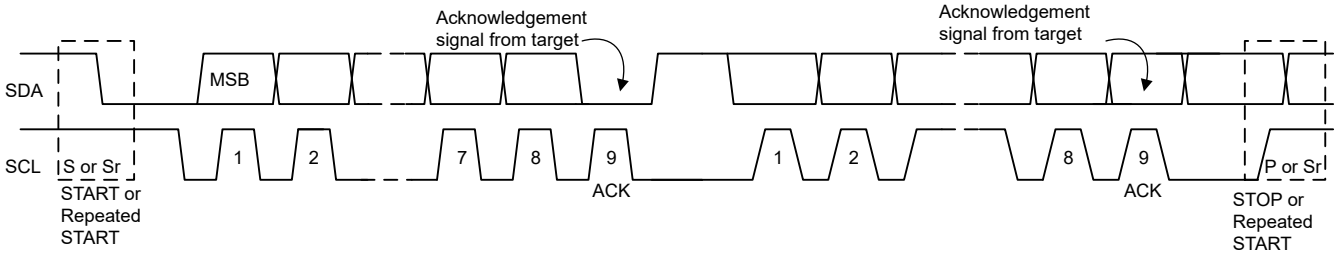


図 6-9. Data Transfer on the I²C Bus

6.3.9.4 Acknowledge (ACK) and Not Acknowledge (NACK)

The ACK signaling takes place after byte. The ACK bit allows the target to signal the controller that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the controller.

The controller releases the SDA line during the acknowledge clock pulse so the target can pull the SDA line LOW and it remains stable LOW during the HIGH period of this 9th clock pulse.

A NACK is signaled when the SDA line remains HIGH during the 9th clock pulse. The controller can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

6.3.9.5 Target Address and Data Direction Bit

After the START signal, a target address is sent. This address is 7 bits long, followed by the 8 bit as a data direction bit (bit R/ $\overline{W}$). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ). The device 7-bit address is defined as 1101 011' (0x6B) by default.

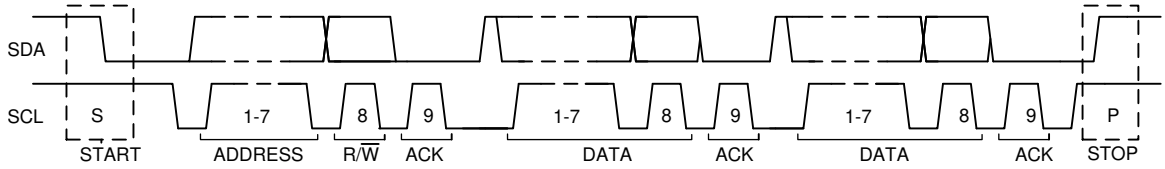


図 6-10. Complete Data Transfer on the I²C Bus

6.3.9.6 Single Write and Read

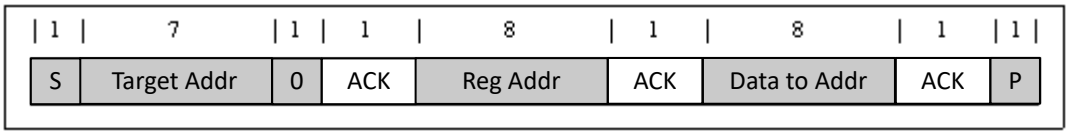


図 6-11. Single Write

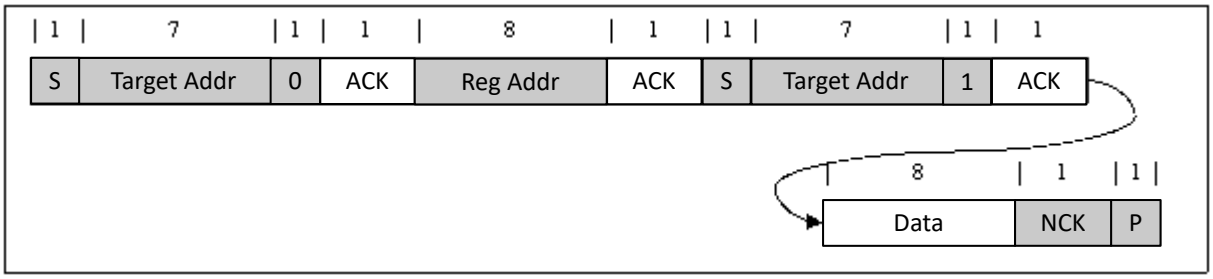


図 6-12. Single Read

If the register address is not defined, the IC sends back NACK and returns to the idle state.

6.3.9.7 Multi-Write and Multi-Read

The device supports multi-read and multi-write of all registers.

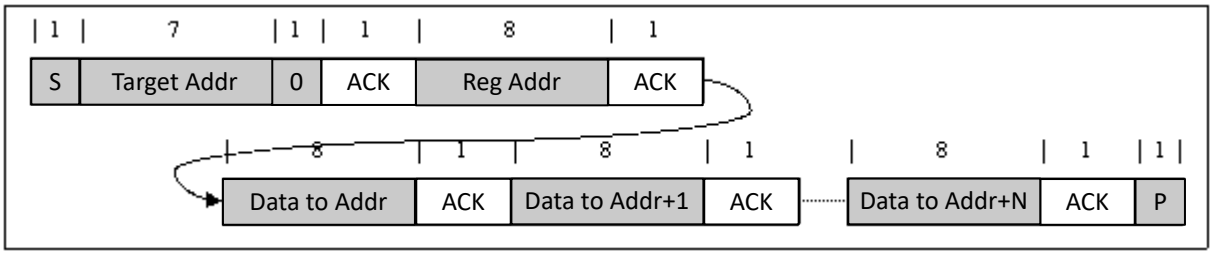


図 6-13. Multi-Write

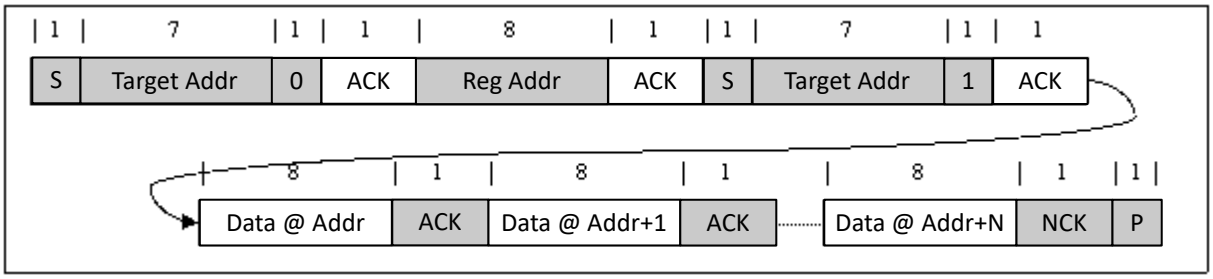


図 6-14. Multi-Read

6.4 Device Functional Modes

6.4.1 Host Mode and Default Mode

The device is a host controlled converter, but it can operate in default mode without host management. In default mode, the device can be used as an autonomous converter with no host or while host is in sleep mode. When the converter is in default mode, WD_STAT bit becomes HIGH, WD_FLAG is set to 1, and a $\overline{INT}$ is asserted low to alert the host (unless masked by WD_MASK). The WD_FLAG bit would read as a '1' upon the first read and then '0' upon subsequent reads. When the converter is in host mode, WD_STAT bit is LOW.

After power-on-reset, the device starts in default mode with watchdog timer expired. All the registers are in the default settings.

In default mode, the device regulates the output voltage to 5 V, with current limit as set by the IOUT pin (refer to セクション 6.3.4.2).

A write to any I^2C register transitions the converter from default mode to host mode, and initiates the watchdog timer. All the device parameters can be programmed by the host. To keep the device in host mode, the host has

to reset the watchdog timer by writing 1 to WD_RST bit before the watchdog timer expires (WD_STAT bit is set), or disable watchdog timer by setting WATCHDOG bits = 00.

When the watchdog timer is expired, the device returns to default mode and select registers are reset to default values as detailed in the Register Map section. The Watchdog timer will be reset on any write if the watchdog timer has expired. When watchdog timer expires, WD_STAT and WD_FLAG is set to 1, and /INT is asserted low to alert the host (unless masked by WD_MASK).

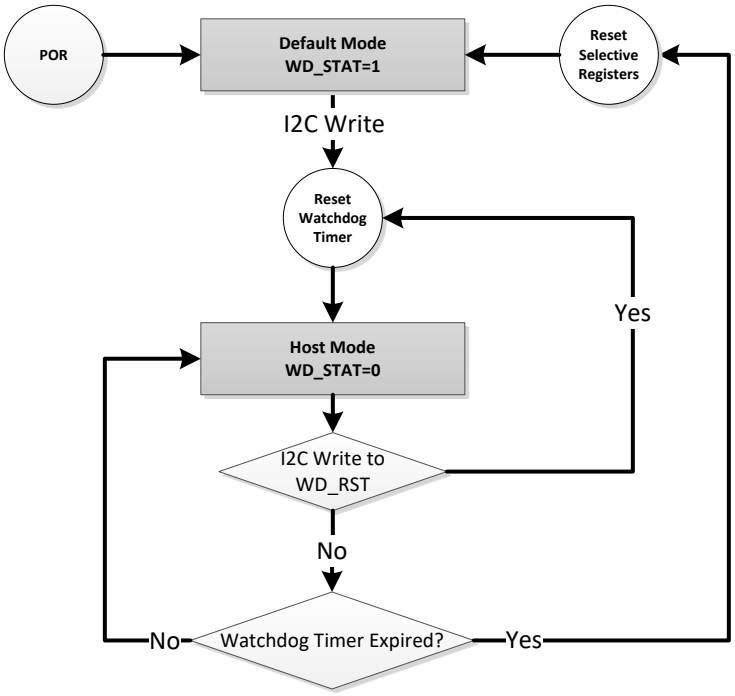


図 6-15. Watchdog Timer Flow Chart

6.4.2 Register Bit Reset

Beside the register reset by the watchdog timer in the default mode, the register and the timer could be reset to the default value by writing the REG_RST bit to 1. The register bits which can be reset by the REG_RST bit, are noted in the Register Map section. After the register reset, the REG_RST bit will go back from 1 to 0 automatically.

6.5 BQ25758 Registers

表 6-4 lists the memory-mapped registers for the BQ25758 registers. All register offset addresses not listed in 表 6-4 should be considered as reserved locations and the register contents should not be modified.

表 6-4. BQ25758 Registers

Address	Acronym	Register Name	Section
0x2	REG0x02_Output_Current_Limit	Output Current Limit	Go
0x4	REG0x04_Output_Voltage_Limit	Output Voltage Limit	Go
0x6	REG0x06_Input_Current_DPM_Limit	Input Current DPM Limit	Go
0x8	REG0x08_Input_Voltage_DPM_Limit	Input Voltage DPM Limit	Go
0xA	REG0x0A_Reverse_Mode_Input_Current_Limit	Reverse Mode Input Current Limit	Go
0xC	REG0x0C_Reverse_Mode_Input_Voltage_Limit	Reverse Mode Input Voltage Limit	Go
0x15	REG0x15_Timer_Control	Timer Control	Go
0x17	REG0x17_Converter_Control	Converter Control	Go
0x18	REG0x18_Pin_Control	Pin Control	Go
0x19	REG0x19_Power_Path_and_Reverse_Mode_Control	Power Path and Reverse Mode Control	Go
0x1B	REG0x1B_TS_Threshold_Control	TS Threshold Control	Go
0x1C	REG0x1C_TS_Region_Behavior_Control	TS Region Behavior Control	Go
0x1D	REG0x1D_TS_Reverse_Mode_Threshold_Control	TS Reverse Mode Threshold Control	Go
0x1E	REG0x1E_Bypass_and_Overload_Control	Bypass and Overload Control	Go
0x21	REG0x21_Status_1	Status 1	Go
0x22	REG0x22_Status_2	Status 2	Go
0x23	REG0x23_Status_3	Status 3	Go
0x24	REG0x24_Fault_Status	Fault Status	Go
0x25	REG0x25_Flag_1	Flag 1	Go
0x26	REG0x26_Flag_2	Flag 2	Go
0x27	REG0x27_Fault_Flag	Fault Flag	Go
0x28	REG0x28_Mask_1	Mask 1	Go
0x29	REG0x29_Mask_2	Mask 2	Go
0x2A	REG0x2A_Fault_Mask	Fault Mask	Go
0x2B	REG0x2B_ADC_Control	ADC Control	Go
0x2C	REG0x2C_ADC_Channel_Control	ADC Channel Control	Go
0x2D	REG0x2D_IAC_ADC	IAC ADC	Go
0x2F	REG0x2F_IOUT_ADC	IOUT ADC	Go
0x31	REG0x31_VAC_ADC	VAC ADC	Go
0x33	REG0x33_VOUT_ADC	VOUT ADC	Go
0x37	REG0x37_TS_ADC	TS ADC	Go
0x3B	REG0x3B_Gate_Driver_Strength_Control	Gate Driver Strength Control	Go
0x3C	REG0x3C_Gate_Driver_Dead_Time_Control	Gate Driver Dead Time Control	Go
0x3D	REG0x3D_Part_Information	Part Information	Go
0x62	REG0x62_Reverse_Mode_Current	Reverse Mode Current	Go

Complex bit access types are encoded to fit into small table cells. 表 6-5 shows the codes that are used for access types in this section.

表 6-5. BQ25758 Access Type Codes

Access Type	Code	Description
Read Type		

表 6-5. BQ25758 Access Type Codes (続き)

Access Type	Code	Description
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

6.5.1 REG0x02_Output_Current_Limit Register (Address = 0x2) [Reset = 0x0640]

REG0x02_Output_Current_Limit is shown in 表 6-6.

Return to the Summary Table.

I2C REG0x03=[15:8], I2C REG0x02=[7:0]

表 6-6. REG0x02_Output_Current_Limit Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:11	RESERVED	R	0x0		Reserved
10:2	IOUT_REG	R/W	0x190	Reset by: REG_RESET WATCHDOG	Output Current Regulation Limit with 5mΩ ROUT_SNS: Actual current is the lower of IOUT_REG and IOUT pin POR: 20000mA (190h) Range: 400mA-20000mA (8h-190h) Clamped Low Clamped High Bit Step: 50mA
1:0	RESERVED	R	0x0		Reserved

6.5.2 REG0x04_Output_Voltage_Limit Register (Address = 0x4) [Reset = 0x03E8]

REG0x04_Output_Voltage_Limit is shown in 表 6-7.

Return to the Summary Table.

I2C REG0x05=[15:8], I2C REG0x04=[7:0]

表 6-7. REG0x04_Output_Voltage_Limit Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:14	RESERVED	R	0x0		Reserved
13:2	VOUT_REG	R/W	0xFA	Reset by: REG_RESET	Output Voltage Regulation Limit: POR: 5000mV (FAh) Range: 3300mV-60000mV (A5h-BB8h) Clamped Low Clamped High Bit Step: 20mV
1:0	RESERVED	R	0x0		Reserved

6.5.3 REG0x06_Input_Current_DPM_Limit Register (Address = 0x6) [Reset = 0x0640]

REG0x06_Input_Current_DPM_Limit is shown in 表 6-8.

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I2C REG0x07=[15:8], I2C REG0x06=[7:0]

表 6-8. REG0x06_Input_Current_DPM_Limit Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:11	RESERVED	R	0x0		Reserved
10:2	IAC_DPM	R/W	0x190	Reset by: REG_RESET	Input Current DPM Regulation Limit with 5mΩ RAC_SNS: Actual input current limit is the lower of IAC_DPM and IIN pin POR: 20000mA (190h) Range: 400mA-20000mA (8h-190h) Clamped Low Clamped High Bit Step: 50mA
1:0	RESERVED	R	0x0		Reserved

6.5.4 REG0x08_Input_Voltage_DPM_Limit Register (Address = 0x8) [Reset = 0x0348]

REG0x08_Input_Voltage_DPM_Limit is shown in 表 6-9.

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I2C REG0x09=[15:8], I2C REG0x08=[7:0]

表 6-9. REG0x08_Input_Voltage_DPM_Limit Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:14	RESERVED	R	0x0		Reserved
13:2	VAC_DPM	R/W	0xD2	Reset by: REG_RESET	Input Voltage Regulation Limit: POR: 4200mV (D2h) Range: 4200mV-60000mV (D2h-BB8h) Clamped Low Clamped High Bit Step: 20mV
1:0	RESERVED	R	0x0		Reserved

6.5.5 REG0x0A_Reverse_Mode_Input_Current_Limit Register (Address = 0xA) [Reset = 0x0640]

REG0x0A_Reverse_Mode_Input_Current_Limit is shown in 表 6-10.

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I2C REG0x0B=[15:8], I2C REG0x0A=[7:0]

表 6-10. REG0x0A_Reverse_Mode_Input_Current_Limit Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:11	RESERVED	R	0x0		Reserved
10:2	IAC_REV	R/W	0x190	Reset by: REG_RESET	Input Current Regulation in Reverse Mode with 5mΩ RAC_SNS: POR: 20000mA (190h) Range: 400mA-20000mA (8h-190h) Clamped Low Clamped High Bit Step: 50mA
1:0	RESERVED	R	0x0		Reserved

6.5.6 REG0x0C_Reverse_Mode_Input_Voltage_Limit Register (Address = 0xC) [Reset = 0x03E8]

REG0x0C_Reverse_Mode_Input_Voltage_Limit is shown in 表 6-11.

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I2C REG0x0D=[15:8], I2C REG0x0C=[7:0]

表 6-11. REG0x0C_Reverse_Mode_Input_Voltage_Limit Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:14	RESERVED	R	0x0		Reserved
13:2	VAC_REV	R/W	0xFA	Reset by: REG_RESET	VAC Voltage Regulation in Reverse Mode: POR: 5000mV (FAh) Range: 3300mV-60000mV (A5h-BB8h) Clamped Low Clamped High Bit Step: 20mV
1:0	RESERVED	R	0x0		Reserved

6.5.7 REG0x15_Timer_Control Register (Address = 0x15) [Reset = 0x10]

REG0x15_Timer_Control is shown in 表 6-12.

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表 6-12. REG0x15_Timer_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7:6	RESERVED	R	0x0		Reserved
5:4	WATCHDOG	R/W	0x1	Reset by: REG_RESET	Watchdog timer control: 00b = Disable 01b = 40s 10b = 80s 11b = 160s
3	RESERVED	R	0x0		Reserved
2:1	RESERVED	R	0x0		Reserved
0	RESERVED	R	0x0		Reserved

6.5.8 REG0x17_Converter_Control Register (Address = 0x17) [Reset = 0x09]

REG0x17_Converter_Control is shown in 表 6-13.

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表 6-13. REG0x17_Converter_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7:6	RESERVED	R	0x0		Reserved
5	WD_RST	R/W	0x0	Reset by: REG_RESET	I2C Watchdog timer reset control: 0b = Normal 1b = Reset (bit goes back to 0 after timer reset)
4	DIS_CE_PIN	R/W	0x0	Reset by: REG_RESET	/CE pin function disable: 0b = /CE pin enabled 1b = /CE pin disabled

表 6-13. REG0x17_Converter_Control Register Field Descriptions (続き)

Bit	Field	Type	Reset	Notes	Description
3	EN_CHG_BIT_RESET_BEHAVIOR	R/W	0x1	Reset by: REG_RESET	Controls the EN_CHG bit behavior when WATCHDOG expires: 0b = EN_CHG bit resets to 0 1b = EN_CHG bit resets to 1
2	EN_HIZ	R/W	0x0	Reset by: REG_RESET WATCHDOG Adapter Plug In	HIZ mode enable: 0b = Disable 1b = Enable
1	EN_IBAT_LOAD	R/W	0x0	Sinks current from SRN to GND. Recommend to disable IBAT ADC (IBAT_ADC_DIS = 1) while this bit is active. Reset by: REG_RESET WATCHDOG	Battery Load (IBAT_LOAD) Enable: 0b = Disabled 1b = Enabled
0	EN_CHG	R/W	0x1	Reset by: REG_RESET WATCHDOG	Enable control: 0b = Disable 1b = Enable

6.5.9 REG0x18_Pin_Control Register (Address = 0x18) [Reset = 0xC0]

REG0x18_Pin_Control is shown in 表 6-14.

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表 6-14. REG0x18_Pin_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	EN_IOUT_PIN	R/W	0x1	Reset by: REG_RESET WATCHDOG	IOUT pin function enable: 0b = IOUT pin disabled 1b = IOUT pin enabled
6	EN_IIN_PIN	R/W	0x1	Reset by: REG_RESET WATCHDOG	IIN pin function enable: 0b = IIN pin disabled 1b = IIN pin enabled
5	DIS_PG_PIN	R/W	0x0	Reset by: REG_RESET	PG pin function disable: 0b = PG pin enabled 1b = PG pin disabled
4	DIS_STAT_PIN	R/W	0x0	Reset by: REG_RESET	STAT pin function disable: 0b = STAT pin enabled 1b = STAT pin disabled
3	FORCE_STAT4_ON	R/W	0x0	Reset by: REG_RESET	CE_STAT4 pin override: Can only be forced on if DIS_CE_PIN = 1 0b = CE_STAT4 open-drain off 1b = CE_STAT4 pulls LOW
2	FORCE_STAT3_ON	R/W	0x0	Reset by: REG_RESET	PG_STAT3 pin override: Can only be forced on if DIS_PG_PIN = 1 0b = PG_STAT3 open-drain off 1b = PG_STAT3 pulls LOW
1	RESERVED	R	0x0		Reserved

表 6-14. REG0x18_Pin_Control Register Field Descriptions (続き)

Bit	Field	Type	Reset	Notes	Description
0	FORCE_STAT_ON	R/W	0x0	Reset by: REG_RESET	STAT pin override: Can only be forced on if DIS_STAT_PIN = 1 0b = STAT open-drain off 1b = STAT pulls LOW

6.5.10 REG0x19_Power_Path_and_Reverse_Mode_Control Register (Address = 0x19) [Reset = 0x00]

REG0x19_Power_Path_and_Reverse_Mode_Control is shown in 表 6-15.

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表 6-15. REG0x19_Power_Path_and_Reverse_Mode_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	REG_RST	R/W	0x0	Reset by: REG_RESET	Register reset to default values: 0b = Not reset 1b = Reset (bit goes back to 0 after register reset)
6	EN_IAC_LOAD	R/W	0x0	Reset by: REG_RESET WATCHDOG	VAC Load (IAC_LOAD) Enable: 0b = Disabled 1b = Enabled
5	EN_PFM	R/W	0x0	This bit is reset upon a valid SYNC signal detection on FSW_SYNC pin. Host can set this bit back to 1 to force PFM operation even with a valid SYNC input Reset by: REG_RESET	Enable PFM mode to improve light-load efficiency: 0b = Disable (Fixed-frequency DCM operation) 1b = Enable (PFM operation)
4	RESERVED	R	0x0		Reserved
3	PWRPATH_REDUCE_VDRV	R/W	0x0	Reset by: REG_RESET WATCHDOG	Bypass Mode Gate-Drive Voltage Select: 0b = 10V 1b = 7V
2	RESERVED	R	0x0		Reserved
1	RESERVED	R	0x0		
0	EN_REV	R/W	0x0	Reset by: REG_RESET WATCHDOG Adapter Plug In	Reverse Mode control: 0b = Disable 1b = Enable

6.5.11 REG0x1B_TS_Threshold_Control Register (Address = 0x1B) [Reset = 0x82]

REG0x1B_TS_Threshold_Control is shown in 表 6-16.

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表 6-16. REG0x1B_TS_Threshold_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7:6	TS_T5	R/W	0x2		Reserved
5:4	RESERVED	R	0x0		Reserved
3:2	RESERVED	R	0x0		Reserved
1:0	RESERVED	R/W	0x2		Reserved

6.5.12 REG0x1C_TS_Region_Behavior_Control Register (Address = 0x1C) [Reset = 0x00]

REG0x1C_TS_Region_Behavior_Control is shown in 表 6-17.

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表 6-17. REG0x1C_TS_Region_Behavior_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	RESERVED	R	0x0		Reserved
6:5	RESERVED	R	0x0		Reserved
4	RESERVED	R	0x0		Reserved
3:2	RESERVED	R	0x0		Reserved
1	RESERVED	R	0x0	EN_VREG_TEMP_COMP and EN_JEITA cannot be set to 1 at the same time.	Reserved
0	RESERVED	R/W	0x0	Reset by: REG_RESET	Reserved

6.5.13 REG0x1D_TS_Reverse_Mode_Threshold_Control Register (Address = 0x1D) [Reset = 0x40]

REG0x1D_TS_Reverse_Mode_Threshold_Control is shown in 表 6-18.

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表 6-18. REG0x1D_TS_Reverse_Mode_Threshold_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7:6	BHOT	R/W	0x1	Reset by: REG_RESET	Reverse Mode TS HOT temperature threshold control: 00b = 37.7% (55C) 01b = 34.2% (60C) 10b = 31.25%(65C) 11b = Disable
5	BCOLD	R/W	0x0	Reset by: REG_RESET	Reverse Mode TS COLD temperature threshold control: 0b = 77.15% (-10C) 1b = 80% (-20C)
4:0	RESERVED	R	0x0		Reserved

6.5.14 REG0x1E_Bypass_and_Overload_Control Register (Address = 0x1E) [Reset = 0x20]

REG0x1E_Bypass_and_Overload_Control is shown in 表 6-19.

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表 6-19. REG0x1E_Bypass_and_Overload_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	RESERVED	R	0x0		Reserved
6	TOVLD_SET	R/W	0x0	Reset by: REG_RESET	TOVLD timer control: 0b = 25ms 1b = 50ms
5	SYSREV_UV	R/W	0x1	Reset by: REG_RESET	Reverse Mode System UVP: 0b = 80% of VSYS_REV target 1b = Fixed at 3.3V

表 6-19. REG0x1E_Bypass_and_Overload_Control Register Field Descriptions (続き)

Bit	Field	Type	Reset	Notes	Description
4	EN_BYPASS	R/W	0x0	Bypass mode only supported in forward mode, not operational in reverse mode. Reset by: REG_RESET WATCHDOG	Bypass mode control: Note the device automatically clears this bit and sets EN_HIZ bit when the output current exceeds IOUT_REG register value in bypass mode. 0b = Disable 1b = Enable
3	EN_OVLD_TMAX	R/W	0x0	Reset by: REG_RESET	TMAX counter control: 0b = Disable TMAX: allows new overload event after tOVLD and current falling below ILIM1 1b = Enable TMAX: allow new overload event after tMAX, even if current does not fall below ILIM1
2	EN_OVLD_3L	R/W	0x0	Reset by: REG_RESET	Three-level overload mode control: 0b = Disable 1b = Enable
1	OVLD_ILIM2	R/W	0x0	Reset by: REG_RESET	Overload higher current limit (percentage above IIN or IOUT): 0b = 1.5 1b = 2
0	EN_OVLD	R/W	0x0	Reset by: REG_RESET	Overload Mode control: 0b = Disable 1b = Enable

6.5.15 REG0x21_Status_1 Register (Address = 0x21) [Reset = 0x00]

REG0x21_Status_1 is shown in 表 6-20.

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表 6-20. REG0x21_Status_1 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	ADC_DONE_STAT	R	0x0		ADC conversion status (in one-shot mode only): 0b = Conversion not complete 1b = Conversion complete
6	IAC_DPM_STAT	R	0x0		Input Current regulation status: 0b = Normal 1b = In Input Current regulation (ILIM pin or IAC_DPM)
5	VAC_DPM_STAT	R	0x0		Input Voltage regulation status: 0b = Normal 1b = In Input Voltage regulation (VAC_DPM or VSYS_REV)
4	RESERVED	R	0x0		Reserved
3	WD_STAT	R	0x0		I2C Watchdog timer status: 0b = Normal 1b = WD timer expired

表 6-20. REG0x21_Status_1 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Notes	Description
2:0	CHARGE_STAT	R	0x0		Converter status: 000b = Not switching 001b = Reserved 010b = Reserved 011b = CC Mode 100b = CV Mode 101b = CV Mode 110b = CV Mode 111b = Reserved

6.5.16 REG0x22_Status_2 Register (Address = 0x22) [Reset = 0x00]

REG0x22_Status_2 is shown in 表 6-21.

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表 6-21. REG0x22_Status_2 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	PG_STAT	R	0x0		Input Power Good status: 0b = Not Power Good 1b = Power Good
6:4	TS_STAT	R	0x0		TS status: 000b = Normal 001b = TS Warm 010b = TS Cool 011b = TS Cold 100b = TS Hot
3:2	RESERVED	R	0x0		Reserved
1:0	RESERVED	R	0x0		Reserved

6.5.17 REG0x23_Status_3 Register (Address = 0x23) [Reset = 0x00]

REG0x23_Status_3 is shown in 表 6-22.

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表 6-22. REG0x23_Status_3 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7:6	RESERVED	R	0x0		Reserved
5:4	FSW_SYNC_STAT	R	0x0		FSW_SYNC pin status: 00b = Normal, no external clock detected 01b = Valid ext. clock detected 10b = Pin fault (frequency out-of-range) 11b = Reserved
3	RESERVED	R	0x0		Reserved
2	REVERSE_STAT	R	0x0		Converter Reverse Mode status: 0b = Reverse Mode off 1b = Reverse Mode On
1	RESERVED	R	0x0		Reserved
0	RESERVED	R	0x0		Reserved

6.5.18 REG0x24_Fault_Status Register (Address = 0x24) [Reset = 0x00]

REG0x24_Fault_Status is shown in 表 6-23.

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表 6-23. REG0x24_Fault_Status Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	VAC_UV_STAT	R	0x0		Input under-voltage status: 0b = Input Normal 1b = Device in Input under-voltage protection
6	VAC_OV_STAT	R	0x0		Input over-voltage status: 0b = Input Normal 1b = Device in Input over-voltage protection
5	IBAT_OCP_STAT	R	0x0		Battery over-current status: 0b = Battery current normal 1b = Battery over-current detected
4	VBAT_OV_STAT	R	0x0		Battery over-voltage status: 0b = Normal 1b = Device in Battery over-voltage protection
3	TSHUT_STAT	R	0x0		Thermal shutdown status: 0b = Normal 1b = Device in thermal shutdown protection
2	RESERVED	R	0x0		Reserved
1	DRV_OKZ_STAT	R	0x0	In battery-only mode with ADC disabled, this bit always reads '1'	DRV_SUP pin voltage status: 0b = Normal 1b = DRV_SUP pin voltage is out of valid range
0	RESERVED	R	0x0		Reserved

6.5.19 REG0x25_Flag_1 Register (Address = 0x25) [Reset = 0x00]

REG0x25_Flag_1 is shown in 表 6-24.

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表 6-24. REG0x25_Flag_1 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	ADC_DONE_FLAG	R	0x0		ADC conversion INT flag (in one-shot mode only): Note: always reads 0 in continuous mode Access: R (ClearOnRead) 0b = Conversion not complete 1b = Conversion complete
6	IAC_DPM_FLAG	R	0x0		Input Current regulation INT flag: Access: R (ClearOnRead) 0b = Normal 1b = Device entered Input Current regulation
5	VAC_DPM_FLAG	R	0x0		Input Voltage regulation INT flag: Access: R (ClearOnRead) 0b = Normal 1b = Device entered Input Voltage regulation
4	RESERVED	R	0x0		Reserved

表 6-24. REG0x25_Flag_1 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Notes	Description
3	WD_FLAG	R	0x0		I2C Watchdog timer INT flag: Access: R (ClearOnRead) 0b = Normal 1b = WD_STAT rising edge detected
2	RESERVED	R	0x0		Reserved
1	RESERVED	R	0x0		Reserved
0	RESERVED	R	0x0		Reserved

6.5.20 REG0x26_Flag_2 Register (Address = 0x26) [Reset = 0x00]

REG0x26_Flag_2 is shown in 表 6-25.

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表 6-25. REG0x26_Flag_2 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	PG_FLAG	R	0x0		Input Power Good INT flag: Access: R (ClearOnRead) 0b = Normal 1b = PG signal toggle detected
6	RESERVED	R	0x0		Reserved
5	RESERVED	R	0x0		Reserved
4	TS_FLAG	R	0x0		TS INT flag: Access: R (ClearOnRead) 0b = Normal 1b = TS_STAT[2:0] bits changed (transitioned to any state)
3	REVERSE_FLAG	R	0x0		Reverse Mode INT flag: Access: R (ClearOnRead) 0b = Normal 1b = Reverse Mode toggle detected
2	RESERVED	R	0x0		Reserved
1	FSW_SYNC_FLAG	R	0x0		FSW_SYNC pin signal INT flag: Access: R (ClearOnRead) 0b = Normal 1b = FSW_SYNC status changed
0	RESERVED	R	0x0		Reserved

6.5.21 REG0x27_Fault_Flag Register (Address = 0x27) [Reset = 0x00]

REG0x27_Fault_Flag is shown in 表 6-26.

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表 6-26. REG0x27_Fault_Flag Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	VAC_UV_FLAG	R	0x0		Input under-voltage INT flag: Access: R (ClearOnRead) 0b = Normal 1b = Entered input under-voltage fault

表 6-26. REG0x27_Fault_Flag Register Field Descriptions (続き)

Bit	Field	Type	Reset	Notes	Description
6	VAC_OV_FLAG	R	0x0		Input over-voltage INT flag: Access: R (ClearOnRead) 0b = Normal 1b = Entered Input over-voltage fault
5	IBAT_OCP_FLAG	R	0x0		Battery over-current INT flag: Access: R (ClearOnRead) 0b = Normal 1b = Entered Battery over-current fault
4	VBAT_OV_FLAG	R	0x0		Battery over-voltage INT flag: Access: R (ClearOnRead) 0b = Normal 1b = Entered battery over-voltage fault
3	TSHUT_FLAG	R	0x0		Thermal shutdown INT flag: Access: R (ClearOnRead) 0b = Normal 1b = Entered TSHUT fault
2	RESERVED	R	0x0		Reserved
1	DRV_OKZ_FLAG	R	0x0		DRV_SUP pin voltage INT flag: Access: R (ClearOnRead) 0b = Normal 1b = DRV_SUP pin fault detected
0	RESERVED	R	0x0		Reserved

6.5.22 REG0x28_Mask_1 Register (Address = 0x28) [Reset = 0x00]

REG0x28_Mask_1 is shown in 表 6-27.

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表 6-27. REG0x28_Mask_1 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	ADC_DONE_MASK	R/W	0x0	Reset by: REG_RESET	ADC conversion INT mask (in one-shot mode only): 0b = ADC_DONE produces INT pulse 1b = ADC_DONE does not produce INT pulse
6	IAC_DPM_MASK	R/W	0x0	Reset by: REG_RESET	Input Current regulation INT mask: 0b = IAC_DPM_FLAG produces INT pulse 1b = IAC_DPM_FLAG does not produce INT pulse
5	VAC_DPM_MASK	R/W	0x0	Reset by: REG_RESET	Input Voltage regulation INT mask: 0b = VAC_DPM_FLAG produces INT pulse 1b = VAC_DPM_FLAG does not produce INT pulse
4	RESERVED	R	0x0		Reserved
3	WD_MASK	R/W	0x0	Reset by: REG_RESET	I2C Watchdog timer INT mask: 0b = WD expiration produces INT pulse 1b = WD expiration does not produce INT pulse
2	RESERVED	R	0x0		Reserved
1	RESERVED	R	0x0		Reserved
0	RESERVED	R/W	0x0	Reset by: REG_RESET	Reserved

6.5.23 REG0x29_Mask_2 Register (Address = 0x29) [Reset = 0x00]

REG0x29_Mask_2 is shown in 表 6-28.

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表 6-28. REG0x29_Mask_2 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	PG_MASK	R/W	0x0	Reset by: REG_RESET	Input Power Good INT mask: 0b = PG toggle produces INT pulse 1b = PG toggle does not produce INT pulse
6	RESERVED	R	0x0		Reserved
5	RESERVED	R	0x0		Reserved
4	TS_MASK	R/W	0x0	Reset by: REG_RESET	TS INT mask: 0b = TS_STAT change produces INT pulse 1b = TS_STAT change does not produce INT pulse
3	REVERSE_MASK	R/W	0x0	Reset by: REG_RESET	Reverse Mode INT mask: 0b = REVERSE_STAT toggle produces INT pulse 1b = REVERSE_STAT toggle does no produce INT pulse
2	RESERVED	R	0x0		Reserved
1	FSW_SYNC_MASK	R/W	0x0	Reset by: REG_RESET	FSW_SYNC pin signal INT mask: 0b = FSW_SYNC status change produces INT pulse 1b = FSW_SYNC status change does not produce INT pulse
0	RESERVED	R	0x0		Reserved

6.5.24 REG0x2A_Fault_Mask Register (Address = 0x2A) [Reset = 0x00]

REG0x2A_Fault_Mask is shown in 表 6-29.

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表 6-29. REG0x2A_Fault_Mask Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	VAC_UV_MASK	R/W	0x0	Reset by: REG_RESET	Input under-voltage INT mask: 0b = Input under-voltage event produces INT pulse 1b = Input under-voltage event does not produce INT pulse
6	VAC_OV_MASK	R/W	0x0	Reset by: REG_RESET	Input over-voltage INT mask: 0b = Input over-voltage event produces INT pulse 1b = Input over-voltage event does not produce INT pulse
5	IBAT_OCP_MASK	R/W	0x0	Reset by: REG_RESET	Battery over-current INT mask: 0b = Battery over-current event produces INT pulse 1b = Battery over-current event does not produce INT pulse
4	VBAT_OV_MASK	R/W	0x0	Reset by: REG_RESET	Battery over-voltage INT mask: 0b = Battery over-voltage event produces INT pulse 1b = Battery over-voltage event does not produce INT pulse
3	TSHUT_MASK	R/W	0x0	Reset by: REG_RESET	Thermal shutdown INT mask: 0b = TSHUT event produces INT pulse 1b = TSHUT event does not produce INT pulse

表 6-29. REG0x2A_Fault_Mask Register Field Descriptions (続き)

Bit	Field	Type	Reset	Notes	Description
2	RESERVED	R	0x0		Reserved
1	DRV_OKZ_MASK	R/W	0x0	Reset by: REG_RESET	DRV_SUP pin voltage INT mask: 0b = DRV_SUP pin fault produces INT pulse 1b = DRV_SUP pin fault does not produce INT pulse
0	RESERVED	R	0x0		Reserved

6.5.25 REG0x2B_ADC_Control Register (Address = 0x2B) [Reset = 0x60]

REG0x2B_ADC_Control is shown in 表 6-30.

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表 6-30. REG0x2B_ADC_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	ADC_EN	R/W	0x0	When EN_VREG_TEMP_COMP = 1, the ADC will be automatically enabled, regardless of the status of ADC_EN Reset by: REG_RESET WATCHDOG	ADC control: 0b = Disable ADC 1b = Enable ADC
6	ADC_RATE	R/W	0x1	Reset by: REG_RESET	ADC conversion rate control: 0b = Continuous conversion 1b = One-shot conversion
5:4	ADC_SAMPLE	R/W	0x2	Reset by: REG_RESET	ADC sample speed: 00b = 15 bit effective resolution 01b = 14 bit effective resolution 10b = 13 bit effective resolution 11b = Reserved
3	ADC_AVG	R/W	0x0	Reset by: REG_RESET	ADC average control: 0b = Single value 1b = Running average
2	ADC_AVG_INIT	R/W	0x0	Reset by: REG_RESET	ADC average initial value control: 0b = Start average using existing register value 1b = Start average using new ADC conversion
1:0	RESERVED	R	0x0		Reserved

6.5.26 REG0x2C_ADC_Channel_Control Register (Address = 0x2C) [Reset = 0x0A]

REG0x2C_ADC_Channel_Control is shown in 表 6-31.

Return to the Summary Table.

表 6-31. REG0x2C_ADC_Channel_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	IAC_ADC_DIS	R/W	0x0	Reset by: REG_RESET	IAC ADC control 0b = Enable 1b = Disable

表 6-31. REG0x2C_ADC_Channel_Control Register Field Descriptions (続き)

Bit	Field	Type	Reset	Notes	Description
6	IOUT_ADC_DIS	R/W	0x0	Recommend to disable IOUT ADC channel when EN_IBAT_LOAD bit is 1 Reset by: REG_RESET	IOUT ADC control 0b = Enable 1b = Disable
5	VAC_ADC_DIS	R/W	0x0	Reset by: REG_RESET	VAC ADC control 0b = Enable 1b = Disable
4	VOUT_ADC_DIS	R/W	0x0	Reset by: REG_RESET	VOUT ADC control 0b = Enable 1b = Disable
3	RESERVED	R	0x0		Reserved
2	TS_ADC_DIS	R/W	0x0	Reset by: REG_RESET	TS ADC control 0b = Enable 1b = Disable
1	RESERVED	R	0x0		Reserved
0	RESERVED	R	0x0		Reserved

6.5.27 REG0x2D_IAC_ADC Register (Address = 0x2D) [Reset = 0x0000]

REG0x2D_IAC_ADC is shown in 表 6-32.

Return to the Summary Table.

I2C REG0x2E=[15:8], I2C REG0x2D=[7:0]

表 6-32. REG0x2D_IAC_ADC Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:0	IAC_ADC	R	0x0		IAC ADC reading with 5mΩ RAC_SNS: Reported as 2s complement POR: 0mA(0h) Format: 2s Complement Range: -20000mA - 20000mA (9E58h-61A8h) Clamped Low Clamped High Bit Step: 0.8mA

6.5.28 REG0x2F_IOUT_ADC Register (Address = 0x2F) [Reset = 0x0000]

REG0x2F_IOUT_ADC is shown in 表 6-33.

Return to the Summary Table.

I2C REG0x30=[15:8], I2C REG0x2F=[7:0]

表 6-33. REG0x2F_IOUT_ADC Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:0	IOUT_ADC	R	0x0		IOUT ADC reading with 5mΩ RBAT_SNS: Reported as 2s complement POR: 0mA (0h) Format: 2s Complement Range: -20000mA-20000mA (D8F0h-2710h) Clamped Low Clamped High Bit Step: 2mA

6.5.29 REG0x31_VAC_ADC Register (Address = 0x31) [Reset = 0x0000]

REG0x31_VAC_ADC is shown in 表 6-34.

Return to the Summary Table.

I2C REG0x32=[15:8], I2C REG0x31=[7:0]

表 6-34. REG0x31_VAC_ADC Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:0	VAC_ADC	R	0x0		VAC ADC reading: Reported as unsigned integer POR: 0mV (0h) Format: 2s Complement Range: 0mV-65534mV (0h-7FFFh) Clamped Low Bit Step: 2mV

6.5.30 REG0x33_VOUT_ADC Register (Address = 0x33) [Reset = 0x0000]

REG0x33_VOUT_ADC is shown in 表 6-35.

Return to the Summary Table.

I2C REG0x34=[15:8], I2C REG0x33=[7:0]

表 6-35. REG0x33_VOUT_ADC Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:0	VOUT_ADC	R	0x0		VOUT ADC reading: Reported as unsigned integer POR: 0mV (0h) Format: 2s Complement Range: 0mV-65534mV (0h-7FFFh) Clamped Low Bit Step: 2mV

6.5.31 REG0x37_TS_ADC Register (Address = 0x37) [Reset = 0x0000]

REG0x37_TS_ADC is shown in 表 6-36.

Return to the Summary Table.

I2C REG0x38=[15:8], I2C REG0x37=[7:0]

表 6-36. REG0x37_TS_ADC Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:0	TS_ADC	R	0x0		TS ADC reading as percentage of REGN: Reported as unsigned integer POR: 0%(0h) Range: 0% - 99.90234375% (0h-3FFh) Clamped High Bit Step: 0.09765625%

6.5.32 REG0x3B_Gate_Driver_Strength_Control Register (Address = 0x3B) [Reset = 0x00]

REG0x3B_Gate_Driver_Strength_Control is shown in 表 6-37.

Return to the Summary Table.

表 6-37. REG0x3B_Gate_Driver_Strength_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7:6	BOOST_HS_DRV	R/W	0x0	Reset by: REG_RESET	Boost High Side FET Gate Driver Strength: 00b = Fastest 01b = Faster 10b = Slower 11b = Slowest
5:4	BUCK_HS_DRV	R/W	0x0	Reset by: REG_RESET	Buck High Side FET Gate Driver Strength: 00b = Fastest 01b = Faster 10b = Slower 11b = Slowest
3:2	BOOST_LS_DRV	R/W	0x0	Reset by: REG_RESET	Boost Low Side FET Gate Driver Strength: 00b = Fastest 01b = Faster 10b = Slower 11b = Slowest
1:0	BUCK_LS_DRV	R/W	0x0	Reset by: REG_RESET	Buck Low Side FET Gate Driver Strength: 00b = Fastest 01b = Faster 10b = Slower 11b = Slowest

6.5.33 REG0x3C_Gate_Driver_Dead_Time_Control Register (Address = 0x3C) [Reset = 0x00]

REG0x3C_Gate_Driver_Dead_Time_Control is shown in 表 6-38.

Return to the Summary Table.

表 6-38. REG0x3C_Gate_Driver_Dead_Time_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7:4	RESERVED	R	0x0		Reserved
3:2	BOOST_DEAD_TIME	R/W	0x0	Reset by: REG_RESET	Boost Side FETs Dead Time Control: 00b = 45ns 01b = 75ns 10b = 105ns 11b = 135ns

表 6-38. REG0x3C_Gate_Driver_Dead_Time_Control Register Field Descriptions (続き)

Bit	Field	Type	Reset	Notes	Description
1:0	BUCK_DEAD_TIME	R/W	0x0	Reset by: REG_RESET	Buck Side FETs Dead Time Control: 00b = 45ns 01b = 75ns 10b = 105ns 11b = 135ns

6.5.34 REG0x3D_Part_Information Register (Address = 0x3D) [Reset = 0x22]

REG0x3D_Part_Information is shown in 表 6-39.

Return to the Summary Table.

表 6-39. REG0x3D_Part_Information Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	RESERVED	R	0x0		Reserved
6:3	PART_NUM	R	0x4		Part Number: 100 - BQ25758
2:0	DEV_REV	R	0x2		Device Revision:

6.5.35 REG0x62_Reverse_Mode_Current Register (Address = 0x62) [Reset = 0x02]

REG0x62_Reverse_Mode_Current is shown in 表 6-40.

Return to the Summary Table.

表 6-40. REG0x62_Reverse_Mode_Current Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7:6	IBAT_REV	R/W	0x0	Reset by: REG_RESET	Reverse mode current limit: 00b = 20A 01b = 15A 10b = 10A 11b = 5A
5:2	RESERVED	R	0x0		Reserved
1	EN_CONV_FAST_TRANSIENT	R/W	0x1	Reset by: REG_RESET	Enable converter fast transient response - 0b = Disable 1b = Enable
0	RESERVED	R	0x0		Reserved

7 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

7.1 Application Information

The BQ25758 controller is ideal for high current applications (up-to 20 A). The BQ25758EVM evaluation module is a complete module for evaluating the device performance. The application curves were taken using the BQ25758EVM.

7.2 Typical Applications

7.2.1 Typical Application (Buck-Boost configuration)

The device is configured as a buck-boost with input range from 4.2 V to 60 V. An optional gate drive voltage can be provided using the DRV_SUP pin to reduce switching losses. 図 7-1 shows a typical schematic when using the device with 19.5-V or 48-V input, configurable output voltage for USB-PD EPR and 5-A output current.

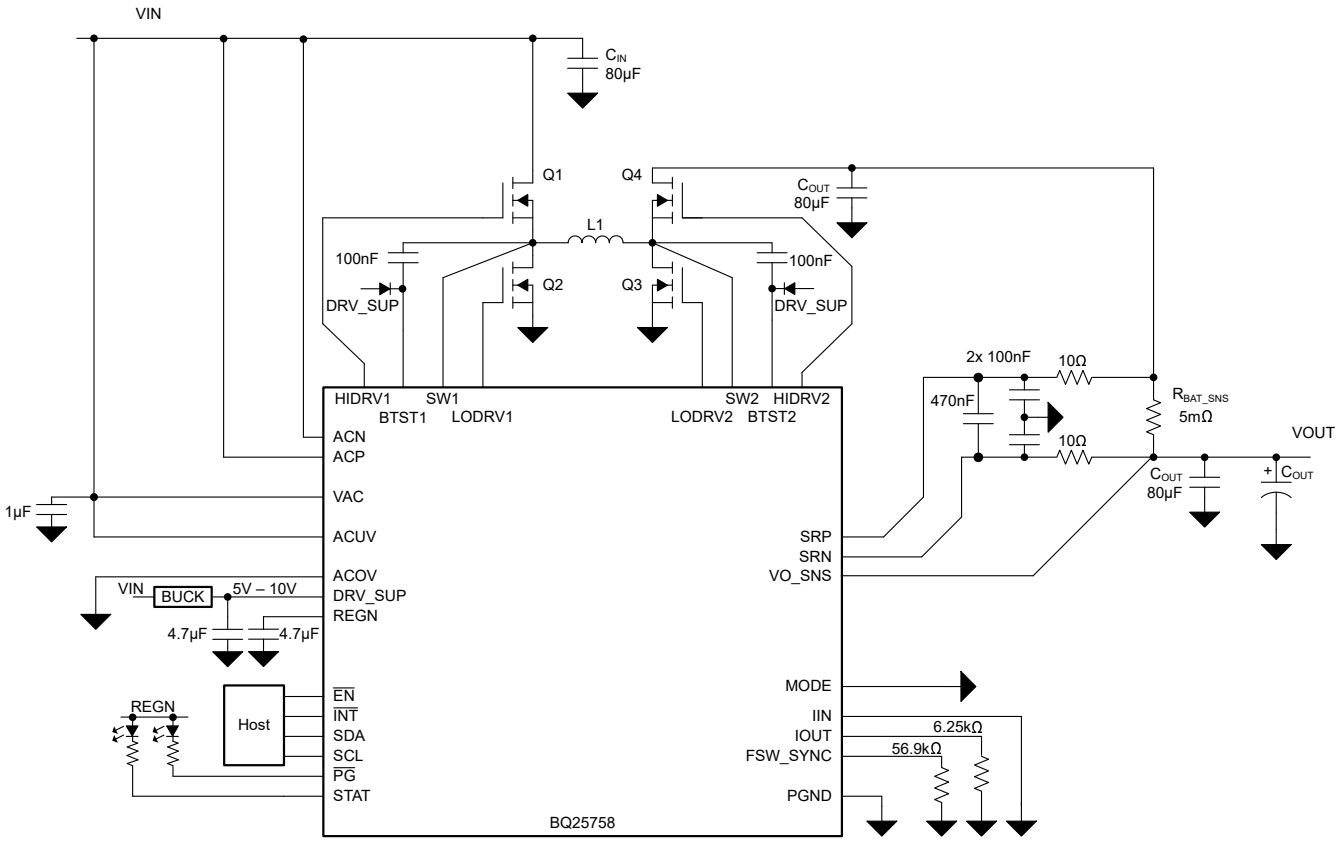


図 7-1. BQ25758: 19.5-V or 48-Vin, Buck-Boost with Configurable Output Voltage for USB-PD EPR, and 5-A Output Current

表 7-1. Recommended Part Numbers for up-to 48-V EPR (5-A output):

COMPONENT	VALUE	RECOMMENDED PART NO.
Q1, Q2, Q3, Q4	80 V, 6.2 mΩ	SiR880BDP

表 7-1. Recommended Part Numbers for up-to 48-V EPR (5-A output): (続き)

COMPONENT	VALUE	RECOMMENDED PART NO.
L1	10 µH, 22 mΩ	CMLB135T-100MS

表 7-2. Recommended Part Numbers for 28-V EPR only (5-A output):

COMPONENT	VALUE	RECOMMENDED PART NO.
Q1, Q2, Q3, Q4	40 V, 3.5 mΩ	AONS66408
L1	4.7 µH, 22 mΩ	CMLE104T-4R7MS

7.2.1.1 Design Requirements

For this design example, use the parameters shown in the table below.

表 7-3. Design Parameters

PARAMETER	VALUE
Input voltage operating range (V_{AC})	4.2 V to 60 V
Input current limit (I_{AC})	No limit
Output current limit (I_{OUT})	5 A
Output voltage (V_{OUT_REG})	5 V, 9 V, 15 V, 20 V, 28 V, 36 V, 48 V
Switching frequency	450 kHz

7.2.1.2 Detailed Design Procedure

7.2.1.2.1 ACUV / ACOV Input Voltage Operating Window Programming

The input voltage operating window is programmed by an ACUV / ACOV window with a resistor divider from VAC to GND. The top resistor, RAC1 is typically selected as 1,000 kΩ to minimize the input voltage leakage current. Assuming the desired trip-points for under-voltage and over-voltage protection are labeled V_{VACUVP} and V_{VACOVP}, the resistor divider required can be calculated as follows. The internal reference for the over-voltage threshold (VREF_ACOV) is 1.2 V. The internal reference for the under-voltage threshold (VREF_ACUV) is 1.1 V.

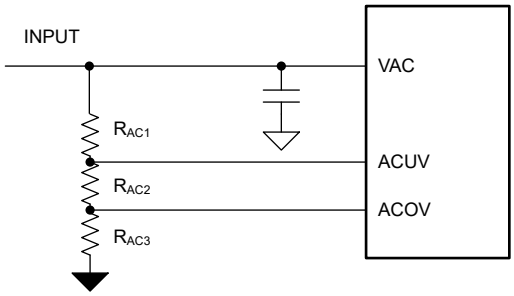


図 7-2. ACUV and ACOV Resistor Divider

$$V_{VACOVP} = \frac{1.2V(1{,}000k\Omega + R_{AC2} + R_{AC3})}{R_{AC3}} \quad (6)$$

$$V_{VACUVP} = \frac{1.1V(1{,}000k\Omega + R_{AC2} + R_{AC3})}{R_{AC2} + R_{AC3}} \quad (7)$$

For the default device operating window of 4.2 V to 60 V, the ACUV can be pulled up directly to VAC, while the ACOV can be pulled directly to GND.

7.2.1.2.2 Switching Frequency Selection

The switching frequency is set by a resistor connected from the FSW_SYNC pin to PGND. The RFSW resistor required to set the desired frequency is calculated using 式 3 or 表 6-3. A 0.1% standard resistor of 56.9 kΩ is selected to set f_{SW} = 450 kHz.

7.2.1.2.3 Inductor Selection

Higher switching frequency allows the use of smaller inductor and capacitor values. Inductor saturation current should be higher than the inductor current (I_L) plus half the ripple current (I_{RIPPLE}):

$$I_{SAT} \geq I_L + \frac{1}{2} I_{RIPPLE} \tag{8}$$

The inductor ripple current in buck operation depends on input voltage (V_{AC}), duty cycle ($D_{BUCK} = V_{BAT}/V_{AC}$), switching frequency ($f_{SW}$) and inductance (L):

$$I_{RIPPLE\_BUCK} = \frac{V_{AC} \times D_{BUCK} \times (1 - D_{BUCK})}{f_{SW} \times L} \tag{9}$$

During boost operation, the duty cycle is: $D_{BOOST} = 1 – (V_{AC}/V_{BAT})$. The inductor ripple current is:

$$I_{RIPPLE\_BOOST} = \frac{V_{AC} \times D_{BOOST}}{f_{SW} \times L} \tag{10}$$

The maximum inductor ripple current happens with D = 0.5 or close to 0.5. Ripple calculations should be analyzed for both forward and reverse operating modes if applicable.

Usually inductor ripple is designed in the range of (20 – 40%) maximum inductor current (in either forward or reverse mode) as a trade-off between inductor size and efficiency for a practical design.

7.2.1.2.4 Input (VAC) Capacitor

Input capacitor should have enough ripple current rating to absorb input switching ripple current. The worst case RMS ripple current is half of the output when duty cycle is 0.5 in forward buck mode, or reverse boost mode. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current occurs where the duty cycle is closest to 50% and can be estimated by 式 11:

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1 - D)} \tag{11}$$

A combination of ceramic and bulk capacitors should be used to provide a short path for high di/dt current and to reduce the voltage ripple. Ceramic capacitors should be placed close to the switching half-bridge. Given total bulk input capacitance, it is recommended to distribute equally on either side of R_{AC_SNS}. The complete schematic is a good starting point for input capacitor for typical applications.

7.2.1.2.5 Output (VBAT) Capacitor

In forward boost mode or reverse buck mode, the output capacitor conducts high ripple current. The output capacitor RMS ripple current is given by where the minimum VAC corresponds to the maximum capacitor current.

$$I_{CBAT} = I_{BAT} \sqrt{\frac{V_{BAT}}{V_{AC}} - 1} \tag{12}$$

A 5-mΩ output capacitor ESR causes an output voltage ripple of 74 mV as given by:

$$\Delta V_{RIPPLE(ESR)} = I_{BAT} \times \frac{V_{BAT}}{V_{AC,min}} \times ESR \tag{13}$$

A 140-µF output capacitor causes a capacitive ripple voltage of 66 mV as given by:

$$\Delta V_{RIPPLE(CBAT)} = I_{BAT} \times \frac{\left(1 - \frac{V_{AC,min}}{V_{BAT}}\right)}{C_{BAT} \times f_{SW}} \quad (14)$$

A combination of ceramic and bulk capacitors should be used to provide low ESR and high ripple current capacity. Ceramic capacitors should be placed close to the switching half-bridge. Given total bulk output capacitance, it is recommended to distribute equally on either side of R_{BAT_SNS}. The complete schematic is a good starting point for C_{BAT} for typical applications.

7.2.1.2.6 Sense Resistor (R_{AC_SNS} and R_{BAT_SNS}) and Current Programming

The battery current sense resistor between SRP and SRN is fixed at 5 mΩ; using a different value is not recommended. The input current sense resistor between ACP and ACN is typically 2 mΩ, but can be increased to achieve better accuracy at lower sensed currents. In USB-PD EPR applications, a 5-mΩ sense resistor is recommended to achieve programmability in 50 mA/step. In addition, if input current limit function is not desired, ACP and ACN may be shorted together. For both of these sense resistors, a filter network is recommended as shown in the Typical Application.

For both the input current and the output current, the limits may be programmed using the I^2C interface or an external programming resistor on IIN and IOUT pins, respectively.

表 7-4. Sense Resistor and Current Programming

PARAMETER	FORMULA	VALUE
Input Current Hardware Limit	Unused	Pull IIN pin to GND
Input Current Software Limit	Unused	REG06 = 0x0640 (50 A with 2-mΩ R_{AC_SNS})
Output Current Hardware Limit	$R_{IOUT} = K_{ICHG}$ / 8 A	6.25 kΩ for 8 A with 5-mΩ R_{BAT_SNS}
Output Current Software Limit	ICHG = 5 A	REG02 = 0x0190 (5 A)

The default input sense resistor (R_{AC_SNS}) is 2 mΩ, and the register allows for a range of up-to 50-A input current limit. If lower currents are desired, it is possible to use a higher resistor, such as 5 mΩ. In this case, the IAC_DPM register value should be multiplied by a factor of 2/5 to program the correct current. For example, if a 5-mΩ R_{AC_SNS} is used, and the register is programmed to a value of 0x60, the true maximum current across the R_{AC_SNS} will be: 12A * 2/5 = 4.8 A. Similarly, the K_{ILIM} parameter used to set the IIN pull-down resistor should be scaled by 2/5. For example, with a 5-mΩ R_{AC_SNS} resistor, a 6-A current limit would be achieved as: $R_{ILIM} = K_{ILIM} * (2/5) / 6A = 3.3$ kΩ.

7.2.1.2.7 Converter Fast Transient Response

The device integrates all the loop compensation, thereby providing a high density solution with ease of use. For faster transient reponse, the EN_CONV_FAST_TRANSIENT bit can be set to 1. If device is not used in boost mode operation, this section can be disregarded.

When the converter is operating in boost mode, the non-continuous inductor current flow to the load results in a right-half plane (RHP) zero. The RHP zero location is:

$$RHPz = \frac{V_{IN,boost}}{I_{IN,boost}} \frac{1}{2\pi L} \quad (15)$$

For good phase margin, the unity gain bandwidth (UGBW) of the converter should be about 1/3 of the RHPz. The boost output capacitor (C_{load}), and the converter transient parameters (R_1, gm_1) need to be scaled to move the location of the UGBW of the converter.

$$1 \approx \frac{Adiv \times gm_1(sR_1C_1 + 1)}{sC_1}\left[\frac{V_i}{I_o \times 50m}\right]\left[\frac{1}{1 + s\frac{C_{load}R_{load}}{2}}\right] \quad (16)$$

The device adjusts *Adiv*, gm_1 and R_1 based on the output voltage and the EN_CONV_FAST_TRANSIENT bit setting per the table below. During some boost case scenarios, the C_{load} needs to be adjusted to limit the converter bandwidth.

表 7-5. Converter Fast Transient Response

BOOST OUTPUT VOLTAGE	*Adiv*	C_1	EN_CONV_FAST_TRANSIENT = 0		EN_CONV_FAST_TRANSIENT = 1	
			gm_1	R_1	gm_1	R_1
≤8 V	1/5	75 pF	0.4 µ	600 kΩ	2 µ	1.3 MΩ
8 V to 16 V	1/10	75 pF	0.47 µ	1 MΩ	2 µ	1.8 MΩ
16 V to 32 V	1/20	75 pF	0.67 µ	2.8 MΩ	2 µ	2.8 MΩ
>32 V	1/40	75 pF	2 µ	2.8 MΩ	2 µ	2.8 MΩ

As an example, assume the device operates in boost mode from a 5V supply to provide a 7V boost output voltage with load up-to 5A and 10µH inductor. The RHPz is approximately located at:

$$RHPz = \frac{V_{IN,boost}}{I_{IN,boost}} \frac{1}{2\pi L} = 11.4kHz \tag{17}$$

For best stability, the UGBW of the converter should be limited to 1/3 of the RHP zero, or 3.8kHz. If EN_CONV_FAST_TRANSIENT = 1, the equation becomes:

$$1 \approx \frac{0.2 \times 2\mu\,(j\omega \times 1.3M\Omega \times 75pF + 1)}{j\omega \times 75pF} \left[\frac{5V}{5A \times 50m}\right] \left[\frac{1}{1 + j\omega \frac{C_{load} \times 1.4}{2}}\right] \tag{18}$$

Solving the above for C_{load} gives ≥674 µF capacitor requirement.

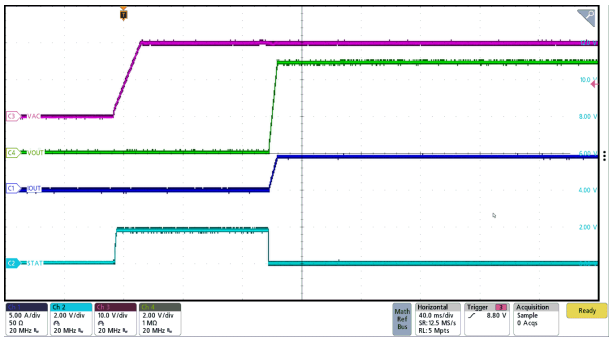
Conversely, if EN_CONV_FAST_TRANSIENT = 0, the UGBW equation becomes:

$$1 \approx \frac{0.2 \times 0.4\mu\,(j\omega \times 0.6M\Omega \times 75pF + 1)}{j\omega \times 75pF} \left[\frac{5V}{5A \times 50m}\right] \left[\frac{1}{1 + j\omega \frac{C_{load} \times 1.4}{2}}\right] \tag{19}$$

Solving the above for C_{load} gives ≥51 µF capacitor requirement. However, the minimum recommended capacitor for converter stability is 80 µF, so this minimum value should be used.

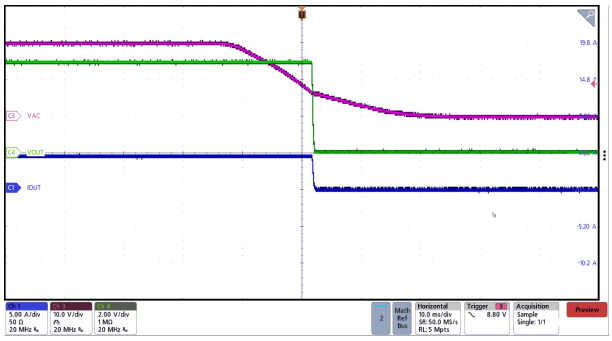
7.2.1.3 Application Curves

C_{VAC} = 160 µF, C_{OUT} = 160 µF, V_{VAC} = 20 V, V_{OUT} = 5 V (unless otherwise specified)



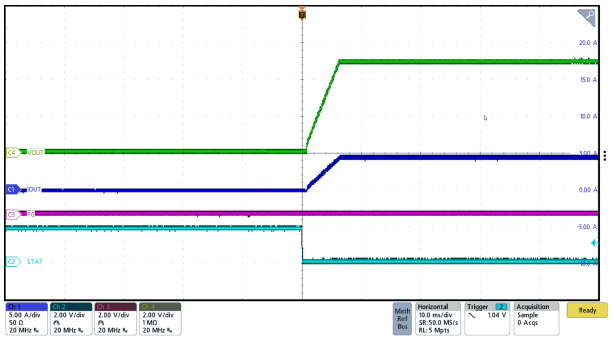
VAC = 20 V

図 7-3. VAC Plug-In Power Up with 5-A Load



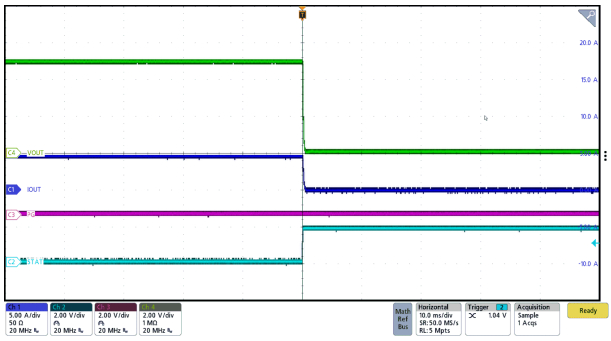
VAC = 20 V → 0 V

図 7-4. VAC Unplug Power Down with 5-A Load



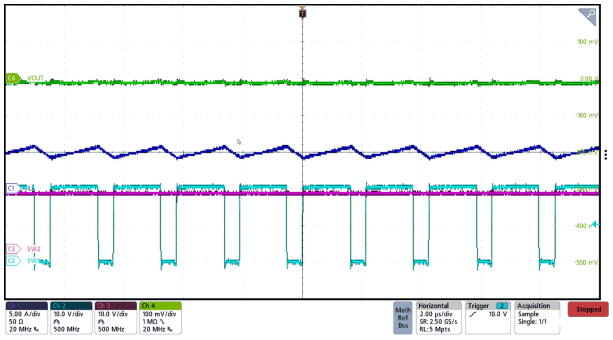
VAC = 20 V

図 7-5. Power Up via I²C with 5-A Load



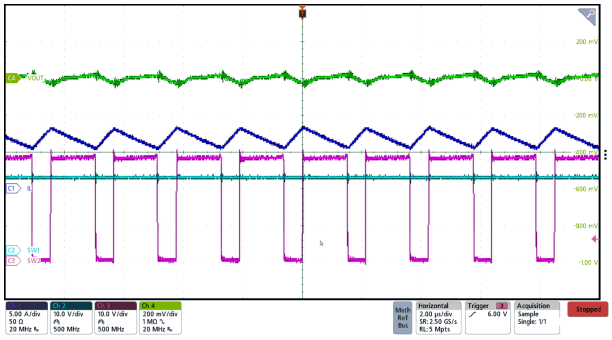
VAC = 20 V

図 7-6. Power Down via I²C with 5-A Load



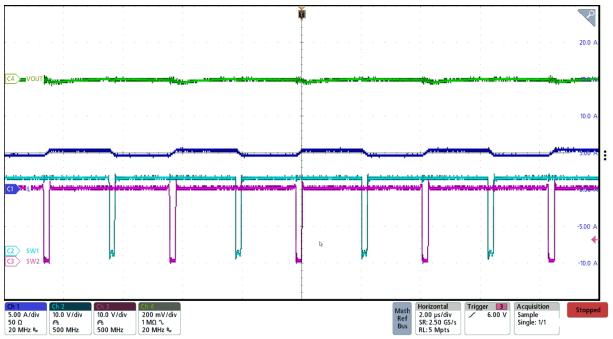
VAC = 20 V VOUT = 15 V IOUT = 5 A

図 7-7. Buck Switching Waveform



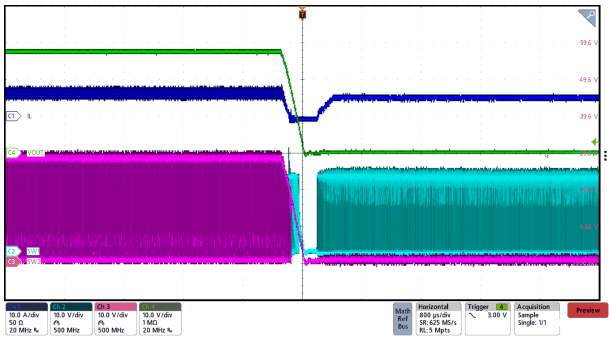
VAC = 20 V VOUT = 28 V IOUT = 5 A

図 7-8. Boost Switching Waveform



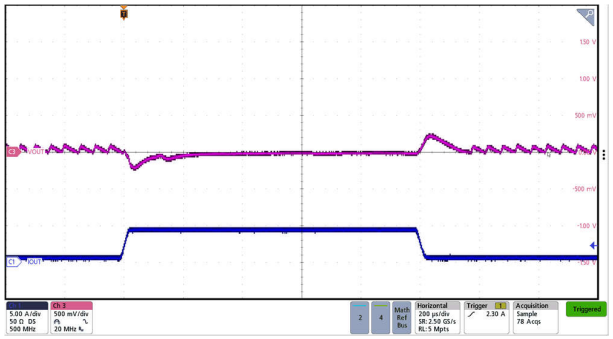
VAC = 20 V VOUT = 20 V IOUT = 5 A

図 7-9. Buck-Boost Switching Waveform



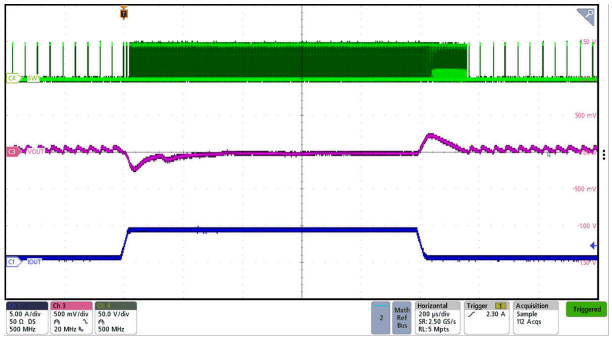
VAC = 20 V

図 7-10. Output Short Circuit Response



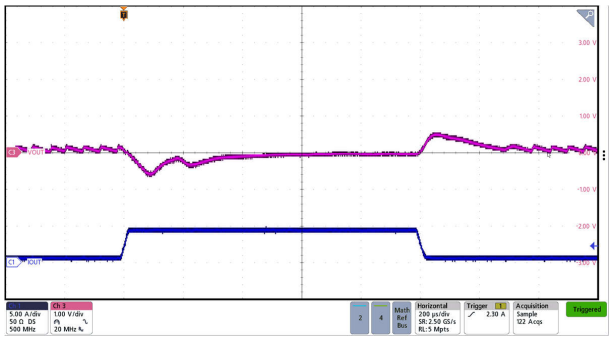
VAC = 20 V VOUT = 5 V ILOAD = 0.5 A → 4.5 A

図 7-11. Forward Mode 5-V Transient Reponse with 20 Vin



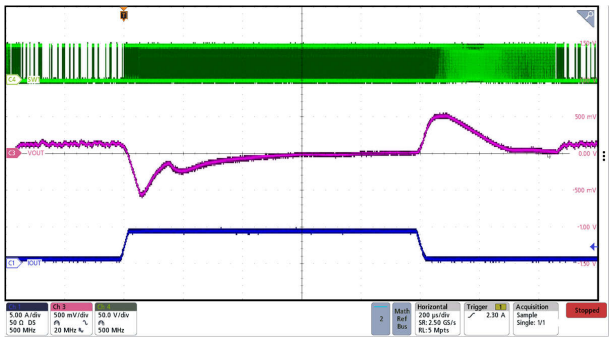
VAC = 48 V VOUT = 5 V ILOAD = 0.5 A → 4.5 A

図 7-12. Forward Mode 5-V Transient Reponse with 48 Vin



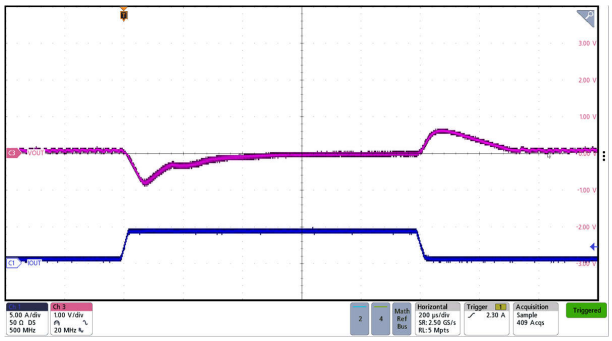
VAC = 20 V VOUT = 20 V ILOAD = 0.5 A → 4.5 A

図 7-13. Forward Mode 20-V Transient Reponse with 20 Vin



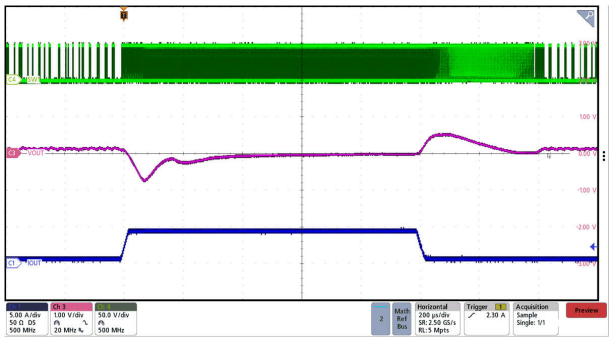
VAC = 48 V VOUT = 20 V ILOAD = 0.5 A → 4.5 A

図 7-14. Forward Mode 20-V Transient Reponse with 48 Vin



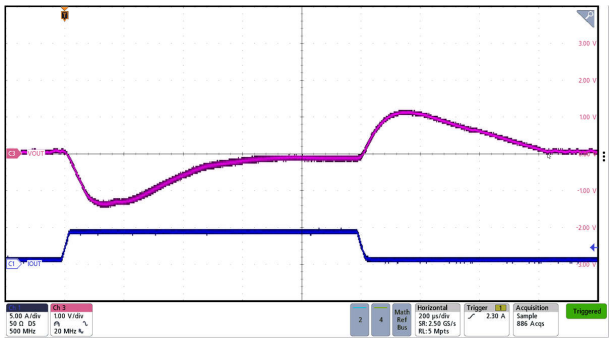
VAC = 20 V VOUT = 28 V ILOAD = 0.5 A → 4.5 A

図 7-15. Forward Mode 28-V Transient Reponse with 20 Vin



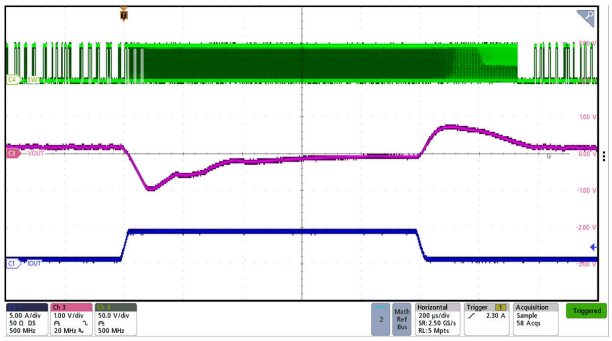
VAC = 48 V VOUT = 28 V ILOAD = 0.5 A → 4.5 A

図 7-16. Forward Mode 28-V Transient Reponse with 48 Vin



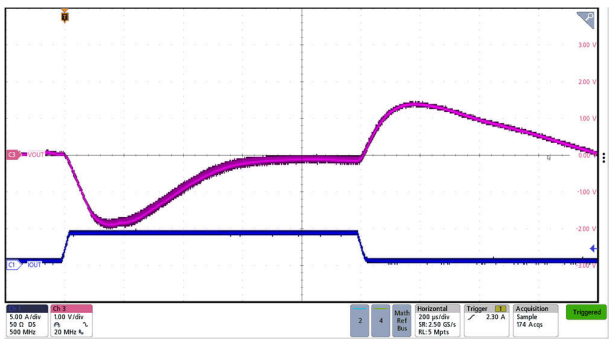
VAC = 20 V VOUT = 36 V ILOAD = 0.5 A → 4.5 A

図 7-17. Forward Mode 36-V Transient Reponse with 20 Vin



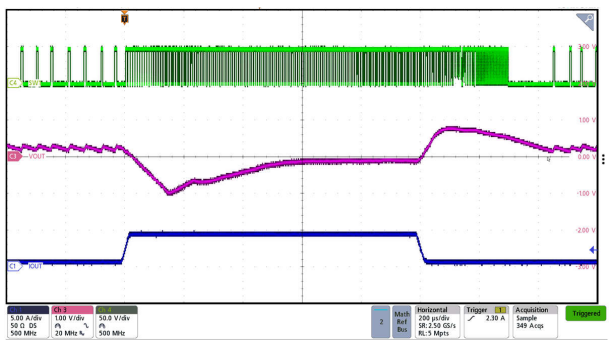
VAC = 48 V VOUT = 36 V ILOAD = 0.5 A → 4.5 A

図 7-18. Forward Mode 36-V Transient Reponse with 48 Vin



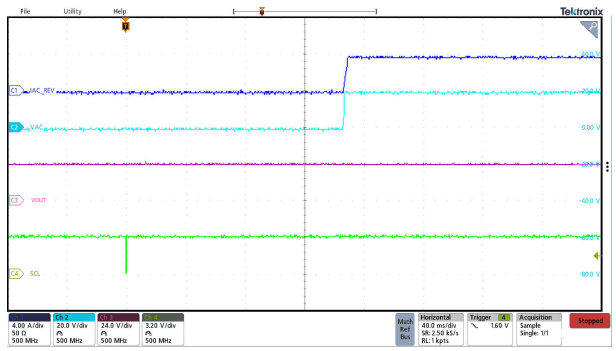
VAC = 20 V VOUT = 48 V ILOAD = 0.5 A → 4.5 A

図 7-19. Forward Mode 48-V Transient Reponse with 20 Vin



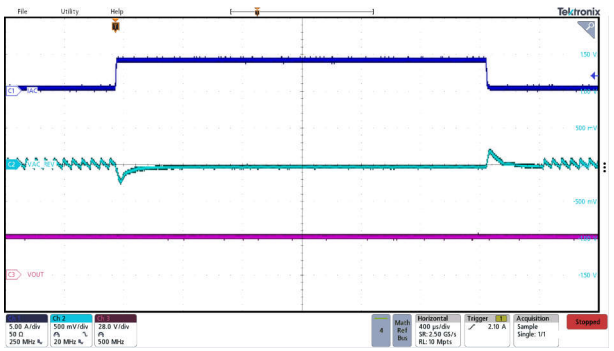
VAC = 48 V VOUT = 48 V ILOAD = 0.5 A → 4.5 A

図 7-20. Forward Mode 48-V Transient Reponse with 48 Vin



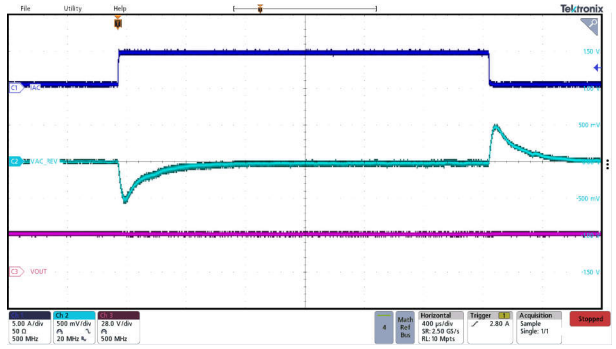
VOUT = 24 V VAC_REV = 20 V ILOAD = 4 A

図 7-21. Reverse Mode Power Up with 4-A Load



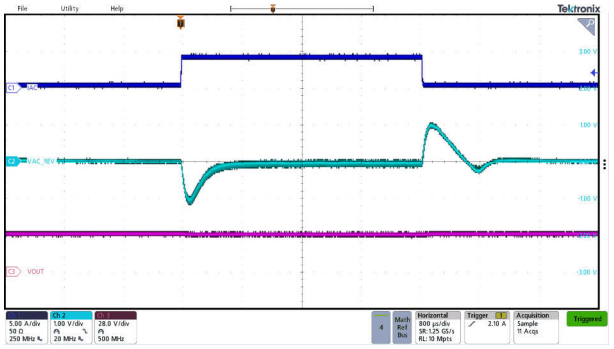
VOUT = 28 V VAC_REV = 5 V ILOAD = 0.5 A → 4.5 A

図 7-22. Reverse Mode Buck Transient Reponse



VOUT = 28 V VAC_REV = 28 V ILOAD = 0.5 A → 4.5 A

図 7-23. Reverse Mode Buck-Boost Transient Reponse



VOUT = 28 V VAC_REV = 48 V ILOAD = 0.5 A → 4.5 A

図 7-24. Reverse Mode Boost Transient Reponse

7.2.2 Typical Application (Buck-only configuration)

The device can be configured as buck-only using the MODE pin as described in MODE Pin Configuration section. In this mode, the Q3 and Q4 FETs must be removed from the system. Please see the diagram below showing buck-only mode without the boost FETs Q3 and Q4. An optional gate drive voltage can be provided using the DRV_SUP pin to reduce switching losses. 図 7-25 shows a typical schematic when using the device as a buck with 48-V input, configurable output voltage for USB-PD EPR and 5-A output current.

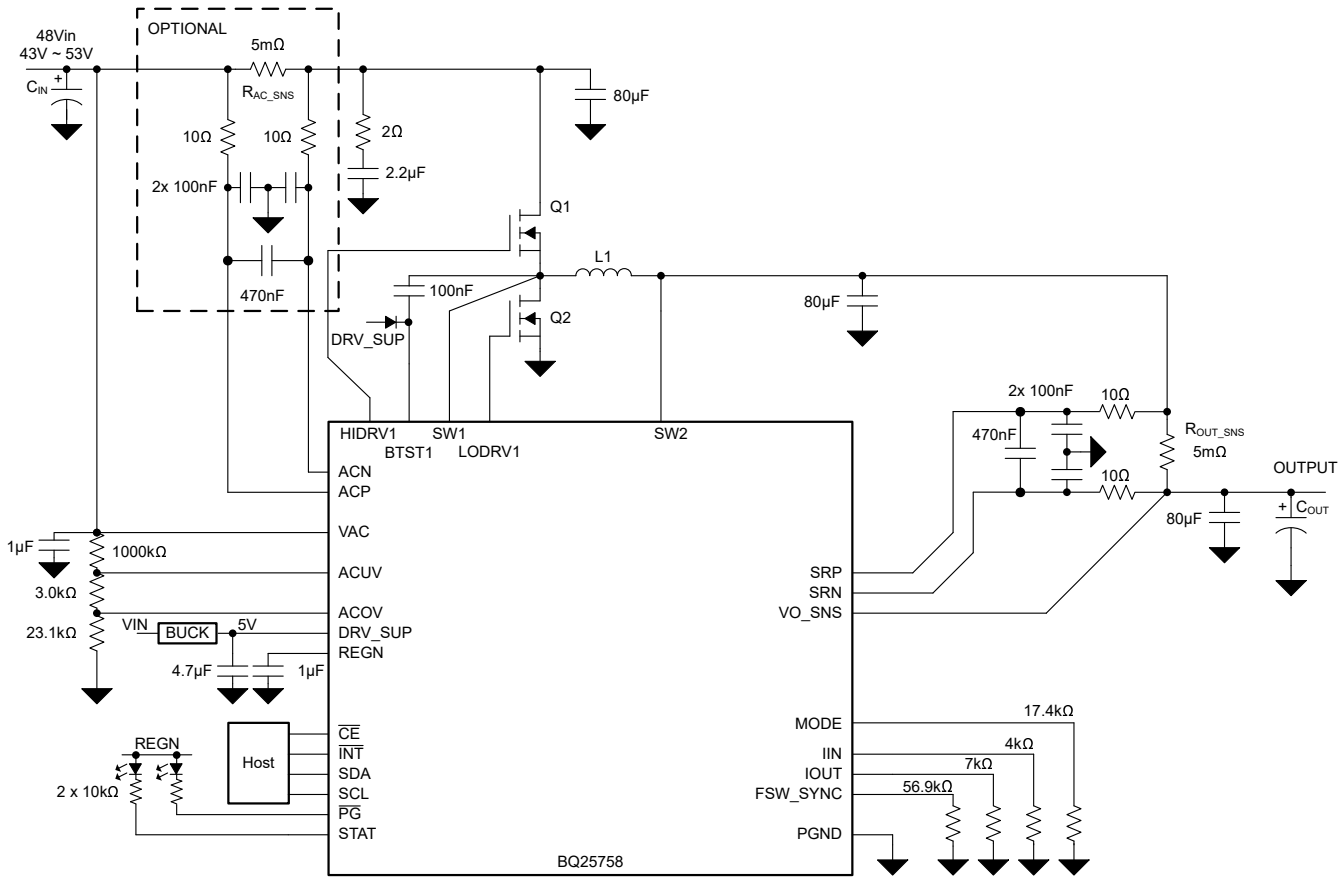


図 7-25. BQ25758: 48-Vin, Buck-Only with Configurable Output Voltage for USB-PD EPR, and 5-A Output Current

表 7-6. Recommended Part Numbers:

COMPONENT	VALUE	RECOMMENDED PART NO.
Q1, Q2	80 V, 6.2 mΩ	SiR880BDP
L1	10 μH, 22 mΩ	CMLB135T-100MS

7.2.2.1 Design Requirements

For this design example, use the parameters shown in the table below.

表 7-7. Design Parameters

PARAMETER	VALUE
Input voltage operating range (V_{AC})	43 V to 53 V
Input current limit (I_{AC})	No limit
Output current limit (I_{OUT})	5 A
Output voltage (V_{OUT_REG})	5 V, 9 V, 15 V, 20 V, 28 V, 36 V
Switching frequency	450 kHz

8 Power Supply Recommendations

The power supply for the device is any DC voltage source within the specified input range. The supply should also be capable of supplying sufficient current based on the programmed input current limit. The input supply should be bypassed with a combination of electrolytic and ceramic capacitors to avoid ringing due to the parasitic impedance of the connecting cables.

When device is operating in the reverse direction, the supply at the OUTPUT should follow the same recommendations as the input supply mentioned above.

9 Layout

9.1 Layout Guidelines

Proper layout of the components to minimize high frequency current path loops is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Here is a PCB layout priority list for proper layout.

表 9-1. PCB Layout Guidelines

COMPONENTS	FUNCTION	IMPACT	GUIDELINES
Buck high side FET, Buck low side FET, input capacitors	Buck input loop	High frequency noise, ripple, efficiency	This path forms a high frequency switching loop due to the pulsating current at the input of the buck. Place components on the same side of the board. Minimize loop area to reduce parasitic inductance. Maximize trace width to reduce parasitic resistance. Place input ceramic capacitors close to the switching FETs.
Boost low side FET, boost high side FET, output capacitors	Boost output loop	High frequency noise, ripple, efficiency	This path forms a high frequency switching loop due to the pulsating current at the output of the boost. Place components on the same side of the board. Minimize loop area to reduce parasitic inductance. Maximize trace width to reduce parasitic resistance. Place output ceramic capacitors close to the switching FETs.
Sense resistors, switching FETs, inductor	Current path	Efficiency	The current path from input to output through the power stage and sense resistors has low impedance. Pay attention to via resistance if they are not on the same side. The number of vias can be estimated as 1-to 2-A per via for a 10-mil via with 1 oz. copper thickness.
Switching FETs, inductor	Power stage	Thermal, efficiency	The switching FETs and inductor are the components with highest power loss. Allow enough copper area for heat dissipation. Multiple thermal vias can be used to connect more copper layers together and dissipate more heat.
DRV_SUP, BTST1, BTST2 capacitors	Switching FET gate drive	High frequency noise, parasitic ringing, gate drive integrity	The DRV_SUP capacitor is used to supply the power to drive the low side FETs. The BTST capacitors are used to drive the high side FETs. It is recommended to place the capacitors as close as possible to the IC.
LODRV1, LODRV2	Low side gate drive	High frequency noise, parasitic ringing, gate drive integrity	LODRV1 and LODRV2 supplies the gate drive current to turn on the low side FETs. The return of LODRV1 and LODRV2 is PGND. As current take the path of least impedance, a ground plane close to the low side gate drive traces is recommended. Minimize gate drive length and aim for at least 20-mil gate drive trace width.
HIDRV1, HIDRV2, SW1 (pin trace), SW2 (pin trace)	High side gate drive	High frequency noise, parasitic ringing, gate drive integrity	HIDRV1 and HIDRV2 supplies the gate drive current to turn on the high side FETs. The return of HIDRV1 and HIDRV2 are SW1 and SW2, respectively. Route HIDRV1/SW1 and HIDRV2/SW2 pair next to each other to reduce gate drive parasitic inductance. Minimize gate drive length and aim for at least 20-mil gate drive trace width.

表 9-1. PCB Layout Guidelines (続き)

COMPONENTS	FUNCTION	IMPACT	GUIDELINES
Current limit resistors, FSW_SYNC resistor	IC programmable settings	Regulation accuracy, switching integrity	Pin voltage determines the settings for input current limit, output current limit and switching frequency. Ground noise on these could lead to inacuracy. Minimize ground return from these resistors to the IC ground pin.
Input (ACP, ACN) and output (SRP, SRN) current sense	Current regulation	Regulation accuracy	Use Kelvin-sensing technique for input and output current sense resistors. Connect the current sense traces to the center of the pads, and run current sense traces as differential pairs, away from switching nodes.
Input (ACUV), and output (FB, VO_SNS) voltage sensing	Voltage sense and regulation	Regulation accuracy	ACUV divider sets internal input voltage regulation in forward mode (V_{ACUV_DPM}). Route the top of the divider point to the target regulation location. VO_SNS sets the output voltage regulation in forward mode ($V_{OUT\_REG\_ACC}$). Route directly to the target regulation location. Avoid routing close to high power switching nodes.
Bypass capacitors	Noise filter	Noise immunity	Place lowest value capacitors closest to the IC.

9.2 Layout Example

Based on the above layout guidelines, the buck-boost PCB layout example top view is shown below including all the key power components.

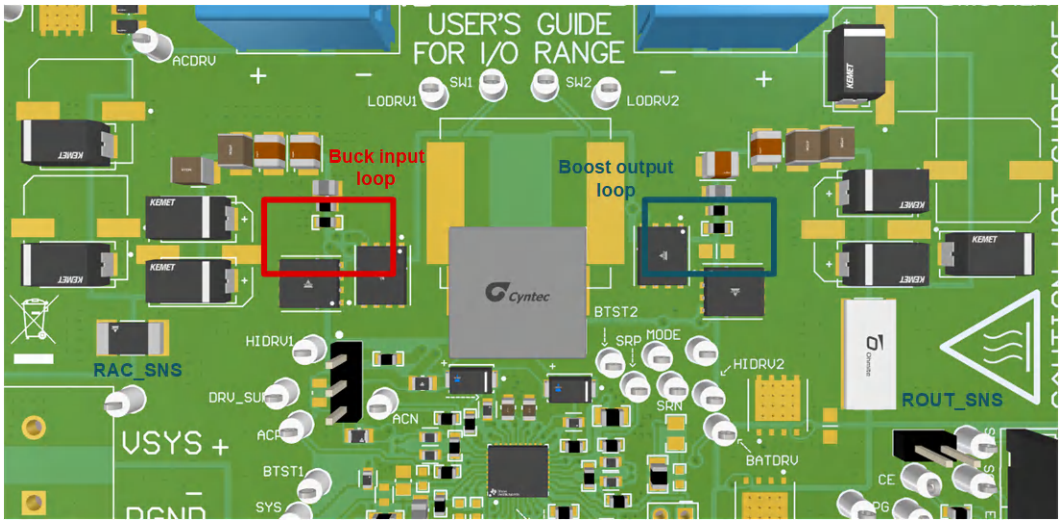


図 9-1. PCB Layout Reference Example Top View

For both input and output current sensing resistors, differential sensing and routing method are suggested and highlighted in figure below. Use wide trace for gate drive traces, minimum 20-mil trace width. Connect all analog grounds to a dedicated low-impedance copper plane, which is tied to the power ground underneath the IC exposed pad.

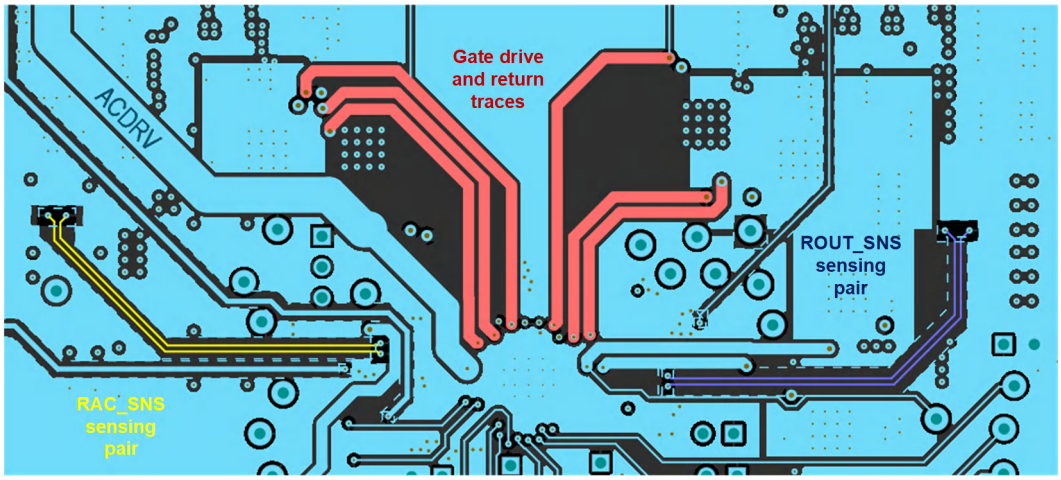


図 9-2. PCB Layout Gate Drive and Current Sensing Signal Layer Routing

10 Device and Documentation Support

10.1 Device Support

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10.6 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (July 2023) to Revision B (March 2024)	Page
• 「非公開」から「公開」リリースに変更	1

Changes from Revision * (December 2022) to Revision A (July 2023)	Page
• データシート全体にわたって双方向 / 逆方向モードを追加	1
• データシート全体にわたって降圧専用モードを追加	1
• Updated CIN/COUT requirement	6
• Improve 5V regulation accuracy	8
• Added KIOUT factor	8
• Updated VACUV_DPM limits	8
• Added Reverse Mode Regulation parameters to EC table	8
• Added IBYPASS_OCP	8
• Updated VREGN limts	8
• Increased IAC_LOAD and IBAT_LOAD values	8
• Updated t_{OVLD} typical value	12
• Added セクション 6.3.5	22
• Added セクション 6.3.8.1.3	26
• Added セクション 6.3.8.1.4	26
• Added Reverse mode registers to セクション 6.5	30

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ25758RRVR	Active	Production	VQFN (RRV) | 36	3000 | LARGE T&R	Yes	POST PLATE AG RING	Level-1-260C-UNLIM	-40 to 85	BQ25758
BQ25758RRVR.A	Active	Production	VQFN (RRV) | 36	3000 | LARGE T&R	Yes	POST PLATE AG RING	Level-1-260C-UNLIM	-40 to 85	BQ25758

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

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(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

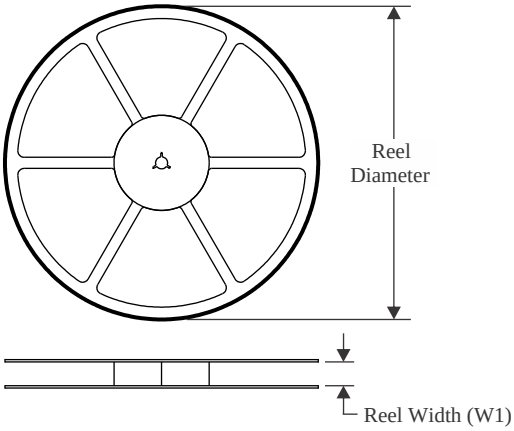
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

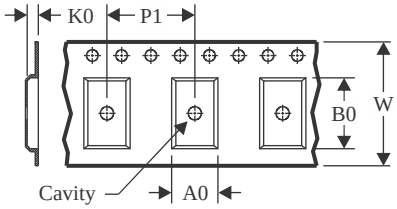
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

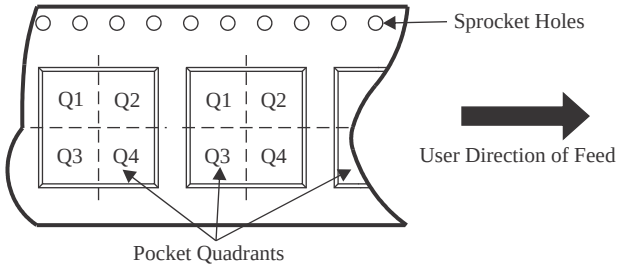


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

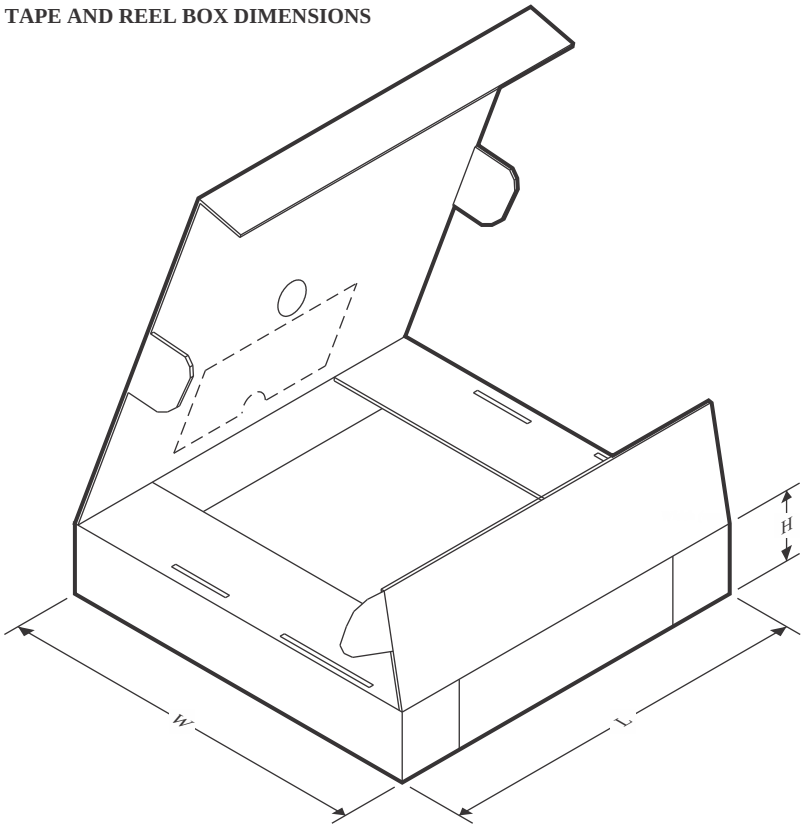
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ25758RRVR	VQFN	RRV	36	3000	330.0	12.4	5.3	6.3	1.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ25758RRVR	VQFN	RRV	36	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

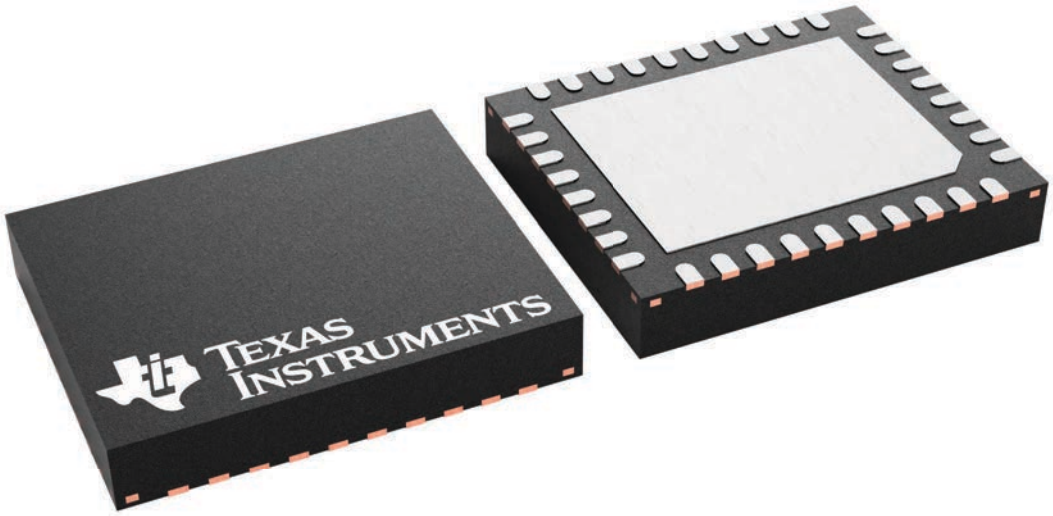
RRV 36

VQFN - 1 mm max height

5 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



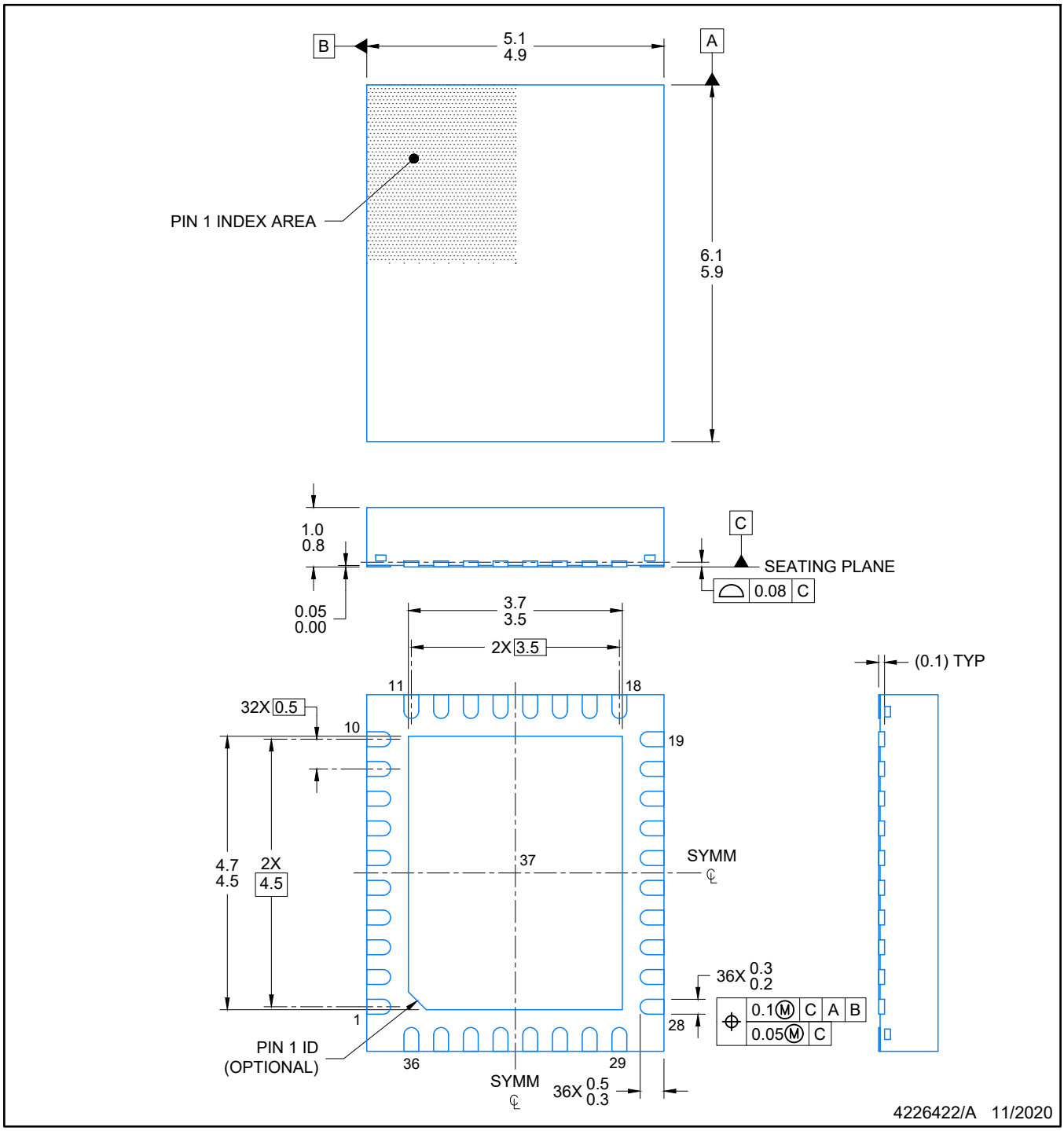
4229484/A

PACKAGE OUTLINE

RRV0036A

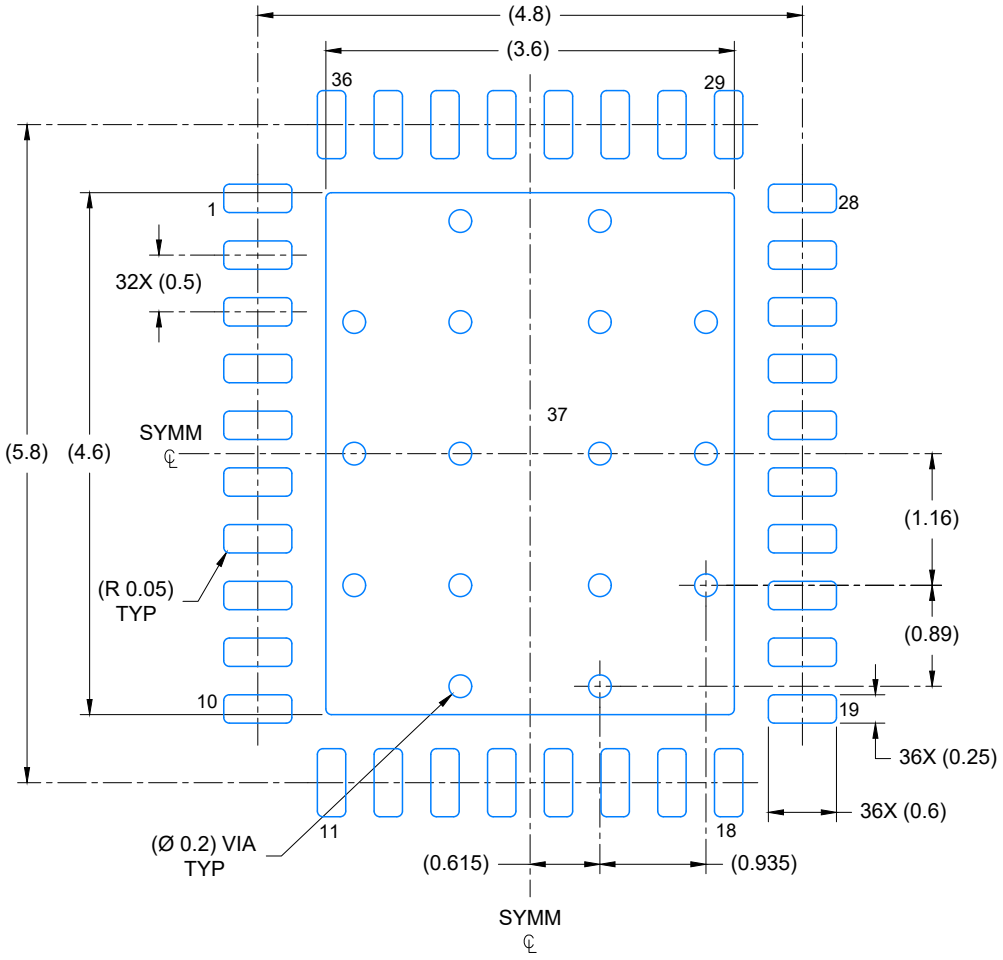
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD

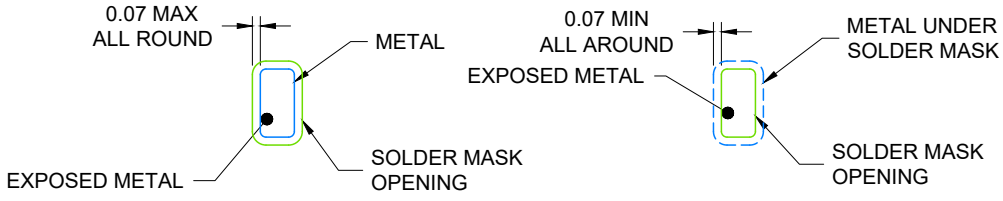


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



NON- SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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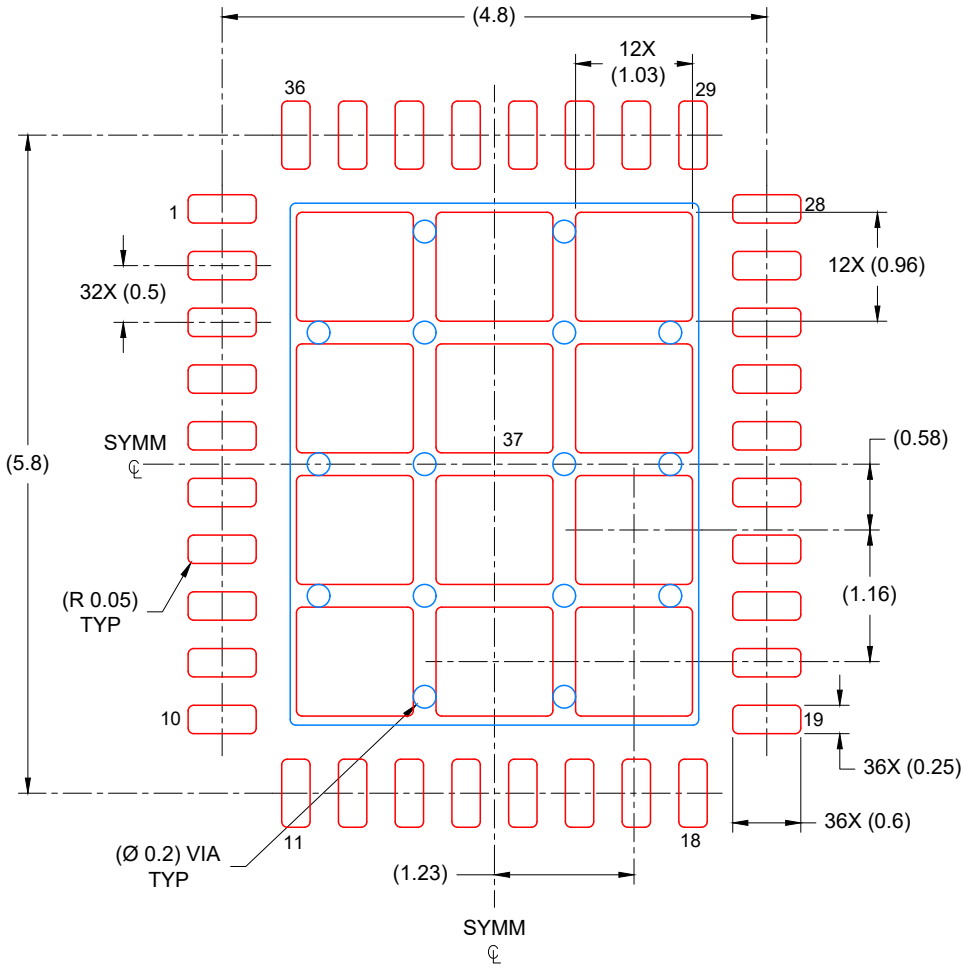
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
72% PRINTED COVERAGE BY AREA
SCALE: 15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月