TEXAS INSTRUMENTS
BQ77307
JAJSSH0 – DECEMBER 2023

BQ77307 リチウムイオン、リチウムポリマ、$LiFePO_4$ (LFP)、および LTO バッテリ パック向け、2 直列～7 直列、高精度バッテリ 1 次側 / 2 次側プロテクタ

1 特長

- 自律的な回復オプション搭載、2 直列～7 直列セル向け、1 次側または 2 次側の電圧、電流、温度からの保護
- 電圧保護：
  - セル過電圧 (COV)：0V～5.5V 1mV 刻み、 ±4mV 精度
  - セル低電圧 (CUV)：0V～5.5V 1mV 刻み、 ±4mV 精度
- 電流保護：
  - 放電時の短絡 (SCD)：10mV～500mV、可変ステップ
  - 充電時の過電流 (OCC)：3mV～123mV、2mV 刻み
  - 放電 1 および 2 の過電流 (OCD1 および OCD2)：4mV～200mV、2mV 刻み
- 外部 NTC サーミスタを使用した温度保護：
  - 充電および放電時の過熱 (OTC および OTD)
  - 充電および放電時の低温 (UTC および UTD)
  - 内部ダイの過熱
- NFET 保護用のローサイド ドライバを内蔵 (オプションの自律回復機能付き)
- 低消費電力動作：
  - 通常モード、両方の FET をイネーブル：8µA
  - 通常モード、FET をディセーブル：5µA
  - シャットダウン・モード：1µA 未満
- 45V の高電圧耐性 (セル接続および他の一部のピン)
- テキサス・インスツルメンツによりプログラム済みのデバイス設定用ワンタイム プログラマブル (OTP) メモリを内蔵
- ホスト プロセッサの割り込みをプログラム可能、I^2C 経由でステータス情報を利用可能
- 400kHz I^2C シリアル通信 (オプションの CRC サポート付き)
- 外部システムで使用するためのプログラム可能な LDO
- 20 ピン QFN 3.5mm × 3.5mm × 0.9mm (RGR) パッケージ

2 アプリケーション

- コードレス電動工具および園芸用具
- 掃除機
- 非軍事用ドローン
- その他産業用バッテリ パック(2 直列～7 直列)

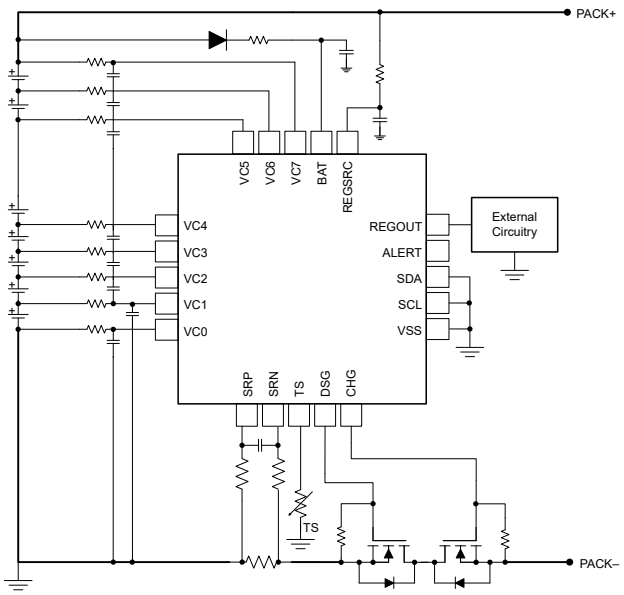
3 概要

テキサス・インスツルメンツの BQ77307 製品ファミリは、2～7 直列リチウムイオン、リチウムポリマ、$LiFePO_4$ (LFP)、LTO バッテリ パック向けの高集積高精度 1 次側プロテクタを搭載しています。各デバイスには、高精度の電圧、電流、温度保護サブシステムと、ローサイド保護 NFET ドライバ、および外部システム用のプログラム可能な LDO が搭載されています。BQ77307 はホスト プロセッサに割り込みを供給するほか、I^2C ホスト通信インターフェースを内蔵しており、最大 400kHz の動作をサポートしているほか、オプションの CRC を使用してステータス情報とプログラム設定を読み取ることができます。BQ77307 は、20 ピン QFN パッケージで供給されます。

製品情報

部品番号	パッケージ (1)	パッケージ・サイズ (公称)
BQ77307	RGR (20 ピン)	3.5mm × 3.5mm × 0.9mm、0.5mm ピッチ

(1) 巻末の注文情報を参照してください。



概略回路図

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4 Device Comparison Table

BQ77307xy DEVICE FAMILY		
PART NUMBER	CELL COUNT SUPPORTED	REGOUT STATUS
BQ77307	7	Enabled, 3.3 V
BQ77307xy(1)	2–7	1.8 V–5.0 V

(1) PRODUCT PREVIEW

5 Pin Configuration and Functions

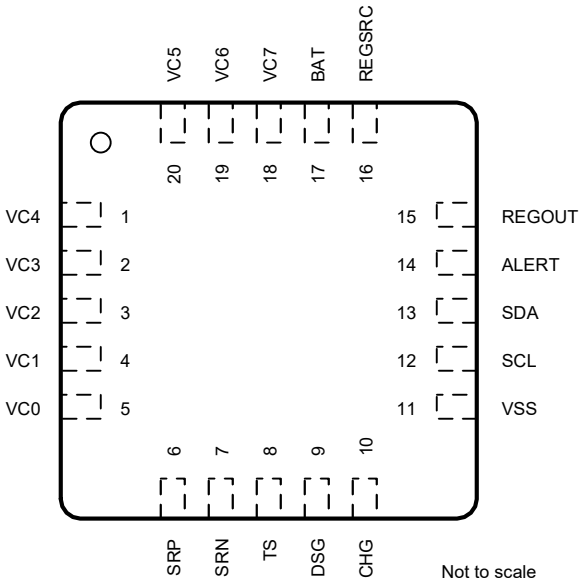


図 5-1. BQ77307 Pinout

表 5-1. BQ77307 Pin Functions

PIN		I/O	TYPE	DESCRIPTION
NO.	NAME			
1	VC4	I	IA	Sense voltage input pin for the fourth cell from the bottom of the stack
2	VC3	I	IA	Sense voltage input pin for the third cell from the bottom of the stack
1	VC2	I	IA	Sense voltage input pin for the second cell from the bottom of the stack
2	VC1	I	IA	Sense voltage input pin for the first cell from the bottom of the stack
3	VC0	I	IA	Sense voltage input pin for negative terminal of the first cell from the bottom of stack and functions as wakeup from SHUTDOWN
6	SRP	I	IA	Analog input pin connected to the internal current protection subsystem, which detects a voltage between SRP and SRN, where SRP is the top of the sense resistor. A charging current generates a positive voltage at SRP relative to SRN.
7	SRN	I	IA	Analog input pin connected to the internal current protection subsystem, which detects a small voltage between SRP and SRN, where SRN is the bottom of the sense resistor. A charging current generates a positive voltage at SRP relative to SRN.
8	TS	I/O	I/OA	Thermistor input and functions as wakeup from SHUTDOWN
9	DSG	O	OA	NMOS Discharge FET drive output pin
10	CHG	O	OA	NMOS Charge FET drive output pin
11	VSS	—	P	Device ground
12	SCL	I/O	I/OD	I^2C serial communication bus clock
13	SDA	I/O	I/OD	I^2C serial communication bus data
14	ALERT	O	OD	Digital interrupt output pin

表 5-1. BQ77307 Pin Functions (続き)

PIN		I/O	TYPE	DESCRIPTION
NO.	NAME			
15	REGOUT	O	OA	LDO output, which can be programmed for 1.8 V, 2.5 V, 3.0 V, 3.3 V, or 5.0 V
16	REGSRC	I	IA	Input pin for REGOUT LDO also functions as a supply for the CHG and DSG FET drivers.
17	BAT	I	P	Primary power supply input pin
18	VC7	I	IA	Sense voltage input pin for the seventh cell from the bottom of the stack
19	VC6	I	IA	Sense voltage input pin for the sixth cell from the bottom of the stack
20	VC5	I	IA	Sense voltage input pin for the fifth cell from the bottom of the stack

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

DESCRIPTION	PINS	MIN	MAX	UNIT
Supply voltage range, $V_{IN(DC)}$ (2)	BAT, REGSRC	VSS–0.3	VSS+40	V
Short duration input voltage range, $V_{IN(short)}$ (2)	VC1 - VC7, BAT, REGSRC, CHG		VSS+45	V
DC input voltage range, $V_{IN(DC)}$	ALERT, SCL, SDA	VSS–0.3	VSS+6	V
DC input voltage range, $V_{IN(DC)}$	TS	VSS–0.3	2.1	V
DC input voltage range, $V_{IN(DC)}$ (2)	SRP, SRN	VSS–0.3	2.1	V
DC input voltage range, $V_{IN(DC)}$ (2)	VC7	Maximum of VSS–0.3 and VC6–0.3	VSS+40	V
DC input voltage range, $V_{IN(DC)}$ (2)	VC6	Maximum of VSS–0.3 and VC5–0.3	VSS+40	V
DC input voltage range, $V_{IN(DC)}$ (2)	VC5	Maximum of VSS–0.3 and VC4–0.3	VSS+40	V
DC input voltage range, $V_{IN(DC)}$ (2)	VC4	Maximum of VSS–0.3 and VC3–0.3	VSS+40	V
DC input voltage range, $V_{IN(DC)}$ (2)	VC3	Maximum of VSS–0.3 and VC2–0.3	VSS+40	V
DC input voltage range, $V_{IN(DC)}$ (2)	VC2	Maximum of VSS–0.3 and VC1–0.3	VSS+40	V
DC input voltage range, $V_{IN(DC)}$ (2)	VC1	Maximum of VSS–0.3 and VC0–0.3	VSS+40	V
DC input voltage range, $V_{IN(DC)}$	VC0	VSS–0.3	VSS+6	V
DC input voltage range, $V_{IN(DC)}$ (2)	CHG	VSS–30	VSS+40	V
Output voltage range, V_O	DSG	VSS–0.3	VSS+20	V
Output voltage range, V_O	REGOUT	VSS–0.3	VSS+6	V
Junction temperature, T_J		–65	150	°C
Storage temperature, T_{STG}		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Stresses applied above $V_{IN(DC)}$ and below $V_{IN(SHORT)}$ should be limited to less than 100 hours over the lifetime of the device. These stresses may occur during brief transient events but DC voltages in this range should not be applied.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1000	V
$V_{(ESD)}$	Electrostatic discharge	Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±250	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Typical values stated where T_A = 25°C and V_{BAT} = 25.9 V, min/max values stated where T_A = -40°C to 110°C and V_{BAT} = 3 V to 38.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BAT}	Supply voltage	Voltage on BAT pin (normal operation)	3		38.5	V
$V_{BAT(UVLO)}$	Under voltage lockout level	Falling voltage on BAT causing device reset		2.5		V
$V_{WAKEONTS}$	Wake on TS voltage	Voltage on BAT pin in valid range	0.65		1.2	V
$V_{WAKEONVC0}$	Wake on VC0 voltage	Voltage on BAT pin in valid range	0.65		1.2	V
V_{IN}	Input voltage range	ALERT, SCL, SDA	0		5.5	V
V_{IN}	Input voltage range for thermistor temperature protection	TS	–0.2		1.8	V
V_{IN}	Input voltage range	SRP, SRN	–0.2		1.8	V
V_{IN}	Input voltage range(3)	$V_{VC(0)}$	–0.2		3.0	V
V_{IN}	Input voltage range	$V_{VC(x)}$, 1 ≤ x ≤ 4	maximum of $V_{VC(x–1)}$ – 0.2 or VSS – 0.2		minimum of $V_{VC(x–1)}$+5.5 or VSS + 38.5	V
V_{IN}	Input voltage range	$V_{VC(x)}$, x ≥ 5	maximum of $V_{VC(x–1)}$ – 0.2 or VSS + 2.0		minimum of $V_{VC(x–1)}$ + 5.5 or VSS + 38.5	V
V_O	Output voltage range	CHG	–25		38.5	V
V_O	Output voltage range	DSG	–0.2		14	V
R_C	External cell input resistance(2) (3)		10		1000	Ω
C_C	External cell input capacitance(2) (3)		0.1		10	µF
R_f	External supply filter resistance (BAT pin)(3)		50		1000	Ω
C_f	External supply filter capacitance (BAT pin)(3)		1		40	µF
R_{filt}	Sense resistor filter resistance(3)			100	200	Ω
C_{REGSRC}	REGSRC capacitance(3)		1			µF
R_{TS}	External thermistor nominal resistance (103-AT) at 25°C			10		kΩ
T_{OPR}	Junction temperature during operation(1)		–40		110	°C

(1) Power dissipated within device should be limited to ensure junction temperature remains within specification during operation.
(2) External cell input resistance times external input capacitance should be limited to 200µs or below.
(3) Specified by design

6.4 Thermal Information BQ77307

THERMAL METRIC(1)		BQ77307 RGR (QFN) 20 PINS	UNIT
$R_{θJA}$	Junction-to-ambient thermal resistance	47.2	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	47.9	°C/W
$R_{θJC(bottom)}$	Junction-to-case (bottom) thermal resistance	8.3	°C/W

6.4 Thermal Information BQ77307 (続き)

THERMAL METRIC(1)		BQ77307 RGR (QFN) 20 PINS	UNIT
$R_{\theta JB}$	Junction-to-board thermal resistance	23.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	23.4	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Supply Current

Typical values stated where T_A = 25°C and V_{BAT} = 25.9 V, min/max values stated where T_A = -40°C to 110°C and V_{BAT} = 3 V to 38.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{SLEEP}	NORMAL Mode	NORMAL mode, REGOUT = OFF, CHG = OFF, DSG = ON, no communication, **Power:Normal:Voltage Time** = 5 s		6		µA
$I_{SHUTDOWN}$	SHUTDOWN Mode	All blocks powered down, no protections, no communication		1	2	µA

6.6 Digital I/O

Typical values stated where T_A = 25°C and V_{BAT} = 25.9 V, min/max values stated where T_A = -40°C to 110°C and V_{BAT} = 3 V to 38.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input	SCL, SDA	1.23		5.5	V
V_{IL}	Low-level input	SCL, SDA			0.53	V
V_{OL}	Output voltage low	ALERT, SCL, SDA, V_{BAT} ≥ 3 V, I_{OL} = 5 mA, 10 pF load			0.4	V
C_{IN}	Input capacitance(1)	ALERT, SCL, SDA		2		pF
I_{LKG}	Input leakage current	ALERT, SCL, SDA, device in SHUTDOWN mode			1	µA

(1) Specified by design

6.7 REGOUT LDO

Typical values stated where T_A = 25°C and V_{BAT} = 25.9 V, min/max values stated where T_A = -40°C to 110°C and V_{BAT} = 3 V to 38.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{REGOUT\_1.8\_LOW}$	Regulator voltage (nominal 1.8 V setting)	V_{BAT}, V_{REGSRC} = 3.0 V, I_{REGOUT} = 10 mA	1.62	1.8	1.92	V
$V_{REGOUT\_1.8}$	Regulator voltage (nominal 1.8 V setting) (1)	V_{BAT} ≥ 3.0 V, V_{REGSRC} ≥ 3.8 V, I_{REGOUT} = 0 mA to 20 mA	1.62	1.8	1.92	V
$V_{REGOUT\_2.5\_LOW}$	Regulator voltage (nominal 2.5 V setting) (1)	V_{BAT}, V_{REGSRC} = 3.0 V, I_{REGOUT} = 10 mA	2.25	2.5	2.75	V
$V_{REGOUT\_2.5}$	Regulator voltage (nominal 2.5 V setting) (1)	V_{BAT} ≥ 3.0 V, V_{REGSRC} ≥ 3.8 V, I_{REGOUT} = 0 mA to 20 mA	2.25	2.5	2.75	V
$V_{REGOUT\_3.0}$	Regulator voltage (nominal 3.0 V setting) (1)	V_{BAT} ≥ 3.0 V, V_{REGSRC} ≥ 3.8 V, I_{REGOUT} = 0 mA to 20 mA	2.7	3.0	3.3	V
$V_{REGOUT\_3.3}$	Regulator voltage (nominal 3.3 V setting) (1)	V_{BAT} ≥ 3.0 V, V_{REGSRC} ≥ 4.2 V, I_{REGOUT} = 0 mA to 20 mA	3	3.3	3.6	V

6.7 REGOUT LDO (続き)

Typical values stated where T_A = 25°C and V_{BAT} = 25.9 V, min/max values stated where T_A = -40°C to 110°C and V_{BAT} = 3 V to 38.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{REGOUT\_5.0}$	Regulator voltage (nominal 5.0 V setting) (1)	V_{BAT} ≥ 3.0 V, V_{REGSRC} ≥ 5.5 V, I_{REGOUT} = 0 mA to 20 mA	4.5	5.0	5.5	V
$\Delta V_{O(TEMP)}$	Regulator output over temperature	ΔV_{REGOUT} vs (V_{REGOUT} at 25°C, I_{REGOUT} = 20 mA, V_{BAT} = 3.0 V, V_{REGSRC} = 5.5 V, V_{REGOUT} set to nominal 3.3 V setting)		±0.015%		per °C
$\Delta V_{O(LINE)}$	Line regulation(1)	ΔV_{REGOUT} vs (V_{REGOUT} at 25°C, V_{BAT} = 3.0 V, V_{REGSRC} = 4.2 V, I_{REGOUT} = 5 mA), as V_{REGSRC} varies from 4.2 V to 38.5 V, V_{REGOUT} set to nominal 3.3 V setting	–1%		1%	
I_{SC}	Regulator short-circuit current limit	V_{REGOUT} = 0 V	23		50	mA
C_{EXT}	External capacitor REGOUT to VSS(2)		1			µF

(1) Specified by a combination of characterization and production test.
(2) Specified by design

6.8 Voltage References

Typical values stated where T_A = 25°C and V_{BAT} = 25.9 V, min/max values stated where T_A = -40°C to 110°C and V_{BAT} = 3 V to 38.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOLTAGE REFERENCE 1						
$V_{(REF1)}$	Internal reference voltage (1)	T_A = 25°C	1.1955	1.1962	1.1969	V
$V_{(REF1DRIFT)}$	Internal reference voltage drift (1)	T_A = -40°C to 110°C		±29		PPM/°C
VOLTAGE REFERENCE 2						
$V_{(REF2)}$	Internal reference voltage (2)	T_A = 25°C	1.226	1.227	1.229	V
$V_{(REF2DRIFT)}$	Internal reference voltage drift(2)	T_A = -40°C to 110°C		±52		PPM/°C

(1) $V_{(REF1)}$ is used for the cell voltage and thermistor threshold voltage detection subsystem.
(2) $V_{(REF2)}$ is used for the LDOs and current protection subsystem

6.9 Current Detector

Typical values stated where T_A = 25°C and V_{BAT} = 25.9 V, min/max values stated where T_A = -40°C to 110°C and V_{BAT} = 3 V to 38.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{CUR\_DET\_THR}$	Current detection voltage threshold (V_{SRP} – V_{SRN}), setting = 1, positive threshold (charging current) (1)	T_A = -20°C to 65°C. Measured using averaged data to remove effects of noise.	186	271	355	µV
$V_{CUR\_DET\_THR}$	Current detection voltage threshold (V_{SRP} – V_{SRN}), setting = 2, positive threshold (charging current) (1)	T_A = -20°C to 65°C. Measured using averaged data to remove effects of noise.	670	794	921	µV
$V_{CUR\_DET\_THR}$	Current detection voltage threshold (V_{SRP} – V_{SRN}), setting = 3, positive threshold (charging current) (1)	T_A = -20°C to 65°C. Measured using averaged data to remove effects of noise.	1145	1317	1503	µV
$V_{CUR\_DET\_THR}$	Current detection voltage threshold (V_{SRP} – V_{SRN}), setting = 4, positive threshold (charging current) (1)	T_A = -20°C to 65°C. Measured using averaged data to remove effects of noise.	1594	1838	2089	µV
$V_{CUR\_DET\_THR}$	Current detection voltage threshold (V_{SRP} – V_{SRN}), setting = 5, positive threshold (charging current) (1)	T_A = -20°C to 65°C. Measured using averaged data to remove effects of noise.	2056	2364	2676	µV

6.9 Current Detector (続き)

Typical values stated where T_A = 25°C and V_{BAT} = 25.9 V, min/max values stated where T_A = -40°C to 110°C and V_{BAT} = 3 V to 38.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{CUR\_DET\_THR}$	Current detection voltage threshold ($V_{SRP} – V_{SRN}$), setting = 6, positive threshold (charging current) (1)	T_A = -20°C to 65°C. Measured using averaged data to remove effects of noise.	2516	2890	3276	µV
$V_{CUR\_DET\_THR}$	Current detection voltage threshold ($V_{SRP} – V_{SRN}$), setting = 7, positive threshold (charging current) (1)	T_A = -20°C to 65°C. Measured using averaged data to remove effects of noise.	3000	3419	3851	µV
$V_{CUR\_DET\_THR}$	Current detection voltage threshold ($V_{SRP} – V_{SRN}$), setting = 8, positive threshold (charging current) (1)	T_A = -20°C to 65°C. Measured using averaged data to remove effects of noise.	3460	3942	4443	µV
$V_{CUR\_DET\_THR}$	Current detection voltage threshold ($V_{SRP} – V_{SRN}$), setting = 9, positive threshold (charging current) (1)	T_A = -20°C to 65°C. Measured using averaged data to remove effects of noise.	3893	4466	5045	µV
$V_{CUR\_DET\_THR}$	Current detection voltage threshold ($V_{SRP} – V_{SRN}$), setting = 10, positive threshold (charging current) (1)	T_A = -20°C to 65°C. Measured using averaged data to remove effects of noise.	4386	4994	5627	µV
$V_{CUR\_DET\_THR}$	Current detection voltage threshold ($V_{SRP} – V_{SRN}$), setting = 1, positive threshold (charging current) (1)	T_A = -40°C to 110°C. Measured using averaged data to remove effects of noise.	88	275	462	µV
$V_{CUR\_DET\_THR}$	Current detection voltage threshold ($V_{SRP} – V_{SRN}$), setting = 2, positive threshold (charging current) (1)	T_A = -40°C to 110°C. Measured using averaged data to remove effects of noise.	581	794	978	µV
$V_{CUR\_DET\_THR}$	Current detection voltage threshold ($V_{SRP} – V_{SRN}$), setting = 3, positive threshold (charging current) (1)	T_A = -40°C to 110°C. Measured using averaged data to remove effects of noise.	1050	1317	1537	µV
$V_{CUR\_DET\_THR}$	Current detection voltage threshold ($V_{SRP} – V_{SRN}$), setting = 4, positive threshold (charging current) (1)	T_A = -40°C to 110°C. Measured using averaged data to remove effects of noise.	1527	1836	2106	µV
$V_{CUR\_DET\_THR}$	Current detection voltage threshold ($V_{SRP} – V_{SRN}$), setting = 5, positive threshold (charging current) (1)	T_A = -40°C to 110°C. Measured using averaged data to remove effects of noise.	1974	2360	2711	µV
$V_{CUR\_DET\_THR}$	Current detection voltage threshold ($V_{SRP} – V_{SRN}$), setting = 6, positive threshold (charging current) (1)	T_A = -40°C to 110°C. Measured using averaged data to remove effects of noise.	2483	2885	3290	µV
$V_{CUR\_DET\_THR}$	Current detection voltage threshold ($V_{SRP} – V_{SRN}$), setting = 7, positive threshold (charging current) (1)	T_A = -40°C to 110°C. Measured using averaged data to remove effects of noise.	2897	3412	3885	µV
$V_{CUR\_DET\_THR}$	Current detection voltage threshold ($V_{SRP} – V_{SRN}$), setting = 8, positive threshold (charging current) (1)	T_A = -40°C to 110°C. Measured using averaged data to remove effects of noise.	3357	3933	4498	µV
$V_{CUR\_DET\_THR}$	Current detection voltage threshold ($V_{SRP} – V_{SRN}$), setting = 9, positive threshold (charging current) (1)	T_A = -40°C to 110°C. Measured using averaged data to remove effects of noise.	3793	4458	5062	µV
$V_{CUR\_DET\_THR}$	Current detection voltage threshold ($V_{SRP} – V_{SRN}$), setting = 10, positive threshold (charging current) (1)	T_A = -40°C to 110°C. Measured using averaged data to remove effects of noise.	4261	4986	5654	µV
$V_{CUR\_DET\_THR}$	Current detection voltage threshold ($V_{SRP} – V_{SRN}$), setting = 1, negative threshold (discharging current) (1)	T_A = -20°C to 65°C. Measured using averaged data to remove effects of noise.	–719	–635	–546	µV
$V_{CUR\_DET\_THR}$	Current detection voltage threshold ($V_{SRP} – V_{SRN}$), setting = 2, negative threshold (discharging current) (1)	T_A = -20°C to 65°C. Measured using averaged data to remove effects of noise.	–1234	–1118	–1005	µV
$V_{CUR\_DET\_THR}$	Current detection voltage threshold ($V_{SRP} – V_{SRN}$), setting = 3, negative threshold (discharging current) (1)	T_A = -20°C to 65°C. Measured using averaged data to remove effects of noise.	–1736	–1605	–1469	µV

6.9 Current Detector (続き)

Typical values stated where T_A = 25°C and V_{BAT} = 25.9 V, min/max values stated where T_A = -40°C to 110°C and V_{BAT} = 3 V to 38.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{CUR\_DET\_THR}$	Current detection voltage threshold ($V_{SRP} – V_{SRN}$), setting = 4, negative threshold (discharging current) (1)	T_A = -20°C to 65°C. Measured using averaged data to remove effects of noise.	–2262	–2088	–1917	µV
$V_{CUR\_DET\_THR}$	Current detection voltage threshold ($V_{SRP} – V_{SRN}$), setting = 5, negative threshold (discharging current) (1)	T_A = -20°C to 65°C. Measured using averaged data to remove effects of noise.	–2794	–2579	–2354	µV
$V_{CUR\_DET\_THR}$	Current detection voltage threshold ($V_{SRP} – V_{SRN}$), setting = 6, negative threshold (discharging current) (1)	T_A = -20°C to 65°C. Measured using averaged data to remove effects of noise.	–3324	–3067	–2805	µV
$V_{CUR\_DET\_THR}$	Current detection voltage threshold ($V_{SRP} – V_{SRN}$), setting = 7, negative threshold (discharging current) (1)	T_A = -20°C to 65°C. Measured using averaged data to remove effects of noise.	–3849	–3552	–3245	µV
$V_{CUR\_DET\_THR}$	Current detection voltage threshold ($V_{SRP} – V_{SRN}$), setting = 8, negative threshold (discharging current) (1)	T_A = -20°C to 65°C. Measured using averaged data to remove effects of noise.	–4369	–4037	–3704	µV
$V_{CUR\_DET\_THR}$	Current detection voltage threshold ($V_{SRP} – V_{SRN}$), setting = 9, negative threshold (discharging current) (1)	T_A = -20°C to 65°C. Measured using averaged data to remove effects of noise.	–4913	–4527	–4129	µV
$V_{CUR\_DET\_THR}$	Current detection voltage threshold ($V_{SRP} – V_{SRN}$), setting = 10, negative threshold (discharging current) (1)	T_A = -20°C to 65°C. Measured using averaged data to remove effects of noise.	–5425	–5012	–4577	µV
$V_{CUR\_DET\_THR}$	Current detection voltage threshold ($V_{SRP} – V_{SRN}$), setting = 1, negative threshold (discharging current) (1)	T_A = -40°C to 110°C. Measured using averaged data to remove effects of noise.	–862	–630	–369	µV
$V_{CUR\_DET\_THR}$	Current detection voltage threshold ($V_{SRP} – V_{SRN}$), setting = 2, negative threshold (discharging current) (1)	T_A = -40°C to 110°C. Measured using averaged data to remove effects of noise.	–1340	–1113	–865	µV
$V_{CUR\_DET\_THR}$	Current detection voltage threshold ($V_{SRP} – V_{SRN}$), setting = 3, negative threshold (discharging current) (1)	T_A = -40°C to 110°C. Measured using averaged data to remove effects of noise.	–1887	–1600	–1284	µV
$V_{CUR\_DET\_THR}$	Current detection voltage threshold ($V_{SRP} – V_{SRN}$), setting = 4, negative threshold (discharging current) (1)	T_A = -40°C to 110°C. Measured using averaged data to remove effects of noise.	–2387	–2087	–1765	µV
$V_{CUR\_DET\_THR}$	Current detection voltage threshold ($V_{SRP} – V_{SRN}$), setting = 5, negative threshold (discharging current) (1)	T_A = -40°C to 110°C. Measured using averaged data to remove effects of noise.	–2949	–2575	–2179	µV
$V_{CUR\_DET\_THR}$	Current detection voltage threshold ($V_{SRP} – V_{SRN}$), setting = 6, negative threshold (discharging current) (1)	T_A = -40°C to 110°C. Measured using averaged data to remove effects of noise.	–3487	–3064	–2622	µV
$V_{CUR\_DET\_THR}$	Current detection voltage threshold ($V_{SRP} – V_{SRN}$), setting = 7, negative threshold (discharging current) (1)	T_A = -40°C to 110°C. Measured using averaged data to remove effects of noise.	–3991	–3548	–3083	µV
$V_{CUR\_DET\_THR}$	Current detection voltage threshold ($V_{SRP} – V_{SRN}$), setting = 8, negative threshold (discharging current) (1)	T_A = -40°C to 110°C. Measured using averaged data to remove effects of noise.	–4599	–4033	–3420	µV
$V_{CUR\_DET\_THR}$	Current detection voltage threshold ($V_{SRP} – V_{SRN}$), setting = 9, negative threshold (discharging current) (1)	T_A = -40°C to 110°C. Measured using averaged data to remove effects of noise.	–5067	–4521	–3918	µV
$V_{CUR\_DET\_THR}$	Current detection voltage threshold ($V_{SRP} – V_{SRN}$), setting = 10, negative threshold (discharging current) (1)	T_A = -40°C to 110°C. Measured using averaged data to remove effects of noise.	–5580	–5011	–4415	µV

6.9 Current Detector (続き)

Typical values stated where T_A = 25°C and V_{BAT} = 25.9 V, min/max values stated where T_A = -40°C to 110°C and V_{BAT} = 3 V to 38.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{CUR_DET}	Measurement interval			2.44		ms

(1) Specified by a combination of characterization and production test

6.10 Thermistor Pullup Resistor

Typical values stated where T_A = 25°C and V_{BAT} = 25.9 V, min/max values stated where T_A = -40°C to 110°C and V_{BAT} = 3 V to 38.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{(TS\_PU)}$	Internal pullup resistance at 25°C(1)		19.75	20	20.25	kΩ
$R_{(TS\_PU\_DRIFT)}$	Internal pullup resistance change over temperature (1) (2)	Change over -20°C/+65°C vs value at 25°C for nominal 20-kΩ	–36		28	Ω
$R_{(TS\_PU\_DRIFT)}$	Internal pullup resistance change over temperature (1) (2)	Change over -40°C/+110°C vs value at 25°C for nominal 20-kΩ	–53		98	Ω

(1) The internal pullup resistance includes only the resistance between the REG18 internal LDO and the point where the voltage is sensed by the protection subsystem.
(2) Specified by characterization

6.11 Hardware Overtemperature Detector

Typical values stated where T_A = 25°C and V_{BAT} = 25.9 V, min/max values stated where T_A = -40°C to 110°C and V_{BAT} = 3 V to 38.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(OTSD)}$	Hardware overtemperature detector threshold(1)		118		132	°C

(1) Specified by design

6.12 Internal Oscillator

Typical values stated where T_A = 25°C and V_{BAT} = 25.9 V, min/max values stated where T_A = -40°C to 110°C and V_{BAT} = 3 V to 38.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Low-frequency Oscillator						
f_{LFO}	Operating frequency			32.770		kHz
$f_{LFOS(ERR)}$	Frequency drift (1)	Change in frequency vs value at 25°C, T_A = –20°C to +65°C.	–1.0%	±0.33%	1.0%	
$f_{LFOS(ERR)}$	Frequency drift (1)	Change in frequency vs value at 25°C, T_A = –40°C to +110°C.	–1.6%	±0.67%	1.9%	
$f_{LFO(FAIL)}$	Failure detection frequency	Detects oscillator failure if the frequency falls below this level.	11	14.1	18	kHz

(1) Specified by characterization

6.13 Charge and Discharge FET Drivers

Typical values stated where T_A = 25°C and V_{BAT} = 25.9 V, min/max values stated where T_A = -40°C to 110°C and V_{BAT} = 3 V to 38.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(FETON\_DSG)}$	DSG driver enabled	V_{REGSRC} ≥ 12 V, C_L= 20 nF	10.5	11.5	13	V
$V_{(FETON\_CHG)}$	CHG driver enabled	V_{REGSRC} ≥ 12 V, C_L= 20 nF	10	11	12	V
$V_{(FETON\_LOBAT\_DSG)}$	DSG driver enabled	V_{REGSRC} < 12 V, C_L = 20 nF	V_{REGSRC} – 1.0		V_{REGSRC}	V
$V_{(FETON\_LOBAT\_CHG)}$	CHG driver enabled	V_{REGSRC} < 12 V, C_L = 20 nF	V_{REGSRC} – 1.75		V_{REGSRC}	V
$t_{(CHG\_ON)}$	CHG FET driver rise time	CHG C_L = 20 nF, R_{GATE} = 100 Ω, V_{REGSRC} = 12 V, 0.5 V to 5 V		50	85	µs
$t_{(DSG\_ON)}$	DSG FET driver rise time	DSG C_L = 20 nF, R_{GATE} = 100 Ω, V_{REGSRC} = 12 V, 0.5 V to 5 V		35	55	µs
$t_{(CHG\_OFF)}$	CHG FET driver fall time	CHG C_L = 20 nF, R_{GATE} = 100 Ω, V_{REGSRC} = 12 V, 80% to 20% of $V_{(FETON\_CHG)}$		24	35	µs
$t_{(DSG\_OFF)}$	DSG FET driver fall time	DSG C_L = 20 nF, R_{GATE} = 100 Ω, V_{REGSRC} = 12 V, 80% to 20% of $V_{(FETON\_DSG)}$		2	3	µs
$I_{(CHG\_ON)}$	CHG FET driver output current	CHG enabled and pin held at 8 V, V_{REGSRC} = 12 V		1		mA
$I_{(DSG\_ON)}$	DSG FET driver output current	DSG enabled and pin held at 8 V, V_{REGSRC} = 12 V		1.56		mA
$R_{(DSG\_OFF)}$	DSG FET driver off resistance	DSG off and pin held at 100 mV		15	30	Ω
$V_{(CHG\_DETECT)}$	CHG detector threshold	CHG pin voltage rising	1.2		1.8	V
$V_{(CHG\_DET\_HYS)}$	CHG detector hysteresis			0.95		V

6.14 Protection Subsystem

Typical values stated where T_A = 25°C and V_{BAT} = 25.9 V, min/max values stated where T_A = -40°C to 110°C and V_{BAT} = 3 V to 38.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(CV\_ACC)}$	Cell overvoltage (COV) and cell undervoltage (CUV) protection threshold voltage accuracy (2)	0 V < $V_{VC(x)}$ - $V_{VC(x-1)}$ < 4.5 V, T_A = 25°C, 1 ≤ x ≤ 7, using an input network of 10-Ω and 220 nF	–4		4	mV
		0 V < $V_{VC(x)}$ - $V_{VC(x-1)}$ < 4.5 V, T_A = –20°C to 65°C, 1 ≤ x ≤ 7, using an input network of 10-Ω and 220 nF	–8		7	mV
		0 V < $V_{VC(x)}$ - $V_{VC(x-1)}$ < 4.5 V, T_A = –40°C to 110°C, 1 ≤ x ≤ 7, using an input network of 10-Ω and 220 nF	–10		10	mV
		0 V < $V_{VC(x)}$ - $V_{VC(x-1)}$ < 5.5 V, T_A = –40°C to 110°C, 1 ≤ x ≤ 7, using an input network of 10-Ω and 220 nF	–13		12	mV
$V_{(CV\_DLY)}$	Cell overvoltage (COV) and cell undervoltage (CUV) detection delay accuracy (1)	Error in delay versus nominal delay setting	–5%		5%	
$V_{(TS\_ACC)}$	Thermistor temperature protection threshold accuracy (2)	Error in threshold versus nominal setting, threshold set in terms of V_{TS} / V_{REG18}.	–2%		2%	
$V_{(TS\_DLY)}$	Thermistor temperature protection delay accuracy (2)	Error in delay versus nominal setting	–5%		5%	

6.14 Protection Subsystem (続き)

Typical values stated where T_A = 25°C and V_{BAT} = 25.9 V, min/max values stated where T_A = -40°C to 110°C and V_{BAT} = 3 V to 38.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(TINT\_ACC)}$	Internal temperature protection threshold accuracy (2)	Error in threshold versus nominal setting, T_A = –20°C to 65°C	–5.8		5.0	℃
		Error in threshold versus nominal setting, T_A = –40°C to 110°C	–7.8		5.3	℃
$V_{(SCD)}$	Short circuit in discharge voltage threshold range	Nominal settings, threshold based on $V_{SRP} – V_{SRN}$		–10, –20, –40, –60, –80, –100, –125, –150, –175, –200, –250, –300, –350, –400, –450, –500		mV
$V_{(SCD\_ACC)}$	Short circuit in discharge voltage threshold detection accuracy (2)	–10 mV setting	–36%		22%	
		–20 mV setting	–19%		12%	
		–40 mV setting	–14%		6%	
		Settings –60 mV to –500 mV	–11%		6%	
$V_{(SCD\_DLY)}$	Short circuit in discharge detection delay(1)	Fastest setting (with 3 mV overdrive)		8		µs
		Fastest setting (with 25 mV overdrive)		0.6		µs
		Setting for 15 µs (with 3 mV overdrive)		20	28	µs
		Setting for 15 µs (with 25 mV overdrive)			20	µs
		Settings for 31 µs (with 25 mV overdrive)	14		35	µs
		Settings for 61 µs (with 25 mV overdrive)	42		66	µs
		Settings for 122 µs (with 25 mV overdrive)	102		130	µs
		Settings for 244 µs (with 25 mV overdrive)	218		258	µs
		Settings for 488 µs (with 25 mV overdrive)	452		510	µs
		Settings for 977 µs (with 25 mV overdrive)	920		1018	µs
		Settings for 1953 µs (with 25 mV overdrive)	1860		2034	µs
		Settings for 3906 µs (with 25 mV overdrive)	3735		4065	µs
		Setting for 7797 µs (with 25 mV overdrive)	7470		8112	µs
$V_{(OCC)}$	Overcurrent in charge (OCC) voltage threshold range	Nominal settings, threshold based on $V_{SRP} – V_{SRN}$		3 mV to 123 mV in 2 mV steps		mV
$V_{(OCC\_ACC)}$	Overcurrent in charge (OCC) voltage threshold accuracy (2)	Settings 3 mV to 19 mV	–1.17		1.32	mV
$V_{(OCC\_ACC)}$	Overcurrent in charge (OCC) voltage threshold accuracy (2)	Settings 21 mV to 55 mV	–1.68		2.99	mV

6.14 Protection Subsystem (続き)

Typical values stated where T_A = 25°C and V_{BAT} = 25.9 V, min/max values stated where T_A = -40°C to 110°C and V_{BAT} = 3 V to 38.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(OCC\_ACC)}$	Overcurrent in charge (OCC) voltage threshold accuracy (2)	Settings 57 mV to 123 mV	–1.61		4.10	mV
$V_{(OCD)}$	Overcurrent in discharge (OCD1, OCD2) voltage threshold ranges	Nominal settings, thresholds based on $V_{SRP} – V_{SRN}$		–4 mV to –200 mV in 2 mV steps		mV
$V_{(OCD\_ACC)}$	Overcurrent (OCD1, OCD2) detection voltage threshold accuracy (2)	Settings –4 mV to –18 mV	–1.23		0.84	mV
		Settings –20 mV to –56 mV	–2.84		1.59	mV
		Settings –58 mV to –100 mV	–2.15		2.58	mV
		Settings –102 mV to –200 mV	–2,86		4,19	mV
$V_{(OC\_DLY)}$	Overcurrent (OCC, OCD1, OCD2) detection delay (independent delay setting for each protection)	Fastest setting		0.46		ms
		Nominal settings, low range		1.22 ms to 20.435 ms in 0.305 ms steps		ms
		Nominal settings, medium low range		22.875 ms to 176.595 ms in 2.441 ms steps		ms
		Nominal settings, medium high range		181.475 ms to 488.915 ms in 4.883 ms steps		ms
		Nominal settings, high range		498.675 ms to 1103.795 ms in 9.766 ms steps		ms
$V_{(OC\_DLY)}$	Overcurrent (OCC, OCD1, OCD2) detection delay accuracy(1)	Fastest setting	–0.35		0.35	ms
		Nominal settings, low range	–1.2		0.90	ms
		Nominal settings, medium low range	–7.5		7.2	ms
		Nominal settings, medium high range	–20		20	ms
		Nominal settings, high range	–45		45	ms

(1) Specified by design
(2) Specified by a combination of characterization and production test

6.15 Timing Requirements - I²C Interface, 100kHz Mode

Typical values stated where T_A = 25°C and V_{BAT} = 25.9 V, min/max values stated where T_A = -40°C to 110°C and V_{BAT} = 3 V to 38.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCL}	Clock operating frequency(1)	SCL duty cycle = 50%			100	kHz
$t_{HD:STA}$	START condition hold time(1)		4.0			µs
t_{LOW}	Low period of the SCL clock(1)		4.7			µs
t_{HIGH}	High period of the SCL clock(1)		4.0			µs

6.15 Timing Requirements - I²C Interface, 100kHz Mode (続き)

Typical values stated where T_A = 25°C and V_{BAT} = 25.9 V, min/max values stated where T_A = -40°C to 110°C and V_{BAT} = 3 V to 38.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{SU:STA}$	Setup repeated START(1)		4.7			µs
$t_{HD:DAT}$	Data hold time (SDA input)(1)		0			ns
$t_{SU:DAT}$	Data setup time (SDA input)(1)		250			ns
t_r	Clock rise time(1)	10% to 90%			1000	ns
t_f	Clock fall time(1)	90% to 10%			300	ns
$t_{SU:STO}$	Setup time STOP condition(1)		4.0			µs
t_{BUF}	Bus free time STOP to START(1)		4.7			µs
t_{RST}	I²C bus reset(1)	Bus interface is reset if SCL is detected low for this duration	1.9		2.1	s
R_{PULLUP}	Pullup resistor(1)	Pullup voltage rail ≤ 5 V	1.1			kΩ

(1) Specified by design

6.16 Timing Requirements - I²C Interface, 400kHz Mode

Typical values stated where T_A = 25°C and V_{BAT} = 25.9 V, min/max values stated where T_A = -40°C to 110°C and V_{BAT} = 3 V to 38.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCL}	Clock operating frequency(1)	SCL duty cycle = 50%			400	kHz
$t_{HD:STA}$	START condition hold time(1)		0.6			µs
t_{LOW}	Low period of the SCL clock(1)		1.3			µs
t_{HIGH}	High period of the SCL clock(1)		600			ns
$t_{SU:STA}$	Setup repeated START(1)		600			ns
$t_{HD:DAT}$	Data hold time (SDA input)(1)		0			ns
$t_{SU:DAT}$	Data setup time (SDA input)(1)		100			ns
t_r	Clock rise time(1)	10% to 90%			300	ns
t_f	Clock fall time(1)	90% to 10%			300	ns
$t_{SU:STO}$	Setup time STOP condition(1)		0.6			µs
t_{BUF}	Bus free time STOP to START(1)		1.3			µs
t_{RST}	I²C bus reset(1)	Bus interface is reset if SCL is detected low for this duration	1.9		2.1	s
R_{PULLUP}	Pullup resistor(1)	Pullup voltage rail ≤ 5 V	1.1			kΩ

(1) Specified by design

6.17 Timing Diagram

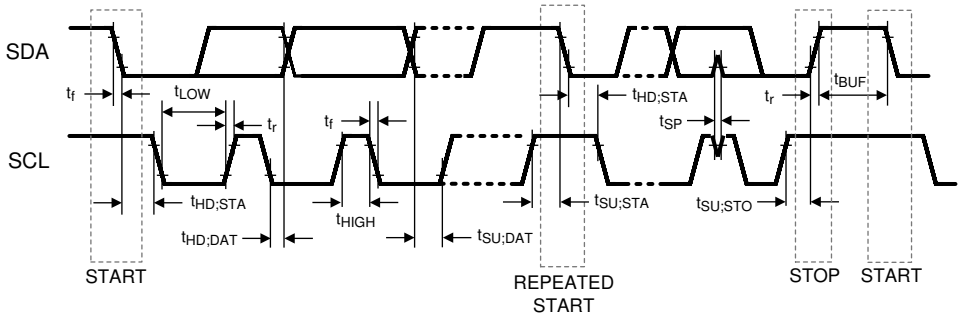


図 6-1. I²C Communications Interface Timing

6.18 Typical Characteristics

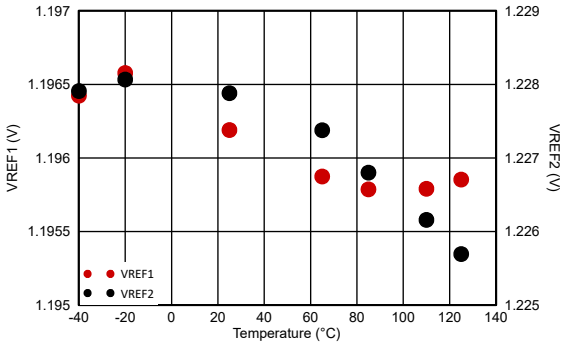


図 6-2. Internal Voltage References vs. Temperature (VREF1 and VREF2)

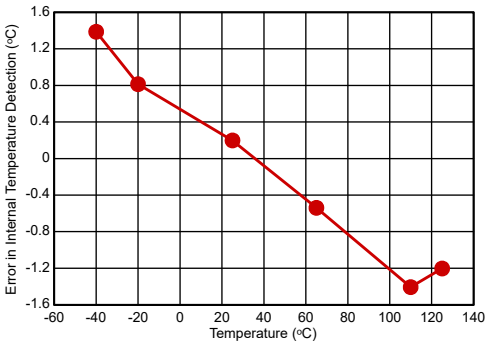


図 6-3. Internal Temperature Protection Error vs. Temperature

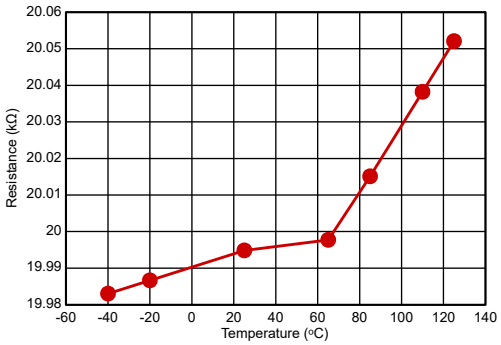


図 6-4. Thermistor Pullup Resistance vs. Temperature

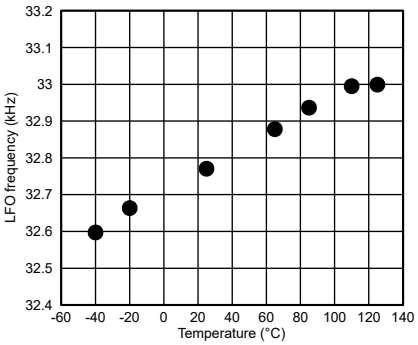


図 6-5. Low Frequency Oscillator (LFO) Accuracy vs. Temperature

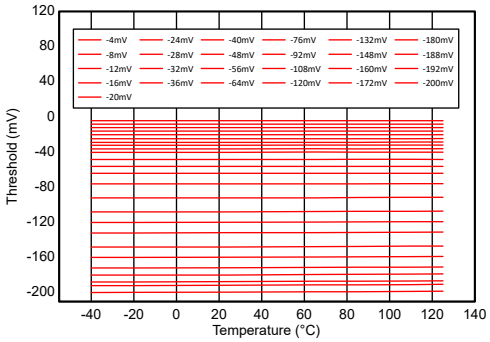


図 6-6. Overcurrent in Discharge Protection 1 (OCD1) Threshold vs. Temperature

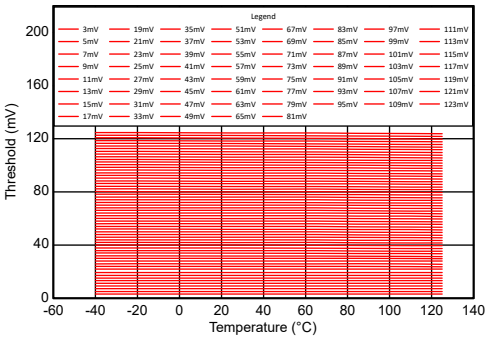


図 6-7. Overcurrent in Charge Protection (OCC) Threshold vs. Temperature

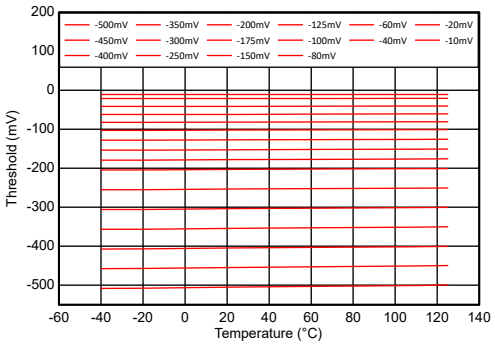


図 6-8. Short Circuit in Discharge Protection (SCD) Threshold vs. Temperature

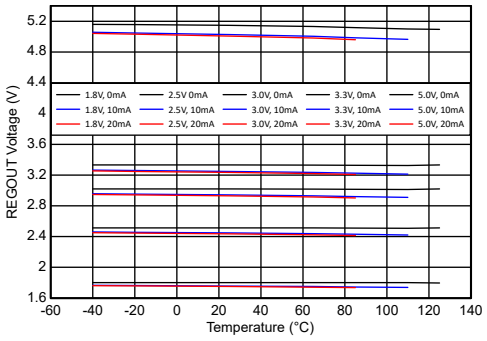


図 6-9. REGOUT Voltage vs. Temperature and Load

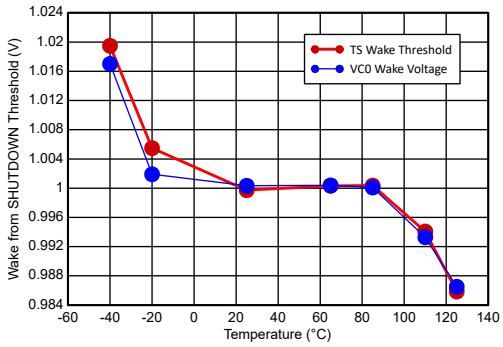
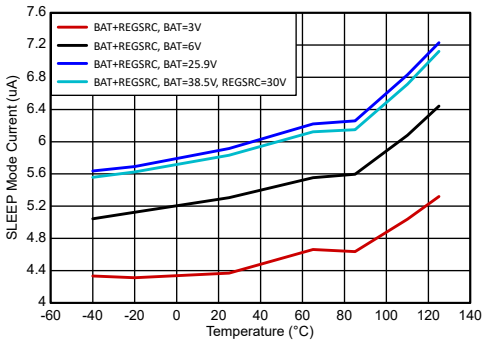


図 6-10. TS and VC0 Wake Voltage vs. Temperature



No communications, REGOUT disabled

図 6-11. Supply Current in NORMAL Mode vs. Temperature

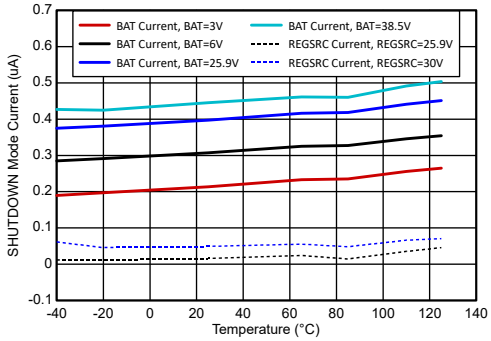


図 6-12. Supply Current in SHUTDOWN Mode vs. Temperature

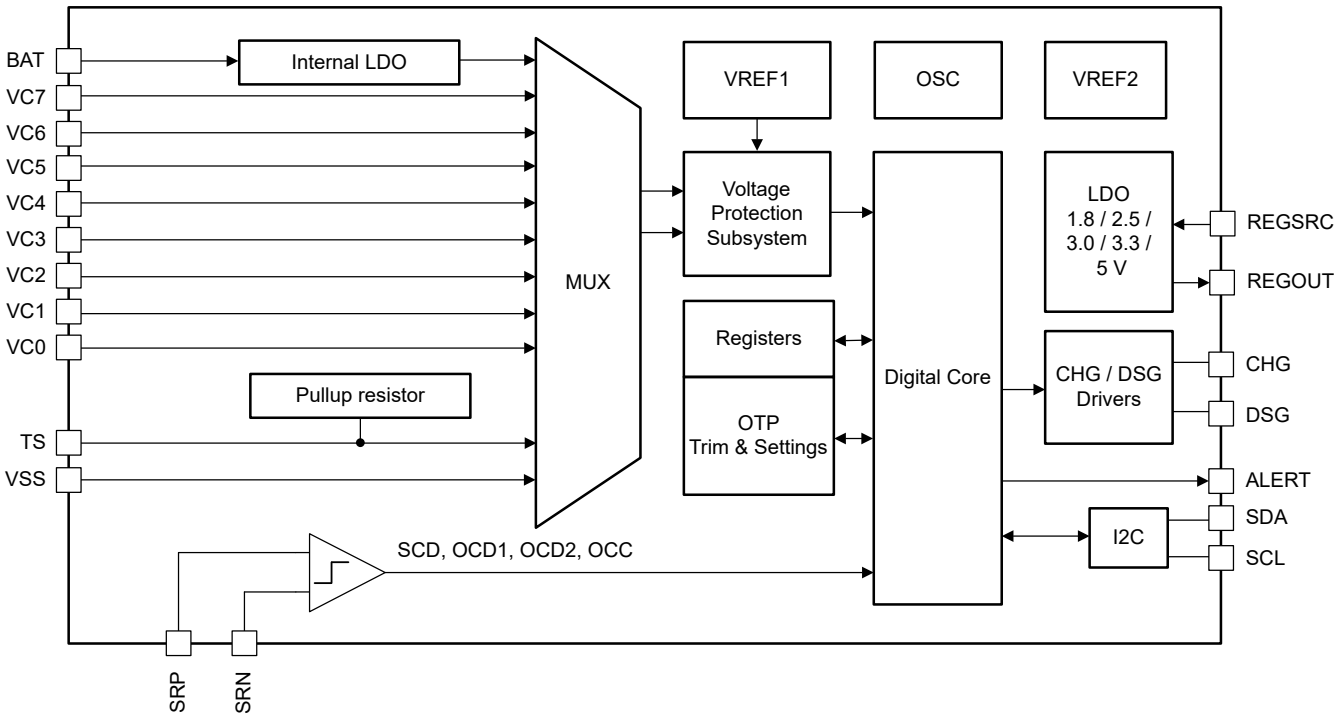
7 Detailed Description

7.1 Overview

The BQ77307 family is a highly integrated, accurate primary or secondary protector for 2-series to 7-series Li-ion, Li-polymer, $LiFePO_4$ (LFP), and LTO battery packs. Each device includes high-accuracy voltage, current, and temperature protections, which can be triggered and recovered completely autonomously by the device or under full control of a host processor. Integrated FET drivers drive low-side charge and discharge protection NFETs. A programmable LDO is included for external system use, with voltage programmable to 1.8 V, 2.5 V, 3.0 V, 3.3 V, or 5.0 V, capable of providing up to 20 mA.

The BQ77307 device includes one-time-programmable (OTP) memory, which TI programs to configure device operation settings. A 400-kHz I^2C communication interface with optional CRC and an ALERT interrupt output enable communication with a host processor to read status information. The device temperature protections include support for an external thermistor, as well as internal die overtemperature protection. The BQ77307 is available in a 20-pin QFN package

7.2 Functional Block Diagram



7.3 Device Configuration

7.3.1 Commands and Subcommands

The BQ77307 device includes support for direct commands and subcommands. The direct commands are accessed using a 7-bit command address sent from a host through the device serial communications interface and either triggers an action, or provides a data value to be written to the device, or instructs the device to report data back to the host. Subcommands are additional commands that are accessed indirectly using the 7-bit command address space and provide the capability for block data transfers. For more information on the commands and subcommands the device supports, refer to *BQ77307 Technical Reference Manual*.

7.3.2 Configuration Using OTP or Registers

The BQ77307 device includes registers with values that are loaded automatically from one-time programmable (OTP) memory. At initial power-up, the device loads OTP settings into registers, which are used by the device

during operation. The OTP settings are programmed into the device by TI during manufacturing. Register values are preserved while the device is in NORMAL mode. If the device enters SHUTDOWN mode, all register memory is cleared, and the device will reload values from OTP when powered again.

7.3.3 Device Security

The BQ77307 device includes two security modes: SEALED and FULLACCESS, which can be used to limit the ability to view or change settings.

- In SEALED mode, most data and status can be read using commands and subcommands, but only selected settings can be changed. Data memory settings cannot be changed directly.
- FULLACCESS mode allows the capability to read and modify all device settings.

Selected settings in the device can be modified while the device is in operation through supported commands and subcommands, but in order to modify all settings, the device must enter CONFIG_UPDATE mode (see CONFIG_UPDATE Mode), which stops device operation while the settings are updated. After the update is completed, the operation is restarted using the new settings. CONFIG_UPDATE mode is only available in FULLACCESS mode.

The BQ77307 device implements a key-access scheme to transition between SEALED and FULLACCESS modes. Changing from SEALED to FULLACCESS requires that a unique set of keys be sent to the device through subcommands. Refer to *BQ77307 Technical Reference Manual* for more details.

7.4 Device Hardware Features

7.4.1 Voltage Protection Subsystem

The BQ77307 device integrates a voltage protection subsystem which is multiplexed between differential cell voltages, an internal temperature sensor, the TS pin, and for diagnostic purposes also evaluates the internal 1.8-V LDO voltage and the VSS rail. The BQ77307 device supports cell voltage protections for individual cells arranged in a series configuration, ranging from 2-series cells to 7-series cells. Each differential cell voltage is evaluated between two adjacent cell input pins, such as VC1-VC0, VC2-VC1, and so on. The cell voltage protections support a recommended differential voltage range from -0.2 V to 5.5 V.

7.4.2 Current Protection Subsystem

The BQ77307 device monitors pack current using a low-side sense resistor that connects to the SRP and SRN pins through an external RC filter, which should be connected such that a charging current will create a positive voltage on SRP relative to SRN. The differential voltage between SRP and SRN is compared to programmable current protection thresholds to generate protection alerts and faults when a threshold is exceeded. The device supports independent thresholds and delay between an alert occurring and a fault being asserted for short circuit in discharge (SCD), overcurrent in discharge 1 and 2 (OCD1, OCD2), and overcurrent in charge (OCC).

7.4.3 Unused VC Pins

If the BQ77307 device is used in a system with fewer than 5 series cells, specific cells must be used for connection to real cells, as shown in 表 7-1. The unused cell inputs should be shorted out on the circuit board. The device only implements protections for those cells designated as real cells.

表 7-1. Cell Usage

NUMBER OF CELL USED	CELL CONNECTIONS	SHORTED CONNECTIONS
7	VC7–VC6, VC6–VC5, VC5–VC4, VC4–VC3, VC3–VC2, VC2–VC1, VC1–VC0	—
6	VC7–VC6, VC6–VC5, VC5–VC4, VC3–VC2, VC2–VC1, VC1–VC0	VC4–VC3
5	VC7–VC6, VC5–VC4, VC3–VC2, VC2–VC1, VC1–VC0	VC6–VC5, VC4–VC3
4	VC7–VC6, VC5–VC4, VC3–VC2, VC1–VC0	VC6–VC5, VC4–VC3, VC2–VC1

表 7-1. Cell Usage (続き)

NUMBER OF CELL USED	CELL CONNECTIONS	SHORTED CONNECTIONS
3	VC7–VC6, VC5–VC4, VC1–VC0	VC6–VC5, VC4–VC3, VC3–VC2, VC2–VC1
2	VC7–VC6, VC1–VC0	VC6–VC5, VC5–VC4,VC4–VC3, VC3–VC2, VC2–VC1

The unused cell input pins should be shorted to adjacent cell input pins, as shown in 図 7-1 for a 6-series system.

It is also important to note that the range of voltages supported by the different VC pins differs depending on the pin. For example, pins VC5, VC6, and VC7 can only support accurate cell voltage protections if their pin voltage is greater than or equal to 2 V. Thus, if implementing a 2-series system using the top and bottom cell input pins, the upper cell voltage may not be evaluated correctly if the lower cell voltage drops below 2 V, since then VC6 would be below 2 V.

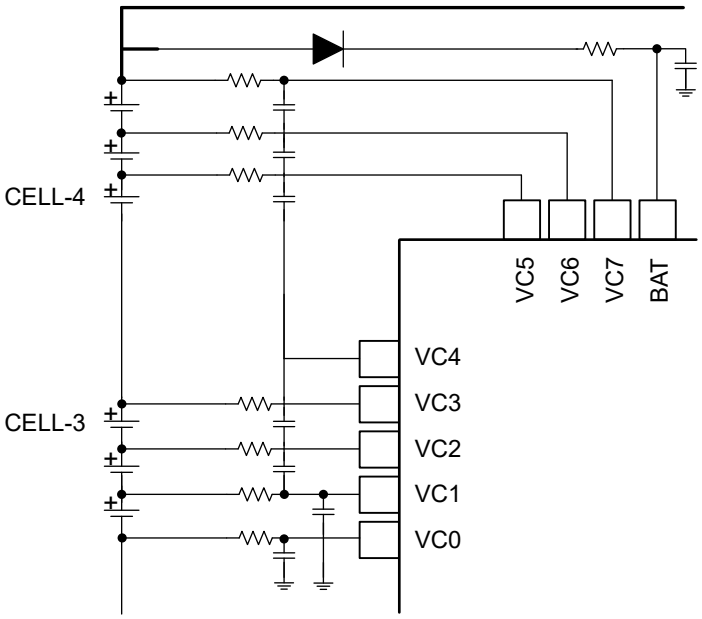


図 7-1. Connecting an Unused Cell Input Pin

The device data memory must be configured to specify which cell inputs are used for actual cells. The device uses this information to disable cell voltage protections associated with inputs that are not used. See the *BQ77307 Technical Reference Manual* for further details.

7.4.4 Internal Temperature Protection

The BQ77307 device integrates the capability to compare its internal die temperature (based on the difference between internal transistor base-emitter voltages) to a programmable threshold to implement a die overtemperature protection. In response to this protection, the device can be configured to disable FETs and optionally enter SHUTDOWN mode. For more information on this, refer to the Internal Overtemperature Protection section in the *BQ77307 Technical Reference Manual*.

7.4.5 Thermistor Temperature Protections

The BQ77307 device supports cell temperature protections using an external thermistor on the TS pin. The device includes an internal 20-kΩ pullup resistor to bias the thermistor during evaluation. In order to provide a high precision evaluation, the device uses the same 1.8-V internal LDO voltage for the evaluation circuitry as is used for biasing the thermistor pullup resistor, thereby implementing a ratiometric operation. Because the pullup

resistor is only enabled periodically, it is recommended to limit the capacitance at this node to below 4 nF to reduce the effect of incomplete settling when the pullup resistor is biased.

7.4.6 Protection FET Drivers

The BQ77307 integrates low-side CHG and DSG FET drivers, which can directly drive low-side protection NFET transistors. The device supports both series and parallel FET configurations, providing FET body diode protection when configured for a series FET configuration, if one FET driver is on, and the other FET driver is off. When body diode protection is enabled, the DSG driver may be turned on to prevent FET damage if the battery pack is charging while a discharge inhibit fault condition is present. Similarly, the CHG driver may be turned on if the pack is discharging while a charge inhibit fault condition is present. These decisions depend on detection of a current with absolute value in excess of the programmable body diode threshold.

The DSG pin is driven high when not blocked by command and when no related faults (such as UV, OTD, UTD, OCD1, OCD2, SCD, and select diagnostics) which are configured for autonomous control are present, or for body diode protection. The driver can be forced on by command, but the command will only take effect if configuration settings allow.

The DSG driver is designed to allow users to select an optimal resistance in series between the DSG pin and the DSG FET gate to achieve the desired FET rise and fall time per the application requirement and the choice of FET characteristics. When the DSG FET is turned off, the DSG pin drives low, and all overcurrent in discharge protections (OCD1, OCD2, SCD) are disabled to better conserve power. These resume operation when the DSG FET is turned on. Device configuration settings determine which protection will autonomously control the appropriate FET driver.

The CHG pin is driven high only when not blocked by a command and when no related faults (OV, OTC, UTC, OCC, SCD, and select diagnostics) that are configured for autonomous control are present, or for body diode protection. The driver can be forced on by a command, but the command will only take effect if configuration settings allow. Turning off the CHG pin has no influence on the overcurrent protection circuitry. The CHG FET driver actively drives the CHG pin high when enabled, and actively drives the pin low to approximately 0.5 V above the VSS voltage for about 100 µs when disabled, then allows the pin to settle to the PACK- voltage through the external CHG FET gate-source resistor. If a charger is attached to the pack while the CHG FET is disabled, the CHG pin can fall to a voltage as low as 25 V below the device VSS, per the device's electrical specifications. Due to the 100 µs time interval during which CHG is actively pulled low, the time constant of the CHG drive circuit (made up of the driver effective resistance, any series resistance between the CHG pin and the CHG FET gate, and the FET gate capacitance) should be kept well below this level.

7.4.7 Voltage References

The BQ77307 device includes two voltage references, VREF1 and VREF2, with VREF1 used by the voltage protection subsystem, which includes protections for cell overvoltage and undervoltage, temperature protections, and the VREF and VSS diagnostics. VREF2 is used by the current protection subsystem, the integrated LDOs, and the internal oscillator. The device includes a diagnostic check of VREF1 vs VREF2, such that if the ratio of the two voltages changes beyond an allowed range, a diagnostic alert or fault is triggered (if enabled by settings).

7.4.8 Multiplexer

The multiplexer connects various signals to the voltage protection subsystem, including the individual differential cell voltage pins, the on-chip temperature sensor, the biased thermistor pin, the internal 1.8 V LDO voltage, and the VSS pin voltage. The multiplexer input circuitry is customized to support the range and level of voltage required for each particular input.

7.4.9 LDOs

The BQ77307 contains an integrated 1.8-V LDO (REG18) that provides a regulated 1.8-V supply voltage for the device's internal circuitry and digital logic. The supply current for this LDO is drawn from the BAT pin.

The device also integrates a programmable LDO (REGOUT) for external circuitry, such as a host processor or external transceiver circuitry. The REGOUT LDO takes its input from the REGSRC pin, which is generally expected to be connected to the top-of-stack, or the REGSRC voltage can be generated by a separate DC/DC converter in the system. The REGOUT LDO can provide an output current of up to 20 mA if thermal conditions permit.

The REGOUT LDO can be programmed to either remain disabled or power up automatically whenever the device exits SHUTDOWN mode, depending on OTP configuration. The LDO output voltage can be programmed to 1.8 V, 2.5 V, 3.0 V, 3.3 V, or 5.0 V by modifying configuration settings. When the REGOUT LDO is disabled and the device is in NORMAL mode, its output is pulled to VSS with an internal resistance of approximately 2.5 kΩ. If the LDO is configured based on OTP settings to be powered, then at each later power-up the device will autonomously load the OTP settings and enable the LDO as configured, without requiring communications first.

The BQ77307 is designed to operate properly with a die temperature up to 110°C, therefore the system design must avoid drawing excessive current from the REGOUT LDO if it could result in the die temperature exceeding this level. For example, with a stack voltage of 22.5 V, and REGOUT programmed to an output voltage of 2.5 V, the device will dissipate approximately 400 mW when supplying 20 mA of load current. The package thermal impedance can be used to calculate the resulting die temperature based on the maximum ambient temperature expected. If this exceeds the device's specified temperature range, the load current may need to be limited in the system.

The BQ77307 includes a die temperature monitor which detects if the die temperature exceeds approximately 120°C. If this occurs, the REGOUT LDO is disabled, and depending on the configuration setting, the device will also enter SHUTDOWN mode. If the REGOUT LDO is disabled due to overtemperature (but the device is not shut down) and the die temperature reduces below the threshold, the REGOUT LDO will automatically power on again.

7.4.10 Standalone Versus Host Interface

The BQ77307 can be configured to operate in a completely standalone mode, without any host processor in the system, or together with a host processor. If in standalone mode, the device can monitor conditions, control FETs based on threshold settings, and recover FETs when conditions allow, all without requiring any interaction with an external processor. If a host processor is present, the device can still be configured to operate fully autonomously, while the host processor can read status information and exercise control as desired. Alternatively, the device can be configured for manual host control, such that the device can monitor and provide a flag when a protection alert or fault has occurred, but will rely on the host to disable FETs. Using the device in standalone mode requires that all settings are programmed into the OTP by TI. This is only available for cases involving a significant shipment volume. Please contact your TI sales representative for information on this option.

The BQ77307 can also be entirely configured by a host processor writing all settings to the device's internal registers across the serial communications interface, without requiring any OTP programming. Using this approach, settings must be reloaded from the host each time the device is reset or enters SHUTDOWN mode and is restarted.

7.4.11 ALERT Pin Operation

The BQ77307 includes functionality to generate an alarm signal at the ALERT pin, which can be used as an interrupt to a host processor. The ALERT pin is an open-drain pin which will be pulled low by the device whenever an alarm signal is generated. The alarm function includes a programmable mask, to allow the customer to decide which flags or events can trigger an alarm. The selected alarm flags remain latched until the host processor reads their status and clears the triggered alarm bits. The alarm mask can be changed during field operation, to mask or unmask individual flags from generating an alarm signal. The device also provides the unlatched, instantaneous value of each flag, in addition to the latched version. See the *BQ77307 Technical Reference Manual* for more details on this function.

7.4.12 Low Frequency Oscillator

The low frequency oscillator (LFO) in the BQ77307 operates continuously while in NORMAL mode. The LFO runs at approximately 32.768 kHz in NORMAL mode. The LFO is trimmed during manufacturing to meet the specified accuracy across temperatures.

7.4.13 I²C Serial Communications Interface

The I²C serial communications interface in the BQ77307 device acts as a target device and supports rates up to 400 kHz with an optional CRC check. The BQ77307 will initially power up by default in a mode determined by the OTP settings factory programmed by TI. The host can change the CRC mode setting while in CONFIG_UPDATE mode, then the new setting will take effect upon exit of CONFIG_UPDATE mode.

The I²C device address (as an 8-bit value including target address and R/W bit) is set by default as 0x10 (write), 0x11 (read), which can also be changed by the configuration setting.

The communications interface includes programmable timeout capability, with the internal I²C bus logic reset when an enabled timeout occurs. This is described in detail in the *BQ77307 Technical Reference Manual*.

An I²C write transaction is shown in 図 7-2. Block writes are allowed by sending additional data bytes before the Stop. The I²C logic will auto-increment the register address after each data byte. The shaded regions show when the device may be clock stretching.

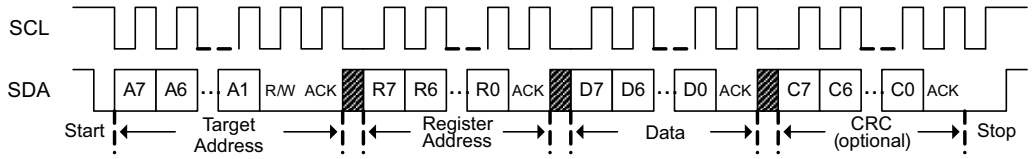


図 7-2. I²C Write

The CRC check is enabled by setting a data memory bit. When enabled, the CRC is calculated as follows:

- Note that the CRC is reset after each data byte and after each stop.
- In a single-byte write transaction, the CRC is calculated over the target address, register address, and data.
- In a block write transaction, the CRC for the first data byte is calculated over the target address, register address, and data. The CRC for subsequent data bytes is calculated over the data byte only.

The CRC polynomial is $x^8 + x^2 + x + 1$, and the initial value is 0.

When the target detects an invalid CRC, the I²C target will NACK the CRC, which causes the I²C target to go to an idle state.

図 7-3 shows a read transaction using a Repeated Start. The shaded regions show when the device may be clock stretching.

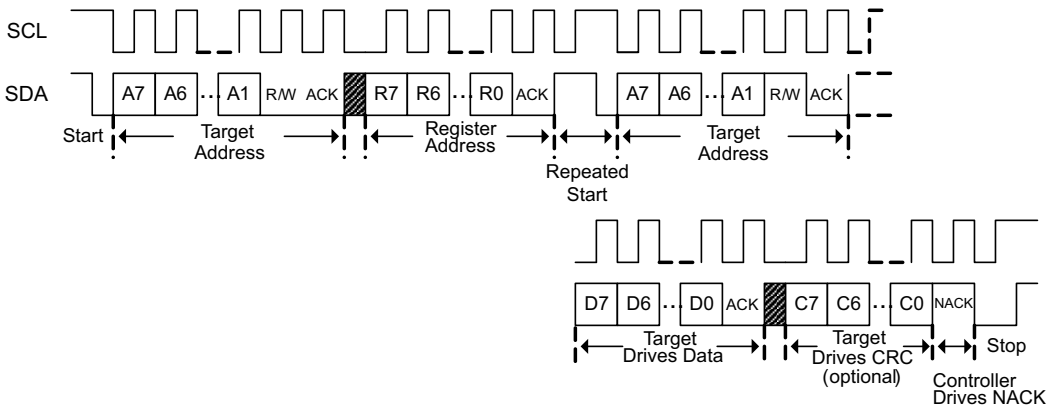


図 7-3. I²C Read with Repeated Start

図 7-4 shows a read transaction where a Repeated Start is not used, for example if not available in hardware. For a block read, the controller ACK's each data byte except the last and continues to clock the interface. The I²C block will auto-increment the register address after each data byte. The shaded regions show when the device may be clock stretching.

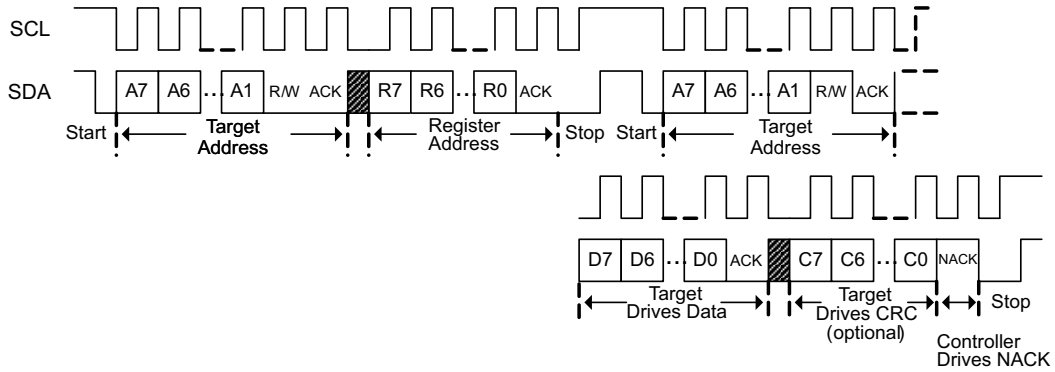


図 7-4. I²C Read Without Repeated Start

When enabled, the CRC for a read transaction is calculated as follows:

- Note that the CRC is reset after each data byte and after each stop.
- In a single-byte read transaction using a repeated start, the CRC is calculated beginning at the first start, so will include the target address, the register address, then the target address with read bit set, then the data byte.
- In a single-byte read transaction using a stop after the initial register address, the CRC is reset after the stop, so will only include the target address with read bit set and the data byte.
- In a block read transaction using repeated starts, the CRC for the first data byte is calculated beginning at the first start and will include the target address, the register address, then the target address with read bit set, then the data byte. The CRC for subsequent data bytes is calculated over the data byte only.
- In a block read transaction using a stop after the initial register address, the CRC is reset after the stop, so will only include the target address with read bit set and the first data byte. The CRC for subsequent data bytes is calculated over the data byte only.

The CRC polynomial is $x^8 + x^2 + x + 1$, and the initial value is 0.

When the controller detects an invalid CRC, the I²C controller will NACK the CRC, which causes the I²C target to go to an idle state.

For more information, see the *BQ77307 Technical Reference Manual*.

7.5 Protection Subsystem

7.5.1 Protections Overview

The BQ77307 integrates an extensive primary protection subsystem which can monitor a variety of parameters, initiate protective actions, and autonomously recover based on conditions. The device also includes a wide range of flexibility, such that the device can be configured to monitor and initiate protective action, but with recovery controlled by the host processor, or such that the device only monitors and alerts the host processor whenever conditions warrant protective action, but with action and recovery fully controlled by the host processor.

The protection subsystem includes a suite of individual protections which can be individually enabled and configured, including cell undervoltage and overvoltage, overcurrent in charge, two separate overcurrent in discharge protections, short circuit current in discharge, cell overtemperature and undertemperature in charge and discharge, internal die overtemperature, and a host processor communication watchdog timeout (for systems that expect a host processor to remain active). The device integrates NFET drivers for low-side CHG

and DSG protection FETs, which can be configured in a series or parallel configuration, and provides body diode protection when in series configuration.

7.5.2 Primary Protections

The BQ77307 integrates a broad suite of protections for battery management and provides the capability to enable individual protections, as well as to select which protections will result in autonomous control of the FETs. See the *BQ77307 Technical Reference Manual* for detailed descriptions of each protection function. The primary protection features include:

- Cell Undervoltage Protection
- Cell Overvoltage Protection
- Cell Open Wire Protection
- Overcurrent in Charge Protection
- Overcurrent in Discharge Protection (two tiers)
- Short Circuit in Discharge Protection
- Current Protection Latch
- Undertemperature in Charge Protection
- Undertemperature in Discharge Protection
- Overtemperature in Charge Protection
- Overtemperature in Discharge Protection
- Internal Overtemperature Protection
- Host Watchdog Fault Protection

The device also includes additional diagnostic checks that can also result in autonomous control of the FETs, depending on configuration settings.

7.5.3 Cell Open Wire Protection

The BQ77307 device supports detection of a broken connection between a cell in the pack and the cell attachment to the PCB containing the BQ77307 device. Without this check, the voltage at the cell input pin of the BQ77307 device may persist for some time on the board-level capacitor, leading to incorrect voltage readings. The Cell Open Wire detection in the BQ77307 device operates by enabling a small current source from each cell to VSS at programmable intervals. If a cell input pin is floating due to an open wire condition, this current discharges the capacitance, causing the voltage at the pin to slowly drop. This drop in voltage eventually triggers a protection fault on that particular cell and the cell above it.

The Cell Open Wire current will be enabled at a periodic interval set by configuration register. This provides programmability in the average current drawn from ≈10 pA to ≈10 µA, based on the typical current level of 55 µA. See the *BQ77307 Technical Reference Manual* for more details.

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The Cell Open Wire check can create a cell imbalance, so the settings should be selected appropriately.

7.5.4 Diagnostic Checks

The BQ77307 includes several checks for diagnostic purposes. Some of these will trigger a protection fault, but they generally do not include an alert phase with programmable delay period, they will immediately trigger a fault when they are detected. They are not all autonomously recoverable, but some can be manually recovered using a subcommand sent by the host. For more detail on each diagnostic, see the *BQ77307 Technical Reference Manual*.

VREF1 vs VREF2 Check—The device performs a regular comparison of the ratio between the two internal voltage references and can trigger a fault if the result is outside an acceptable range.

VSS Check—The device also includes a regular check of the VSS voltage, comparing the result to the expected result, in order to implement the VSSF Diagnostic Protection.

REGOUT Check—The REGOUT LDO generates a flag if an error is detected, such as the regulator is in short circuit current limit. When detected, the device triggers the REGOUT Diagnostic Fault and can disable FETs based on settings.

LFO Integrity Check—The device integrates a special hardware block that monitors if the LFO stops oscillating or drops significantly in frequency versus its expected value. If this is detected, the device immediately transitions into SHUTDOWN mode.

Internal Factory Trim Check—The device includes a check of the digital trim and setting information within the device at initial power-up or after any full reset. If an error is detected during this check, the device will immediately transition to SHUTDOWN mode.

Hardware Overtemperature Detector—The device integrates a hardware overtemperature detection circuit, which determines when the die temperature passes an excessive temperature of approximately 120°C. If this detector triggers, the device will automatically begin the sequence to enter SHUTDOWN, based on the configuration setting.

7.6 Device Power Modes

7.6.1 Overview of Power Modes

The BQ77307 device supports a normal operating mode as well as a full shutdown mode, with the device able to transition from NORMAL mode to SHUTDOWN mode autonomously, based on settings.

- NORMAL mode: In this mode, the device evaluates system current, cell voltages, internal and thermistor temperature, and various diagnostic checks, operates protections as configured, and provides interrupt and status updates. Battery protections are enabled, and the FET drivers are typically enabled (in the absence of any protection fault).
- SHUTDOWN mode: The device is completely disabled (including the internal 1.8 V and REGOUT LDOs), the CHG and DSG FETs are both disabled, and all battery protections are disabled. This is the lowest power state of the device, which may be used for shipment or long-term storage. All register settings that were not written into OTP by TI are lost when in SHUTDOWN mode.

The device also includes a CONFIG_UPDATE mode, which is used for parameter updates. Transitioning between operational modes is shown in BQ77307 Power Modes.

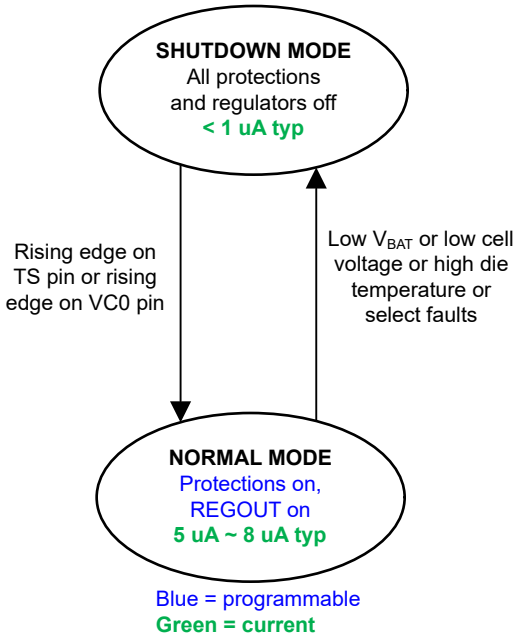

図 7-5. BQ77307 Power Modes

7.6.2 NORMAL Mode

When in NORMAL mode, the BQ77307 continuously evaluates cell voltage, pack current, and thermistor and internal die temperature, implementing all enabled battery protections, and controlling FET drivers based on programmed settings.

The device will remain in this mode continuously, unless it autonomously enters SHUTDOWN mode if the stack voltage or the minimum cell voltage drops below programmable thresholds, or the TS pin thermistor temperature is detected above a programmable threshold, or an excessive die temperature is detected.

7.6.3 SHUTDOWN Mode

SHUTDOWN mode is the lowest power mode of the BQ77307, which can be used for shipping or long-term storage. In this mode, the device loses all register state information, the internal logic is powered down, and the protection FETs are all disabled, so no voltage is provided at the battery pack terminals. All protections are disabled, and no communications are supported. When the device exits SHUTDOWN, the BQ77307 reads parameters stored in OTP (which is programmed by TI), which effectively sets the default values for settings. After device power-up, settings can then be changed by the host writing device registers, if the device has not been SEALED by default.

The device can be configured to enter SHUTDOWN mode automatically based on the minimum top-of-stack voltage, the minimum cell voltage, the maximum TS thermistor temperature, or an excessive die temperature. The shutdown based on cell voltage does not apply to cell input pins not used for actual cells.

When the device is wakened from SHUTDOWN, it requires approximately 10 ms for the internal circuitry to power up, load settings from OTP memory, perform an initial evaluation of conditions relative to enabled protections, and then enable FETs if conditions and settings allow.

The BQ77307 integrates a hardware overtemperature detection circuit, which determines when the die temperature passes an excessive temperature of approximately 120°C. If this detector triggers, the device automatically begins the sequence to enter SHUTDOWN, based on the configuration setting.

The BQ77307 wakes from SHUTDOWN if a voltage is applied at the TS or VC0 pins above a level of approximately 1.2 V. If the shutdown sequence has been initiated, but the device detects the wakeup criteria (either the TS or VCO pin voltage detected high) is present, then the device stays in a "soft shutdown" state until the wakeup criteria is removed (meaning both the TS and VCO pin voltages must be detected low). While

in "soft shutdown," FETs and protections are disabled. The device exits "soft shutdown" when conditions allow the device to continue into SHUTDOWN mode. The host can stop the entry into SHUTDOWN mode with a command, and the device restarts operation with a full reset.

7.6.4 CONFIG_UPDATE Mode

The BQ77307 uses a special CONFIG_UPDATE mode to make changes to the data memory settings, if the device has not been SEALED by default by TI programming. If changes were made to the data memory settings while the normal protection functions were in operation, it could result in unexpected operation or consequences if settings used by the logic changed in the midst of operation. Changes to the data memory settings should generally only be done on the customer manufacturing line or in an offline condition, such as immediately after being powered from SHUTDOWN.

When in CONFIG_UPDATE mode, the device stops all protection monitoring. The host can then make changes to data memory settings. After changes are complete, the host then sends the command to exit CONFIG_UPDATE mode, at which point the device restarts normal operation using the new data memory settings. For more information, see the *BQ77307 Technical Reference Manual*.

8 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The BQ77307 device can be used with 2-series to 7-series battery packs, supporting a top-of-stack voltage ranging from 3 V up to 38.5 V. To design and implement a comprehensive set of parameters for a specific battery pack, during development customers can use the Battery Management Studio (bqStudio), which is a graphical user-interface tool installed on a PC. Using bqStudio, the device can be configured for specific application requirements during development once the system parameters, such as fault trigger thresholds for protection, enable or disable of certain features for operation, configuration of cells, and more are known. This results in a "golden image" of settings that can then be programmed into the device registers, or can be programmed into the device by TI.

8.2 Typical Application

A simplified application schematic for a 7-series battery pack is shown in BQ77307 7-Series Cell Typical Implementation (Simplified Schematic), using the BQ77307 as a primary protector together with a host microcontroller and a communications transceiver. This configuration uses low-side CHG and DSG FETs in series. Several points to consider in an implementation are included below:

- A series diode is recommended at the BAT pin, together with a capacitor from the pin to VSS. These components allow the device to continue operating for a short time when a pack short circuit occurs, which may cause the top-of-stack voltage to drop to approximately 0 V. In this case, the diode prevents the BAT pin from being pulled low with the stack, and the device will continue to operate, drawing current from the capacitor. Generally, operation is only required for a short time until the device detects the short circuit event and disables the DSG FET. A Schottky diode can be used if low voltage pack operation is needed, or a conventional diode can be used otherwise.
- The FET CHG and DSG drivers use the REGSRC pin for their supply, so the user may also prefer to include a diode between the top of the stack and the REGSRC pin, similar to that used for the BAT pin. If any resistance (> 1 Ω) is included in series between the top of the stack and the REGSRC pin, it is recommended to include a 1 µF capacitor at the REGSRC pin to VSS. The REGSRC pin can be shorted to the BAT pin and a single diode used, but this may result in the BAT pin voltage dropping more rapidly during a short circuit event due to the increased loading of the REGOUT regulator drawing from the REGSRC pin.
- The recommended minimum voltage on the VC0 to VC4 pins extends down to –0.2 V, while the recommended minimum voltage on the VC5, VC6, and VC7 pins is limited to 2.0 V, relative to VSS. This restriction exists to ensure the specified accuracy of cell voltage protections.
- TI recommends using 100-Ω resistors in series with the SRP and SRN pins, and a 100 nF with optional 100-pF differential filter capacitance between the pins for filtering. The routing of these components, together with the sense resistor, to the pins should be minimized and fully symmetric, with all components recommended to stay on the same side of the PCB with the device. Capacitors connected from the pins to VSS can provide filtering of common mode transients from reaching the pins, but they may also have a slight impact on current protection performance.
- The filter network connected between the sense resistor and the SRP and SRN pins introduces an analog filter delay that can be important when fast current protections are required, such as in determining the short circuit in discharge (SCD) time until FETs are disabled. If the delay introduced by this network is too long, the resistance and capacitance values can be reduced. This will have a tradeoff of providing less analog filtering of high-frequency components.
- Due to thermistors often being attached to cells and possibly needing long wires to connect back to the device, it may be helpful to add a capacitor from the thermistor pin to the device VSS. However, it is important

to not use too large of a value of capacitor, since this will affect the settling time when the thermistor is biased and checked periodically. It is recommended to keep the value of external capacitance below 7.5 nF.

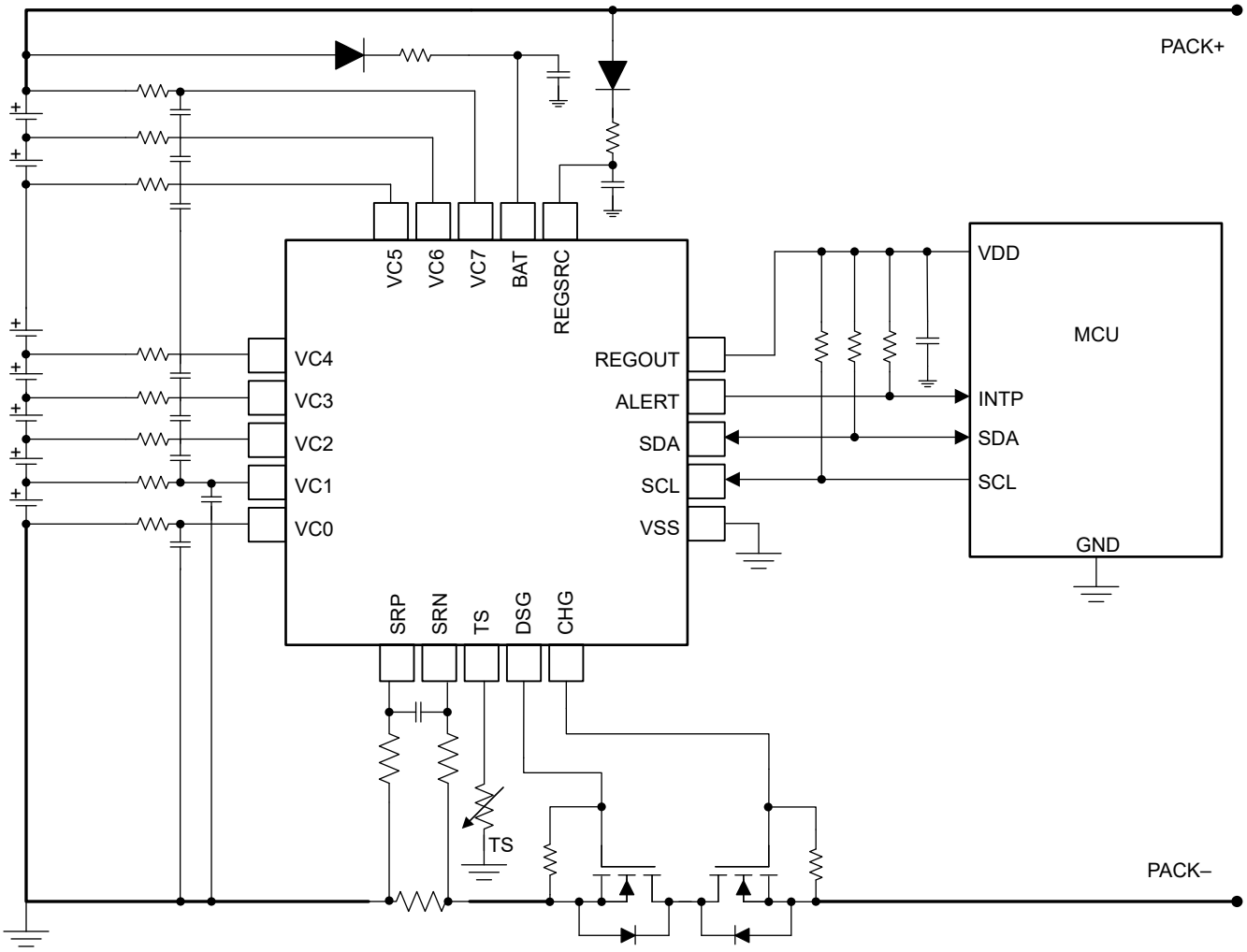

図 8-1. BQ77307 7-Series Cell Typical Implementation (Simplified Schematic)

A full schematic of a basic monitor circuit based on the BQ77307 for a 7-series battery pack is shown below. セクション 10.2 shows the board layout for this design.

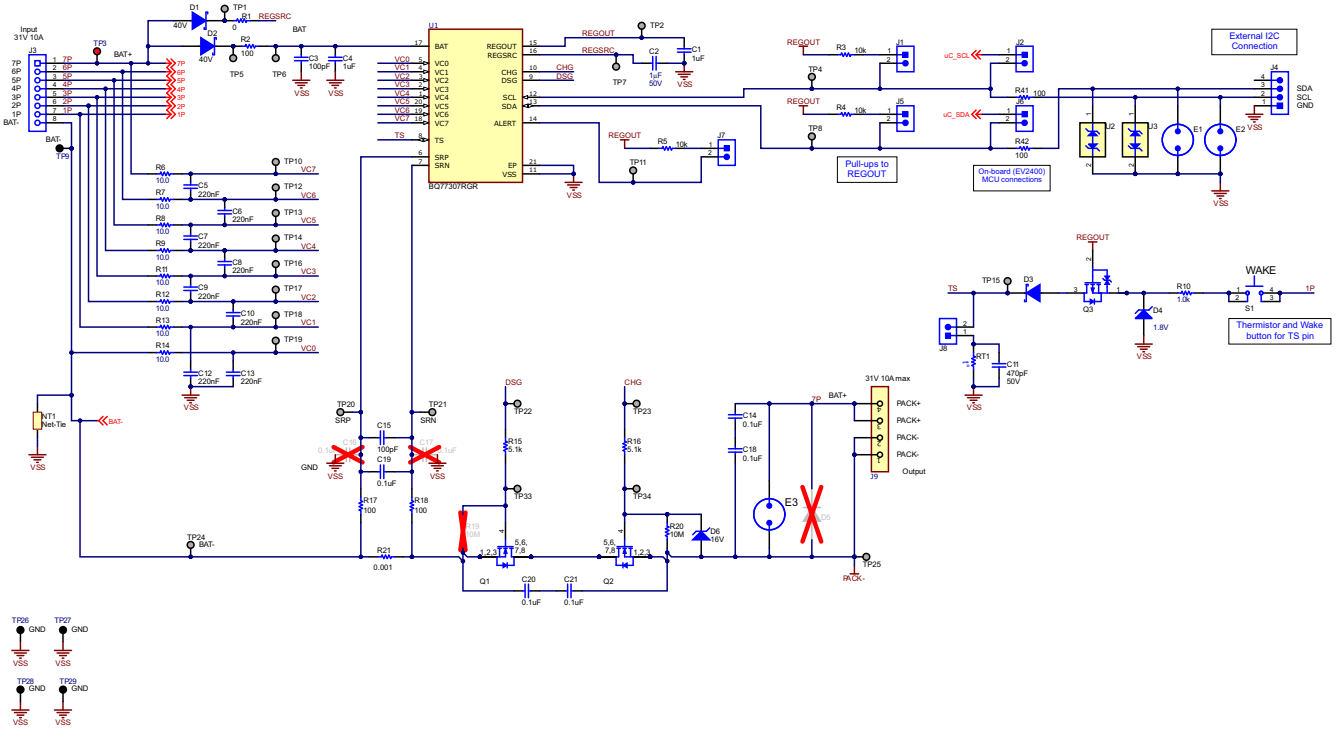

図 8-2. BQ77307 7-Series Cell Schematic Diagram—Monitor

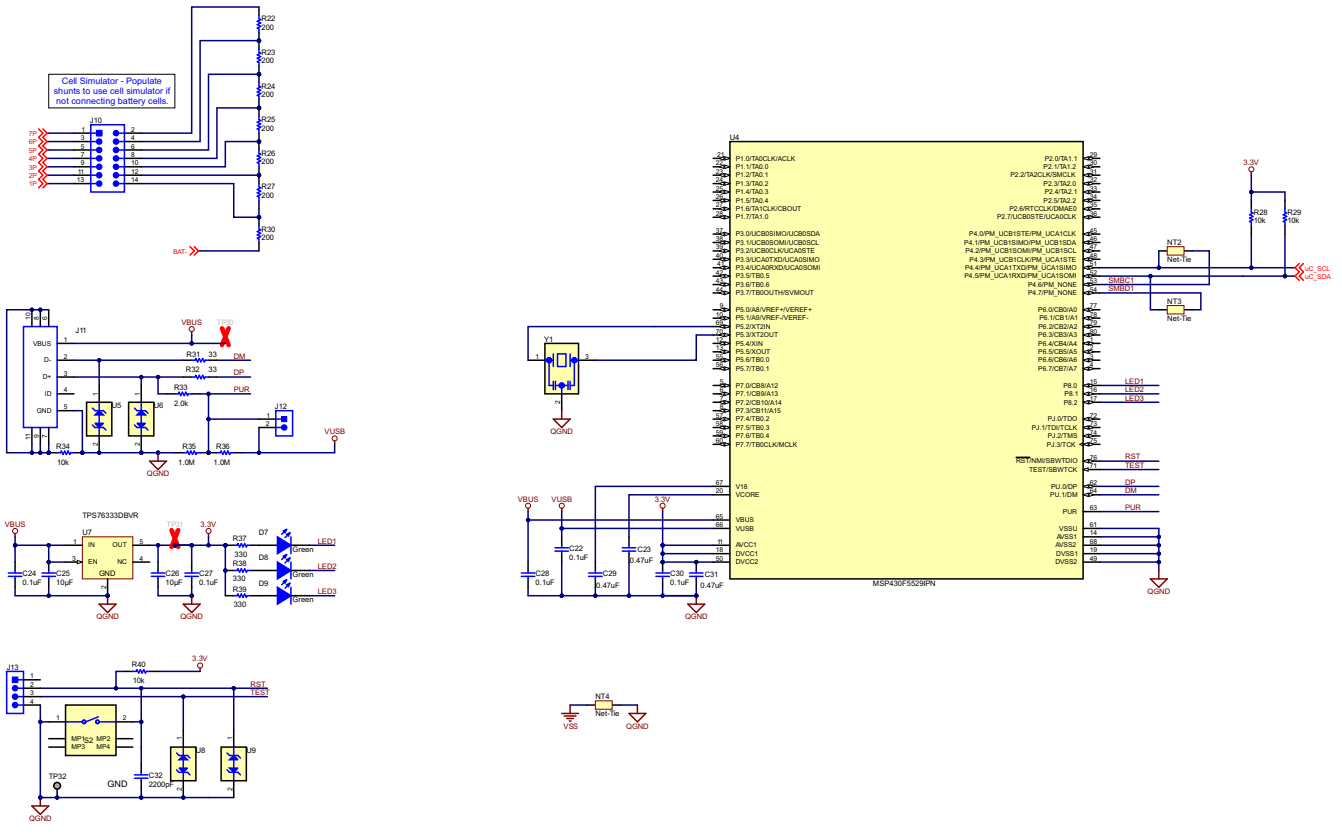

図 8-3. BQ77307 7-Series Cell Schematic Diagram—Additional Circuitry

8.2.1 Design Requirements

表 8-1. BQ77307 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
Minimum system operating voltage	17.5 V
Cell minimum operating voltage	2.5 V
Series cell count	7
Sense resistor	1 mΩ
Thermistor in use	yes
Charge voltage	29.75 V
Maximum charge current	6.0 A
Peak discharge current	40.0 A
Configuration settings	programmed by TI
Protection subsystem configuration	Series FET configuration, device monitors, disables FETs upon fault, recovers autonomously
OV protection threshold	4.30 V
OV protection delay	375 ms
OV protection recovery hysteresis	100 mV
UV protection threshold	2.5 V
UV protection delay	141 ms
UV protection recovery hysteresis	100 mV
SCD protection threshold	80 mV (corresponding to a nominal 80 A, based on a 1-mΩ sense resistor)
SCD protection delay	45 to 60 µs
OCD1 protection threshold	68 mV (corresponding to a nominal 68 A, based on a 1-mΩ sense resistor)
OCD1 protection delay	10 ms
OCD2 protection threshold	56 mV (corresponding to a nominal 56 A, based on a 1-mΩ sense resistor)
OCD2 protection delay	81 ms
OCC protection threshold	8 mV (corresponding to a nominal 8 A, based on a 1-mΩ sense resistor)
OCC protection delay	159.2 ms
OTD protection threshold	Setting = 48 (corresponding to approximately 60°C)
OTD protection delay	2 seconds
OTD protection recovery	Setting = 55 (corresponding to approximately 55°C) for 2 seconds
OTC protection threshold	Setting = 72 (corresponding to approximately 45°C)
OTC protection delay	2 seconds
OTC protection recovery	Setting = 82 (corresponding to approximately 40°C) for 2 seconds
UTD protection threshold	Setting = 197 (corresponding to approximately –20°C)
UTD protection delay	8 seconds
UTD protection recovery	Setting = 174 (corresponding to approximately –10°C) for 2 seconds
UTC protection threshold	Setting = 147 (corresponding to approximately 0°C)
UTC protection delay	5 seconds
UTC protection recovery	Setting = 134 (corresponding to approximately 5°C) for 2 seconds
Host watchdog timeout protection delay	5 seconds
ALERT pin functionality	Used for alarm interrupt function
REGOUT LDO Usage	Enabled with 3.3-V output

8.2.2 Detailed Design Procedure

- Determine the number of series cells.

  - This value depends on the cell chemistry and the load requirements of the system. For example, to support a minimum battery voltage of 12 V using Li-CO_2 type cells with a cell minimum voltage of 3 V, at least 4-series cells are required.
  - For the correct cell connections, see セクション 7.4.3.
- Protection FET selection and configuration
  - The BQ77307 device is designed for use with low-side NFET protection
  - The configuration should be selected for series versus parallel FETs, which may lead to different FET selection for charge versus discharge direction.
  - These FETs should be rated for the maximum:
    - Voltage, which should be approximately 5 V (DC) to 10 V (peak) per series cell.
    - Current, which should be calculated based on both the maximum DC current and the maximum transient current with some margin.
    - Power Dissipation, which can be a factor of the RDS(ON) rating of the FET, the FET package, and the PCB design.
- Sense resistor selection
  - The resistance value should be selected to maximize the input range of the SCD, OCD, and OCC protections but not exceed the absolute maximum ratings, and avoid excessive heat generation within the resistor.
    - Using the normal maximum charge or discharge current, the sense resistor = 200 mV / 40.0 A = 5 mΩ maximum.
    - Considering a short circuit discharge current of 80 A, the recommended maximum SRP, SRN voltage of ≈0.75 V, and the maximum SCD threshold of 500 mV, the sense resistor should be below 500 mV / 80 A= 6.25 mΩ maximum.
  - Further tolerance analysis (value tolerance, temperature variation, and so on) and PCB design margin should also be considered, so a sense resistor of 1 mΩ is suitable with a 50-ppm temperature coefficient and power rating of 1 W.
- The REGOUT is selected to provide the supply for an external host processor and the pullup supply for the I^2C bus and ALERT pin, with output voltage selected for 3.3 V.
  - A 1 µF or larger capacitor should be placed at the REGOUT pin.
  - The REGOUT draws its input current from the REGSRC pin. This pin is connected to PACK+ through a series diode and 10 Ω resistor, with a 1-µF capacitor to VSS placed at the REGSRC pin.

8.2.3 Application Performance Plot

The scope plot example below shows the response of the device to a short circuit in discharge (SCD) event and subsequent protection. The device example is configured with an SCD threshold = 10 mV and SCD delay of 0 µs to 15 µs. A short circuit is applied through a 1-mΩ sense resistor. The input filter network on the SRP and SRN pins consists of 100-Ω resistors and a 100-nF differential capacitor, which results in a 20-µs time constant. The *[SSA]* bit in *AlarmStatus()* causes the ALERT pin to fall, which occurs between approximately 15 µs and 30 µs after the safety status is triggered and the DSG driver is disabled. The circuit includes a 5.1-kΩ resistor between the DSG pin and the DSG FET gate. The load current is shown using the differential voltage at the SRN-SRP pins, which includes an RC delay versus the voltage at the sense resistor

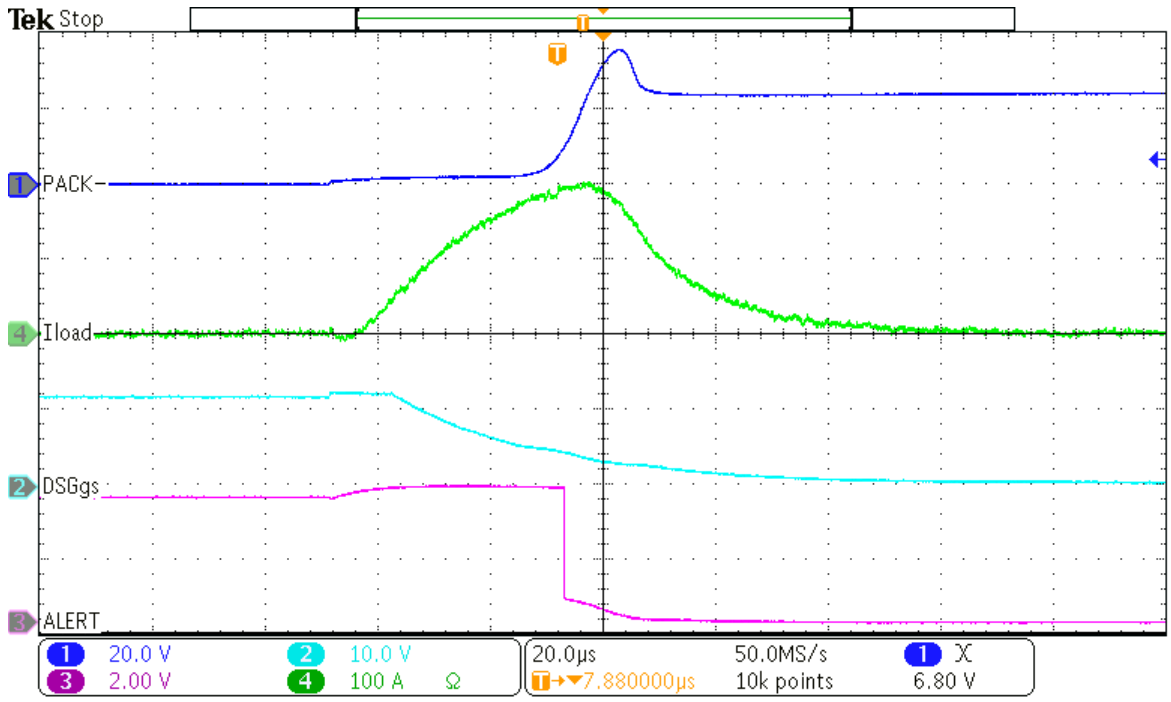

図 8-4. Scope Plot of SCD Event and Protection

8.2.4 Random Cell Connection Support

The BQ77307 device supports a random connection sequence of cells to the device during pack manufacturing. For example, cell-6 in a 7-cell stack might be first connected at the input terminals leading to pins VC6 and VC5, then cell-2 may next be connected at the input terminals leading to pins VC2 and VC1, and so on. It is not necessary to connect the negative terminal of cell-1 first at VC0. As another example, consider a cell stack that is already assembled and cells already interconnected to each other, then the stack is connected to the PCB through a connector, which is plugged or soldered to the PCB. In this case, the sequence order in which the connections are made to the PCB can be random in time, they do not need to be controlled in a certain sequence.

There are some restrictions to how the cells are connected during manufacturing:

- To avoid misunderstanding, note that the cells in a stack cannot be randomly connected to any VC pin on the device, such as the lowest cell (cell-1) connected to VC7, while the top cell (cell-7) is connected to VC2, and so on. It is important that the cells in the stack be connected in ascending pin order, with the lowest cell (cell-1) connected between VC1 and VC0, the next higher voltage cell (cell-2) connected between VC2 and VC1, and so on.
- The random cell connection support is possible due to high voltage tolerance on pins VC1–VC7.

注

VC0 has a lower voltage tolerance. This is because VC0 should be connected through the series-cell input resistor to the VSS pin on the PCB, before any cells are attached to the PCB. Thus, the VC0 pin voltage is expected to remain close to the VSS pin voltage during cell attach. If VC0 is not connected through the series resistor to VSS on the PCB, then cells cannot be connected in random sequence.

- Each of the VC1–VC7 pins includes a diode between the pin and the adjacent lower cell input pin (that is, between VC7 and VC6, between VC6 and VC5, and so on), which is reverse biased in normal operation. This

means an upper cell input pin should not be driven to a low voltage while a lower cell input pin is driven to a higher voltage, since this would forward bias these diodes. During cell attach, the cell input terminals should generally be floating before they are connected to the appropriate cell. It is expected that transient current will flow briefly when each cell is attached, but the cell voltages will quickly stabilize to a state without DC current flowing through the diodes. However, if a large capacitance is included between a cell input pin and another terminal (such as VSS or another cell input pin), the transient current may become excessive and lead to device heating. Therefore, it is recommended to limit capacitances applied at each cell input pin to the values recommended in the specifications.

8.2.5 Startup Timing

At the initial power-up of the BQ77307 device from a SHUTDOWN state, the device progresses through a sequence of events before entering NORMAL mode operation. These events are described below for two example configurations, with approximate timing shown.

表 8-2. Startup Sequence and Timing

STEP	COMMENT	APPROXIMATE TIME (RELATIVE TO WAKEUP EVENT)
Wakeup event	Either the TS pin or the VC0 pin is pulled up, triggering the device to exit SHUTDOWN mode.	0
REGOUT powered	Timing measured with the OTP programmed to autonomously power the REGOUT LDO.	2.6 ms
FETs enabled (7 series)	Timing measured with the OTP programmed to autonomously enable FETs.	9.4 ms
FETs enabled (5 series)	Timing measured with the OTP programmed to autonomously enable FETs.	8.6 ms

8.2.6 FET Driver Turn-Off

The low-side CHG and DSG FET drivers operate differently when they are triggered to turn off their respective FET. The DSG driver includes an internal switch that drives the DSG pin toward the VSS pin level when the driver is disabled. The driver is specified with a maximum fall time into a 20-nF capacitive load, with 100-Ω series resistance between the DSG pin and the DSG gate. If the driver is used with a larger capacitive load, the fall time generally increases. The system designer can optimize the series resistance value based on the board components and DSG FET(s) used.

The external series gate resistor between the DSG pin and the DSG FET gate is used to adjust the speed of the turn-off transient. A low resistance (such as 100 Ω) provides a fast turn-off during a short circuit event, but this may result in an overly large inductive spike at the top of stack when the FET is disabled. A larger resistor value (such as 1 kΩ or 4.7 kΩ) reduces this speed and the corresponding inductive spike level.

The CHG FET driver discharges the CHG pin toward the VSS pin level, but it includes an additional series PFET to support voltages below VSS. This is generally needed when a pack is heavily discharged, for example, if cells in a 7-S pack are at 2.5 V per cell, then PACK+ = 17.5 V relative to device VSS. Then if a charger is attached while the CHG FET is disabled and applies a full charge voltage across PACK+ relative to PACK-, such as 4.3 V per cell, or 30.1 V for the 7-S pack, this results in PACK- dropping to approximately –12.6 V relative to VSS. To keep the CHG FET disabled, its gate voltage must drop to near this –12 V level.

To support this type of case, the CHG FET driver in BQ77307 is designed to withstand voltages as low as –25 V (recommended) relative to the VSS pin voltage by including a series PFET at the pin, with its gate connected to VSS. When the CHG driver is disabled, the driver pulls the pin voltage downward. As the pin voltage nears VSS, the PFET is disabled, so the pin becomes high impedance. At this point, the external gate-source resistor on the CHG FET pulls the pin voltage lower to the PACK– level, keeping the CHG FET disabled.

Oscilloscope captures of the DSG driver turn-off are shown below, with the DSG pin driving the gate of a CSD18532Q5B NFET, which has a typical C_{iss} of 3900 pF. 図 8-5 shows the signals when using a 1.35-kΩ series gate resistor between the DSG pin and the FET gate, and a 2A load connected between PACK+ and PACK–.

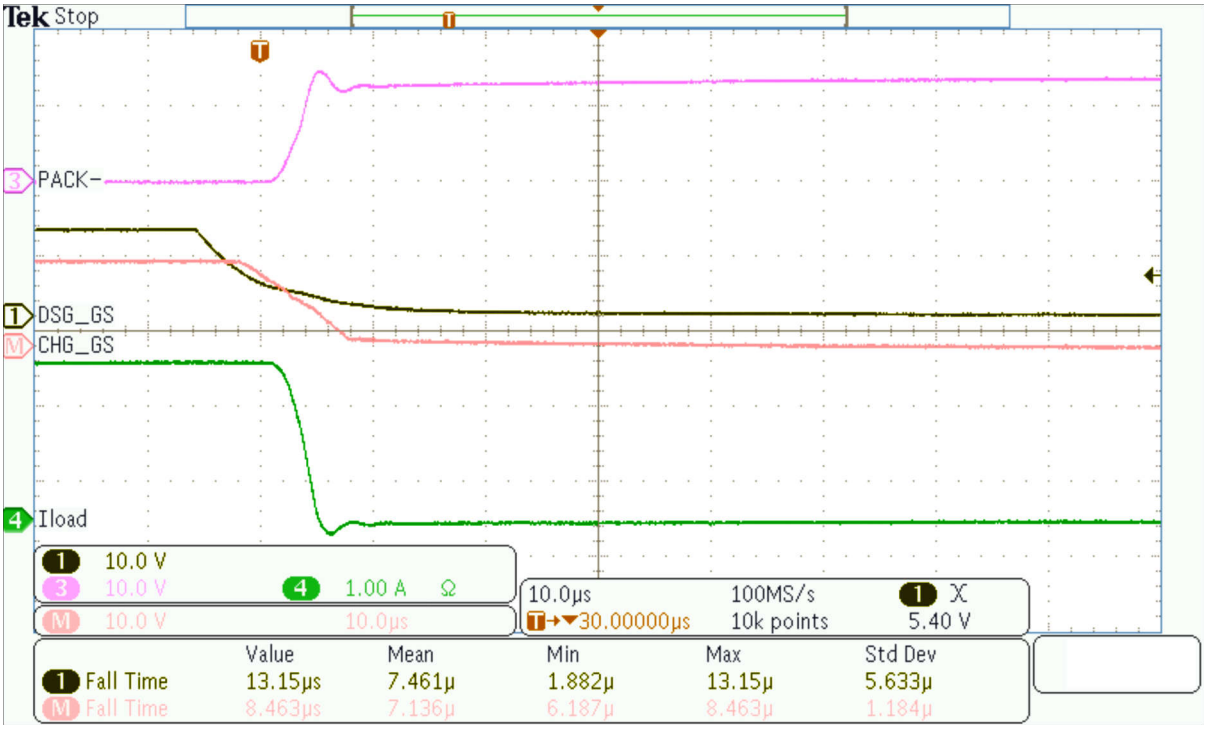

図 8-5. Moderate Speed DSG FET Turn-Off, Using a 1.35-kΩ Series Gate Resistor, and a 2A Load Between PACK+ and PACK–

A slower turn-off case is shown in 図 8-6, using a 4.7-kΩ series gate resistor, and a 2A load between PACK+ and PACK–.

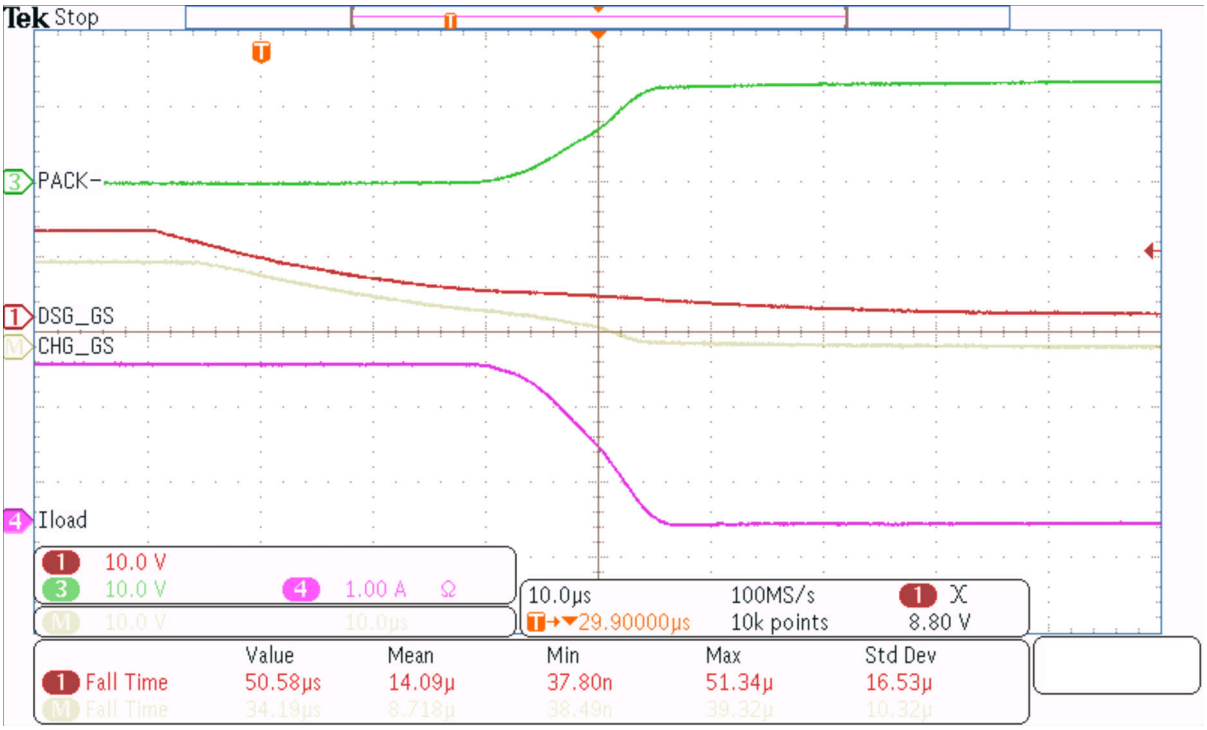

図 8-6. A Slower Turn-Off Case Using a 4.5-kΩ Series Gate Resistor

A fast turn-off case is shown in 図 8-7, in which a 100-Ω series gate resistor is used between the DSG pin and the FET gate.

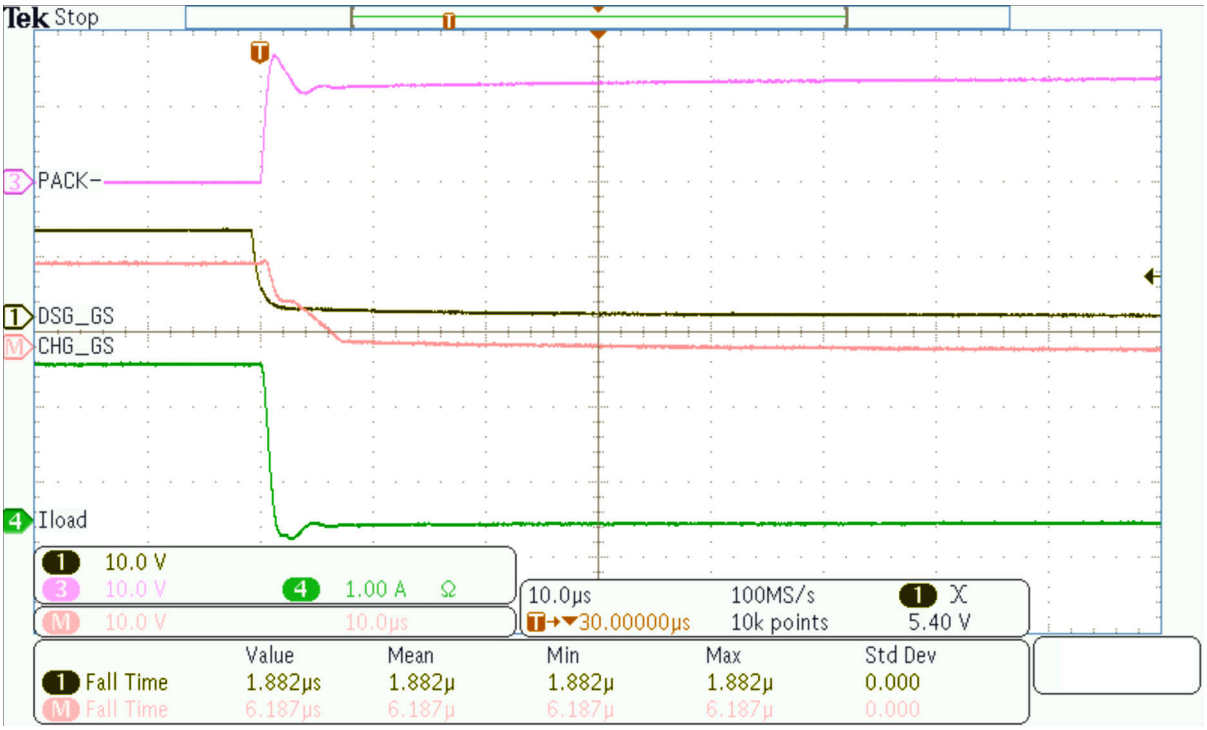

図 8-7. A Fast Turn-Off Case with a 100-Ω Series Gate Resistor

8.2.7 Usage of Unused Pins

Some device pins may not be needed in a particular application. Terminating Unused Pins shows the manner in which each pin is terminated in this case.

表 8-3. Terminating Unused Pins

PIN	NAME	RECOMMENDATION
1–5, 18–20	VC0–VC7	Cell inputs 1 and 7 must always be connected to actual cells, with cells connected between VC1 and VC0, and between VC7 and VC6. VC0 must be connected through a resistor and capacitor on the PCB to pin 11 (VSS). Pins related to unused cells (which may be cell 2 to cell 6, pins 1–3, 20) must be shorted directly to an adjacent VC pin. All VC pins must be connected to either an adjacent VC pin or an actual cell (through R and C).
6, 7	SRP, SRN	If not used, connect these pins to pin 11 (VSS).
8	TS	If not used, connect this pin to pin 11 (VSS).
9, 10	DSG, CHG	If not used, leave these pins floating.
12, 13	SCL, SDA	If not used, connect these pins to pin 11 (VSS).
14, 15	ALERT, REGOUT	If not used, leave these pins floating.
16	REGSRC	If neither the REGOUT regulator nor the CHG and DSG drivers are used, connect this pin to pin 17 (BAT).

9 Power Supply Recommendations

The BQ77307 device draws its supply current from the BAT pin, which is typically connected to the top of stack point through a series diode, to protect against any fault within the device resulting in unintended charging of the pack. A series resistor and capacitor is included to lowpass filter fast variations on the stack voltage. During a short circuit event, the stack voltage may be momentarily pulled to a very low voltage before the protection FETs are disabled. In this case, the charge on the BAT pin capacitor will temporarily support the BQ77307 device's supply current, to avoid the device losing power.

The REGSRC pin serves as the supply voltage for the integrated REGOUT customer regulator and for the CHG and DSG FET drivers. This pin can also be connected to the top of stack through a diode, to similarly allow the voltage to hold up longer during a short circuit event. If a diode or any series resistance (> 1 Ω) is included between the top of stack and the REGSRC pin, a minimum 1-µF capacitor is recommended to be included at the REGSRC pin to VSS. It is also acceptable to short the REGSRC pin to the BAT pin, such that the same diode and filter circuit can support both pins. However, the load on the REGOUT pin will discharge the BAT capacitor faster in this case and should be considered by the system designer.

10 Layout

10.1 Layout Guidelines

- The quality of the Kelvin connections at the sense resistor is critical. The sense resistor should have a temperature coefficient no greater than 50 ppm in order to minimize current detection drift with temperature. Choose the value of the sense resistor to correspond to the available overcurrent and short-circuit ranges of the BQ77307 device. Parallel resistors can be used as long as good Kelvin sensing is ensured.
- In reference to the system circuitry, the following features require attention for component placement and layout: Differential Low-Pass Filter, and I^2C communication.
- For best performance, 100-Ω resistors should be included from the sense resistor terminals to the SRP and SRN inputs of the device, with a 0.1-µF filter capacitor placed across the SRP and SRN pins. Optional 0.1-µF filter capacitors can be added for additional noise filtering at each sense input pin to ground. All filter components should be placed as close as possible to the device, rather than close to the sense resistor, and the traces from the sense resistor routed in parallel to the filter circuit. A ground plane can also be included around the filter network to add additional noise immunity.
- These filter components between the sense resistor and the SRP and SRN terminals provide filtering of noise components, but they also introduce an RC time constant delay, nominally 20 µs using the two 100-Ω and single differential 0.1-µF components. If this delay introduces too much additional time into the response of the device to short circuit events, the filter time constant can be reduced, with the tradeoff of providing less filtering.
- The I^2C clock and data pins have integrated ESD protection circuits; however, adding a Zener diode and series resistor on each pin provides more robust ESD performance.

10.2 Layout Example

An example circuit layout using the BQ77307 device in a 7s-series cell design is described below. The design implements the schematic shown in the BQ77307 7-Series Cell Schematic Diagram—Monitor and BQ77307 7-Series Cell Schematic Diagram—Additional Circuitry and uses a 2.175-inch × 1.400-inch 2-layer circuit card assembly, with cell connections on the left edge, and pack connections along the bottom edge of the board. Wide trace areas are used, reducing voltage drops on the high current paths.

The board layout, which is shown in BQ77307 Two-Layer Board Layout–Top Layer and BQ77307 Two-Layer Board Layout–Bottom Layer, includes spark gaps with the reference designator prefix *E*. These spark gaps are fabricated with the board and no component is installed.

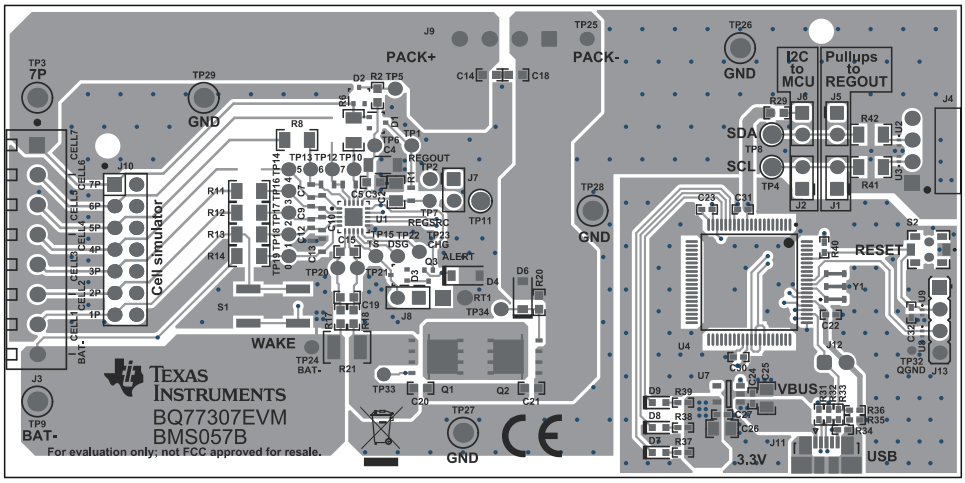

図 10-1. BQ77307 Two-Layer Board Layout–Top Layer

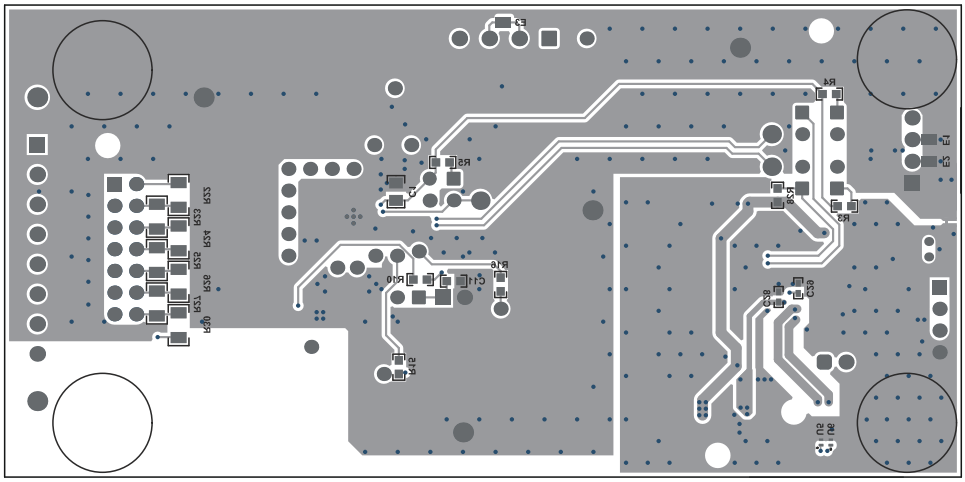

図 10-2. BQ77307 Two-Layer Board Layout–Bottom Layer

11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

11.1 Documentation Support

11.1.1 Related Documentation

For additional information, see the following related documents:

- *BQ77307 Technical Reference Manual*
- *Battery Management Studio (bqStudio) Software*

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 サポート・リソース

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11.6 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

12 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
December 2023	*	Initial Release

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ77307RGRR	Active	Production	VQFN (RGR) | 20	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 110	77307
BQ77307RGRR.A	Active	Production	VQFN (RGR) | 20	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 110	77307

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

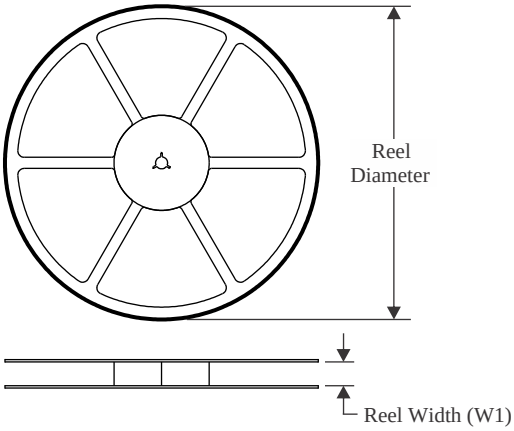
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

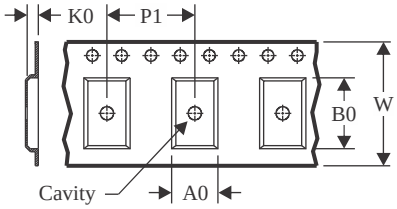
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

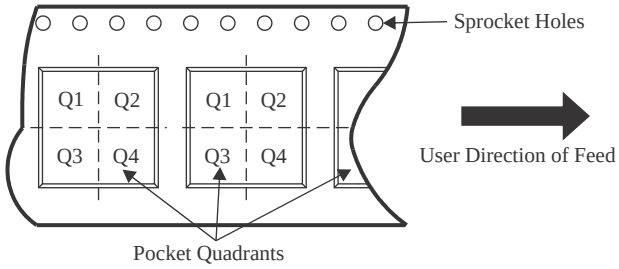


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

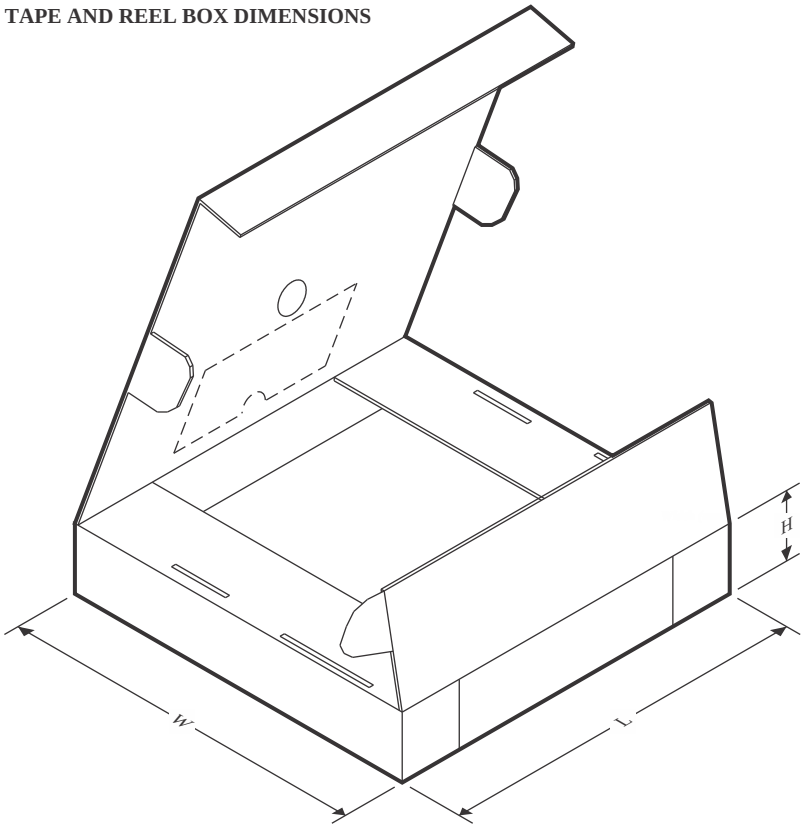
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ77307RGRR	VQFN	RGR	20	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ77307RGRR	VQFN	RGR	20	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

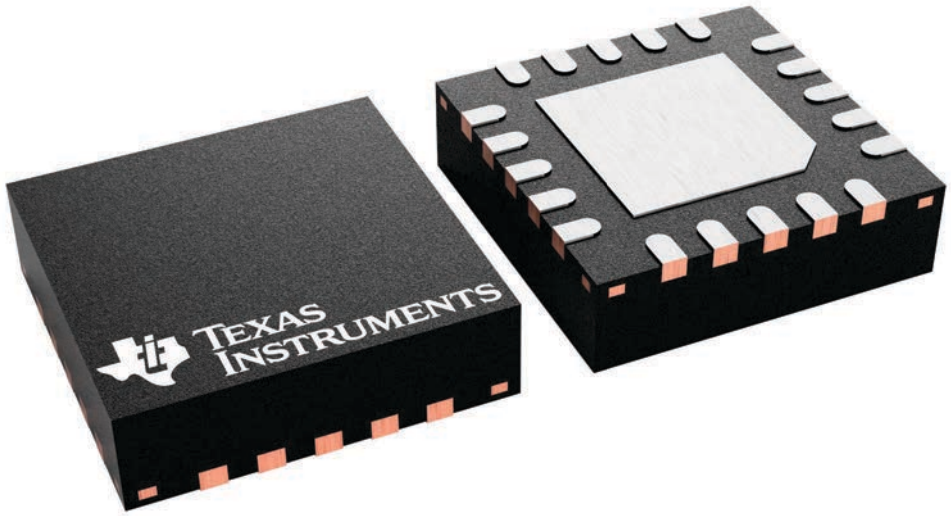
RGR 20

VQFN - 1 mm max height

3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



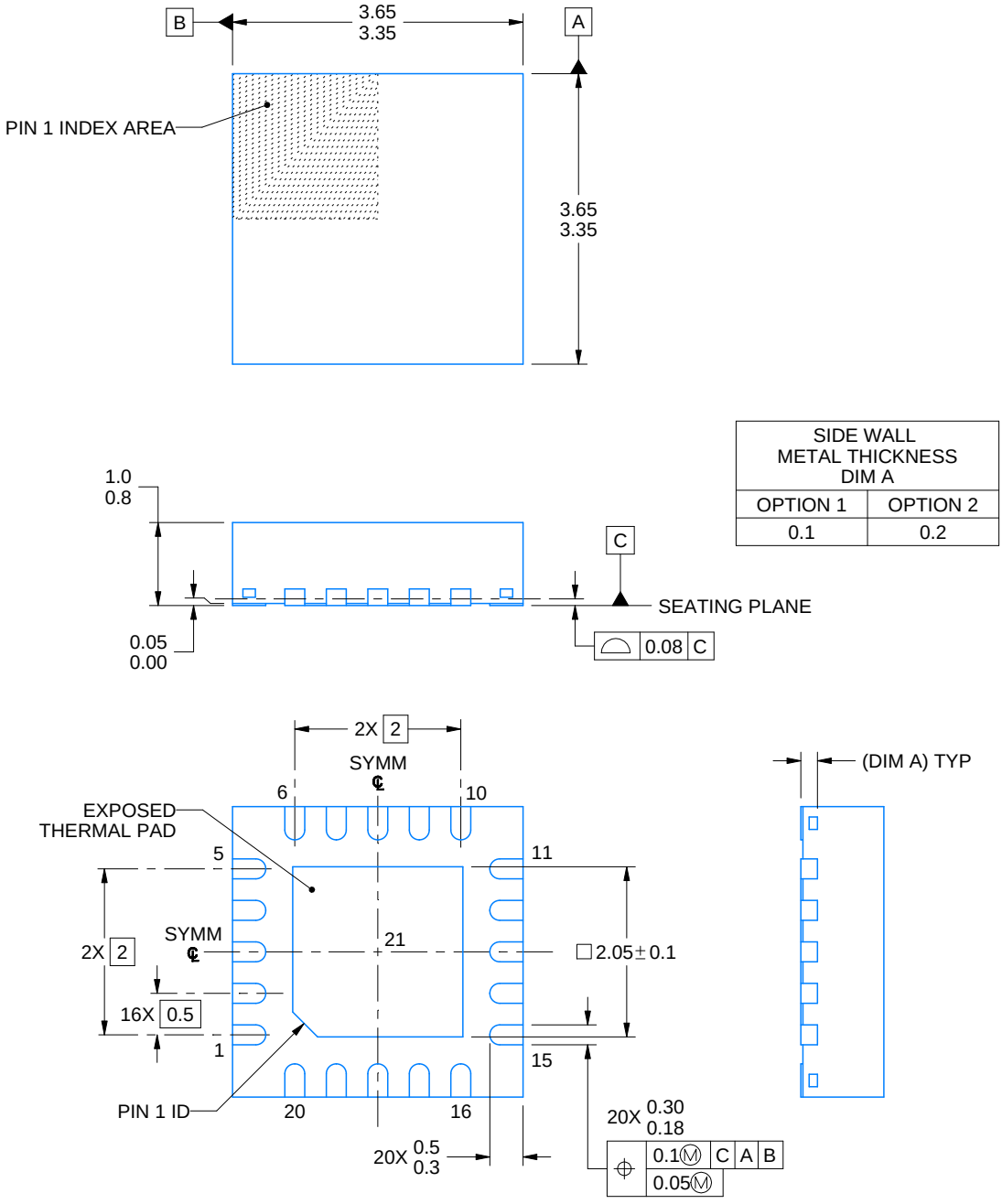
4228482/A

PACKAGE OUTLINE

RGR0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2

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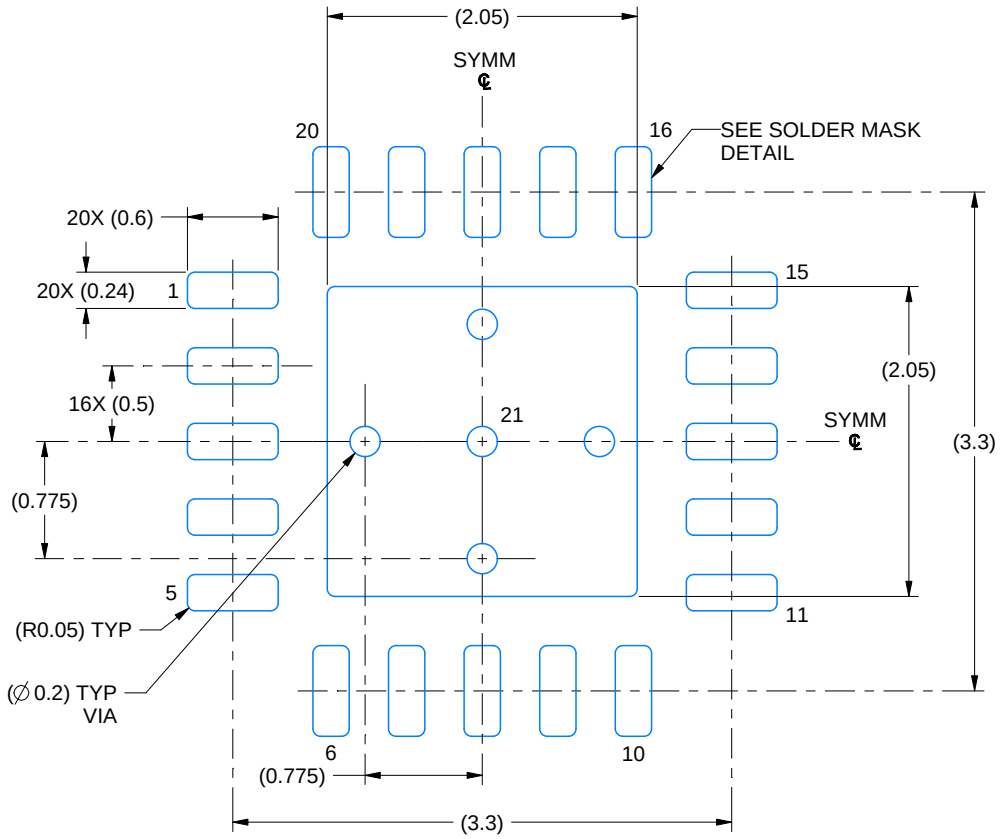
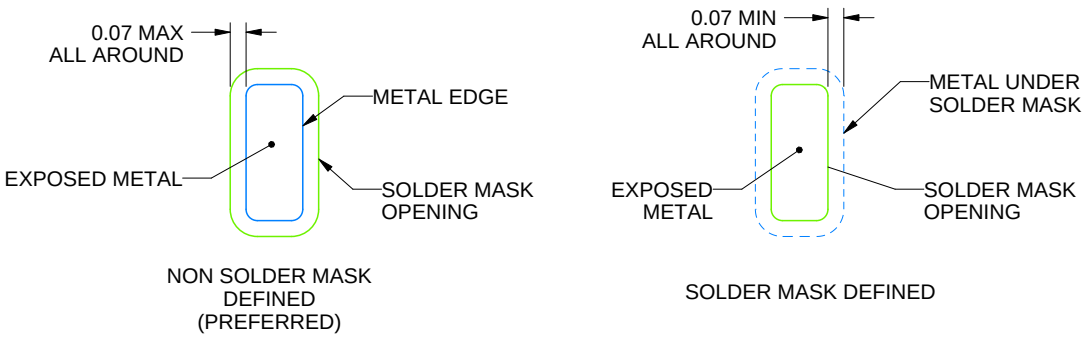
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

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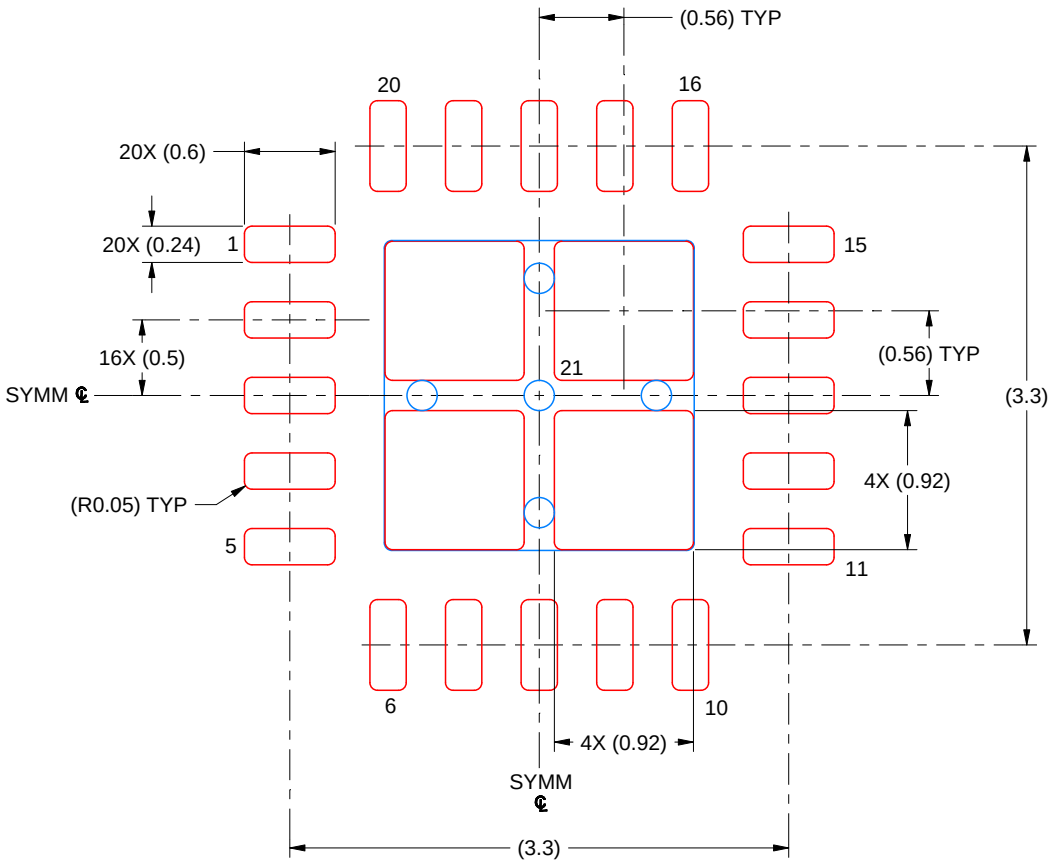
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 21
81% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月