CD405xB 8 チャネルを 1 セット備えた、CMOS アナログ・マルチプレクサ / デマルチプレクサ、ロジック・レベル変換付き

1 特長

- 幅広いデジタルおよびアナログ信号レベル：
  - デジタル：3V 〜 20V
  - アナログ：$20V_{P-P}$ 以下
- 単電源電圧範囲：3V〜20V（VDD が 3V 未満の場合は性能が低下）
- 両電源電圧範囲：±3V〜±10V
- 低いオン抵抗、V_{DD} = 15V の信号入力範囲で、125Ω (代表値)
- V_{DD} = 15V で ±10pA (代表値) という低いチャネルリーク
- 低静止電力消費量: 0.2μW (標準値)
- Break-Before-Make スイッチングにより、チャネルのオーバーラップを排除
- 双方向の信号パス
- ESD 保護 (HBM)：3000V、CDM：2000V
- 業界標準の 4051 マルチプレクサとピン互換

2 アプリケーション

- アナログおよびデジタルの多重化 / 多重分離
- アナログ・デジタルおよびデジタル・アナログ変換
- 信号ゲーティング
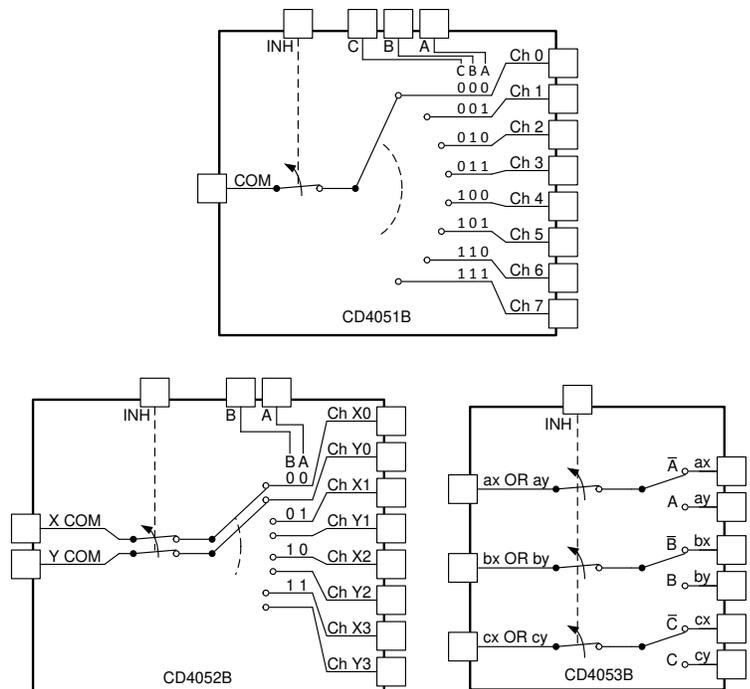- ファクトリ・オートメーション
- テレビ
- 電化製品
- 民生用オーディオ
- プログラム可能な論理回路
- センサ

3 概要

CD405xB アナログ マルチプレクサ / デマルチプレクサは、オン状態のインピーダンスが低くオフ状態のリーク電流が非常に小さいデジタル制御のアナログ スイッチです。これらのマルチプレクサ回路は、制御信号の論理状態にかかわらず、V_{DD} - V_{SS} および V_{DD} - V_{EE} の電源電圧範囲全体にわたって非常に小さな静止電力しか消費しません。

パッケージ情報

部品番号	パッケージ [1]	パッケージ サイズ [2]
CD405xB	J (CDIP、16)	19.50mm × 6.92mm
	N (PDIP、16)	19.3mm × 9.4mm
	D (SOIC、16)	9.9mm × mm
	NS (SOP、16)	10.2mm × 7.8mm
	PW (TSSOP、16)	5mm × 6.4mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。

CD4051B の機能図

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Product Folder Links: *CD4051B CD4052B CD4053B*

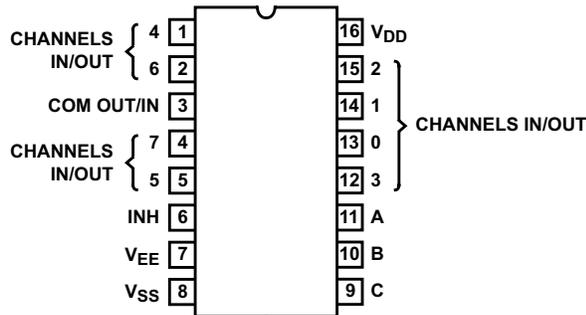English Data Sheet: SCHS047

4 Pin Configuration and Functions

図 4-1. CD4051B E, M, NS, and PW Package, 16-Pin PDIP, CDIP, SOIC, SOP, and TSSOP (Top View)
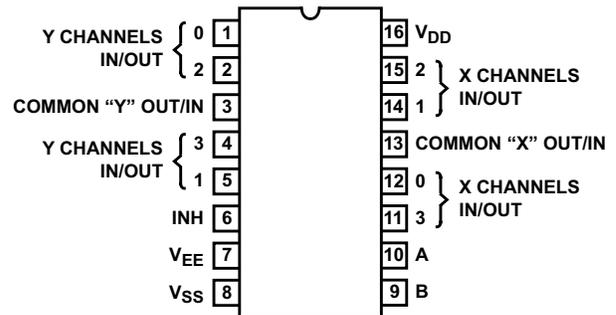
図 4-2. CD4052B E, M, NS, and PW Package, 16-Pin PDIP, CDIP, SOP, and TSSOP (Top View)
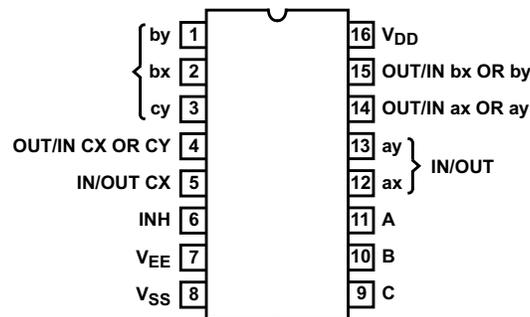
図 4-3. CD4053B E, M, NS, and PW Package, 16-Pin PDIP, CDIP, SOP, and TSSOP (Top View)

表 4-1. Pin Functions CD4051B

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
1	CH 4 IN/OUT	I/O	Channel 4 in/out
2	CH 6 IN/OUT	I/O	Channel 6 in/out
3	COM OUT/IN	I/O	Common out/in
4	CH 7 IN/OUT	I/O	Channel 7 in/out
5	CH 5 IN/OUT	I/O	Channel 5 in/out
6	INH	I	Disables all channels. See 表 7-1.
7	V_{EE}	—	Negative power input
8	V_{SS}	—	Ground
9	C	I	Channel select C. See 表 7-1.
10	B	I	Channel select B. See 表 7-1.
11	A	I	Channel select A. See 表 7-1.
12	CH 3 IN/OUT	I/O	Channel 3 in/out
13	CH 0 IN/OUT	I/O	Channel 0 in/out
14	CH 1 IN/OUT	I/O	Channel 1 in/out
15	CH 2 IN/OUT	I/O	Channel 2 in/out
16	V_{DD}	—	Positive power input

(1)   I = input, O = output

資料に関するフィードバック (ご意見やお問い合わせ) を送信   3

Product Folder Links: *CD4051B CD4052B CD4053B*

English Data Sheet: SCHS047

表 4-2. Pin Functions CD4052B

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
1	Y CH 0 IN/OUT	I/O	Channel Y0 in/out
2	Y CH 2 IN/OUT	I/O	Channel Y2 in/out
3	Y COM OUT/IN	I/O	Y common out/in
4	Y CH 3 IN/OUT	I/O	Channel Y3 in/out
5	Y CH 1 IN/OUT	I/O	Channel Y1 in/out
6	INH	I	Disables all channels. See 表 7-1.
7	V_{EE}	—	Negative power input
8	V_{SS}	—	Ground
9	B	I	Channel select B. See 表 7-1.
10	A	I	Channel select A. See 表 7-1.
11	X CH 3 IN/OUT	I/O	Channel X3 in/out
12	X CH 0 IN/OUT	I/O	Channel X0 in/out
13	X COM IN/OUT	I/O	X common out/in
14	X CH 1 IN/OUT	I/O	Channel in/out
15	X CH 2 IN/OUT	I/O	Channel in/out
16	V_{DD}	—	Positive power input

(1)   I = input, O = output

表 4-3. Pin Functions CD4053B

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
1	BY IN/OUT	I/O	B channel Y in/out
2	BX IN/OUT	I/O	B channel X in/out
3	CY IN/OUT	I/O	C channel Y in/out
4	CX OR CY OUT/IN	I/O	C common out/in
5	CX IN/OUT	I/O	C channel X in/out
6	INH	I	Disables all channels. See 表 7-1.
7	V_{EE}	—	Negative power input
8	V_{SS}	—	Ground
9	C	I	Channel select C. See 表 7-1.
10	B	I	Channel select B. See 表 7-1.
11	A	I	Channel select A. See 表 7-1.
12	AX IN/OUT	I/O	A channel X in/out
13	AY IN/OUT	I/O	A channel Y in/out
14	AX OR AY OUT/IN	I/O	A common out/in
15	BX OR BY OUT/IN	I/O	B common out/in
16	V_{DD}	—	Positive power input

(1)   I = input, O = output

Product Folder Links: *CD4051B CD4052B CD4053B*

English Data Sheet: SCHS047

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1] [2]

			MIN	MAX	UNIT
	Supply Voltage	V+ to V-, Voltages Referenced to V_{SS} Terminal	−0.5	20	V
	DC Input Voltage		−0.5	V_{DD}+0.5	V
	DC Input Current	Any One Input	−10	10	mA
T_{JMAX1}	Maximum junction temperature, ceramic package			175	°C
T_{JMAX2}	Maximum junction temperature, plastic package			150	°C
T_{stg}	Storage temperature		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±3000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±2000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Temperature Range	−55		125	°C

5.4 Thermal Information

THERMAL METRIC[1]		CD405x				UNIT
		E (PDIP)	M (SOIC)	NS (SOP)	PW (TSSOP)	
		16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	67	73	64	116.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

Over operating free-air temperature range, V_{SUPPLY} = ±5V, and R_L = 100Ω, (unless otherwise noted)[1]

PARAMETER	TEST CONDITIONS					MIN	TYP	MAX	UNIT
SIGNAL INPUTS (V_{IS}) AND OUTPUTS (V_{OS})									
	V_{IS} (V)	V_{EE} (V)	V_{SS} (V)	V_{DD} (V)	TEMP				
Quiescent Device Current, I_{DD} Max		0V	0V	5V	−55°C			60	µA
					−40°C			60	
					25°C		17	60	
					85°C			150	
					125°C			150	
		0V	0V	10V	−55°C			60	
					−40°C			60	
					25°C		18	60	
					85°C			300	
					125°C			300	
		0V	0V	15V	−55°C			60	
					−40°C			60	
					25°C		18	60	
					85°C			600	
					125°C			600	
		0V	0V	20V	−55°C			100	
					−40°C			100	
					25°C		18	100	
					85°C			3000	
					125°C			3000	
Drain to Source ON Resistance r_{ON} Max $0 \le V_{IS} \le V_{DD}$		0V	0V	5V	−55°C			800	Ω
					−40°C			850	
					25°C		470	1050	
					85°C			1200	
					125°C			1300	
		0V	0V	10V	−55°C			310	
					−40°C			300	
					25°C		180	400	
					85°C			520	
					125°C			550	
		0V	0	15V	−55°C			200	
					−40°C			210	
					25°C		125	240	
					85°C			300	
					125°C			300	
Change in ON Resistance (Between Any Two Channels), ΔR_{ON}		0V	0V	5V	25°C		15		Ω
		0V	0V	10V			10		
		0V	0V	15V			5		

Product Folder Links: *CD4051B CD4052B CD4053B*

English Data Sheet: SCHS047

5.5 Electrical Characteristics (続き)

Over operating free-air temperature range, V_{SUPPLY} = ±5V, and R_L = 100Ω, (unless otherwise noted)[1]

PARAMETER			TEST CONDITIONS				MIN	TYP	MAX	UNIT
OFF Channel Leakage Current: Any Channel OFF (Max) or ALL Channels OFF (COMMON OUT/IN) (Max)			0V	0V	18V	−55°C			± 100	nA
						−40°C			± 100	
						25°C		± 0.3	± 100 [2]	
						85°C			± 1000 [2]	
						125°C			± 1000 [2]	
ON Channel Leakage Current: Any Channel ON (Max) or ALL Channels ON (COMMON OUT/IN) (Max)		5 or 0	−5V	0V	10.5V	85°C			± 300	nA
		5	0V	0V	18V	85°C			± 300	
Capaci tance	Input, C_{IS}		0V	0V	10V	25°C		5		pF
	Output, C_{OS}	CD4 051						30		
	Output, C_{OS}	CD4 052						18		
	Output, C_{OS}	CD4 053						9		
	Feed through, C_{IOS}							0.2		
Prop Delay			V_{DD}	R_L = 200kΩ	5V	25°C		30	60	ns
				C_L = 50pF	10V			15	30	
				t_r, t_f = 20ns	15V			10	20	

5.5 Electrical Characteristics (続き)

Over operating free-air temperature range, V_{SUPPLY} = ±5V, and R_L = 100Ω, (unless otherwise noted)[1]

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
CONTROL (ADDRESS OR INHIBIT), V_C							
Input Low Voltage, V_{IL}, Max		5V	−55°C		0.8		V
			−40°C		0.8		
			25°C			0.8	
			85°C		0.8		
			125°C		0.8		
		10V	−55°C		0.8		
			−40°C		0.8		
			25°C			0.8	
			85°C		0.8		
			125°C		0.8		
		15V	−55°C		0.8		
			−40°C		0.8		
			25°C			0.8	
			85°C		0.8		
			125°C		0.8		
Input High Voltage, V_{IH}, Min		5V	−55°C		3.5		V
			−40°C		3.5		
			25°C	3.5			
			85°C		3.5		
			125°C		3.5		
		10V	−55°C		7		
			−40°C		7		
			25°C	7			
			85°C		7		
			125°C		7		
		15V	−55°C		11		
			−40°C		11		
			25°C	11			
			85°C		11		
			125°C		11		
Input current, I_{IN} (Max)	V_{IN} = 0, 18	18V	−55°C			±1	µA
			−40°C			±1	
			25°C		±0.6	±1	
			85°C			±1	
			125°C			±1	

						MIN	TYP	MAX	UNIT
Propagation Delay Time	Address-to-Signal OUT (Channels ON or OFF) (See Figure 10, Figure 11, and Figure 15)	t_r , t_f = 20ns, C_L = 50pF, R_L = 10kΩ	0V	0V	5V			450	720	ns
			0V	0V	10V			160	320	
			0V	0V	15V			120	240	
			−5V	0V	5V			225	450	

Product Folder Links: *CD4051B CD4052B CD4053B*

English Data Sheet: SCHS047

5.5 Electrical Characteristics (続き)

Over operating free-air temperature range, V_{SUPPLY} = ±5V, and R_L = 100Ω, (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS					MIN	TYP	MAX	UNIT
Propagation Delay Time	Inhibit-to-Signal OUT (Channel Turning ON) (See Figure 11)	t_r, t_f = 20ns, C_L = 50pF, R_L = 1kΩ	0V	0V	5V			400	720	ns
			0V	0V	10V			160	320	
			0V	0V	15V			120	240	
			−10V	0V	5V			200	400	
Propagation Delay Time	Inhibit-to-Signal OUT (Channel Turning OFF) (See Figure 17)	t_r, t_f = 20ns, C_L = 50pF, R_L = 10kΩ	0V	0V	5V			200	450	ns
			0V	0V	10V			90	210	
			0V	0V	15V			70	160	
			−10V	0V	5V			130	300	
Input Capacitance, C_{IN} (Any Address or Inhibit Input)			−5V	0V	5V	25°C		5	7.5	pF

(1)   Peak-to-Peak voltage symmetrical about ($V_{DD} - V_{EE}$) / 2.
(2)   Determined by minimum feasible leakage measurement for automatic testing.

5.6 AC Performance Characteristics

V_{DD} = +15V, V_{SS} = V_{EE} = 0V, T_A = 25℃ (unless otherwise noted)

PARAMETER	TEST CONDITIONS						TYP	UNIT
	V_{IS} (V)	V_{DD} (V)	R_L (kΩ)					
Cutoff (–3dB) Frequency Channel ON (Sine Wave Input)	5[1]	10	1	V_{OS} at Common OUT/IN		CD4053	30	MHz
		10	1			CD4052	25	
		10	1			CD4051	20	
	V_{EE} = V_{SS} , 20Log(V_{OS}/V_{IS}) = –3dB			V_{OS} at Any Channel			60	
Total Harmonic Distortion, THD	2[1]	5	10				0.3%	%
	3[1]	10	10				0.2%	
	5[1]	15	10				0.12%	
	V_{EE} = V_{SS}, f_{IS} = 1kHz Sine Wave							
–40dB Feedthrough Frequency (All Channels OFF)	5[1]	10	1	V_{OS} at Common OUT/IN		CD4053	8	MHz
						CD4052	10	
	V_{EE} = V_{SS} , 20Log(V_{OS}/V_{IS}) = –40dB					CD4051	12	
				V_{OS} at Any Channel			8	
–40dB Signal Crosstalk Frequency	5[1]	10	1				3	MHz
	V_{EE} = V_{SS} , 20Log(V_{OS}/V_{IS}) = –3dB			Between Sections, CD4052 Only		Measured on Common	6	
						Measured on Any Channel	10	
				Between Any Two Sections, CD4053 Only		In Pin 2, Out Pin 14	2.5	
						In Pin 15, Out Pin 14	6	
Address-or-Inhibit-to-Signal Crosstalk		10	10[2]				65	mV$_{PEAK}$
	V_{EE} = 0, V_{SS} = 0, t_r , t_f = 20ns, mVPEAK V_{CC} = V_{DD} – V_{SS} (Square Wave)						65	mV$_{PEAK}$

(1)   Peak-to-Peak voltage symmetrical about (V_{DD} - V_{EE}) / 2.
(2)   Both ends of channel.

Product Folder Links: *CD4051B CD4052B CD4053B*

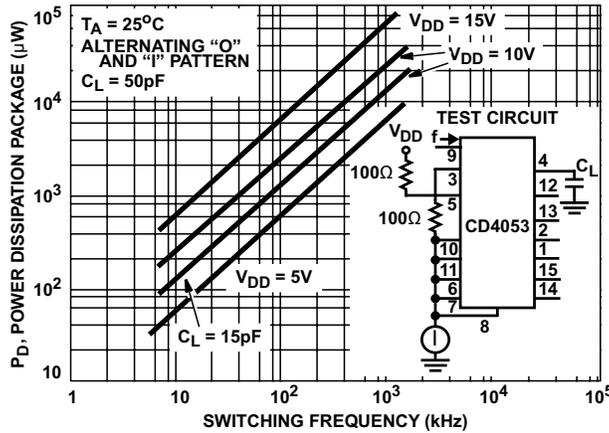English Data Sheet: *SCHS047*

5.7 Typical Characteristics
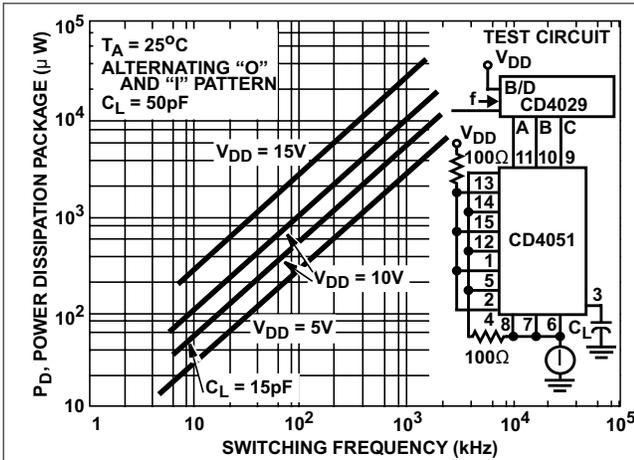
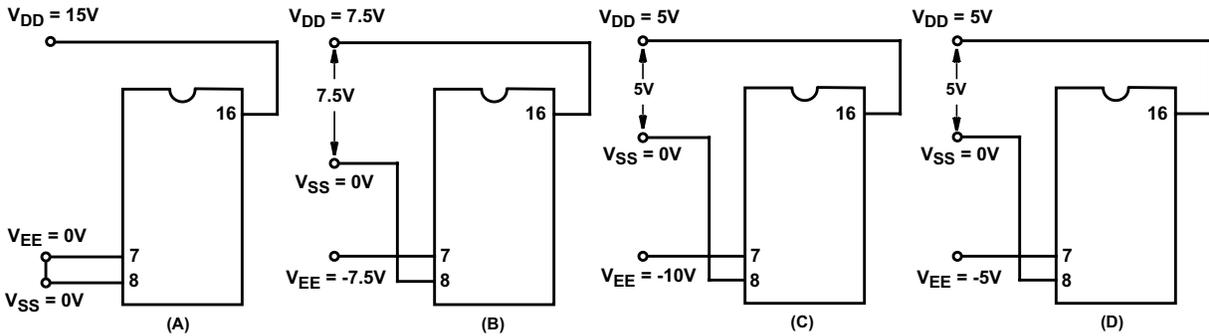図 5-1. Dynamic Power Dissipation vs Switching Frequency (CD4051B)
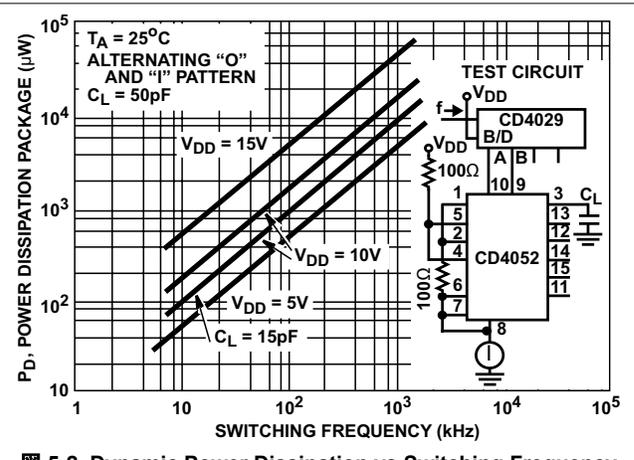
図 5-2. Dynamic Power Dissipation vs Switching Frequency (CD4052B)

図 5-3. Dynamic Power Dissipation vs Switching Frequency (CD4053B)

6 Parameter Measurement Information

図 6-1. Typical Bias Voltages

注

The ADDRESS (digital-control inputs) and INHIBIT logic levels are: $0 = V_{SS}$ and $1 = V_{DD}$. The analog signal (through the TG) may swing from V_{EE} to V_{DD}.
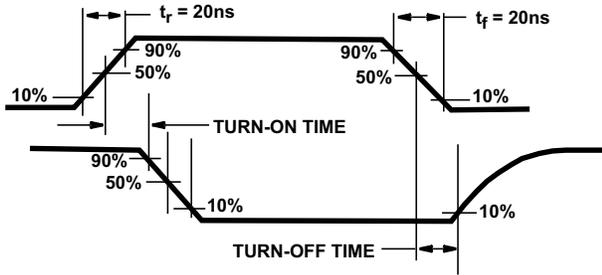
図 6-2. Waveforms, Channel Being Turned ON (R_L = 1kΩ)
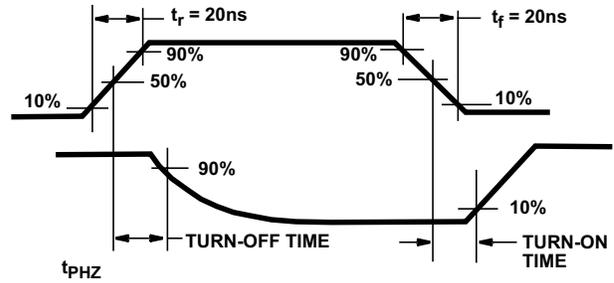
図 6-3. Waveforms, Channel Being Turned OFF (R_L = 1kΩ)
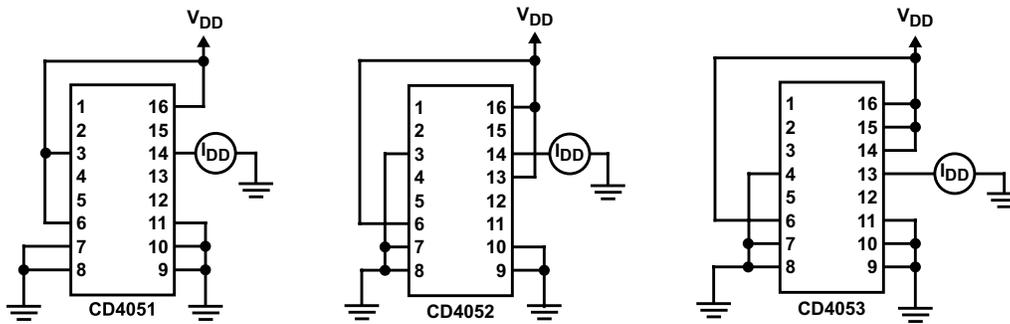
図 6-4. OFF Channel Leakage Current – Any Channel OFF
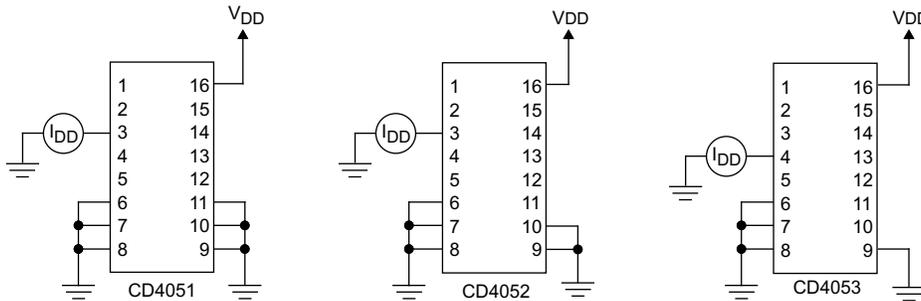
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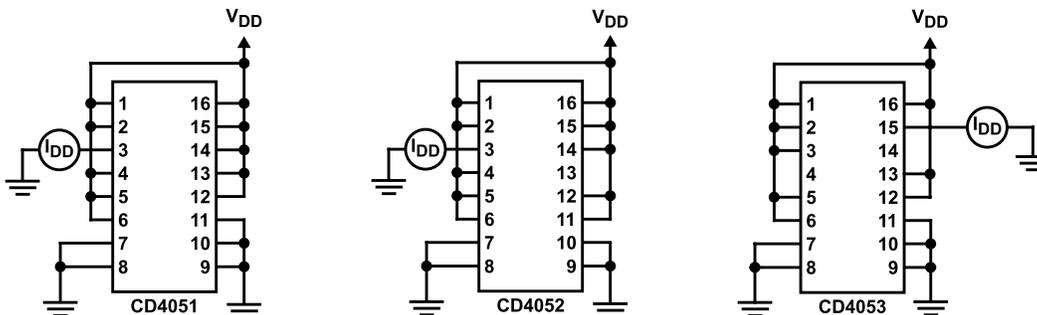図 6-5. On Channel Leakage Current – Any Channel On

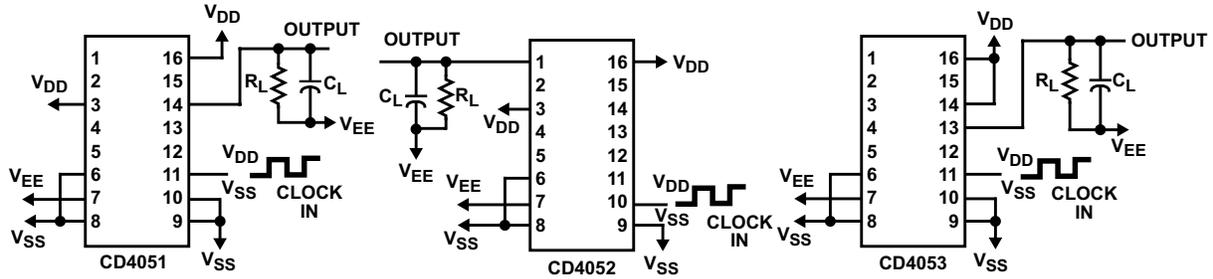図 6-6. OFF Channel Leakage Current – All Channels OFF

Product Folder Links: *CD4051B CD4052B CD4053B*

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図 6-7. Propagation Delay – Address Input to Signal Output
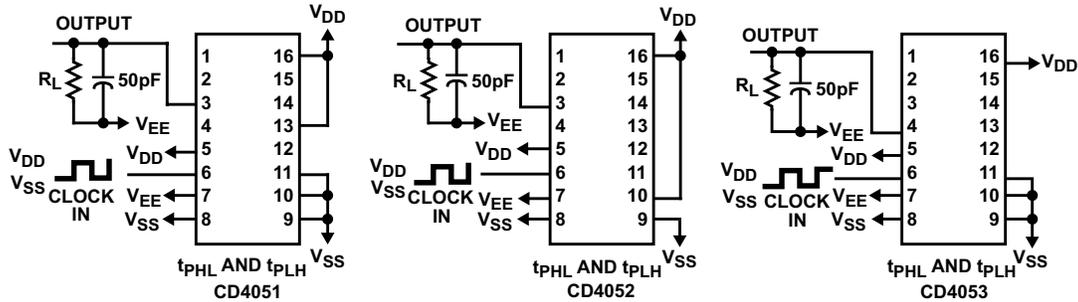
図 6-8. Propagation Delay – Inhibit Input to Signal Output

MEASURE < 2μA ON ALL
"OFF" CHANNELS (e.g., CHANNEL 6)

MEASURE < 2μA ON ALL
"OFF" CHANNELS (e.g., CHANNEL 2x)

MEASURE < 2μA ON ALL
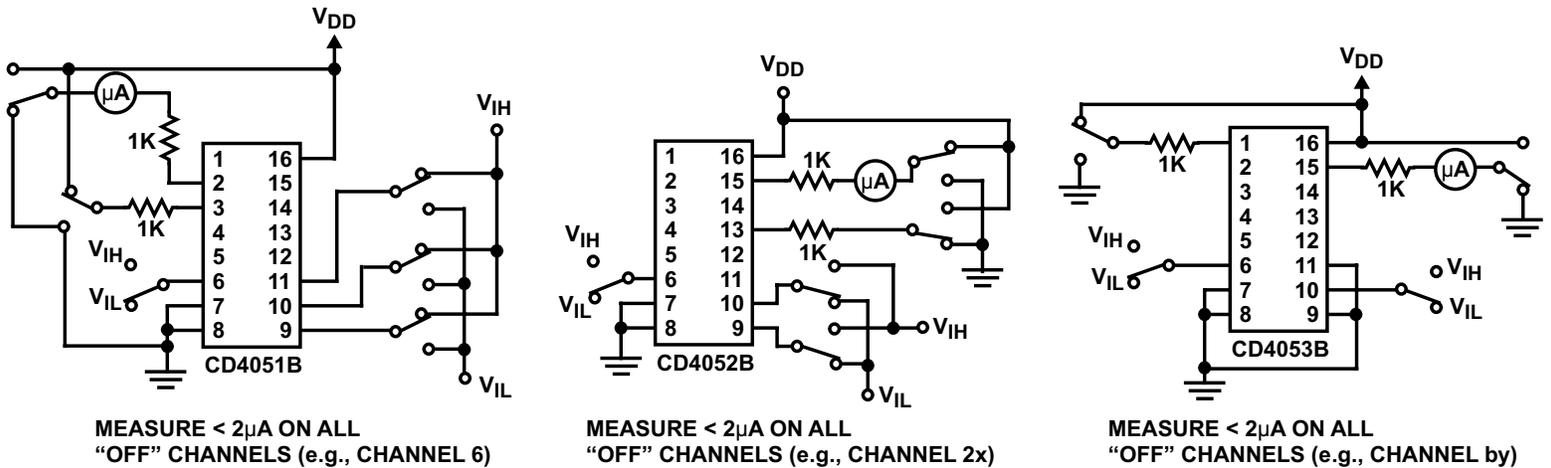"OFF" CHANNELS (e.g., CHANNEL by)

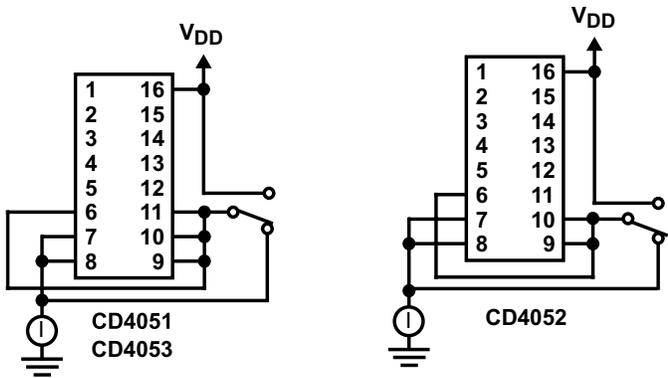図 6-9. Input Voltage Test Circuits (Noise Immunity)

図 6-10. Quiescent Device Current
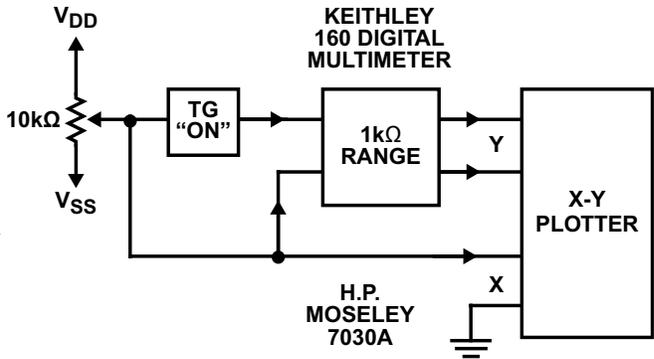
図 6-11. Channel ON Resistance Measurement Circuit

NOTE: Measure inputs sequentially, to both V_{DD} and V_{SS} connect all unused inputs to either V_{DD} or V_{SS}.

NOTE: Measure inputs sequentially, to both V_{DD} and V_{SS} connect all unused inputs to either V_{DD} or V_{SS}.
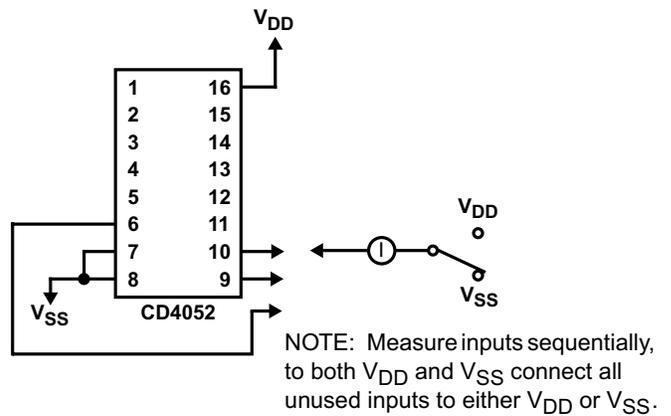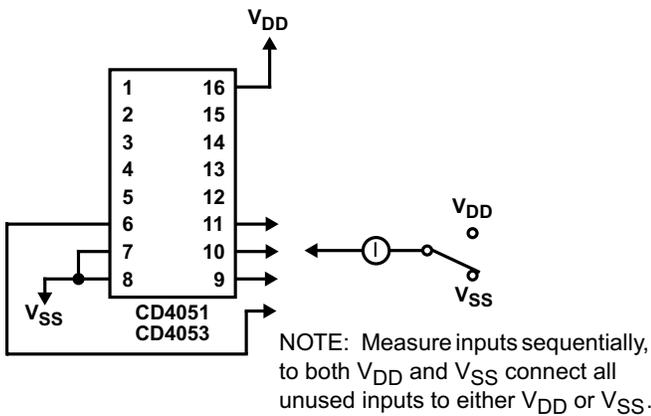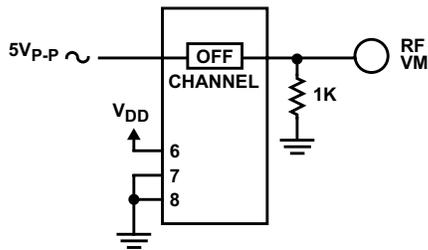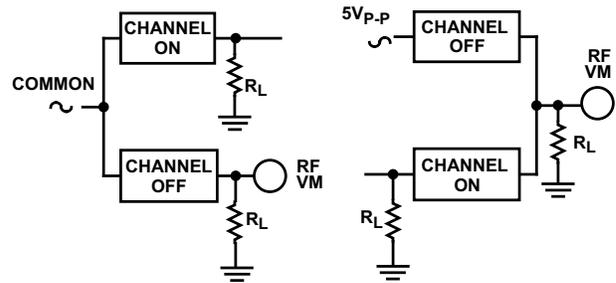
図 6-12. Input Current
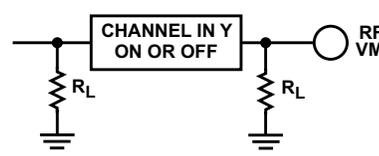

図 6-13. Feed-Through (All Types)

図 6-14. Crosstalk Between Any Two Channels (All Types)
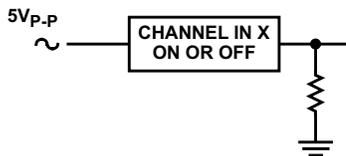
**図 6-15. Crosstalk Between Duals or Triplets (CD4052B, CD4053B)**

図 6-16. Typical Time-Division Application of the CD4052B
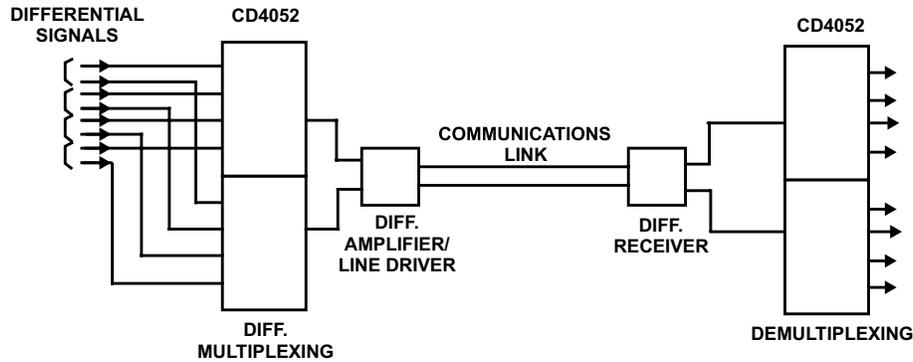
Special Considerations: In applications where separate power sources are used to drive V_{DD} and the signal inputs, the V_{DD} current capability should exceed V_{DD}/R_L (R_L = effective external load). This provision avoids permanent current flow or clamp action on the V_{DD} supply when power is applied or removed from the CD4051B, CD4052B or CD4053B.
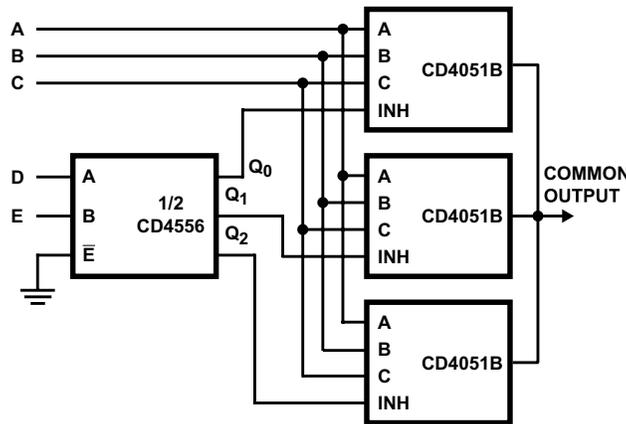
図 6-17. 24-to-1MUX Addressing

7 Detailed Description

7.1 Overview

The CD4051B device is a single 8-channel multiplexer having three binary control inputs, A, B, and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned on, and connect one of the 8 inputs to the output.

The CD4052B device is a differential 4-channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 of 4 pairs of channels to be turned on and connect the analog inputs to the outputs.

The device is a triple 2-channel multiplexer having three separate digital control inputs, A, B, and C, and an inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole, double-throw configuration.

When these devices are used as demultiplexers, the CHANNEL IN/OUT terminals are the outputs and the COMMON OUT/IN terminals are the inputs.

7.2 Functional Block Diagrams
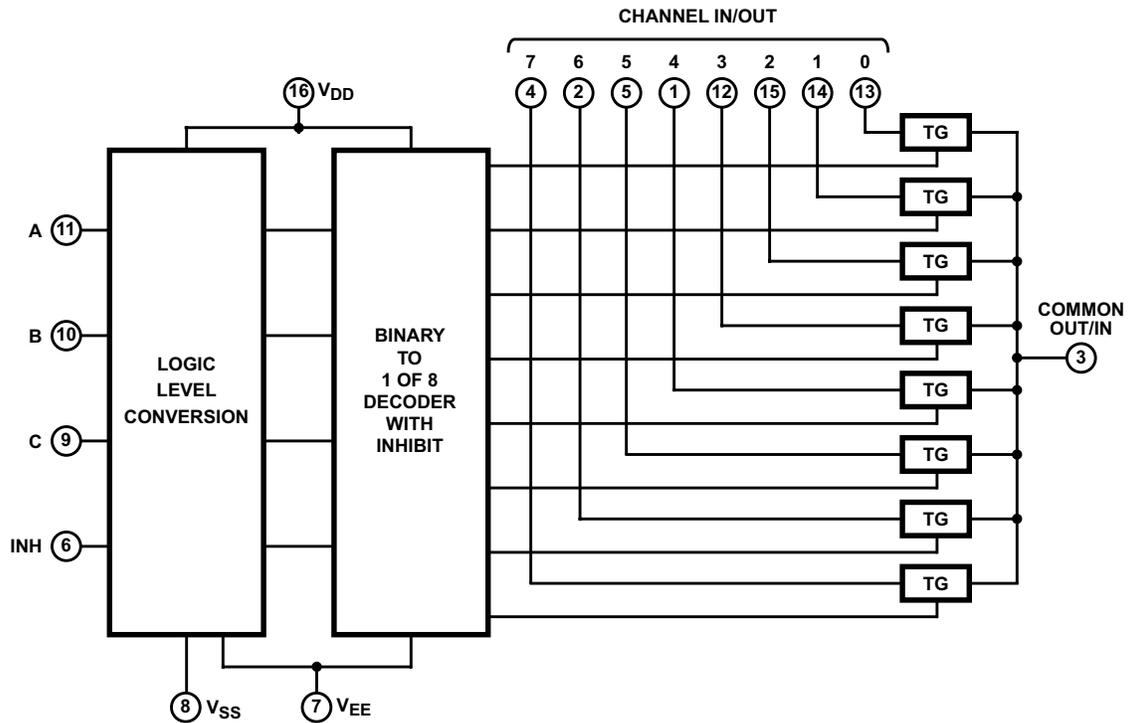
All inputs are protected by standard CMOS protection network.

図 7-1. Functional Block Diagram, CD4051B
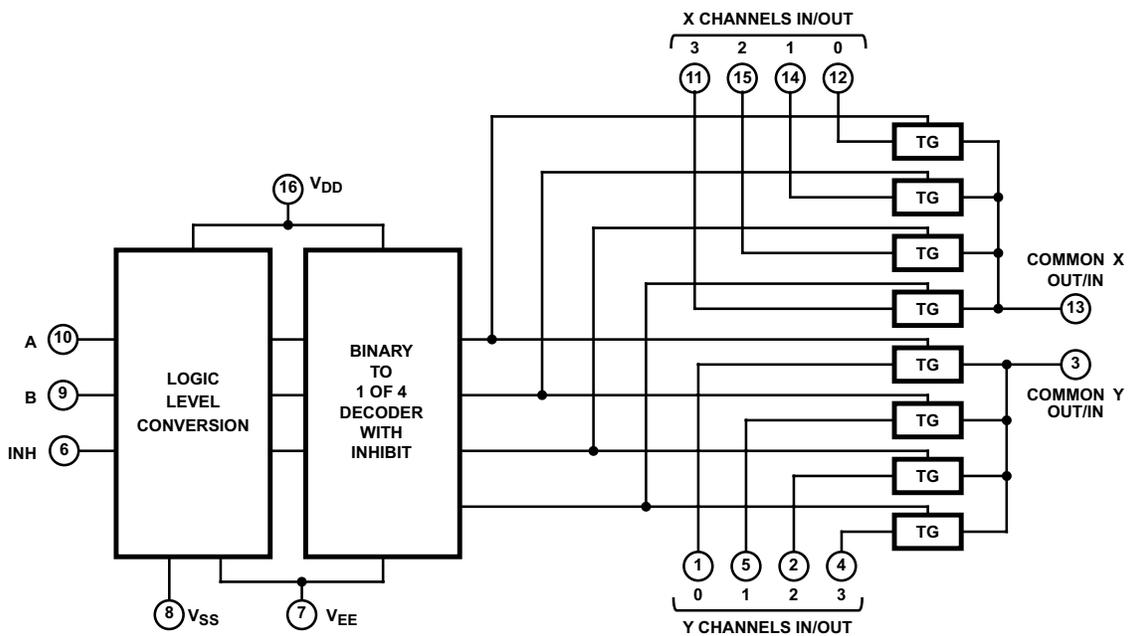
All inputs are protected by standard CMOS protection network.

図 7-2. Functional Block Diagram, CD4052B
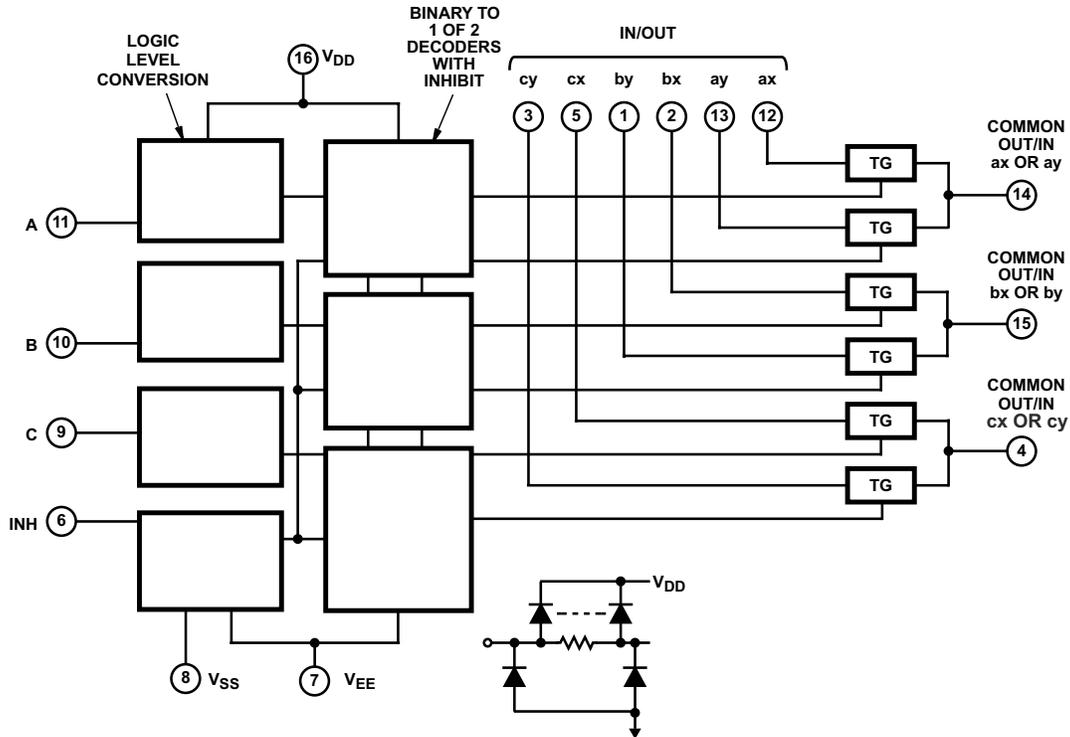
図 7-3. Functional Block Diagram, CD4053B

All inputs are protected by standard CMOS protection network.

7.3 Feature Description

The CD405xB line of multiplexers and demultiplexers can accept a wide range of digital and analog signal levels. Digital signals range from 3V to 20V, and analog signals are accepted at levels ≤ 20V. The devices have low ON resistance, typically 125Ω over 15V$_{P-P}$ signal input range for V$_{DD}$ − V$_{EE}$ = 18V. This feature allows for very little signal loss through the switch.

The CD405xB devices also have high OFF resistance, which keeps from the devices from wasting power when the switch is in the OFF position, with typical channel leakage of ±100pA at V$_{DD}$ − V$_{EE}$ = 18V.

Binary address decoding on the chip makes channel selection simple. When channels are changed, a break-before-make system eliminates channel overlap.

Product Folder Links: *CD4051B CD4052B CD4053B*

English Data Sheet: SCHS047

7.4 Device Functional Modes

表 7-1. Truth Table [1]

INPUT STATES				ON CHANNEL(S)
INHIBIT	**C**	**B**	**A**	
CD4051B				
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	X	X	X	None
CD4052B				
0		0	0	0x, 0y
0		0	1	1x, 1y
0		1	0	2x, 2y
0		1	1	3x, 3y
1		X	X	None
CD4053B				
0	X	X	0	ax
0	X	X	1	ay
0	X	0	X	bx
0	X	1	X	by
0	0	X	X	cx
0	1	X	X	cy
1	X	X	X	None

(1)   X = Do not care

8 Application and Implementation

> **注**
>
> 以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The CD405xB multiplexers and demultiplexers can be used for a wide variety of applications.

8.2 Typical Application

One application of the CD4051B is to use it in conjunction with a microcontroller to poll a keypad. 図 8-1 shows the basic schematic for such a polling system. The microcontroller uses the channel select pins to cycle through the different channels while reading the input to see if a user is pressing any of the keys. This application is a very robust setup, allowing for multiple simultaneous key-presses with very little power consumption. This setup also uses very few pins on the microcontroller. The down side of polling is that the microcontroller must continually scan the keys for a press and can do little else during this process.
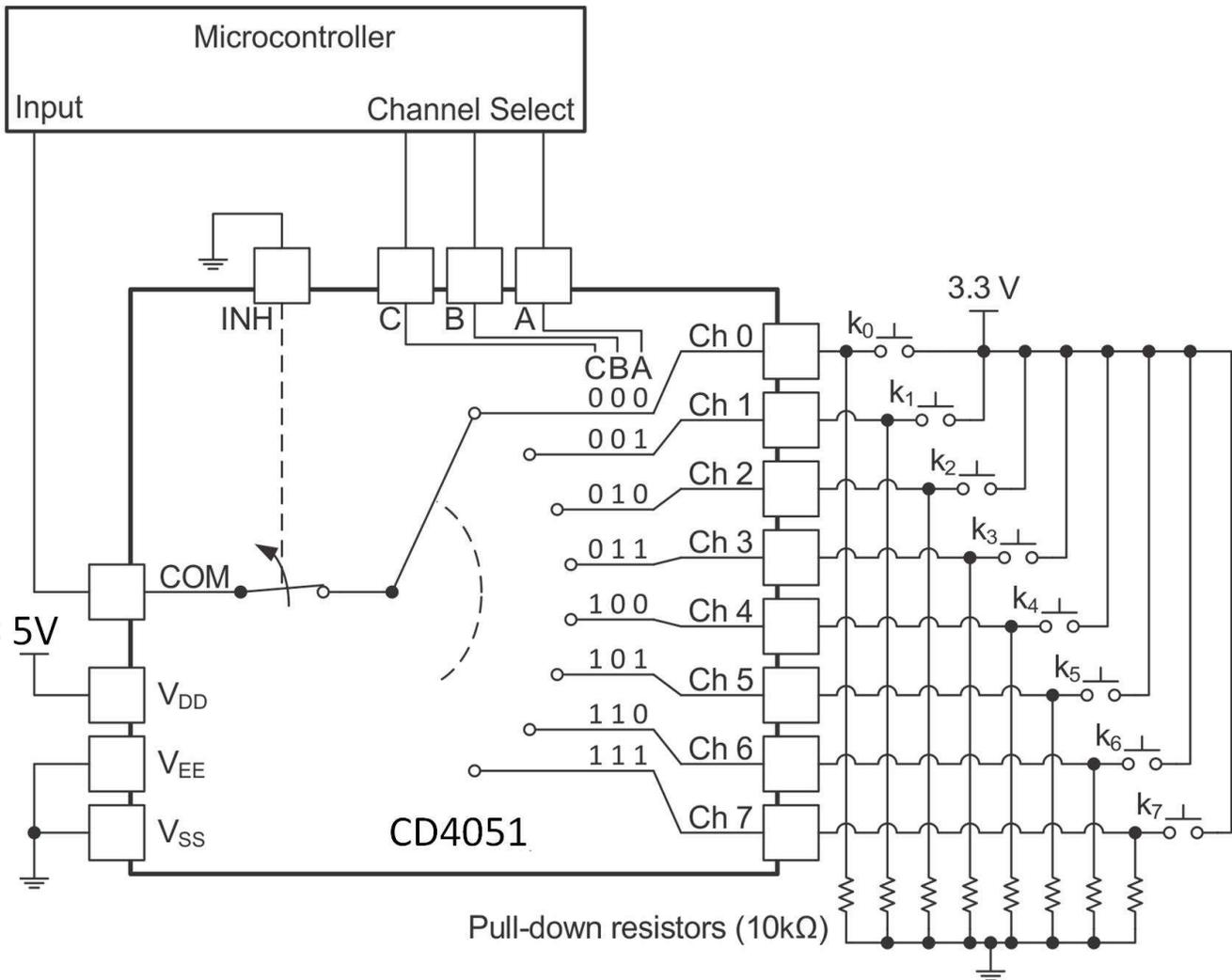

図 8-1. The CD4051B Being Used to Help Read Button Presses on a Keypad

8.2.1 Design Requirements

These devices use CMOS technology and have balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

8.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
   - For switch time specifications, see propagation delay times in *Electrical Characteristics*.
   - Inputs should not be pushed more than 0.5V above V_{DD} or below V_{EE}.
   - For input voltage level specifications for control inputs, see V_{IH} and V_{IL} in *Electrical Characteristics*.
2. Recommended Output Conditions:
   - Outputs should not be pulled above V_{DD} or below V_{EE}.
3. Input or output current consideration:
   - The CD405xB series of parts do not have internal current drive circuitry and thus cannot sink or source current. Any current will be passed through the device.

8.2.3 Application Curve
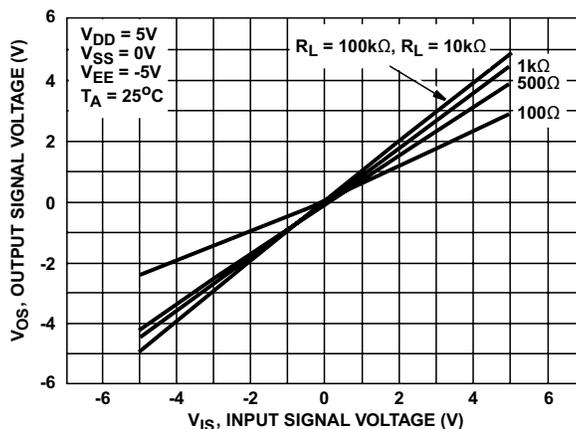
図 8-2. ON Characteristics for 1 of 8 Channels (CD4051B)

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Electrical Characteristics*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1µF bypass capacitor is recommended. If there are multiple pins labeled V_{CC}, then a 0.01µF or 0.022µF capacitor is recommended for each V_{CC} because the V_{CC} pins will be tied together internally. For devices with dual supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1µF bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1µF and 1µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This reflection is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self−inductance of the trace — resulting in the reflection. It is a given that not all PCB traces can be straight, and so they will have to turn corners. 図 8-3 shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

8.4.2 Layout Example

WORST BETTER BEST

2W

1W min.

W

図 8-3. Trace Example

Product Folder Links: *CD4051B CD4052B CD4053B*

English Data Sheet: SCHS047
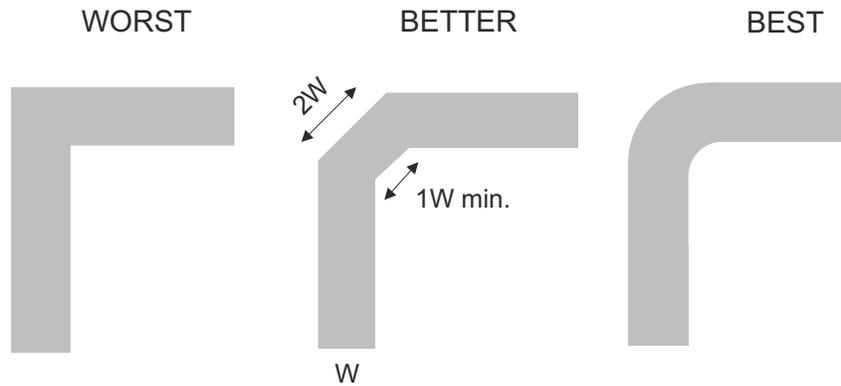
9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs*

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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9.4 Trademarks

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9.5 静電気放電に関する注意事項

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

重要なお知らせと免責事項

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
7901502EA	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7901502EA CD4052BF3A
8101801EA	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8101801EA CD4053BF3A
CD4051BE	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4051BE
CD4051BE.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4051BE
CD4051BEE4	Obsolete	Production	PDIP (N) | 16	-	-	Call TI	Call TI	-55 to 125	CD4051BE
CD4051BF	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4051BF
CD4051BF.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4051BF
CD4051BF3A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4051BF3A
CD4051BF3A.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4051BF3A
CD4051BM96	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4051BM
CD4051BM96.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4051BM
CD4051BM96G3	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	CD4051BM
CD4051BM96G4	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	CD4051BM
CD4051BMT	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	CD4051BM
CD4051BNSR	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4051B
CD4051BNSR.A	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4051B
CD4051BPW	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-55 to 125	CM051B
CD4051BPWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM051B
CD4051BPWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM051B
CD4051BPWRG4	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-55 to 125	CM051B
CD4052BE	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4052BE
CD4052BE.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4052BE
CD4052BEE4	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4052BE
CD4052BF	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4052BF
CD4052BF.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4052BF
CD4052BF3A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7901502EA CD4052BF3A

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD4052BF3A.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7901502EA CD4052BF3A
CD4052BM	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	CD4052BM
CD4052BM96	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4052BM
CD4052BM96.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4052BM
CD4052BM961G4	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4052BM
CD4052BM961G4.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4052BM
CD4052BM96G3	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	CD4052BM
CD4052BM96G4	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	CD4052BM
CD4052BMT	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	CD4052BM
CD4052BNSR	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4052B
CD4052BNSR.A	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4052B
CD4052BPW	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-55 to 125	CM052B
CD4052BPWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM052B
CD4052BPWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM052B
CD4052BPWRG3	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-55 to 125	CM052B
CD4052BPWRG4	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-55 to 125	CM052B
CD4053BE	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4053BE
CD4053BE.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4053BE
CD4053BEE4	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4053BE
CD4053BF	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4053BF
CD4053BF.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4053BF
CD4053BF3A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8101801EA CD4053BF3A
CD4053BF3A.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8101801EA CD4053BF3A
CD4053BM	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	CD4053M
CD4053BM96	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4053M
CD4053BM96.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4053M
CD4053BM96G3	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	CD4053M
CD4053BM96G4	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	CD4053M

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD4053BMT	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	CD4053M
CD4053BNSR	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4053B
CD4053BNSR.A	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4053B
CD4053BPW	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-55 to 125	CM053B
CD4053BPWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM053B
CD4053BPWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM053B
CD4053BPWRG3	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-55 to 125	CM053B
CD4053BPWRG4	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-55 to 125	CM053B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF CD4051B, CD4051B-MIL, CD4052B, CD4052B-MIL, CD4053B, CD4053B-MIL :

● Catalog : CD4051B, CD4052B, CD4053B

● Automotive : CD4051B-Q1, CD4051B-Q1, CD4053B-Q1, CD4053B-Q1

● Military : CD4051B-MIL, CD4052B-MIL, CD4053B-MIL

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

● Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

● Military - QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4051BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4051BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4051BNSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
CD4051BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4051BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4052BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4052BM961G4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4052BNSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
CD4052BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4052BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4053BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4053BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4053BNSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
CD4053BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4053BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4051BM96	SOIC	D	16	2500	340.5	336.1	32.0
CD4051BM96	SOIC	D	16	2500	353.0	353.0	32.0
CD4051BNSR	SOP	NS	16	2000	353.0	353.0	32.0
CD4051BPWR	TSSOP	PW	16	2000	353.0	353.0	32.0
CD4051BPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
CD4052BM96	SOIC	D	16	2500	353.0	353.0	32.0
CD4052BM961G4	SOIC	D	16	2500	353.0	353.0	32.0
CD4052BNSR	SOP	NS	16	2000	353.0	353.0	32.0
CD4052BPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
CD4052BPWR	TSSOP	PW	16	2000	353.0	353.0	32.0
CD4053BM96	SOIC	D	16	2500	353.0	353.0	32.0
CD4053BM96	SOIC	D	16	2500	353.0	353.0	32.0
CD4053BNSR	SOP	NS	16	2000	353.0	353.0	32.0
CD4053BPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
CD4053BPWR	TSSOP	PW	16	2000	353.0	353.0	32.0

TUBE
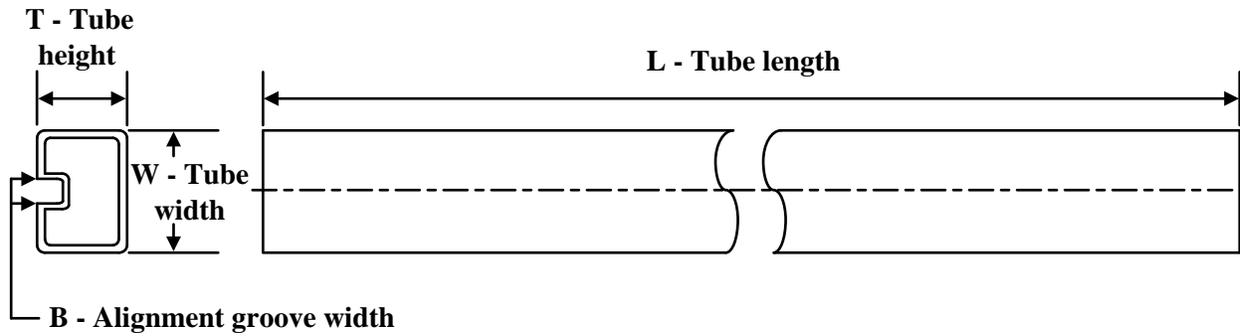
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD4051BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4051BE.A	N	PDIP	16	25	506	13.97	11230	4.32
CD4052BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4052BE.A	N	PDIP	16	25	506	13.97	11230	4.32
CD4052BEE4	N	PDIP	16	25	506	13.97	11230	4.32
CD4053BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4053BE.A	N	PDIP	16	25	506	13.97	11230	4.32
CD4053BEE4	N	PDIP	16	25	506	13.97	11230	4.32

D (R−PDSO−G16)   PLASTIC SMALL OUTLINE
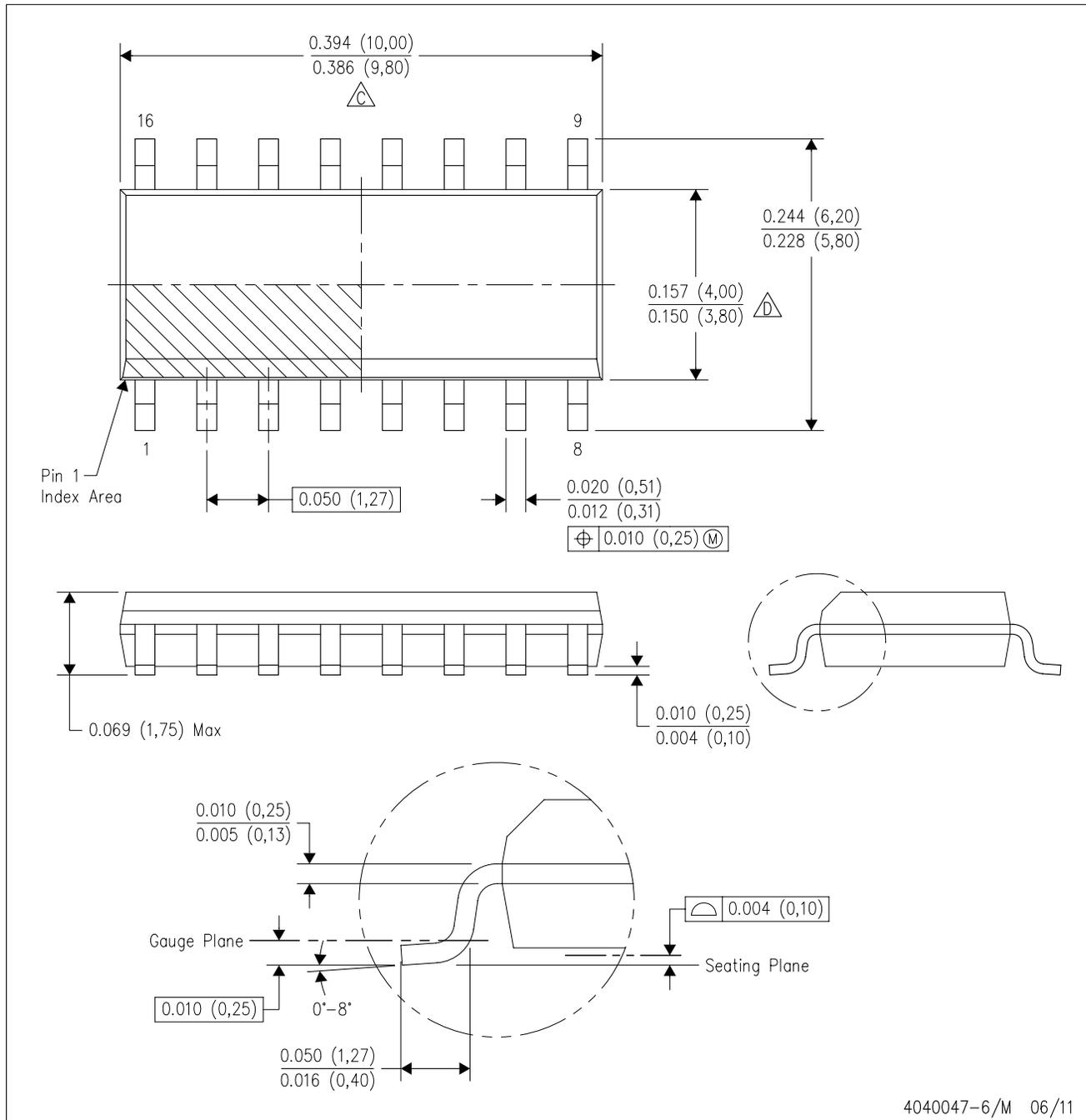
0.394 (10,00)
0.386 (9,80)
⟨C⟩

16   9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80) ⟨D⟩

1   8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)

4040047-6/M   06/11

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         ⟨C⟩ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
              not exceed 0.006 (0,15) each side.
         ⟨D⟩ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
         E.   Reference JEDEC MS−012 variation AC.
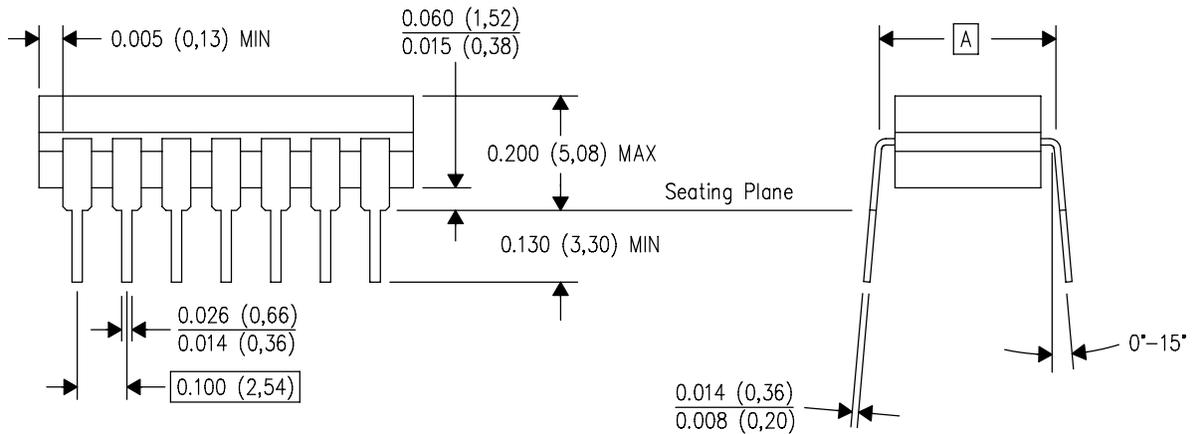
Texas
Instruments
www.ti.com

J (R-GDIP-T**)   CERAMIC DUAL IN-LINE PACKAGE
14 LEADS SHOWN
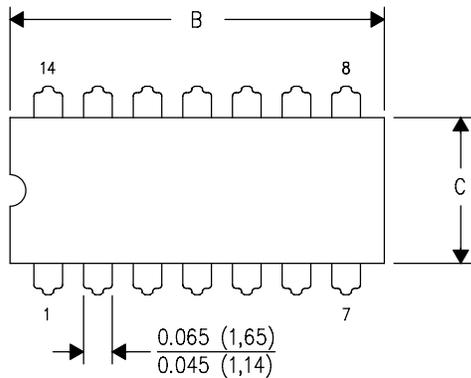
PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

C

1   7

0.065 (1,65)
0.045 (1,14)

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

A

0°-15°

0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   This package is hermetically sealed with a ceramic lid using glass frit.
         D.   Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
         E.   Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

6.6
6.2 TYP

A

PIN 1 INDEX AREA

14X 0.65

16

1

5.1
4.9
NOTE 3

2X
4.55

8

9

B

4.5
4.3
NOTE 4

16X 0.30
0.17

⊕ 0.1 Ⓜ C A B

SEATING
PLANE

C

⌒ 0.1 C

4X (0° -12°)

1.2 MAX

SEE DETAIL A

(0.15) TYP

0.25
GAGE PLANE

0.15
0.05

0.75
0.50

0° -8°

DETAIL A
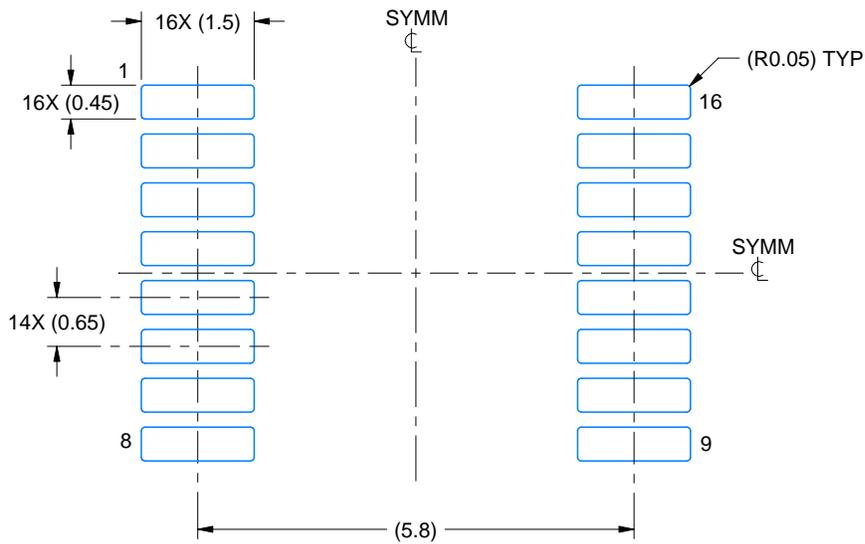TYPICAL
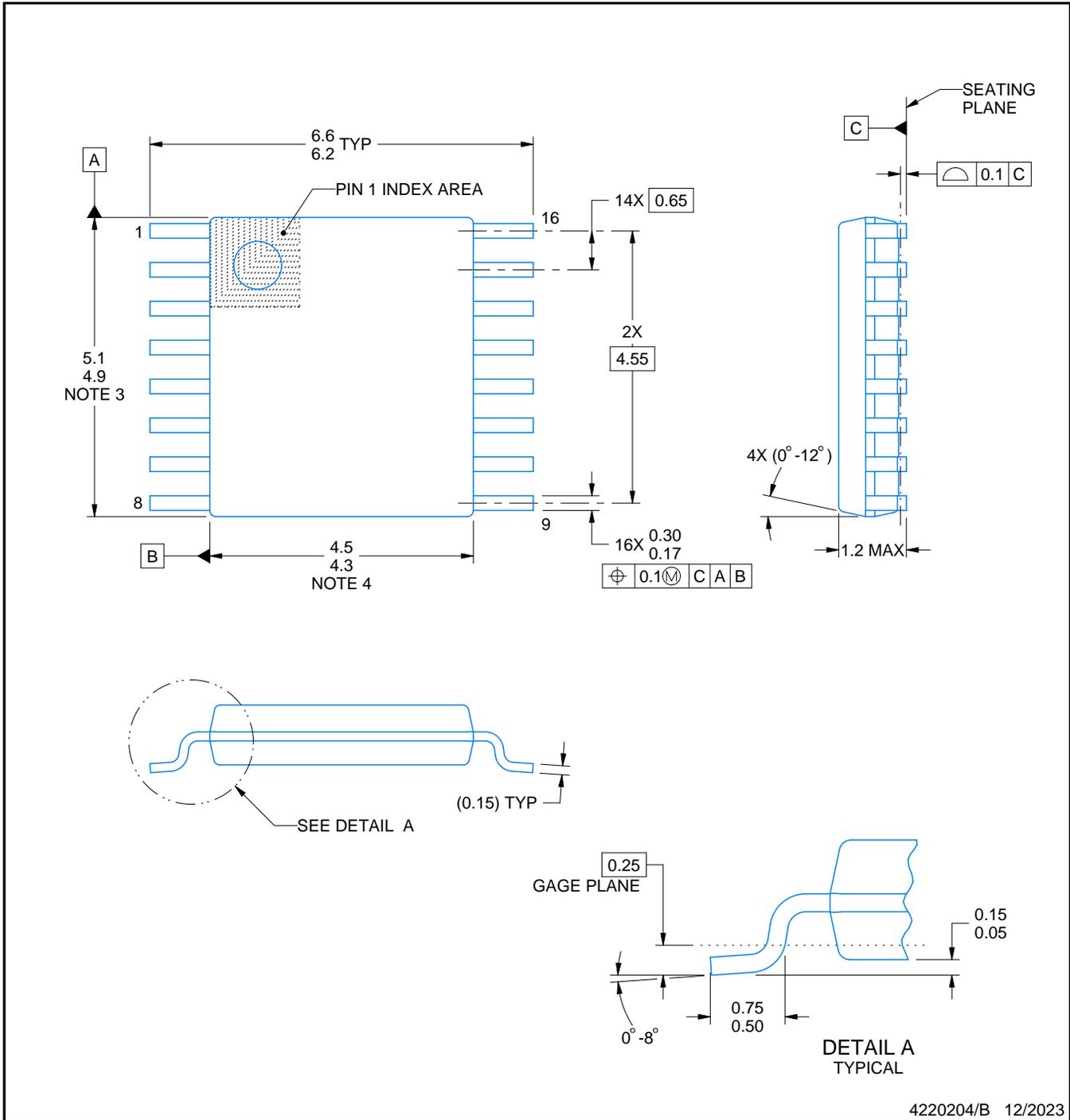
4220204/B   12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

16X (1.5)

SYMM

1

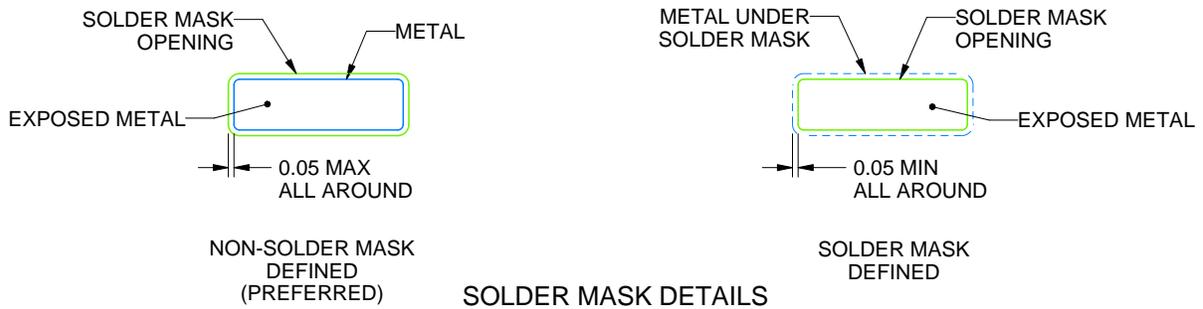16X (0.45)

(R0.05) TYP

16

SYMM

14X (0.65)

8

9

(5.8)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

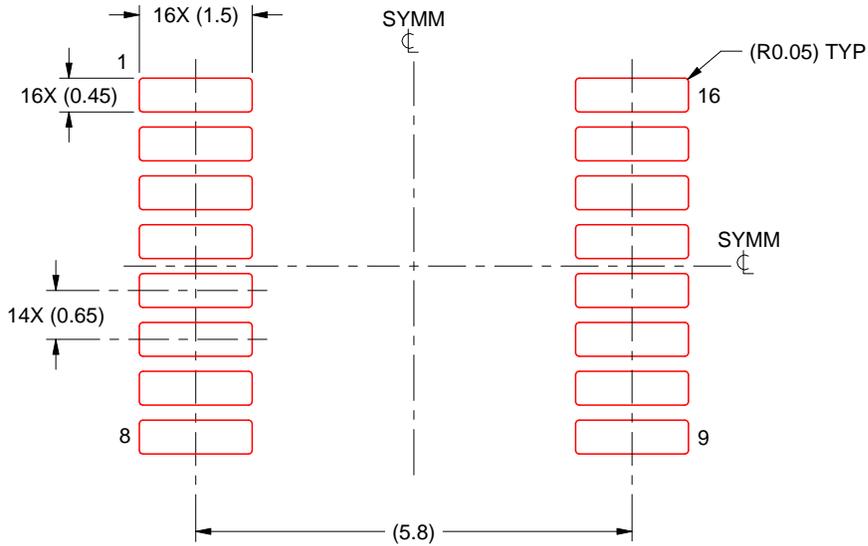4220204/B   12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

16X (1.5)

SYMM

1

16X (0.45)

(R0.05) TYP

16

SYMM

14X (0.65)

8

9

(5.8)

SOLDER PASTE EXAMPLE
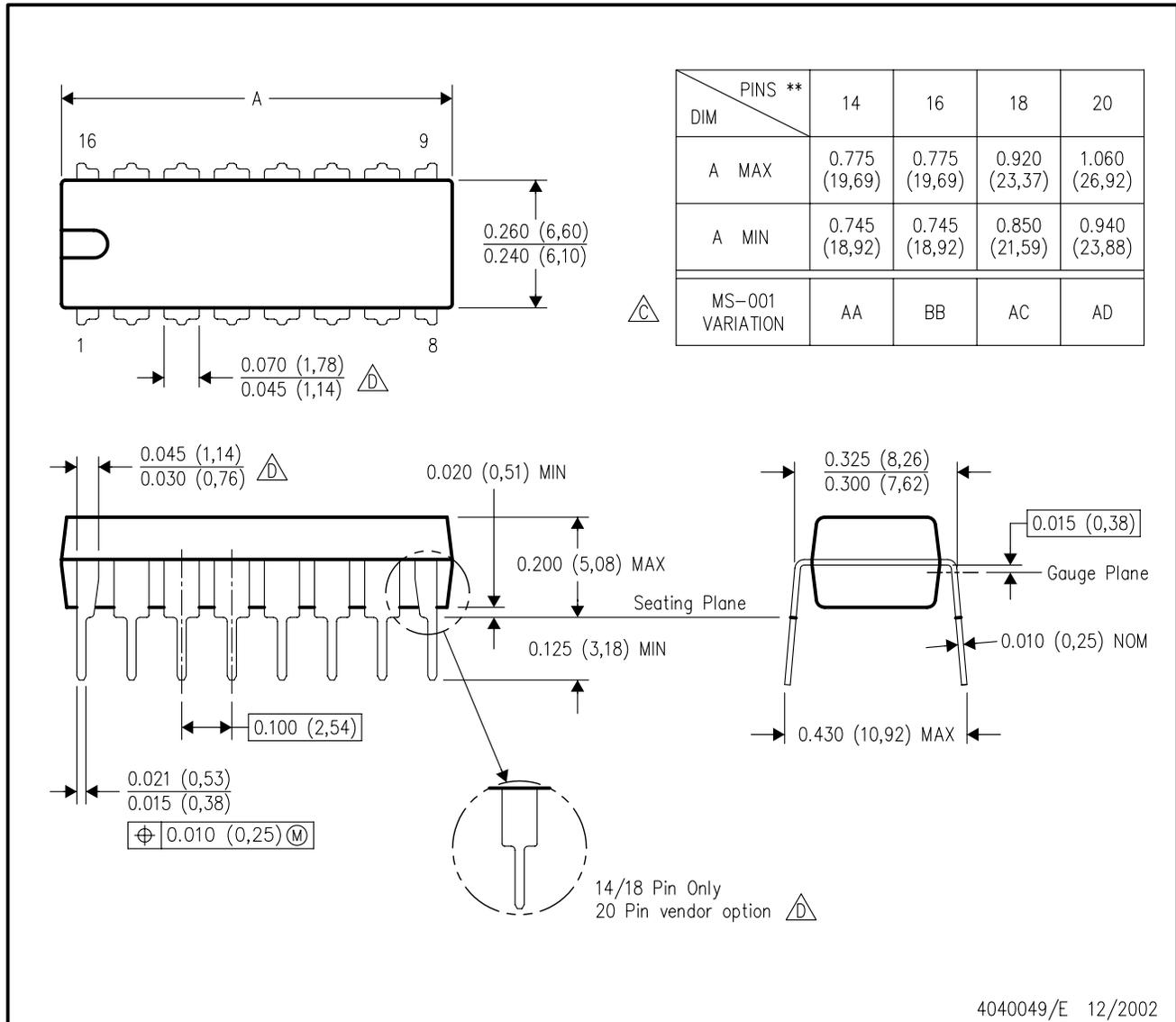BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B   12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R−PDIP−T**)
16 PINS SHOWN

PLASTIC DUAL−IN−LINE PACKAGE

PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

A

16   9

$\dfrac{0.260\ (6,60)}{0.240\ (6,10)}$

1   8

$\dfrac{0.070\ (1,78)}{0.045\ (1,14)}$ △D

$\dfrac{0.045\ (1,14)}{0.030\ (0,76)}$ △D

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

$\dfrac{0.021\ (0,53)}{0.015\ (0,38)}$

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option △D

$\dfrac{0.325\ (8,26)}{0.300\ (7,62)}$

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

△C

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
    △C Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
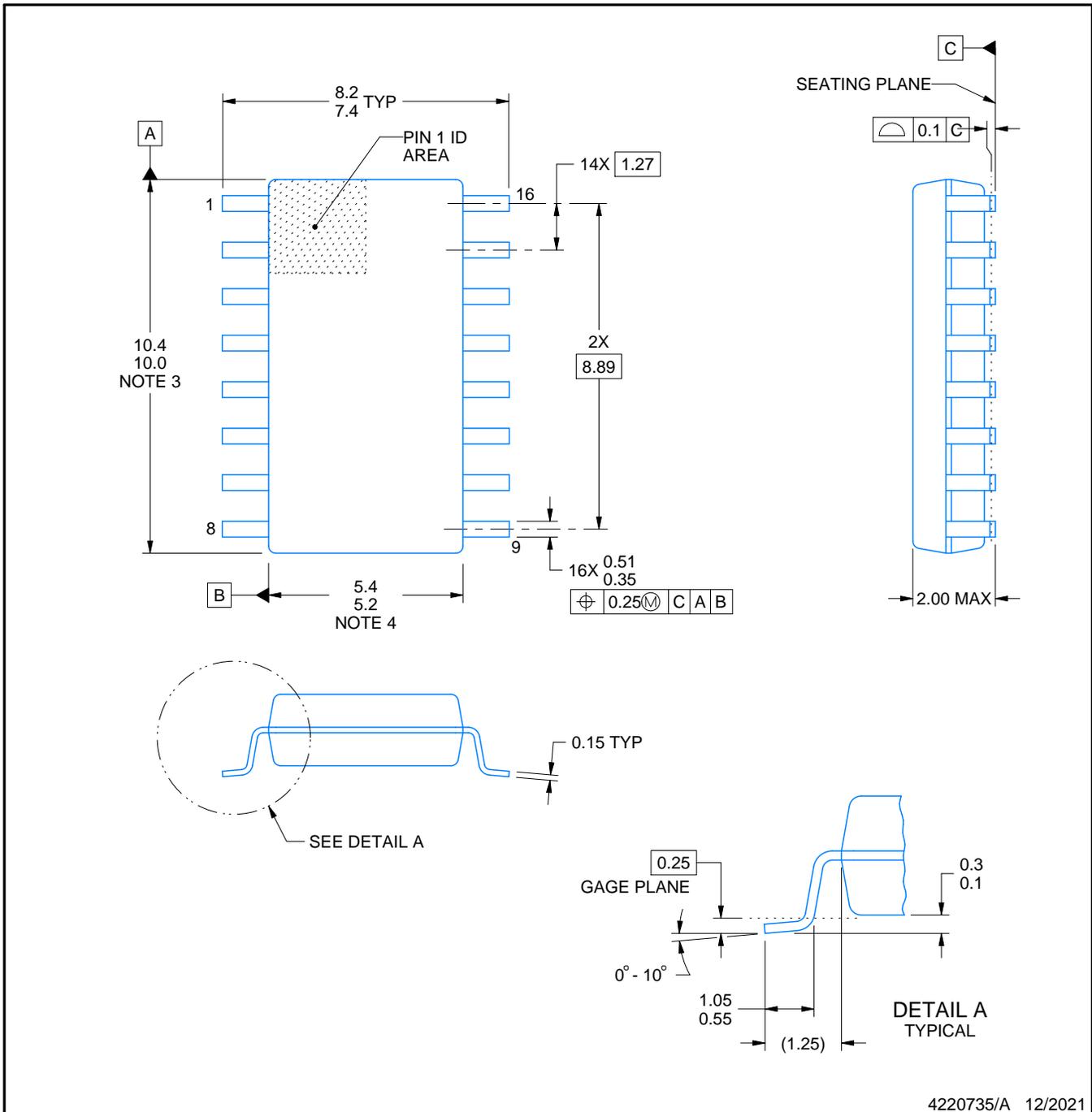   △D The 20 pin end lead shoulder width is a vendor option, either half or full width.

PIN 1 ID AREA

8.2 / 7.4 TYP

A

14X [1.27]

16

2X [8.89]

10.4 / 10.0 NOTE 3

1

8

9

16X 0.51 / 0.35

⊕ | 0.25Ⓜ | C | A | B

B

5.4 / 5.2 NOTE 4

C

SEATING PLANE

◠ | 0.1 | C

2.00 MAX

SEE DETAIL A

0.15 TYP

0.25

GAGE PLANE

0.3 / 0.1

0° - 10°

1.05 / 0.55

(1.25)

DETAIL A
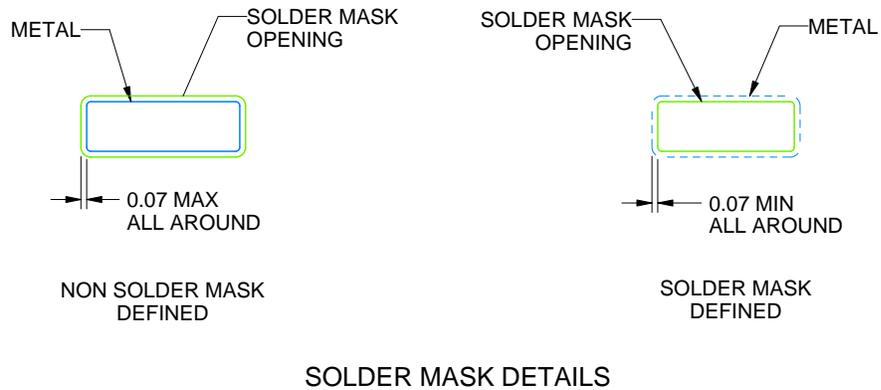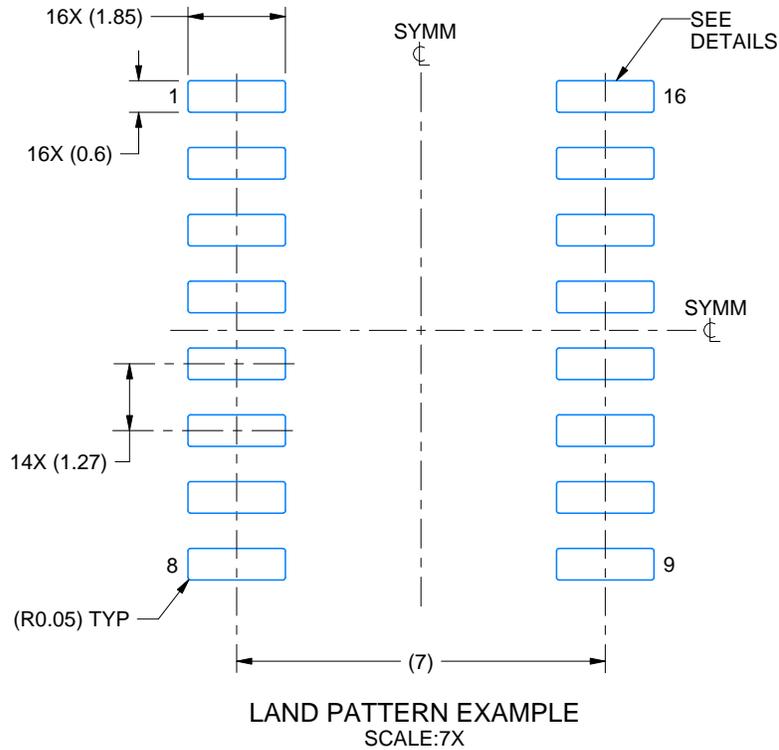TYPICAL

4220735/A   12/2021

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

16X (1.85)

SYMM

SEE DETAILS

1

16

16X (0.6)

SYMM

14X (1.27)

8

9

(R0.05) TYP

(7)

LAND PATTERN EXAMPLE
SCALE:7X

METAL

SOLDER MASK OPENING

SOLDER MASK OPENING

METAL

0.07 MAX
ALL AROUND

0.07 MIN
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A   12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

16X (1.85)

SYMM
℄

1

16

16X (0.6)

SYMM
℄

14X (1.27)

8

9

(R0.05) TYP

(7)
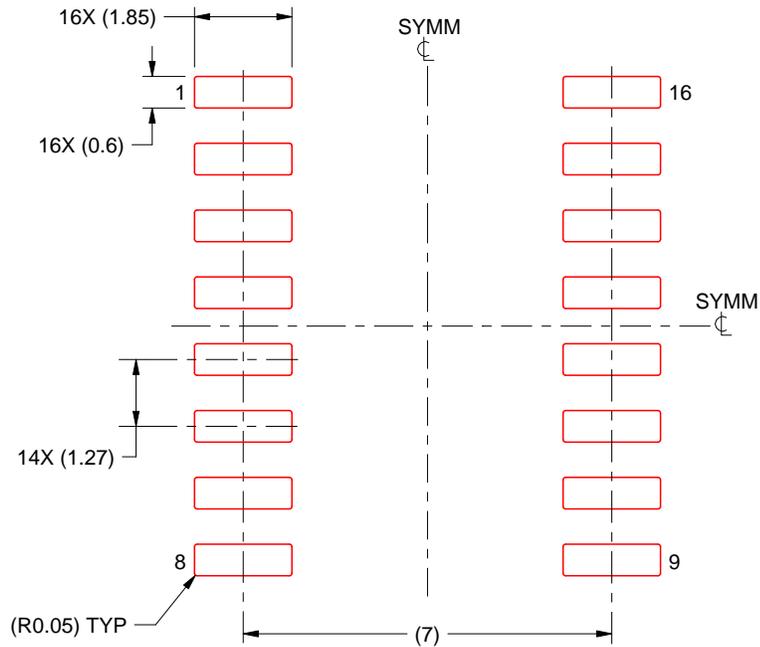
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A   12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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