

CD4059A Types

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V _{DD}) Voltages referenced to V _{SS} Terminal)	-0.5V to +15V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5V to V _{DD} +0.5V
POWER DISSIPATION PER PACKAGE (P _D):	
For T _A = -55°C to +100°C	500mW
For T _A = +100°C to +125°C	Derate Linearly to 100mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T _A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100mW
OPERATING-TEMPERATURE RANGE (T _A)	-55°C to +125°C
STORAGE TEMPERATURE RANGE (T _{stg})	-85°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max	

OPERATING CONDITIONS AT T_A = 25°C (Unless otherwise specified)

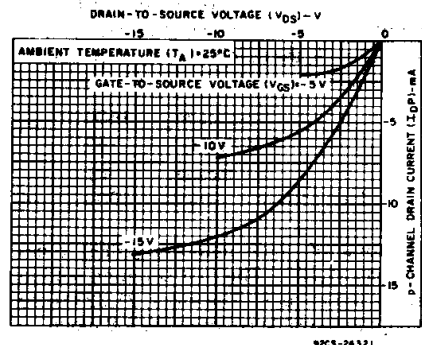
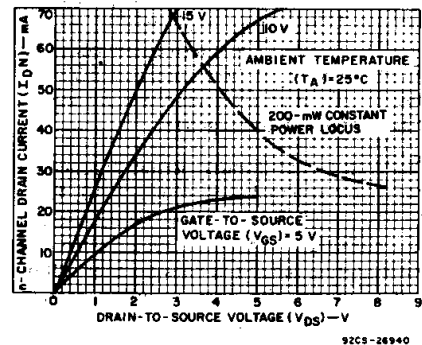
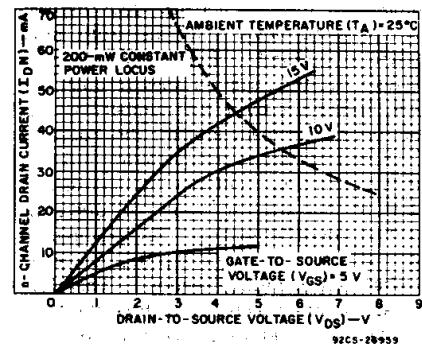
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	V _{DD}	Min.	Max.	Units
Supply Voltage Range (over full temp. range)	-	3	12	V
Clock Pulse Width	5	200	-	ns
Clock Input Frequency	10	-	1.5	MHz
Clock Input Rise and Fall Time	5	-	15	μs

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits							Units
	V _O (V)	V _{IN} (V)	V _{DD} (V)	-55°	-40°	+85°	+125°	+25°			
								Min.	Typ.	Max.	
Quiescent Device Current, I _L Max.			5	10	10	700	300	-	0.02	10	μA
			10	20	20	200	400	-	0.02	20	
			15	-	-	-	-	-	-	500	
Output Voltage:											V
	Low Level, V _{OL} Max.	0.5	5		0.05				0	0.05	
	High Level, V _{OH} Min.	0.5	5		4.95				4.95	5	
		0.10	10		9.95				9.95	10	
Noise Immunity:											V
	Inputs Low, V _{NL} Min.		5		1.5			1.5	2.25	-	
	Inputs High, V _{NH} Min.		10		3			3	4.5	-	
			5		1.5			1	2.25	-	
Noise Margin:											V
	Inputs Low, V _{NML} Min.	4.5	5				1				
	Inputs High, V _{NMH} Min.	9	10				1				
		0.5	5				1				
Output Drive Current:											mA
	N-Channel (Sink) I _{DN} Min.	0.4	5	2.5	2.3	1.6	1.4	2	4	-	
		0.5	10	5	4.7	3.3	2.8	4	9	-	
	P-Channel (Source) I _{DP} Min.	2.5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	-	
	4.6	5	-0.5	-0.45	-0.36	-0.3	-0.4	-0.8	-		
	9.5	10	-1.1	-1	-0.75	-0.65	-0.9	-1.8	-		
Input Leakage Current: * I _{IL} , I _{IH} Max.			15			±1			±10 ⁻⁵	±1	μA

* Any Input



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DYNAMIC ELECTRICAL CHARACTERISTICS AT $T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$, Input $t_r, t_f = 20\text{ ns}$, $R_L = 200\text{ k}\Omega$

CHARACTERISTIC	CONDITIONS V_{DD} (V)	LIMITS ALL PACKAGES			UNITS
		Min.	Typ.	Max.	
Propagation-Delay Time: t_{PHL} , t_{PLH}	5	—	180	360	ns
	10	—	90	180	
Transition Time:	t_{THL}	5	—	35	ns
		10	—	20	
	t_{TLH}	5	—	100	
		10	—	50	
Maximum Clock Input Frequency, f_{CL}	5	1.5	3	MHz	
	10	3	6		
Average Input Capacitance, C_i (any input)	—	—	5	—	pF

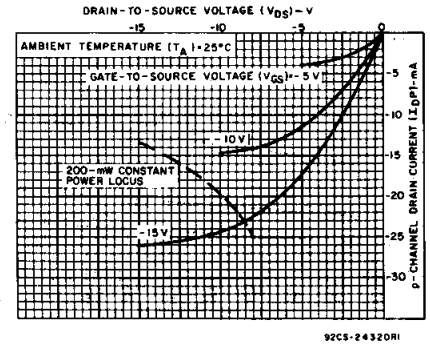


Fig.6 – Typical output p-channel drain characteristics.

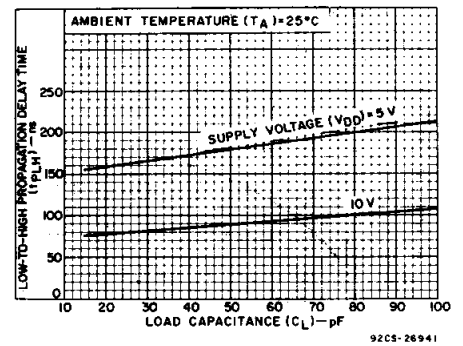


Fig.7 – Typical low-to-high propagation delay time vs. load capacitance.

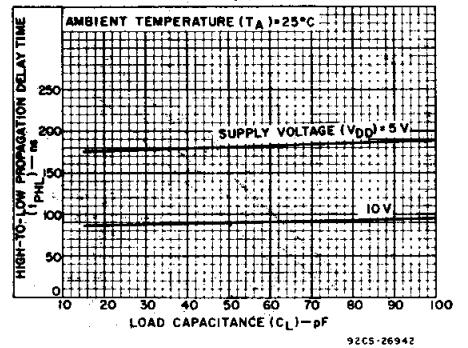


Fig.8 – Typical high-to-low propagation delay time vs. load capacitance.

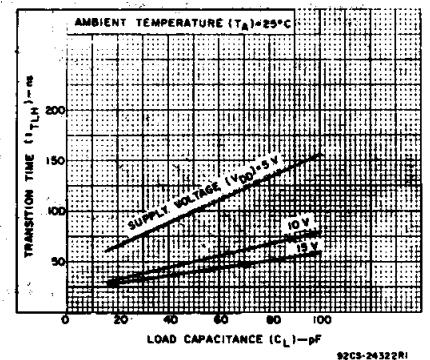
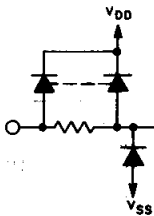
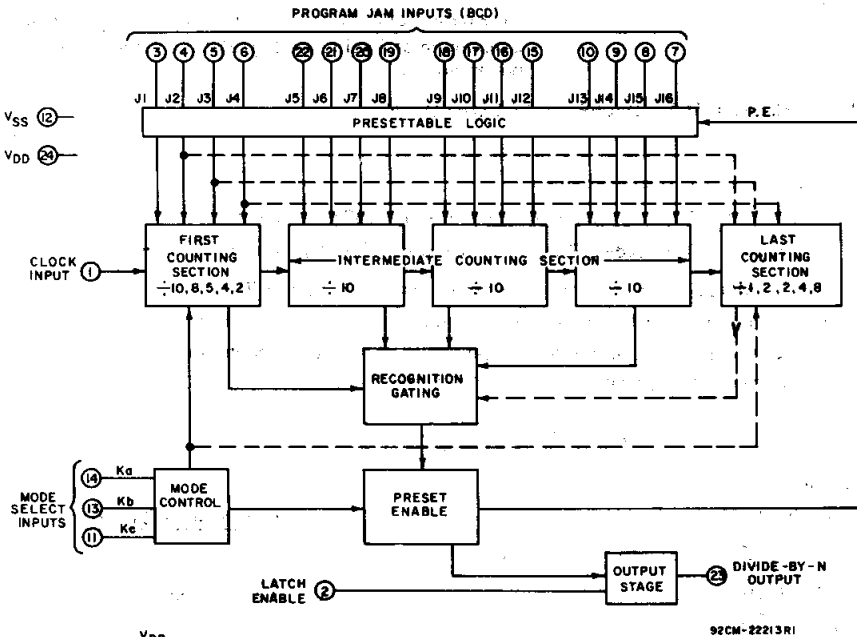


Fig.9 – Typical low-to-high transition time vs. load capacitance.



ALL INPUTS (TERMS. 1-11, 13-22) PROTECTED BY CMOS PROTECTION NETWORK

Fig.5 – Functional block diagram.

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COMMERCIAL CMOS
SPECIAL FUNCTION ICs

CD4059A Types

TABLE I

MODE SELECT INPUT			FIRST COUNTING SECTION			LAST COUNTING SECTION			COUNTER RANGE	
									DESIGN	EXTENDED
Ka	Kb	Kc	MODE	Can be preset to a max of:	Jam [▲] inputs used:	MODE	Can be preset to a max of:	Jam [▲] inputs used:	Max.	Max.
			Di-vides by:			Di-vides by:			Max.	Max.
1	1	1	2	1	J1	8	7	J2,J3,J4	15,999	17,331
0	1	1	4	3	J1,J2	4	3	J3,J4	15,999	18,663
1	0	1	5 [#]	4	J1,J2,J3	2	1	J4	9,999	13,329
0	0	1	8	7	J1,J2,J3	2	1	J4	15,999	21,327
1	1	0	10	9	J1,J2,J3,J4	1	0	—	9,999	16,659
X	0	0	MASTER PRESET			MASTER PRESET			—	—

X = Don't Care

▲ J1 = Least significant bit.

J4 = Most significant bit.

Operation in the ÷5 mode (1st counting section) requires going through the Master Preset mode prior to going into the ÷5 mode. At power turn-on, kc must be a logic "0" for a period of 3 input clock pulses after V_{DD} reaches a minimum of 3 volts. See Fig. 21 for a suggested external preset circuit.

HOW TO PRESET THE CD4059A TO DESIRED ÷ N

The value N is determined as follows:

$$N = [\text{MODE}^*] \cdot [1000 \times \text{Decade 5 Preset} + 100 \times \text{Decade 4 Preset} + 10 \times \text{Decade 3 Preset} + 1 \times \text{Decade 2 Preset}] + \text{Decade 1 Preset} \quad (1)$$

* MODE = First counting section divider (10, 8, 5, 4 or 2)

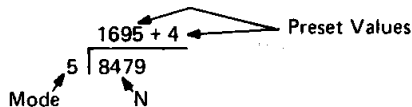
To calculate preset values for any N count, divide the N count by the Mode.

The resultant is the corresponding preset values of the 5th through 2nd decade with the remainder being equal to the 1st decade value.

$$\text{Preset Value} = \frac{N}{\text{Mode}} \quad (2)$$

Examples:

A) N = 8479, Mode = 5



MODE SELECT = 5

Ka Kb Kc
1 0 1

PROGRAM JAM INPUTS (BCD)

4				1				5				9				6			
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16				
0	0	1	1	1	0	1	0	1	0	0	1	0	1	1	0				

To verify the results use equation 1 :

$$N = 5 (1000 \times 1 + 100 \times 6 + 10 \times 9 + 1 \times 5) + 4$$

$$N = 8479$$

MODE SELECT = 8

B) N = 12382, Mode = 8

$$\begin{array}{r} 1547 + 6 \\ 8 \overline{) 12382} \end{array}$$

Ka Kb Kc
0 0 1

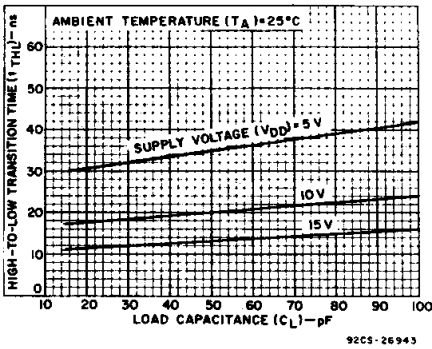


Fig.10 – Typical high-to-low transition time vs. load capacitance.

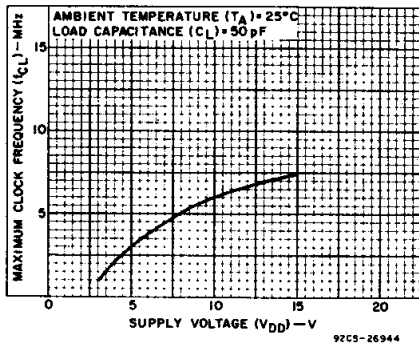


Fig.11 – Typical max. clock frequency vs. supply voltage.

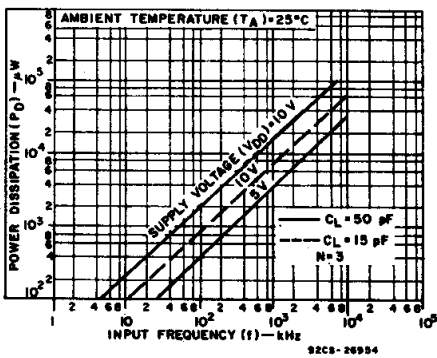


Fig.12 – Typical power dissipation vs. input frequency.

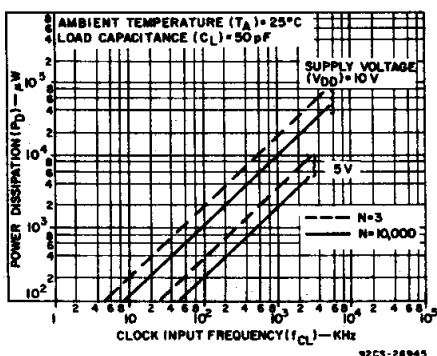


Fig.13 – Typical power dissipation vs. clock input frequency.

CD4059A Types

PROGRAM JAM INPUTS																			
6				1				7				4				5			
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16				
0	1	1	1	1	1	1	0	0	0	1	0	1	0	1	0				

To verify:

$$N = 8 (1000 \times 1 + 100 \times 5 + 10 \times 4 + 1 \times 7) + 6$$

$$N = 12382$$

MODE SELECT = 10

C) N = 8479, Mode = 10

$$10 \overline{) 08479} \\ \underline{80} \\ 47 \\ \underline{40} \\ 79$$

Ka Kb Kc
1 1 0

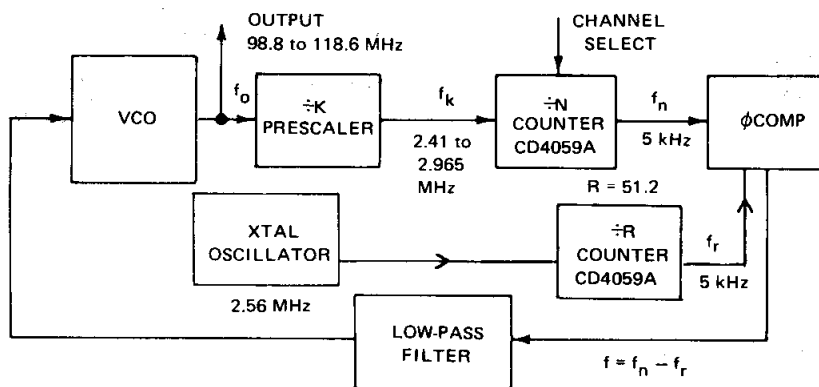
PROGRAM JAM INPUTS															
9				7				4				8			
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16
1	0	0	1	1	1	1	0	0	0	1	0	0	0	0	1

To Verify:

$$N = 10 (1000 \times 0 + 100 \times 8 + 10 \times 4 + 1 \times 7) + 9$$

$$N = 8479$$

DIGITAL PHASE-LOCKED LOOP (PLL) FOR FM BAND SYNTHESIZER



1) Calculating Min & Max "N" Values :

Output Freq. Range (f_o) = 98.8 to 118.6 MHz

Channel Spacing Freq. (f_c) = 200 kHz

Division Factor (k) = 40

$$\text{Reference Freq. } (f_r) = \frac{f_c}{k} = \frac{200}{40} \text{ kHz} = 5 \text{ kHz}$$

$$f_k = \frac{f_o}{40} : f_{k\text{Max.}} = \frac{118.6 \text{ MHz}}{40} = 2.965 \text{ MHz}; f_{k\text{Min.}} = \frac{98.8 \text{ MHz}}{40} = 2.47 \text{ MHz}$$

$$\therefore N = \frac{f_o}{f_c}$$

$$N_{\text{Max}} = \frac{118.6 \text{ MHz}}{200 \text{ kHz}} = 593$$

$$N_{\text{Min}} = \frac{98.8 \text{ MHz}}{200 \text{ kHz}} = 494$$

$$R = \frac{2.56 \text{ MHz}}{5 \text{ kHz}} = 512$$

"CASCADING" VIA OTHER COUNTERS

Fig. 14 shows a BCD-switch compatible arrangement suitable for $\div 8$ and $\div 5$ modes, which can be adapted, with slight changes, to the other divide-by-modes. In order to be able to preset to any number from three to about 256,000, while preserving the BCD-switch compatible character of the jam inputs, a rather complex cascading scheme is required. Such a cascading scheme is necessary because the CD4059A can never be preset to a count less than 3 and logic is needed to detect the condition that one of the numbers to be preset in the CD4059A is rather small. In order to simplify the detection logic, only that condition is detected where the jam inputs to terminals 6, 7, and 9 would be low during one count. If such a condition is detected, and if at least 1 is expected to be jammed into the MSB counter, the detection logic removes one from the number to be jammed into the MSB counter (with a place value of 2000 times the divide-by-mode) and jams the same 2000 into the CD4059A by forcing terminals 6, 7, and 9 high.

The clock of the CD4013A may be driven directly from the output of the CD4059A, as shown by dashed option (1), or by the inverted output of the CD4059A, option (2). If option (2) is used the CD4029A cannot count cycles shorter than 3. If option (1) is used propagation delay problems may occur at high counting speeds.

The general circuit in Fig.14 can be simplified considerably if the range of the cascaded counters does not have to start at a very low value. Fig.15 shows an arrangement in the $\div 4$ mode, where the counting range extends in a BCD-switch compatible manner from 88,003 to 103,999. The arrangement shown in Fig.15 is easy to follow; once during each cycle, the less significant digits are jammed in (14,712 in this case) and then 11,000 (4×2750) is jammed in eight times in succession, by forcing jam inputs high or low, as required.

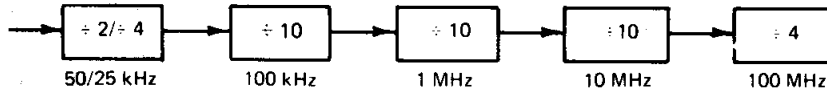
Numbers larger than the extended counter range can also be produced by cascading the CD4059A with some other counting device. Fig.16 shows such an arrangement where only one fixed divide-by number is desired which is close to three times the extended counter range as shown in the last column of Table I. The dual flip-flop wired to produce a $\div 3$ count, can be replaced by other counters such as the CD4029, CD4510, CD4516, CD4017, or the CD4022. In Fig.16 the $\div N$ subsystem is preset once to a number smaller than the desired divide-by number. This smaller number represents the less significant digits of the divide-by number. The subsystem is then preset one or more times to a round number (e.g. 1000, 2000) and multiplied by the number of the divide-by mode ($\div 2$ in the example of Fig.16). It is important that the second counting device has an output that is high or low, as the case may be, during only one of its counting states.

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CD4059A Types

2) ÷ N Counter Configuration for UHF – 220 to 400 MHz

Channel Spacing: 50 kHz or 25 kHz

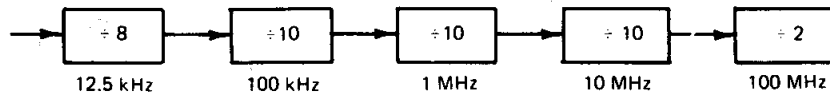


$$N_{Max} = \frac{400 \text{ MHz}}{25 \text{ kHz}} = 16,000 \quad N_{Max} = \frac{400 \text{ MHz}}{50 \text{ kHz}} = 8,000$$

$$N_{Min} = \frac{220 \text{ MHz}}{25 \text{ kHz}} = 8,800 \quad N_{Min} = \frac{220 \text{ MHz}}{50 \text{ kHz}} = 4,400$$

3) ÷ N Counter Configuration to VHF – 116 MHz

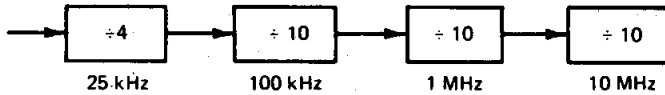
Channel Spacing = 12.5 kHz



$$N_{Max} = \frac{160 \text{ MHz}}{12.5 \text{ kHz}} = 12,800 \quad N_{Min} = \frac{116 \text{ MHz}}{12.5 \text{ kHz}} = 9,300$$

4) ÷ N Counter Configuration for VHF – 30 to 80 MHz

Channel Spacing: 25 kHz

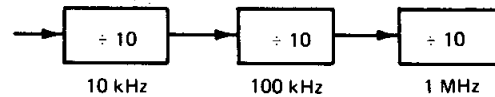


$$N_{Max} = \frac{80 \text{ MHz}}{25 \text{ kHz}} = 3,200$$

$$N_{Min} = \frac{30 \text{ MHz}}{25 \text{ kHz}} = 1,200$$

5) ÷ N Counter Configuration for AM – 995 to 2055 kHz

Channel Spacing = 10 kHz



$$N_{Max} = \frac{2055 \text{ kHz}}{10 \text{ kHz}} = 205$$

$$N_{Min} = \frac{995 \text{ kHz}}{10 \text{ kHz}} = 99$$

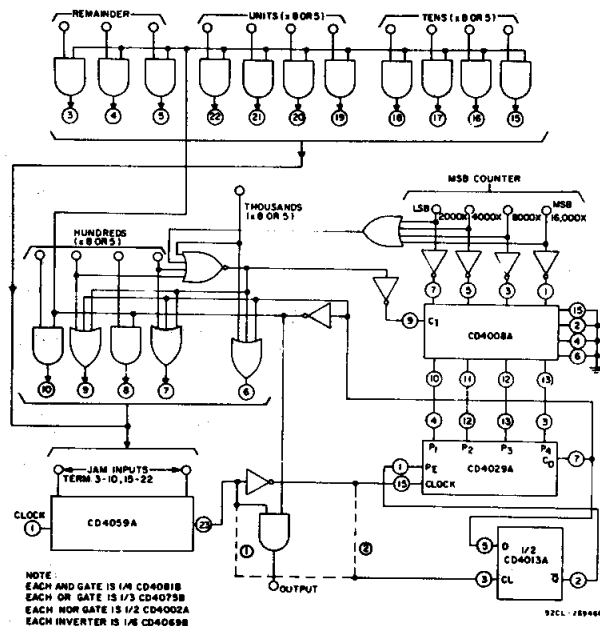
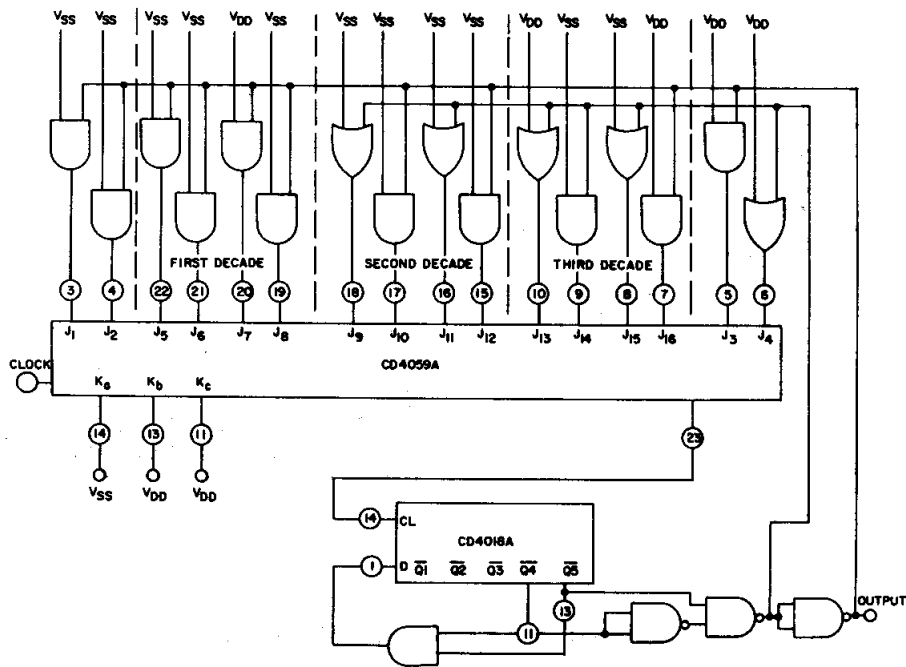


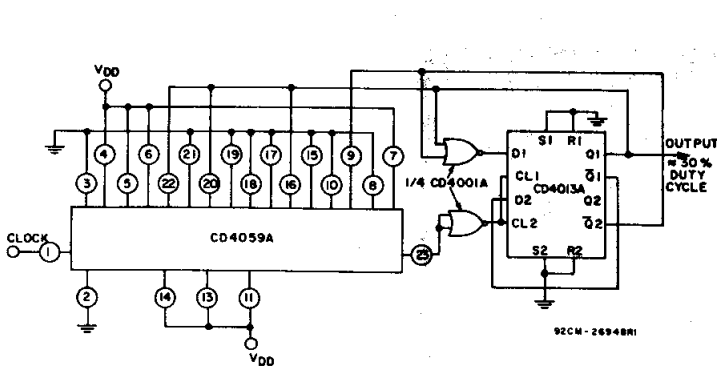
Fig. 14 – BCD switch-compatible ÷N system of the most general kind.

CD4059A Types



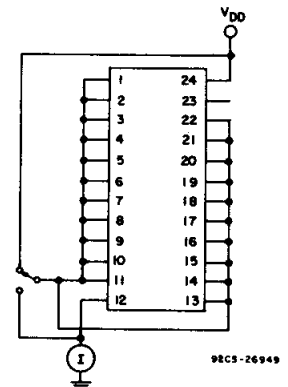
92CL-26947

Fig. 15 — Dividing by any number from 88,003 to 103,999.



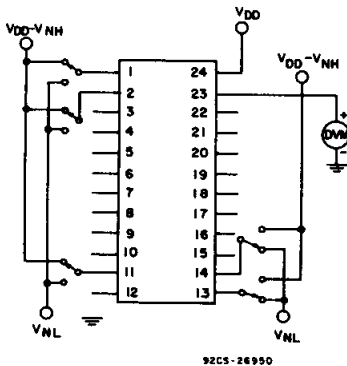
92CM-26948R1

Fig. 16 — Division by 47,690 in $\div 2$ mode.



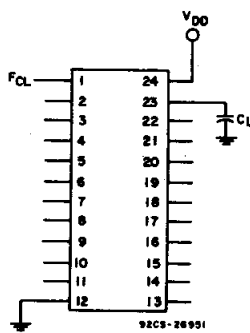
92CS-26949

Fig. 17 — Quiescent device current test circuit.



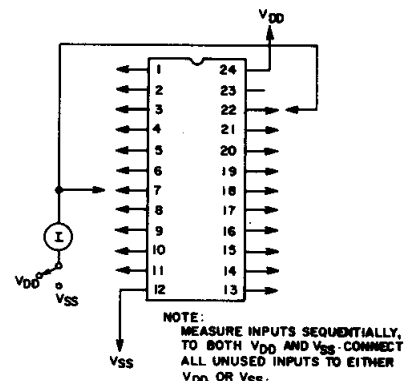
92CS-26950

Fig. 18 — Noise immunity test circuit.



92CS-26951

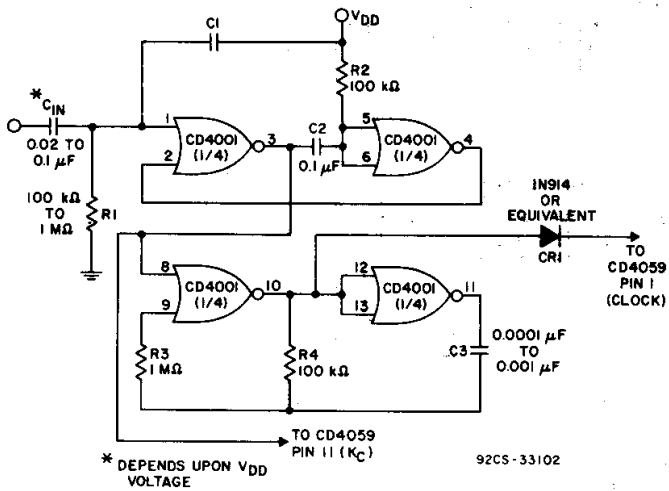
Fig. 19 — Power dissipation test circuit (all \div modes).



92CS-26952

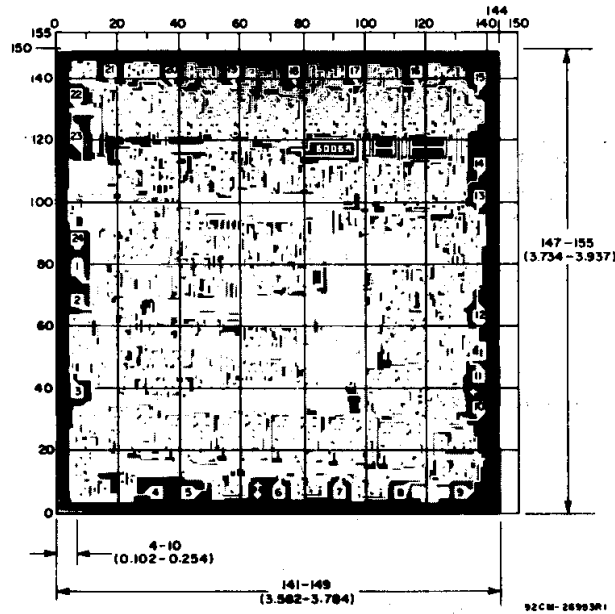
Fig. 20 — Input leakage current test circuit.

CD4059A Types



For changing from any mode other than mode 5 (with power on), apply positive pulse to C_{in} . This circuit automatically selects master preset mode ($K_a = 0, K_c = 0$) before going into the select conditions for mode 5 ($K_a = 1, K_b = 0, K = 1$). The selection of C_1 and C_2 is critical! C_1 is determined by the V_{DD} voltage--the lower V_{DD} 's need larger C_1 's. C_2 must be $0.1 \mu F$ or larger.

Fig.21 - CD4059A mode 5 power on master preset circuit.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Dimensions and pad layout for CD4059AH.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD4059AD3	Active	Production	CDIP SB (JD) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4059AD/3
CD4059AD3.A	Active	Production	CDIP SB (JD) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4059AD/3
CD4059AM	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4059AM
CD4059AM.A	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4059AM
CD4059AMG4	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4059AM

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF CD4059A, CD4059A-MIL :

- Catalog : [CD4059A](#)
- Military : [CD4059A-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TUBE

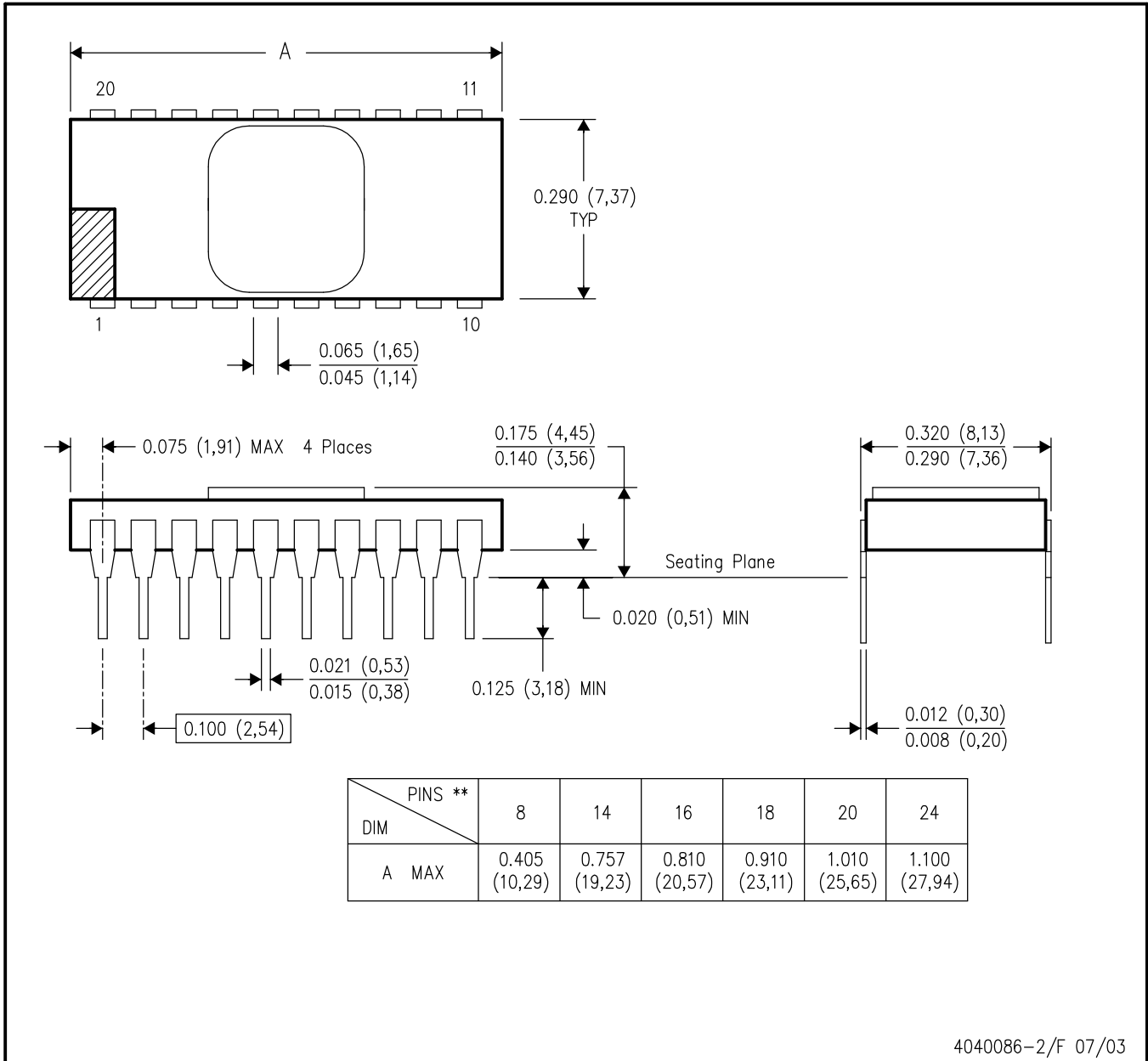

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD4059AM	DW	SOIC	24	25	506.98	12.7	4826	6.6
CD4059AM.A	DW	SOIC	24	25	506.98	12.7	4826	6.6
CD4059AMG4	DW	SOIC	24	25	506.98	12.7	4826	6.6

JD (R-CDIP-T**)

CERAMIC SIDE-BRAZE DUAL-IN-LINE PACKAGE

20 PINS SHOWN



4040086-2/F 07/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within MIL STD 1835 CDIP2 - T8, T14, T16, T18, T20 and T24 respectively.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AD.

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