

CD4070B, CD4077B

CMOS Quad Exclusive-OR and Exclusive-NOR Gate

Features

- High-Voltage Types (20V Rating)
- CD4070B - Quad Exclusive-OR Gate
- CD4077B - Quad Exclusive-NOR Gate
- Medium Speed Operation
 - $t_{PHL}, t_{PLH} = 65\text{ns}$ (Typ) at $V_{DD} = 10\text{V}$, $C_L = 50\text{pF}$
- 100% Tested for Quiescent Current at 20V
- Standardized Symmetrical Output Characteristics
- 5V, 10V and 15V Parametric Ratings
- Maximum Input Current of $1\mu\text{A}$ at 18V Over Full Package Temperature Range
 - 100nA at 18V and 25°C
- Noise Margin (Over Full Package Temperature Range)
 - 1V at $V_{DD} = 5\text{V}$, 2V at $V_{DD} = 10\text{V}$, 2.5V at $V_{DD} = 15\text{V}$
- Meets All Requirements of JEDEC Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Logical Comparators
- Adders/Subtractors
- Parity Generators and Checkers

Description

The Harris CD4070B contains four independent Exclusive-OR gates. The Harris CD4077B contains four independent Exclusive-NOR gates.

The CD4070B and CD4077B provide the system designer with a means for direct implementation of the Exclusive-OR and Exclusive-NOR functions, respectively.

Ordering Information

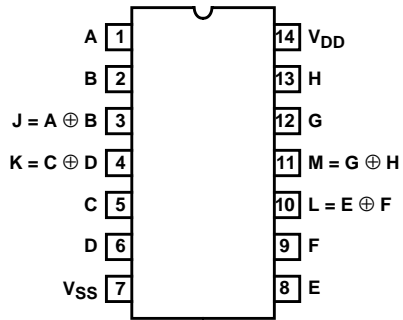
| PART NUMBER | TEMP. RANGE (°C) | PACKAGE |
|-------------|------------------|--------------|
| CD4070BE | -55 to 125 | 14 Ld PDIP |
| CD4070BF3A | -55 to 125 | 14 Ld CERDIP |
| CD4070BM | -55 to 125 | 14 Ld SOIC |
| CD4070BMT | -55 to 125 | 14 Ld SOIC |
| CD4070BM96 | -55 to 125 | 14 Ld SOIC |
| CD4070BNSR | -55 to 125 | 14 Ld SOP |
| CD4070BPW | -55 to 125 | 14 Ld TSSOP |
| CD4070BPWR | -55 to 125 | 14 Ld TSSOP |
| CD4077BE | -55 to 125 | 14 Ld PDIP |
| CD4077BF3A | -55 to 125 | 14 Ld CERDIP |
| CD4077BM | -55 to 125 | 14 Ld SOIC |
| CD4077BMT | -55 to 125 | 14 Ld SOIC |
| CD4077BM96 | -55 to 125 | 14 Ld SOIC |
| CD4077BNSR | -55 to 125 | 14 Ld SOP |
| CD4077BPW | -55 to 125 | 14 Ld TSSOP |
| CD4077BPWR | -55 to 125 | 14 Ld TSSOP |

NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

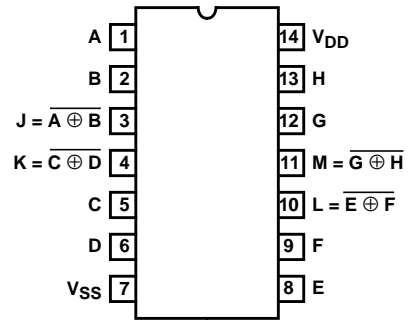
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Pinouts

CD4070B
(PDIP, Cerdip, SOIC, SOP, TSSOP)
TOP VIEW

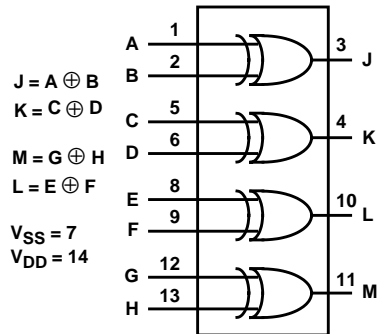


CD4077B
(PDIP, Cerdip, SOIC, SOP, TSSOP)
TOP VIEW

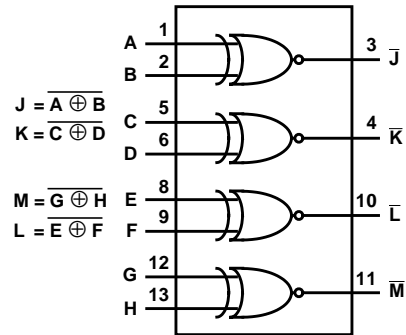


Functional Diagrams

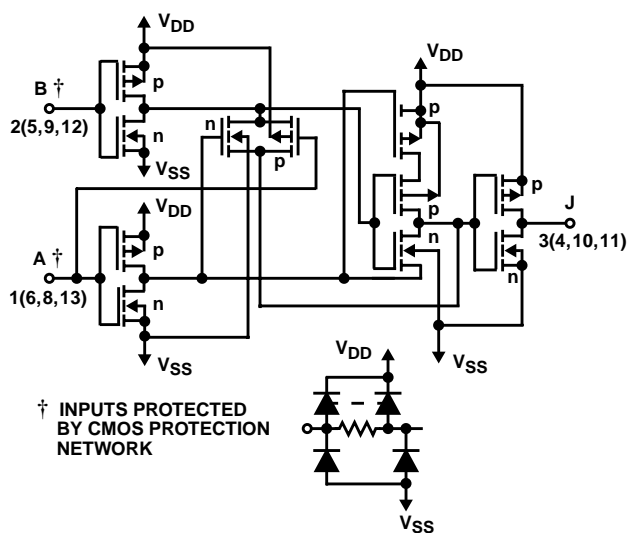
CD4070B



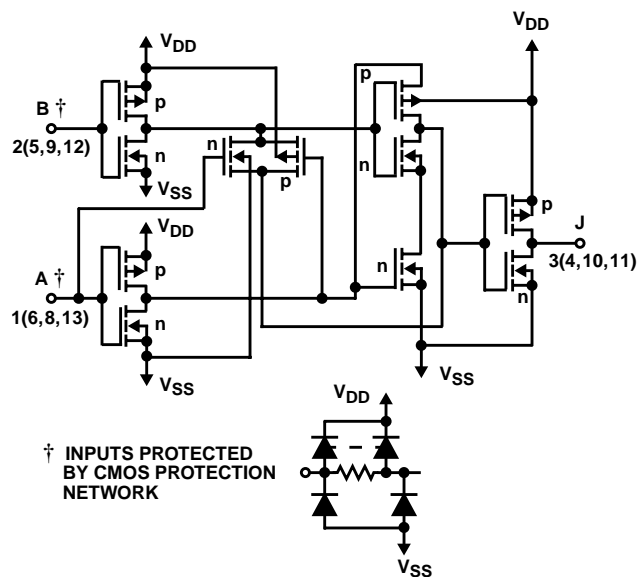
CD4077B



CD4070B, CD4077B



**FIGURE 1. SCHEMATIC DIAGRAM FOR CD4070B
(1 OF 4 IDENTICAL GATES)**



**FIGURE 2. SCHEMATIC DIAGRAM FOR CD4077B
(1 OF 4 IDENTICAL GATES)**

CD4070B TRUTH TABLE (1 OF 4 GATES)

| A | B | J |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 1 | 0 |

NOTE:
 1 = High Level
 0 = Low Level
 J = A ⊕ B

CD4077B TRUTH TABLE (1 OF 4 GATES)

| A | B | J |
|---|---|---|
| 0 | 0 | 1 |
| 1 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 1 | 1 |

NOTE:
 1 = High Level
 0 = Low Level
 J = A ⊕ B

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Absolute Maximum Ratings

DC Supply Voltage Range (V_{DD}) -0.5V to 20V
 Input Voltage Range, All Inputs -0.5V to V_{DD} 0.5V
 DC Input Current ± 10 mA

Operating Conditions

Temperature Range (T_A) -55°C to 125°C
 Supply Voltage Range (Typical) 3V to 18V

Thermal Information

Package Thermal Impedance, θ_{JA} (see Note 1):
 E (PDIP) Package 80°C/W
 M (SOIC) Package 86°C/W
 NS (SOP) Package 76°C/W
 PW (TSSOP) Package 113°C/W
 Maximum Junction Temperature (Hermetic Package or Die) . 175°C
 Maximum Junction Temperature (Plastic Package) 150°C
 Maximum Storage Temperature Range -65°C to 150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

| PARAMETER | CONDITIONS | | | LIMITS AT INDICATED TEMPERATURES (°C) | | | | | | | UNITS |
|--|--------------|-----------------|-----------------|---------------------------------------|-----------|---------|---------|-------|---------------|-----------|---------|
| | | | | -55 | -40 | 85 | 125 | 25 | | | |
| | V_O (V) | V_{IN} (V) | V_{DD} (V) | | | | | MIN | TYP | MAX | |
| Quiescent Device Current I_{DD} Max | - | 0, 5 | 5 | 0.25 | 0.25 | 7.5 | 7.5 | - | 0.01 | 0.25 | μ A |
| | - | 0, 10 | 10 | 0.5 | 0.5 | 15 | 15 | - | 0.01 | 0.5 | μ A |
| | - | 0, 15 | 15 | 1 | 1 | 30 | 30 | - | 0.01 | 1 | μ A |
| | - | 0, 20 | 20 | 5 | 5 | 150 | 150 | - | 0.02 | 5 | μ A |
| Output Low (Sink) Current I_{OL} Min | 0.4 | 0, 5 | 5 | 0.64 | 0.61 | 0.42 | 0.36 | 0.51 | 1 | - | mA |
| | 0.5 | 0, 10 | 10 | 1.6 | 1.5 | 1.1 | 0.9 | 1.3 | 2.6 | - | mA |
| | 1.5 | 0, 15 | 15 | 4.2 | 4 | 2.8 | 2.4 | 3.4 | 6.8 | - | mA |
| Output High (Source) Current I_{OH} Min | 4.6 | 0, 5 | 5 | -0.64 | -0.61 | -0.42 | -0.36 | -0.51 | -1 | - | mA |
| | 2.5 | 0, 5 | 5 | -2 | -1.8 | -1.3 | -1.15 | -1.6 | -3.2 | - | mA |
| | 9.5 | 0, 10 | 10 | -1.6 | -1.5 | -1.1 | -0.9 | -1.3 | -2.6 | - | mA |
| | 13.5 | 0, 15 | 15 | -4.2 | -4 | -2.8 | -2.4 | -3.4 | -6.8 | - | mA |
| Output Voltage: Low Level, V_{OL} Max | - | 0, 5 | 5 | 0.05 | 0.05 | 0.05 | 0.05 | - | 0 | 0.05 | V |
| | - | 0, 10 | 10 | 0.05 | 0.05 | 0.05 | 0.05 | - | 0 | 0.05 | V |
| | - | 0, 15 | 15 | 0.05 | 0.05 | 0.05 | 0.05 | - | 0 | 0.05 | V |
| Output Voltage: High Level, V_{OH} Min | - | 0, 5 | 5 | 4.95 | 4.95 | 4.95 | 4.95 | 4.95 | 5 | - | V |
| | - | 0, 10 | 10 | 9.95 | 9.95 | 9.95 | 9.95 | 9.95 | 10 | - | V |
| | - | 0, 15 | 15 | 14.95 | 14.95 | 14.95 | 14.95 | 14.95 | 15 | - | V |
| Input Low Voltage, V_{IL} Max | 0.5, 4.5 | - | 5 | 1.5 | 1.5 | 1.5 | 1.5 | - | - | 1.5 | V |
| | 1, 9 | - | 10 | 3 | 3 | 3 | 3 | - | - | 3 | V |
| | 1.5, 13.5 | - | 15 | 4 | 4 | 4 | 4 | - | - | 4 | V |
| Input High Voltage, V_{IH} Min | 0.5, 4.5 | - | 5 | 3.5 | 3.5 | 3.5 | 3.5 | 3.5 | - | - | V |
| | 1, 9 | - | 10 | 7 | 7 | 7 | 7 | 7 | - | - | V |
| | 1.5, 13.5 | - | 15 | 11 | 11 | 11 | 11 | 11 | - | - | V |
| Input Current, I_{IN} Max | - | 0, 18 | 18 | ± 0.1 | ± 0.1 | ± 1 | ± 1 | - | $\pm 10^{-5}$ | ± 0.1 | μ A |

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AC Electrical Specifications

$T_A = 25^\circ\text{C}$, Input $t_r, t_f = 20\text{ns}$, $C_L = 50\text{pF}$, $R_L = 200\text{k}\Omega$

| PARAMETER | SYMBOL | TEST CONDITIONS | LIMITS ON ALL TYPES | | UNITS |
|------------------------|--------------------|-----------------|---------------------|-----|-------|
| | | V_{DD} (V) | TYP | MAX | |
| Propagation Delay Time | t_{PHL}, t_{PLH} | 5 | 140 | 280 | ns |
| | | 10 | 65 | 130 | ns |
| | | 15 | 50 | 100 | ns |
| Transition Time | t_{THL}, t_{TLH} | 5 | 100 | 200 | ns |
| | | 10 | 50 | 100 | ns |
| | | 15 | 40 | 80 | ns |
| Input Capacitance | C_{IN} | Any Input | 5 | 7.5 | pF |

Typical Performance Curves

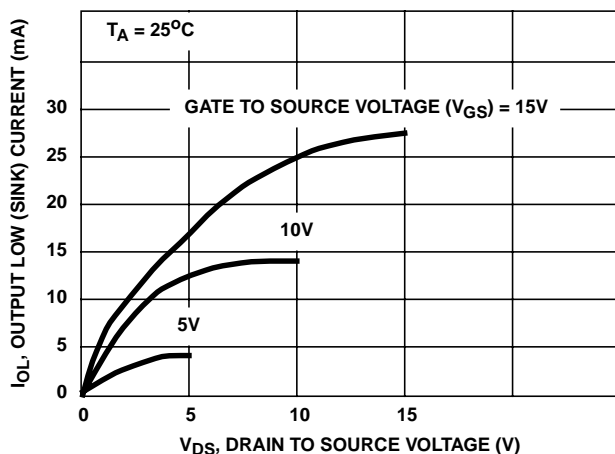


FIGURE 3. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

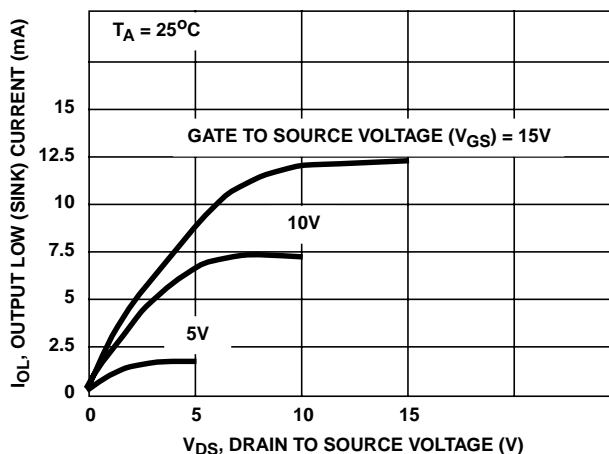


FIGURE 4. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

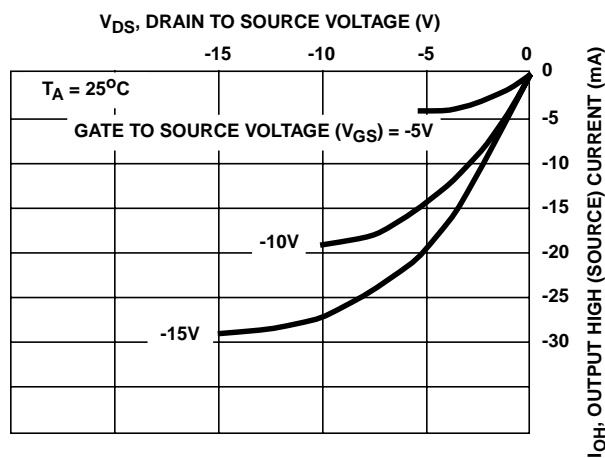


FIGURE 5. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

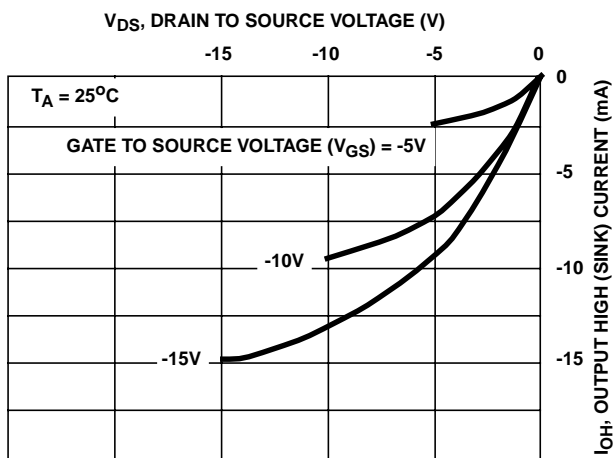


FIGURE 6. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

Typical Performance Curves (Continued)

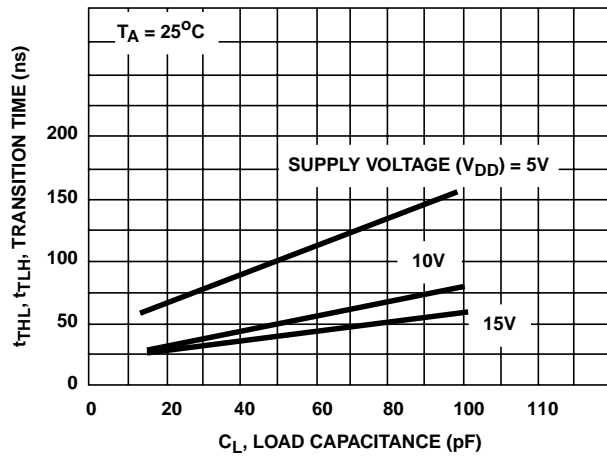


FIGURE 7. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

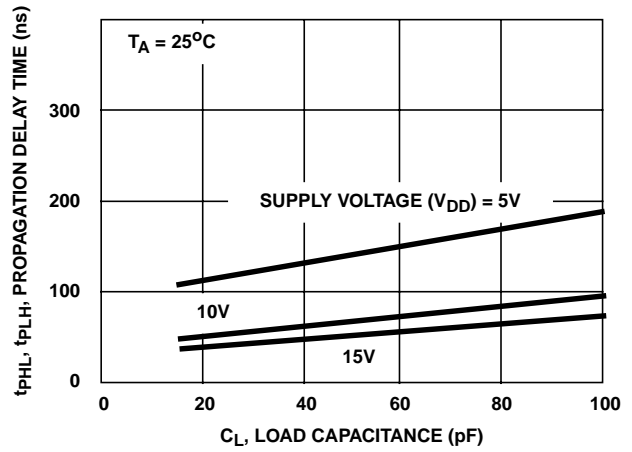


FIGURE 8. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE

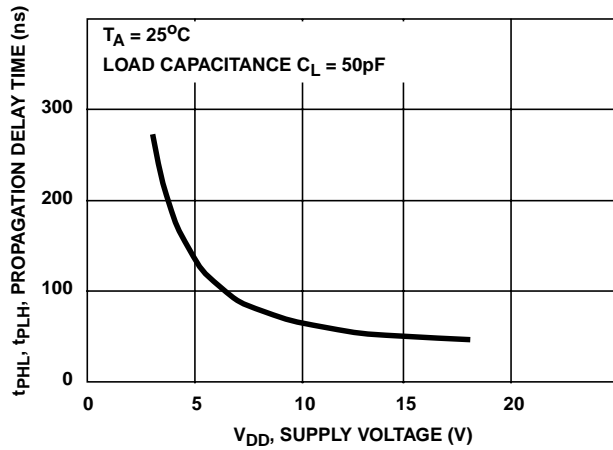


FIGURE 9. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF SUPPLY VOLTAGE

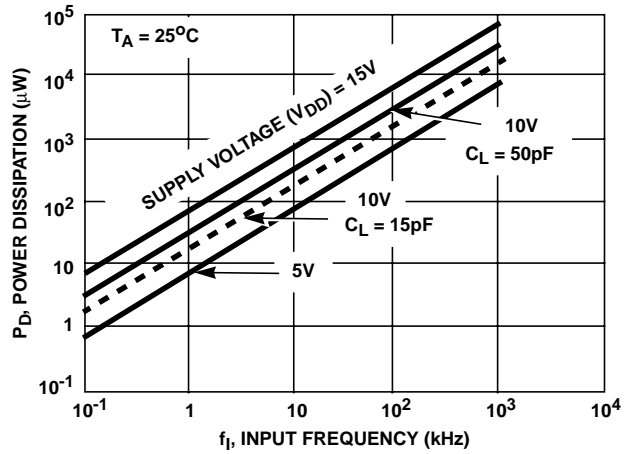


FIGURE 10. TYPICAL DYNAMIC POWER DISSIPATION AS A FUNCTION OF INPUT FREQUENCY

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| CD4070BE | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD4070BEE4 | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD4070BF | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type |
| CD4070BF3A | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type |
| CD4070BF3AS2534 | OBSOLETE | CDIP | J | 14 | | TBD | Call TI | Call TI |
| CD4070BM | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4070BM96 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4070BM96E4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4070BM96G4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4070BME4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4070BMG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4070BMT | ACTIVE | SOIC | D | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4070BMTE4 | ACTIVE | SOIC | D | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4070BMTG4 | ACTIVE | SOIC | D | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4070BNSR | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4070BNSRE4 | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4070BNSRG4 | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4070BPW | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4070BPWE4 | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4070BPWG4 | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4070BPWR | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4070BPWRE4 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4070BPWRG4 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4077BE | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD4077BEE4 | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD4077BF | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type |
| CD4077BF3A | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type |

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| CD4077BM | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4077BM96 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4077BM96E4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4077BM96G4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4077BME4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4077BMG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4077BMT | ACTIVE | SOIC | D | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4077BMTE4 | ACTIVE | SOIC | D | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4077BMTG4 | ACTIVE | SOIC | D | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4077BNSR | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4077BNSRE4 | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4077BNSRG4 | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4077BPW | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4077BPWE4 | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4077BPWG4 | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4077BPWR | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4077BPWRE4 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4077BPWRG4 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| JM38510/17203BCA | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS

compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD4070BM96 | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| CD4070BNSR | SO | NS | 14 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| CD4070BPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 7.0 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| CD4077BM96 | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| CD4077BNSR | SO | NS | 14 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| CD4077BPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 7.0 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD4070BM96 | SOIC | D | 14 | 2500 | 346.0 | 346.0 | 33.0 |
| CD4070BNSR | SO | NS | 14 | 2000 | 346.0 | 346.0 | 33.0 |
| CD4070BPWR | TSSOP | PW | 14 | 2000 | 346.0 | 346.0 | 29.0 |
| CD4077BM96 | SOIC | D | 14 | 2500 | 346.0 | 346.0 | 33.0 |
| CD4077BNSR | SO | NS | 14 | 2000 | 346.0 | 346.0 | 33.0 |
| CD4077BPWR | TSSOP | PW | 14 | 2000 | 346.0 | 346.0 | 29.0 |

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AB.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|----------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| CD4070BE | Active | Production | PDIP (N) 14 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD4070BE |
| CD4070BE.A | Active | Production | PDIP (N) 14 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD4070BE |
| CD4070BEE4 | Active | Production | PDIP (N) 14 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD4070BE |
| CD4070BF | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | CD4070BF |
| CD4070BF.A | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | CD4070BF |
| CD4070BF3A | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | CD4070BF3A |
| CD4070BF3A.A | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | CD4070BF3A |
| CD4070BM | Obsolete | Production | SOIC (D) 14 | - | - | Call TI | Call TI | -55 to 125 | CD4070BM |
| CD4070BM96 | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4070BM |
| CD4070BM96.A | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4070BM |
| CD4070BM96E4 | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4070BM |
| CD4070BMT | Obsolete | Production | SOIC (D) 14 | - | - | Call TI | Call TI | -55 to 125 | CD4070BM |
| CD4070BNSR | Active | Production | SOP (NS) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4070B |
| CD4070BNSR.A | Active | Production | SOP (NS) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4070B |
| CD4070BPW | Obsolete | Production | TSSOP (PW) 14 | - | - | Call TI | Call TI | -55 to 125 | CM070B |
| CD4070BPWR | Active | Production | TSSOP (PW) 14 | 2000 LARGE T&R | Yes | NIPDAU SN | Level-1-260C-UNLIM | -55 to 125 | CM070B |
| CD4070BPWR.A | Active | Production | TSSOP (PW) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM070B |
| CD4077BE | Active | Production | PDIP (N) 14 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD4077BE |
| CD4077BE.A | Active | Production | PDIP (N) 14 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD4077BE |
| CD4077BF | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | CD4077BF |
| CD4077BF.A | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | CD4077BF |
| CD4077BF3A | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | CD4077BF3A |
| CD4077BF3A.A | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | CD4077BF3A |
| CD4077BM | Obsolete | Production | SOIC (D) 14 | - | - | Call TI | Call TI | -55 to 125 | CD4077BM |
| CD4077BM96 | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4077BM |
| CD4077BM96.A | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4077BM |
| CD4077BMT | Obsolete | Production | SOIC (D) 14 | - | - | Call TI | Call TI | -55 to 125 | CD4077BM |
| CD4077BNSR | Active | Production | SOP (NS) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4077B |
| CD4077BNSR.A | Active | Production | SOP (NS) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4077B |

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|----------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|----------------------|
| CD4077BPW | Active | Production | TSSOP (PW) 14 | 90 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM077B |
| CD4077BPW.A | Active | Production | TSSOP (PW) 14 | 90 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM077B |
| JM38510/17203BCA | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 17203BCA |
| JM38510/17203BCA.A | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 17203BCA |
| M38510/17203BCA | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 17203BCA |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF CD4070B, CD4070B-MIL, CD4077B, CD4077B-MIL :

- Catalog : [CD4070B](#), [CD4077B](#)
- Military : [CD4070B-MIL](#), [CD4077B-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD4070BM96 | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| CD4070BNSR | SOP | NS | 14 | 2000 | 330.0 | 16.4 | 8.1 | 10.4 | 2.5 | 12.0 | 16.0 | Q1 |
| CD4070BPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| CD4070BPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| CD4077BM96 | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| CD4077BNSR | SOP | NS | 14 | 2000 | 330.0 | 16.4 | 8.1 | 10.4 | 2.5 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD4070BM96 | SOIC | D | 14 | 2500 | 353.0 | 353.0 | 32.0 |
| CD4070BNSR | SOP | NS | 14 | 2000 | 353.0 | 353.0 | 32.0 |
| CD4070BPWR | TSSOP | PW | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| CD4070BPWR | TSSOP | PW | 14 | 2000 | 353.0 | 353.0 | 32.0 |
| CD4077BM96 | SOIC | D | 14 | 2500 | 353.0 | 353.0 | 32.0 |
| CD4077BNSR | SOP | NS | 14 | 2000 | 353.0 | 353.0 | 32.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| CD4070BE | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD4070BE.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD4070BEE4 | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD4077BE | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD4077BE.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD4077BPW | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| CD4077BPW.A | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |



D0014A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J 14

GENERIC PACKAGE VIEW
CDIP - 5.08 mm max height
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

J0014A



PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



PW0014A



PACKAGE OUTLINE
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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