

CMOS Dual 4-Bit Latch

High-Voltage Types (20-Volt Rating)

- CD4508B dual 4-bit latch contains two identical 4-bit latches with separate STROBE, RESET, and OUTPUT DISABLE controls. With the STROBE line in the high state, the data on the "D" inputs appear at the corresponding "Q" outputs provided the DISABLE line is in the low state. Changing the STROBE line to the low state locks the data into the latch. A high on the reset line forces the outputs to a low level regardless of the state of the STROBE input. The outputs are forced to the high-impedance state for bus line applications by a high level on the DISABLE input.

The CD4508B types are supplied in 24-lead hermetic dual-in-line ceramic packages (F3A suffix), 24-lead dual-in-line plastic packages (E suffix), 24-lead small-outline packages (M, M96, and NSR suffixes), and 24-lead thin shrink small-outline packages (PW and PWR suffixes).

The CD4508B is similar to industry type MC14508.

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

Voltages referenced to V_{SS} Terminal) -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS -0.5V to V_{DD} +0.5V

DC INPUT CURRENT, ANY ONE INPUT $\pm 10\text{mA}$

POWER DISSIPATION PER PACKAGE (P_D):

For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$ 500mW

For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$ Derate Linearity at $12\text{mW}/^\circ\text{C}$ to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR $T_A =$ FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW

OPERATING-TEMPERATURE RANGE (T_A) -55°C to +125°C

STORAGE TEMPERATURE RANGE (T_{stg}) -65°C to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance $1/16 \pm 1/32$ inch ($1.59 \pm 0.79\text{mm}$) from case for 10s max $+265^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS at $T_A = 25^\circ\text{C}$, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

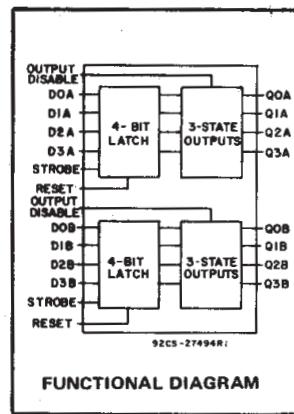
CHARACTERISTIC	V_{DD} (V)	LIMITS		UNITS
		Min.	Max.	
Supply-Voltage Range (For $T_A =$ Full Package- Temperature Range)		3	18	V
Reset Pulse Width, $t_{W(R)}$	5	200	—	
	10	140	—	
	15	100	—	
Strobe Pulse Width, $t_{W(st)}$	5	140	—	
	10	80	—	
	15	70	—	
Setup Time, t_{SU}	5	50	—	
	10	30	—	
	15	20	—	
Hold Time, t_H	5	0	—	
	10	0	—	
	15	0	—	

Features:

- Two independent 4-bit latches
- Individual master reset for each 4-bit latch
- 3-state outputs with high-impedance state for bus line applications
- Medium-speed operation: $t_{PHL} = t_{PLH} = 70\text{ ns}$ (typ.) at $V_{DD} = 10\text{ V}$ and $C_L = 50\text{ pF}$
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Standardized, symmetrical output characteristics
- Maximum input current of $1\text{ }\mu\text{A}$ at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) =
 - 1 V at $V_{DD} = 5\text{ V}$
 - 2 V at $V_{DD} = 10\text{ V}$
 - 2.5 V at $V_{DD} = 15\text{ V}$
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Buffer storage
- Holding registers
- Data storage and multiplexing



FUNCTIONAL DIAGRAM

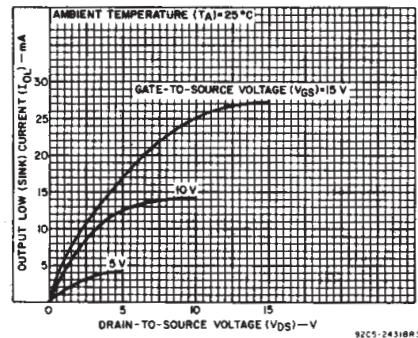


Fig.2 – Typical output low (sink) current characteristics.

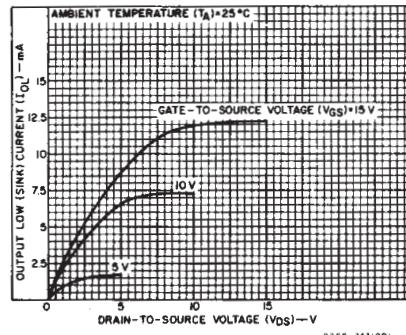


Fig.3 – Minimum output low (sink) current characteristics.

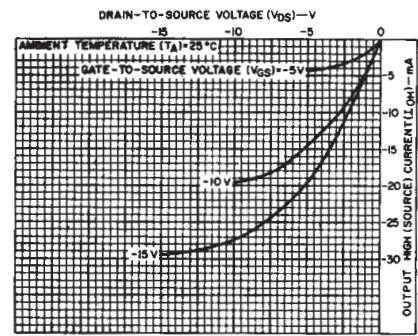


Fig.4 – Typical output high (source) current characteristics.

CD4508B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)						UNITS	
	V _O (V)	V _{IN} (V)	V _{DD} (V)	+25							
				-55	-40	+85	+125	Min.	Typ.		
Quiescent Device Current, I _{DD} Max.	-	0.5	5	5	5	150	150	-	0.04	μA	
	-	0.10	10	10	10	300	300	-	0.04	10	
	-	0.15	15	20	20	600	600	-	0.04	20	
	-	0.20	20	100	100	3000	3000	-	0.08	100	
Output Low (Sink) Current I _{OL} Min.	0.4	0.5	5	0.64	0.61	0.42	0.36	0.51	1	-	
	0.5	0.10	10	1.6	1.5	1.1	0.9	1.3	2.6	-	
	1.5	0.15	15	4.2	4	2.8	2.4	3.4	6.8	-	
Output High (Source) Current, I _{OH} Min.	4.6	0.5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	-	
	2.5	0.5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	-	
	9.5	0.10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	-	
	13.5	0.15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	-	
Output Voltage: Low-Level, VOL Max.	-	0.5	5	0.05			-	0	0.05	-	
	-	0.10	10	0.05			-	0	0.05	-	
	-	0.15	15	0.05			-	0	0.05	-	
Output Voltage: High-Level, VOH Min.	-	0.5	5	4.95			4.95	5	-	-	
	-	0.10	10	9.95			9.95	10	-	-	
	-	0.15	15	14.95			14.95	15	-	-	
Input Low Voltage, V _{IL} Max.	0.5, 4.5	-	5	1.5			-	-	1.5	-	
	1.9	-	10	3			-	-	3	-	
	1.5, 13.5	-	15	4			-	-	4	-	
Input High Voltage, V _{IH} Min.	0.5, 4.5	-	5	3.5			3.5	-	-	-	
	1.9	-	10	7			7	-	-	-	
	1.5, 13.5	-	15	11			11	-	-	-	
Input Current I _{IN} Max.	-	0.18	18	±0.1	±0.1	±1	±1	-	±10 ⁻⁵	±0.1	
3-State Output Leakage Current I _{OUT} Max.	0.18	0.18	18	±0.4	±0.4	±12	±12	-	±10 ⁻⁴	±0.4	

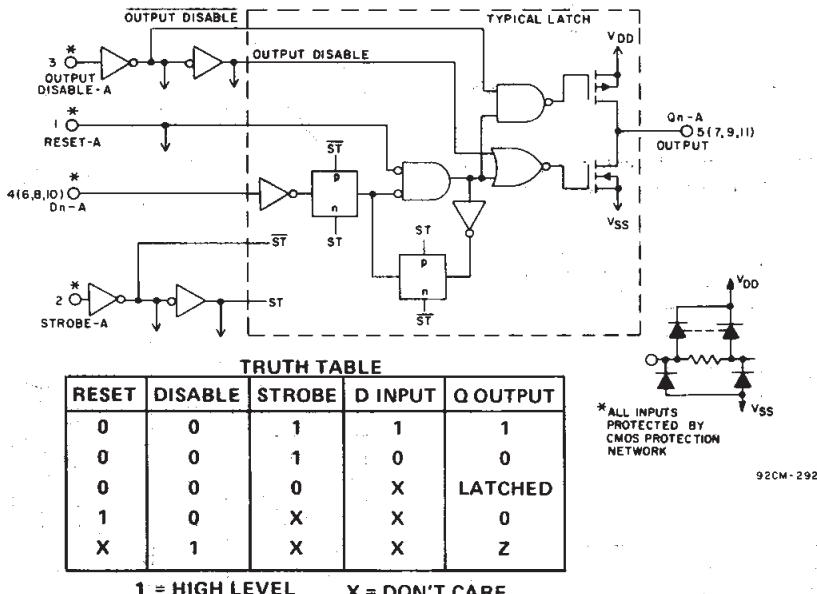


Fig. 7 — Logic diagram (A-Section), 1 of 4 identical latches with common output disable, reset, and strobe.

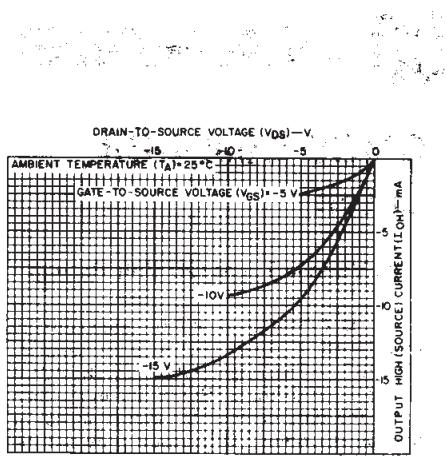


Fig. 4 — Minimum output high (source) current characteristics.

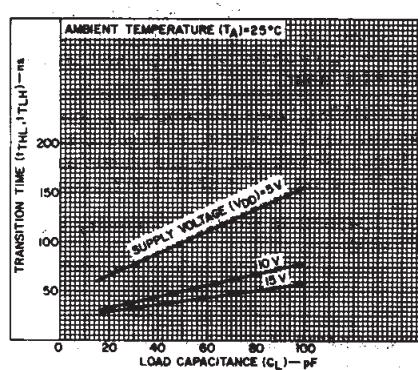


Fig. 5 — Typical transition time as a function of load capacitance.

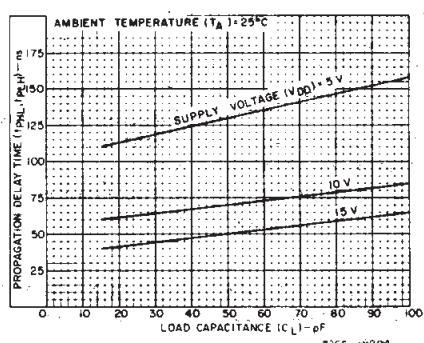


Fig. 6 — Typical propagation delay time as a function of load capacitance (strobe to data out).

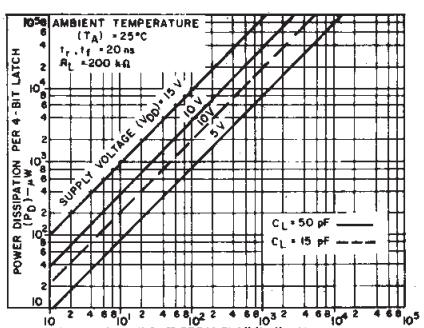


Fig. 8 — Typical power dissipation as a function of frequency.

CD4508B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$; Input $t_r, t_f = 20\text{ ns}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$, unless otherwise specified.

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		V _{DD}	Typ.	Max.	
Transition Time, t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Minimum Reset Pulse Width, $t_{W(R)}$		5	100	200	ns
		10	70	140	
		15	50	100	
Minimum Strobe Pulse Width, $t_{W(st)}$		5	70	140	ns
		10	40	80	
		15	35	70	
Minimum Setup Time, t_{SU}		5	25	50	ns
		10	15	30	
		15	10	20	
Minimum Hold Time, t_H		5	0	0	ns
		10	0	0	
		15	0	0	
Propagation Delay Times: t_{PHL}, t_{PLH} Strobe to Data Out		5	130	260	ns
		10	70	140	
		15	50	100	
Data In to Data Out		5	105	210	ns
		10	60	120	
		15	45	90	
Reset to Data Out		5	90	180	ns
		10	50	100	
		15	40	80	
3-State Propagation Delay Times: Output High to High Impedance, t_{PHZ}		5	90	180	ns
		10	50	100	
		15	35	70	
High Impedance to Output High, t_{PZH}		5	90	180	ns
		10	50	100	
		15	35	70	
Output Low to High Impedance, t_{PLZ}		5	90	180	ns
		10	50	100	
		15	35	70	
High Impedance to Output Low, t_{PZL}		5	90	180	ns
		10	50	100	
		15	35	70	
Input Capacitance, C_{IN}	Any Input	—	5	7.5	pF

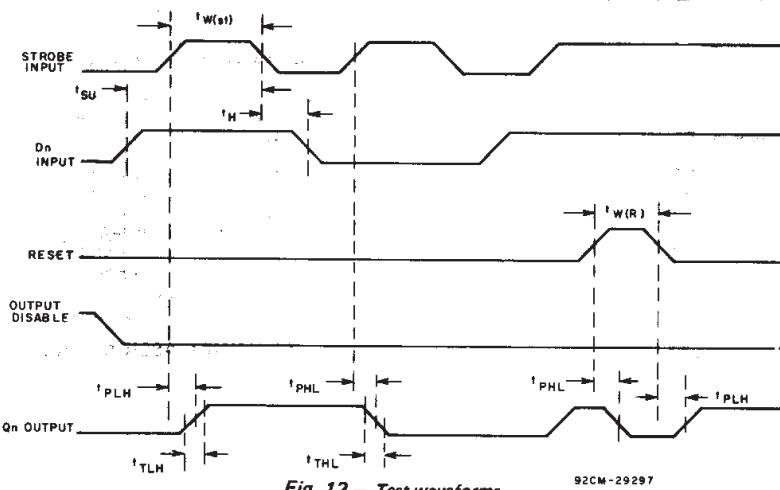
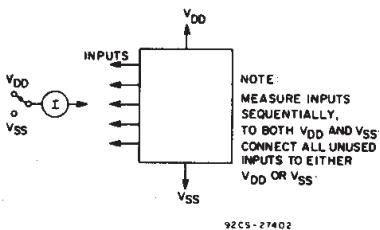
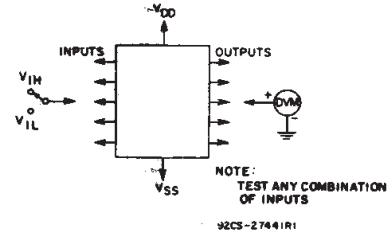
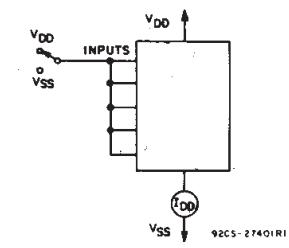
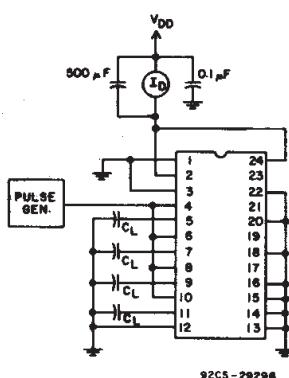


Fig. 12 — Test waveforms.



CD4508B Types

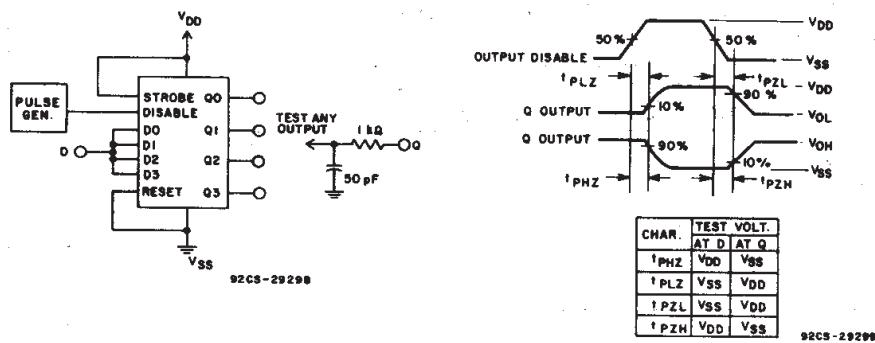


Fig.14 – Output disable test circuit and waveforms.

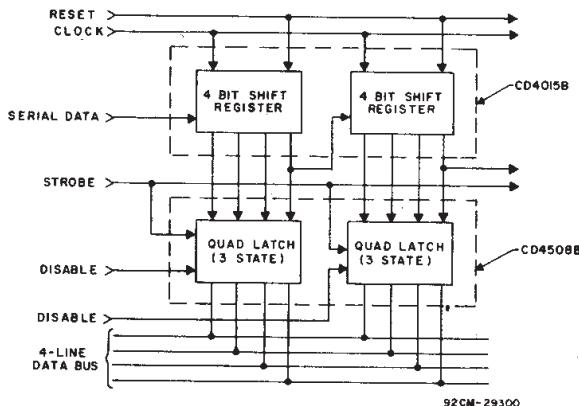


Fig.15 – Bus register.

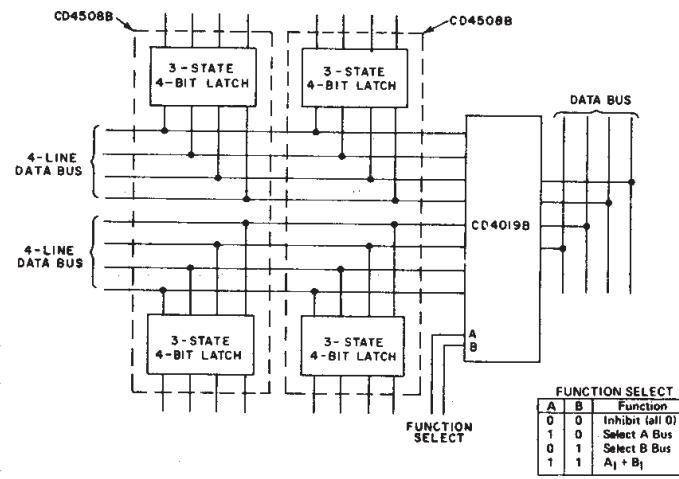
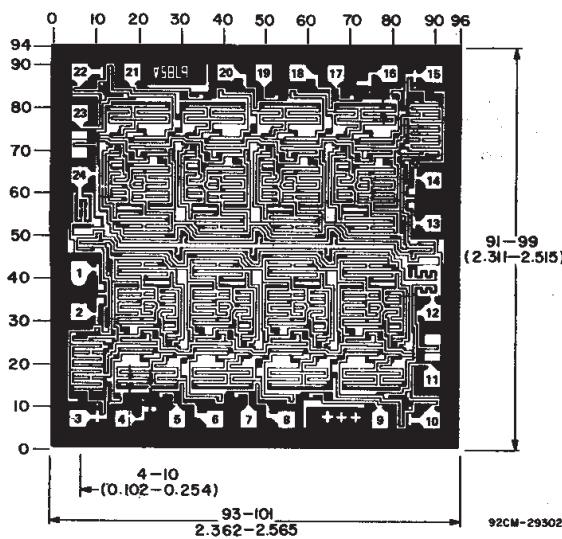


Fig.16 – Dual multiplexed bus register with function select.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Chip dimensions and pad layout for CD4508B.

TERMINAL ASSIGNMENT

RESET A	1	24	V _{DD}
STROBE A	2	23	Q _{3B}
OUTPUT	3	22	D _{3B}
DISABLE A	4	21	Q _{2B}
D _{0A}	5	20	D _{2B}
Q _{0A}	6	19	Q _{1B}
D _{1A}	7	18	D _{1B}
Q _{1A}	8	17	Q _{0B}
D _{2A}	9	16	D _{0B}
Q _{2A}	10	15	OUTPUT
D _{3A}	11	14	DISABLE B
Q _{3A}	12	13	STROBE B
V _{SS}			RESET B

TOP VIEW

92CS-27604

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD4508BD3	Last Time Buy	Production	CDIP SB (JD) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4508BD/3
CD4508BD3.A	Last Time Buy	Production	CDIP SB (JD) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4508BD/3
CD4508BF3A	Active	Production	CDIP (J) 24	15 TUBE	No	Call TI	N/A for Pkg Type	-55 to 125	CD4508BF3A
CD4508BF3A.A	Active	Production	CDIP (J) 24	15 TUBE	No	Call TI	N/A for Pkg Type	-55 to 125	CD4508BF3A
CD4508BM	Obsolete	Production	SOIC (DW) 24	-	-	Call TI	Call TI	-55 to 125	CD4508BM
CD4508BM96	Active	Production	SOIC (DW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4508BM
CD4508BM96.A	Active	Production	SOIC (DW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4508BM
CD4508BNSR	Active	Production	SOP (NS) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4508B
CD4508BNSR.A	Active	Production	SOP (NS) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4508B
CD4508BPW	Active	Production	TSSOP (PW) 24	60 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM508B
CD4508BPW.A	Active	Production	TSSOP (PW) 24	60 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM508B

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

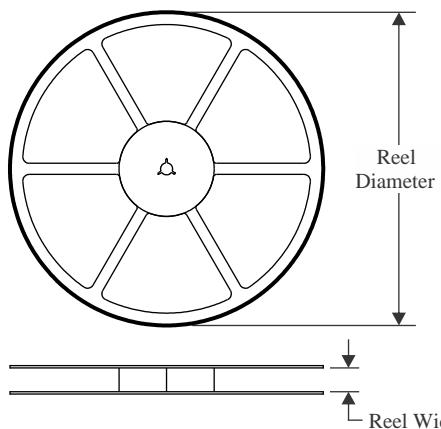
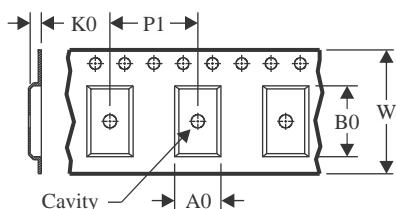
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD4508B, CD4508B-MIL :

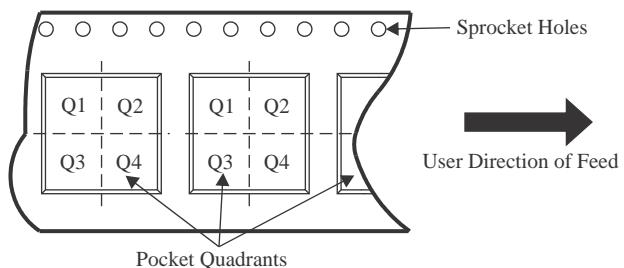
- Catalog : [CD4508B](#)
- Military : [CD4508B-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

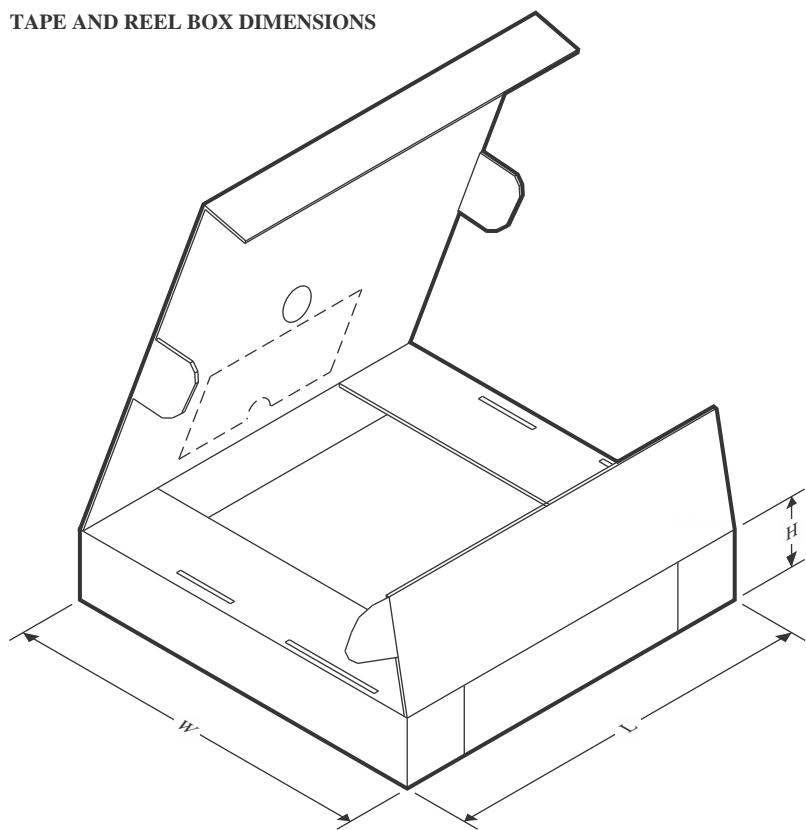
TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


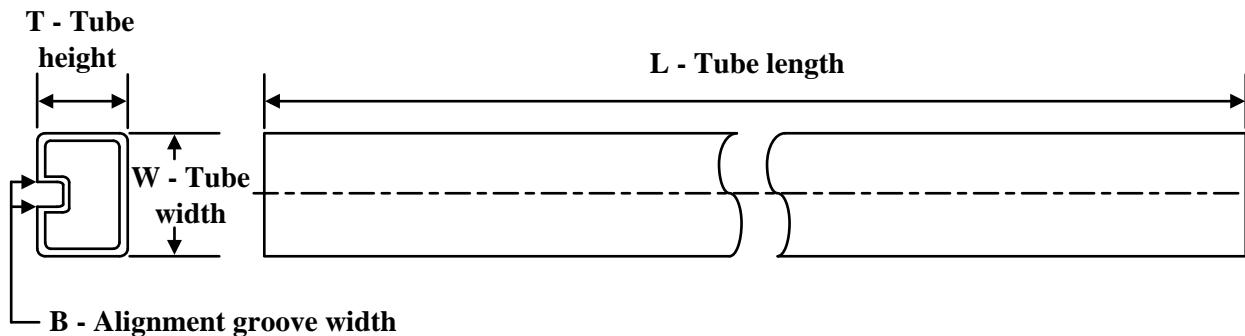
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4508BM96	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4508BM96	SOIC	DW	24	2000	350.0	350.0	43.0

TUBE


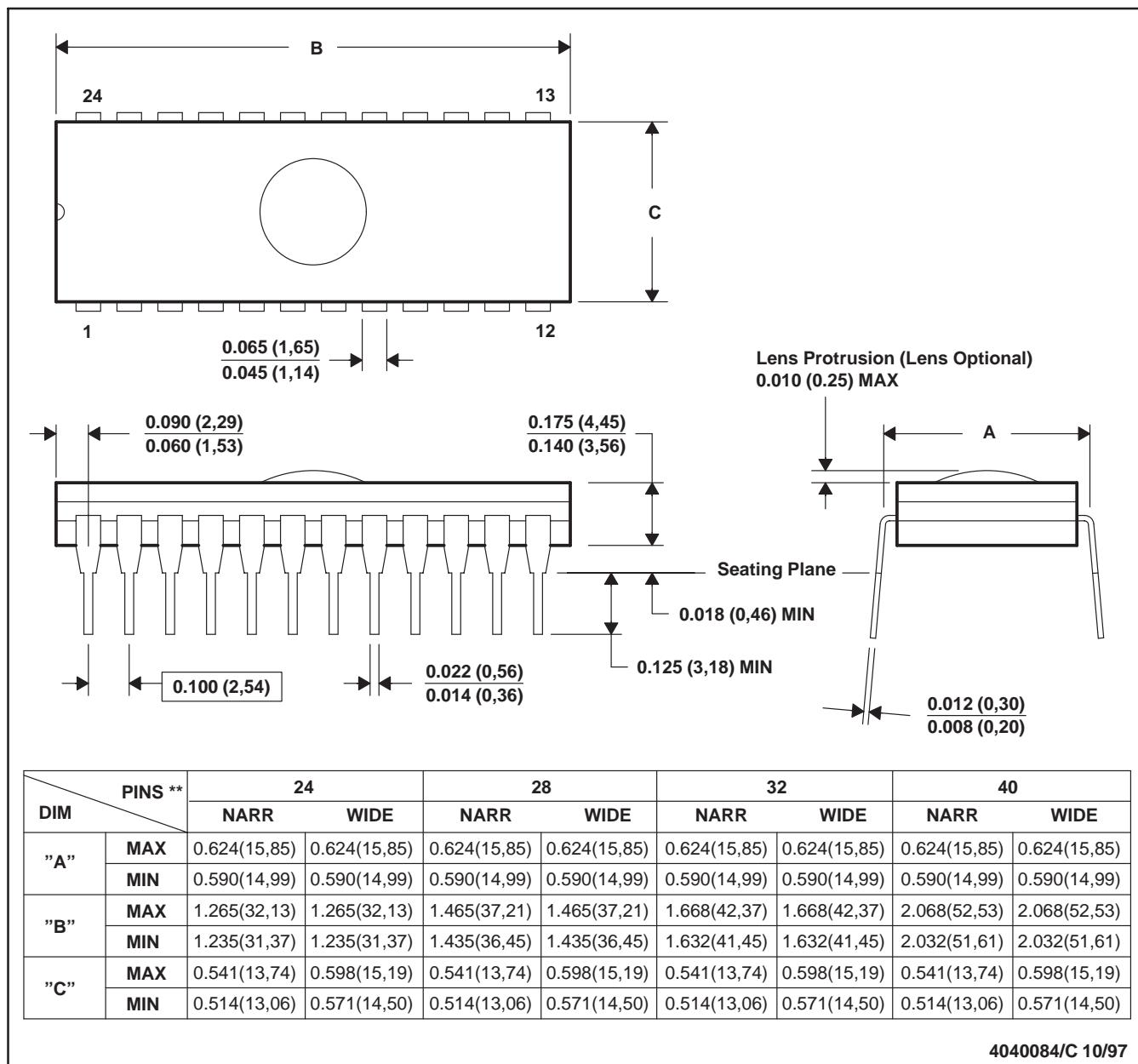
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD4508BPW	PW	TSSOP	24	60	530	10.2	3600	3.5
CD4508BPW.A	PW	TSSOP	24	60	530	10.2	3600	3.5

J (R-GDIP-T**)

CERAMIC DUAL-IN-LINE PACKAGE

24 PINS SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Window (lens) added to this group of packages (24-, 28-, 32-, 40-pin).
 D. This package can be hermetically sealed with a ceramic lid using glass frit.
 E. Index point is provided on cap for terminal identification.

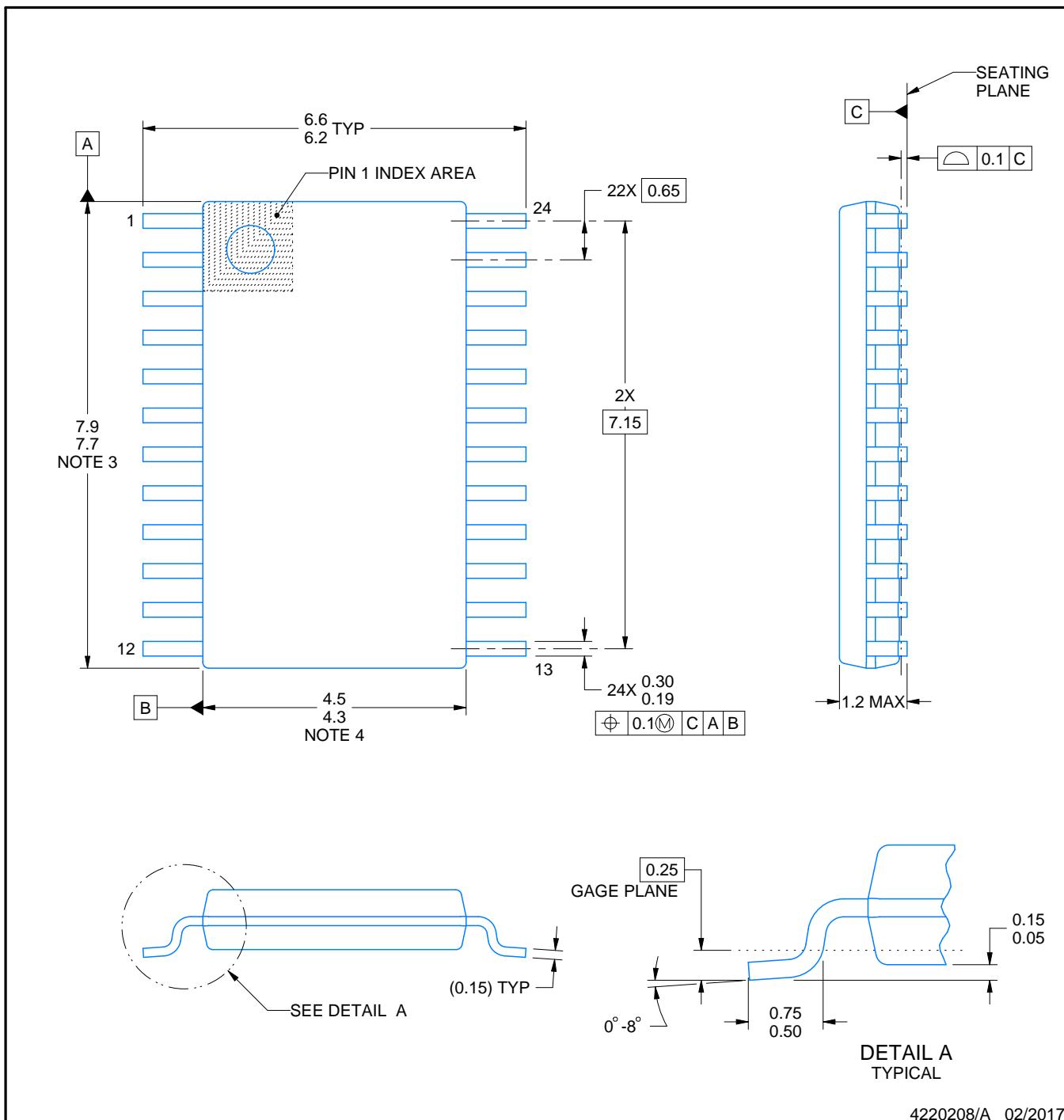
PACKAGE OUTLINE

PW0024A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

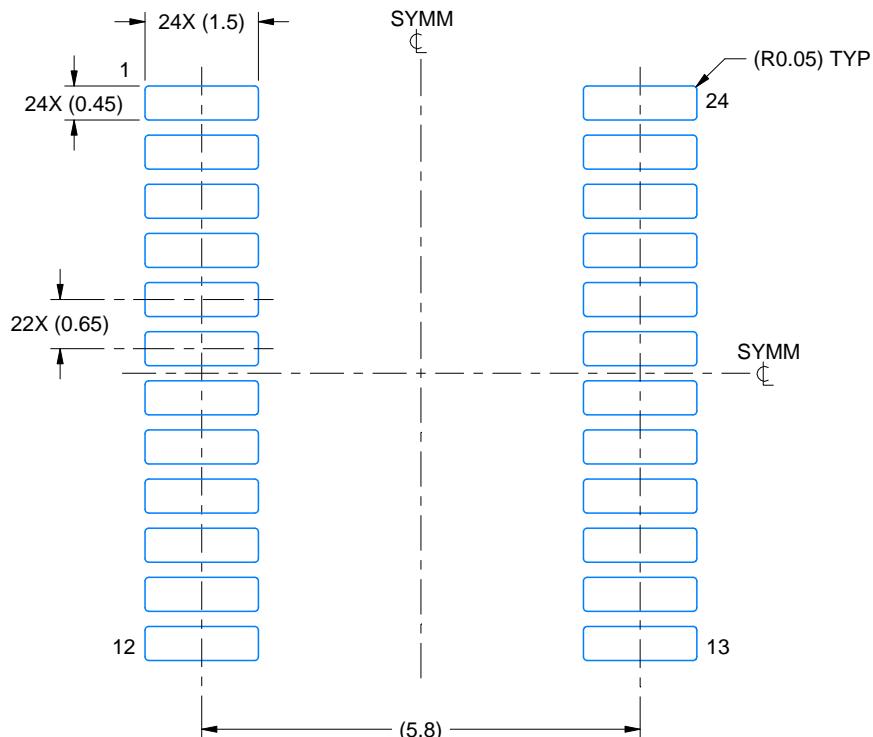
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

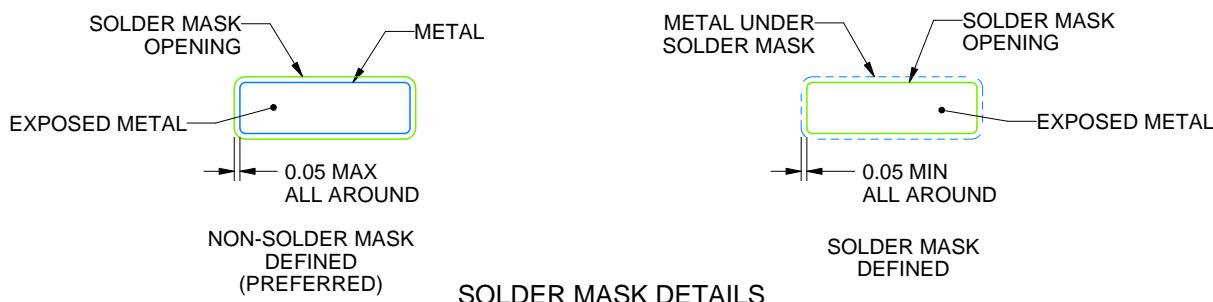
PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

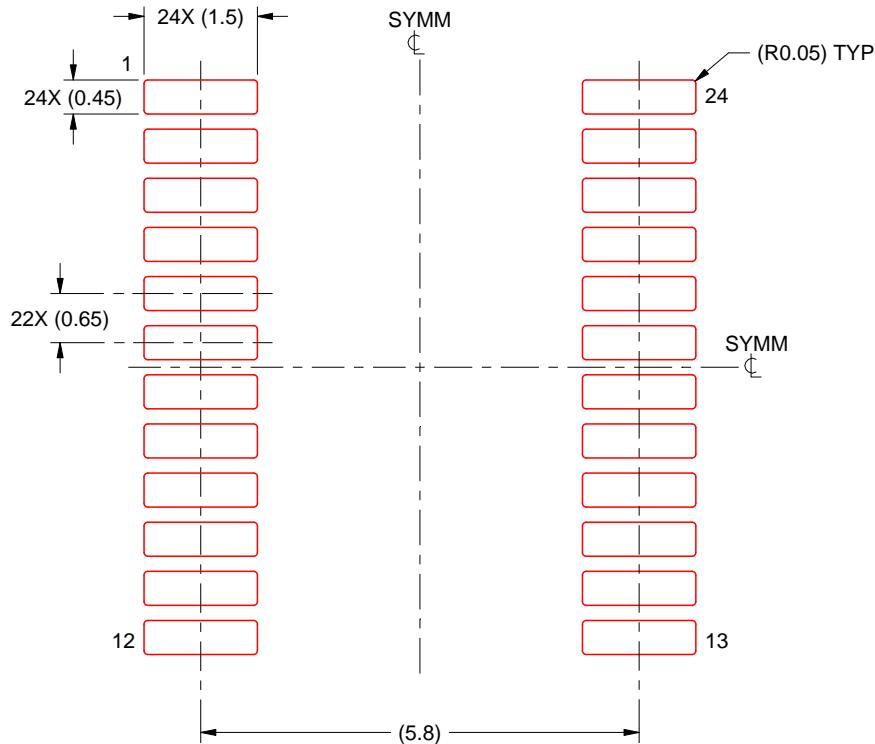
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

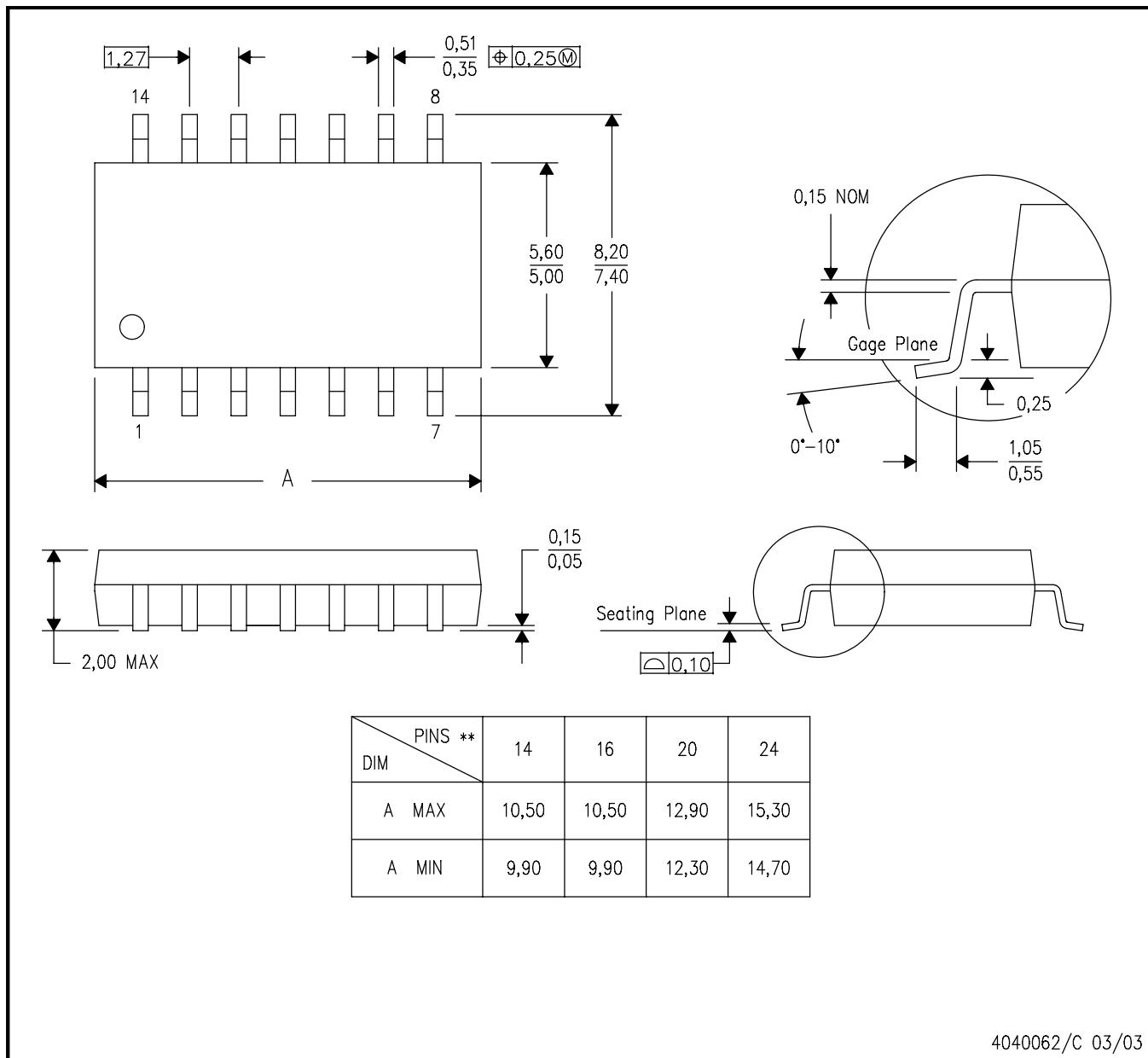
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



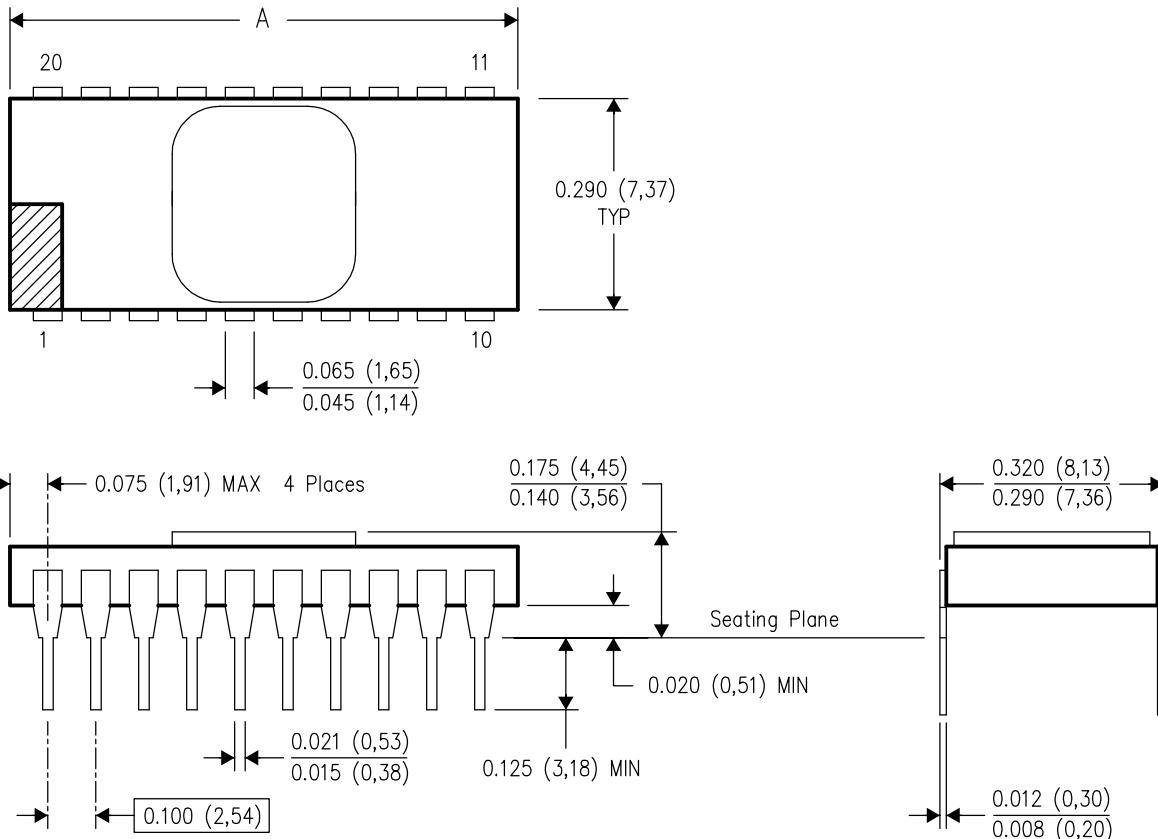
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

JD (R-CDIP-T**)

20 PINS SHOWN

CERAMIC SIDE-BRAZE DUAL-IN-LINE PACKAGE



PINS ** DIM	8	14	16	18	20	24
A MAX	0.405 (10.29)	0.757 (19.23)	0.810 (20.57)	0.910 (23.11)	1.010 (25.65)	1.100 (27.94)

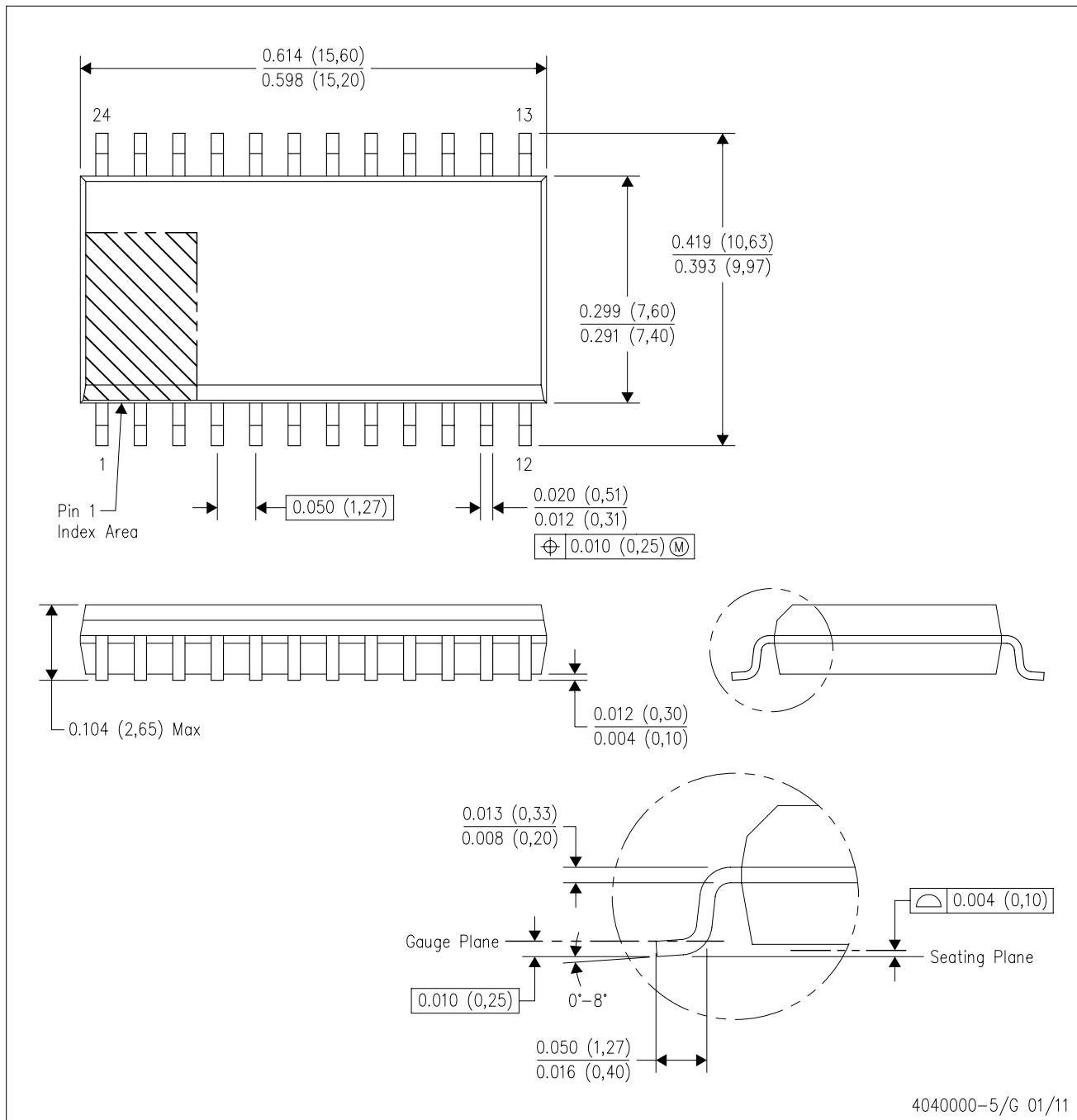
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NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a metal lid.
- D. The terminals are gold plated.
- E. Falls within MIL STD 1835 CDIP2 – T8, T14, T16, T18, T20 and T24 respectively.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



NOTES:

- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).
- Falls within JEDEC MS-013 variation AD.

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