

# CDx4AC245、CDx4ACT245 オクタル・バス・トランシーバ、3 ステート、非反転型

## 1 特長

- バッファ付き入力
- 伝搬遅延時間 (標準値)
  - $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ ,  $C_L = 50pF$  で 4ns
- SCR ラッチアップ耐性の高い CMOS プロセスと回路設計
- 消費電力を大幅に低減した、バイポーラ FAST™/AS/S の速度
- 伝搬遅延時間の平衡化
- AC タイプは 1.5V~5.5V で動作し、バランスのとれたノイズ耐性を電源の 30% で実現
- $\pm 24mA$  出力駆動電流
  - 15 個の FAST™ IC にファンアウト
  - 50Ω 伝送ラインを駆動します

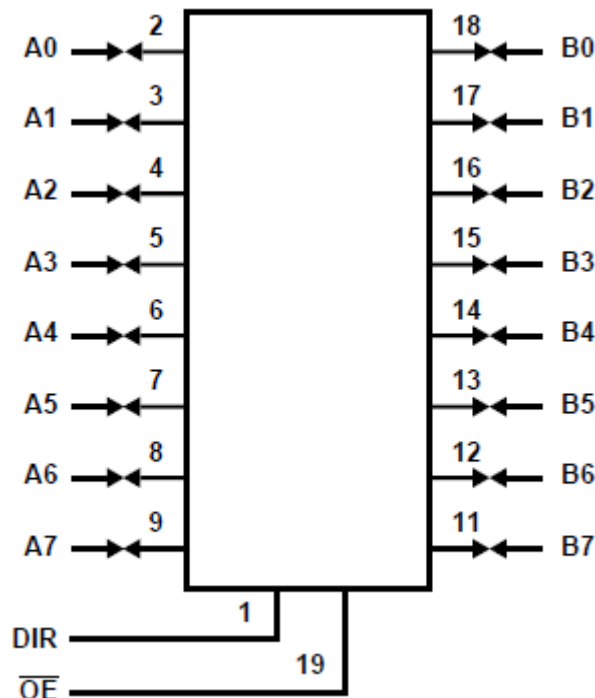
## 2 概要

「AC245」と「ACT245」は、アドバンスト CMOS ロジック テクノロジーを採用したオクタル バストランシーバです。

### 製品情報

| 部品番号                     | パッケージ (1)     | パッケージ サイズ (2)    | 本体サイズ (3)        |
|--------------------------|---------------|------------------|------------------|
| CD74AC245/<br>CD74ACT245 | N (PDIP, 20)  | 24.33mm × 9.4mm  | 24.33mm × 6.35mm |
|                          | DW (SOIC, 20) | 12.80mm × 10.3mm | 12.80mm × 7.50mm |
| CD54AC245/<br>CD54ACT245 | J (CDIP, 20)  | 24.2mm × 7.62mm  | 24.2mm × 6.92mm  |
|                          | DB (SSOP, 20) | 7.2mm × 7.8mm    | 7.2mm × 5.3mm    |

- 詳細については、[セクション 10](#) を参照してください。
- パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。
- 本体サイズ (長さ × 幅) は公称値であり、ピンは含まれません。



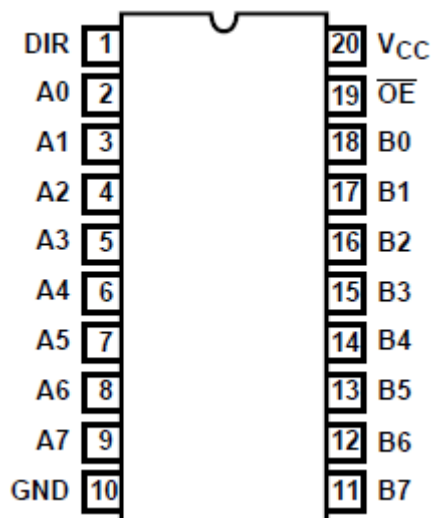
論理図 (正論理)



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## 3 Pin Configuration and Functions



3-1. CD54AC245, CD54ACT245 (CERDIP), CD74AC245, CD74ACT245 (PDIP, SOIC, SSOP) Top View

Pin Functions

| PIN |                 | TYPE <sup>1</sup> | DESCRIPTION     |
|-----|-----------------|-------------------|-----------------|
| NO. | NAME            |                   |                 |
| 1   | DIR             | I/O               | Direction Pin   |
| 2   | A0              | I/O               | A1 Input/Output |
| 3   | A1              | I/O               | A2 Input/Output |
| 4   | A2              | I/O               | A3 Input/Output |
| 5   | A3              | I/O               | A4 Input/Output |
| 6   | A4              | I/O               | A5 Input/Output |
| 7   | A5              | I/O               | A6 Input/Output |
| 8   | A6              | I/O               | A7 Input/Output |
| 9   | A7              | I/O               | A8 Input/Output |
| 10  | GND             | —                 | Ground Pin      |
| 11  | B7              | I/O               | B7 Input/Output |
| 12  | B6              | I/O               | B6 Input/Output |
| 13  | B5              | I/O               | B5 Input/Output |
| 14  | B4              | I/O               | B4 Input/Output |
| 15  | B3              | I/O               | B3 Input/Output |
| 16  | B2              | I/O               | B2 Input/Output |
| 17  | B1              | I/O               | B1 Input/Output |
| 18  | B0              | I/O               | B0 Input/Output |
| 19  | OE              | I/O               | Output Enable   |
| 20  | V <sub>CC</sub> | —                 | Power Pin       |

(1) Signal Types: I = Input, O = Output, I/O = Input or Output

## 4 Specifications

### 4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                                |                                              |                                                                   | MIN  | MAX   | UNIT |
|--------------------------------|----------------------------------------------|-------------------------------------------------------------------|------|-------|------|
| V <sub>CC</sub>                | Supply voltage                               |                                                                   | -0.5 | 6     | V    |
| I <sub>IK</sub>                | Input diode current                          | V <sub>I</sub> < -0.5V or V <sub>I</sub> > V <sub>CC</sub> + 0.5V |      | ± 20  | mA   |
| I <sub>OK</sub>                | Output diode current                         | V <sub>O</sub> < -0.5V or V <sub>O</sub> > V <sub>CC</sub> + 0.5V |      | ± 50  | mA   |
| I <sub>O</sub>                 | Output source or sink current per output pin | V <sub>O</sub> > -0.5V or V <sub>O</sub> < V <sub>CC</sub> + 0.5V |      | ± 50  | mA   |
| I <sub>OK</sub> <sup>(2)</sup> | V <sub>CC</sub> or ground current            | I <sub>CC</sub> or I <sub>GND</sub>                               |      | ± 100 | mA   |
| T <sub>stg</sub>               | Storage temperature                          |                                                                   | -65  | 150   | °C   |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) For up to 4 outputs per device, add ±25mA for each additional output.

### 4.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                                 |                               | CDx4AC245    |                 | CDx4ACT245 |                 | UNIT |
|---------------------------------|-------------------------------|--------------|-----------------|------------|-----------------|------|
|                                 |                               | MIN          | MAX             | MIN        | MAX             |      |
| V <sub>CC</sub>                 | Supply voltage <sup>(1)</sup> | 1.5V         | 5.5V            | 4.5V       | 5.5V            | V    |
| V <sub>I</sub> , V <sub>O</sub> | Input or Output Voltage       | 0V           | V <sub>CC</sub> | 0V         | V <sub>CC</sub> | V    |
| dt/dv                           | Input Rise and Fall Slew Rate | 1.5V to 3V   | 50              |            |                 | ns   |
|                                 |                               | 3.6V to 5.5V | 20              |            |                 |      |
|                                 |                               | 4.5V to 5.5V |                 |            | 10              |      |
| T <sub>A</sub>                  | Temperature range             | -55          | 125             | -55        | 125             | °C   |

(1) Unless otherwise specified, all voltages are referenced to ground.

### 4.3 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                        | CDx4AC14/ CDx4ACT14 |           |           | UNIT |
|-------------------------------|----------------------------------------|---------------------|-----------|-----------|------|
|                               |                                        | N (PDIP)            | DW (SOIC) | DB (SSOP) |      |
|                               |                                        | 20 PINS             |           |           |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance | 69                  | 98.6      | 105.4     | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 4.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER       | TEST CONDITIONS              |                                                                              |                  | V <sub>CC</sub> | T <sub>A</sub> = 25°C |      | -40°C TO 85°C |                  | -55°C TO 125°C |  | UNIT |
|-----------------|------------------------------|------------------------------------------------------------------------------|------------------|-----------------|-----------------------|------|---------------|------------------|----------------|--|------|
|                 | V <sub>I</sub> (V)           | I <sub>O</sub> (mA)                                                          | MIN              |                 | MAX                   | MIN  | MAX           | MIN              | MAX            |  |      |
| AC TYPES        |                              |                                                                              |                  |                 |                       |      |               |                  |                |  |      |
| V <sub>IH</sub> | High-level input voltage     |                                                                              |                  | 1.5             | 1.2                   | 1.2  | 1.2           | V                |                |  |      |
|                 |                              |                                                                              |                  | 3               | 2.1                   | 2.1  | 2.1           |                  |                |  |      |
|                 |                              |                                                                              |                  | 5.5             | 3.85                  | 3.85 | 3.85          |                  |                |  |      |
| V <sub>IL</sub> | Low-level input voltage      | V <sub>IL</sub>                                                              |                  | 1.5             | 0.3                   | 0.3  | 0.3           | V                |                |  |      |
|                 |                              |                                                                              |                  | 3               | 0.9                   | 0.9  | 0.9           |                  |                |  |      |
|                 |                              |                                                                              |                  | 5.5             | 1.65                  | 1.65 | 1.65          |                  |                |  |      |
| V <sub>OH</sub> | High-level output voltage    | V <sub>IH</sub> or V <sub>IL</sub>                                           | -0.05            | 1.5             | 1.4                   | 1.4  | 1.4           | V <sub>VOH</sub> |                |  |      |
|                 |                              |                                                                              | -0.05            | 3               | 2.9                   | 2.9  | 2.9           |                  |                |  |      |
|                 |                              |                                                                              | -0.05            | 4.5             | 4.4                   | 4.4  | 4.4           |                  |                |  |      |
|                 |                              |                                                                              | -4               | 3               | 2.58                  | 2.48 | 2.4           |                  |                |  |      |
|                 |                              |                                                                              | -24              | 4.5             | 3.94                  | 3.8  | 3.7           |                  |                |  |      |
|                 |                              |                                                                              | -75              | 5.5             |                       | 3.85 |               |                  |                |  |      |
|                 |                              |                                                                              | -50              | 5.5             |                       |      | 3.85          |                  |                |  |      |
| V <sub>OL</sub> | Low-level output voltage     | V <sub>IH</sub> or V <sub>IL</sub>                                           | 0.05             | 1.5 V           | 0.1                   | 0.1  | 0.1           | V                |                |  |      |
|                 |                              |                                                                              | 0.05             | 3 V             | 0.1                   | 0.1  | 0.1           |                  |                |  |      |
|                 |                              |                                                                              | 0.05             | 4.5 V           | 0.1                   | 0.1  | 0.1           |                  |                |  |      |
|                 |                              |                                                                              | 12               | 3 V             | 0.36                  | 0.44 | 0.5           |                  |                |  |      |
|                 |                              |                                                                              | 24               | 4.5 V           | 0.36                  | 0.44 | 0.5           |                  |                |  |      |
|                 |                              |                                                                              | 75 <sup>1</sup>  | 5.5 V           |                       | 1.65 |               |                  |                |  |      |
|                 |                              |                                                                              | 50 <sup>1</sup>  | 5.5 V           |                       |      | 1.65          |                  |                |  |      |
| I <sub>I</sub>  | Input leakage current        | V <sub>CC</sub> or GND                                                       |                  | 5.5             | ± 0.1                 | ± 1  | ± 1           | μ A              |                |  |      |
| I <sub>OZ</sub> | Three-state leakage current  | V <sub>IH</sub> or V <sub>IL</sub> , V <sub>O</sub> = V <sub>CC</sub> or GND |                  | 5.5 V           | ± 0.5                 | ± 5  | ± 10          | μ A              |                |  |      |
| I <sub>CC</sub> | Quiescent supply current MSI | V <sub>CC</sub> or GND                                                       | 0                | 5.5 V           | 8                     | 80   | 160           | μ A              |                |  |      |
| ACT TYPES       |                              |                                                                              |                  |                 |                       |      |               |                  |                |  |      |
| V <sub>IH</sub> | High-level input voltage     |                                                                              |                  | 4.5 V to 5.5 V  | 2                     | 2    | 2             | V                |                |  |      |
| V <sub>IL</sub> | Low-level input voltage      |                                                                              |                  | 4.5 V to 5.5 V  | 0.8                   | 0.8  | 0.8           | V                |                |  |      |
| V <sub>OH</sub> | High-level output voltage    | V <sub>IH</sub> or V <sub>IL</sub>                                           | -0.05            | 4.5 V           | 4.4                   | 4.4  | 4.4           | 0.8              | V              |  |      |
|                 |                              |                                                                              | -24              | 4.5 V           | 3.94                  | 3.8  | 3.7           |                  |                |  |      |
|                 |                              |                                                                              | -75 <sup>1</sup> | 5.5 V           |                       | 3.85 |               |                  |                |  |      |
|                 |                              |                                                                              | -50              | 5.5 V           |                       |      | 3.85          |                  |                |  |      |

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                                                                           | TEST CONDITIONS                              |                 | $V_{CC}$   | $T_A = 25^\circ\text{C}$ |           | $-40^\circ\text{C TO } 85^\circ\text{C}$ |         | $-55^\circ\text{C TO } 125^\circ\text{C}$ |          | UNIT          |
|-------------------------------------------------------------------------------------|----------------------------------------------|-----------------|------------|--------------------------|-----------|------------------------------------------|---------|-------------------------------------------|----------|---------------|
|                                                                                     | $V_I$ (V)                                    | $I_O$ (mA)      |            | MIN                      | MAX       | MIN                                      | MAX     | MIN                                       | MAX      |               |
| $V_{OL}$ Low-level output voltage                                                   | $V_{IH}$ or $V_{IL}$                         | 0.05            | 4.5        |                          | 0.1       |                                          | 0.1     |                                           | 0.1      | V             |
|                                                                                     |                                              | 24              | 4.5        |                          | 0.36      |                                          | 0.44    |                                           | 0.5      |               |
|                                                                                     |                                              | 75 <sup>1</sup> | 5.5        |                          |           |                                          | 1.65    |                                           |          |               |
|                                                                                     |                                              | 50 <sup>1</sup> | 5.5        |                          |           |                                          |         |                                           | 1.65     |               |
|                                                                                     |                                              |                 |            |                          |           |                                          |         |                                           |          | V             |
| $I_I$ Input leakage current                                                         | $V_{CC}$ or GND                              |                 | 5.5 V      |                          | $\pm 0.1$ |                                          | $\pm 1$ |                                           | $\pm 1$  | $\mu\text{A}$ |
| $I_{OZ}$ Three-state or leakage current                                             | $V_{IH}$ or $V_{IL}$ , $V_O = V_{CC}$ or GND |                 | 5.5 V      |                          | $\pm 0.5$ |                                          | $\pm 5$ |                                           | $\pm 10$ | $\mu\text{A}$ |
| $I_{CC}$ Quiescent supply current MSI                                               | $V_{CC}$ or GND                              | 0               | 5.5 V      |                          | 8         |                                          | 80      |                                           | 160      | $\mu\text{A}$ |
| $\Delta I_{CC}$ Additional supply current per input pin TTL inputs high 1 unit load | $V_{CC} - 2.1$                               |                 | 4.5 to 5.5 |                          | 2.4       |                                          | 2.8     |                                           | 3        | mA            |

- Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation. Test verifies a minimum 50 $\Omega$  transmission-line-drive capability at 85°C, 75 $\Omega$  at 125°C.

#### 4.5 Switching Characteristics

Input  $t_r$ ,  $t_f = 3\text{ns}$ ,  $C_L = 50\text{pF}$  (Worst Case). Over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

| PARAMETER                           |                                                                                                      | V <sub>CC</sub> (V) | -40°C TO 85°C |           |      | -55°C TO 125°C |           |      | UNIT |
|-------------------------------------|------------------------------------------------------------------------------------------------------|---------------------|---------------|-----------|------|----------------|-----------|------|------|
|                                     |                                                                                                      |                     | MIN           | TYP       | MAX  | MIN            | TYP       | MAX  |      |
| AC TYPES                            |                                                                                                      |                     |               |           |      |                |           |      |      |
| t <sub>PLH</sub> , t <sub>PHL</sub> | Propagation delay, data to output                                                                    | 1.5                 |               |           | 96   |                |           | 106  | ns   |
|                                     |                                                                                                      | 3.3                 |               | 3.2       | 10.8 |                | 3         | 11.9 |      |
|                                     |                                                                                                      | 5                   |               | 2.2       | 7.7  |                | 2.1       | 8.5  |      |
| t <sub>PLZ</sub> , t <sub>PHZ</sub> | Propagation delay, output disable to output                                                          | 1.5                 |               |           | 159  |                |           | 175  | ns   |
|                                     |                                                                                                      | 3.3                 |               | 4.7       | 15.9 |                | 4.4       | 17.5 |      |
|                                     |                                                                                                      | 5                   |               | 3.7       | 12.7 |                | 3.5       | 14   |      |
| t <sub>PZL</sub> , t <sub>PZH</sub> | Propagation delay, output enable to output                                                           | 1.5                 |               |           | 159  |                |           | 175  | ns   |
|                                     |                                                                                                      | 3.3                 |               | 5.6       | 19   |                | 5.3       | 21   |      |
|                                     |                                                                                                      | 5                   |               | 3.7       | 12.7 |                | 3.5       |      |      |
| V <sub>OHV</sub>                    | Minimum (Valley) V <sub>OH</sub> During switching of other outputs (output under test not switching) | 5                   |               | 4 at 25°C |      |                | 4 at 25°C |      | V    |

Input  $t_r$ ,  $t_f$  = 3ns,  $C_L$  = 50pF (Worst Case). Over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

| PARAMETER                           |                                                                                                      | V <sub>CC</sub> (V) | -40°C TO 85°C |     |     | -55°C TO 125°C |     |      | UNIT |
|-------------------------------------|------------------------------------------------------------------------------------------------------|---------------------|---------------|-----|-----|----------------|-----|------|------|
|                                     |                                                                                                      |                     | MIN           | TYP | MAX | MIN            | TYP | MAX  |      |
| V <sub>OLP</sub>                    | Maximum (Peak) V <sub>OL</sub> During switching of other outputs (output under test not switching)   | 5                   | 1 at 25°C     |     |     | 1 at 25°C      |     |      | V    |
| C <sub>O</sub>                      | Three-state output capacitance                                                                       |                     | 15            |     |     | 15             |     |      | pF   |
| C <sub>I</sub>                      | Input capacitance                                                                                    |                     | 10            |     |     | 10             |     |      | pF   |
| C <sub>PD</sub>                     | Power dissipation capacitance                                                                        |                     | 57            |     |     | 57             |     |      | pF   |
| ACT TYPES                           |                                                                                                      |                     |               |     |     |                |     |      |      |
| t <sub>PLH</sub> , t <sub>PHL</sub> | Propagation delay, data to output                                                                    | 5                   | 2.7           |     |     | 9.1            | 2.5 | 10   | ns   |
| t <sub>PLZ</sub> , t <sub>PHZ</sub> | Propagation delay, output disable to output                                                          | 5                   | 3.7           |     |     | 12.7           | 3.5 | 14   | ns   |
| t <sub>PZL</sub> , t <sub>PZH</sub> | Propagation delay, output enable to output                                                           | 5                   | 3.8           |     |     | 13.1           | 3.6 | 14.4 | ns   |
| V <sub>OHV</sub>                    | Minimum (Valley) V <sub>OH</sub> During switching of other outputs (output under test not switching) | 5                   | 4 at 25°C     |     |     | 4 at 25°C      |     |      | V    |
| V <sub>OLP</sub>                    | Maximum (Peak) V <sub>OL</sub> During switching of other outputs (output under test not switching)   | 5                   | 1 at 25°C     |     |     | 1 at 25°C      |     |      | V    |
| C <sub>O</sub>                      | Three-state output capacitance                                                                       |                     | 15            |     |     | 15             |     |      | pF   |
| C <sub>I</sub>                      | Input capacitance                                                                                    |                     | 10            |     |     | 10             |     |      | pF   |
| C <sub>PD</sub>                     | Power dissipation capacitance                                                                        |                     | 57            |     |     | 57             |     |      | pF   |

- Limits tested 100%
- 3.3V Min is at 3.6V, Max is at 3V
- 5V Min is at 5.5V, Max is at 4.5V
- CPD is used to determine the dynamic power consumption per channel
  - AC:  $PD = VCC^2 f_i (CPD + CL)$
  - ACT:  $PD = VCC^2 f_i (CPD + CL) + VCC \Delta ICC$  where  $f_i$  = input frequency,  $CL$  = output load capacitance,  $VCC$  = supply voltage

## 4.6 Timing Diagrams

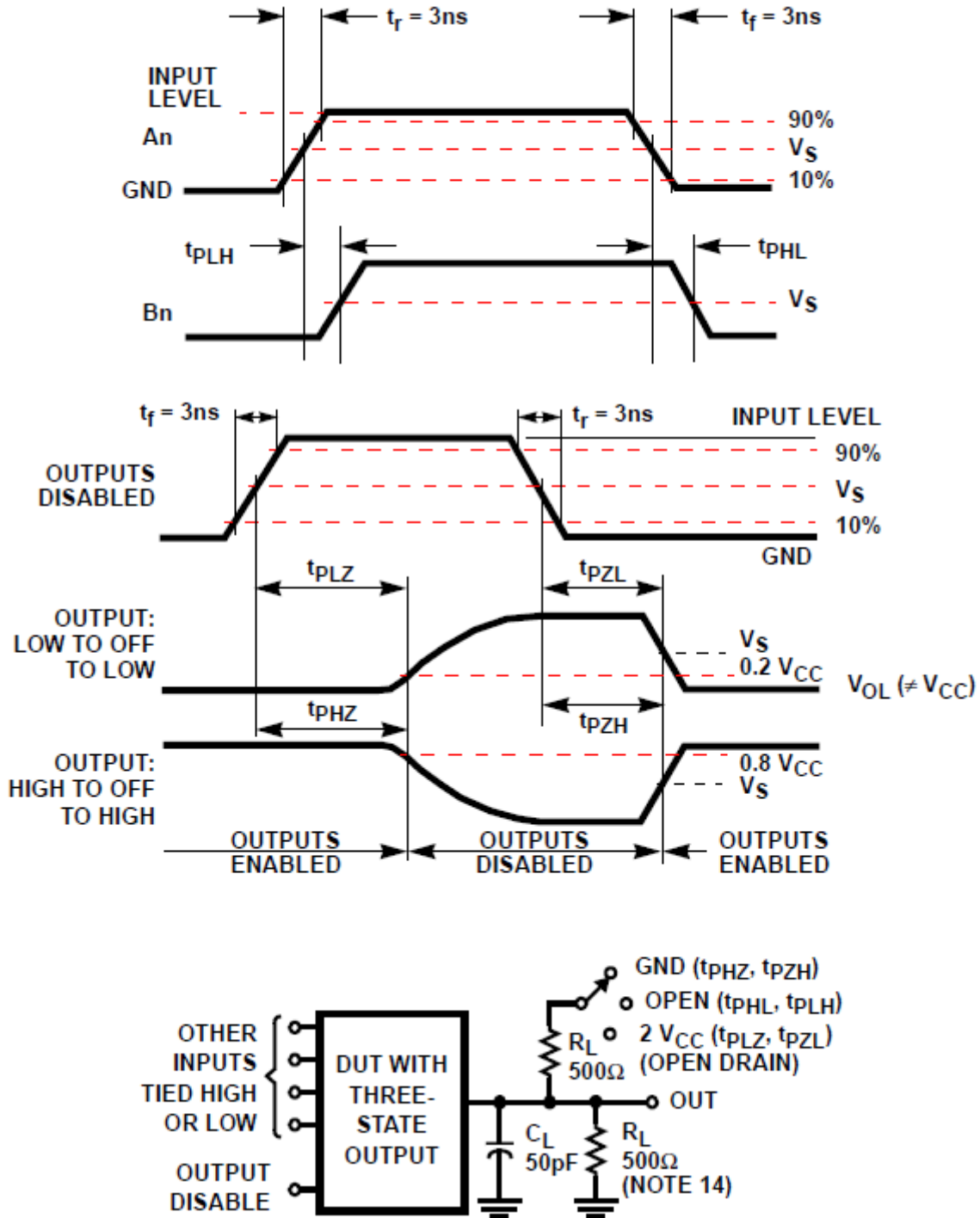


図 4-1. THREE-STATE PROPAGATION DELAY TIMES AND TEST CIRCUIT

図 4-1. SIMULTANEOUS SWITCHING TRANSIENT WAVEFORMS

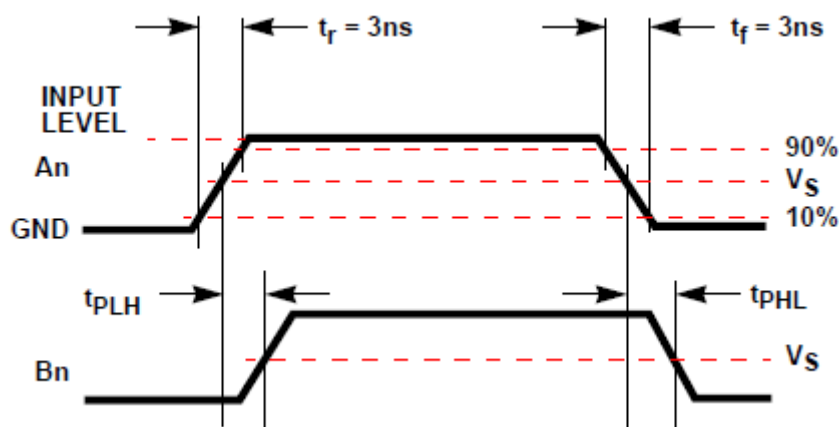
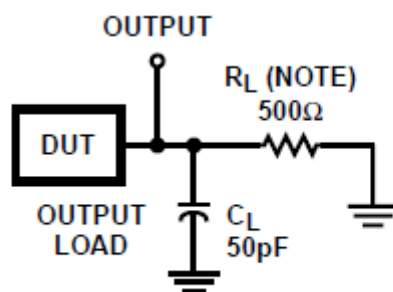


図 4-3. PROPAGATION DELAY TIMES



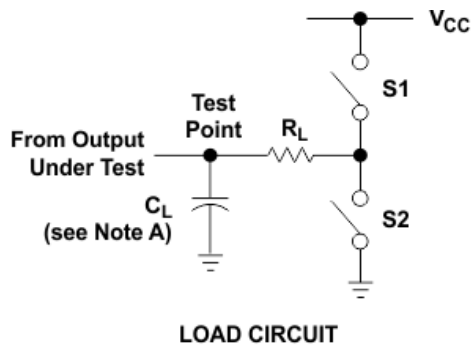
NOTE: For AC Series Only: When  $V_{CC} = 1.5V$ ,  $R_L = 1k\Omega$ .

表 4-1.

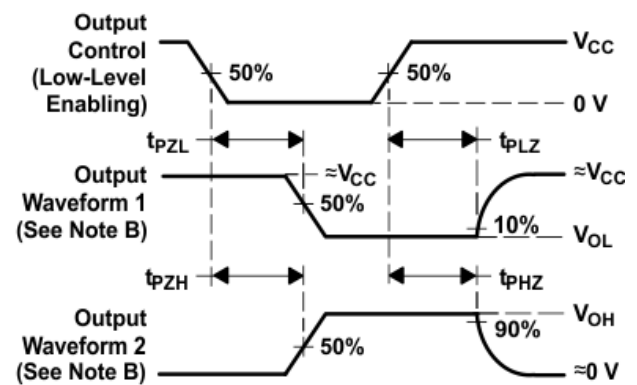
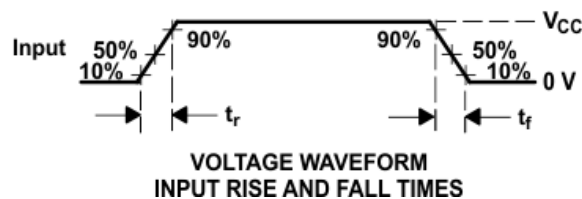
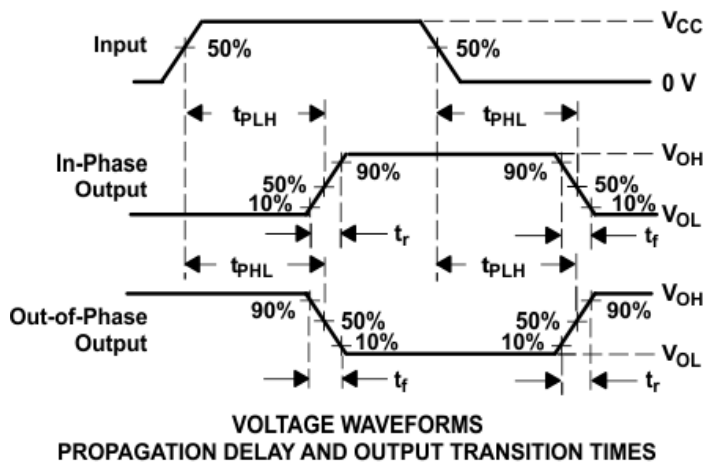
|                                 | AC           | ACT          |
|---------------------------------|--------------|--------------|
| Input Level                     | $V_{CC}$     | 3V           |
| Input Switching Voltage, $V_S$  | $0.5 V_{CC}$ | 1.5V         |
| Output Switching Voltage, $V_S$ | $0.5 V_{CC}$ | $0.5 V_{CC}$ |

図 4-4. PROPAGATION DELAY TIMES

## 5 Parameter Measurement Information



| PARAMETER         |           | $R_L$        | $C_L$           | S1     | S2     |
|-------------------|-----------|--------------|-----------------|--------|--------|
| $t_{en}$          | $t_{pZH}$ | 1 k $\Omega$ | 50 pF or 150 pF | Open   | Closed |
|                   | $t_{pZL}$ |              |                 | Closed | Open   |
| $t_{dis}$         | $t_{pHZ}$ | 1 k $\Omega$ | 50 pF           | Open   | Closed |
|                   | $t_{pLZ}$ |              |                 | Closed | Open   |
| $t_{pd}$ or $t_t$ |           | --           | 50 pF or 150 pF | Open   | Open   |

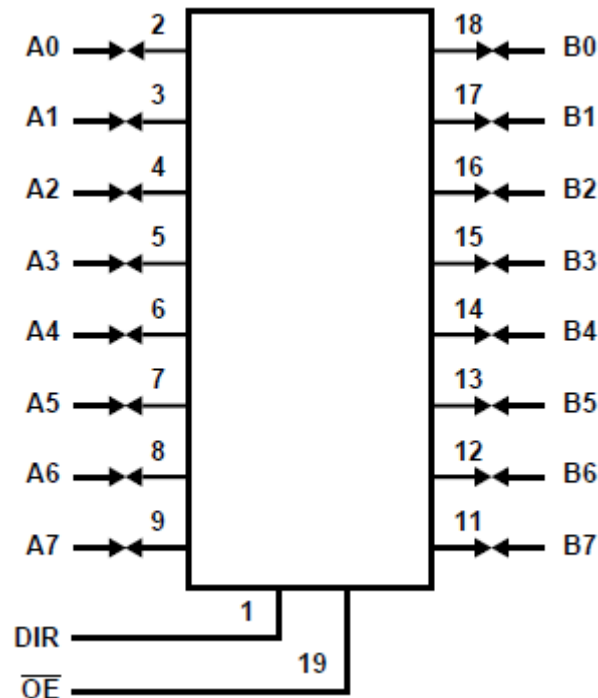


## 6 Detailed Description

### 6.1 Overview

The 'AC245 and 'ACT245 are non-inverting three-state bidirectional transceiver-buffers intended for two-way transmission from “A” bus to “B” bus or “B” bus to “A”. The logic level present on the direction input (DIR) determines the data direction. When the output enable input ( $\overline{OE}$ ) is HIGH, the outputs are in the high-impedance state.

### 6.2 Functional Block Diagram



Logic Diagram (Positive Logic)

### 6.3 Device Functional Modes

[Function Table](#) lists the function modes of the CDx4AC245, CDx4ACT245.

**表 6-1. Function Table**

| INPUTS <sup>(1)</sup> |     | OPERATION       |
|-----------------------|-----|-----------------|
| OE                    | DIR |                 |
| L                     | L   | B data to A bus |
| L                     | H   | A data to B bus |
| H                     | X   | Isolation       |

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care

## 7 Application and Implementation

### 注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

### 7.1 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [セクション 4.2](#).

Each  $V_{CC}$  pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1  $\mu\text{F}$  is recommended; if there are multiple  $V_{CC}$  pins, then 0.01  $\mu\text{F}$  or 0.022  $\mu\text{F}$  is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1  $\mu\text{F}$  and a 1  $\mu\text{F}$  are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

### 7.2 Layout

#### 7.2.1 Layout Guidelines

When using multiple-bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. [セクション 7.2.2](#) specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the IOs, so they cannot float when disabled.

#### 7.2.2 Layout Example

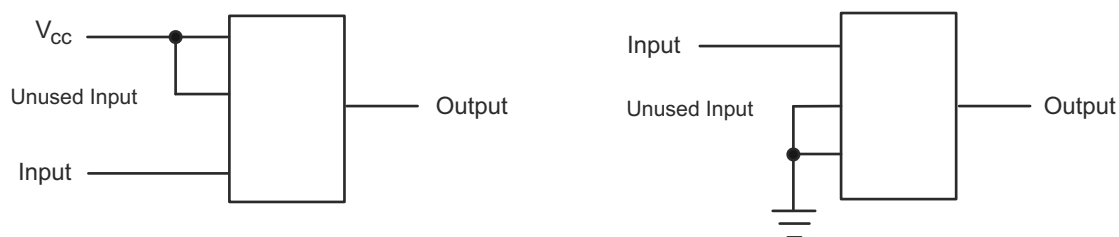


図 7-1. Layout Diagram

## 8 Device and Documentation Support

### 8.1 Documentation Support

#### 8.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 8-1. Related Links

| PARTS      | PRODUCT FOLDER             | SAMPLE & BUY               | TECHNICAL DOCUMENTS        | TOOLS & SOFTWARE           | SUPPORT & COMMUNITY        |
|------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| CD54AC245  | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| CD74AC245  | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| CD54ACT245 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| CD74ACT245 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |

### 8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[www.tij.co.jp](http://www.tij.co.jp) のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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### 8.6 用語集

#### テキサス・インスツルメンツ用語集

この用語集には、用語や略語の一覧および定義が記載されています。

## 9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| Changes from Revision C (May 2023) to Revision D (April 2024)                    | Page |
|----------------------------------------------------------------------------------|------|
| 「アプリケーションと実装」セクション、「デバイスおよびドキュメントのサポート」セクション、「製品情報」表のパッケージサイズを追加.....            | 1    |
| Updated RθJA values: DW = 58 to 98.6, DB = 70 to 105.4, all values in °C/W ..... | 4    |

**Changes from Revision B (April 2002) to Revision C (May 2023)****Page**

- 「パッケージ情報」表、「ピンの機能」表、「熱に関する情報」表を追加 ..... 1

**10 Mechanical, Packaging, and Orderable Information**

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable part number          | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|--------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">CD54AC245F3A</a>   | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | CD54AC245F3A        |
| CD54AC245F3A.A                 | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | CD54AC245F3A        |
| <a href="#">CD54ACT245F3A</a>  | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | CD54ACT245F3A       |
| CD54ACT245F3A.A                | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | CD54ACT245F3A       |
| <a href="#">CD74AC245E</a>     | Active        | Production           | PDIP (N)   20  | 20   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD74AC245E          |
| CD74AC245E.A                   | Active        | Production           | PDIP (N)   20  | 20   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD74AC245E          |
| CD74AC245EE4                   | Active        | Production           | PDIP (N)   20  | 20   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD74AC245E          |
| <a href="#">CD74AC245M</a>     | Obsolete      | Production           | SOIC (DW)   20 | -                     | -           | Call TI                              | Call TI                           | -55 to 125   | AC245M              |
| <a href="#">CD74AC245M96</a>   | Active        | Production           | SOIC (DW)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | AC245M              |
| CD74AC245M96.A                 | Active        | Production           | SOIC (DW)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | AC245M              |
| <a href="#">CD74ACT245E</a>    | Active        | Production           | PDIP (N)   20  | 20   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD74ACT245E         |
| CD74ACT245E.A                  | Active        | Production           | PDIP (N)   20  | 20   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD74ACT245E         |
| CD74ACT245EE4                  | Active        | Production           | PDIP (N)   20  | 20   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD74ACT245E         |
| <a href="#">CD74ACT245M</a>    | Obsolete      | Production           | SOIC (DW)   20 | -                     | -           | Call TI                              | Call TI                           | -55 to 125   | ACT245M             |
| <a href="#">CD74ACT245M96</a>  | Active        | Production           | SOIC (DW)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | (ACT245, ACT245M)   |
| CD74ACT245M96.A                | Active        | Production           | SOIC (DW)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | (ACT245, ACT245M)   |
| <a href="#">CD74ACT245SM96</a> | Active        | Production           | SSOP (DB)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | (ACT245, ACT245SM)  |
| CD74ACT245SM96.A               | Active        | Production           | SSOP (DB)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | (ACT245, ACT245SM)  |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF CD54AC245, CD54ACT245, CD74AC245, CD74ACT245 :**

- Catalog : [CD74AC245](#), [CD74ACT245](#)
- Military : [CD54AC245](#), [CD54ACT245](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD74AC245M96   | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| CD74ACT245M96  | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.9    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| CD74ACT245M96  | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| CD74ACT245SM96 | SSOP         | DB              | 20   | 2000 | 330.0              | 16.4               | 8.2     | 7.5     | 2.5     | 12.0    | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



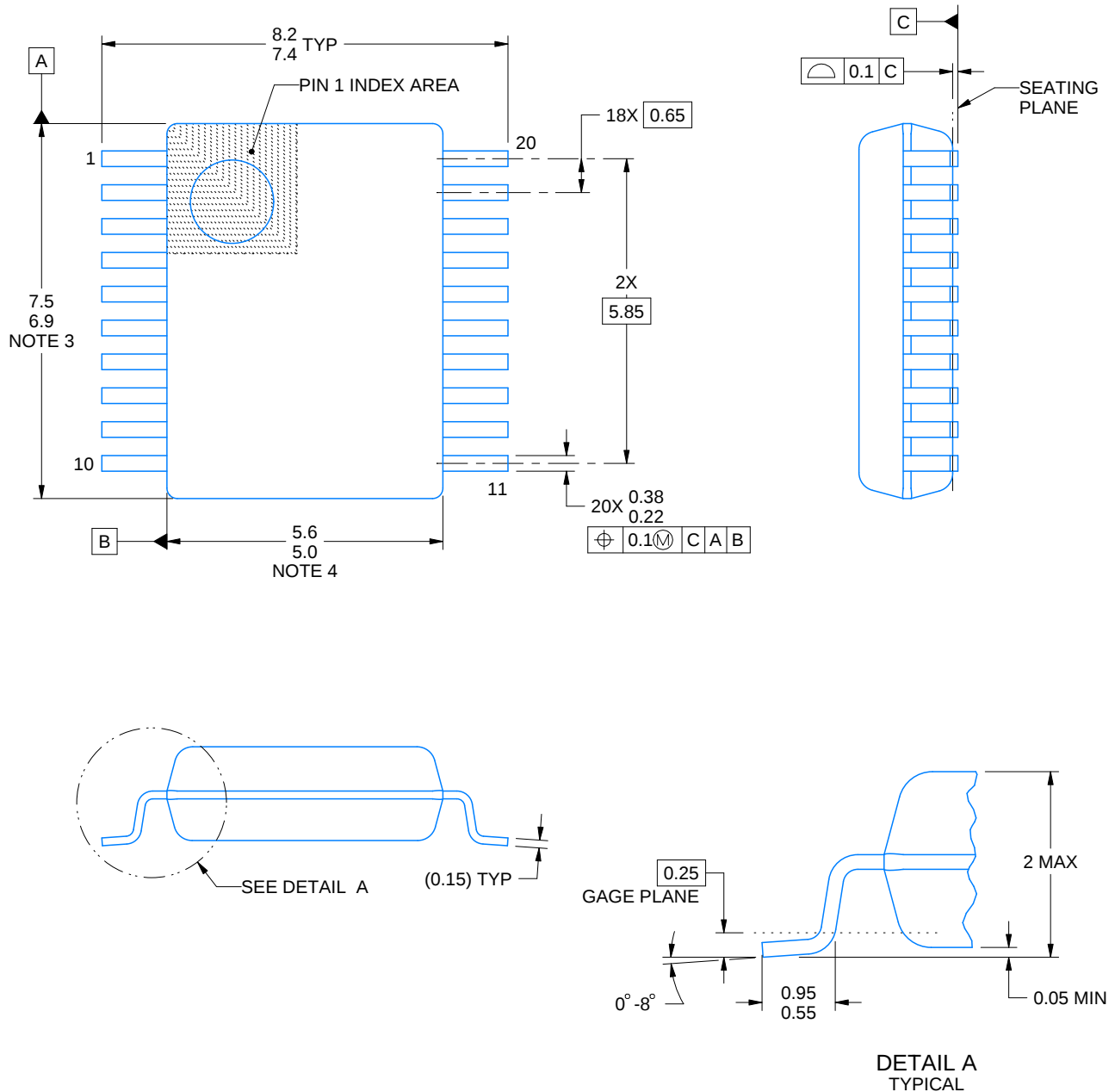
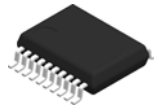
\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD74AC245M96   | SOIC         | DW              | 20   | 2000 | 356.0       | 356.0      | 45.0        |
| CD74ACT245M96  | SOIC         | DW              | 20   | 2000 | 356.0       | 356.0      | 45.0        |
| CD74ACT245M96  | SOIC         | DW              | 20   | 2000 | 356.0       | 356.0      | 45.0        |
| CD74ACT245SM96 | SSOP         | DB              | 20   | 2000 | 353.0       | 353.0      | 32.0        |

**TUBE**


\*All dimensions are nominal

| Device        | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|---------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| CD74AC245E    | N            | PDIP         | 20   | 20  | 506    | 13.97  | 11230  | 4.32   |
| CD74AC245E.A  | N            | PDIP         | 20   | 20  | 506    | 13.97  | 11230  | 4.32   |
| CD74AC245EE4  | N            | PDIP         | 20   | 20  | 506    | 13.97  | 11230  | 4.32   |
| CD74ACT245E   | N            | PDIP         | 20   | 20  | 506    | 13.97  | 11230  | 4.32   |
| CD74ACT245E.A | N            | PDIP         | 20   | 20  | 506    | 13.97  | 11230  | 4.32   |
| CD74ACT245EE4 | N            | PDIP         | 20   | 20  | 506    | 13.97  | 11230  | 4.32   |



4214851/B 08/2019

## NOTES:

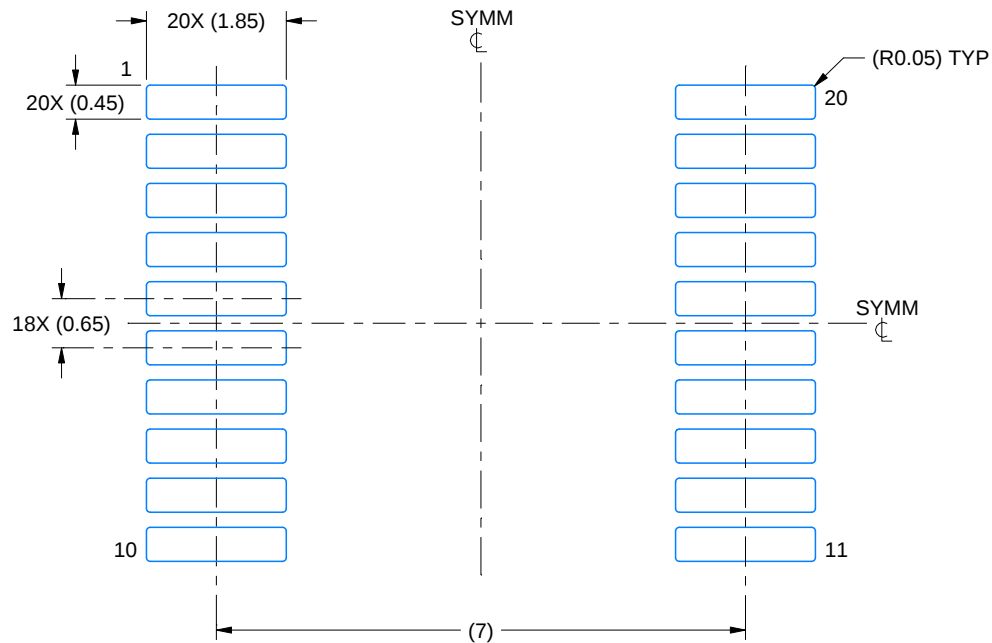
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

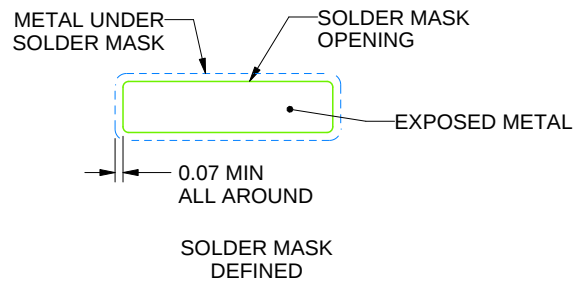
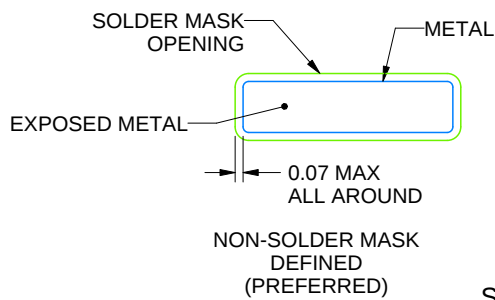
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

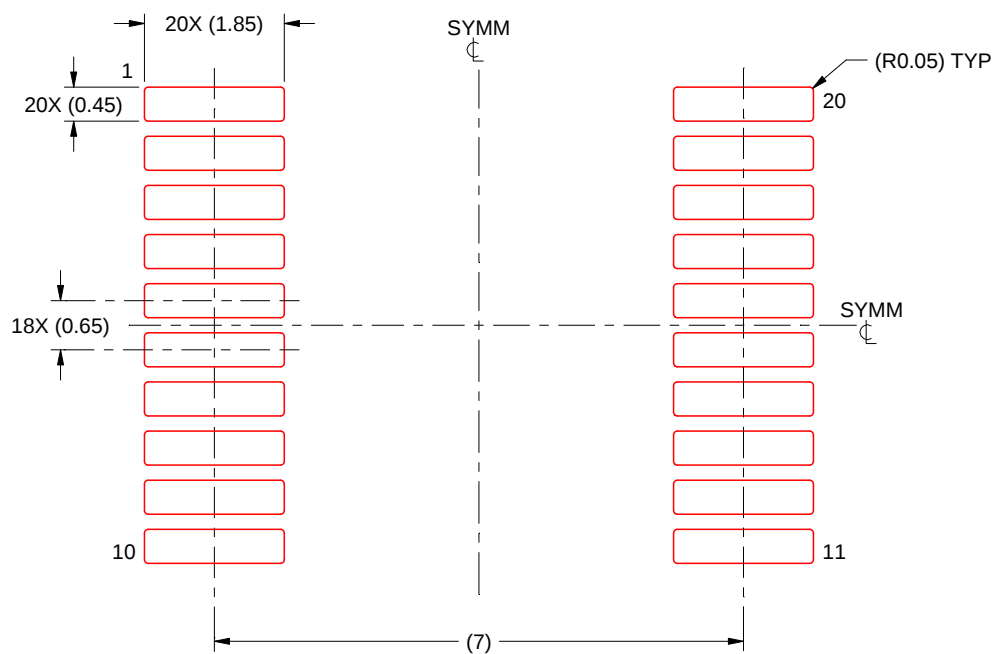
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

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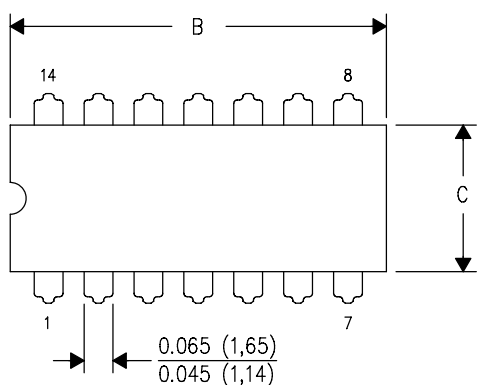
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

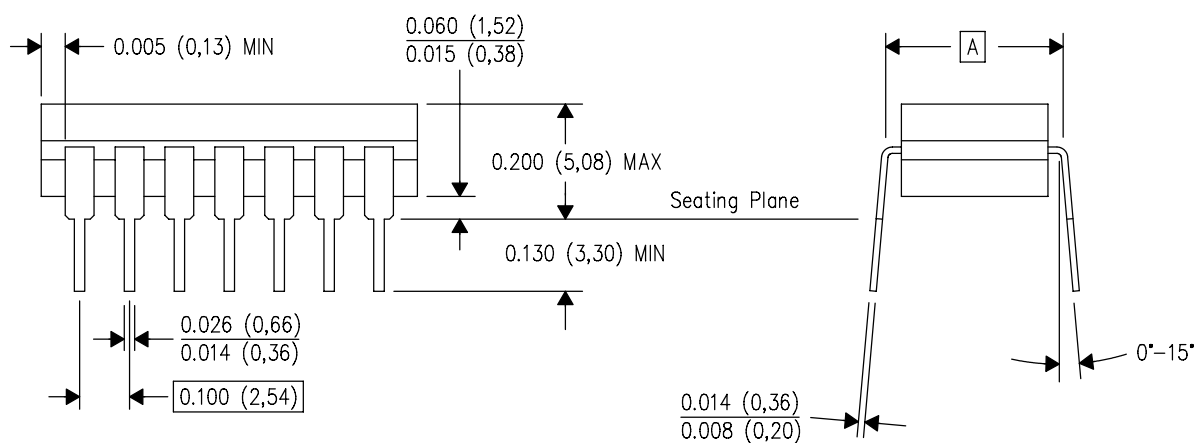
J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



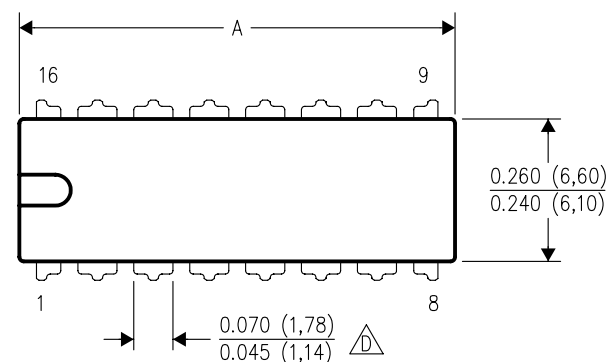
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

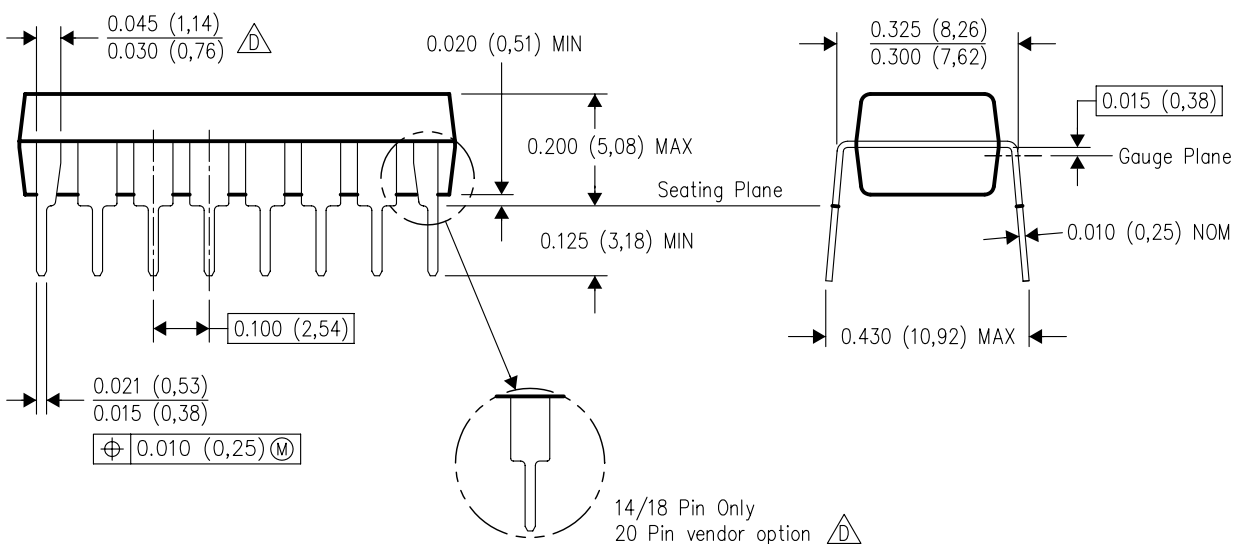
N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **<br>DIM      | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



4040049/E 12/2002

NOTES:

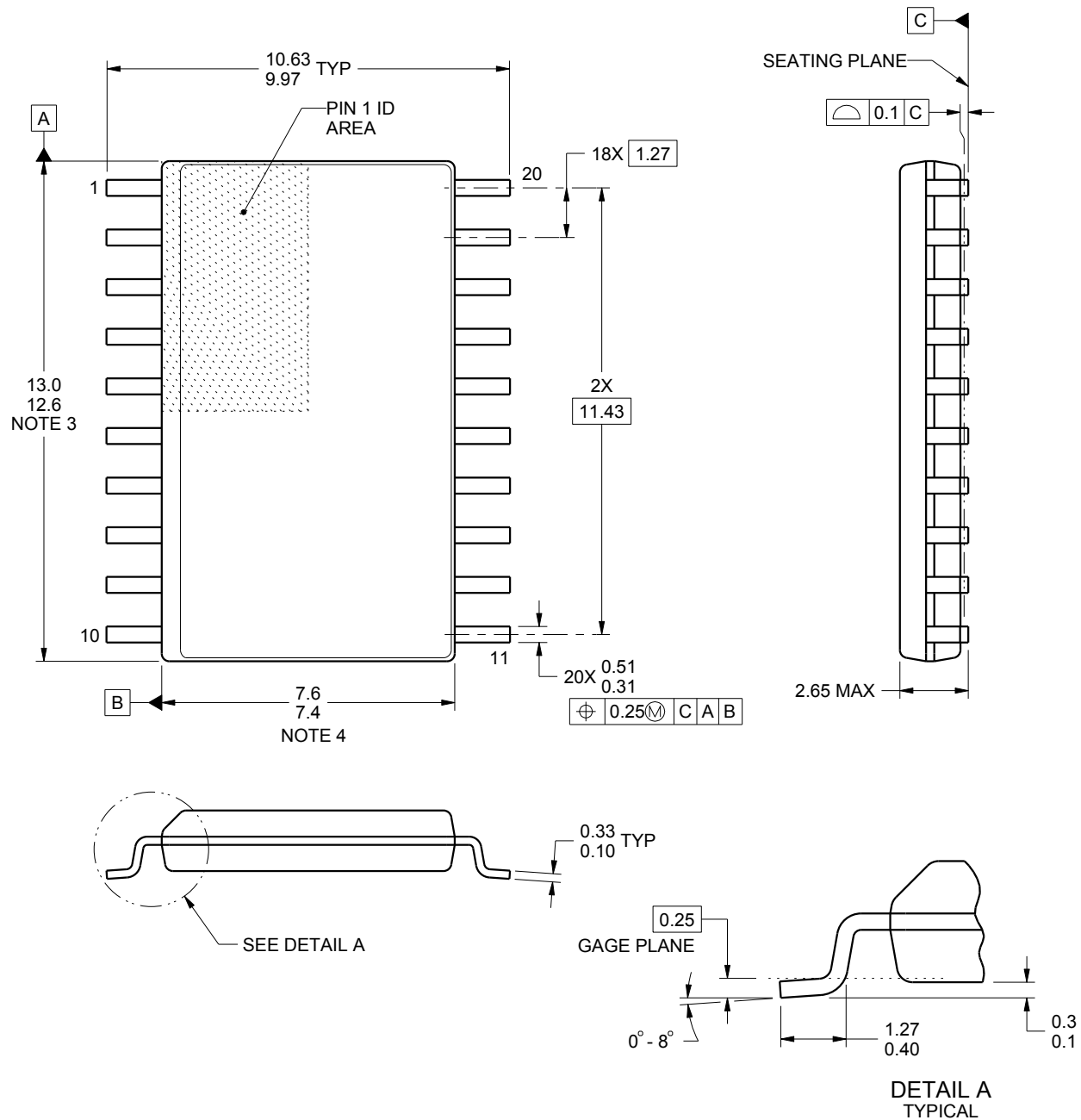
- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

**DW0020A**

## PACKAGE OUTLINE

**SOIC - 2.65 mm max height**

SOIC



4220724/A 05/2016

NOTES:

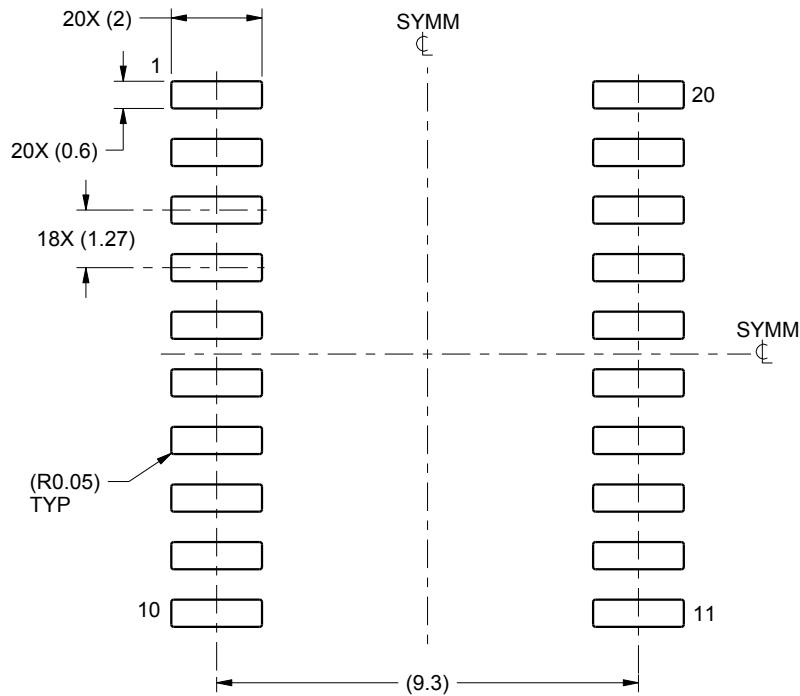
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

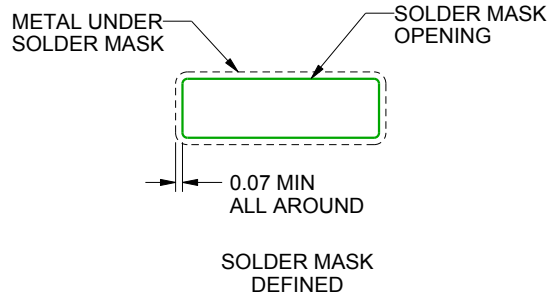
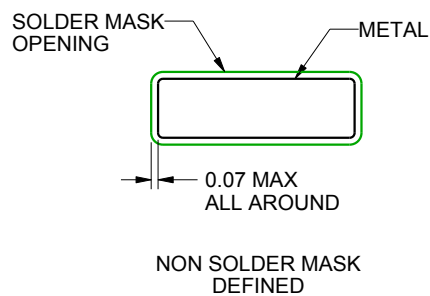
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

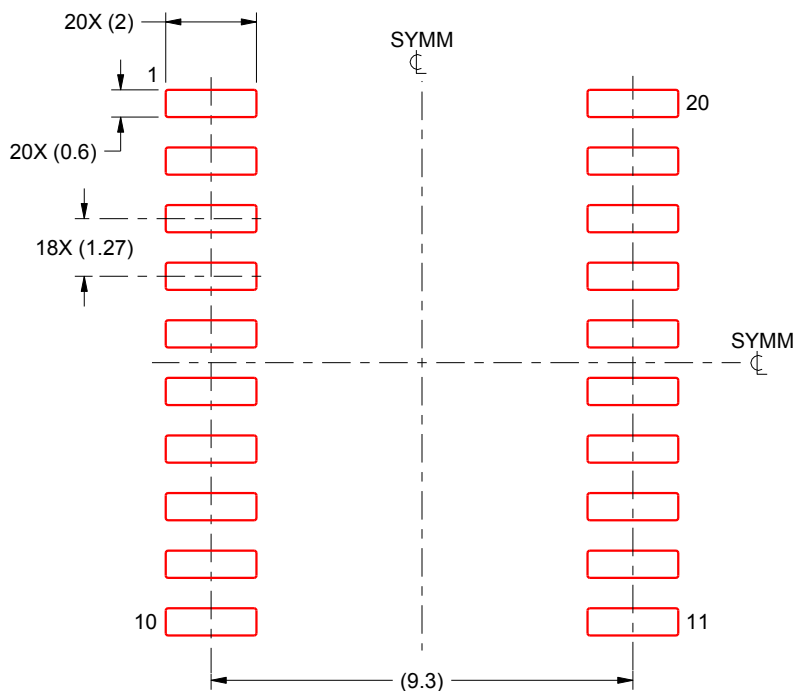
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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