

CDx4HC4094、CD74HCT4094 高速 CMOS ロジック 8 段シフトおよびストア・バス・レジスタ、3 ステート

1 特長

- バッファ付き入力
- カスケード接続のため、正と負のクロック・エッジに同期する個別のシリアル出力
- ファンアウト (全温度範囲にわたって)
 - 標準出力: 10 個の LSTTL 負荷
 - バス・ドライバ出力: 15 個の LSTTL 負荷
- 広い動作電圧範囲: $-55^{\circ}\text{C} \sim 125^{\circ}\text{C}$
- 平衡のとれた伝搬遅延と遷移時間
- LSTTL ロジック IC に比べて消費電力を大幅削減
- HC タイプ
 - 2V~6V で動作
 - 優れたノイズ耐性: V_{CC} に対して $N_{\text{IL}} = 30\%$ 、 $N_{\text{IH}} = 30\%$ ($V_{\text{CC}} = 5\text{V}$ 時)
- HCT タイプ
 - 4.5V~5.5V で動作
 - LSTTL 入力ロジックと直接互換、 $V_{\text{IL}} = 0.8\text{V}$ (最大値)、 $V_{\text{IH}} = 2\text{V}$ (最小値)
 - CMOS 入力互換、 V_{OL} 、 V_{OH} で $I_{\text{I}} \leq 1\mu\text{A}$

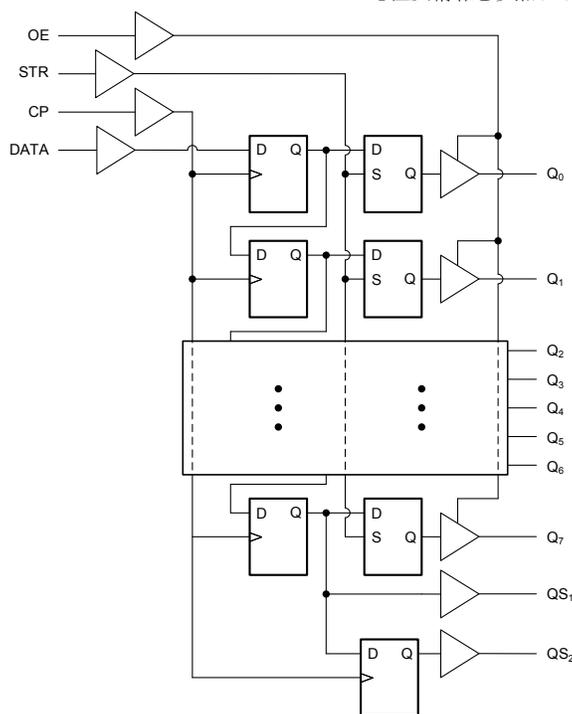
2 説明

CDx4HC4094 および CD74HCT4094 は、8 段のシリアル・シフト・レジスタで、シリアル入力からパラレル・バッファ付きトライステート出力へのストロブ・データ用として各段にストレージ・ラッチを備えています。パラレル出力は、共通のバス・ラインに直接接続できます。正のクロック遷移時にデータがシフトされます。シフト・レジスタの各ステージのデータは、ストロブ入力が高レベルのときにストレージ・レジスタへ転送されます。ストレージ・レジスタのデータは、出力イネーブル信号が高レベルのとき、常に出力に現れません。

デバイス情報

部品番号	パッケージ ⁽¹⁾	本体サイズ (公称)
CD54HC4094F3A	CDIP (16)	24.38mm × 6.92mm
CD74HC4094M	SOIC (16)	9.90mm × 3.90mm
CD74HC4094E	PDIP (16)	19.31mm × 6.35mm
CD74HC4094NSR	SO (16)	6.20mm × 5.30mm
CD74HC4094PW	TSSOP (16)	5.00mm × 4.40mm
CD74HCT4094M	SOIC (16)	9.90mm × 3.90mm
CD74HCT4094E	PDIP (16)	19.31mm × 6.35mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



機能ブロック図



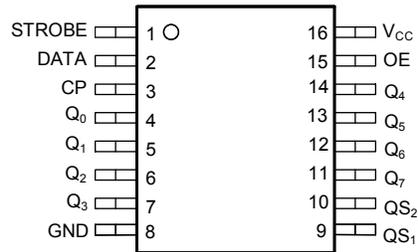
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3 Revision History

Changes from Revision E (December 2010) to Revision F (March 2022)	Page
• 最新のデータシート規格を反映するように、文書全体にわたって表、図、相互参照の採番方法を更新.....	1

4 Pin Configuration and Functions



J, N, D, NS, or PW package
16-Pin CDIP, PDIP, SOIC, SO, or TSSOP
Top View

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	-0.5	7	V
I _{IK}	Input diode current	For V _I < -0.5 V or V _I > V _{CC} + 0.5 V		±20 mA
I _{OK}	Output diode current	For V _O < -0.5 V or V _O > V _{CC} + 0.5 V		±20 mA
I _O	Output source or sink current per output pin	For V _O > -0.5 V or V _O < V _{CC} + 0.5 V		±25 mA
	Continuous current through V _{CC} or GND			±50 mA
T _J	Junction temperature			150 °C
T _{stg}	Storage temperature	-65	150	°C
	Maximum lead temperature (Soldering 10s) (SOIC - lead tips only)			300 °C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage range	HC types		6	V
		HCT types	4.5	5.5	
V _I , V _O	Input or output voltage	0		V _{CC}	V
t _t	Input rise and fall time	2 V		1000	ns
		4.5 V		500	
		6 V		400	
T _A	Temperature range	-55		125	°C

5.3 Thermal Information

THERMAL METRIC		N (PDIP)	D (SOIC) ⁽²⁾	NS (SOP)	PW (TSSOP)	UNIT
		PINS	PINS	PINS	PINS	
R _{θJA}	Junction-to-ambient thermal resistance ⁽¹⁾	67	73	64	108	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.
 (2) Lead tips only

5.4 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽²⁾	V _{CC} (V)	25°C			–40°C to 85°C		–55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
V _{IH}	High-level input voltage		2	1.5		1.5		1.5		V	
			4.5	3.15		3.15		3.15		V	
			6	4.2		4.2		4.2		V	
V _{IL}	Low-level input voltage		2		0.5		0.5		0.5	V	
			4.5		1.35		1.35		1.35	V	
			6		1.8		1.8		1.8	V	
V _{OH}	High-level output voltage CMOS loads	I _{OH} = –20µA	2	1.9		1.9		1.9		V	
		I _{OH} = –20µA	4.5	4.4		4.4		4.4		V	
		I _{OH} = –20µA	6	5.9		5.9		5.9		V	
	High-level output voltage TTL loads	I _{OH} = –6mA	4.5	3.98		3.84		3.7		V	
		I _{OH} = –7.8mA	6	5.48		5.34		5.2		V	
V _{OL}	Low-level output voltage CMOS loads	I _{OL} = 20µA	2		0.1		0.1		0.1	V	
		I _{OL} = 20µA	4.5		0.1		0.1		0.1	V	
		I _{OL} = 20µA	6		0.1		0.1		0.1	V	
	Low-level output voltage TTL loads	I _{OL} = 6mA	4.5		0.26		0.33		0.4	V	
		I _{OL} = 7.8mA	6		0.26		0.33		0.4	V	
I _I	Input leakage current	V _{CC} or GND	6		±0.1		±1		±1	µA	
I _{CC}	Supply current	V _{CC} or GND	6		8		80		160	µA	
HCT TYPES											
V _{IH}	High-level input voltage		4.5 to 5.5	2		2		2		V	
V _{IL}	Low-level input voltage		4.5 to 5.5		0.8		0.8		0.8	V	
V _{OH}	High-level output voltage CMOS loads	I _{OH} = –20µA	4.5	4.4		4.4		4.4		V	
	High-level output voltage TTL loads	I _{OH} = –6mA	4.5	3.98		3.84		3.7		V	
V _{OL}	Low-level output voltage CMOS loads	I _{OL} = 20µA	4.5		0.1		0.1		0.1	V	
	Low-level output voltage TTL loads	I _{OL} = 6mA	4.5		0.26		0.33		0.4	V	
I _I	Input leakage current	V _{CC} and GND	5.5		±0.1		±1		±1	µA	
I _{CC}	Supply Current	V _{CC} and GND	5.5		8		80		160	µA	
ΔI _{CC} ^{(1) (3)}	Additional quiescent device current per input pin: 1 unit load	D	4.5 to 5.5		40	144		180		196	µA
		CP, OE	4.5 to 5.5		150	540		675		735	µA
		STR	4.5 to 5.5		100	360		450		490	µA

(1) For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

(2) V_I = V_{IH} or V_{IL}, unless otherwise noted.

(3) Inputs held at V_{CC} – 2.1.

5.5 Prerequisite for Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		V _{CC} (V)	25°C		–40 to 85°C		–55 to 125°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
HC TYPES									
t _W	CP pulse duration	2	80	100	120	ns			
		4.5	16	20	24				
		6	14	17	20				
t _{WH}	STR pulse duration	2	80	100	120	ns			
		4.5	16	20	24				
		6	14	17	20				
t _{SU}	Data set-up time	2	50	65	75	ns			
		4.5	10	13	15				
		6	9	11	13				
t _H	Data hold time	2	3	3	3	ns			
		4.5	3	3	3				
		6	3	3	3				
t _{SU}	STR set-up time	2	100	125	150	ns			
		4.5	20	25	30				
		6	17	21	26				
t _H	STR hold time	2	0	0	0	ns			
		4.5	0	0	0				
		6	0	0	0				
f _{CL (MAX)}	Maximum CP frequency	2	6	5	4	MHz			
		4.5	30	24	20				
		6	35	28	24				
HCT TYPES									
t _W	CP pulse duration	4.5	16	20	24	ns			
t _{WH}	STR pulse duration	4.5	16	20	24	ns			
t _{SU}	Data set-up time	4.5	10	13	15	ns			
t _H	Data hold time	4.5	4	4	4	ns			
t _{SU}	STR set-up time	4.5	20	25	30	ns			
t _H	STR hold time	4.5	0	0	0	ns			
f _{CL (MAX)}	Maximum CP frequency	4.5	30	24	20	MHz			

5.6 Switching Characteristics

 Input t_r , t_f = 6 ns. Unless otherwise specified, CL = 50pF [Parameter Measurement Information](#)

PARAMETER		V _{CC} (V)	25°C			–40 to 85°C		–55 to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES										
t _{pd}	Propagation delay time CP to QS ₁	2		150		190		225	ns	
		4.5		12 ⁽³⁾	30		38	45		
		6		26		33		38		
t _{pd}	CP to QS ₂	2		135		170		205	ns	
		4.5		11 ⁽³⁾	27		34	41		
		6		23		29		35		
t _{pd}	CP to Q _n	2		195		245		295	ns	
		4.5		16 ⁽³⁾	39		49	59		
		6		33		42		50		
t _t	STR to Q _n	2		180		225		270	ns	
		4.5		36		45		54		
		6		31		38		46		
t _{PZH} , t _{PZL}	Output enable to Q _n	2		175		220		265	ns	
		4.5		35		44		53		
		6		30		37		45		
t _{PHZ} , t _{PLZ}	Output disable to Q _n	2		125		155		190	ns	
		4.5		25		31		38		
		6		21		26		32		
t _{TLH} , t _{THL}	Output transition time	2		75		95		110	ns	
		4.5		15		19		22		
		6		13		16		19		
t _{PHZ} , t _{PLZ}	Output disabling time	5		10 ⁽³⁾					ns	
f _{MAX}	Maximum CP frequency	5		60 ⁽³⁾					MHz	
C _{IN}	Input capacitance			10		10		10	pF	
C _{PD}	Power dissipation capacitance ^{(1), (2)}	5		90 ⁽³⁾					pF	
C _O	Tri-state output capacitance			15		15		15	pF	
HCT TYPES										
t _{PLH} , t _{PHL}	Propagation delay time CP to QS ₁	4.5		16 ⁽³⁾	39					ns
	CP to QS ₂	4.5		15 ⁽³⁾	36					ns
	CP to Q _n	4.5		18 ⁽³⁾	43					ns
	STR to Q _n	4.5			39					ns
t _{PZH} , t _{PZL}	Output enable to Q _n	4.5		35						ns
t _{PHZ} , t _{PLZ}	Output disable to Q _n	4.5		35						ns
t _{TLH} , t _{THL}	Output transition time	4.5		15						ns
t _{PHZ} , t _{PLZ}	Output disabling time	5		14 ⁽³⁾						ns
f _{MAX}	Maximum CP frequency	5		60 ⁽³⁾						MHz
C _{IN}	Input capacitance			10		10		10		pF

Input t_r , $t_f = 6$ ns. Unless otherwise specified, $C_L = 50$ pF [Parameter Measurement Information](#)

PARAMETER		V_{CC} (V)	25°C			-40 to 85°C		-55 to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
C_{PD}	Power dissipation capacitance ⁽¹⁾ , (2)	5	110 ⁽³⁾							pF
C_O	Tri-state output capacitance				15		15		15	pF

- (1) C_{PD} is used to determine the dynamic power consumption, per register.
- (2) $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = Input frequency, C_L = Output load capacitance, V_{CC} = Supply voltage.
- (3) Typical value tested at 5V, $C_L = 15$ pF

6 Parameter Measurement Information

t_{PD} is the maximum between t_{PLH} and t_{PHL}

t_t is the maximum between t_{TLH} and t_{THL}

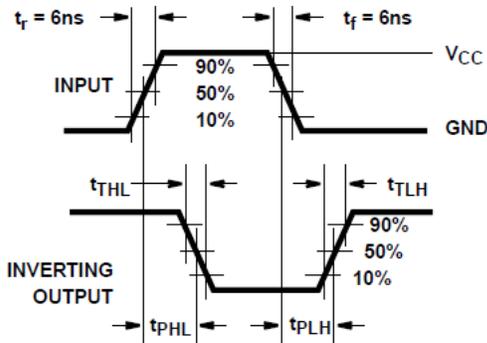


FIG 6-1. HC and HCT transition times and propagation delay times, combination logic

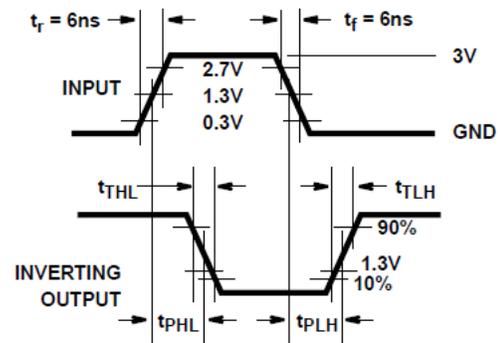


FIG 6-2. HCT transition times and propagation delay times, combination logic

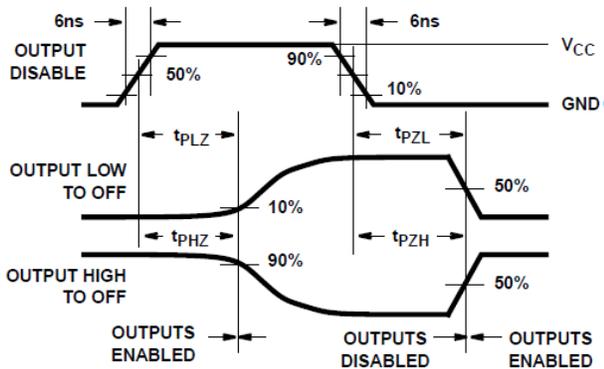


FIG 6-3. HC three-state propagation delay waveform

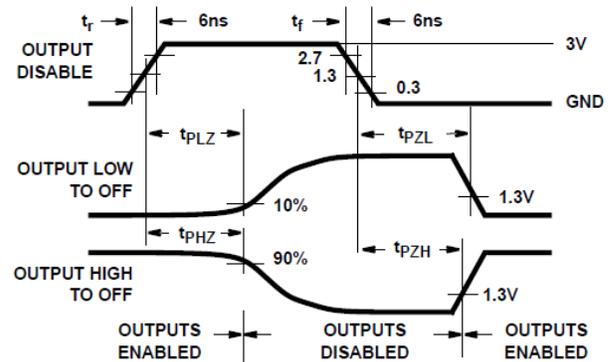
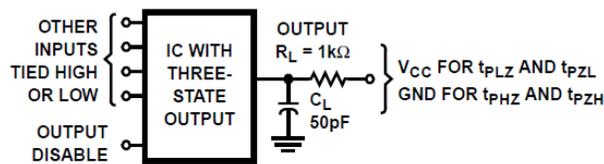


FIG 6-4. HCT three-state propagation delay waveform



NOTE: Open drain waveforms t_{PLZ} and t_{PZL} are the same as those for three-state shown on the left. The test circuit is Output $R_L = 1k\Omega$ to V_{CC} , $C_L = 50pF$.

FIG 6-5. HC and HCT three-state propagation delay test circuit

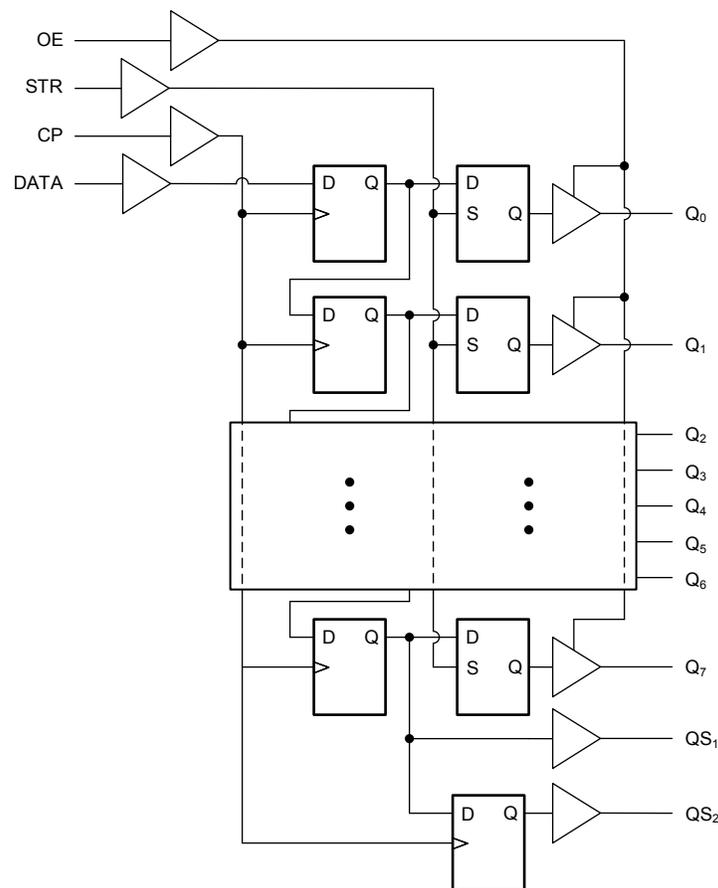
7 Detailed Description

7.1 Overview

The CDx4HC4094 and CD74HCT4094 are 8-stage serial shift registers having a storage latch associated with each stage for strobing data from the serial input to parallel buffered tri-state outputs. The parallel outputs may be connected directly to common bus lines. Data is shifted on positive clock transitions. The data in each shift register stage is transferred to the storage register when the Strobe input is high. Data in the storage register appears at the outputs whenever the Output-Enable signal is high.

Two serial outputs are available for cascading a number of these devices. Data is available at the QS₁ serial output terminal on positive clock edges to allow for high-speed operation in cascaded system in which the clock rise time is fast. The same serial information, available at the QS₂ terminal on the next negative clock edge, provides a means for cascading these devices when the clock rise time is slow.

7.2 Functional Block Diagram



7.3 Device Functional Modes

表 7-1. Truth Table

Inputs ⁽²⁾				Parallel Outputs		Serial Outputs	
CP	OE	STR	D	Q ₀	Q _n	QS ₁ ⁽¹⁾	QS ₂
↑	L	X	X	Z	Z	Q ₆	NC
↓	L	X	X	Z	Z	NC	Q ₇
↑	H	L	X	NC	NC	Q ₆	NC
↑	H	H	L	L	Q _n – 1	Q ₆	NC
↑	H	H	H	H	Q _n – 1	Q ₆	NC
↓	H	H	H	NC	NC	NC	Q ₇

- (1) At the positive clock edge the information in the seventh register stage is transferred to the eighth register stage and QS₁ output.
- (2) H = High voltage level, L = Low voltage level, X = Don't care, NC = No charge, Z = High-impedance off-state, ↑ = Transition from low-to-high level, ↓ = Transition from high to low.

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μF and 1- μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 サポート・リソース

[TI E2E™ サポート・フォーラム](#)は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の[使用条件](#)を参照してください。

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD54HC4094F3A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC4094F3A
CD54HC4094F3A.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC4094F3A
CD74HC4094DYYR	Active	Production	SOT-23-THIN (DYY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4094
CD74HC4094DYYR.A	Active	Production	SOT-23-THIN (DYY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HJ4094
CD74HC4094E	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC4094E
CD74HC4094E.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC4094E
CD74HC4094M	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	HC4094M
CD74HC4094M96	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-55 to 125	HC4094M
CD74HC4094M96.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4094M
CD74HC4094M96G3	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-55 to 125	HC4094M
CD74HC4094M96G3.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-55 to 125	HC4094M
CD74HC4094M96G4	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4094M
CD74HC4094M96G4.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4094M
CD74HC4094MT	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	HC4094M
CD74HC4094NSR	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4094M
CD74HC4094NSR.A	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4094M
CD74HC4094NSRE4	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4094M
CD74HC4094PW	Obsolete	Production	TSSOP (PW) 16	-	-	Call TI	Call TI	-55 to 125	HJ4094
CD74HC4094PWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-55 to 125	HJ4094
CD74HC4094PWR.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4094
CD74HC4094PWRE4	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4094
CD74HC4094PWRG4	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4094
CD74HC4094PWRG4.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4094
CD74HCT4094E	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT4094E
CD74HCT4094E.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT4094E
CD74HCT4094EE4	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT4094E
CD74HCT4094M	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	HCT4094M
CD74HCT4094M96	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-55 to 125	HCT4094M

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD74HCT4094M96.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4094M

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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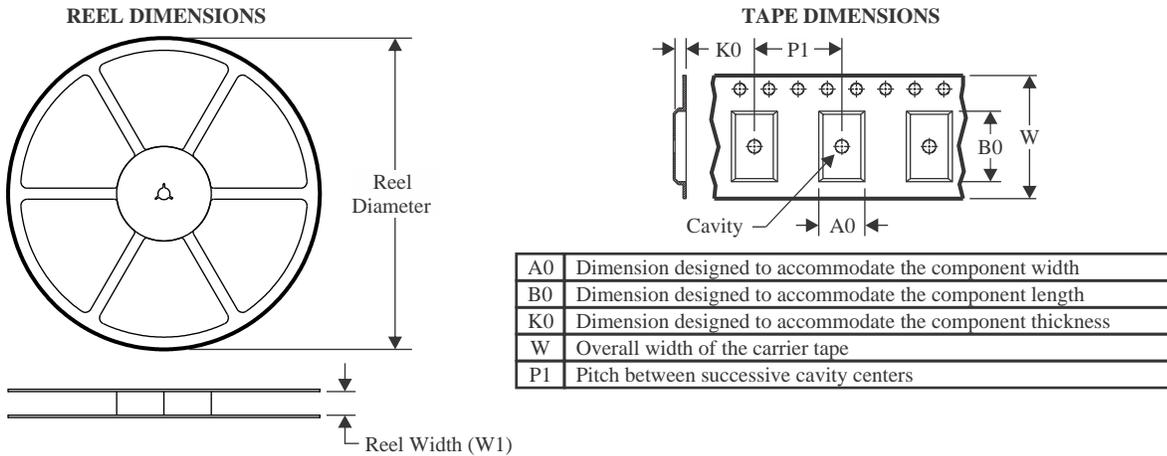
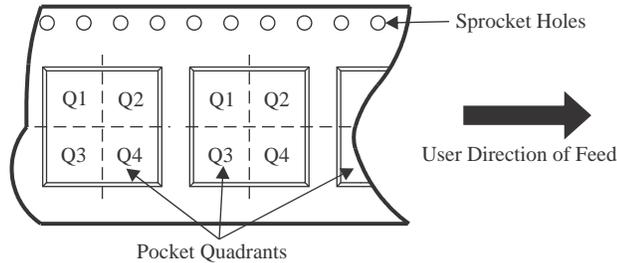
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD54HC4094, CD74HC4094 :

- Catalog : [CD74HC4094](#)
- Military : [CD54HC4094](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


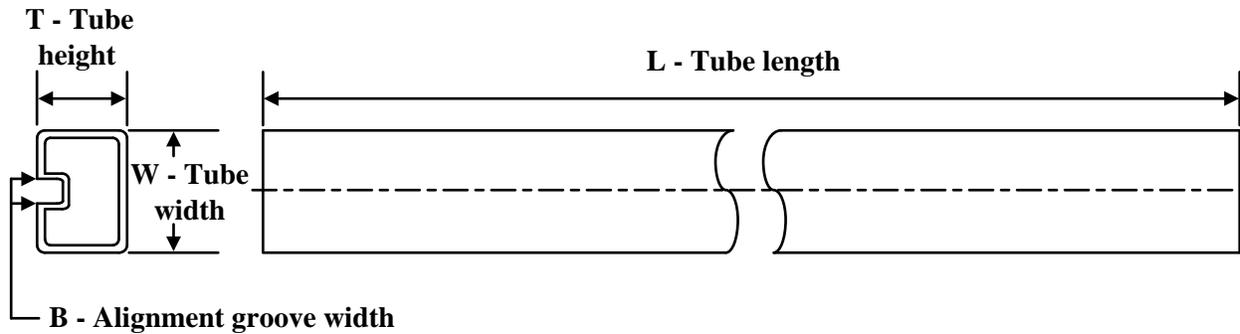
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC4094DYR	SOT-23-THIN	DYY	16	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
CD74HC4094M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC4094M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC4094M96G3	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC4094M96G4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC4094NSR	SOP	NS	16	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
CD74HC4094NSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
CD74HC4094PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4094PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4094PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4094PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HCT4094M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC4094DYYR	SOT-23-THIN	DYY	16	3000	336.6	336.6	31.8
CD74HC4094M96	SOIC	D	16	2500	340.5	336.1	32.0
CD74HC4094M96	SOIC	D	16	2500	340.5	336.1	32.0
CD74HC4094M96G3	SOIC	D	16	2500	364.0	364.0	27.0
CD74HC4094M96G4	SOIC	D	16	2500	353.0	353.0	32.0
CD74HC4094NSR	SOP	NS	16	2000	353.0	353.0	32.0
CD74HC4094NSR	SOP	NS	16	2000	353.0	353.0	32.0
CD74HC4094PWR	TSSOP	PW	16	2000	353.0	353.0	32.0
CD74HC4094PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
CD74HC4094PWR	TSSOP	PW	16	2000	353.0	353.0	32.0
CD74HC4094PWRG4	TSSOP	PW	16	2000	353.0	353.0	32.0
CD74HCT4094M96	SOIC	D	16	2500	353.0	353.0	32.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD74HC4094E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC4094E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC4094E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC4094E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT4094E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT4094E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT4094E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT4094E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT4094EE4	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT4094EE4	N	PDIP	16	25	506	13.97	11230	4.32

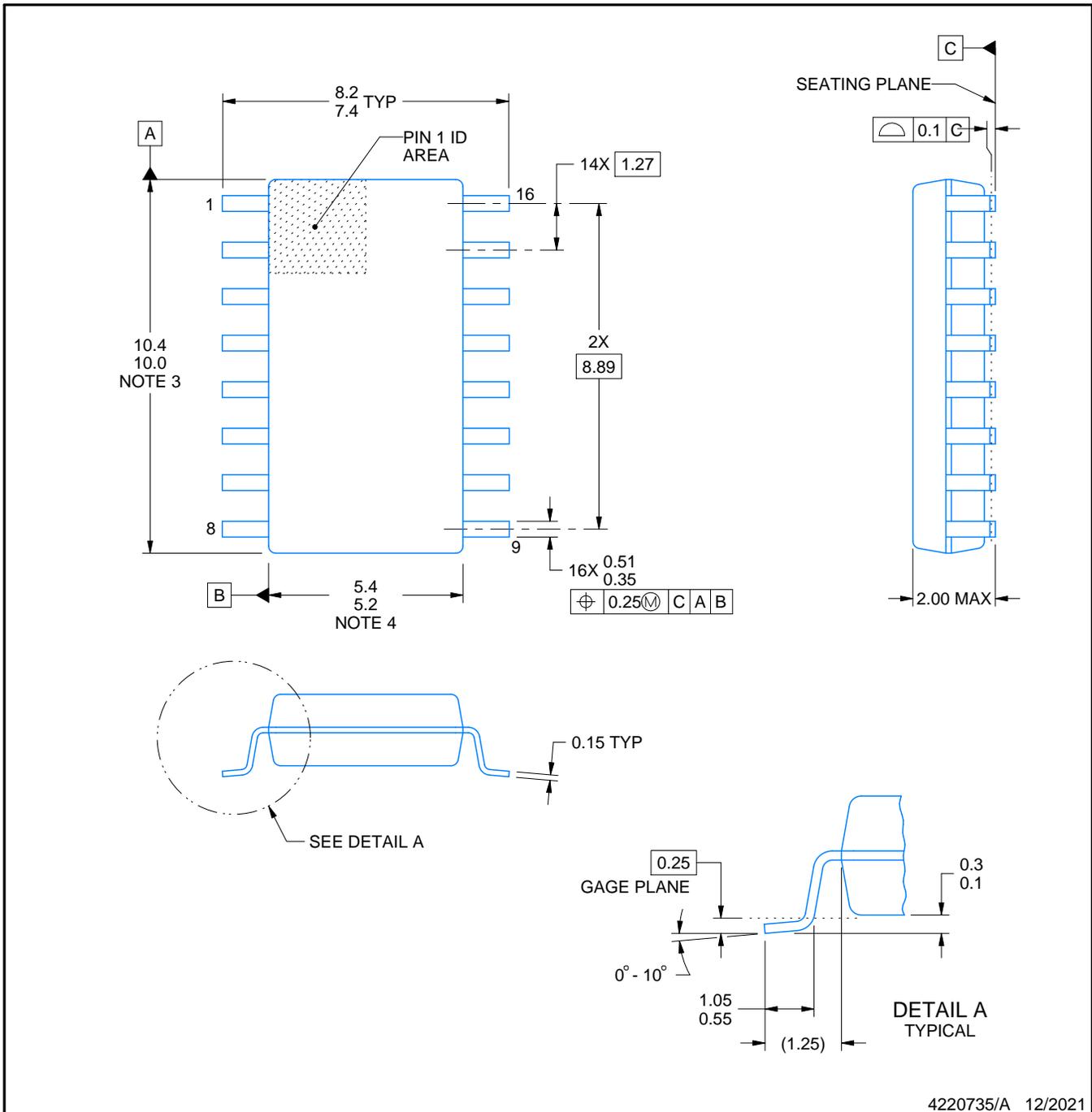


PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



NOTES:

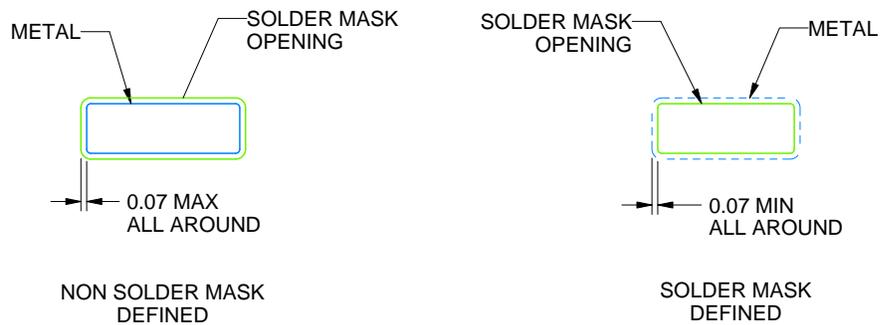
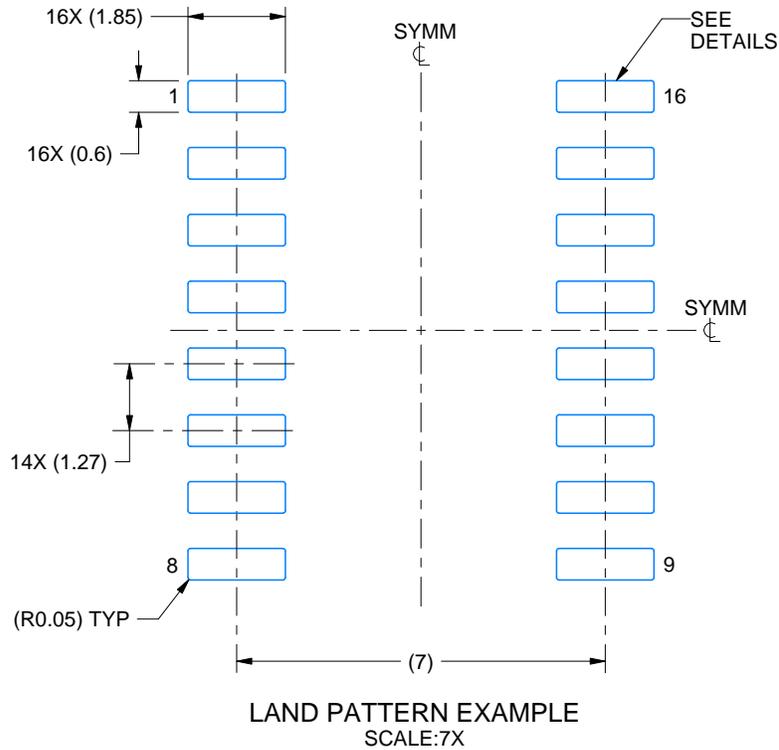
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

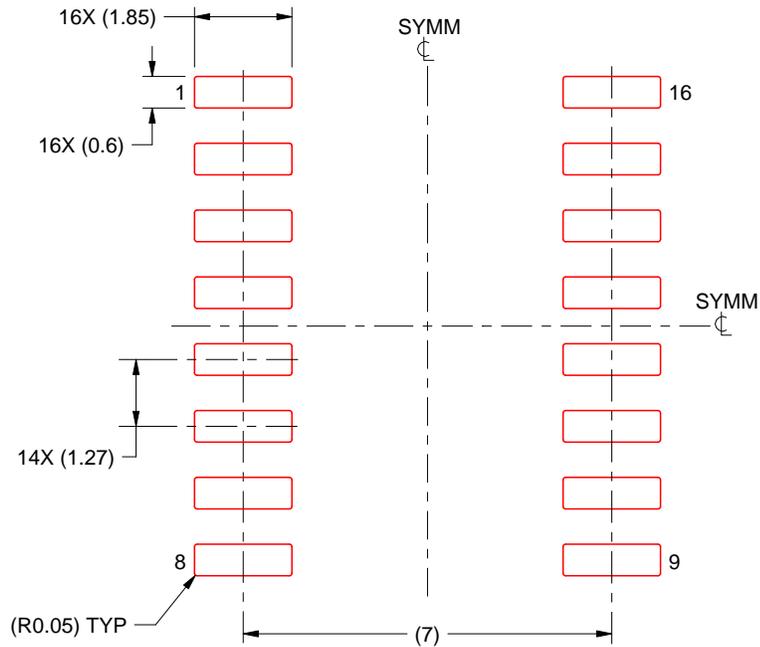
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP

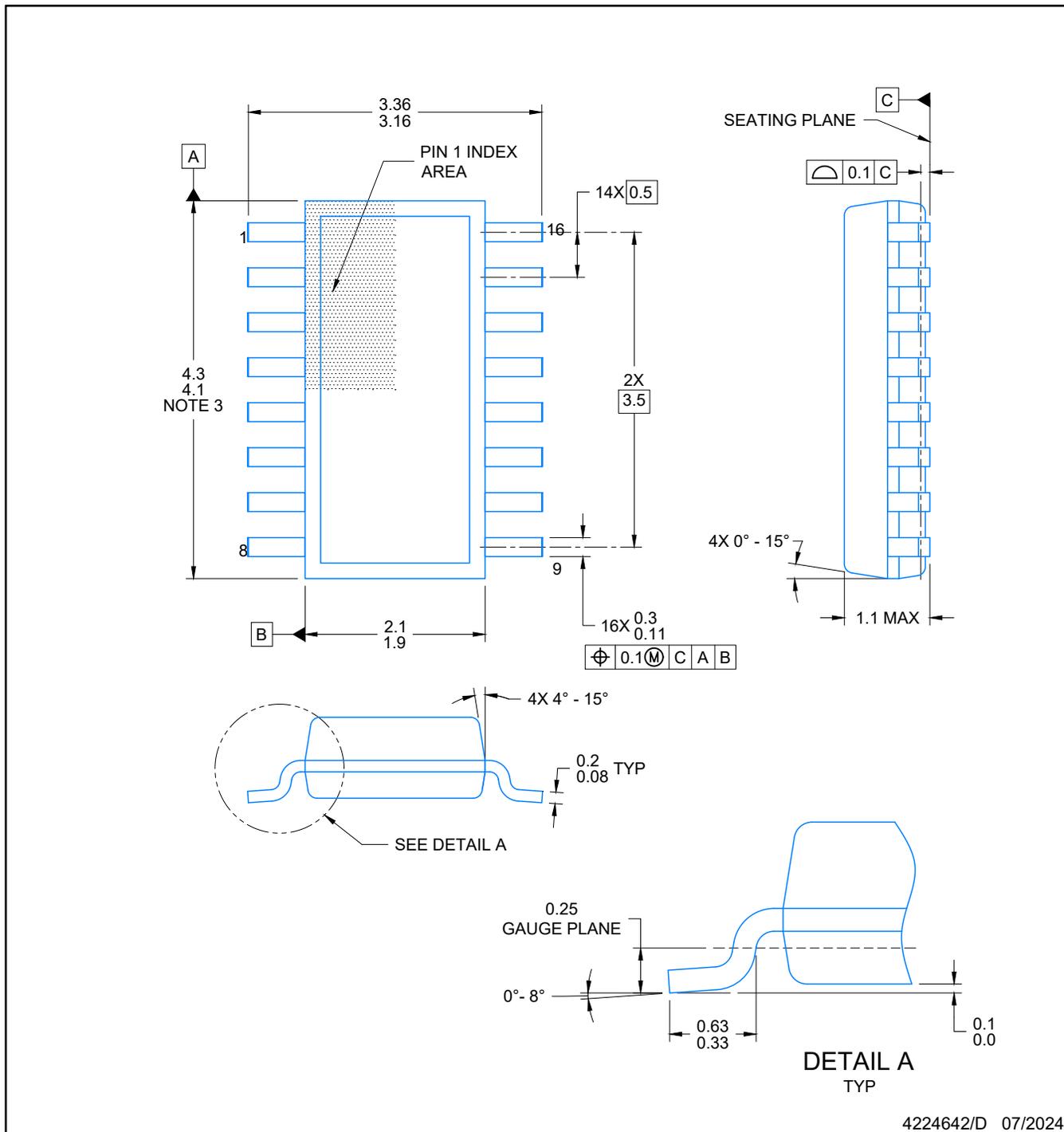


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

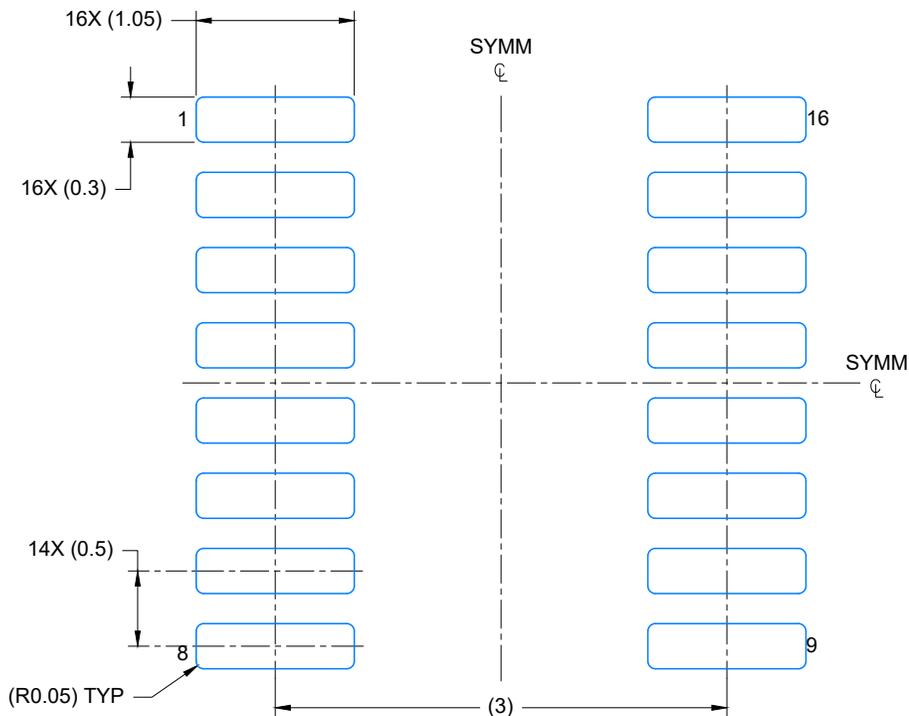
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



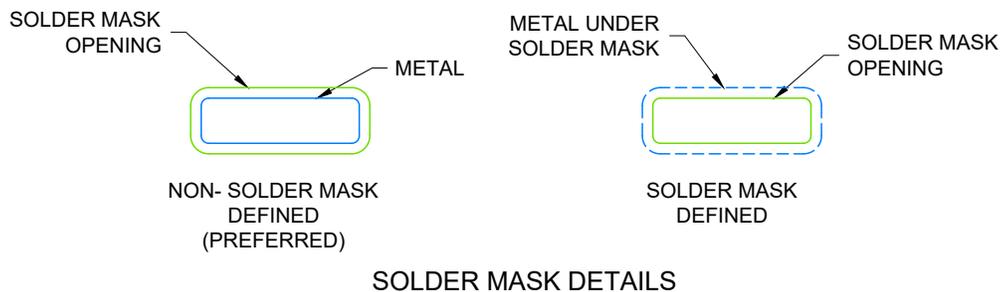
4224642/D 07/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AA



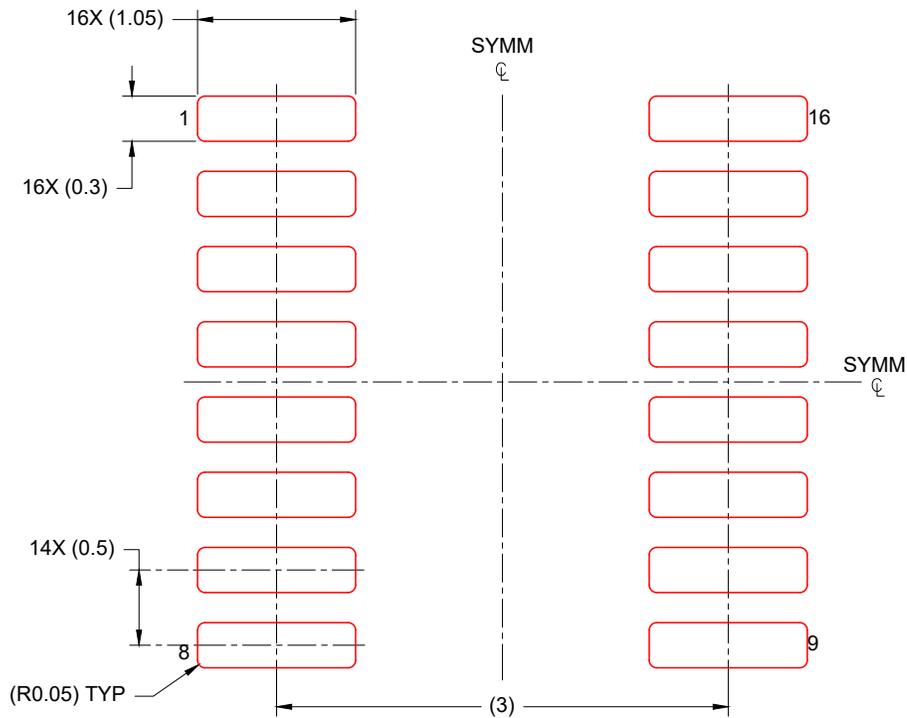
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224642/D 07/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224642/D 07/2024

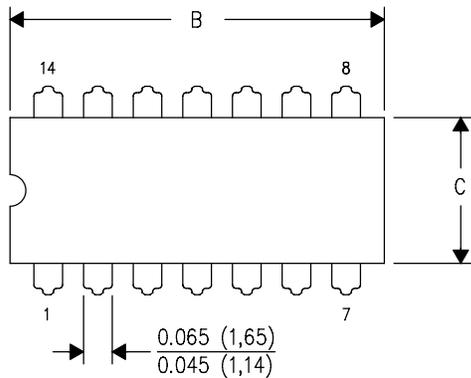
NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.

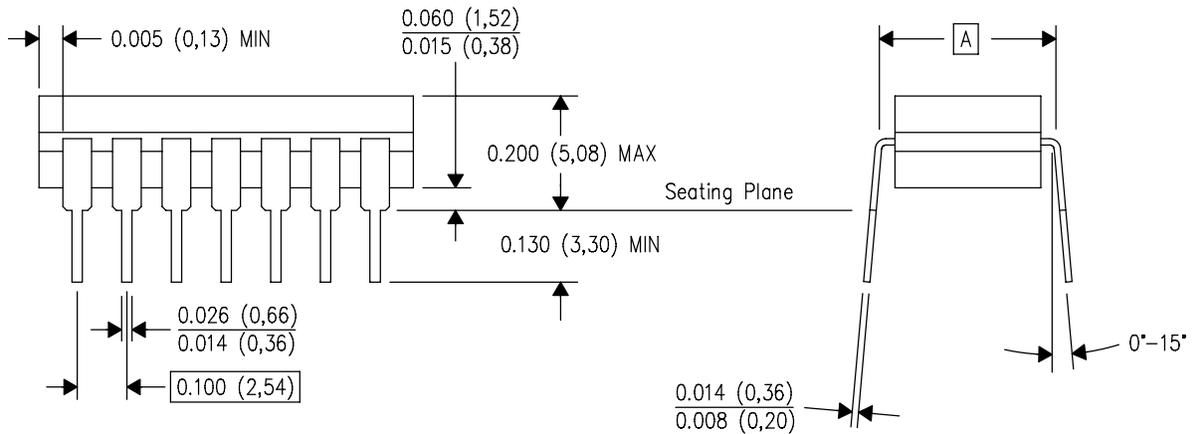
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE

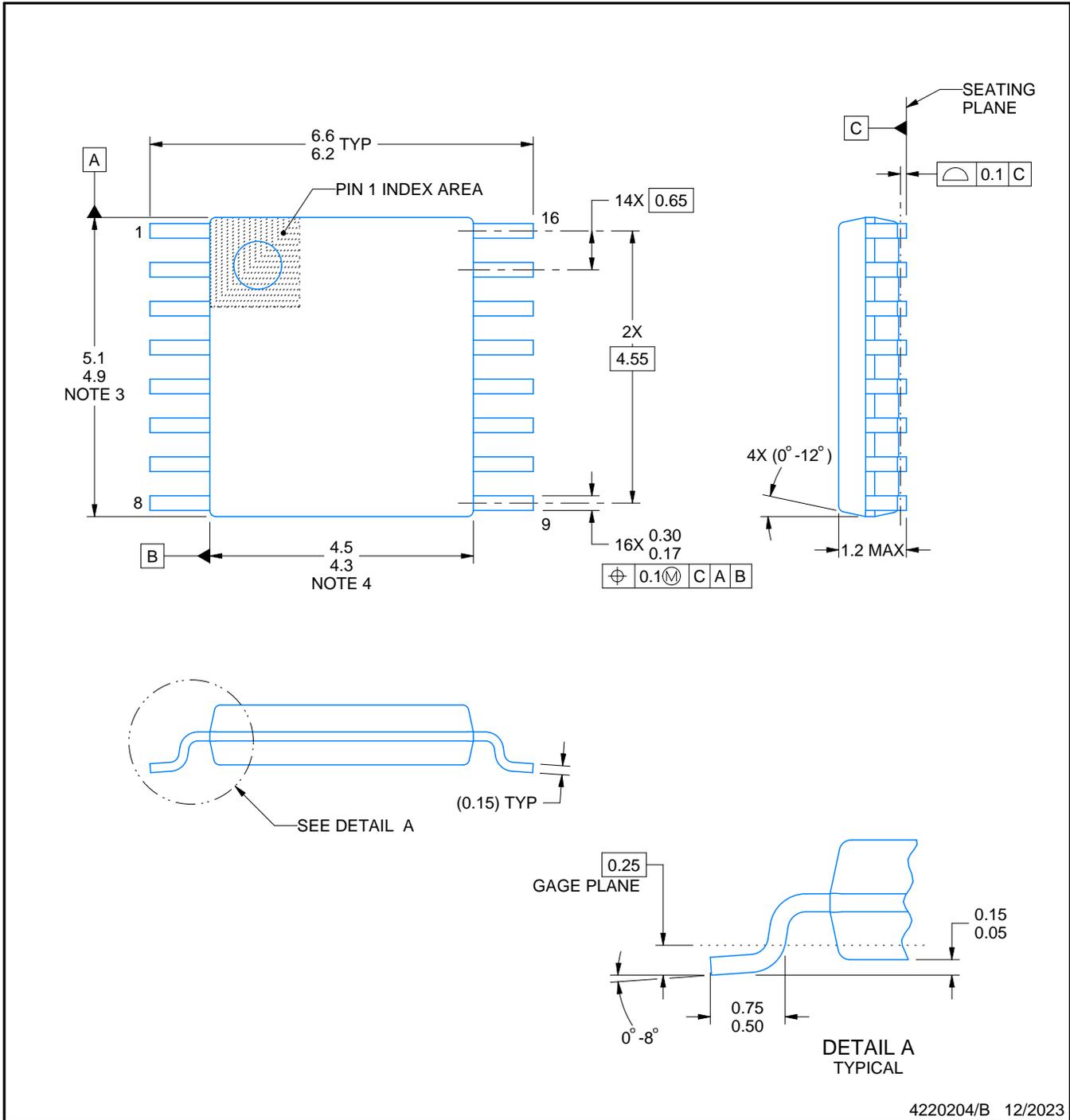


DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.



4220204/B 12/2023

NOTES:

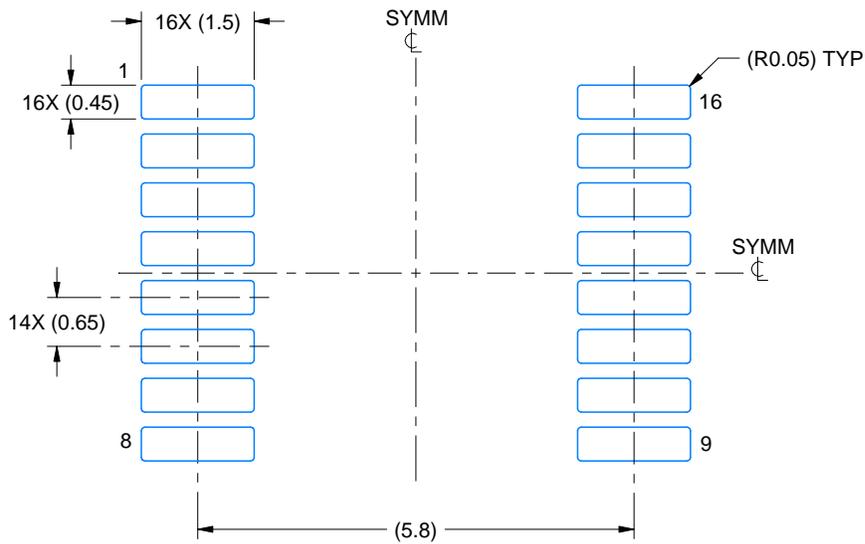
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

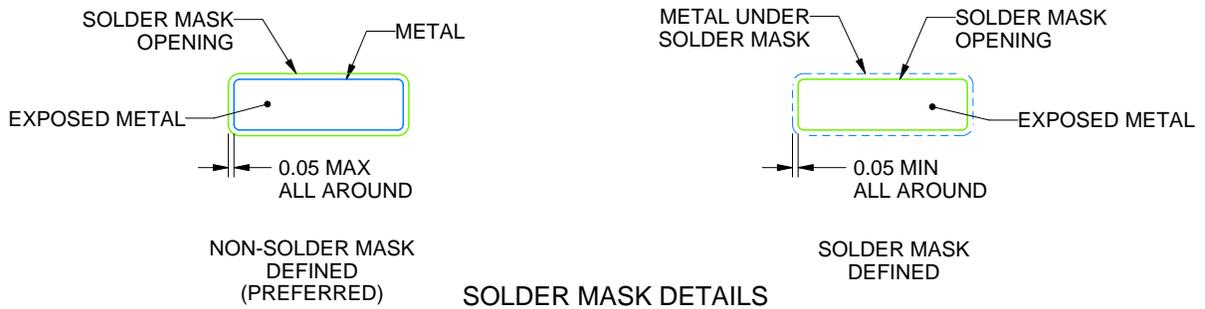
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220204/B 12/2023

NOTES: (continued)

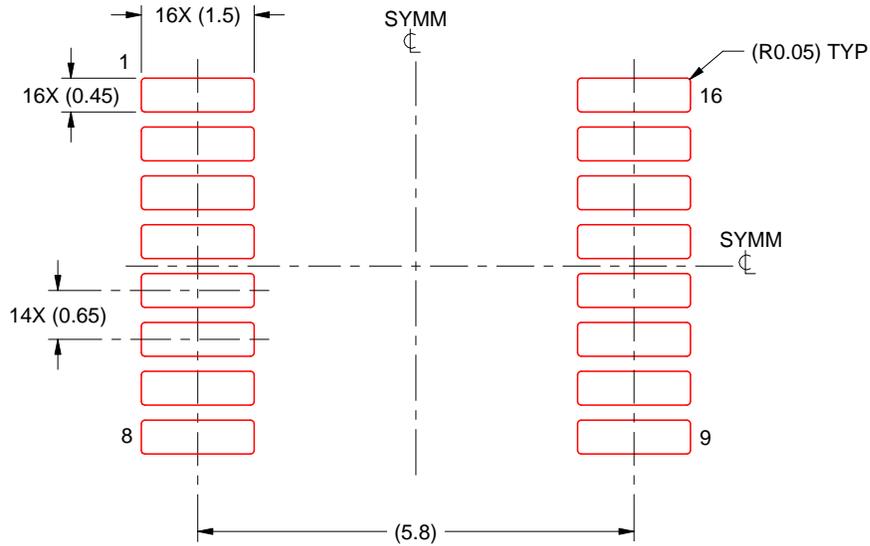
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

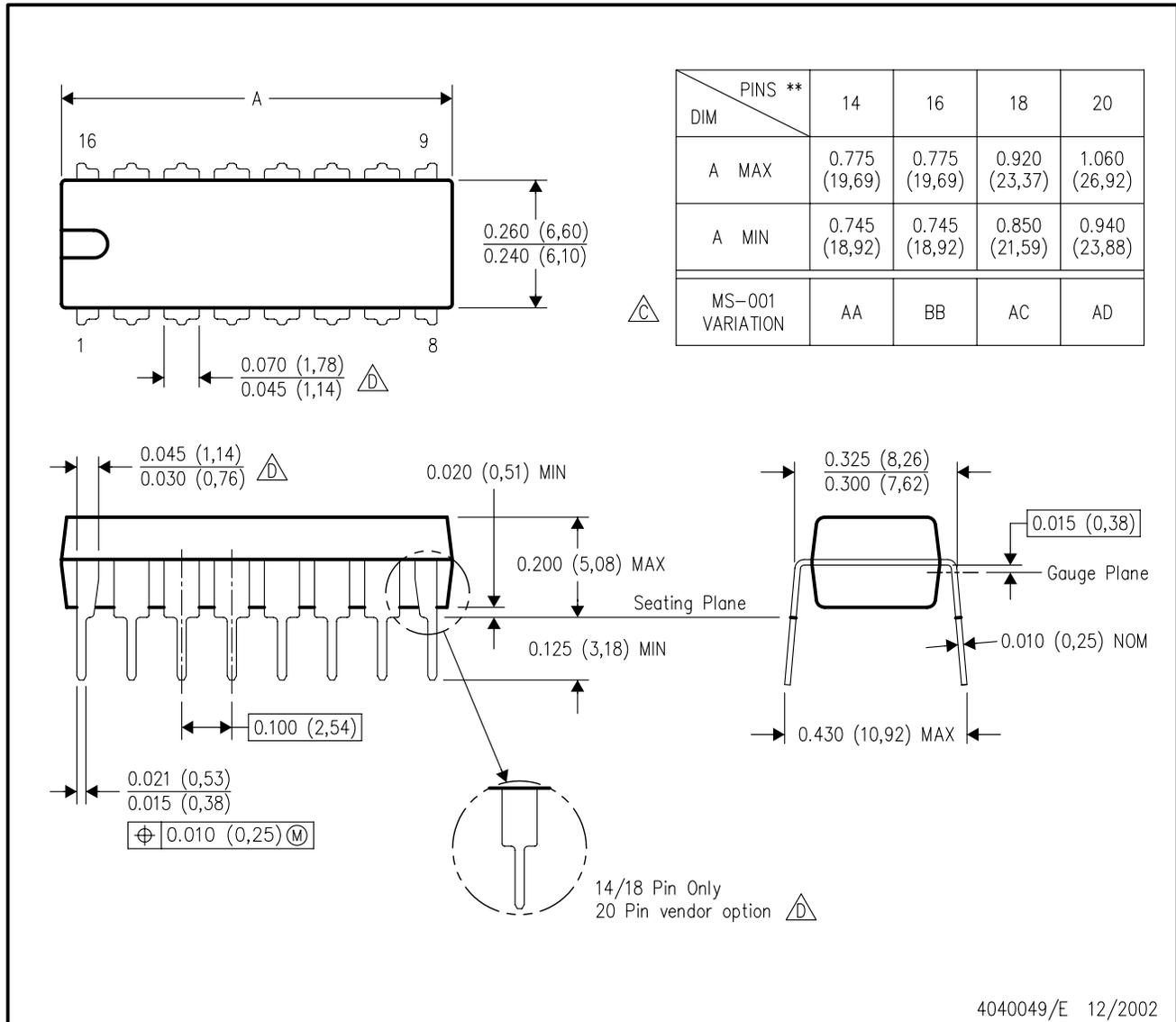
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

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最終更新日 : 2025 年 10 月