

# CDx4HC243、CDx4HCT243 3 ステート出力の高速 CMOS ロジック・クワッド・バス・トランシーバ

## 1 特長

- 7ns の伝搬遅延 (A から B / B から A、標準値、 $V_{CC} = 5V$ 、 $C_L = 15pF$ 、 $T_A = 25^\circ C$ )
- 3 ステート出力
- バッファ付き入力
- ファンアウト (全温度範囲にわたって)
  - 標準出力: 10 の LSTTL 負荷
  - バス・ドライバ出力: 15 の LSTTL 負荷
- 広い動作温度範囲:  $-55^\circ C \sim 125^\circ C$
- 平衡な伝搬遅延と遷移時間
- LSTTL ロジック IC に比べて消費電力を大幅削減
- HC タイプ
  - 2V~6V で動作
  - 優れたノイズ耐性:  $N_{IL} = V_{CC}$  の 30%、 $N_{IH} = V_{CC}$  の 30% ( $V_{CC} = 5V$  の場合)
- HCT タイプ
  - 4.5V~5.5V で動作
  - LSTTL 入力ロジックと直接互換、 $V_{IL} = 0.8V$  (最大値)、 $V_{IH} = 2V$  (最小値)
  - CMOS 入力互換、 $V_{OL}$ 、 $V_{OH}$  で  $I_I \leq 1\mu A$

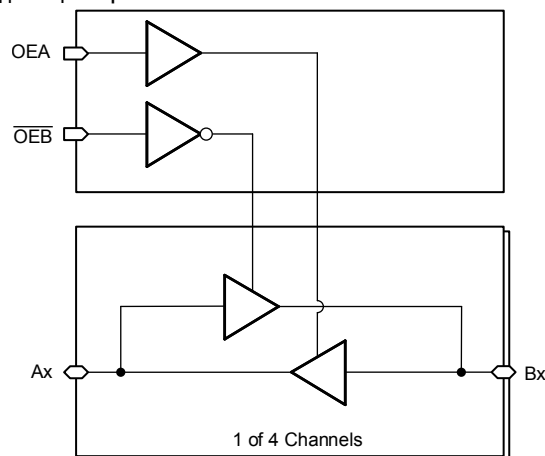
## 2 概要

CDx4HC243 および CDx4HCT243 は 3 ステート出力のクワッド・バス・トランシーバです。OEA と  $\overline{OEB}$  入力により、高インピーダンス状態と、デバイスを介した通信方向の両方を制御します。

### 製品情報

部品番号	パッケージ <sup>(1)</sup>	本体サイズ (公称)
CD54HC243F	CDIP (14)	19.55mm × 6.71mm
CD74HC243E	PDIP (14)	19.31mm × 6.35mm
CD74HC243M	SOIC (14)	8.65mm × 3.90mm
CD74HCT243E	PDIP (14)	19.31mm × 6.35mm
CD74HCT243M	SOIC (14)	8.65mm × 3.90mm

- (1) すべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



機能ブロック図



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### 3 Revision History

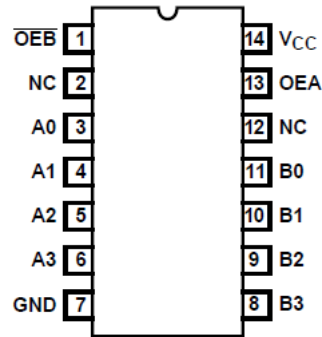
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

#### Changes from Revision D (October 2003) to Revision E (March 2022)

Page

- 最新のデータシート規格を反映するように、文書全体にわたって表、図、相互参照の採番方法を更新..... 1

## 4 Pin Configuration and Functions



**J, N, or D Package  
14-Pin CDIP, PDIP, or SOIC  
Top View**

## 5 Specifications

### 5.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	-0.5	7	V
I <sub>IK</sub>	Input diode current	For V <sub>I</sub> < -0.5V or V <sub>O</sub> > V <sub>CC</sub> + 0.5V		±20 mA
I <sub>OK</sub>	Output diode current	For V <sub>C</sub> < -0.5V or V <sub>O</sub> > V <sub>CC</sub> + 0.5V		±20 mA
I <sub>O</sub>	Drain Current, per output	For -0.5V < V <sub>O</sub> < V <sub>CC</sub> + 0.5V		±35 mA
I <sub>O</sub>	Output source or sink current per output pin	For V <sub>O</sub> > -0.5V or V <sub>O</sub> < V <sub>CC</sub> + 0.5V		±25 mA
	Continuous current through V <sub>CC</sub> or GND		±70	mA
T <sub>stg</sub>	Storage temperature range	-65	150	°C
T <sub>J</sub>	Junction temperature		150	°C
	Lead temperature (Soldering 10s)(SOIC - Lead Tips Only)		300	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 5.2 Recommended Operating Conditions

		MIN	MAX	UNIT	
V <sub>CC</sub>	Supply voltage range	HC Types	2	6	V
		HCT Types	4.5	5.5	
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	V	
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V	
t <sub>t</sub>	Input rise and fall time	V <sub>CC</sub> = 2V		1000	ns
		V <sub>CC</sub> = 4.5V		500	
		V <sub>CC</sub> = 6V		400	
T <sub>A</sub>	Temperature Range	-55	125	°C	

### 5.3 Thermal Information

THERMAL METRIC		N (PDIP)	D (SOIC)	UNIT
		14 PINS	14 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance <sup>(1)</sup>	80	86	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 5.4 Electrical Characteristics

PARAMETER		TEST CONDITIONS <sup>(1)</sup>	V <sub>CC</sub> (V)	25°C			-40°C to 85°C		-55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>											
V <sub>IH</sub>	High-level input voltage		2	1.5		1.5		1.5		V	
			4.5	3.15		3.15		3.15			
			6	4.2		4.2		4.2			
V <sub>IL</sub>	Low-level input voltage		2		0.5		0.5		0.5	V	
			4.5		1.35		1.35		1.35		
			6		1.8		1.8		1.8		
V <sub>OH</sub>	High-level output voltage CMOS loads	I <sub>OH</sub> = -20μA	2	1.9		1.9		1.9		V	
		I <sub>OH</sub> = -20μA	4.5	4.4		4.4		4.4			
		I <sub>OH</sub> = -20μA	6	5.9		5.9		5.9			
	High-level output voltage TTL loads	I <sub>OH</sub> = -6mA	4.5	3.98		3.84		3.7			
		I <sub>OH</sub> = -7.8mA	6	5.48		5.34		5.2			
V <sub>OL</sub>	Low-level output voltage CMOS loads	I <sub>OL</sub> = 20μA	2		0.1		0.1		0.1	V	
		I <sub>OL</sub> = 20μA	4.5		0.1		0.1		0.1		
		I <sub>OL</sub> = 20μA	6		0.1		0.1		0.1		
	Low-level output voltage TTL	I <sub>OL</sub> = 6mA	4.5		0.26		0.33		0.4		
		I <sub>OL</sub> = 7.8mA	6		0.26		0.33		0.4		
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> or GND	6		±0.1		±1		±1	μA	
I <sub>CC</sub>	Supply Current	V <sub>CC</sub> or GND	6		8		80		160	μA	
I <sub>OZ</sub>	Three-state leakage current	V <sub>IL</sub> or V <sub>IH</sub>	6		±0.5		±0.5		±10	μA	
<b>HCT TYPES</b>											
V <sub>IH</sub>	High-level input voltage		4.5 to 5.5	2			2		2	V	
V <sub>IL</sub>	Low-level input voltage		4.5 to 5.5		0.8		0.8		0.8	V	
V <sub>OH</sub>	High-level output voltage CMOS loads	I <sub>OH</sub> = -20μA	4.5	4.4		4.4		4.4		V	
	High-level output voltage TTL loads	I <sub>OH</sub> = -6mA	4.5	3.98		3.84		3.7			
V <sub>OL</sub>	Low-level output voltage CMOS loads	I <sub>OL</sub> = 20μA	4.5		0.1		0.1		0.1	V	
	Low-level output voltage TTL loads	I <sub>OL</sub> = 6mA	4.5		0.26		0.33		0.4		
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> to GND	5.5		±0.1		±1		±1	μA	
I <sub>CC</sub>	Supply current	V <sub>CC</sub> or GND	5.5		8		80		160	μA	
ΔI <sub>CC</sub> <sup>(2)</sup> <sup>(3)</sup>	Additional supply current per input pin	One of An or Bn	4.5 to 5.5	100	396		495		539	μA	
		One of OEA or OEB	4.5 to 5.5	100	216		270		294		
I <sub>OZ</sub>	Three-state leakage current	V <sub>IL</sub> or V <sub>IH</sub>	5.5		±0.5		±5		±10	μA	

(1) V<sub>I</sub> = V<sub>IH</sub> or V<sub>IL</sub>, unless otherwise noted.

(2) For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4 V, V<sub>CC</sub> = 5.5 V) specification is 1.8 mA.

(3) Inputs held at V<sub>CC</sub> - 2.1.

## 5.5 Switching Characteristics

Input  $t_i = 6\text{ns}$ . Unless otherwise specified,  $C_L = 50\text{pF}$

PARAMETER		$V_{CC}$ (V)	25°C		-40°C to 85°C	-55°C to 125°C	UNIT	
			TYP	MAX	MAX	MAX		
<b>HC TYPES</b>								
$t_{pd}$	Propagation delay data to outputs	2		90	115	135	ns	
		4.5		7 <sup>(1)</sup>	18	23		27
		6		15	20	23		
$t_{PZL}, t_{PZH}$	Output high-Z, to high level to low level	2		150	190	225	ns	
		4.5		12 <sup>(1)</sup>	30	38		45
		6		26	33	38		
$t_{PHZ}, t_{PLZ}$	Output high level, output low level to high-Z	2		150	190	225	ns	
		4.5		12 <sup>(1)</sup>	30	38		45
		6		26	33	38		
$t_t$	Output transition times	2		60	75	90	ns	
		4.5		12	15	18		
		6		10	13	15		
$C_i$	Input capacitance			10	10	10	pF	
$C_O$	Three-state output capacitance			20	20	20	pF	
$C_{pd}$ <sup>(2) (3)</sup>	Power dissipation capacitance	5		80			pF	
<b>HCT TYPES</b>								
$t_{pd}$	Propagation delay data to outputs	4.5		9 <sup>(1)</sup>	22	28	33	ns
$t_{PZH}, t_{PLZ}$	Output high-Z to high level to low level	4.5		14 <sup>(1)</sup>	34	43	51	ns
$t_{PHZ}, t_{PLZ}$	Output high level, output low level to high-Z	4.5		14 <sup>(1)</sup>	35	44	53	ns
$t_t$	Output transition times	4.5		12	15	18	ns	
$C_i$	Input capacitance			10	10	10	pF	
$C_O$	Three-state output capacitance			20	20	20	pF	
$C_{pd}$ <sup>(2) (3)</sup>	Power dissipation capacitance	5		91			pF	

(1) Typical value tested at 5V,  $C_L = 15\text{pF}$ .

(2)  $C_{PD}$  is used to determine the dynamic power consumption, per channel.

(3)  $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$  where  $f_i$  = Input Frequency,  $f_O$  = Output Frequency,  $C_L$  = Output Load Capacitance,  $V_{CC}$  = Supply Voltage.

## 6 Parameter Measurement Information

$t_{PD}$  is the maximum between  $t_{PLH}$  and  $t_{PHL}$

$t_t$  is the maximum between  $t_{TLH}$  and  $t_{THL}$

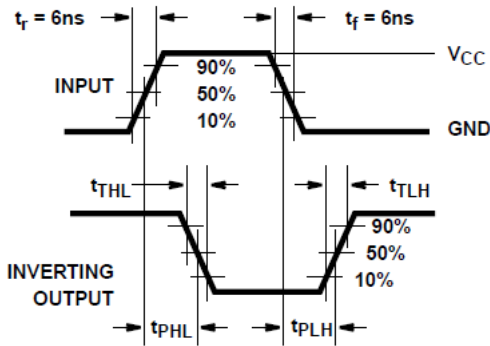


Figure 6-1. HC and HCT transition times and propagation delay times, combination logic

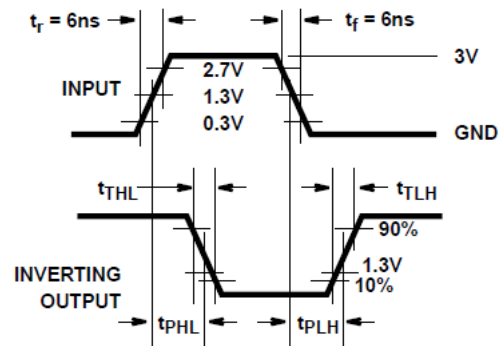


Figure 6-2. HCT transition times and propagation delay times, combination logic

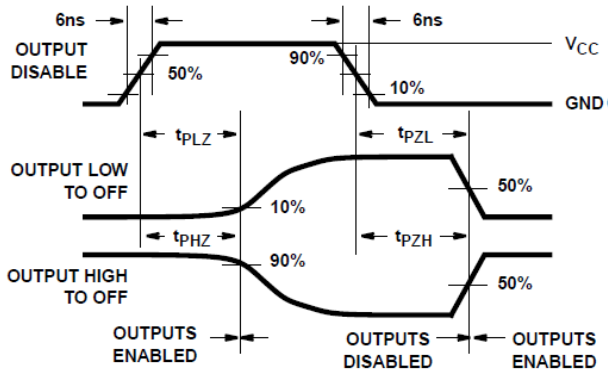


Figure 6-3. HC three-state propagation delay waveform

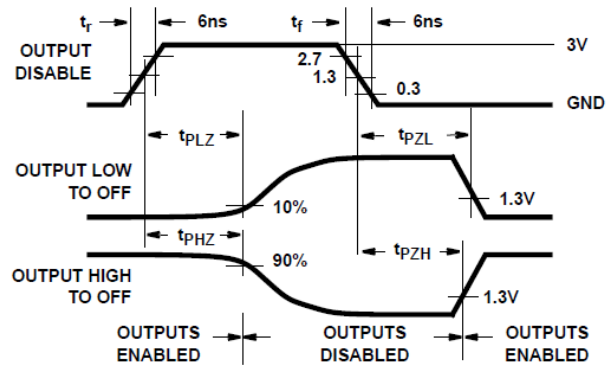
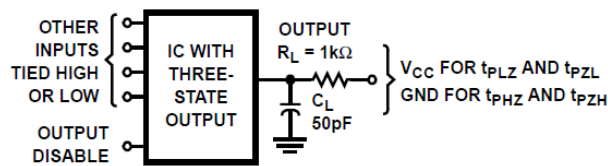


Figure 6-4. HCT three-state propagation delay waveform



NOTE: Open drain waveforms  $t_{PLZ}$  and  $t_{PZL}$  are the same as those for three-state shown on the left. The test circuit is Output  $R_L = 1k\Omega$  to  $V_{CC}$ ,  $C_L = 50pF$ .

Figure 6-5. HC and HCT three-state propagation delay test circuit

## 7 Detailed Description

### 7.1 Overview

The CDx4HC243 and CDx4HCT243 silicon-gate CMOS three-state bidirectional noninverting buffers are intended for two-way asynchronous communication between data buses. They have high-drive-current outputs that enable high-speed operation when driving large bus capacitances. These circuits possess the low power dissipation of CMOS circuits and have speeds comparable to low-power Schottky TTL circuits. They can drive 15 LSTTL loads.

The states of the output-enable ( $\overline{\text{OEB}}$ , OEA) inputs determine both the direction of flow (A to B, B to A), and the three-state mode.

### 7.2 Functional Block Diagram

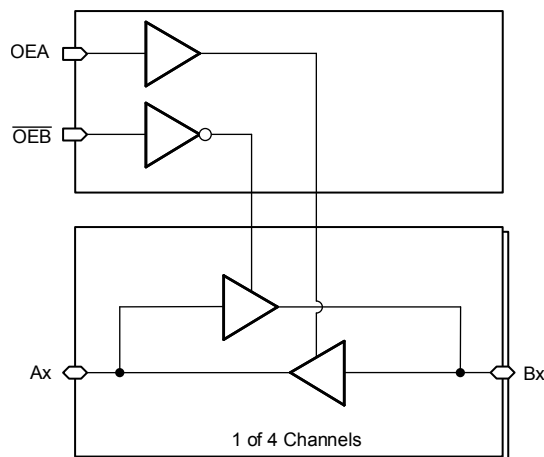


图 7-1. Functional Diagram

### 7.3 Device Functional Modes

表 7-1. Truth Table<sup>(1)(2)</sup>

Control Inputs		HC, HCT243 Series	
		Data port status	
$\overline{\text{OEB}}$	OEA	An	Bn
H	H	O	I
L	H	Z	Z
H	L	Z	Z
L	L	I	O

- (1) H = High voltage level. L = Low voltage level. I = Input. O = Output (Same level as input). Z = High Impedance
- (2) To prevent excess currents in the High Z modes all I/O terminals should be terminated with 10kΩ to 1MΩ resistors.

## 8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- $\mu\text{F}$  capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- $\mu\text{F}$  and 1- $\mu\text{F}$  capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 9 Layout

### 9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

## 10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 10.1 Documentation Support

#### 10.1.1 Related Documentation

### 10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 10.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の [使用条件](#) を参照してください。

### 10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

### 10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 10.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">8409001CA</a>	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8409001CA CD54HC243F3A
<a href="#">CD54HC243F</a>	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC243F
CD54HC243F.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC243F
<a href="#">CD54HC243F3A</a>	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8409001CA CD54HC243F3A
CD54HC243F3A.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8409001CA CD54HC243F3A
<a href="#">CD74HC243E</a>	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC243E
CD74HC243E.A	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC243E
CD74HC243EE4	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC243E
<a href="#">CD74HC243M</a>	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	-55 to 125	HC243M
<a href="#">CD74HC243M96</a>	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-55 to 125	HC243M
CD74HC243M96.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC243M
<a href="#">CD74HC243M96G4</a>	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC243M
CD74HC243M96G4.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC243M
<a href="#">CD74HCT243E</a>	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT243E
CD74HCT243E.A	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT243E
<a href="#">CD74HCT243M</a>	Active	Production	SOIC (D)   14	50   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT243M
CD74HCT243M.A	Active	Production	SOIC (D)   14	50   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT243M

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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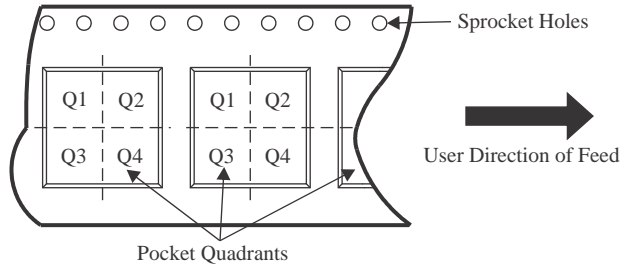
**OTHER QUALIFIED VERSIONS OF CD54HC243, CD74HC243 :**

- Catalog : [CD74HC243](#)
- Military : [CD54HC243](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


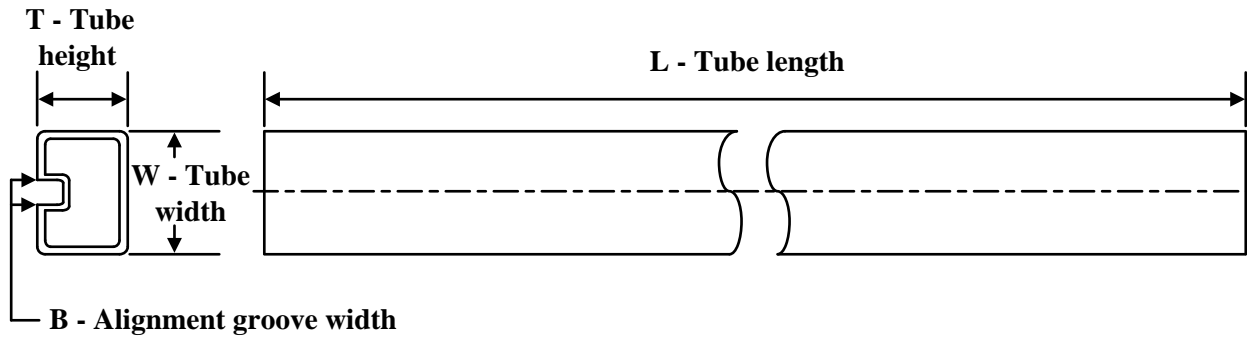
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC243M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74HC243M96	SOIC	D	14	2500	330.0	16.4	6.6	9.3	2.1	8.0	16.0	Q1
CD74HC243M96G4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

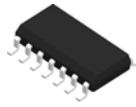

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC243M96	SOIC	D	14	2500	353.0	353.0	32.0
CD74HC243M96	SOIC	D	14	2500	366.0	364.0	50.0
CD74HC243M96G4	SOIC	D	14	2500	353.0	353.0	32.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD74HC243E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC243E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC243E.A	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC243E.A	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC243EE4	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC243EE4	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT243E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT243E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT243E.A	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT243E.A	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT243M	D	SOIC	14	50	506.6	8	3940	4.32
CD74HCT243M.A	D	SOIC	14	50	506.6	8	3940	4.32



# D0014A

# PACKAGE OUTLINE

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

J 14

**GENERIC PACKAGE VIEW**  
**CDIP - 5.08 mm max height**  
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

J0014A



# PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

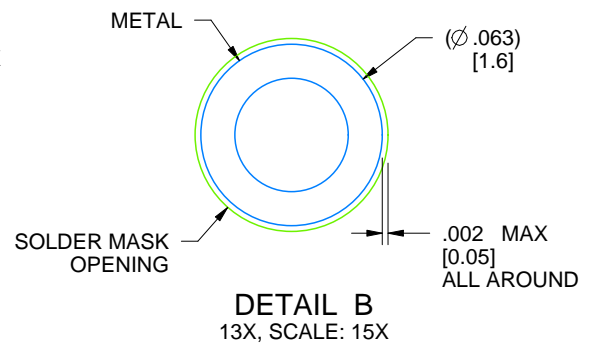
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - (C) Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.

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最終更新日 : 2025 年 10 月