# CDx4HC151、CDx4HCT151 ハイスピード CMOS ロジック、8 入力マルチプレクサ

## 1 特長

- 相補データ出力
- バッファ付き入力および出力
- ファンアウト (全温度範囲にわたって)
  - 標準出力:10 の LSTTL 負荷
  - バス・ドライバ出力:15 の LSTTL 負荷
- 広い動作電圧範囲:-55℃～125℃
- 平衡な伝搬遅延と遷移時間
- LSTTL ロジック IC に比べて消費電力を大幅削減
- Philips 社 / Signetics 社製品を代替
- HC タイプ
  - 2V～6V で動作
  - 優れたノイズ耐性:$N_{IL}$ = $V_{CC}$ の 30%、$N_{IH}$ = $V_{CC}$ の 30% ($V_{CC}$ = 5V の場合)
- HCT タイプ
  - 4.5V～5.5V で動作
  - LSTTL 入力ロジックと直接互換、$V_{IL}$ = 0.8V (最大値)、$V_{IH}$ = 2V (最小値)
  - CMOS 入力互換、$V_{OL}$、$V_{OH}$ で $I_I \leq 1\mu A$

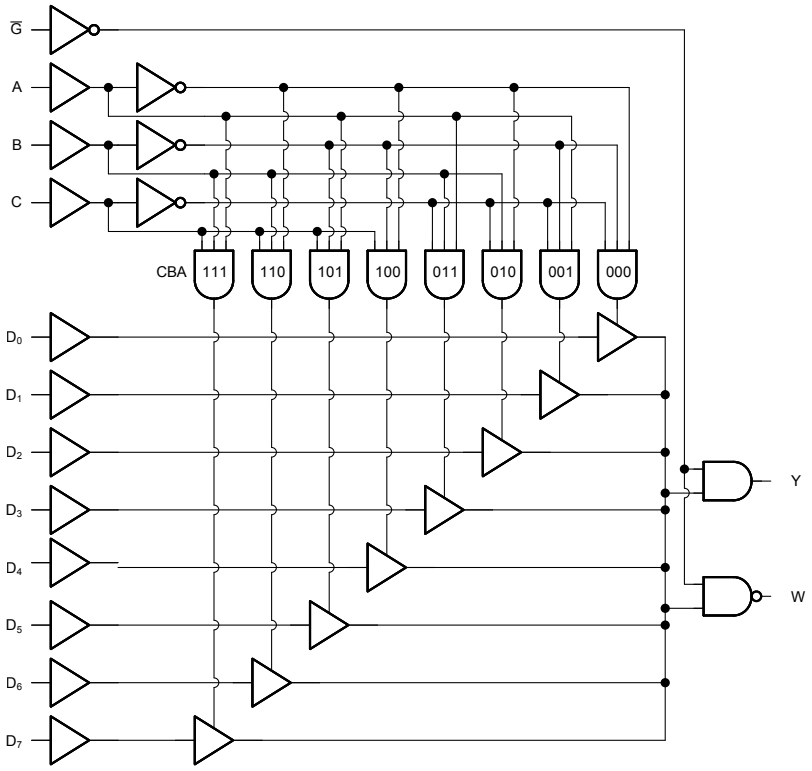
## 2 概要

'HC151 と 'HCT151 は、3 つのバイナリ制御入力 (A、B、C) と 1 つのアクティブ LOW イネーブル ($\overline{G}$) 入力を備えたシングル 8 チャネル・デジタル・マルチプレクサです。3 つのバイナリ信号を使って 8 つのチャネルのうちの 1 つを選択します。出力には、反転 (W) と非反転 (Y) の両方があります。

**製品情報**

| 部品番号 | パッケージ(1) | 本体サイズ (公称) |
|---|---|---|
| CD74HC151M | SOIC (16) | 9.90mm × 3.90mm |
| CD74HC151E | PDIP (16) | 19.31mm × 6.35mm |
| CD54HC151F3A | CDIP (16) | 24.38mm × 6.92mm |

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。




機能ダイアグラム

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# Table of Contents



## 3 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| Changes from Revision C (October 2003) to Revision D (November 2021) | Page |
|---|---|
| • 最新のデータシート規格を反映するように、文書全体の表、図、相互参照の採番と書式設定を更新 | 1 |
| • 現行の TI の命名規則に合わせてピン名を以下のように更新。$I_3$ を $D_3$、$I_2$ を $D_2$、$I_1$ を $D_1$、$I_0$ を $D_0$、$\overline{Y}$ を W、$\overline{E}$ を $\overline{G}$、S2 を C、S1 を B、S0 を A、$I_7$ を $D_7$、$I_6$ を $D_6$、$I_5$ を $D_5$、$I_4$ を $D_4$。 | 1 |


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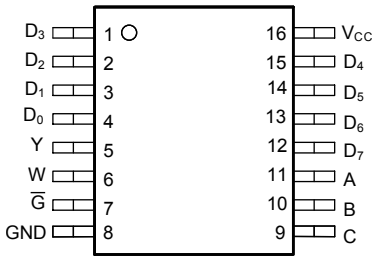
## 4 Pin Configuration and Functions




**J, N, or D package**
**16-Pin CDIP, PDIP, SOIC**
**Top View**

# 5 Specifications

## 5.1 Absolute Maximum Ratings[1]

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | -0.5 | 7 | V |
| $I_{IK}$ | Input diode current | ($V_I$ < -0.5 V or $V_I$ > $V_{CC}$ + 0.5 V) | | ±20 | mA |
| $I_{OK}$ | Output diode current | ($V_O$ < -0.5 V or $V_O$ > $V_{CC}$ + 0.5 V) | | ±20 | mA |
| $I_O$ | Continuous output current | ($V_O$ > -0.5 V or $V_O$ < $V_{CC}$ + 0.5 V) | | ±25 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±50 | mA |
| $T_J$ | Junction temperature | | | 150 | °C |
| $T_{stg}$ | Storage temperature | | -65 | 150 | °C |
| | Lead Temperature (Soldering 10s) | | | 300 | °C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 5.2 Recommended Operating Conditions

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $T_A$ | Temperature Range | | –55 | 125 | ℃ |
| $V_{CC}$ | Supply Voltage Range | HC Types | 2 | 6 | V |
| | | HCT Types | 4.5 | 5.5 | |
| $V_I$,$V_O$ | DC Input or Output Voltage | | 0 | $V_{CC}$ | V |
| $t_t$ | Input Rise and Fall Time | 2 V | | 1000 | ns |
| | | 4.5 V | | 500 | |
| | | 6 V | | 400 | |

## 5.3 Thermal Information

| THERMAL METRIC | | CD74HC151, CD74HCT151 | | UNIT |
|---|---|---|---|---|
| | | D (SOIC) | N (PDIP) | |
| | | 16 PINS | 16 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance[1] | 73 | 67 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.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## 5.4 Electrical Characteristics

| PARAMETER | | TEST CONDITIONS[1] | $V_{CC}$ (V) | 25℃ | | | -40℃ to 85℃ | | -55℃ to 125℃ | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| **HC TYPES** | | | | | | | | | | | |
| $V_{IH}$ | High level input voltage | | 2 | 1.5 | | | 1.5 | | 1.5 | | V |
| | | | 4.5 | 3.15 | | | 3.15 | | 3.15 | | |
| | | | 6 | 4.2 | | | 4.2 | | 4.2 | | |
| $V_{IL}$ | Low level input voltage | | 2 | | | 0.5 | | 0.5 | | 0.5 | V |
| | | | 4.5 | | | 1.35 | | 1.35 | | 1.35 | |
| | | | 6 | | | 1.8 | | 1.8 | | 1.8 | |
| $V_{OH}$ | High level output voltage | $I_{OH}$ = – 20 μA | 2 | 1.9 | | | 1.9 | | 1.9 | | V |
| | | $I_{OH}$ = – 20 μA | 4.5 | 4.4 | | | 4.4 | | 4.4 | | |
| | | $I_{OH}$ = – 20 μA | 6 | 5.9 | | | 5.9 | | 5.9 | | |
| | High level output voltage | $I_{OH}$ = – 4 mA | 4.5 | 3.98 | | | 3.84 | | 3.7 | | |
| | | $I_{OH}$ = – 5.2 mA | 6 | 5.48 | | | 5.34 | | 5.2 | | |
| $V_{OL}$ | Low level output voltage | $I_{OL}$ = 20 μA | 2 | | | 0.1 | | 0.1 | | 0.1 | V |
| | | $I_{OL}$ = 20 μA | 4.5 | | | 0.1 | | 0.1 | | 0.1 | |
| | | $I_{OL}$ = 20 μA | 6 | | | 0.1 | | 0.1 | | 0.1 | |
| | Low level output voltage | $I_{OL}$ = 4 mA | 4.5 | | | 0.26 | | 0.33 | | 0.4 | |
| | | $I_{OL}$ = 5.2 mA | 6 | | | 0.26 | | 0.33 | | 0.4 | |
| $I_I$ | Input leakage current | $V_I$ = $V_{CC}$ or GND | 6 | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | Supply current | $V_I$ = $V_{CC}$ or GND | 6 | | | 8 | | 80 | | 160 | μA |
| **HCT TYPES** | | | | | | | | | | | |
| $V_{IH}$ | High level input voltage | | 4.5 to 5.5 | 2 | | | 2 | | 2 | | V |
| $V_{IL}$ | Low level input voltage | | 4.5 to 5.5 | | | 0.8 | | 0.8 | | 0.8 | V |
| $V_{OH}$ | High level output voltage | $I_{OH}$ = – 20 μA | 4.5 | 4.4 | | | 4.4 | | 4.4 | | V |
| | High level output voltage | $I_{OH}$ = – 4 mA | 4.5 | 3.98 | | | 3.84 | | 3.7 | | |
| $V_{OL}$ | Low level output voltage | $I_{OL}$ = 20 mA | 4.5 | | | 0.1 | | 0.1 | | 0.1 | V |
| | Low level output voltage | $I_{OL}$ = 4 mA | 4.5 | | | 0.26 | | 0.33 | | 0.4 | |
| $I_I$ | Input leakage current | $V_I$ = $V_{CC}$ or GND | 5.5 | | | ± 0.1 | | ±1 | | ± 1 | μA |
| $I_{CC}$ | Supply current | $V_I$ = $V_{CC}$ or GND | 5.5 | | | 8 | | 80 | | 160 | μA |
| $\Delta I_{CC}$ [2] | Additional supply current per input pin | Select inputs held at $V_{CC}$ – 2.1 | 4.5 to 5.5 | | 100 | 540 | | 675 | | 735 | μA |
| | | Data inputs held at $V_{CC}$ – 2.1 | 4.5 to 5.5 | | 100 | 162 | | 202.5 | | 220.5 | |
| | | Enable inputs held at $V_{CC}$ – 2.1 | 4.5 to 5.5 | | 100 | 108 | | 135 | | 147 | |

(1) $V_I$ = $V_{IH}$ or $V_{IL}$, unless otherwise noted.
(2) For dual-supply systems theoretical worst case ($V_I$ = 2.4 V, $V_{CC}$ = 5.5 V) specification is 1.8 mA.

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## 5.5 Switching Characteristics

Input $t_t$ = 6ns. Unless otherwise specified, $C_L$ = 50pF. (See Parameter Measurement Information)

| PARAMETER | | $V_{CC}$ (V) | 25℃ | | | -40℃ to 85℃ | | -55℃ to 125℃ | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| **HC TYPES** | | | | | | | | | | |
| $t_{pd}$ | Any Data Input to Y | 2 | | | 170 | | 215 | | 255 | ns |
| | | 4.5 | | 14(3) | 34 | | 43 | | 51 | |
| | | 6 | | | 29 | | 37 | | 43 | |
| | Any Data Input to W | 2 | | | 185 | | 230 | | 280 | ns |
| | | 4.5 | | 15(3) | 37 | | 46 | | 56 | |
| | | 6 | | | 31 | | 39 | | 48 | |
| | Any Select to Y | 2 | | | 185 | | 230 | | 280 | ns |
| | | 4.5 | | 15(3) | 37 | | 46 | | 56 | |
| | | 6 | | | 31 | | 39 | | 48 | |
| | Any Select to W | 2 | | | 205 | | 255 | | 310 | ns |
| | | 4.5 | | 17(3) | 41 | | 51 | | 62 | |
| | | 6 | | | 35 | | 43 | | 53 | |
| | Enable to Y | 2 | | | 140 | | 175 | | 210 | ns |
| | | 4.5 | | 11(3) | 28 | | 35 | | 42 | |
| | | 6 | | | 24 | | 30 | | 36 | |
| | Enable to W | 2 | | | 145 | | 180 | | 220 | ns |
| | | 4.5 | | 12(3) | 29 | | 36 | | 44 | |
| | | 6 | | | 25 | | 31 | | 38 | |
| $t_t$ | Output Transition Time | 2 | | | 75 | | 95 | | 110 | ns |
| | | 4.5 | | | 15 | | 19 | | 22 | |
| | | 6 | | | 13 | | 16 | | 19 | |
| $C_{IN}$ | Input Capacitance | | | | 10 | | 10 | | 10 | pF |
| $C_{PD}$ | Power Dissipation Capacitance(1) (2) | 5 | | 59 | | | | | | pF |
| **HCT TYPES** | | | | | | | | | | |
| $t_{pd}$ | Any Data Input to Y | 4.5 | | 16(3) | 38 | | 48 | | 57 | ns |
| | Any Data Input to W | 4.5 | | 15(3) | 36 | | 45 | | 54 | ns |
| | Any Select to Y | 4.5 | | 17 (3) | 41 | | 51 | | 62 | ns |
| | Any Select to W | 4.5 | | 18(3) | 43 | | 54 | | 65 | ns |
| | Enable to Y | 4.5 | | 12(3) | 29 | | 36 | | 44 | ns |
| $C_L$ = 50 pF | Enable to W | 4.5 | 15(3) | | 36 | | 46 | | 54 | ns |
| $t_t$ | Output Transition Time | 4.5 | | | 15 | | 19 | | 22 | ns |
| $C_{IN}$ | Input Capacitance | | | | 10 | | 10 | | 10 | pF |
| $C_{PD}$ | Power Dissipation Capacitance(1) (2) | 5 | | 58 | | | | | | pF |

(1) $C_{PD}$ is used to determine the dynamic power consumption, per gate.
(2) $P_D = V_{CC}{}^2 f_i (C_{PD} + C_L)$ where $f_i$ = input frequency, $C_L$ = output load capacitance, $V_{CC}$ = supply voltage.
(3) $C_L$ = 15 pF and $V_{CC}$ = 5 V


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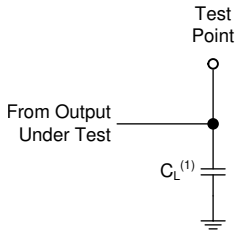
## 6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_t$ < 6 ns.

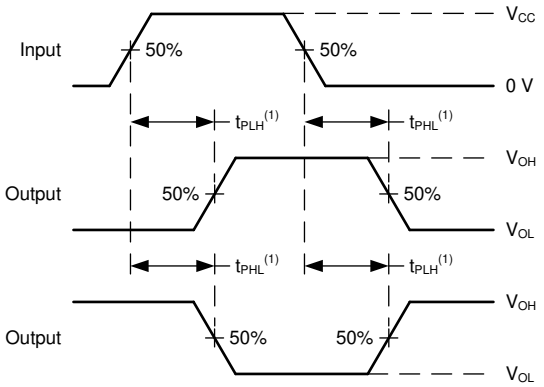
For clock inputs, $f_{max}$ is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



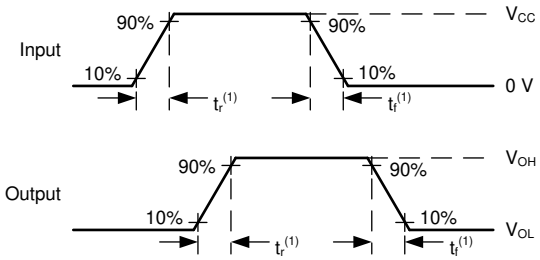

(1) $C_L$ includes probe and test-fixture capacitance.

**図 6-1. Load Circuit for Push-Pull Outputs**



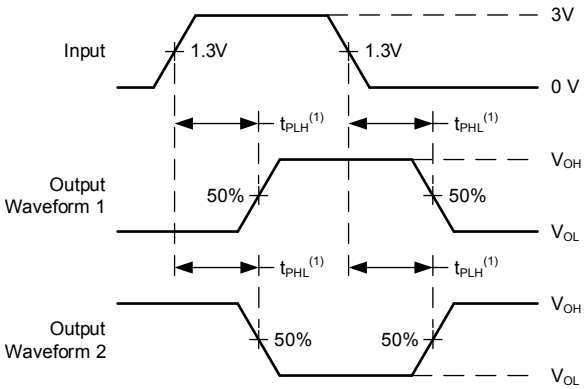

(1) The greater between $t_{PLH}$ and $t_{PHL}$ is the same as $t_{pd}$.

**図 6-2. Voltage Waveforms, Propagation Delays for Standard CMOS Inputs**




(1) The greater between $t_r$ and $t_f$ is the same as $t_t$.

**図 6-3. Voltage Waveforms, Input and Output Transition Times for Standard CMOS Inputs**




(1) The greater between $t_{PLH}$ and $t_{PHL}$ is the same as $t_{pd}$.

**図 6-4. Voltage Waveforms, Propagation Delays for TTL-Compatible Inputs**

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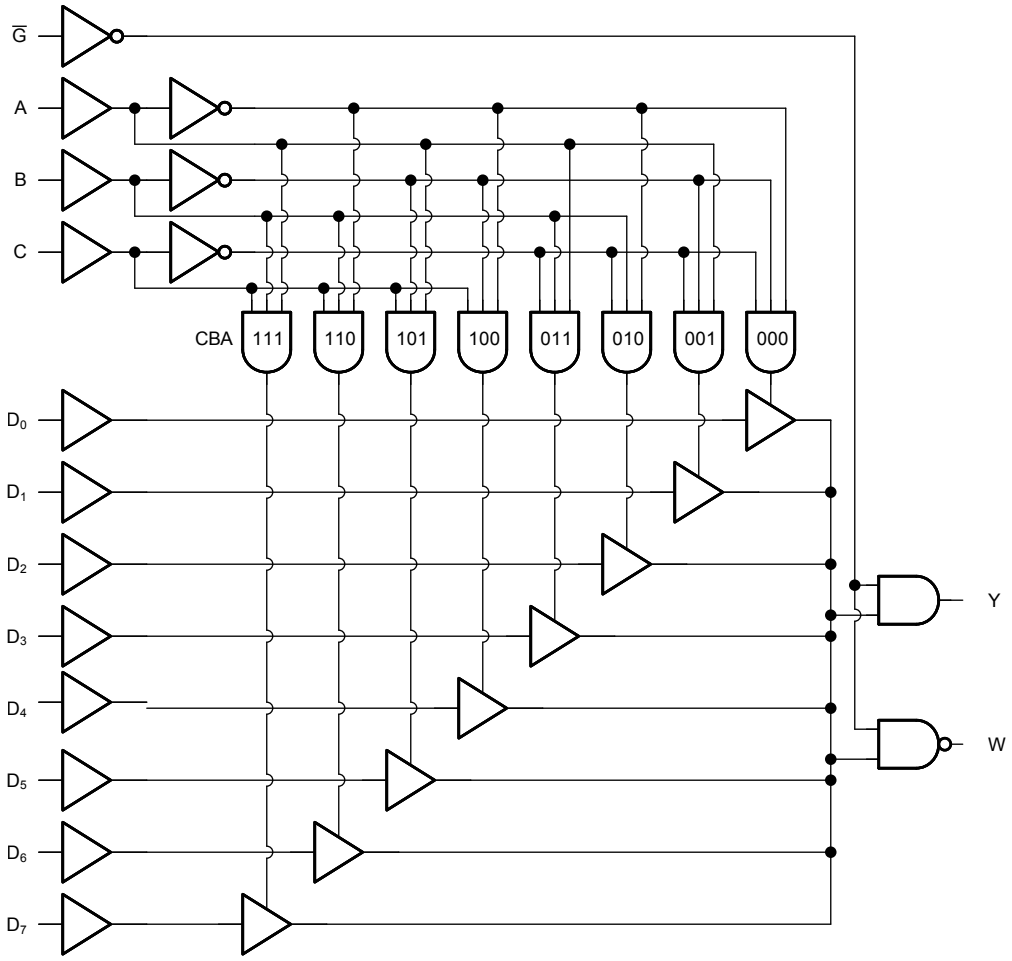
# 7 Detailed Description

## 7.1 Overview

The ’HC151 and ’HCT151 are single 8-channel digital multiplexers having three binary control inputs, A, B and C and an active low enable ($\overline{G}$) input. The three binary signals select 1 of 8 channels. Outputs are both inverting (W) and non-inverting (Y).

## 7.2 Functional Block Diagram





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## 7.3 Device Functional Modes

| SELECT INPUTS(1) | | | DATA INPUTS | | | | | | | | ENABLE | OUTPUT | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C | B | A | $D_0$ | $D_1$ | $D_2$ | $D_3$ | $D_4$ | $D_5$ | $D_6$ | $D_7$ | $\overline{G}$ | W | Y |
| X | X | X | X | X | X | X | X | X | X | X | H | H | L |
| L | L | L | L | X | X | X | X | X | X | X | L | H | L |
| L | L | L | H | X | X | X | X | X | X | X | L | L | H |
| L | L | H | X | L | X | X | X | X | X | X | L | H | L |
| L | L | H | X | H | X | X | X | X | X | X | L | L | H |
| L | H | L | X | X | L | X | X | X | X | X | L | H | L |
| L | H | L | X | X | H | X | X | X | X | X | L | L | H |
| L | H | H | X | X | X | L | X | X | X | X | L | H | L |
| L | H | H | X | X | X | H | X | X | X | X | L | L | H |
| H | L | L | X | X | X | X | L | X | X | X | L | H | L |
| H | L | L | X | X | X | X | H | X | X | X | L | L | H |
| H | L | H | X | X | X | X | X | L | X | X | L | H | L |
| H | L | H | X | X | X | X | X | H | X | X | L | L | H |
| H | H | L | X | X | X | X | X | X | L | X | L | H | L |
| H | H | L | X | X | X | X | X | X | H | X | L | L | H |
| H | H | H | X | X | X | X | X | X | X | L | L | H | L |
| H | H | H | X | X | X | X | X | X | X | H | L | L | H |

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care

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# 8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each $V_{CC}$ terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

# 9 Layout

## 9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or $V_{CC}$, whichever makes more sense for the logic function or is more convenient.


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# 10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

## 10.1 Documentation Support

### 10.1.1 Related Documentation

## 10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 10.3 サポート・リソース

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## 10.4 Trademarks

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## 10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 10.6 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| 5962-9065201MEA | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9065201MEA CD54HCT151F3A |
| CD54HC151F3A | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8412801EA CD54HC151F3A |
| CD54HC151F3A.A | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8412801EA CD54HC151F3A |
| CD54HCT151F3A | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9065201MEA CD54HCT151F3A |
| CD54HCT151F3A.A | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9065201MEA CD54HCT151F3A |
| CD74HC151E | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD74HC151E |
| CD74HC151E.A | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD74HC151E |
| CD74HC151EE4 | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD74HC151E |
| CD74HC151M | Obsolete | Production | SOIC (D) \| 16 | - | - | Call TI | Call TI | -55 to 125 | HC151M |
| CD74HC151M96 | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -55 to 125 | HC151M |
| CD74HC151M96.A | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC151M |
| CD74HC151M96G4 | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC151M |
| CD74HC151M96G4.A | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC151M |
| CD74HC151MT | Obsolete | Production | SOIC (D) \| 16 | - | - | Call TI | Call TI | -55 to 125 | HC151M |
| CD74HCT151E | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD74HCT151E |
| CD74HCT151E.A | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD74HCT151E |
| CD74HCT151M | Obsolete | Production | SOIC (D) \| 16 | - | - | Call TI | Call TI | -55 to 125 | HCT151M |
| CD74HCT151M96 | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCT151M |
| CD74HCT151M96.A | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCT151M |
| CD74HCT151M96G4 | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCT151M |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF CD54HC151, CD54HCT151, CD74HC151, CD74HCT151 :**

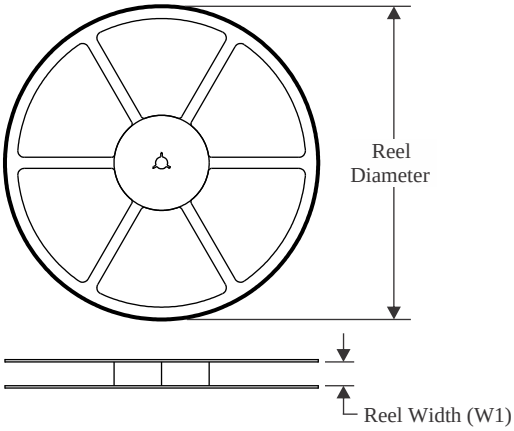
- Catalog : CD74HC151, CD74HCT151
- Military : CD54HC151, CD54HCT151

NOTE: Qualified Version Definitions:

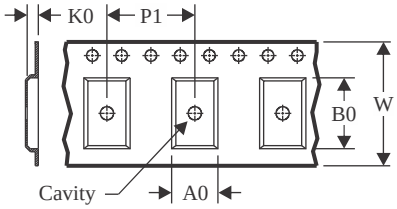
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

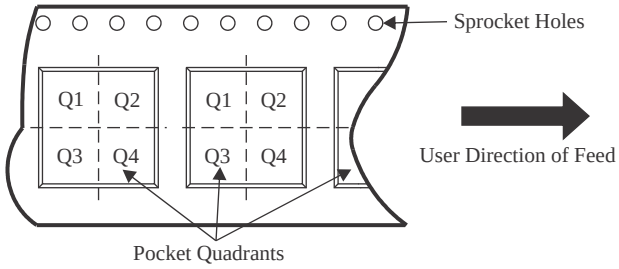



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

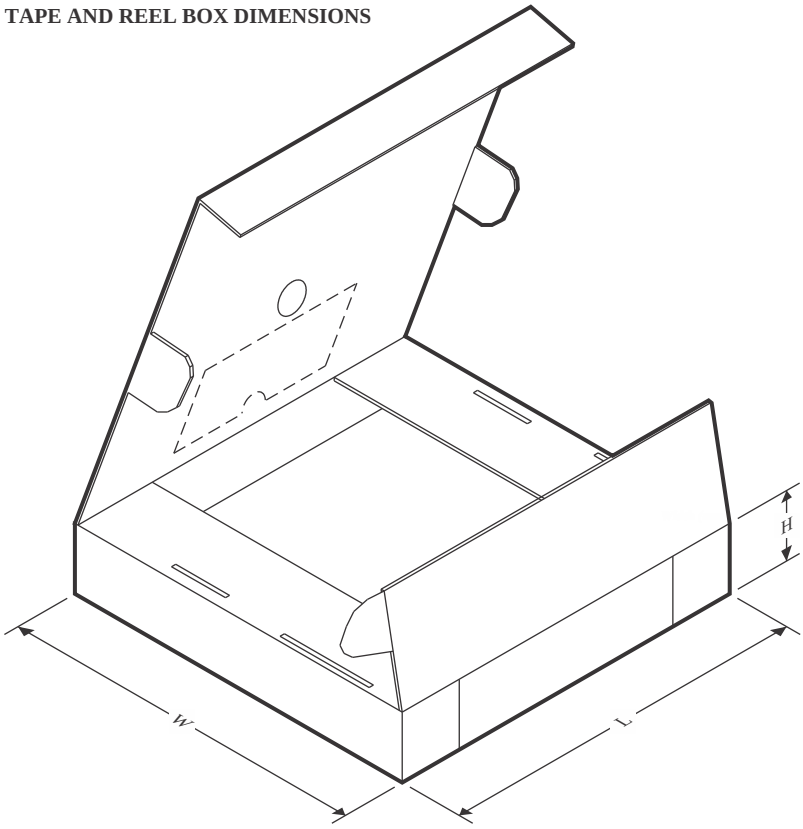
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CD74HC151M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD74HC151M96G4 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD74HCT151M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |

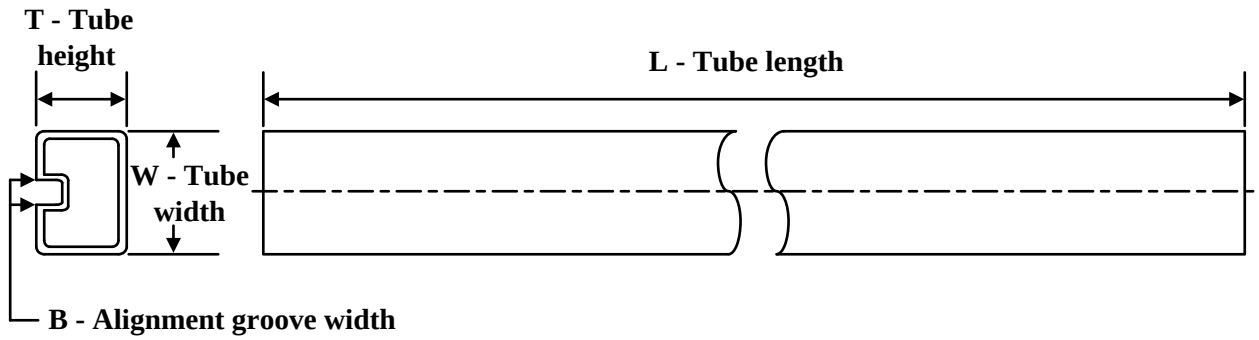
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CD74HC151M96 | SOIC | D | 16 | 2500 | 353.0 | 353.0 | 32.0 |
| CD74HC151M96G4 | SOIC | D | 16 | 2500 | 353.0 | 353.0 | 32.0 |
| CD74HCT151M96 | SOIC | D | 16 | 2500 | 353.0 | 353.0 | 32.0 |

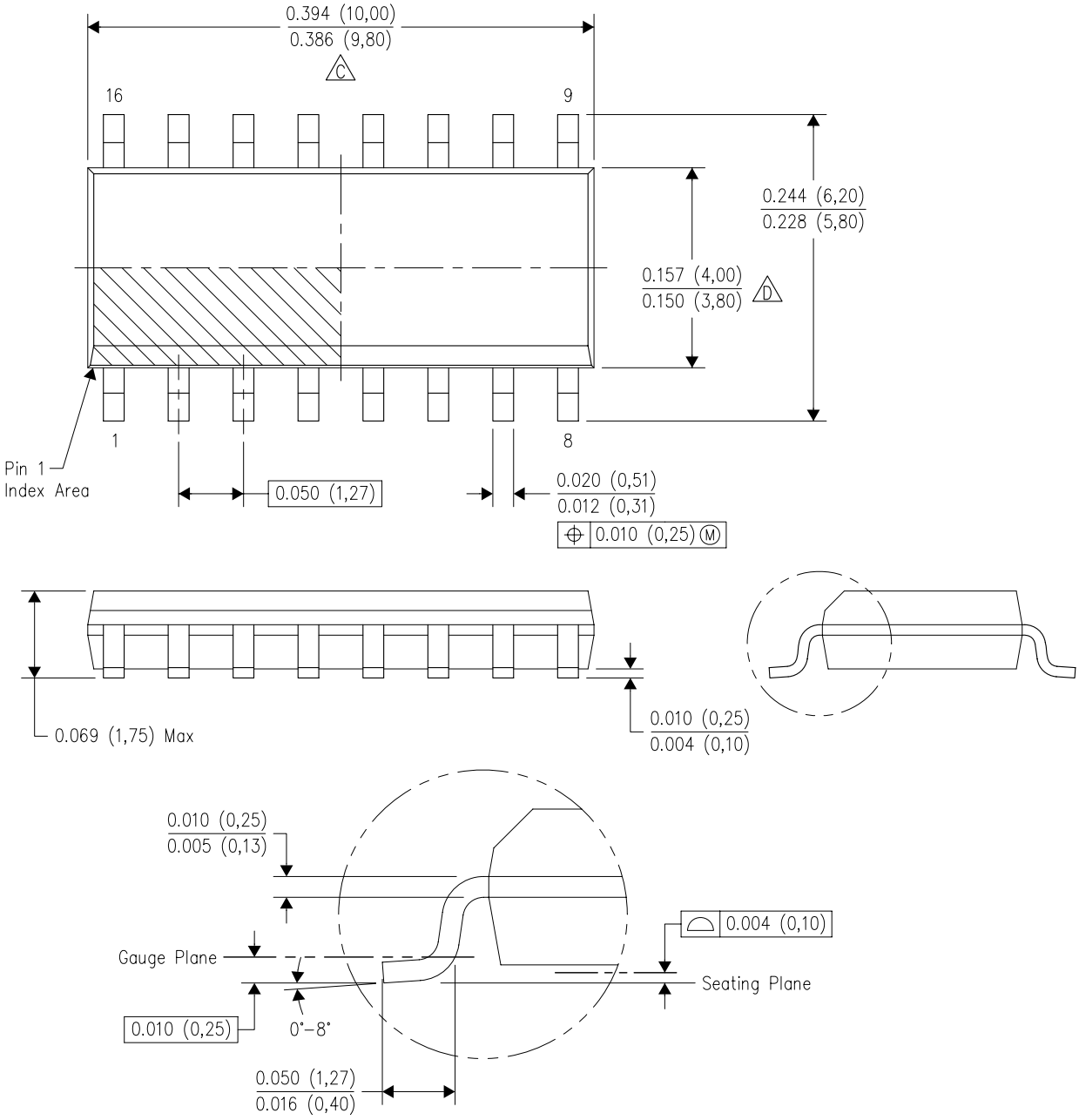
## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| CD74HC151E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HC151E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HC151E.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HC151E.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HC151EE4 | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HC151EE4 | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HCT151E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HCT151E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HCT151E.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HCT151E.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

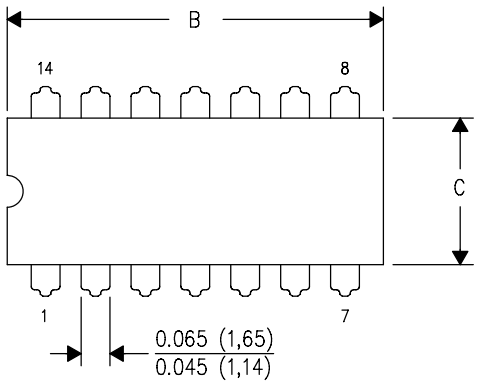



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

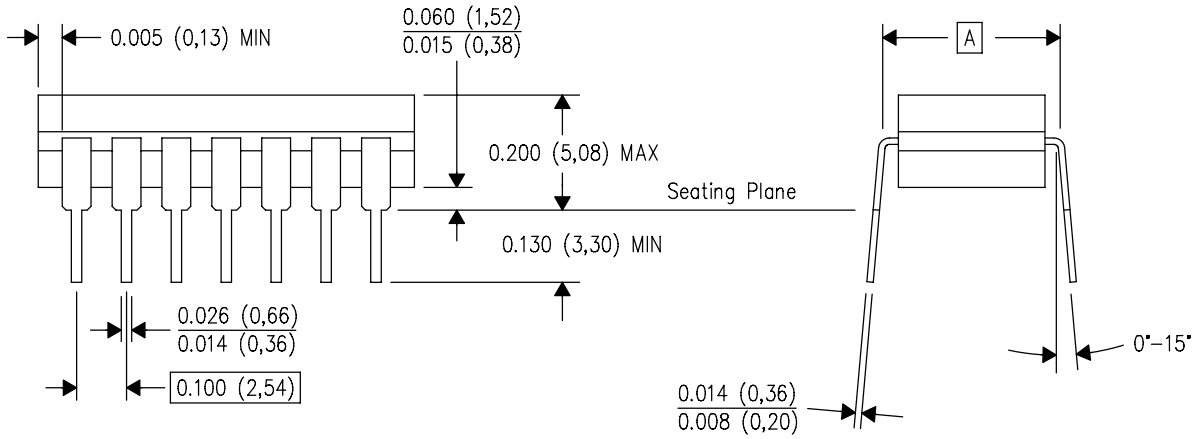
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



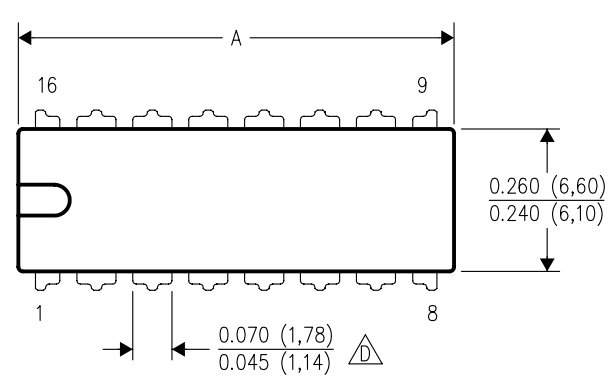

4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

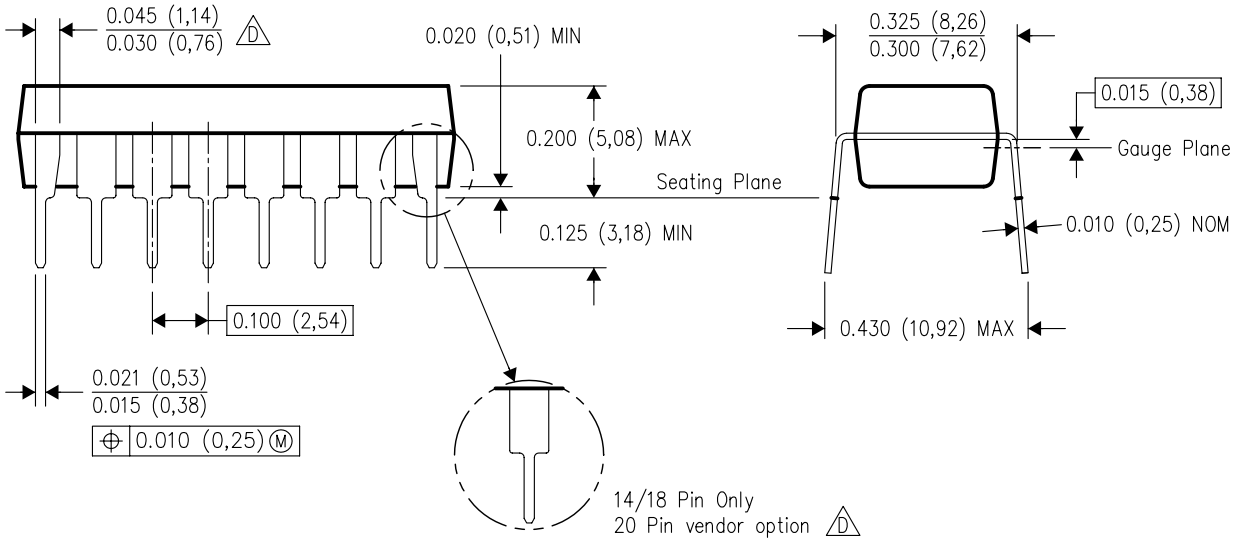
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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