

CDx4HC4020、CDx4HCT4020 高速 CMOS ロジック、14 段バイナリ・カウンタ

1 特長

- 完全静的動作
- バッファ付き入力
- コモン・リセット
- ネガティブ・エッジ・クロッキング
- ファンアウト (全温度範囲にわたって)
 - 標準出力: 10 個の LSTTL 負荷
 - バス・ドライバ出力: 15 個の LSTTL 負荷
- 広い動作温度範囲: -55°C ~ 125°C
- 平衡な伝搬遅延と遷移時間
- LSTTL ロジック IC に比べて消費電力を大幅削減
- HC タイプ
 - 2V ~ 6V で動作
 - 優れたノイズ耐性: V_{CC} に対して $N_{\text{IL}} = 30\%$ 、 $N_{\text{IH}} = 30\%$ ($V_{\text{CC}} = 5\text{V}$ 時)
- HCT タイプ
 - 4.5V ~ 5.5V で動作
 - LSTTL 入力ロジックと直接互換、 $V_{\text{IL}} = 0.8\text{V}$ (最大値)、 $V_{\text{IH}} = 2\text{V}$ (最小値)
 - CMOS 入力互換、 V_{OL} 、 V_{OH} で $I_{\text{L}} \leq 1\mu\text{A}$

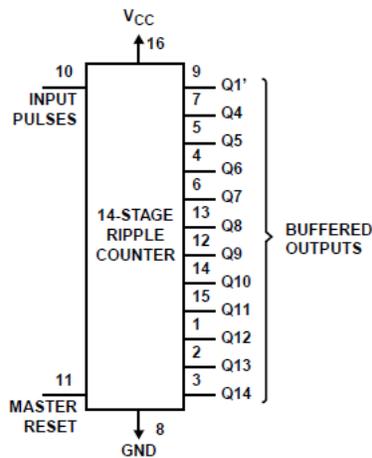
2 概要

'HC4020 および 'HCT4020 は、14 段リップルキャリー・バイナリ・カウンタです。すべてのカウンタ段は、コントローラ / ペリフェラルのフリップ・フロップです。段の状態は、各入力パルスの負のクロック遷移時に 1 カウント進み、MR ラインが High 電圧レベルになると、すべてのカウンタがゼロ状態にリセットされます。すべての入出力はバッファ付きです。

製品情報

部品番号	パッケージ ⁽¹⁾	本体サイズ (公称)
CD54HC4020	J (CDIP, 16)	24.38mm × 6.92mm
CD74HC4020CD74HC4020	D (SOIC, 16)	9.90mm × 3.90mm
	N (PDIP, 16)	19.31mm × 6.35mm
CD54HCT4020	J (CDIP, 16)	24.38mm × 6.92mm
CD74HCT4020CD74HCT4020	D (SOIC, 16)	9.90mm × 3.90mm
	N (PDIP, 16)	19.31mm × 6.35mm

- (1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



機能ブロック図



Table of Contents

1 特長	1	7.2 Functional Block Diagram.....	9
2 概要	1	7.3 Device Functional Modes.....	10
3 Revision History	2	8 Power Supply Recommendations	11
4 Pin Configuration and Functions	3	9 Layout	11
5 Specifications	4	9.1 Layout Guidelines.....	11
5.1 Absolute Maximum Ratings.....	4	10 Device and Documentation Support	12
5.2 Recommended Operating Conditions.....	4	10.1 Receiving Notification of Documentation Updates..	12
5.3 Thermal Information.....	4	10.2 サポート・リソース.....	12
5.4 Electrical Characteristics.....	5	10.3 Trademarks.....	12
5.5 Prerequisite for Switching Characteristics.....	6	10.4 Electrostatic Discharge Caution.....	12
5.6 Switching Characteristics.....	6	10.5 Glossary.....	12
6 Parameter Measurement Information	8	11 Mechanical, Packaging, and Orderable Information	12
7 Detailed Description	9		
7.1 Overview.....	9		

3 Revision History

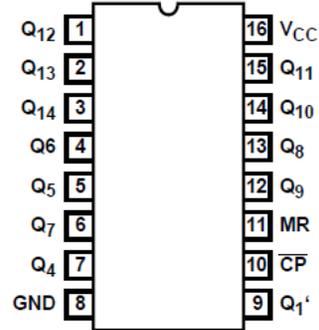
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (October 2003) to Revision D (August 2022)

Page

- 最新のデータシート規格を反映するように、文書全体の採番、書式設定、表、図、相互参照を更新..... 1

4 Pin Configuration and Functions



J, N, or D package
16-PIN CDIP, PDIP, or SOIC
Top View

5 Specifications

5.1 Absolute Maximum Ratings

		MIN	MAX	UNIT
V_{CC}	Supply voltage	-0.5	7	V
I_{IK}	Input diode current	For $V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$		± 20 mA
I_{OK}	Output diode current	For $V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$		± 20 mA
I_O	Output source or sink current per output pin	For $V_O > -0.5\text{ V}$ or $V_O < V_{CC} + 0.5\text{ V}$		± 25 mA
	Continuous current through V_{CC} or GND		± 50	mA
T_J	Junction temperature		150	$^{\circ}\text{C}$
T_{stg}	Storage temperature range	-65	150	$^{\circ}\text{C}$
	Lead temperature (Soldering 10s) (SOIC - lead tips only)		300	$^{\circ}\text{C}$

5.2 Recommended Operating Conditions

		MIN	MAX	UNIT	
V_{CC}	Supply voltage range	HC types	2	6	V
		HCT types	4.5	5.5	
V_I, V_O	DC input or output voltage	0	V_{CC}	V	
	Input rise and fall time	2 V		1000	ns
		4.5 V		500	
		6 V		400	
T_A	Temperature range	-55	125	$^{\circ}\text{C}$	

5.3 Thermal Information

THERMAL METRIC		D (SOIC)	N (PDIP)	UNIT
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance ⁽¹⁾	73	67	$^{\circ}\text{C}/\text{W}$

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.4 Electrical Characteristics

PARAMETER		TEST CONDITIONS ⁽²⁾	V _{CC} (V)	25°C			-40°C to 85°C		-55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
V _{IH}	High level input voltage		2	1.5		1.5		1.5		V	
			4.5	3.15		3.15		3.15			
			6	4.2		4.2		4.2			
V _{IL}	Low level input voltage		2		0.5		0.5		0.5	V	
			4.5		1.35		1.35		1.35		
			6		1.8		1.8		1.8		
V _{OH}	High level output voltage CMOS loads	I _{OH} = -20 μA	2	1.9		1.9		1.9		V	
		I _{OH} = -20 μA	4.5	4.4		4.4		4.4			
		I _{OH} = -20 μA	6	5.9		5.9		5.9			
	High level output voltage TTL loads	I _{OH} = 4 mA	4.5	3.98		3.84		3.7		V	
		I _{OH} = 5.2 mA	6	5.48		5.34		5.2			
V _{OL}	Low level output voltage CMOS loads	I _{OL} = 20 μA	2		0.1		0.1		0.1	V	
		I _{OL} = 20 μA	4.5		0.1		0.1		0.1		
		I _{OL} = 20 μA	6		0.1		0.1		0.1		
	Low level output voltage TTL loads	I _{OL} = 4 mA	4.5		0.26		0.33		0.4	V	
		I _{OL} = 5.2 mA	6		0.26		0.33		0.4		
I _I	Input leakage current	V _{CC} or GND	6		±0.1		±1		±1	μA	
I _{CC}	Supply current	V _{CC} or GND	6		8		80		160	μA	
HCT TYPES											
V _{IH}	High level input voltage		4.5 to 5.5	2			2		2	V	
V _{IL}	Low level input voltage		4.5 to 5.5		0.8		0.8		0.8	V	
V _{OH}	High level output voltage CMOS loads	I _{OH} = -20 μA	4.5	4.4		4.4		4.4		V	
	High level output voltage TTL loads	I _{OH} = -4 mA	4.5	3.98		3.84		3.7		V	
V _{OL}	Low level output voltage CMOS loads	I _{OL} = 20 μA	4.5		0.1		0.1		0.1	V	
	Low level output voltage TTL loads	I _{OL} = 4 mA	4.5		0.26		0.33		0.4	V	
I _I	Input leakage current	V _{CC} and GND	5.5		±0.1		±1		±1	μA	
I _{CC}	Supply current	V _{CC} or GND	5.5		8		80		160	μA	
ΔI _{CC} ⁽¹⁾	Additional supply current per input pin	MR input held at V _{CC} - 2.1	4.5 to 5.5	100	234		292.5		318.5	μA	
		CP input held at V _{CC} - 2.1	4.5 to 5.5	100	180		225		245	μA	

(1) For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

(2) V_I = V_{IH} or V_{IL}, unless otherwise noted.

5.5 Prerequisite for Switching Characteristics

PARAMETER		V _{CC} (V)	25°C			-40°C to 85°C		-55°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES										
f _{MAX}	Maximum input pulse frequency	2	6			5		4		MHz
		4.5	30			25		20		
		6	35			29		24		
t _W	Input pulse width	2	80			100		120		ns
		4.5	16			20		24		
		6	14			17		20		
t _{REM}	Reset removal time	2	50			65		75		ns
		4.5	10			13		15		
		6	9			11		13		
t _W	Reset pulse width	2	80			100		120		ns
		4.5	16			20		24		
		6	14			17		20		
HCT TYPES										
f _{MAX}	Maximum input pulse frequency	4.5	25			20		16		MHz
t _W	Input pulse width	4.5	20			25		30		ns
t _{REC}	Reset recovery time	4.5	10			13		15		ns
t _W	Reset pulse width	4.5	20			25		30		ns

5.6 Switching Characteristics

Input t_r, t_f = 6 ns. See [Parameter Measurement Information](#)

PARAMETER		TEST CONDITIONS	V _{CC} (V)	25°C			-40°C to 85°C		-55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
t _{PLH} , t _{PHL}	Propagation delay time CP to Q1' Output	C _L = 50 pF	2	140			175		210		ns
			4.5	28			35		42		
		C _L = 15 pF	5	11							
		C _L = 50 pF	6	24			30		36		
t _{PLH} , t _{PHL}	Q _n to Q _n + 1	C _L = 50 pF	2	75			95		110		ns
			4.5	15			19		22		
		C _L = 15 pF	5	6							
		C _L = 50 pF	6	13			16		19		
t _{PLH} , t _{PHL}	MR to Q _n	C _L = 50 pF	2	170			215		255		ns
			4.5	34			43		51		
			5	14							
			6	29			37		43		
t _{TLH} , t _{THL}	Output transition time	C _L = 50 pF	2	75			95		110		ns
			4.5	15			19		22		
			6	13			16		19		
C _{IN}	Input capacitance	C _L = 50 pF		10			10		10		pF
C _{PD}	Power dissipation capacitance ^{(1) (2)}	C _L = 15 pF	5	30							pF
HCT TYPES											

5.6 Switching Characteristics (continued)

Input t_r , t_f = 6 ns. See [Parameter Measurement Information](#)

PARAMETER		TEST CONDITIONS	V_{CC} (V)	25°C			-40°C to 85°C		-55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} , t_{PHL}	Propagation delay time	$C_L = 50$ pF	4.5		40		50		60	ns	
	CP to Q1' Output	$C_L = 15$ pF	5	17							
t_{PLH} , t_{PHL}	Q _n to Q _n + 1	$C_L = 50$ pF	4.5		15		19		22	ns	
		$C_L = 15$ pF	5	6							
t_{PLH} , t_{PHL}	MR to Q _n	$C_L = 50$ pF	4.5		40		50		60	ns	
		$C_L = 15$ pF	5	17							
t_{TLH} , t_{THL}	Output transition	$C_L = 50$ pF	4.5		15		19		22	ns	
C_{IN}	Input capacitance	$C_L = 50$ pF			10		10		10	pF	
C_{PD}	Power dissipation capacitance ^{(1) (2)}	$C_L = 15$ pF	5	30						pF	

(1) C_{PD} is used to determine the dynamic power consumption, per package.

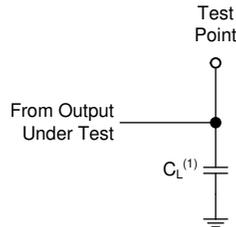
(2) $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = Input frequency, C_L = Output load capacitance, V_{CC} = Supply Voltage.

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_t < 6 \text{ ns}$.

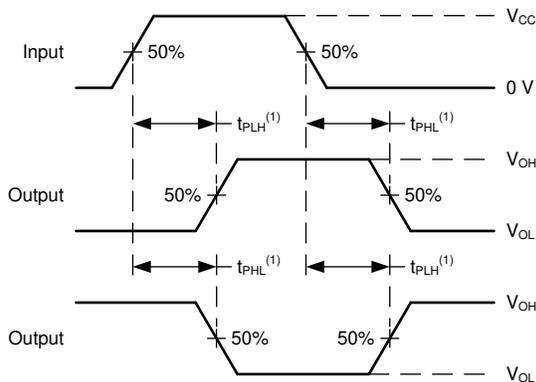
For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



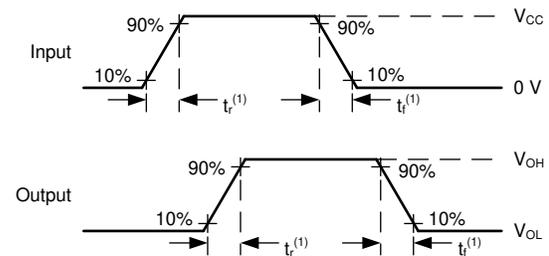
(1) C_L includes probe and test-fixture capacitance.

6-1. Load Circuit for Push-Pull Outputs



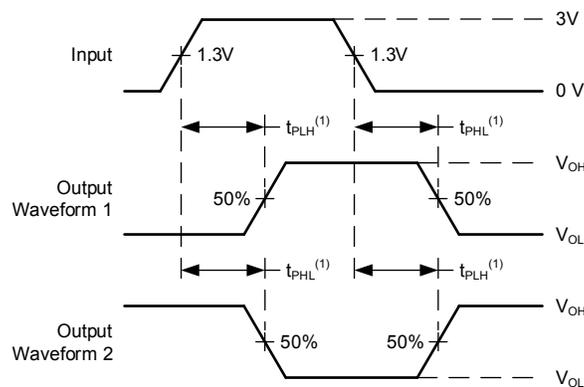
(1) The greater between t_{pLH} and t_{pHL} is the same as t_{pd} .

6-2. Voltage Waveforms, Propagation Delays for Standard CMOS Inputs



(1) The greater between t_r and t_f is the same as t_t .

6-3. Voltage Waveforms, Input and Output Transition Times for Standard CMOS Inputs



(1) The greater between t_{pLH} and t_{pHL} is the same as t_{pd} .

6-4. Voltage Waveforms, Propagation Delays for TTL-Compatible Inputs

7.3 Device Functional Modes

表 7-1. Truth Table

CP COUNT ⁽¹⁾	MR	OUTPUT STATE
↑	L	No change
↓	L	Advance to next state
X	H	All outputs are low

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care
↑ = Transition from Low to High Level, ↓ = Transition from High to Low.

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μF and 1- μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の [使用条件](#) を参照してください。

10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-8945801EA	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8945801EA CD54HCT4020F3A
CD54HC4020F	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC4020F
CD54HC4020F.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC4020F
CD54HC4020F3A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8500301EA CD54HC4020F3A
CD54HC4020F3A.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8500301EA CD54HC4020F3A
CD54HCT4020F3A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8945801EA CD54HCT4020F3A
CD54HCT4020F3A.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8945801EA CD54HCT4020F3A
CD74HC4020E	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC4020E
CD74HC4020E.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC4020E
CD74HC4020EE4	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC4020E
CD74HC4020M	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	HC4020M
CD74HC4020M96	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-55 to 125	HC4020M
CD74HC4020M96.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4020M
CD74HC4020M961G4	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4020M
CD74HC4020M961G4.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4020M
CD74HCT4020E	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT4020E
CD74HCT4020E.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT4020E
CD74HCT4020M	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	HCT4020M
CD74HCT4020M96	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4020M
CD74HCT4020M96.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4020M
CD74HCT4020MT	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	HCT4020M

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD54HC4020, CD54HCT4020, CD74HC4020, CD74HCT4020 :

- Catalog : [CD74HC4020](#), [CD74HCT4020](#)
- Military : [CD54HC4020](#), [CD54HCT4020](#)

NOTE: Qualified Version Definitions:

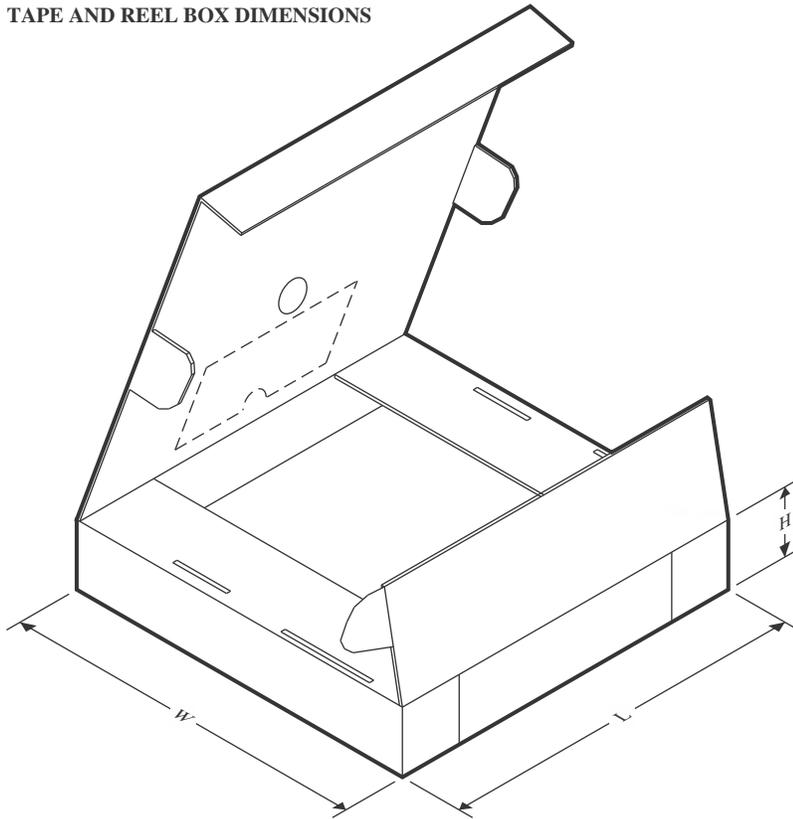
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC4020M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC4020M961G4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HCT4020M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC4020M96	SOIC	D	16	2500	353.0	353.0	32.0
CD74HC4020M961G4	SOIC	D	16	2500	353.0	353.0	32.0
CD74HCT4020M96	SOIC	D	16	2500	340.5	336.1	32.0

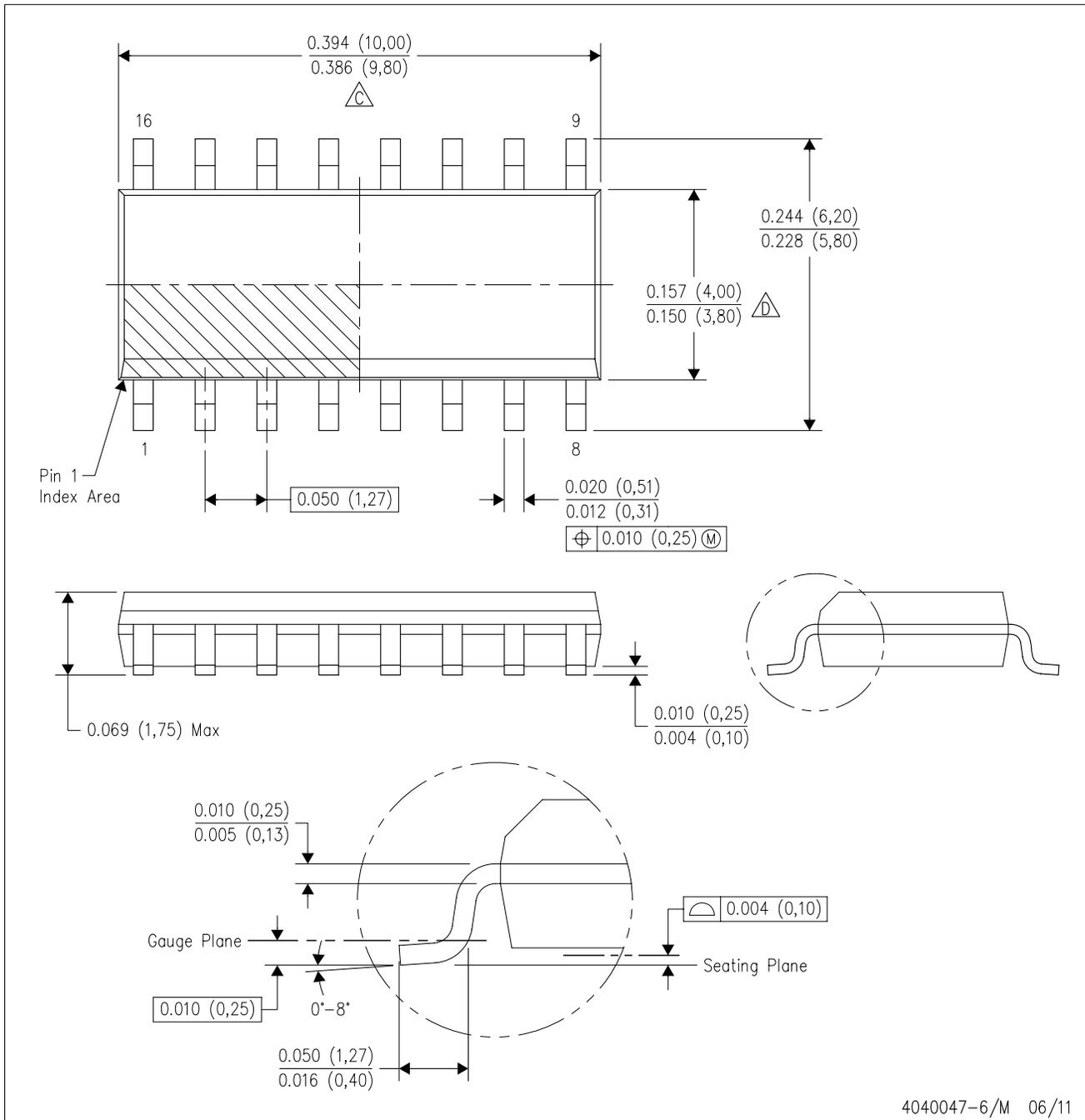
TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD74HC4020E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC4020E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC4020E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC4020E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC4020EE4	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC4020EE4	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT4020E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT4020E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT4020E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT4020E.A	N	PDIP	16	25	506	13.97	11230	4.32

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

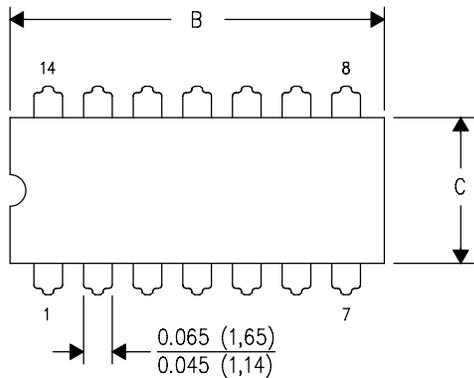


4040047-6/M 06/11

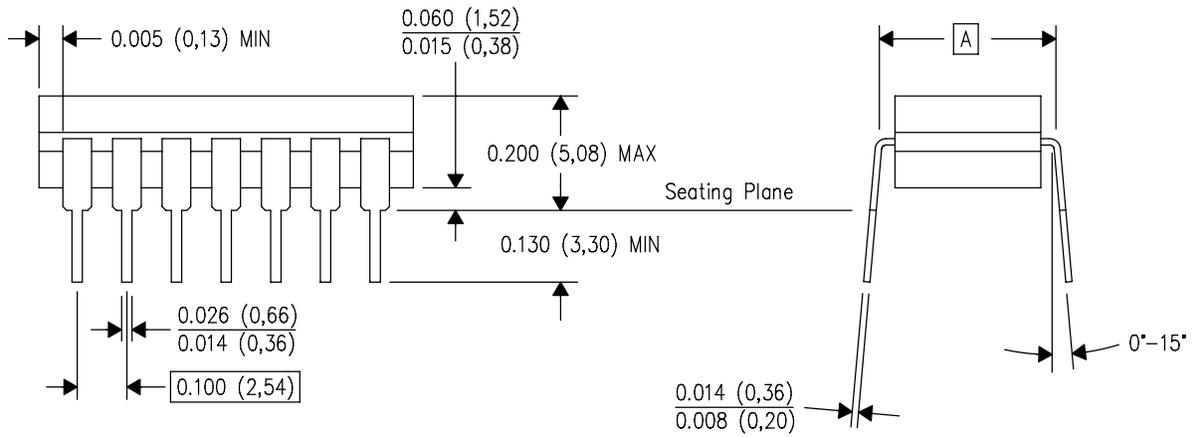
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

J (R-GDIP-T**)
14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、[TI の総合的な品質ガイドライン](#)、[ti.com](#) または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

Copyright © 2026, Texas Instruments Incorporated

最終更新日 : 2025 年 10 月