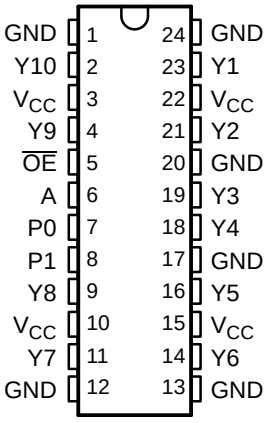
CDC351. CDC351I
1-LINE TO 10-LINE CLOCK DRIVER WITH 3-STATE OUTPUTS

SCAS441D – FEBRUARY 1994 – REVISED OCTOBER 2003

FEATURES

- **Low Output Skew, Low Pulse Skew for Clock-Distribution and Clock-Generation Applications**
- **Operates at 3.3-V V_{CC}**
- **LVTTL-Compatible Inputs and Outputs**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Distributes One Clock Input to Ten Outputs**
- **Distributed V_{CC} and Ground Pins Reduce Switching Noise**
- **High-Drive Outputs (–32-mA I_{OH}, 32-mA I_{OL})**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Package Options Include Plastic Small-Outline (DW) and Shrink Small-Outline (DB) Packages**

DB OR DW PACKAGE
(TOP VIEW)



DESCRIPTION

The CDC351 is a high-performance clock-driver circuit that distributes one input (A) to ten outputs (Y) with minimum skew for clock distribution. The output-enable ($\overline{OE}$) input disables the outputs to a high-impedance state. The CDC351 operates at nominal 3.3-V V_{CC}.

The propagation delays are adjusted at the factory using the P0 and P1 pins. The factory adjustments ensure that the part-to-part skew is minimized and is kept within a specified window. Pins P0 and P1 are not intended for customer use and should be connected to GND.

FUNCTION TABLE

INPUTS		OUTPUTS Yn
A	$\overline{OE}$	
L	H	Z
H	H	Z
L	L	L
H	L	H

AVAILABLE OPTIONS

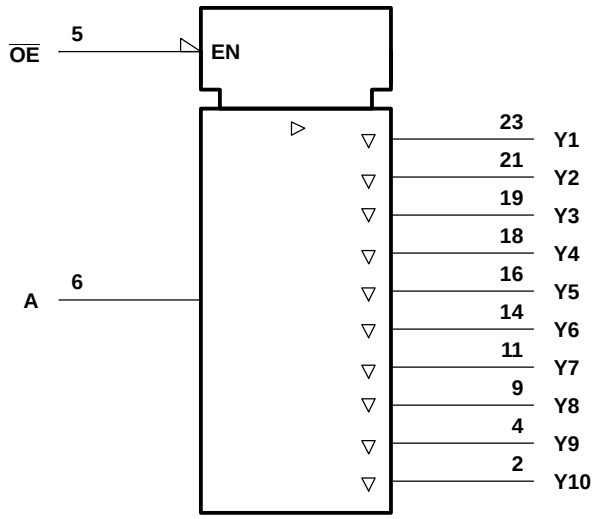
T_A	Shrink Small-Outline Package (DB) (1)	Small-Outline Package (DW) (1)
0°C to 70°C	CDC351DB	CDC351DW
– 40°C to 85°C	CDC351IDB	CDC351IDW

(1) This package is available tape and reel. Order by adding an R to the orderable part number (e.g., CDC351DBR).

EPIC-IIB is a trademark of Texas Instruments.

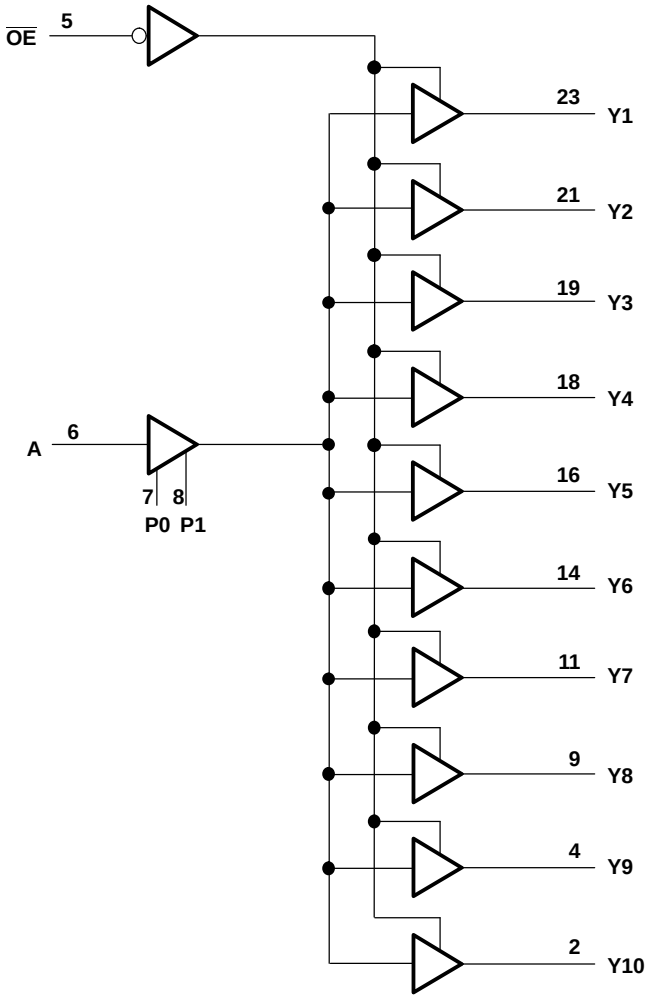
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

LOGIC SYMBOL [A]



Note A: This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

LOGIC DIAGRAM (POSITIVE LOGIC)



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

Supply voltage range, V_{CC}		– 0.5 V to 4.6 V
Input voltage range, V_I (2)		– 0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state,	V_O (2)	– 0.5 V to 3.6 V
Current into any output in the low state, I_O		64 mA
Input clamp current, I_{IK}(V_I < 0)		– 18 mA
Output clamp current, I_{OK} (V_I < 0)		– 50 mA
Package thermal impedance Θ_{JA} (3):	DB package	147°C/ W
	DW package	101°C/ W
Storage temperature range, T_{stg}		– 65°C to 150°C

(1) Stresses beyond those listed under„ absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under„ recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD51.

RECOMMENDED OPERATING CONDITIONS (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		3	3.6	V
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage		0	5.5	V
I_{OH}	High-level output current			– 32	mA
I_{OL}	Low-level output current			32	mA
f_{clock}	Input clock frequency			100	MHz
T_A	Operating free-air temperature	Commercial	0	70	°C
		Industrial	– 40	85	°C

(1) Unused pins (input or I/O) must be held high or low.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IK}	V_{CC} = 3 V,	I_I = –18 mA				–1.2	V
V_{OH}	V_{CC} = 3 V,	I_{OH} = –32 mA		2			V
V_{OL}	V_{CC} = 3 V,	I_{OL} = 32 mA				0.5	V
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND				±1	µA
I_O (1)	V_{CC} = 3.6 V,	V_O = 2.5 V		–15		–150	mA
I_{OZ}	V_{CC} = 3.6 V,	V_O = 3 V or 0				±10	µA
I_{CC}	V_{CC} = 3.6 V, I_O = 0, V_I = V_{CC} or GND		Outputs high			0.3	mA
			Outputs low			25	
			Outputs disabled			0.3	
C_i	V_I = V_{CC} or GND,	V_{CC} = 3.3 V,	f = 10 MHz		4		pF
C_o	V_O = V_{CC} or GND,	V_{CC} = 3.3 V,	f = 10 MHz		6		pF

(1) Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

SWITICHING CHARACTERISTICS

C_L = 50 pF (see Figure 1 and Figure 2)

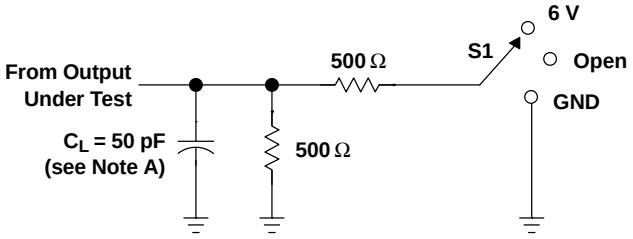
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V, T_A = 25°C			V_{CC} = 3 V to 3.6 V, T_A = 0°C to 70°C		V_{CC} = 3 V to 3.6 V, T_A = -40°C to 85°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	3.2	3.7	4.2					ns
t_{PHL}			3	3.5	4					
t_{PZH}	$\overline{OE}$	Y	1.8	3.8	5.5	1.3	5.9	1.1	6.1	ns
t_{PZL}			1.8	3.8	5.5	1.3	5.9	1.1	6.1	
t_{PHZ}	$\overline{OE}$	Y	1.8	3.9	5.9	1.7	6.3	1.5	6.5	ns
t_{PLZ}			1.8	4.2	5.9	1.7	6.4	1.5	6.6	
$t_{sk(o)}$	A	Y		0.3	0.5		0.5		0.6	ns
$t_{sk(p)}$	A	Y		0.2	0.8		0.8		0.9	ns
$t_{sk(pr)}$	A	Y			1		1		1.1	ns
t_r	A	Y					1.5		1.5	ns
t_f	A	Y					1.5		1.5	ns

SWITCHING CHARACTERISTICS TEMPERATURE AND V_{CC} COEFFICIENTS

over recommended operating free-air temperature and V_{CC} range (1)

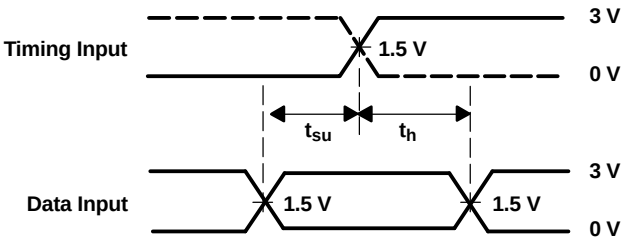
PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
$\S t_{PLH}(T)$	Average temperature coefficient of low to high propagation delay	A	Y		65 (2)	ps/10°C
$\S t_{PHL}(T)$	Average temperature coefficient of high to low propagation delay	A	Y		45 (2)	ps/10°C
$\S t_{PLH}(V_{CC})$	Average V_{CC} coefficient of low to high propagation delay	A	Y		–140 (3)	ps/ 100 mV
$\S t_{PHL}(V_{CC})$	Average V_{CC} coefficient of high to low propagation delay	A	Y		–120 (3)	ps/ 100 mV

(1) These data were extracted from characterization material and are not tested at the factory.
(2) $\S t_{PLH}(T)$ and $\S t_{PHL}(T)$ are virtually independent of V_{CC}.
(3) $\S t_{PLH}(V_{CC})$ and $\S t_{PHL}(V_{CC})$ are virtually independent of temperature.

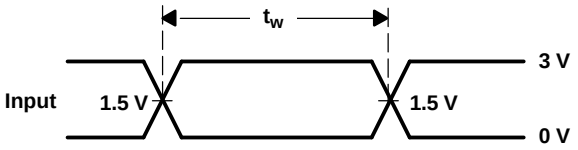


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

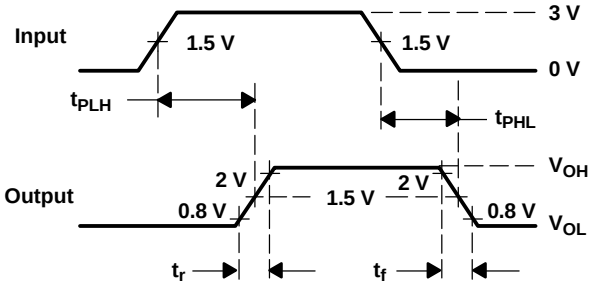
LOAD CIRCUIT



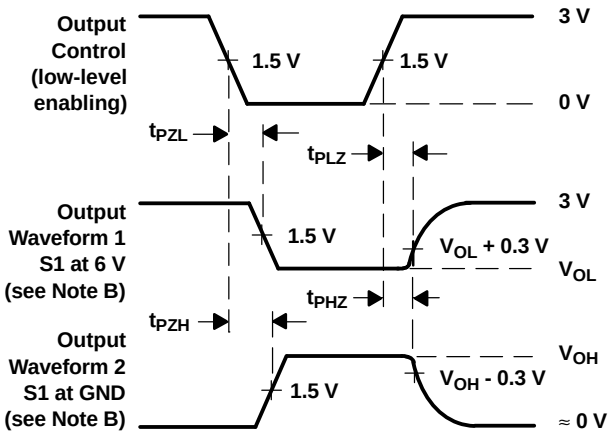
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

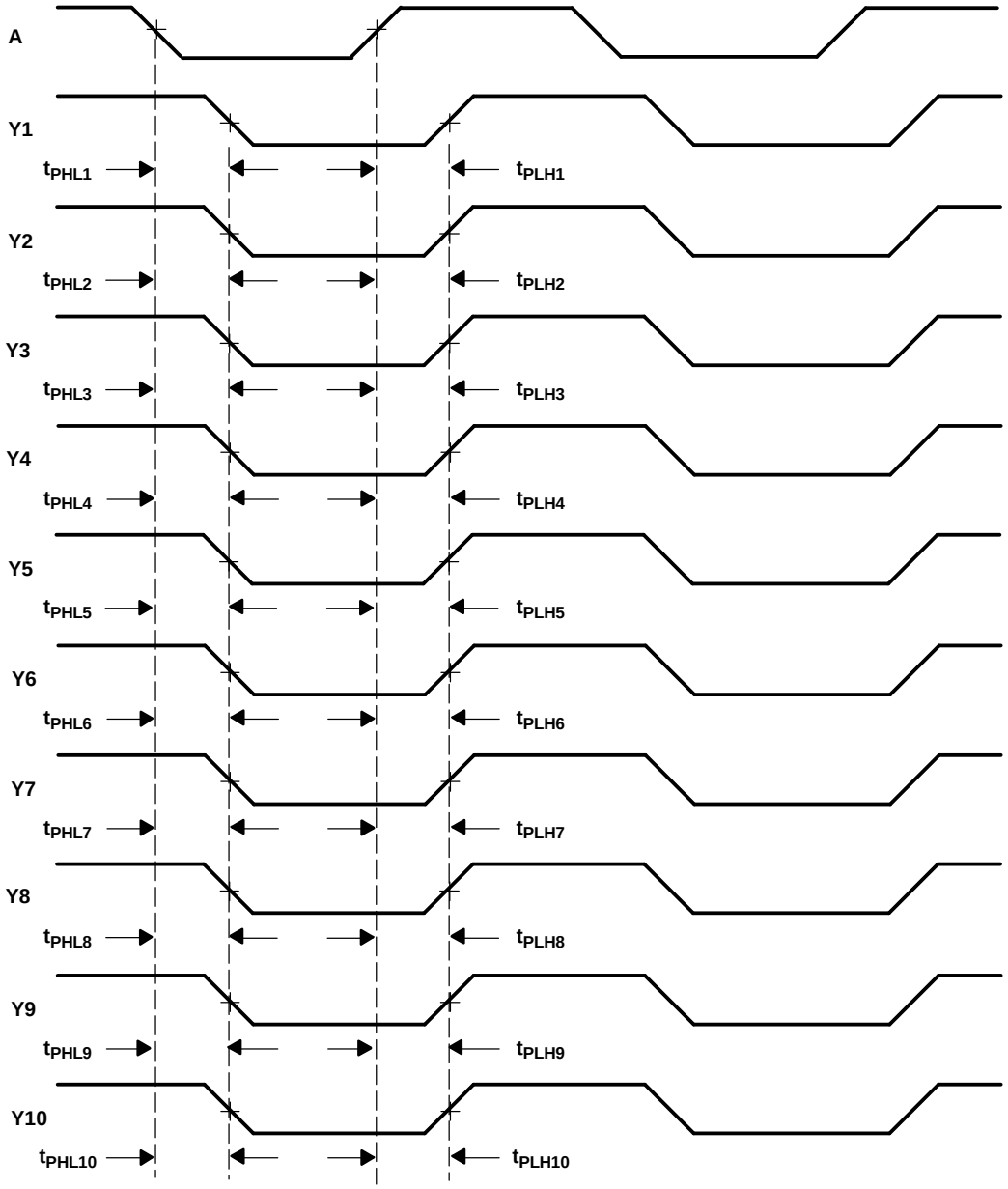
A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r≤ 2.5 ns, t_f≤ 2.5 ns.

D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



A. Output skew, $t_{sk(o)}$, is calculated as the greater of:

— The difference between the fastest and slowest of t_{PLHn} (n = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10)

— The difference between the fastest and slowest of t_{PHLn}(n = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10)

B. Pulse skew, $t_{sk(p)}$, is calculated as the greater of $| t_{PLHn} - t_{PHLn} |$ (n = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10).

C. Process skew, $t_{sk(pr)}$, is calculated as the greater of:

— The difference between the fastest and slowest of t_{PLHn} (n = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10) across multiple devices under identical operating conditions

— The difference between the fastest and slowest of t_{PHLn} (n = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10) across multiple devices under identical operating conditions

Figure 2. Waveforms for Calculation of $t_{sk(o)}$, $t_{sk(p)}$, $t_{sk(pr)}$

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CDC351DB	Active	Production	SSOP (DB) | 24	60 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	CK351
CDC351DB.B	Active	Production	SSOP (DB) | 24	60 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	CK351
CDC351DBG4	Active	Production	SSOP (DB) | 24	60 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CK351
CDC351DBG4.B	Active	Production	SSOP (DB) | 24	60 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CK351
CDC351DBR	Active	Production	SSOP (DB) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	CK351
CDC351DBR.B	Active	Production	SSOP (DB) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	CK351
CDC351DW	Active	Production	SOIC (DW) | 24	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	CDC351
CDC351DW.B	Active	Production	SOIC (DW) | 24	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	CDC351
CDC351DWG4	Active	Production	SOIC (DW) | 24	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	CDC351
CDC351DWR	Active	Production	SOIC (DW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	CDC351
CDC351DWR.B	Active	Production	SOIC (DW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	CDC351
CDC351IDB	Active	Production	SSOP (DB) | 24	60 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CK351-I
CDC351IDB.B	Active	Production	SSOP (DB) | 24	60 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CK351-I
CDC351IDBR	Active	Production	SSOP (DB) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CK351-I
CDC351IDBR.B	Active	Production	SSOP (DB) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CK351-I
CDC351IDBRG4	Active	Production	SSOP (DB) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CK351-I
CDC351IDBRG4.B	Active	Production	SSOP (DB) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CK351-I
CDC351IDW	Active	Production	SOIC (DW) | 24	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDC351-I
CDC351IDW.B	Active	Production	SOIC (DW) | 24	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDC351-I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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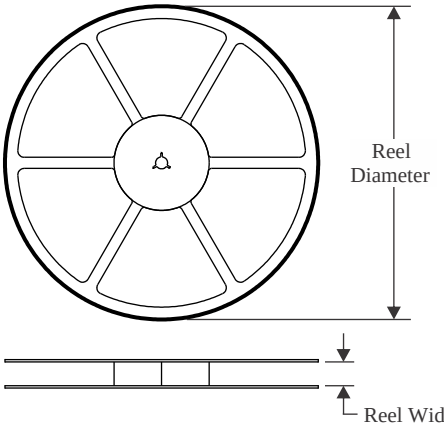
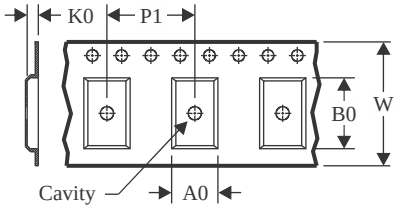
TAPE AND REEL INFORMATION

REEL DIMENSIONS

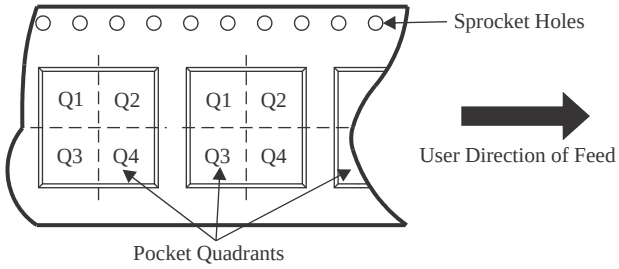


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

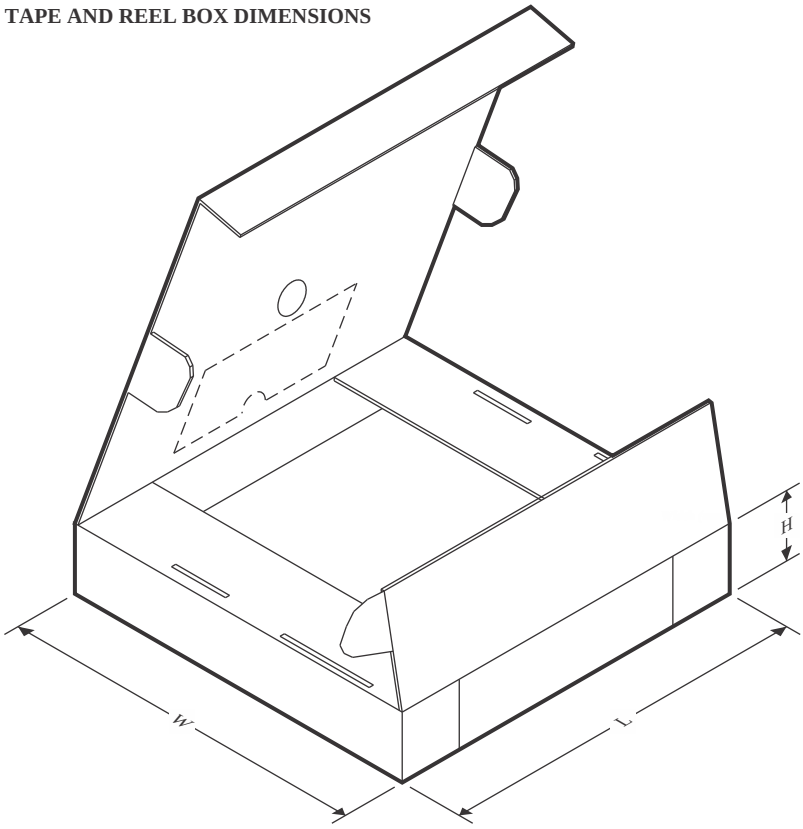
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDC351DBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
CDC351DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
CDC351IDBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
CDC351IDBRG4	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1

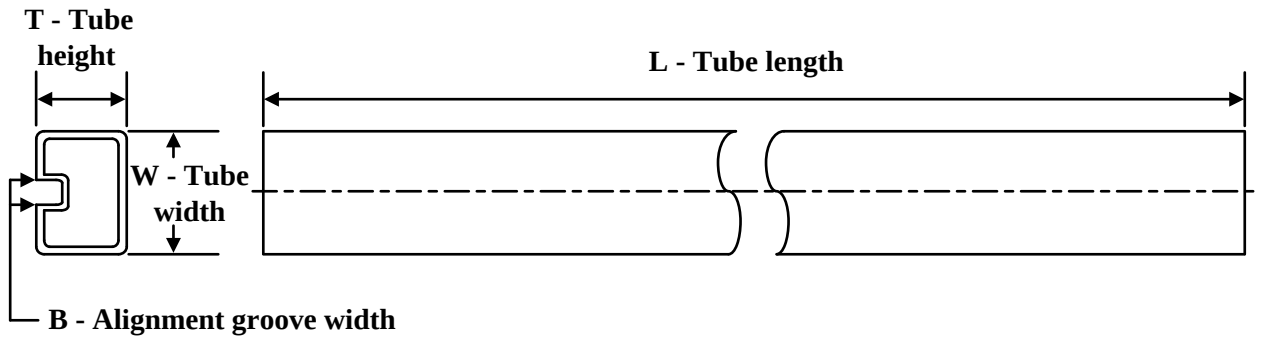
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDC351DBR	SSOP	DB	24	2000	353.0	353.0	32.0
CDC351DWR	SOIC	DW	24	2000	350.0	350.0	43.0
CDC351IDBR	SSOP	DB	24	2000	353.0	353.0	32.0
CDC351IDBRG4	SSOP	DB	24	2000	353.0	353.0	32.0

TUBE



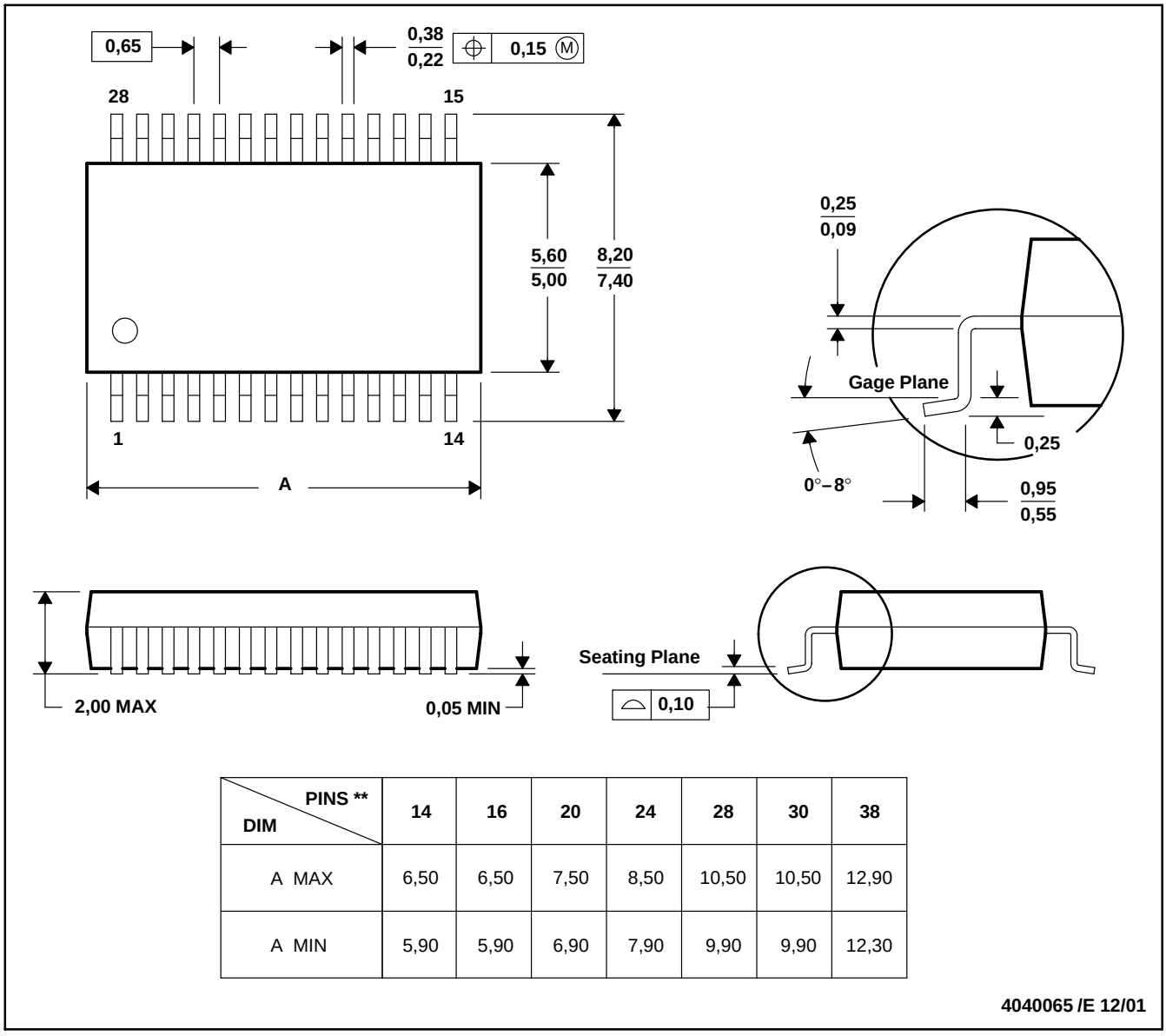
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CDC351DB	DB	SSOP	24	60	530	10.5	4000	4.1
CDC351DB.B	DB	SSOP	24	60	530	10.5	4000	4.1
CDC351DBG4	DB	SSOP	24	60	530	10.5	4000	4.1
CDC351DBG4.B	DB	SSOP	24	60	530	10.5	4000	4.1
CDC351DW	DW	SOIC	24	25	506.98	12.7	4826	6.6
CDC351DW.B	DW	SOIC	24	25	506.98	12.7	4826	6.6
CDC351DWG4	DW	SOIC	24	25	506.98	12.7	4826	6.6
CDC351IDB	DB	SSOP	24	60	530	10.5	4000	4.1
CDC351IDB.B	DB	SSOP	24	60	530	10.5	4000	4.1
CDC351IDW	DW	SOIC	24	25	506.98	12.7	4826	6.6
CDC351IDW.B	DW	SOIC	24	25	506.98	12.7	4826	6.6

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN

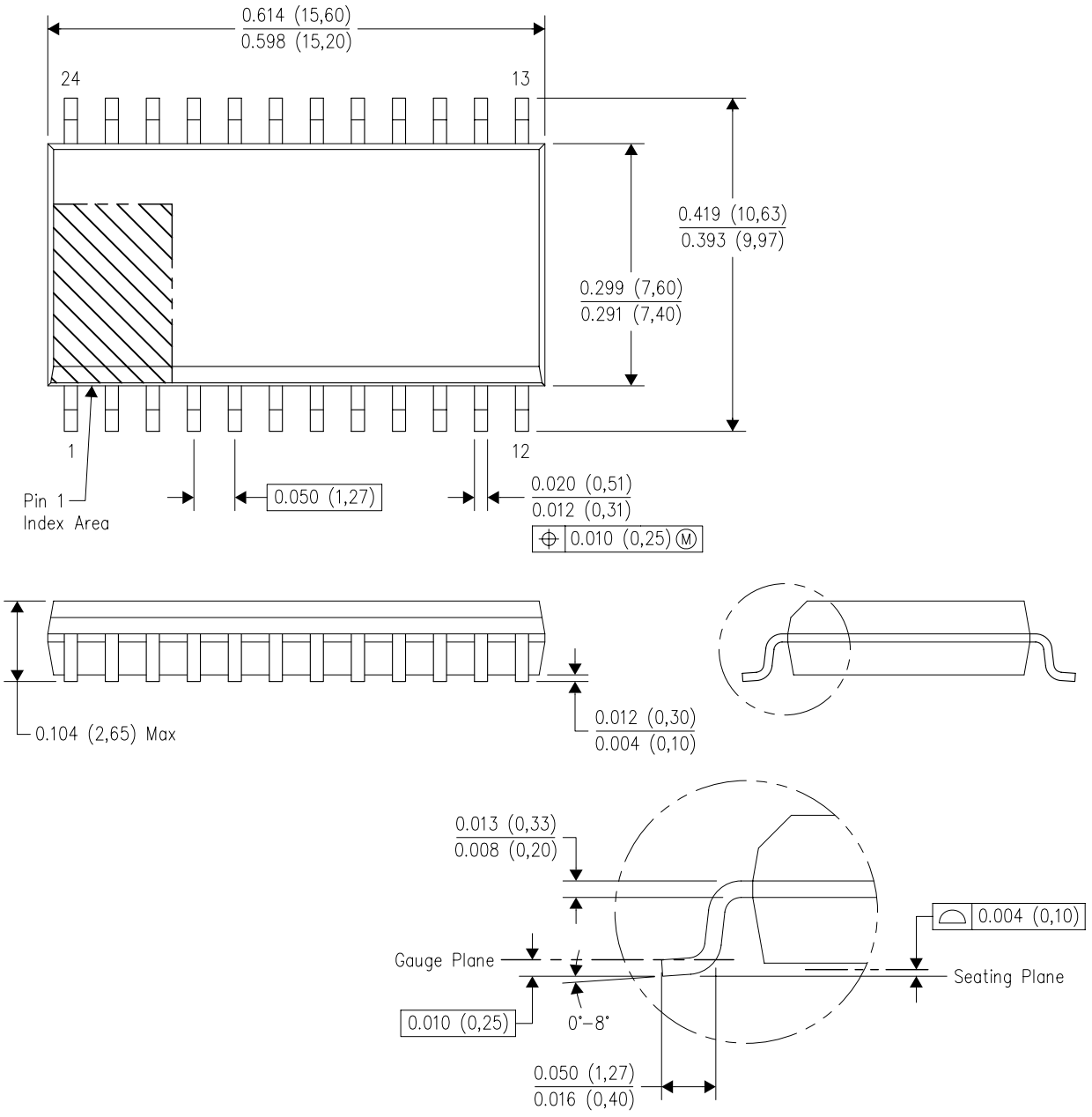


DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

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