

# 30V N-Channel NexFET™ Power MOSFET

 Check for Samples: [CSD17312Q5](#)

## FEATURES

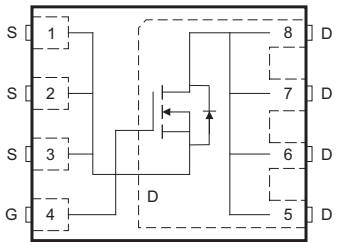
- Optimized for 5V Gate Drive
- Ultra Low  $Q_g$  and  $Q_{gd}$
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5-mm x 6-mm Plastic Package

## APPLICATIONS

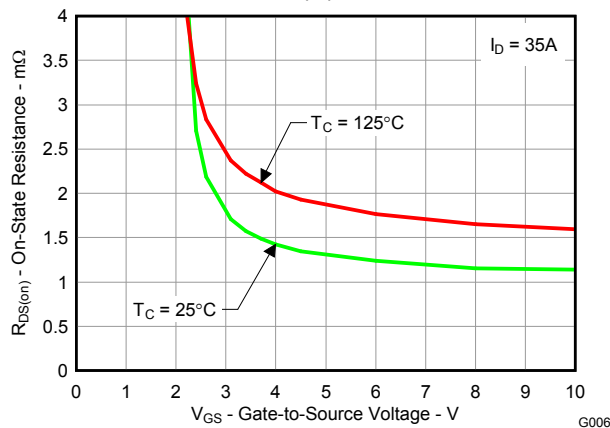
- Notebook Point-of-Load
- Point-of-Load Synchronous Buck in Networking, Telecom and Computing Systems

## DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in power conversion applications and optimized for 5V gate drive applications.

**Top View**


P0094-01

 **$R_{DS(on)}$  vs  $V_{GS}$** 


G006

## PRODUCT SUMMARY

$V_{DS}$	Drain to Source Voltage	30	V
$Q_g$	Gate Charge Total (4.5V)	28	nC
$Q_{gd}$	Gate Charge Gate to Drain	6	nC
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 3V$	1.8 mΩ
		$V_{GS} = 4.5V$	1.4 mΩ
		$V_{GS} = 8V$	1.2 mΩ
$V_{GS(th)}$	Threshold Voltage	1.1	V

## ORDERING INFORMATION

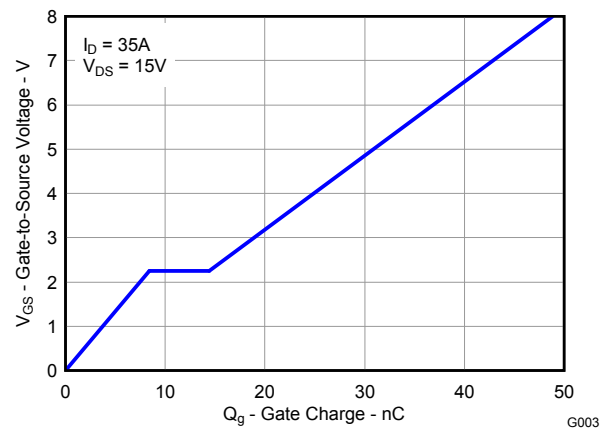
Device	Package	Media	Qty	Ship
CSD17312Q5	SON 5-mm x 6-mm Plastic Package	13-Inch Reel	2500	Tape and Reel

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ unless otherwise stated		VALUE	UNIT
$V_{DS}$	Drain to Source Voltage	30	V
$V_{GS}$	Gate to Source Voltage	+10 / -8	V
$I_D$	Continuous Drain Current, $T_C = 25^\circ\text{C}$	100	A
	Continuous Drain Current <sup>(1)</sup>	38	A
$I_{DM}$	Pulsed Drain Current, $T_A = 25^\circ\text{C}$ <sup>(2)</sup>	200	A
$P_D$	Power Dissipation <sup>(1)</sup>	3.2	W
$T_J, T_{STG}$	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$E_{AS}$	Avalanche Energy, Single Pulse $I_D = 130A, L = 0.1mH, R_G = 25\Omega$	845	mJ

(1) Typical  $R_{\theta JA} = 39^\circ\text{C/W}$  when mounted on a 1-inch<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz. (0.071-mm thick) Cu pad on a 0.06-inch (1.52-mm) thick FR4 PCB.

(2) Pulse duration  $\leq 300\mu\text{s}$ , duty cycle  $\leq 2\%$

**GATE CHARGE**


G003



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ELECTRICAL CHARACTERISTICS

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Static Characteristics</b>						
$BV_{DSS}$	Drain to Source Voltage	$V_{GS} = 0V, I_D = 250\mu\text{A}$	30			V
$I_{DSS}$	Drain to Source Leakage Current	$V_{GS} = 0V, V_{DS} = 24V$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{DS} = 0V, V_{GS} = +10/-8V$			100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	0.9	1.1	1.5	V
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 3V, I_D = 35A$		1.8	2.4	m $\Omega$
		$V_{GS} = 4.5V, I_D = 35A$		1.4	1.7	m $\Omega$
		$V_{GS} = 8V, I_D = 35A$		1.2	1.5	m $\Omega$
$g_{fs}$	Transconductance	$V_{DS} = 15V, I_D = 35A$		200		S
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{GS} = 0V, V_{DS} = 15V,$ $f = 1\text{MHz}$		4030	5240	pF
$C_{oss}$	Output Capacitance			2220	2890	pF
$C_{riss}$	Reverse Transfer Capacitance			93	120	pF
$R_G$	Series Gate Resistance			1.1	2.2	$\Omega$
$Q_g$	Gate Charge Total (4.5V)	$V_{DS} = 15V,$ $I_{DS} = 35A$		28	36	nC
$Q_{gd}$	Gate Charge Gate to Drain			6		nC
$Q_{gs}$	Gate Charge Gate to Source			8.4		nC
$Q_{g(th)}$	Gate Charge at $V_{th}$			4.4		nC
$Q_{oss}$	Output Charge	$V_{DS} = 14.8V, V_{GS} = 0V$		57		nC
$t_{d(on)}$	Turn On Delay Time	$V_{DS} = 15V, V_{GS} = 4.5V,$ $I_{DS} = 35A, R_G = 2\Omega$		9.5		ns
$t_r$	Rise Time			27		ns
$t_{d(off)}$	Turn Off Delay Time			35		ns
$t_f$	Fall Time			23		ns
<b>Diode Characteristics</b>						
$V_{SD}$	Diode Forward Voltage	$I_{SD} = 35A, V_{GS} = 0V$	0.8	1		V
$Q_{rr}$	Reverse Recovery Charge	$V_{DD} = 14.8V, I_F = 35A,$ $di/dt = 300A/\mu\text{s}$		88		nC
$t_{rr}$	Reverse Recovery Time			43		ns

## THERMAL CHARACTERISTICS

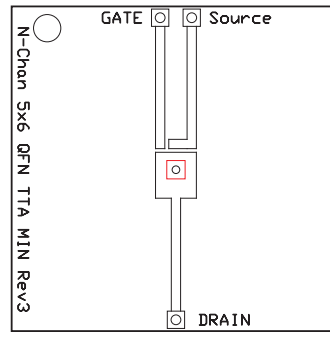
( $T_A = 25^\circ\text{C}$  unless otherwise stated)

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case <sup>(1)</sup>			1	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient <sup>(1)(2)</sup>			49	$^\circ\text{C/W}$

- (1)  $R_{\theta JC}$  is determined with the device mounted on a 1-inch<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB.  $R_{\theta JC}$  is specified by design, whereas  $R_{\theta JA}$  is determined by the user's board design.
- (2) Device mounted on FR4 material with 1-inch<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz. (0.071-mm thick) Cu.



Max  $R_{\theta JA} = 49^{\circ}\text{C/W}$   
when mounted on  
1 inch<sup>2</sup> (6.45 cm<sup>2</sup>) of  
2-oz. (0.071-mm thick)  
Cu.



Max  $R_{\theta JA} = 119^{\circ}\text{C/W}$   
when mounted on a  
minimum pad area of  
2-oz. (0.071-mm thick)  
Cu.

### TYPICAL MOSFET CHARACTERISTICS

( $T_A = 25^{\circ}\text{C}$  unless otherwise stated)

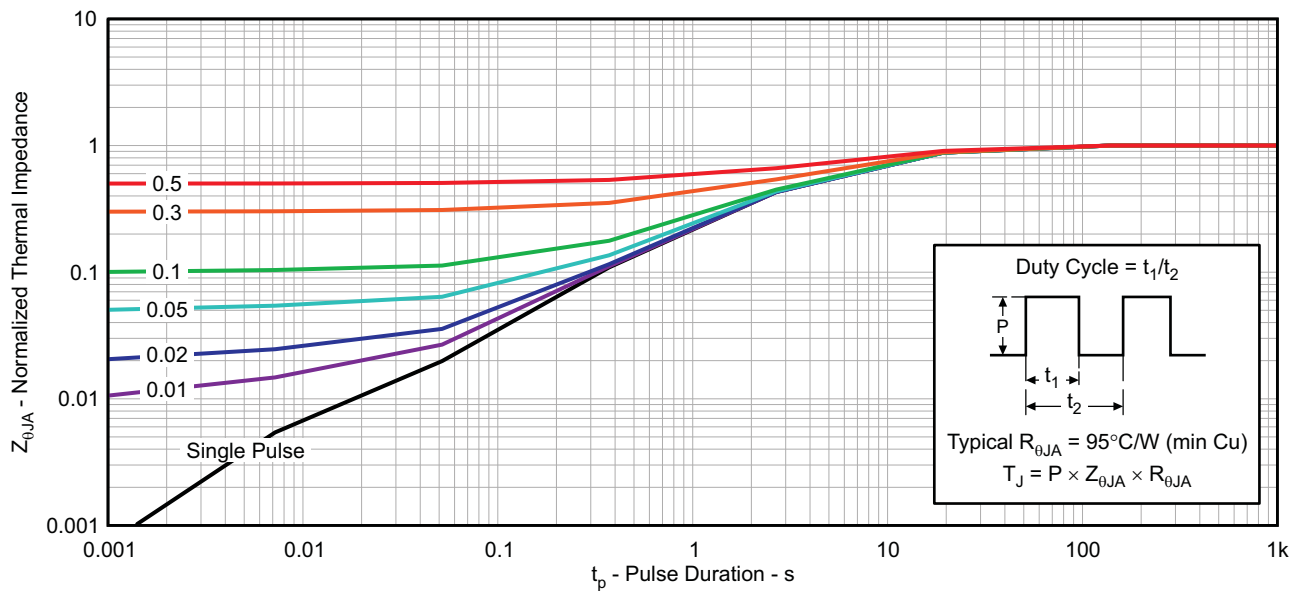
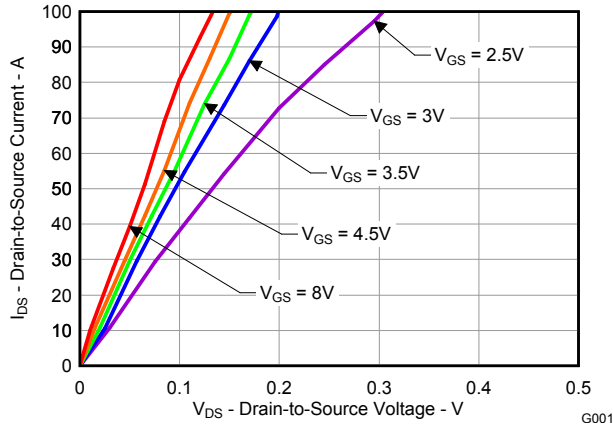


Figure 1. Transient Thermal Impedance

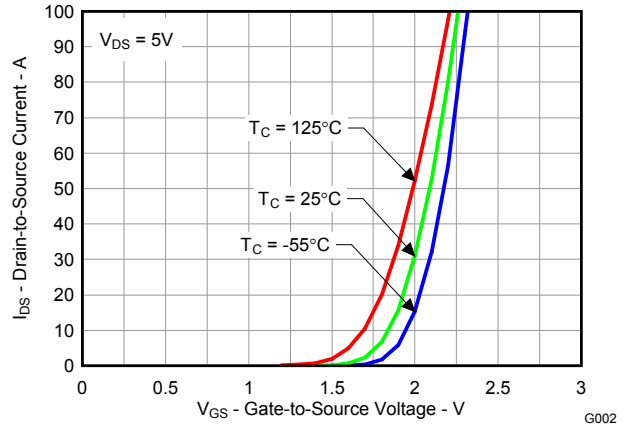
G012

**TYPICAL MOSFET CHARACTERISTICS (continued)**

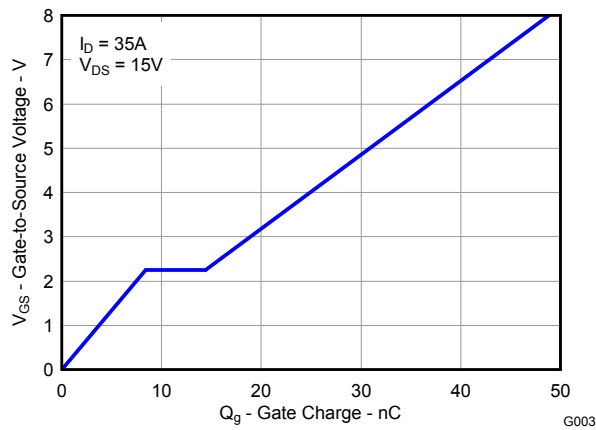
( $T_A = 25^\circ\text{C}$  unless otherwise stated)



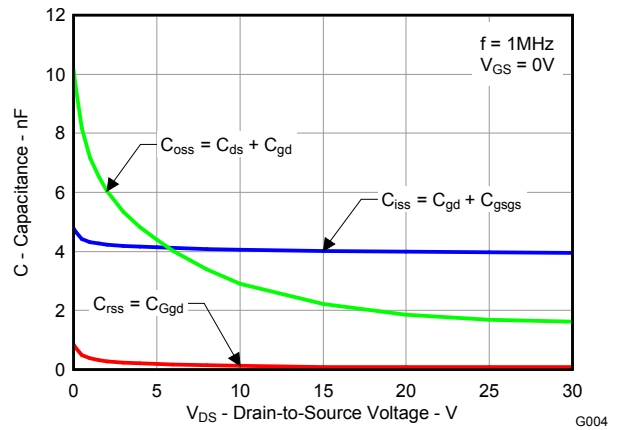
**Figure 2. Saturation Characteristics**



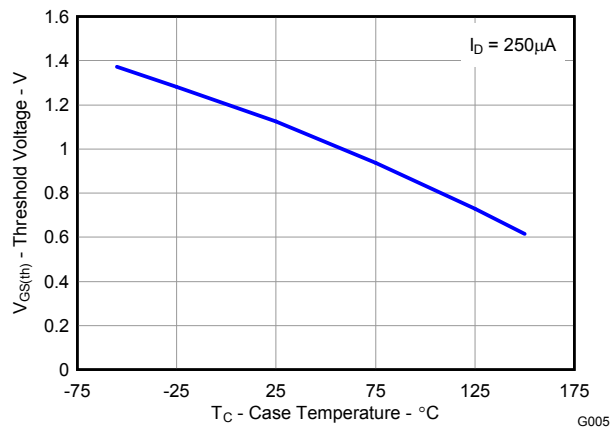
**Figure 3. Transfer Characteristics**



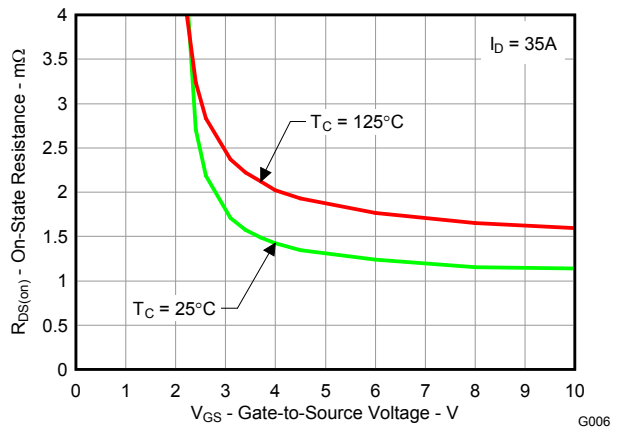
**Figure 4. Gate Charge**



**Figure 5. Capacitance**



**Figure 6. Threshold Voltage vs. Temperature**



**Figure 7. On-State Resistance vs. Gate-to-Source Voltage**

TYPICAL MOSFET CHARACTERISTICS (continued)

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

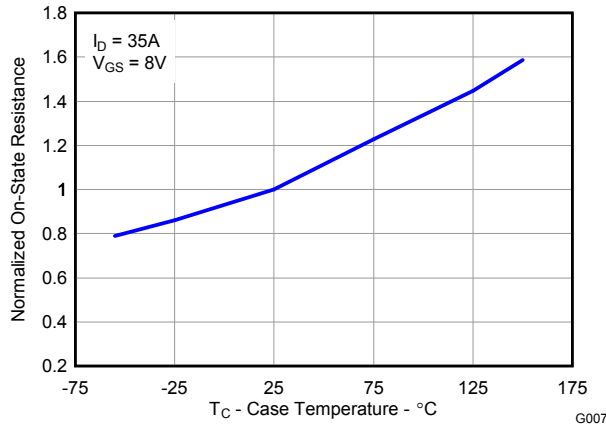


Figure 8. Normalized On-State Resistance vs. Temperature

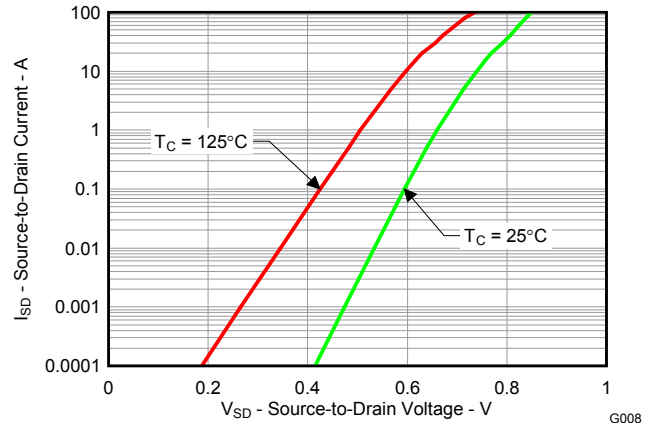


Figure 9. Typical Diode Forward Voltage

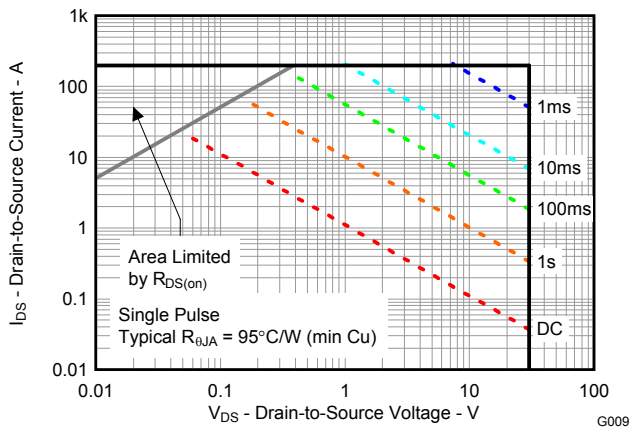


Figure 10. Maximum Safe Operating Area

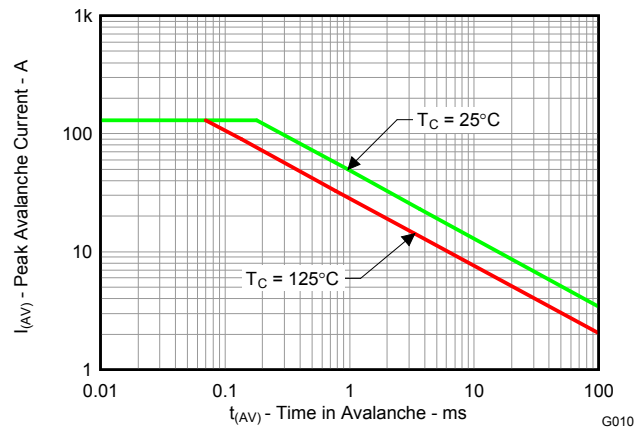


Figure 11. Single Pulse Unclamped Inductive Switching

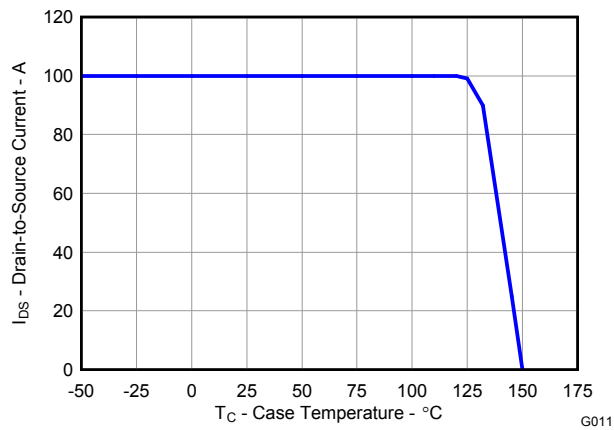
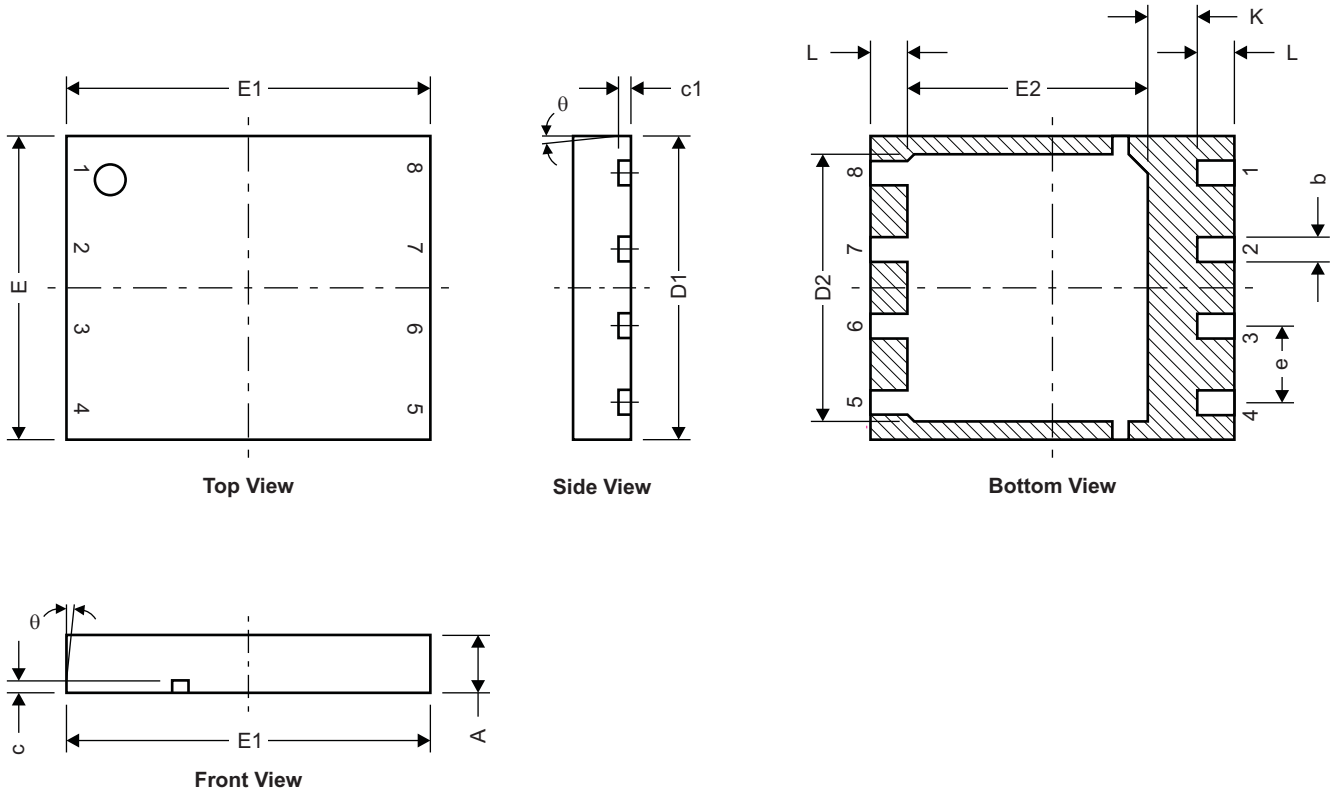


Figure 12. Maximum Drain Current vs. Temperature

**MECHANICAL DATA**

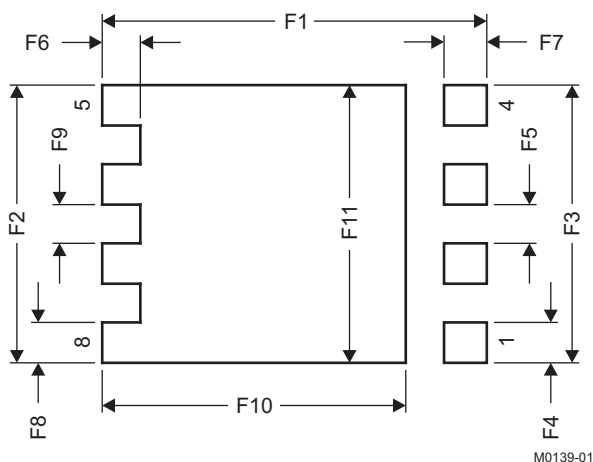
**Q5 Package Dimensions**



M0140-01

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.950	1.050	0.037	0.039
b	0.360	0.460	0.014	0.018
c	0.150	0.250	0.006	0.010
c1	0.150	0.250	0.006	0.010
D1	4.900	5.100	0.193	0.201
D2	4.320	4.520	0.170	0.178
E	4.900	5.100	0.193	0.201
E1	5.900	6.100	0.232	0.240
E2	3.920	4.12	0.154	0.162
e	1.27 TYP		0.050	
K	0.760		0.030	
L	0.510	0.710	0.020	0.028
$\theta$	0.00			

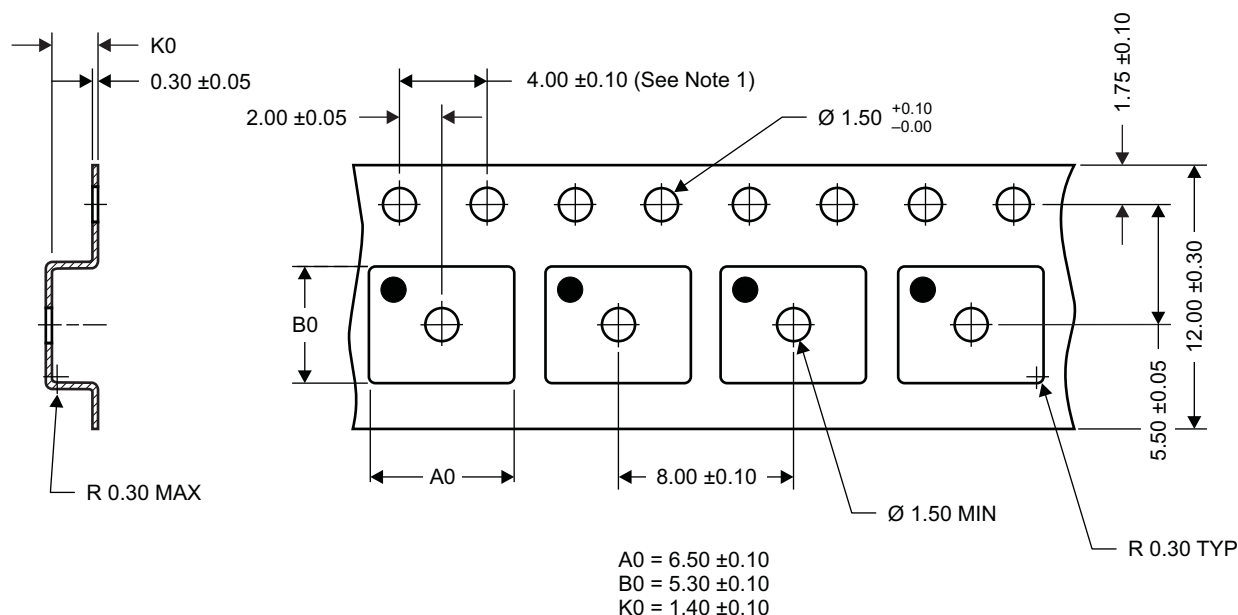
### Recommended PCB Pattern



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F1	6.205	6.305	0.244	0.248
F2	4.460	4.560	0.176	0.180
F3	4.460	4.560	0.176	0.180
F4	0.650	0.700	0.026	0.028
F5	0.620	0.670	0.024	0.026
F6	0.630	0.680	0.025	0.027
F7	0.700	0.800	0.028	0.031
F8	0.650	0.700	0.026	0.028
F9	0.620	0.670	0.024	0.026
F10	4.900	5.000	0.193	0.197
F11	4.460	4.560	0.176	0.180

For recommended circuit layout for PCB designs, see application note [SLPA005 – Reducing Ringing Through PCB Layout Techniques](#).

### Q5 Tape and Reel Information



- Notes:
1. 10-sprocket hole-pitch cumulative tolerance  $\pm 0.2$
  2. Camber not to exceed 1mm in 100mm, noncumulative over 250mm
  3. Material: black static-dissipative polystyrene
  4. All dimensions are in mm, unless otherwise specified.
  5. Thickness:  $0.30 \pm 0.05$ mm
  6. MSL1 260°C (IR and convection) PbF reflow compatible

## REVISION HISTORY

Changes from Original (March 2010) to Revision A	Page
• Deleted the Package Marking Information section .....	<a href="#">7</a>



**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">CSD17312Q5</a>	Active	Production	VSON-CLIP (DQH)   8	2500   LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD17312
CSD17312Q5.B	Active	Production	VSON-CLIP (DQH)   8	2500   LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD17312

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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