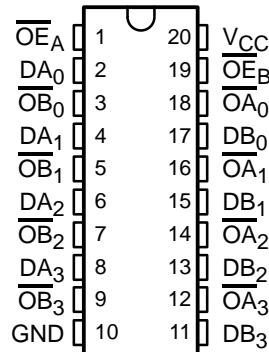
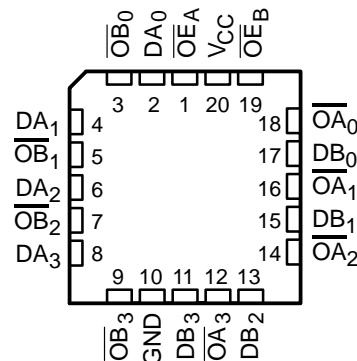


- Function, Pinout, and Drive Compatible With FCT and F Logic
- Reduced  $V_{OH}$  (Typically = 3.3 V) Versions of Equivalent FCT Functions
- Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
- Matched Rise and Fall Times
- Fully Compatible With TTL Input and Output Logic Levels
- CY54FCT240T
  - 48-mA Output Sink Current
  - 12-mA Output Source Current
- CY74FCT240T
  - 64-mA Output Sink Current
  - 32-mA Output Source Current
- 3-State Outputs

**CY54FCT240T . . . D PACKAGE  
CY74FCT240T . . . Q OR SO PACKAGE  
(TOP VIEW)**



**CY54FCT240T . . . L PACKAGE  
(TOP VIEW)**



## description

The 'FCT240T devices are octal buffers and line drivers designed to be employed as memory address drivers, clock drivers, and bus-oriented transmitters/receivers. These devices provide speed and drive capabilities equivalent to their fastest bipolar logic counterparts, while reducing power consumption. The input and output voltage levels allow direct interface with TTL, NMOS, and CMOS devices without external components.

These devices are fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**PRODUCTION DATA** information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



**CY54FCT240T, CY74FCT240T  
8-BIT BUFFERS/LINE DRIVERS  
WITH 3-STATE OUTPUTS**

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**ORDERING INFORMATION**

TA	PACKAGE <sup>†</sup>		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – SO	Tube	4.3	CY74FCT240CTSOC	FCT240C
		Tape and reel	4.3	CY74FCT240CTSOCT	
	QSOP – Q	Tape and reel	4.3	CY74FCT240CTQCT	FCT240C
	SOIC – SO	Tube	4.8	CY74FCT240ATSOC	FCT240A
		Tape and reel	4.8	CY74FCT240ATSOCT	
	QSOP – Q	Tape and reel	4.8	CY74FCT240ATQCT	FCT240A
	SOIC – SO	Tube	8	CY74FCT240TSOC	FCT240
		Tape and reel	8	CY74FCT240TSOCT	
–55°C to 125°C	QSOP – Q	Tape and reel	8	CY74FCT240TQCT	FCT240
	CDIP – D	Tube	4.7	CY54FCT240CTDMB	
	CDIP – D	Tube	5.1	CY54FCT240ATDMB	
	LCC – L	Tube	5.1	CY54FCT240ATLMB	
	CDIP – D	Tube	9	CY54FCT240TDMB	

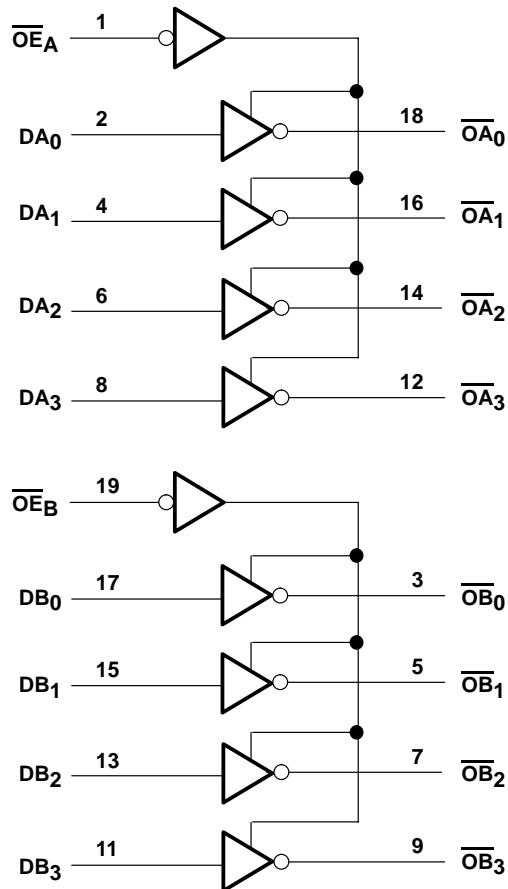
<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

**FUNCTION TABLE**

$\overline{OE}_A$	$\overline{OE}_B$	D	OUTPUT	
			$\overline{O}$	$\overline{O}$
L	L	L	H	
L	L	H	L	
H	H	X	Z	

H = High logic level, L = Low logic level,  
X = Don't care, Z = High-impedance state

## logic diagram (positive logic)



**absolute maximum rating over operating free-air temperature range (unless otherwise noted)†**

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JEDEC 51-7.

NOTE 1: The package thermal impedance is calculated in accordance with JEDEC ST-7.

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**recommended operating conditions (see Note 2)**

		CY54FCT240T			CY74FCT240T			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub>	High-level input voltage		2		2			V
V <sub>IL</sub>	Low-level input voltage			0.8			0.8	V
I <sub>OH</sub>	High-level output current			-12			-32	mA
I <sub>OL</sub>	Low-level output current			48			64	mA
T <sub>A</sub>	Operating free-air temperature	-55		125	-40		85	°C

NOTE 2: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	CY54FCT240T			CY74FCT240T			UNIT
		MIN	TYP <sup>†</sup>	MAX	MIN	TYP <sup>†</sup>	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>IN</sub> = -18 mA		-0.7	-1.2				V
	V <sub>CC</sub> = 4.75 V, I <sub>IN</sub> = -18 mA					-0.7	-1.2	
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -12 mA	2.4	3.3					V
	V <sub>CC</sub> = 4.75 V	I <sub>OH</sub> = -32 mA			2			
		I <sub>OH</sub> = -15 mA			2.4	3.3		
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 48 mA	0.3	0.55					V
	V <sub>CC</sub> = 4.75 V, I <sub>OL</sub> = 64 mA				0.3	0.55		
V <sub>hys</sub>	All inputs	0.2			0.2			V
I <sub>I</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = V <sub>CC</sub>		5					μA
	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> = V <sub>CC</sub>						5	
I <sub>IH</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 2.7 V	±1						μA
	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> = 2.7 V						±1	
I <sub>IL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0.5 V	±1						μA
	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> = 0.5 V						±1	
I <sub>OZH</sub>	V <sub>CC</sub> = 5.5 V, V <sub>OUT</sub> = 2.7 V	10						μA
	V <sub>CC</sub> = 5.25 V, V <sub>OUT</sub> = 2.7 V						10	
I <sub>OZL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>OUT</sub> = 0.5 V	-10						μA
	V <sub>CC</sub> = 5.25 V, V <sub>OUT</sub> = 0.5 V						-10	
I <sub>OS</sub> <sup>‡</sup>	V <sub>CC</sub> = 5.5 V, V <sub>OUT</sub> = 0 V	-60	-120	-225				mA
	V <sub>CC</sub> = 5.25 V, V <sub>OUT</sub> = 0 V				-60	-120	-225	
I <sub>off</sub>	V <sub>CC</sub> = 0 V, V <sub>OUT</sub> = 4.5 V	±1			±1			μA
I <sub>CC</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> ≤ 0.2 V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V	0.1	0.2					mA
	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> ≤ 0.2 V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V				0.1	0.2		
ΔI <sub>CC</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 3.4 V <sup>§</sup> , f <sub>1</sub> = 0, Outputs open	0.5	2					mA
	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> = 3.4 V <sup>§</sup> , f <sub>1</sub> = 0, Outputs open				0.5	2		
I <sub>CCD</sub> <sup>¶</sup>	V <sub>CC</sub> = 5.5 V, One input switching at 50% duty cycle, Outputs open, O <sub>E</sub> <sub>A</sub> = O <sub>E</sub> <sub>B</sub> = GND, V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V	0.06	0.12					mA/ MHz
	V <sub>CC</sub> = 5.25 V, One input switching at 50% duty cycle, Outputs open, O <sub>E</sub> <sub>A</sub> = O <sub>E</sub> <sub>B</sub> = GND, V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V				0.06	0.12		

<sup>†</sup> Typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

<sup>‡</sup> Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

<sup>§</sup> Per TTL-driven input (V<sub>IN</sub> = 3.4 V); all other inputs at V<sub>CC</sub> or GND

<sup>¶</sup> This parameter is derived for use in total power-supply calculations.

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)**

PARAMETER	TEST CONDITIONS	CY54FCT240T			CY74FCT240T			UNIT
		MIN	TYP <sup>†</sup>	MAX	MIN	TYP <sup>†</sup>	MAX	
IC <sup>#</sup>	V <sub>CC</sub> = 5.5 V, Outputs open, OE <sub>A</sub> = OE <sub>B</sub> = GND	One bit switching at f <sub>1</sub> = 10 MHz at 50% duty cycle	V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V	0.7	1.4			mA
		Eight bits switching at f <sub>1</sub> = 2.5 MHz at 50% duty cycle	V <sub>IN</sub> = 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V	1.3	2.6 <sup>  </sup>			
			V <sub>IN</sub> = 3.4 V or GND	3.3	10.6 <sup>  </sup>			
	V <sub>CC</sub> = 5.25 V, Outputs open, OE <sub>A</sub> = OE <sub>B</sub> = GND	One bit switching at f <sub>1</sub> = 10 MHz at 50% duty cycle	V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V			0.7	1.4	
		Eight bits switching at f <sub>1</sub> = 2.5 MHz at 50% duty cycle	V <sub>IN</sub> = 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V			1	2.4	
			V <sub>IN</sub> = 3.4 V or GND			1.3	2.6 <sup>  </sup>	
C <sub>i</sub>				5	10	5	10	pF
C <sub>o</sub>				9	12	9	12	pF

<sup>†</sup> Typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

<sup>#</sup> I<sub>C</sub> = I<sub>CC</sub> + ΔI<sub>CC</sub> × D<sub>H</sub> × N<sub>T</sub> + I<sub>CCD</sub> (f<sub>0</sub>/2 + f<sub>1</sub> × N<sub>1</sub>)

Where:

I<sub>C</sub> = Total supply current

I<sub>CC</sub> = Power-supply current with CMOS input levels

ΔI<sub>CC</sub> = Power-supply current for a TTL high input (V<sub>IN</sub> = 3.4 V)

D<sub>H</sub> = Duty cycle for TTL inputs high

N<sub>T</sub> = Number of TTL inputs at D<sub>H</sub>

I<sub>CCD</sub> = Dynamic current caused by an input transition pair (HLH or LHL)

f<sub>0</sub> = Clock frequency for registered devices, otherwise zero

f<sub>1</sub> = Input signal frequency

N<sub>1</sub> = Number of inputs changing at f<sub>1</sub>

All currents are in milliamperes and all frequencies are in megahertz.

<sup>||</sup> Values for these conditions are examples of the I<sub>CC</sub> formula.

**switching characteristics over operating free-air temperature range (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY54FCT240T		CY54FCT240AT		CY54FCT240CT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	D	$\bar{O}$	1.5	9	1.5	5.1	1.5	4.7	ns
$t_{PHL}$			1.5	9	1.5	5.1	1.5	4.7	
$t_{PZH}$	$\bar{OE}$	$\bar{O}$	1.5	10.5	1.5	6.5	1.5	5.7	ns
$t_{PZL}$			1.5	10.5	1.5	6.5	1.5	5.7	
$t_{PHZ}$	$\bar{OE}$	$\bar{O}$	1.5	10	1.5	5.9	1.5	4.6	ns
$t_{PLZ}$			1.5	10	1.5	5.9	1.5	4.6	

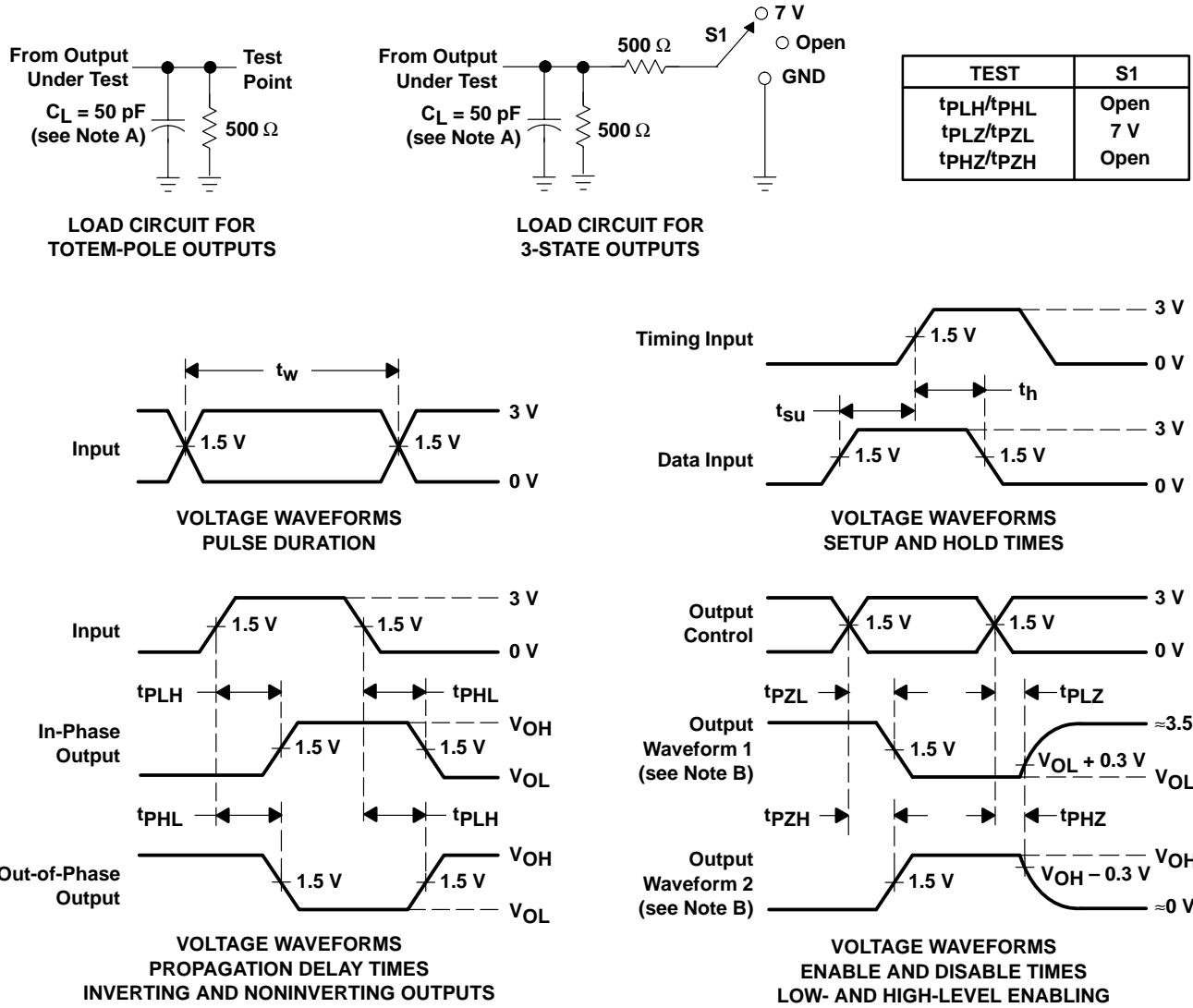
**switching characteristics over operating free-air temperature range (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY74FCT240T		CY74FCT240AT		CY74FCT240CT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	D	$\bar{O}$	1.5	8	1.5	4.8	1.5	4.3	ns
$t_{PHL}$			1.5	8	1.5	4.8	1.5	4.3	
$t_{PZH}$	$\bar{OE}$	$\bar{O}$	1.5	10	1.5	6.2	1.5	5	ns
$t_{PZL}$			1.5	10	1.5	6.2	1.5	5	
$t_{PHZ}$	$\bar{OE}$	$\bar{O}$	1.5	9.5	1.5	5.6	1.5	4.5	ns
$t_{PLZ}$			1.5	9.5	1.5	5.6	1.5	4.5	

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**PARAMETER MEASUREMENT INFORMATION**



NOTES:

- $C_L$  includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9221301MRA	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9221301MR A
5962-9221303M2A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9221303M2A CY54FCT 240ATLMB
5962-9221303MRA	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9221303MR A CY54FCT240ATDM B
5962-9221305MRA	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9221305MR A
CY54FCT240ATDMB	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9221303MR A CY54FCT240ATDM B
CY54FCT240ATLMB	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9221303M2A CY54FCT 240ATLMB
CY74FCT240ATQCT	Active	Production	SSOP (DBQ)   20	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT240A
CY74FCT240ATQCT.B	Active	Production	SSOP (DBQ)   20	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT240A
CY74FCT240ATSOC	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT240A
CY74FCT240ATSOC.B	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT240A
CY74FCT240ATSOCT	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT240A
CY74FCT240ATSOCT.B	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT240A
CY74FCT240TQCT	Active	Production	SSOP (DBQ)   20	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT240
CY74FCT240TQCT.B	Active	Production	SSOP (DBQ)   20	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT240
CY74FCT240TSOC	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT240
CY74FCT240TSOC.B	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT240
CY74FCT240TSOCT	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT240
CY74FCT240TSOCT.B	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT240
CY74FCT240TSOCTG4	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT240

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CY74FCT240TSOCTG4.B	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT240

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

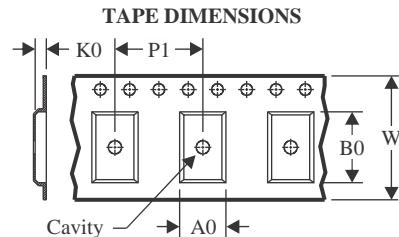
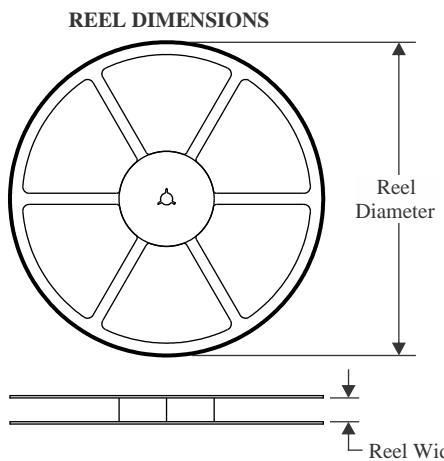
<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

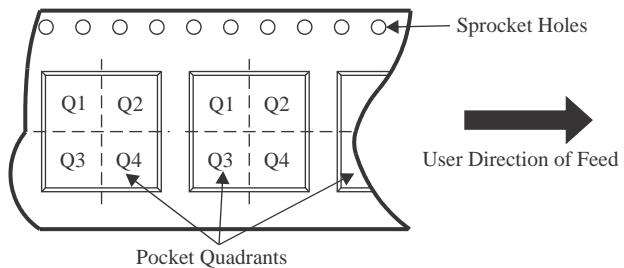
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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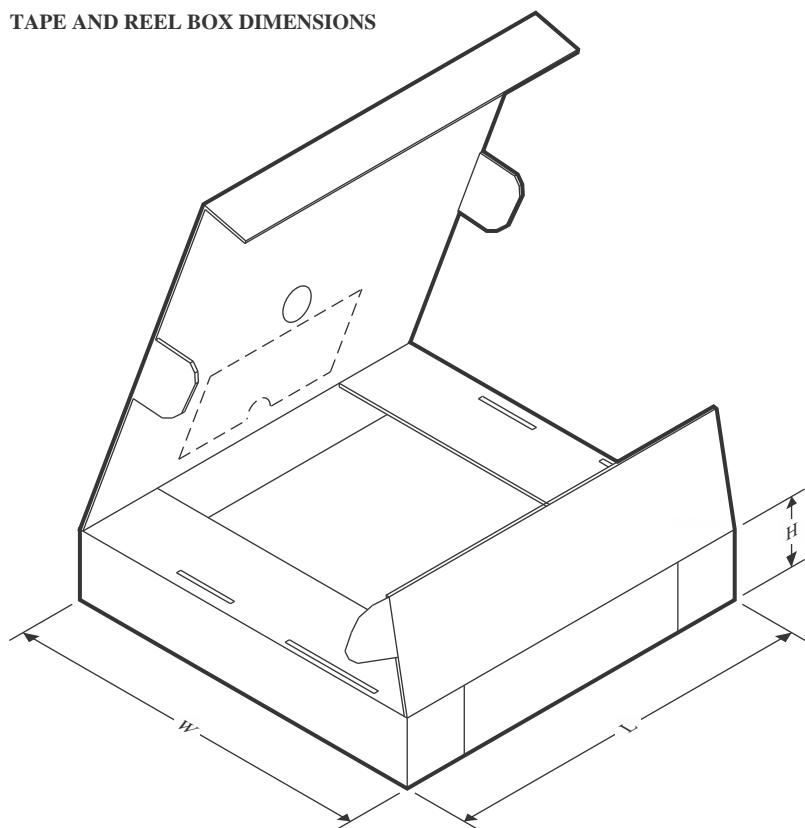
**TAPE AND REEL INFORMATION**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


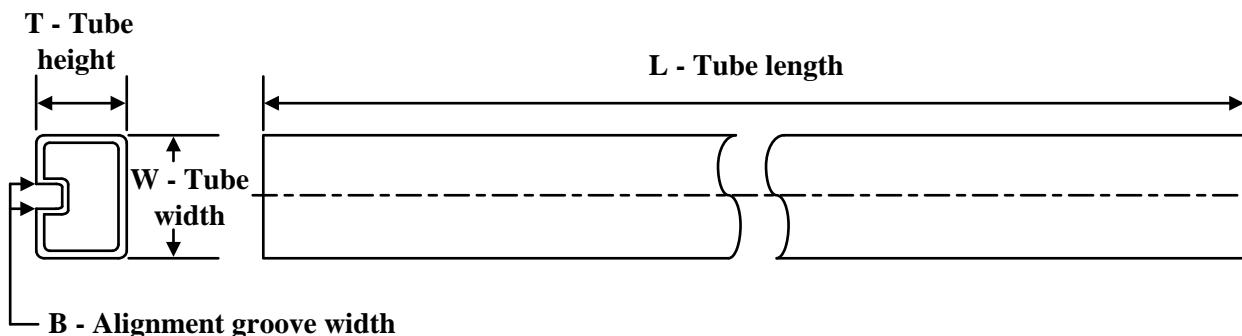
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CY74FCT240ATQCT	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT240ATSOCT	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CY74FCT240TQCT	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT240TSOCT	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CY74FCT240TSOCTG4	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CY74FCT240ATQCT	SSOP	DBQ	20	2500	353.0	353.0	32.0
CY74FCT240ATSOCT	SOIC	DW	20	2000	356.0	356.0	45.0
CY74FCT240TQCT	SSOP	DBQ	20	2500	353.0	353.0	32.0
CY74FCT240TSOCT	SOIC	DW	20	2000	356.0	356.0	45.0
CY74FCT240TSOCTG4	SOIC	DW	20	2000	356.0	356.0	45.0

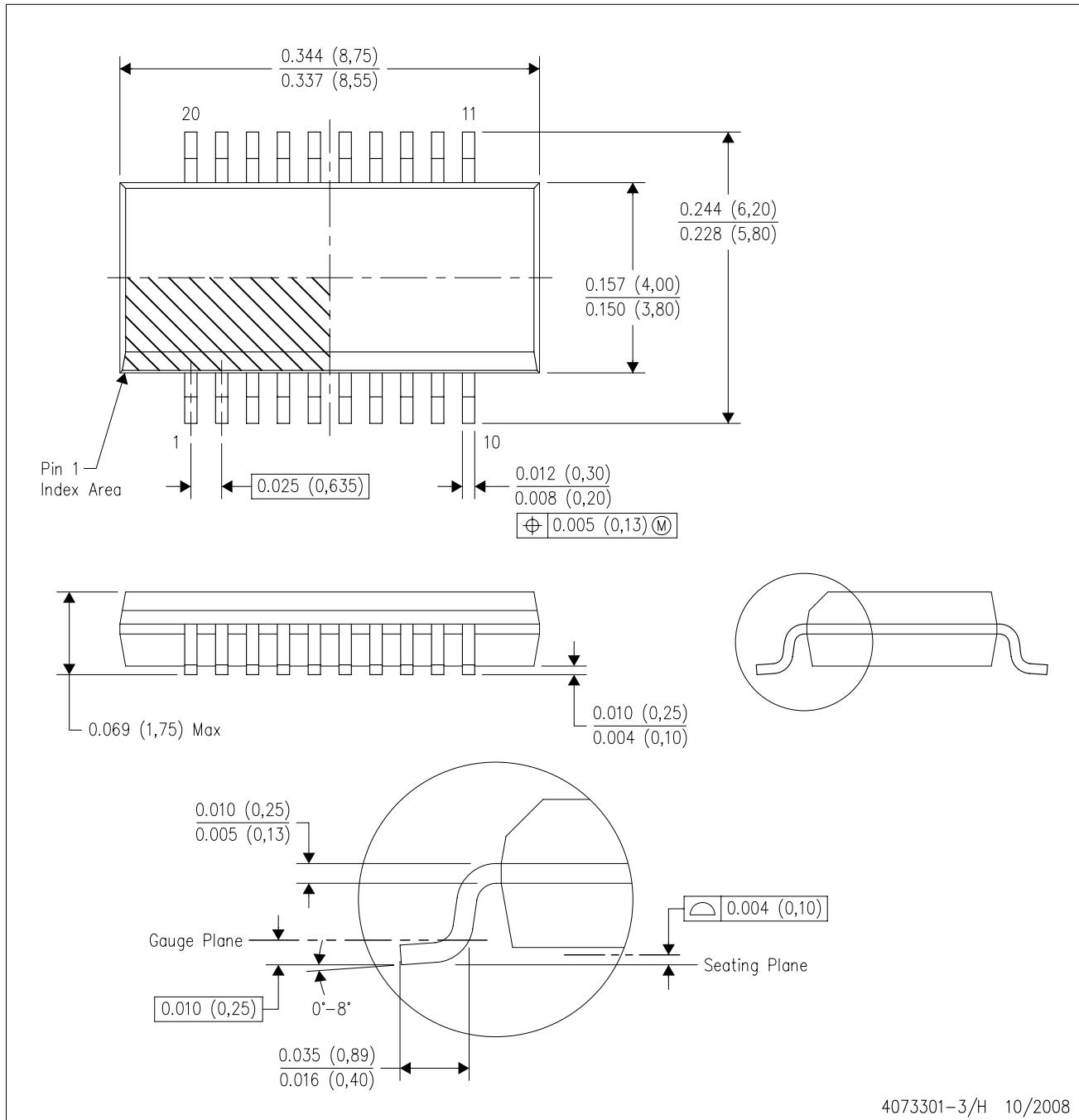
**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T ( $\mu$ m)	B (mm)
5962-9221303M2A	FK	LCCC	20	55	506.98	12.06	2030	NA
CY54FCT240ATLMB	FK	LCCC	20	55	506.98	12.06	2030	NA
CY74FCT240ATSOC	DW	SOIC	20	25	507	12.83	5080	6.6
CY74FCT240ATSOC.B	DW	SOIC	20	25	507	12.83	5080	6.6
CY74FCT240TSOC	DW	SOIC	20	25	507	12.83	5080	6.6
CY74FCT240TSOC.B	DW	SOIC	20	25	507	12.83	5080	6.6

DBQ (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



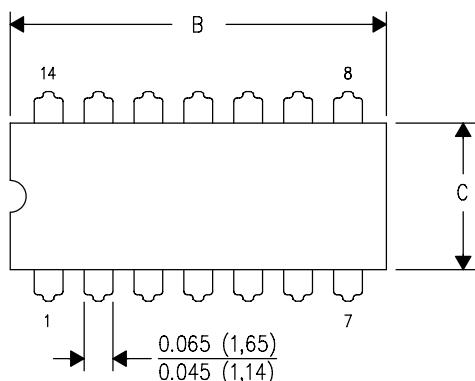
NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
- Falls within JEDEC MO-137 variation AD.

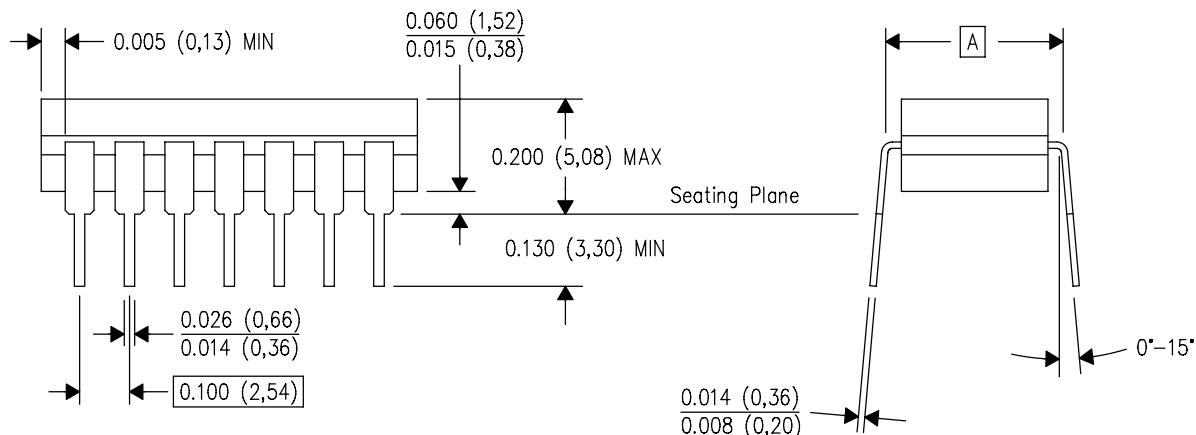
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. This package is hermetically sealed with a ceramic lid using glass frit.  
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.  
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

# GENERIC PACKAGE VIEW

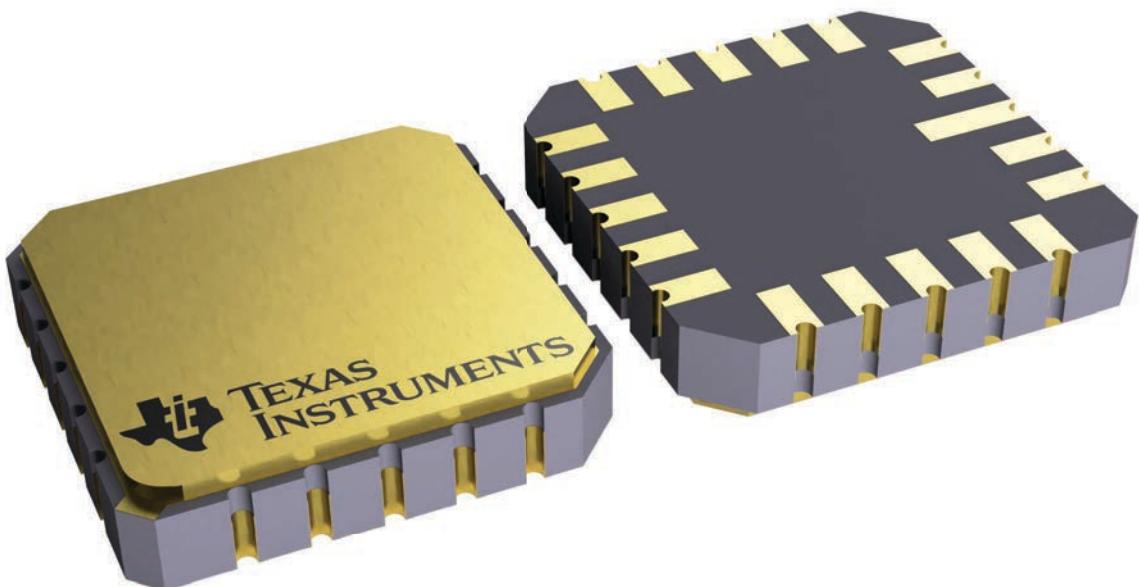
**FK 20**

**LCCC - 2.03 mm max height**

**8.89 x 8.89, 1.27 mm pitch**

**LEADLESS CERAMIC CHIP CARRIER**

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\

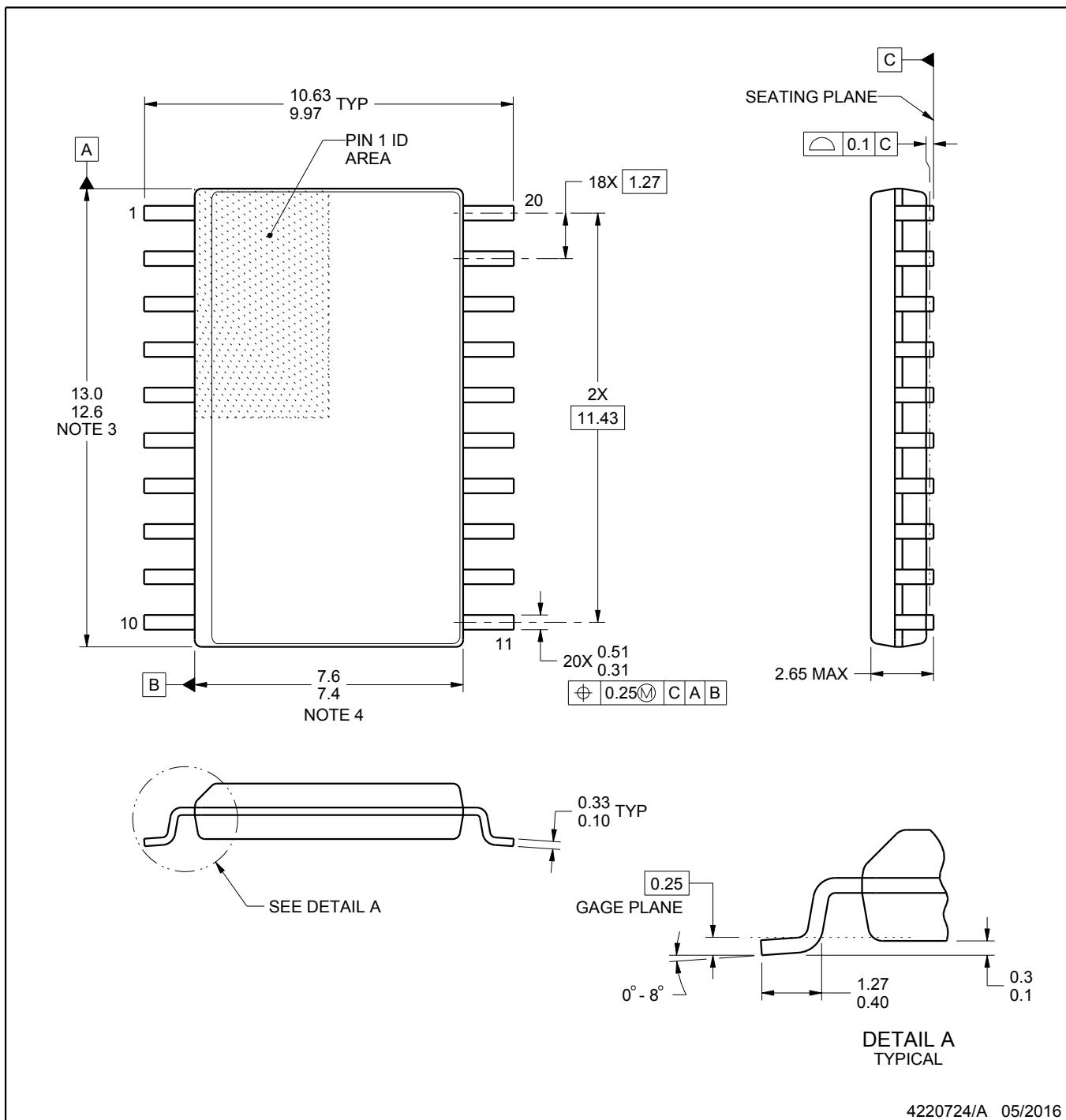
# PACKAGE OUTLINE

DW0020A



SOIC - 2.65 mm max height

SOIC



## NOTES:

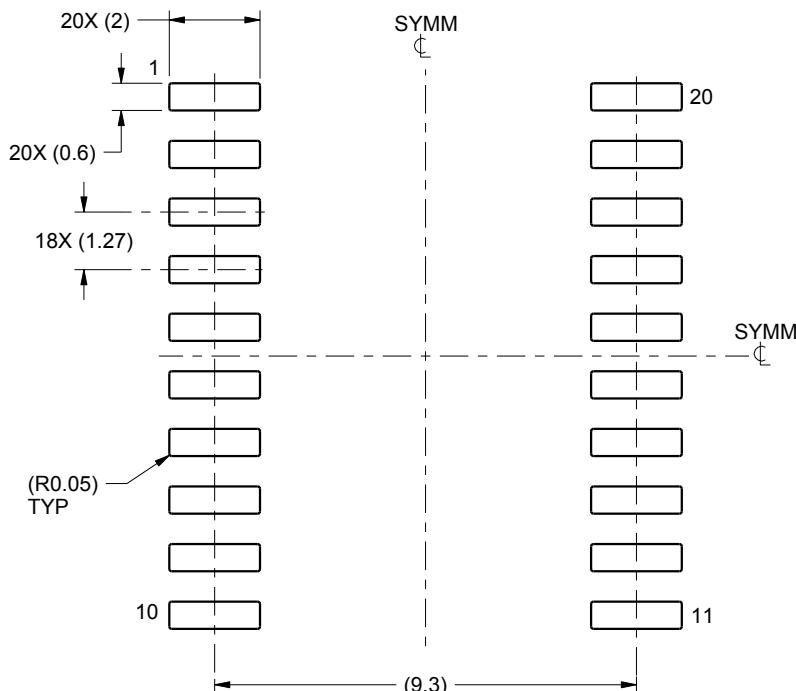
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

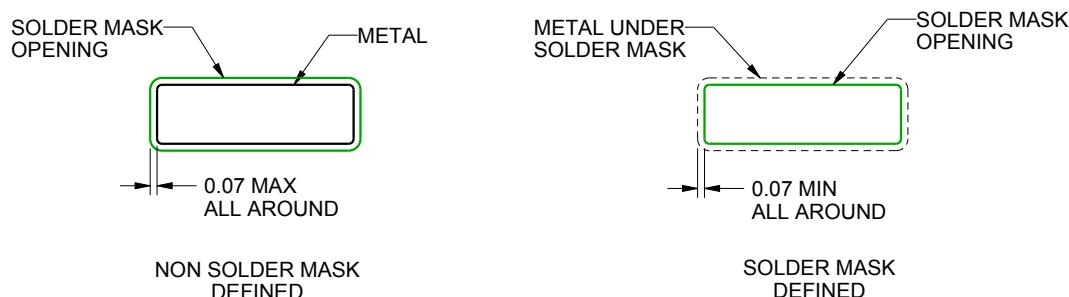
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

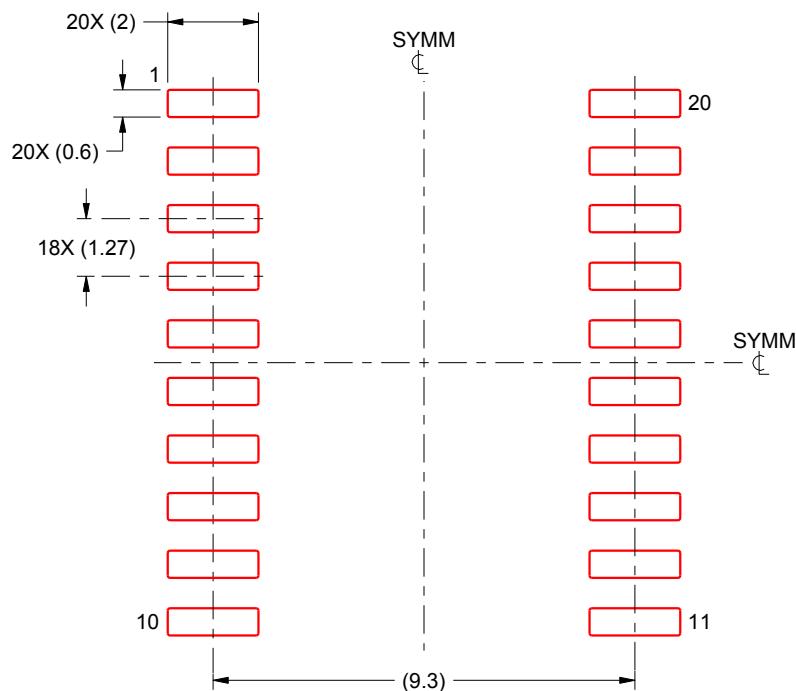
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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