DAC539G2-Q1 汎用入力 (GPI) からパルス幅変調 (PWM) への変換向け、車載用 10 ビット・スマート D/A コンバータ、I²C または SPI 自動検出機能付き

1 特長

- 車載アプリケーション用に AEC-Q100 認定済み:
  - 温度グレード 1:-40℃～+125℃、T_A
- トリプル汎用入力
- のこぎり波または三角波を使用した PWM 出力
- 10 ビットの GPI から電圧への変換出力
  - 1 LSB の DNL
- I²C と SPI を自動的に検出
  - V_{IH}:1.62V (V_{DD} = 5.5V の場合)
- MODE ピンにより、プログラミング・モードとスタンドアロン・モードを選択
- ユーザーがプログラム可能な不揮発性メモリ (NVM)
- 内部、外部、VDD のリファレンス電圧
- PWM 周波数誤差補正のオプション
- 幅広い動作範囲
  - 電源:1.8V～5.5V
- 超小型パッケージ:16 ピン WQFN (3mm × 3mm)

2 アプリケーション

- リア・ライト
- 状況監視モジュール
- 有線制御

3 概要

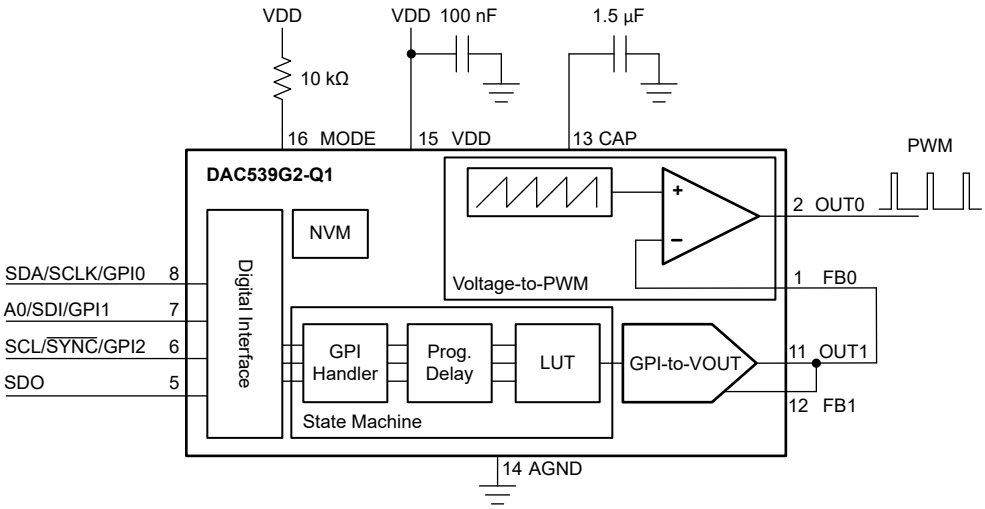
DAC539G2-Q1 は、アプリケーション固有のルックアップ・テーブル (LUT) をベースにする GPI から PWM へのコンバータです。このデバイスには、10 ビットの GPI から電圧への出力コンバータと、電圧から PWM へのコンバータが搭載されています。これらの回路はどちらも、外部から接続して GPI から PWM へのコンバータを作成できます。3 つの GPI は、電圧出力を表す 8 つの 10 ビット・デジタル・コードにマップされます。これらの入力のグリッチを除去するため、GPI の遅延をプログラムできます。ルックアップ・テーブルの値は、I²C または SPI を使用してプログラムされ、NVM に保存されます。GPI は I²C や SPI と多重化されます。電圧から PWM へのコンバータは、1 つの入力を持つコンパレータを、プログラム可能なのこぎり波または三角波として使用し、もう 1 つの入力を外部電圧入力として使用します。

このデバイスは、I²C と SPI を自動的に検出し、内部リファレンスを備えています。DAC539G2-Q1 は、車載用のストップ / ターン・ライトや類似の産業用アプリケーションで、フォルト通信を行うための優れた選択肢です。

パッケージ情報

部品番号	パッケージ (1)	パッケージ・サイズ (2)
DAC539G2-Q1	RTE (WQFN、16)	3.00mm × 3.00mm
DAC539G2W-Q1	RTE (WQFN、16、ウェッタブル・フランク)	

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ・サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



機能ブロック図

Table of Contents

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (January 2023) to Revision A (September 2023)	Page
• ウェッタブル・フランク RTE (WQFN、16) パッケージを追加	1

5 Pin Configuration and Functions

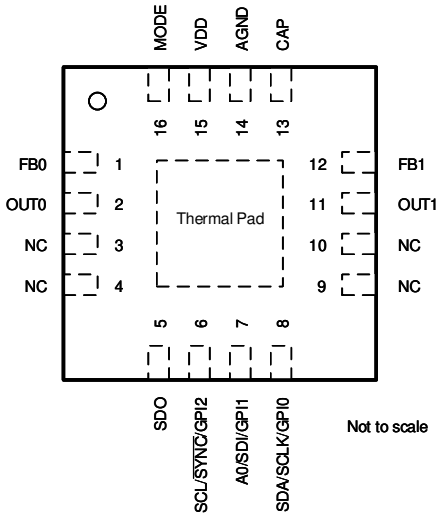


図 5-1. RTE Package, 16-pin WQFN (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	FB0	Input	Comparator input.
2	OUT0	Output	PWM output from comparator.
3	NC	—	Leave this pin unconnected.
4	NC	—	Leave this pin unconnected.
5	SDO	Output	Configuration mode (MODE pin low): SPI serial data output. Connect the pin to the I/O voltage with an external pullup resistor. Standalone mode (MODE pin high): Not connected.
6	SCL/$\overline{\text{SYNC}}$/GPI2	Output	Configuration mode (MODE pin low): I^2C serial interface clock or SPI chip select input. In the SPI chip select function, this pin must be connected to the I/O voltage using an external pullup resistor. Standalone mode (MODE pin high): General-purpose input 2.
7	A0/SDI/GPI1	Input	Configuration mode (MODE pin low): Address configuration input for I^2C or serial data input for SPI. In A0 function, connect this pin to VDD, AGND, SDA, or SCL for address configuration. In SDI function, this pin need not be pulled up or pulled down. Standalone mode (MODE pin high): General-purpose input 1.
8	SDA/SCLK/GPI0	Input/ Output	Configuration mode (MODE pin low): Bidirectional I^2C serial data bus or SPI clock input. In the I^2C mode, connect this pin to the I/O voltage using an external pullup resistor. Standalone mode (MODE pin high): General-purpose input 0.
9	NC	—	Leave this pin unconnected.
10	NC	—	Leave this pin unconnected.
11	OUT1	Output	Voltage output for DAC.
12	FB1	Input	Voltage feedback input for the DAC output amplifier. Connect this pin to OUT1 for closed-loop voltage output.
13	CAP	Power	External bypass capacitor for the internal LDO. Connect a capacitor (approximately 1.5 µF) between CAP and AGND.
14	AGND	Ground	Ground reference point for all circuitry on the device.
15	VDD	Power	Supply voltage: 1.8 V to 5.5 V.
16	MODE	Input	Interface selection and external reference input. Connect a capacitor (approximately 0.1 µF) between MODE and AGND. Use a pullup resistor to VDD when external reference is not used. Do not ramp up this pin before VDD. If external reference is used, make sure the reference ramps up after VDD.

表 5-1. Pin Functions (続き)

PIN		TYPE	DESCRIPTION
NO.	NAME		
—	Thermal Pad	Ground	Connect the thermal pad to AGND.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD}	Supply voltage, V_{DD} to AGND	–0.3	6	V
	Digital inputs to AGND	–0.3	V_{DD} + 0.3	V
	V_{FBX} to AGND	–0.3	V_{DD} + 0.3	V
	V_{OUTX} to AGND	–0.3	V_{DD} + 0.3	V
V_{REF}	External reference, V_{REF} to AGND	–0.3	V_{DD} + 0.3	V
	Current into any pin except the OUTx, VDD, and AGND pins	–10	10	mA
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD classification level 2		±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD classification level C4B	Corner pins (1, 4, 5, 8, 9, 12, 13, and 16)	±750	
			All pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Positive supply voltage to ground (AGND)	1.7		5.5	V
V_{REF}	External reference to ground (AGND)	1.7		V_{DD}	V
V_{IH}	Digital input high voltage, 1.7 V < V_{DD} ≤ 5.5 V	1.62			V
V_{IL}	Digital input low voltage			0.4	V
C_{CAP}	External capacitor on CAP pin	0.5		15	µF
T_A	Ambient temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		DAC539G2-Q1 RTE (WQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	24.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	24.1	°C/W

THERMAL METRIC(1)		DAC539G2-Q1 RTE (WQFN) 16 PINS	UNIT
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	8.7	°C/W

(1) For information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics application report.*

6.5 Electrical Characteristics: Voltage Output

minimum and maximum specifications at T_A = –40°C to +125°C and typical specifications at T_A = 25°C, 1.7 V ≤ V_{DD} ≤ 5.5 V, DAC reference tied to VDD, gain = 1 ×, DAC output pin (OUT) loaded with resistive load (R_L = 5 kΩ to AGND) and capacitive load (C_L = 200 pF to AGND), and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE						
	Resolution		10			Bits
INL	Integral nonlinearity(1)		–1.25		1.25	LSB
DNL	Differential nonlinearity(1)		–1		1	LSB
	Zero-code error(4)	Code 0d into DAC, external reference, V_{DD} = 5.5 V		6	12	mV
	Zero-code error(4)	Code 0d into DAC, internal V_{REF}, gain = 4 ×, V_{DD} = 5.5 V		6	15	mV
	Zero-code error temperature coefficient(4)			±10		µV/°C
	Offset error(4)	1.7 V ≤ V_{DD} < 2.7 V, V_{FB} pin shorted to V_{OUT}, DAC code: 8d	–0.75	0.3	0.75	%FSR
		2.7 V ≤ V_{DD} ≤ 5.5 V, V_{FB} pin shorted to V_{OUT}, DAC code: 8d	–0.5	0.25	0.5	
	Offset-error temperature coefficient(4)	V_{FB} pin shorted to V_{OUT}, DAC code: 8d		±0.0003		%FSR/°C
	Gain error(4)	Between end-point codes: 8d and 1016d	–0.5	0.25	0.5	%FSR
	Gain-error temperature coefficient(4)	Between end-point codes: 8d and 1016d		±0.0008		%FSR/°C
	Full-scale error(4)	1.7 V ≤ V_{DD} < 2.7 V, DAC at full-scale	–1		1	%FSR
	Full-scale error(4)	2.7 V ≤ V_{DD} ≤ 5.5 V, DAC at full-scale	–0.6		0.6	%FSR
	Full-scale-error temperature coefficient(4)	DAC at full-scale		±0.0008		%FSR/°C
OUTPUT						
	Output voltage	Reference tied to V_{DD}	0		V_{DD}	V
C_L	Capacitive load(2)	R_L = infinite, phase margin = 30°			200	pF
		Phase margin = 30°			1000	
	Load regulation	DAC at midscale, –10 mA ≤ I_{OUT} ≤ 10 mA, V_{DD} = 5.5 V, V_{REF} = 5.5 V, V_{REF} not shorted to V_{DD}		0.007		mV/mA
	Short-circuit current	V_{DD} = 1.7 V, full-scale output shorted to AGND or zero-scale output shorted to V_{DD}		15		mA
		V_{DD} = 2.7 V, full-scale output shorted to AGND or zero-scale output shorted to V_{DD}		50		
		V_{DD} = 5.5 V, full-scale output shorted to AGND or zero-scale output shorted to V_{DD}		60		
	Output-voltage headroom(2)	To V_{DD} (DAC output unloaded, internal reference = 1.21 V), V_{DD} ≥ 1.21 V × gain + 0.2 V	0.2			V
		To V_{DD} and to AGND (DAC output unloaded, external reference at V_{DD} (gain = 1 ×), the V_{REF} pin is not shorted to V_{DD})	0.8			%FSR
		To V_{DD} and to AGND (I_{LOAD} = 10 mA at V_{DD} = 5.5 V, I_{LOAD} = 3 mA at V_{DD} = 2.7 V, I_{LOAD} = 1 mA at V_{DD} = 1.8 V), external reference at V_{DD} (gain = 1 ×), the V_{REF} pin is not shorted to V_{DD})	10			%FSR

6.5 Electrical Characteristics: Voltage Output (続き)

minimum and maximum specifications at T_A = –40°C to +125°C and typical specifications at T_A = 25°C, 1.7 V ≤ V_{DD} ≤ 5.5 V, DAC reference tied to VDD, gain = 1 ×, DAC output pin (OUT) loaded with resistive load (R_L = 5 kΩ to AGND) and capacitive load (C_L = 200 pF to AGND), and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	V_{OUT} dc output impedance	DAC output enabled and DAC code = midscale, V_{DD} = 5.5 V, external reference mode		0.007		Ω
		DAC output enabled and DAC code = 8d, V_{DD} = 5.5 V, external reference mode		0.25		
		DAC output enabled and DAC code = 1016d, V_{DD} = 5.5 V, external reference mode		0.25		
Z_O	V_{FB} dc output impedance(3)	DAC output enabled, internal reference (gain = 1.5 × or 2 ×)	400	500	600	kΩ
		DAC output enabled, internal reference (gain = 3 × or 4 ×)	325	400	485	
	Power supply rejection ratio (dc)	Internal V_{REF}, gain = 2 ×, DAC at midscale, V_{DD} = 5 V ±10%		0.25		mV/V
DYNAMIC PERFORMANCE						
t_{sett}	Output voltage settling time	1/4 to 3/4 scale and 3/4 to 1/4 scale settling to 10%FSR, V_{DD} = 5.5 V		20		µs
		1/4 to 3/4 scale and 3/4 to 1/4 scale settling to 10%FSR, V_{DD} = 5.5 V, internal V_{REF}, gain = 4 ×		25		
	Slew rate	V_{DD} = 5.5 V		0.3		V/µs
	Power-on glitch magnitude	At start-up (DAC output disabled)		75		mV
		At start-up (DAC output disabled), R_L = 100 kΩ		200		
	Output-enable glitch magnitude	DAC output disabled to enabled (DAC registers at zero scale), R_L = 100 kΩ		250		mV
V_n	Output noise voltage (peak to peak)	f = 0.1 Hz to 10 Hz, DAC at midscale, V_{DD} = 5.5 V		50		μV_{PP}
		Internal V_{REF}, gain = 4 ×, f = 0.1 Hz to 10 Hz, DAC at midscale, V_{DD} = 5.5 V		90		
	Output noise density	f = 1 kHz, DAC at midscale, V_{DD} = 5.5 V		0.35		µV/√Hz
		Internal V_{REF}, gain = 4 ×, f = 1 kHz, DAC at midscale, V_{DD} = 5.5 V		0.9		
	Power supply rejection ratio (ac)(3)	Internal V_{REF}, gain = 4 ×, 200-mV 50-Hz or 60-Hz sine wave superimposed on power supply voltage, DAC at midscale		−68		dB
	Code change glitch impulse	±1 LSB change around midscale (including feedthrough)		10		nV-s
	Code change glitch impulse magnitude	±1 LSB change around midscale (including feedthrough)		15		mV
POWER						
I_{DD}	Current flowing into VDD(4) (5)	Normal operation, DACs at full scale, digital pins static, external reference at V_{DD} but the V_{REF} pin is not shorted to V_{DD}		150		µA/ch

(1) Measured with DAC output unloaded. For external reference and internal reference V_{DD} ≥ 1.21 × gain + 0.2 V, between end-point codes: 8d and 1016d.
(2) Specified by design and characterization, not production tested.
(3) Specified with 200-mV headroom with respect to reference value when internal reference is used.
(4) Measured with DAC output unloaded.
(5) The total power consumption is calculated by I_{DD} × (total number of channels powered on) + (sleep-mode current).

6.6 Electrical Characteristics: Comparator Mode

minimum and maximum specifications at T_A = –40°C to +125°C and typical specifications at T_A = 25°C, 1.7 V ≤ V_{DD} ≤ 5.5 V, DAC reference tied to VDD, gain = 1 × in voltage output mode, DAC output pin (OUT) loaded with resistive load (R_L = 5 kΩ to AGND) and capacitive load (C_L = 200 pF to AGND), and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE						
	Offset error(1) (2)	1.7 V ≤ V_{DD} ≤ 5.5 V; DAC at midscale, comparator input at Hi-Z, and DAC operating with external reference	–7.5	0	7.5	mV
	Offset error time drift(1)	V_{DD} = 5.5 V, T_A = 125°C, FB in Hi-Z mode, DAC at full scale and V_{FB} at 0 V or DAC at zero scale and V_{FB} at 1.84 V, drift specified for 10 years of continuous operation		4		mV
OUTPUT						
	Input voltage	V_{REF} connected to V_{DD}, V_{FB} resistor network connected to ground	0		V_{DD}	V
		V_{REF} connected to V_{DD}, V_{FB} resistor network disconnected from ground	0		V_{DD} (1/3 – 1/100)	
V_{OL}	Logic low output voltage	I_{LOAD} = 100 µA, output in open-drain mode		0.1		V
DYNAMIC PERFORMANCE						
t_{resp}	Output response time	DAC at midscale with 10-bit resolution, FB input at Hi-Z, and transition step at FB node is (V_{DAC} – 2 LSB) to (V_{DAC} + 2 LSB), transition time measured between 10% and 90% of output, output current of 100 µA, comparator output configured in push-pull mode, load capacitor at DAC output is 25 pF		10		µs

(1) Specified by design and characterization, not production tested.
(2) This specification does not include the total unadjusted error (TUE) of the DAC.

6.7 Electrical Characteristics: General

minimum and maximum specifications at T_A = –40°C to +125°C and typical specifications at T_A = 25°C, 1.7 V ≤ V_{DD} ≤ 5.5 V, DAC reference tied to VDD, gain = 1 × in voltage output mode, DAC output pin (OUT) loaded with resistive load (R_L = 5 kΩ to AGND) in voltage-output mode and capacitive load (C_L = 200 pF to AGND), and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL REFERENCE						
	Initial accuracy	T_A = 25°C	1.1979	1.212	1.224	V
	Reference output temperature coefficient(1) (2)				60	ppm/°C
EXTERNAL REFERENCE						
	External reference input range		1.7		V_{DD}	V
	V_{REF} input impedance(1) (3)			192		kΩ-ch
EEPROM						
	Endurance(1)	–40°C ≤ T_A ≤ +85°C		20000		Cycles
		T_A = 125°C		1000		
	Data retention(1)	T_A = 25°C		50		Years
	EEPROM programming write cycle time(1)				200	ms
	Device boot-up time(1)	Time taken from power valid (V_{DD} ≥ 1.7 V) to output valid state (output state as programmed in EEPROM), 0.5-µF capacitor on the CAP pin		5		ms
DIGITAL INPUTS						
	Digital feedthrough	Voltage output mode, DAC output static at midscale, fast mode plus, SCL toggling		20		nV-s
	Pin capacitance	Per pin		10		pF
POWER-DOWN MODE 2						
I_{DD}	Current flowing into VDD	DAC in sleep mode, internal reference powered down, external reference at 5.5 V			28	µA
	Current flowing into VDD(1)	DAC in sleep mode, internal reference enabled, additional current through internal reference		10		
		DAC channels enabled, internal reference enabled, additional current through internal reference per DAC channel in voltage-output mode		12.5		
HIGH-IMPEDANCE OUTPUT						
I_{LEAK}	Current flowing into V_{OUTX} and V_{FBX}	DAC in Hi-Z output mode, 1.7 V ≤ V_{DD} ≤ 5.5 V		10		nA
		V_{DD} = 0 V, V_{OUT} ≤ 1.5 V, decoupling capacitor between V_{DD} and AGND = 0.1 µF		200		
		V_{DD} = 0 V, 1.5 V < V_{OUT} ≤ 5.5 V, decoupling capacitor between V_{DD} and AGND = 0.1 µF		500		
		100 kΩ between V_{DD} and AGND, V_{OUT} ≤ 1.25 V, series resistance of 10 kΩ at OUT pin		±2		µA

(1) Specified by design and characterization, not production tested.
(2) Measured at –40°C and +125°C and calculated the slope.
(3) Impedances for the DAC channels are connected in parallel.

6.8 Timing Requirements: I²C Standard Mode

all input signals are timed from VIL to 70% of $V_{pull-up}$, 1.7 V ≤ V_{DD} ≤ 5.5 V, –40°C ≤ T_A ≤ +125°C, and 1.7 V ≤ $V_{pull-up}$ ≤ V_{DD}

		MIN	NOM	MAX	UNIT
f_{SCLK}	SCL frequency			100	kHz
t_{BUF}	Bus free time between stop and start conditions	4.7			µs
t_{HDSTA}	Hold time after repeated start	4			µs
t_{SUSTA}	Repeated start setup time	4.7			µs
t_{SUSTO}	Stop condition setup time	4			µs
t_{HDDAT}	Data hold time	0			ns
t_{SUDAT}	Data setup time	250			ns
t_{LOW}	SCL clock low period	4700			ns
t_{HIGH}	SCL clock high period	4000			ns
t_F	Clock and data fall time			300	ns
t_R	Clock and data rise time			1000	ns
t_{VDDAT}	Data valid time, R = 360 Ω, C_{trace} = 23 pF, C_{probe} = 10 pF			3.45	µs
t_{VDACK}	Data valid acknowledge time, R = 360 Ω, C_{trace} = 23 pF, C_{probe} = 10 pF			3.45	µs

6.9 Timing Requirements: I²C Fast Mode

all input signals are timed from VIL to 70% of $V_{pull-up}$, 1.7 V ≤ V_{DD} ≤ 5.5 V, –40°C ≤ T_A ≤ +125°C, and 1.7 V ≤ $V_{pull-up}$ ≤ V_{DD}

		MIN	NOM	MAX	UNIT
f_{SCLK}	SCL frequency			400	kHz
t_{BUF}	Bus free time between stop and start conditions	1.3			µs
t_{HDSTA}	Hold time after repeated start	0.6			µs
t_{SUSTA}	Repeated start setup time	0.6			µs
t_{SUSTO}	Stop condition setup time	0.6			µs
t_{HDDAT}	Data hold time	0			ns
t_{SUDAT}	Data setup time	100			ns
t_{LOW}	SCL clock low period	1300			ns
t_{HIGH}	SCL clock high period	600			ns
t_F	Clock and data fall time			300	ns
t_R	Clock and data rise time			300	ns
t_{VDDAT}	Data valid time, R = 360 Ω, C_{trace} = 23 pF, C_{probe} = 10 pF			0.9	µs
t_{VDACK}	Data valid acknowledge time, R = 360 Ω, C_{trace} = 23 pF, C_{probe} = 10 pF			0.9	µs

6.10 Timing Requirements: I²C Fast Mode Plus

all input signals are timed from VIL to 70% of $V_{pull-up}$, 1.7 V ≤ V_{DD} ≤ 5.5 V, –40°C ≤ T_A ≤ +125°C, and 1.7 V ≤ $V_{pull-up}$ ≤ V_{DD}

		MIN	NOM	MAX	UNIT
f_{SCLK}	SCL frequency			1	MHz
t_{BUF}	Bus free time between stop and start conditions	0.5			µs
t_{HDSTA}	Hold time after repeated start	0.26			µs
t_{SUSTA}	Repeated start setup time	0.26			µs
t_{SUSTO}	Stop condition setup time	0.26			µs
t_{HDDAT}	Data hold time	0			ns
t_{SUDAT}	Data setup time	50			ns
t_{LOW}	SCL clock low period	0.5			µs
t_{HIGH}	SCL clock high period	0.26			µs
t_F	Clock and data fall time			120	ns
t_R	Clock and data rise time			120	ns
t_{VDDAT}	Data valid time, R = 360 Ω, C_{trace} = 23 pF, C_{probe} = 10 pF			0.45	µs
t_{VDACK}	Data valid acknowledge time, R = 360 Ω, C_{trace} = 23 pF, C_{probe} = 10 pF			0.45	µs

6.11 Timing Requirements: SPI Write Operation

all input signals are specified with $t_r = t_f$ = 1 V/ns (10% to 90% of V_{IO}) and timed from a voltage level of (VIL + VIH) / 2, 1.7 V ≤ V_{IO} ≤ 5.5 V, 1.7 V ≤ V_{DD} ≤ 5.5 V, and –40°C ≤ T_A ≤ +125°C

		MIN	NOM	MAX	UNIT
f_{SCLK}	Serial clock frequency			50	MHz
$t_{SCLKHIGH}$	SCLK high time	9			ns
$t_{SCLKLOW}$	SCLK low time	9			ns
t_{SDIS}	SDI setup time	8			ns
t_{SDIH}	SDI hold time	8			ns
t_{CSS}	$\overline{SYNC}$ to SCLK falling edge setup time	18			ns
t_{CSH}	SCLK falling edge to $\overline{SYNC}$ rising edge	10			ns
t_{CSHIGH}	$\overline{SYNC}$ high time	50			ns
$t_{DACWAIT}$	Sequential DAC update wait time (time between subsequent $\overline{SYNC}$ rising edges) for same channel	2			µs

6.12 Timing Requirements: SPI Read and Daisy Chain Operation (FSDO = 0)

all input signals are specified with $t_r = t_f$ = 1 V/ns (10% to 90% of V_{IO}) and timed from a voltage level of (VIL + VIH) / 2, 1.7 V ≤ V_{IO} ≤ 5.5 V, 1.7 V ≤ V_{DD} ≤ 5.5 V, –40°C ≤ T_A ≤ +125°C, and FSDO = 0

		MIN	NOM	MAX	UNIT
f_{SCLK}	Serial clock frequency			1.25	MHz
$t_{SCLKHIGH}$	SCLK high time	350			ns
$t_{SCLKLOW}$	SCLK low time	350			ns
t_{SDIS}	SDI setup time	8			ns
t_{SDIH}	SDI hold time	8			ns
t_{CSS}	$\overline{SYNC}$ to SCLK falling edge setup time	400			ns
t_{CSH}	SCLK falling edge to $\overline{SYNC}$ rising edge	400			ns
t_{CSHIGH}	$\overline{SYNC}$ high time	1			µs
t_{SDODLY}	SCLK rising edge to SDO falling edge, I_{OL} ≤ 5 mA, C_L = 20 pF.			300	ns

6.13 Timing Requirements: SPI Read and Daisy Chain Operation (FSDO = 1)

all input signals are specified with $t_r = t_f$ = 1 V/ns (10% to 90% of V_{IO}) and timed from a voltage level of (VIL + VIH) / 2, 1.7 V ≤ V_{IO} ≤ 5.5 V, 1.7 V ≤ V_{DD} ≤ 5.5 V, –40°C ≤ T_A ≤ +125°C, and FSDO = 1

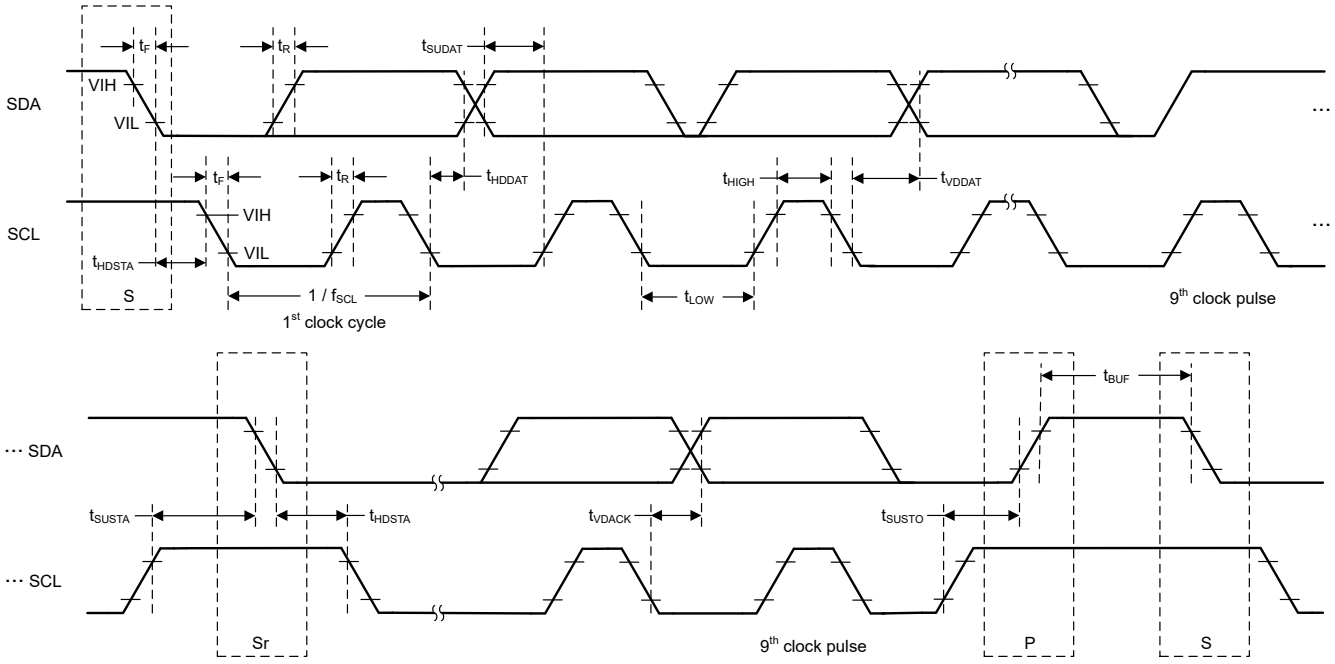
		MIN	NOM	MAX	UNIT
f_{SCLK}	Serial clock frequency			2.5	MHz
$t_{SCLKHIGH}$	SCLK high time	175			ns
$t_{SCLKLOW}$	SCLK low time	175			ns
t_{SDIS}	SDI setup time	8			ns
t_{SDIH}	SDI hold time	8			ns
t_{CSS}	$\overline{SYNC}$ to SCLK falling edge setup time	300			ns
t_{CSH}	SCLK falling edge to $\overline{SYNC}$ rising edge	300			ns
t_{CSHIGH}	$\overline{SYNC}$ high time	1			µs
t_{SDODLY}	SCLK rising edge to SDO falling edge, I_{OL} ≤ 5 mA, C_L = 20 pF.			300	ns

6.14 Timing Requirements: GPIO

all input signals are specified with $t_r = t_f$ = 1 V/ns (10% to 90% of V_{IO}) and timed from a voltage level of (VIL + VIH) / 2, 1.7 V ≤ V_{IO} ≤ 5.5 V, 1.7 V ≤ V_{DD} ≤ 5.5 V, and –40°C ≤ T_A ≤ +125°C

		MIN	NOM	MAX	UNIT
$t_{GPIHIGH}$	GPI high time	2			µs
t_{GPILOW}	GPI low time	2			µs

6.15 Timing Diagrams



S: Start bit, **Sr**: Repeated start bit, **P**: Stop bit

図 6-1. I²C Timing Diagram

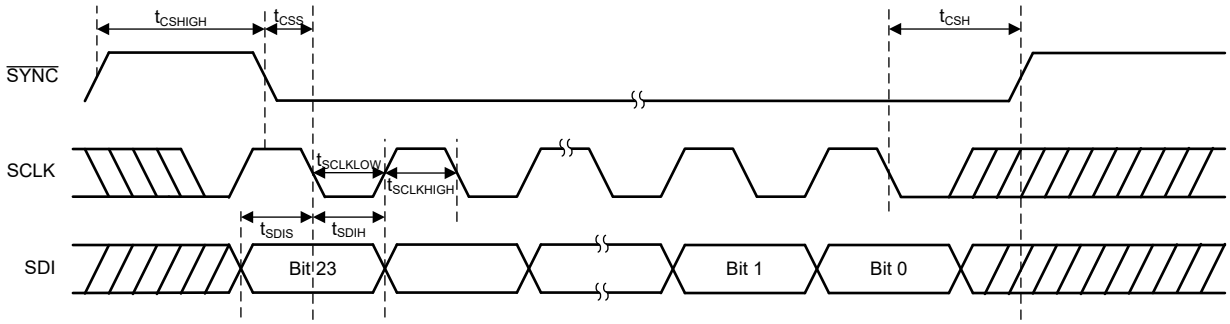


図 6-2. SPI Write Timing Diagram

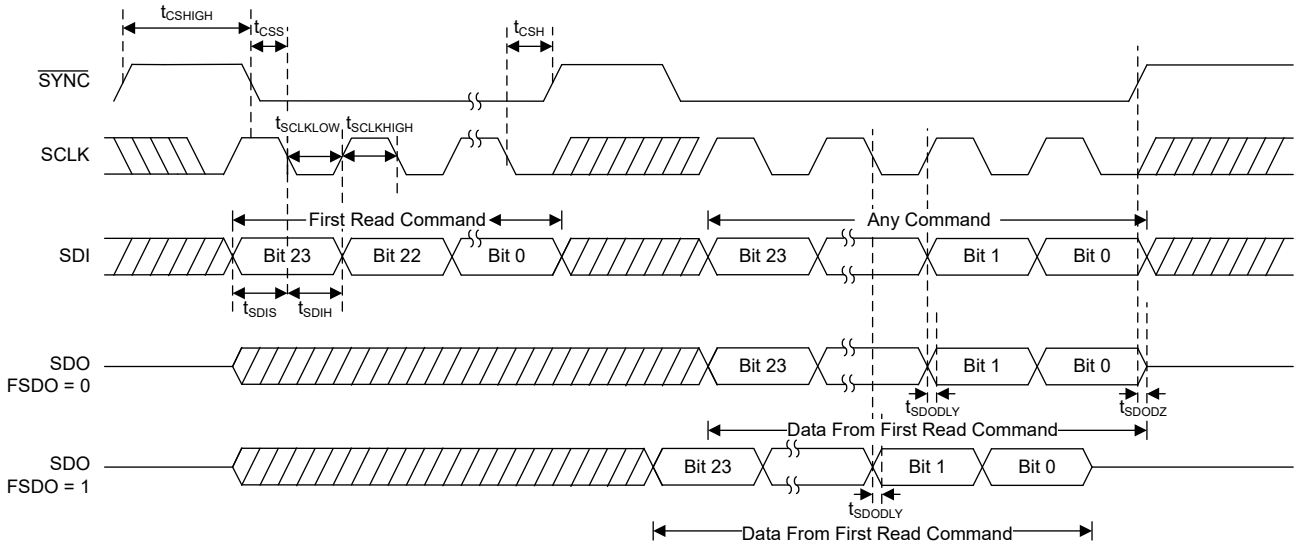


図 6-3. SPI Read Timing Diagram

6.16 Typical Characteristics: Voltage Output

at T_A = 25°C, V_{DD} = 5.5 V, external reference = 5.5 V, gain = 1 ×, and DAC outputs unloaded (unless otherwise noted)

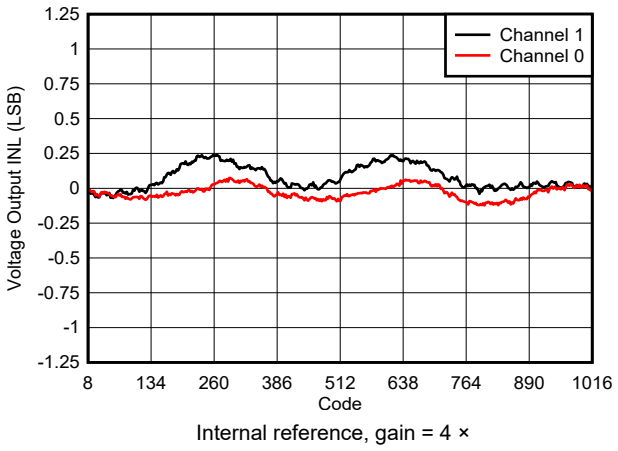


図 6-4. Voltage Output INL vs Digital Input Code

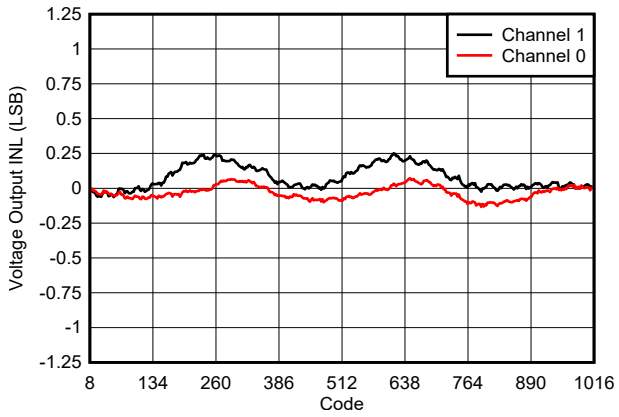


図 6-5. Voltage Output INL vs Digital Input Code

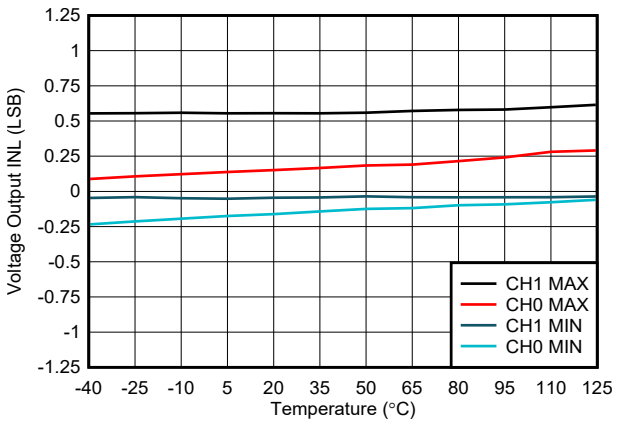


図 6-6. Voltage Output INL vs Temperature

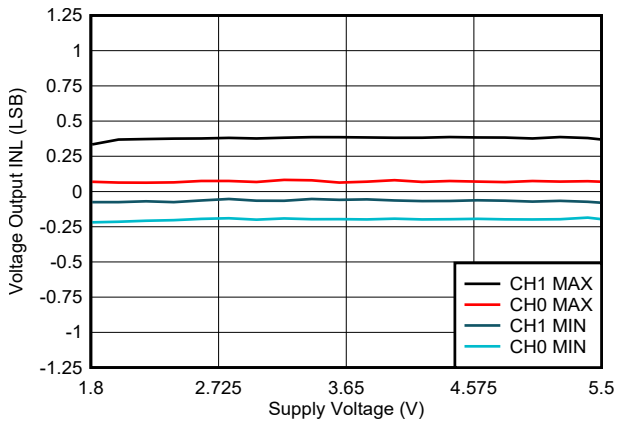


図 6-7. Voltage Output INL vs Supply Voltage

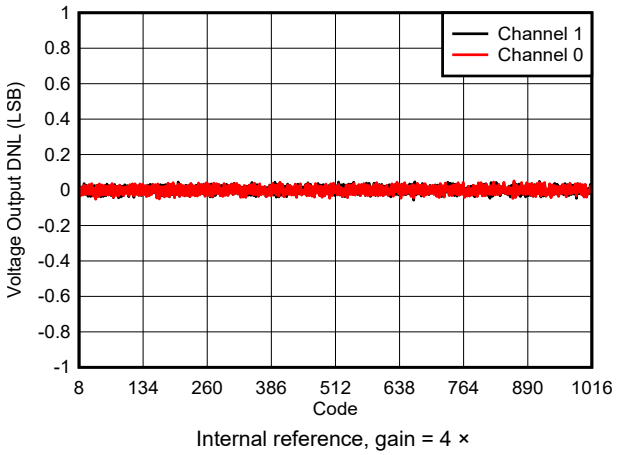


図 6-8. Voltage Output DNL vs Digital Input Code

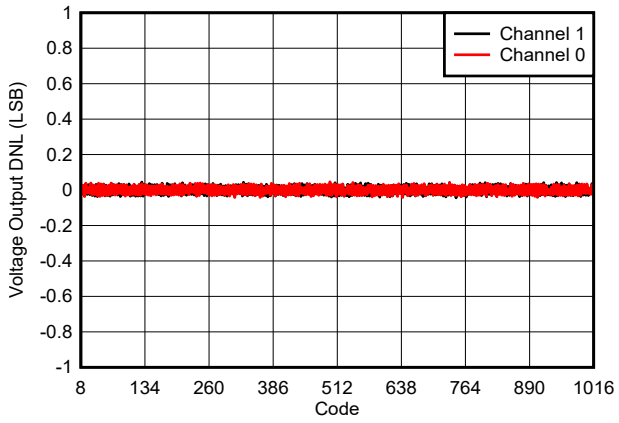


図 6-9. Voltage Output DNL vs Digital Input Code

6.16 Typical Characteristics: Voltage Output (continued)

at T_A = 25°C, V_{DD} = 5.5 V, external reference = 5.5 V, gain = 1 ×, and DAC outputs unloaded (unless otherwise noted)

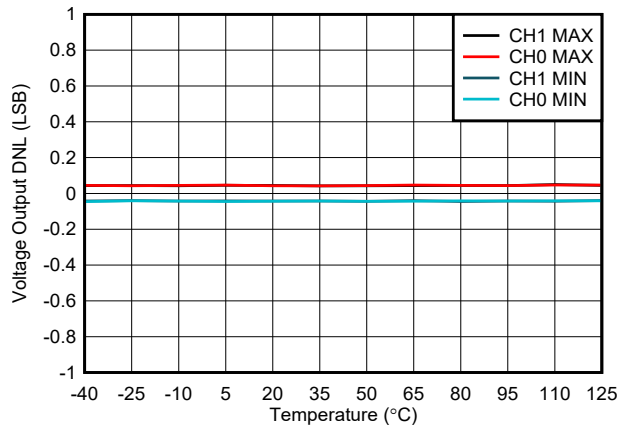


図 6-10. Voltage Output DNL vs Temperature

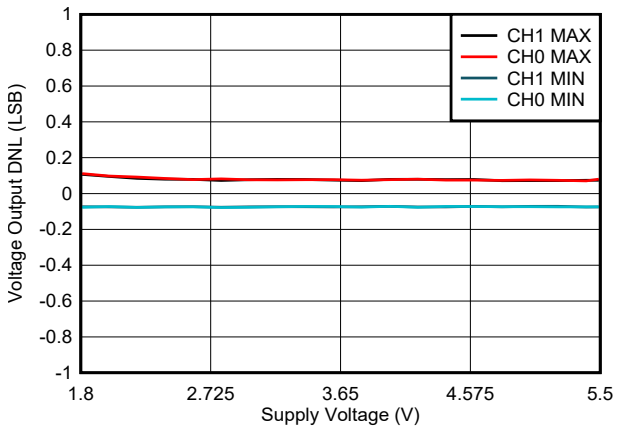
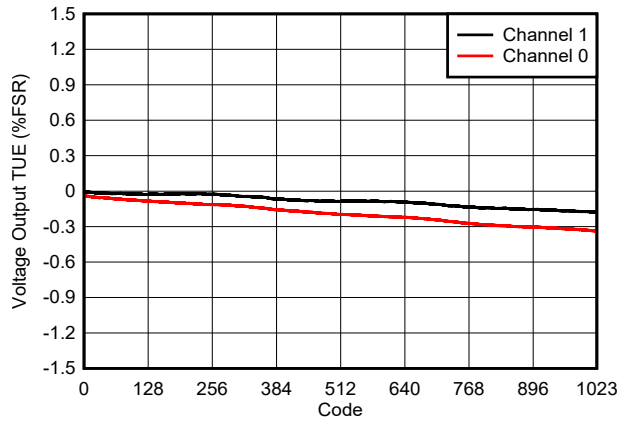


図 6-11. Voltage Output DNL vs Supply Voltage



Internal reference, gain = 4 ×

図 6-12. Voltage Output TUE vs Digital Input Code

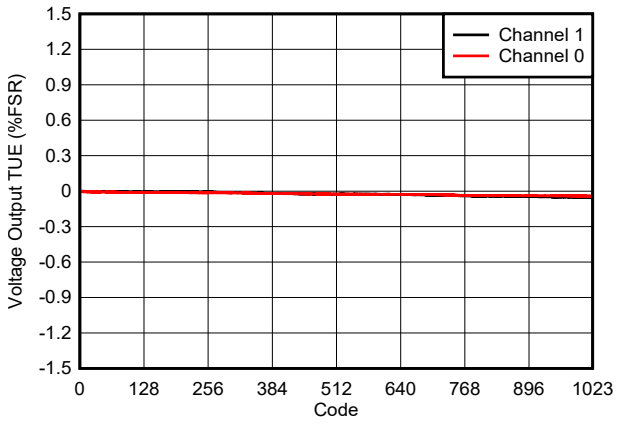
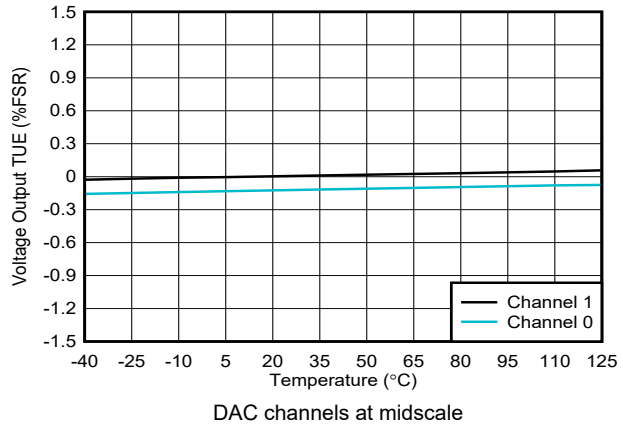
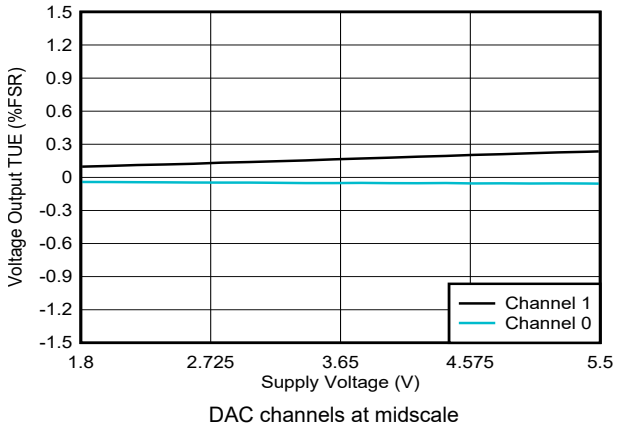


図 6-13. Voltage Output TUE vs Digital Input Code



DAC channels at midscale

図 6-14. Voltage Output TUE vs Temperature



DAC channels at midscale

図 6-15. Voltage Output TUE vs Supply Voltage

6.16 Typical Characteristics: Voltage Output (continued)

at T_A = 25°C, V_{DD} = 5.5 V, external reference = 5.5 V, gain = 1 ×, and DAC outputs unloaded (unless otherwise noted)

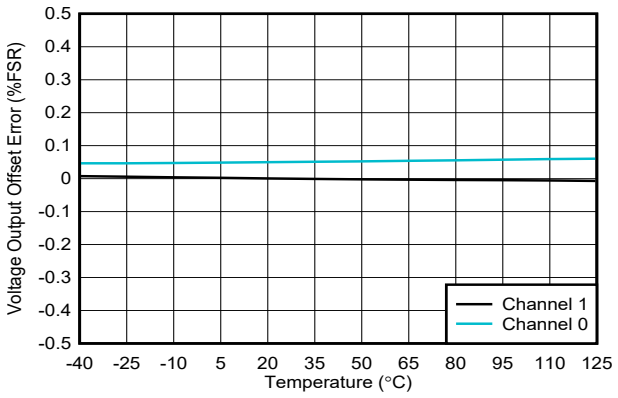


図 6-16. Voltage Output Offset Error vs Temperature

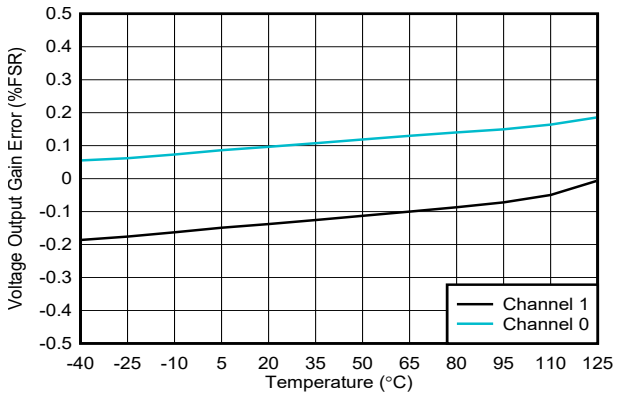
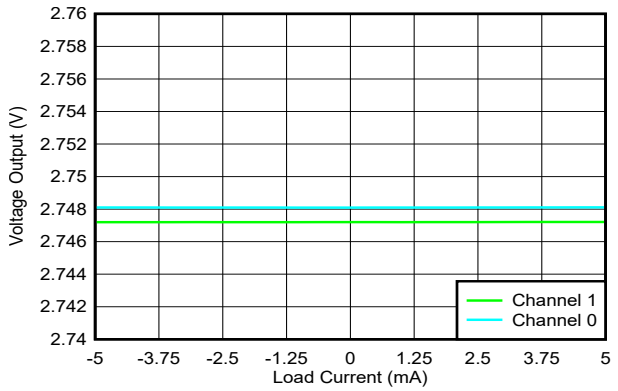


図 6-17. Voltage Output Gain Error vs Temperature



DAC channels at midscale

図 6-18. Voltage Output vs Load Current

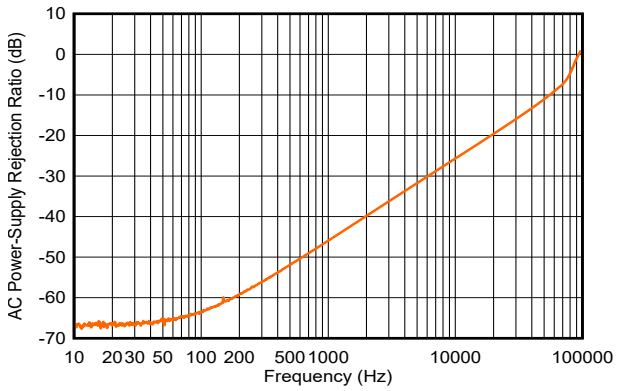


図 6-19. Voltage Output AC PSRR vs Frequency

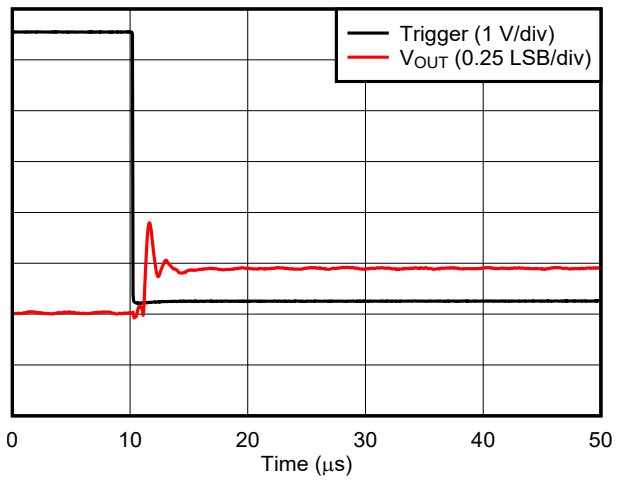


図 6-20. Voltage Output Code-to-Code Glitch - Rising Edge

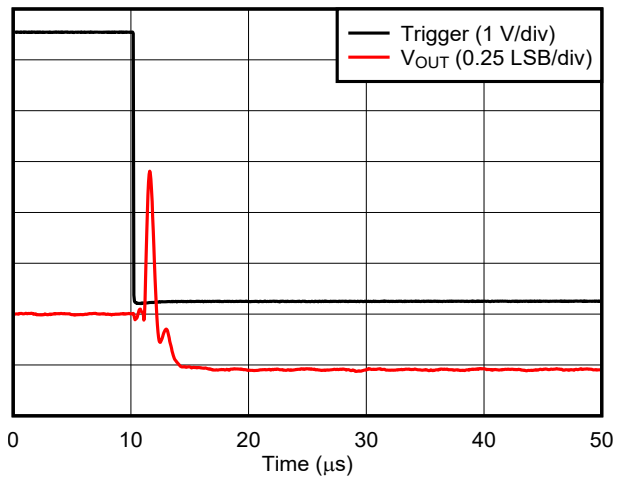
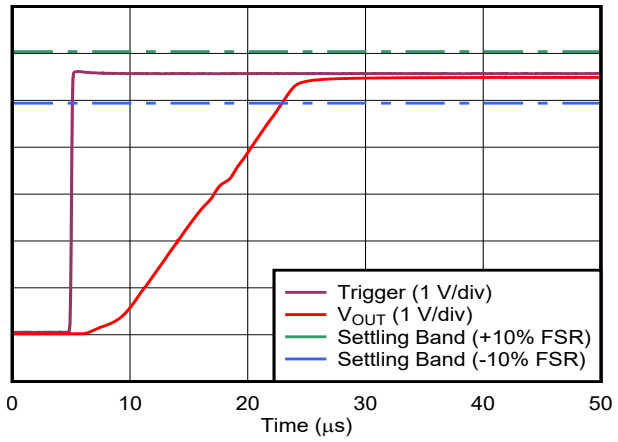


図 6-21. Voltage Output Code-to-Code Glitch - Falling Edge

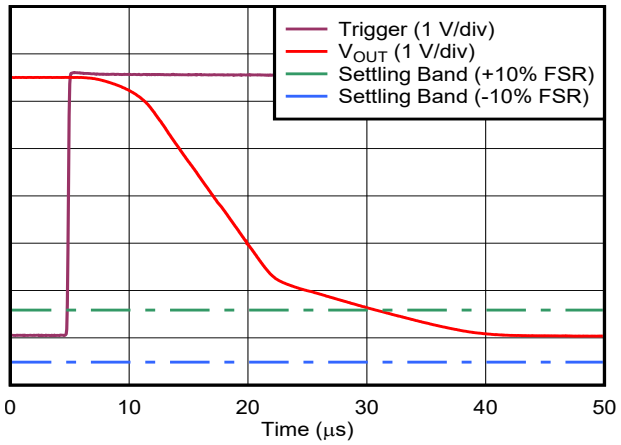
6.16 Typical Characteristics: Voltage Output (continued)

at T_A = 25°C, V_{DD} = 5.5 V, external reference = 5.5 V, gain = 1 ×, and DAC outputs unloaded (unless otherwise noted)



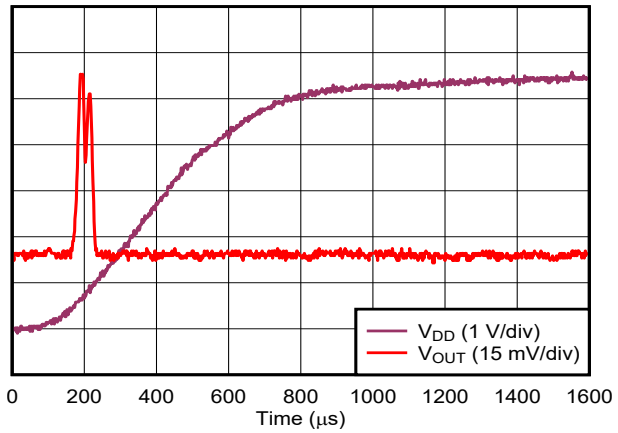
Zero scale to full scale swing

図 6-22. Voltage Output Setting Time - Rising Edge



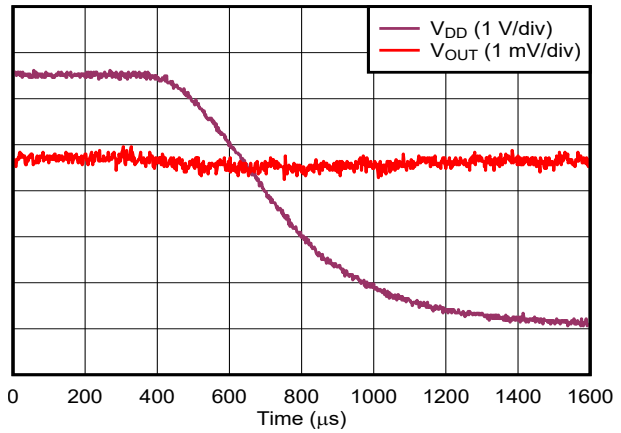
Full scale to zero scale swing

図 6-23. Voltage Output Setting Time - Falling Edge



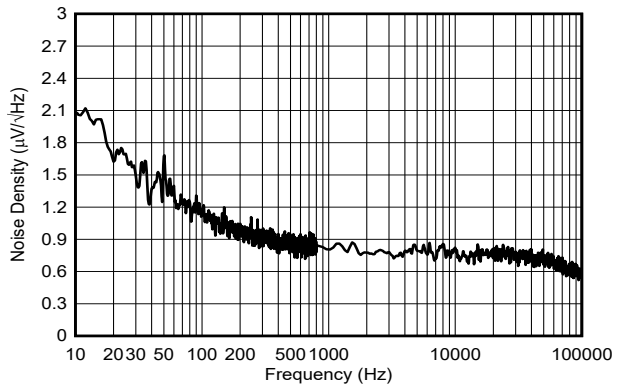
DAC in Hi-Z power-down mode

図 6-24. Voltage Output Power-On Glitch



DAC at zero scale

図 6-25. Voltage Output Power-Off Glitch



Internal reference, gain = 4 ×

図 6-26. Voltage Output Noise Density

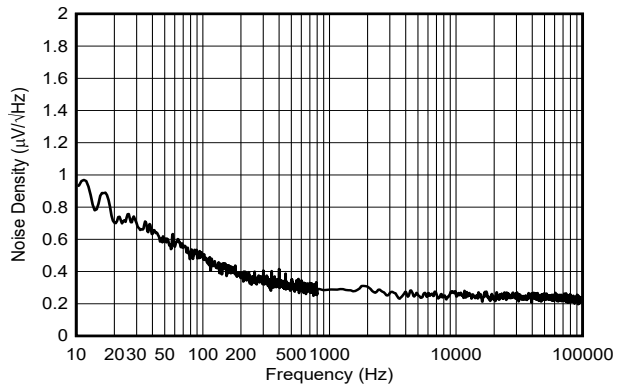
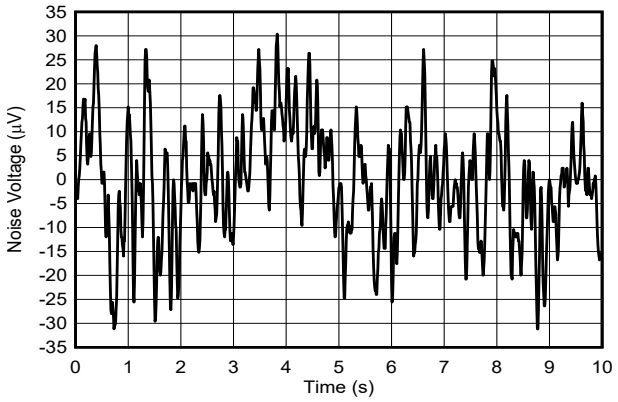


図 6-27. Voltage Output Noise Density

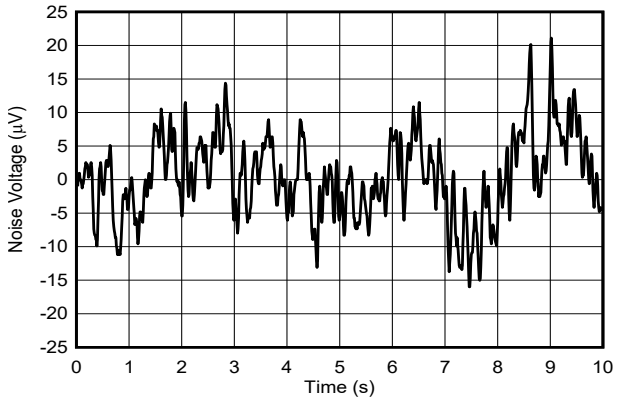
6.16 Typical Characteristics: Voltage Output (continued)

at T_A = 25°C, V_{DD} = 5.5 V, external reference = 5.5 V, gain = 1 ×, and DAC outputs unloaded (unless otherwise noted)



Internal reference, gain = 4x, f = 0.1 Hz to 10 Hz

図 6-28. Voltage Output Flicker Noise



f = 0.1 Hz to 10 Hz

図 6-29. Voltage Output Flicker Noise

6.17 Typical Characteristics: Comparator

at T_A = 25°C, V_{DD} = 5.5 V, external reference = 5.5 V, gain = 1 ×, FBx pin in Hi-Z mode, and DAC outputs unloaded (unless otherwise noted)

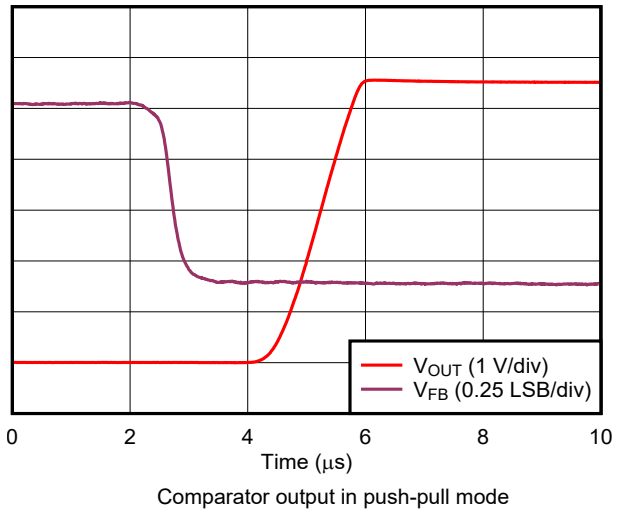


図 6-30. Comparator Response Time: Low-to-High Transition

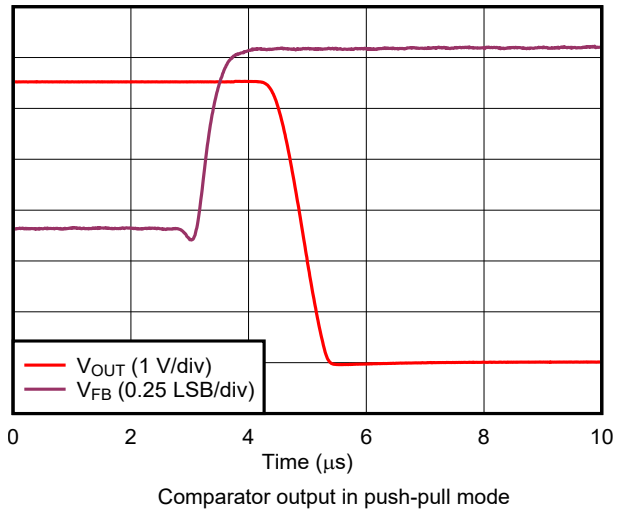


図 6-31. Comparator Response Time: High-to-Low Transition

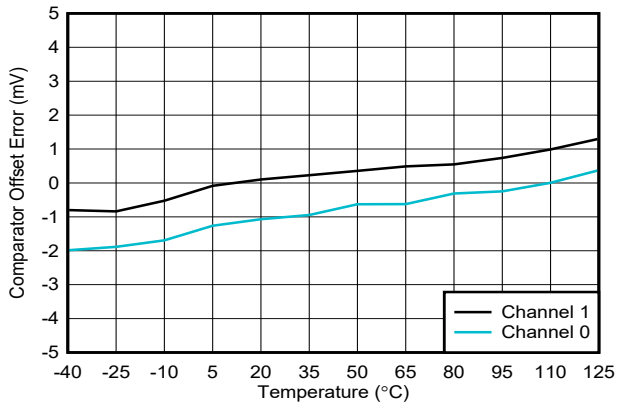
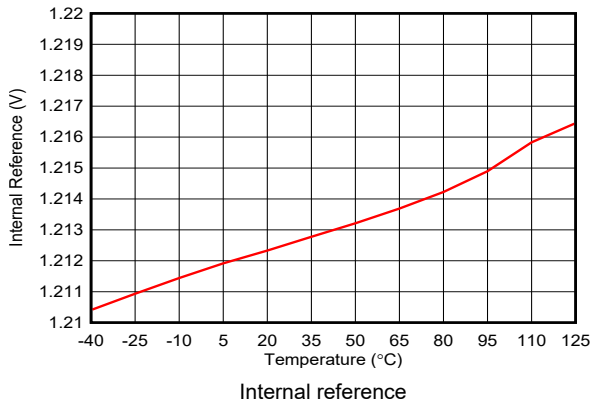


図 6-32. Comparator Offset Error vs Temperature

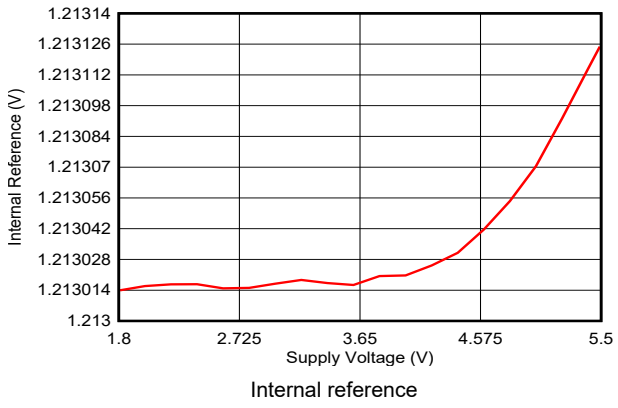
6.18 Typical Characteristics: General

at T_A = 25°C, V_{DD} = 5.5 V, and DAC outputs unloaded (unless otherwise noted)



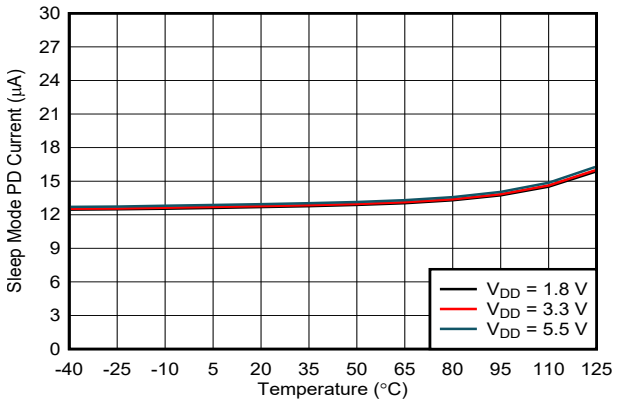
Internal reference

図 6-33. Internal Reference vs Temperature



Internal reference

図 6-34. Internal Reference vs Supply Voltage



Sleep mode, internal reference disabled

図 6-35. Power-Down Current vs Temperature

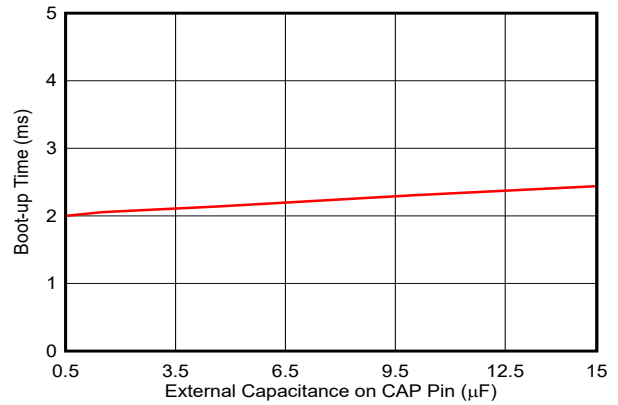


図 6-36. Boot-Up Time vs Capacitance on CAP pin

7 Detailed Description

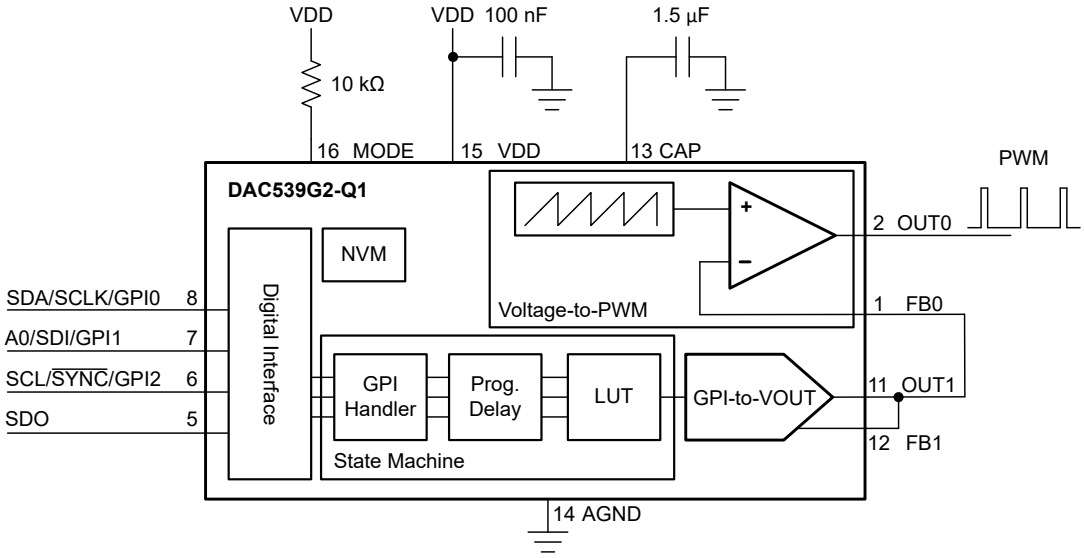
7.1 Overview

The DAC539G2-Q1 is an application-specific, look-up table (LUT) based GPI-to-PWM converter. This device has a 10-bit GPI-to-voltage output converter and a voltage-to-PWM converter. Both these circuits can be externally connected to create a GPI-to-PWM converter. Three GPIs are mapped to eight 10-bit digital codes that represent the voltage output. There is a programmable delay at the GPIs to eliminate glitches on these inputs. The look-up table values are programmed using I^2C or SPI. The GPIs are multiplexed with the I^2C and SPI pins. The voltage-to-PWM converter uses a comparator with one input as a programmable sawtooth or triangle waveform, and the other input as an external voltage input connected from the GPI-to-voltage converter.

This smart DAC use the MODE pin to select between programming mode (I^2C or SPI) and standalone-application mode. The DAC539G2-Q1 provides nonvolatile memory (NVM) to store the register settings at factory using the I^2C or SPI. After being programmed, this device functions autonomously without the need for a processor.

The DAC539G2-Q1 is an excellent choice for fault communication in automotive stop light and turn indicator modules. This device can also be used for fault communication in other industrial and automotive applications.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Smart Digital-to-Analog Converter (DAC) Architecture

The DAC539G2-Q1 uses a string architecture with a voltage-output amplifier for digital-to-analog converter functions. With an external FB pin, channel 0 functions as a programmable comparator. Channel 0 also functions as a voltage-to-PWM converter using a triangle or sawtooth waveform on the noninverting input of the amplifier. Channel 1 functions as a GPI-to-voltage converter using a look-up table with eight entries corresponding to all the binary combinations of the three GPI pins.

セクション 7.2 shows the DAC architecture within the block diagram, which operates from a 1.8-V to 5.5-V power supply. Voltage output mode uses one of the three reference options: the power supply, the DAC internal voltage reference of 1.21 V, or an external reference. This device supports multiple programmable output ranges.

The DAC539G2-Q1 provides a state machine with configurable parameters, which converts three GPI signals to PWM output. 図 7-1 shows the digital architecture of DAC539G2-Q1. The state machine is implemented in one-time programmable (OTP) memory that is one-to-one mapped to a static random access memory (SRAM). The application configuration data are stored in the SRAM section mapped to the NVM (EEPROM). The state machine can access the digital I/O directly while accessing the DAC outputs through the register map. The state machine is inaccessible by the end user. The state machine can be operated in standalone mode without interfacing to a processor (*processor-less* operation).

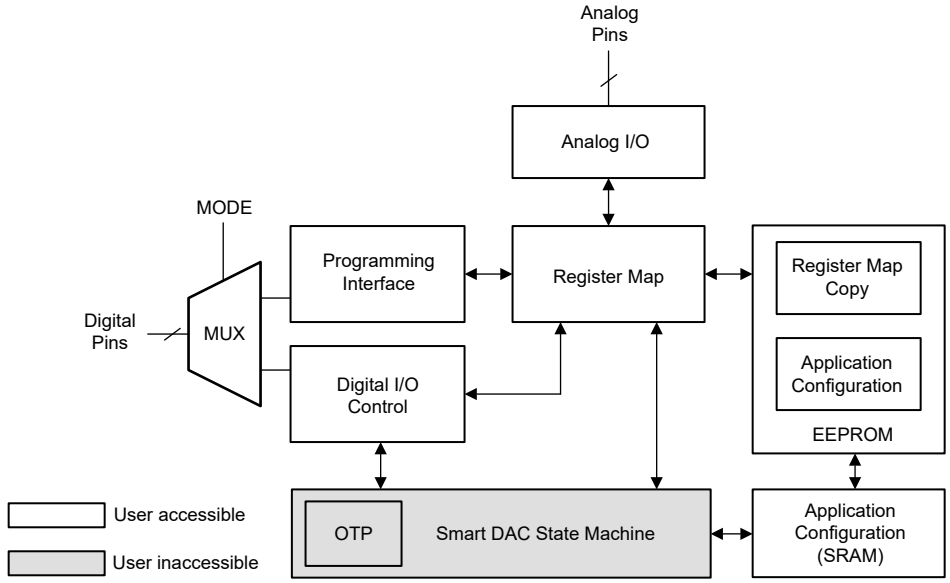


図 7-1. Smart DAC Architecture

7.3.2 Programming Interface

The DAC539G2-Q1 has five digital I/O pins that control I^2C, SPI, GPI, and mode selection. The MODE pin must be at logic low to enable the programming interface. These devices automatically detect I^2C and SPI protocols at the first successful communication after power-on, and then connect to the detected interface. After an interface protocol is connected, any change in the protocol is ignored. The I^2C interface uses the A0 pin to select from among four address options. The SPI is a three-wire interface by default. No readback capability is available in three-wire SPI mode. The SDO pin can be enabled in the register map and then programmed into the NVM. The SPI readback mode is slower than the write mode. The programming interface pins are:

- I^2C: SCL, SDA, A0
- SPI: SCLK, SDI, $\overline{\text{SYNC}}$, SDO

All the digital pins are open drain when used as outputs. Therefore, all the output pins must be pulled up to the desired I/O voltage using external resistors.

7.3.3 Nonvolatile Memory (NVM)

The DAC539G2-Q1 contains nonvolatile memory (NVM) bits. These memory bits are user programmable and erasable, and retain the set values in the absence of a power supply. The highlighted gray cells in 表 7-9 show all the register bits that can be stored in the NVM by setting NVM-PROG = 1 in the COMMON-TRIGGER register. The NVM-PROG bit autoresets. The NVM-BUSY bit in the GENERAL-STATUS register is set to 1 by the device when an NVM write or reload operation is ongoing. During this time, the device blocks all read/write operations from and to the device. The NVM-BUSY bit is set to 0 after the write or reload operation is complete; at this point, all read/write operations from and to the device are allowed. The default value for all the registers in the DAC539G2-Q1 is loaded from NVM as soon as a POR event is issued.

The DAC539G2-Q1 also implements a NVM-RELOAD bit in the COMMON-TRIGGER register. Set this bit to 1 for the device to start an NVM-reload operation. The NVM-reload operation overwrites the register map with the stored data from the NVM. After completion, the device autoresets this bit to 0. During the NVM-RELOAD operation, the NVM-BUSY bit is set to 1.

7.4 Device Functional Modes

7.4.1 GPI-to-Voltage Converter

The output for each channel is enabled by selecting the power-up option in the VOUT-PDN-X fields in the COMMON-CONFIG register. For the GPI-to-voltage converter, short the OUT1 and FB1 pins externally for a closed-loop amplifier output. An open FB1 pin saturates the amplifier output. To achieve the desired voltage output, select the correct reference option, select the amplifier gain for the required output range, and program the look-up table with DAC codes in the VOUT-DATA-X register. 表 7-1 shows the GPI to look-up table register mapping.

表 7-1. GPI-to-Voltage Converter Look up Table

GPI2	GPI1	GPI0	Register	Default Value
0	0	0	VOUT-DATA-0	3900h
0	0	1	VOUT-DATA-1	9940h
0	1	0	VOUT-DATA-2	5900h
0	1	1	VOUT-DATA-3	7940h
1	0	0	VOUT-DATA-4	3900h
1	0	1	VOUT-DATA-5	9940h
1	1	0	VOUT-DATA-6	5900h
1	1	1	VOUT-DATA-7	7940h

The DAC539G2-Q1 also supports a programmable delay to suppress or debounce any unwanted glitch on the GPI pins. A change in the GPI signals is passed to the GPI-to-voltage converter only when the change is stable for more than the delay configured using the DEBOUNCE-DELAY field in the GPI-DEBOUNCE register. The default debounce delay is approximately 50 ms. 図 7-2 shows the flowchart for the GPI-to-voltage conversion.

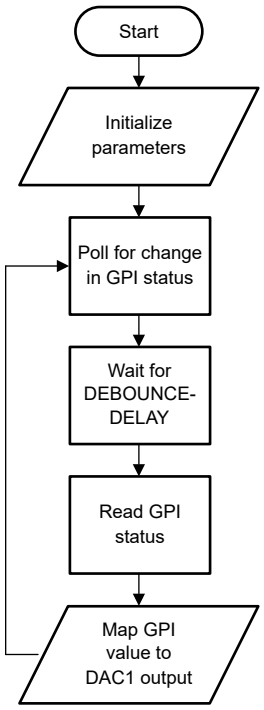


図 7-2. GPI-to-Voltage Conversion Flowchart

7.4.1.1 Voltage Reference and DAC Transfer Function

図 7-3 shows the three possible voltage reference options with the DAC539G2-Q1: the power supply as reference, internal reference, or external reference (MODE pin). The DAC transfer function in the voltage-output and comparator modes changes based on the voltage reference selection.

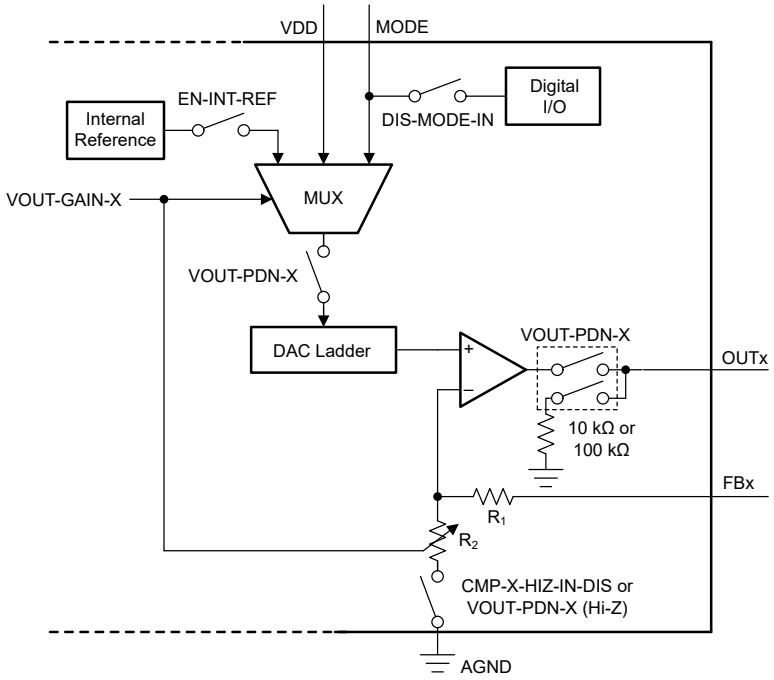


図 7-3. Voltage Reference Selection and Power-Down Logic

7.4.1.2 Power-Supply as Reference

By default, the DAC539G2-Q1 operates with the power-supply pin (VDD) as a reference. 式 1 shows DAC transfer function when the power-supply pin is used as reference. The gain at the output stage is always 1 ×.

$$V_{OUT} = \frac{VOUT\_DATA\_X}{2^N} \times V_{DD} \quad (1)$$

where:

- N is the resolution in bits, that is 10 bits.
- VOUT_DATA_X is the decimal equivalent of the binary code that is loaded to the VOUT-DATA-X field in the VOUT-DATA-X register.
- VOUT_DATA_X ranges from 0 to 2^N – 1.
- V_{DD} is used as the DAC reference voltage.

7.4.1.3 Internal Reference

The DAC539G2-Q1 contains an internal reference that is disabled by default. To enable the internal reference, write 1 to bit EN-INT-REF in the COMMON-CONFIG register. The internal reference generates a fixed 1.21-V voltage (typical). Use the VOUT-GAIN-X field in the DAC-X-VOUT-CMP-CONFIG register to achieve gains of 1.5 ×, 2 ×, 3 ×, or 4 × for the DAC output voltage (V_{OUT}). 式 2 shows DAC transfer function using the internal reference.

$$V_{OUT} = \frac{VOUT\_DATA\_X}{2^N} \times V_{REF} \times GAIN \quad (2)$$

where:

- N is the resolution in bits, that is 10 bits
- VOUT_DATA_X is the decimal equivalent of the binary code that is loaded to the VOUT-DATA-X field in the VOUT-DATA-X register.
- VOUT_DATA_X ranges from 0 to 2^N – 1.
- V_{REF} is the internal reference voltage = 1.21 V.
- GAIN = 1.5 ×, 2 ×, 3 ×, or 4 ×, based on VOUT-X-GAIN bits.

7.4.1.4 External Reference

The DAC539G2-Q1 provide an external reference input. Select the external reference option by configuring the VOUT-GAIN-X field in the DAC-X-VOUT-CMP-CONFIG register appropriately. Write 1 to the DIS-MODE-IN bit in the DEVICE-MODE-CONFIG register to minimize quiescent current. The external reference can be between 1.8 V and VDD. 式 3 shows DAC transfer function when the external reference is used.

注

The external reference must be less than VDD in both transient and steady-state conditions. Therefore, the external reference must ramp up after VDD and ramp down before VDD.

$$V_{OUT} = \frac{DAC\_DATA}{2^N} \times V_{REF} \quad (3)$$

where:

- N is the resolution in bits, 10 bits for DAC539G2-Q1.
- DAC_DATA is the decimal equivalent of the binary code that is loaded to the DAC-X-DATA field in the DAC-X-DATA register.
- DAC_DATA ranges from 0 to 2^N – 1.
- V_{REF} is the external reference voltage.

7.4.2 Voltage-to-PWM Converter

Chanel 0 functions as the voltage-to-PWM converter. Channel 1 can also be used as a comparator, if needed after the application is stopped using the STATE_MACHINE-CONFIG register. To enter the comparator mode for a channel, write 1 to the CMP-X-EN and the CMP-X-OUT-EN bits in the respective DAC-X-VOUT-CMP-CONFIG register. The comparator output can be configured as push-pull or open-drain using the CMP-X-OD-EN bit. To invert the comparator output, write 1 to the CMP-X-INV-EN bit. The FBx pin has a finite impedance. To enable high-impedance on the FBx pin, write 1 to the CMP-X-HIZ-IN-DIS bit.

注

In the Hi-Z input mode, the comparator input range is limited to:

- For GAIN = 1 ×, 1.5 ×, or 2 ×: $V_{FB} \leq (V_{REF} \times GAIN) / 3$
- For GAIN = 3 ×, or 4 ×: $V_{FB} \leq (V_{REF} \times GAIN) / 6$

Any higher input voltage is clipped.

7.4.2.1 Function Generation

The DAC539G2-Q1 implements a continuous waveform generation feature. This device generates a triangular wave or a sawtooth wave on channel 0 for voltage-to-PWM conversion.

7.4.2.1.1 Triangular Waveform Generation

図 7-4 shows that the triangular waveform uses the FUNCTION-MIN and FUNCTION-MAX registers for minimum and maximum levels, respectively. 式 4 calculates the frequency of the waveform depending on the minimum and maximum levels, and the CODE-STEP and TIME-STEP settings. An external resistor-capacitor (RC) load with a time-constant greater than the TIME-STEP settings can be dominant over the internal frequency calculation. The CODE-STEP and TIME-STEP settings are available in the FUNCTION-CONFIG register. Write 0b000 to the FUNCTION-SELECT bit field in the FUNCTION-CONFIG register to select the triangular waveform.

$$f_{TRIANGLE} = \frac{1}{2 \times TIME\_STEP \times CEILING\left(\frac{FUNCTION\_MAX - FUNCTION\_MIN}{CODE\_STEP}\right)} \quad (4)$$

where:

- TIME_STEP is the TIME-STEP setting specified in the FUNCTION-CONFIG register.
- CODE_STEP is the CODE-STEP setting specified in the FUNCTION-CONFIG register.
- FUNCTION_MAX is the decimal value specified in the FUNCTION-MAX register. Specify the value of FUNCTION_MAX as min(full code, (FUNCTION_MIN + n × CODE_STEP)), where n is an integer.
- FUNCTION_MIN is the decimal value specified in the FUNCTION-MIN register.

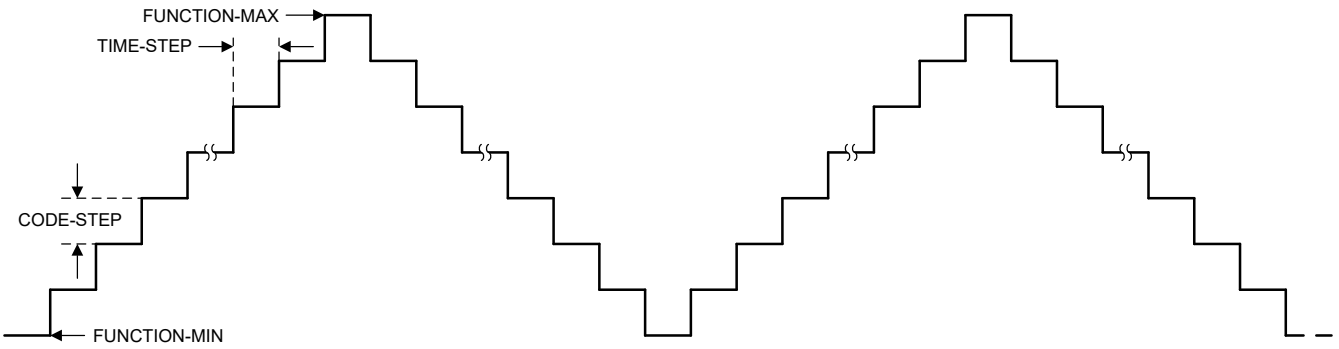


図 7-4. Triangle Waveform

7.4.2.1.2 Sawtooth Waveform Generation

図 7-5 shows that the sawtooth and the inverse sawtooth waveforms use the FUNCTION-MIN and FUNCTION-MAX registers for minimum and maximum levels, respectively. 式 5 calculates the frequency of the waveform, depending on the minimum and maximum levels, and the CODE-STEP and TIME-STEP settings. An external RC load with a time constant greater than the TIME-STEP settings can be dominant over the internal frequency calculation. The CODE-STEP and TIME-STEP settings are available in the FUNCTION-CONFIG register. Write 0b001 to the FUNCTION-SELECT bit field in the FUNCTION-CONFIG register to select the sawtooth waveform, and write 0b010 to select the inverse sawtooth waveform.

$$f_{SAWTOOTH} = \frac{1}{TIME\_STEP \times CEILING\left(\frac{FUNCTION\_MAX - FUNCTION\_MIN}{CODE\_STEP} + 1\right)} \quad (5)$$

where:

- TIME_STEP is the TIME-STEP setting as specified in the FUNCTION-CONFIG register.
- CODE_STEP is the CODE-STEP setting as specified in the FUNCTION-CONFIG register.
- FUNCTION_MAX is the decimal value specified in the FUNCTION-MAX register. Specify the value of FUNCTION_MAX as min(full code, (FUNCTION_MIN + n × CODE_STEP)), where n is an integer.
- FUNCTION_MIN is the decimal value specified in the FUNCTION-MIN register.

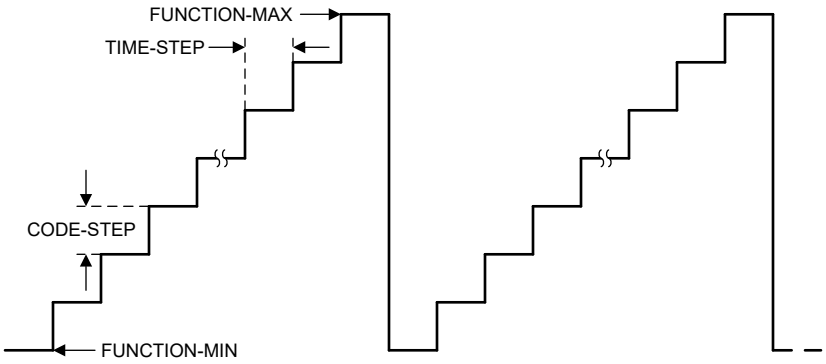


図 7-5. Sawtooth Waveform

7.4.2.1.3 PWM Frequency Correction

The accuracy of the waveform frequencies depend on the accuracy of the internal oscillator. The DAC539G2-Q1 supports a calibration option to get the best PWM frequency accuracy. The FREQUENCY-ERROR bits in the PWM-FREQUENCY-ERROR register store the oscillator error in 2's compliment format. The stored error resolution is 0.2% per LSB. 式 6 calculates the percentage frequency error.

$$f_{ERROR}(\%) = FREQENCY\_ERROR \times 0.2 \quad (6)$$

To correct the PWM frequency error, either FUNCTION-MAX or FUNCTION-MIN or both values need to be adjusted with respect to the error magnitude. Invert 式 4 and 式 5 to calculate the required correction factor.

7.4.3 Device Reset and Fault Management

This section provides the details of power-on-reset (POR), software reset, and other diagnostics and fault-management features of the DAC539G2-Q1.

7.4.3.1 Power-On Reset (POR)

The DAC539G2-Q1 includes a power-on reset (POR) function that controls the output voltage at power up. After the V_{DD} supply has been established, a POR event is issued. The POR causes all registers to initialize to default values, and communication with the device is valid only after a POR (boot-up) delay. The default value for all the registers in the DAC539G2-Q1 is loaded from NVM as soon as the POR event is issued.

When the device powers up, a POR circuit sets the device to the default mode. 図 7-6 shows that the POR circuit requires specific V_{DD} levels to make sure that the internal capacitors discharge and reset the device at power up. To make sure that a POR occurs, V_{DD} must be less than 0.7 V for at least 1 ms. When V_{DD} drops to less than 1.65 V, but remains greater than 0.7 V (shown as the undefined region), the device may or may not reset under all specified temperature and power-supply conditions. In this case, initiate a POR. When V_{DD} remains greater than 1.65 V, a POR does not occur.

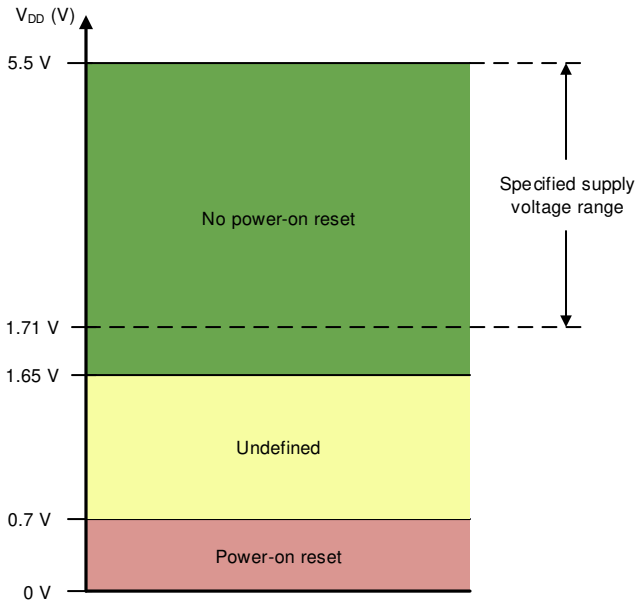


図 7-6. Threshold Levels for V_{DD} POR Circuit

7.4.3.2 External Reset

An external reset to the device is triggered through the register map. To initiate a device software reset event, write the reserved code 0b1010 to the RESET field in the COMMON-TRIGGER register. A software reset initiates a POR event.

7.4.3.3 Register-Map Lock

The DAC539G2-Q1 implements a register-map lock feature that prevents an accidental or unintended write to the DAC registers. The device locks all the registers when the DEV-LOCK bit in the COMMON-CONFIG register is set to 1. However, the software reset function through the COMMON-TRIGGER register is not blocked when using I^2C. To bypass the DEV-LOCK setting, write 0b0101 to the DEV-UNLOCK bits in the COMMON-TRIGGER register.

7.4.3.4 NVM Cyclic Redundancy Check (CRC)

The DAC539G2-Q1 implements a cyclic redundancy check (CRC) feature for the NVM to make sure that the data stored in the NVM is uncorrupted. There are two types of CRC alarm bits implemented in DAC539G2-Q1:

- NVM-CRC-FAIL-USER
- NVM-CRC-FAIL-INT

The NVM-CRC-FAIL-USER bit indicates the status of the user-programmable NVM bits, and the NVM-CRC-FAIL-INT bit indicates the status of the internal NVM bits The CRC feature is implemented by storing a 16-bit CRC (CRC-16-CCITT) along with the NVM data each time an NVM program operation (write or reload) is performed and during the device start-up. The device reads the NVM data and validates the data with the stored CRC. The CRC alarm bits (NVM-CRC-FAIL-USER and NVM-CRC-FAIL-INT in the GENERAL-STATUS register) report any errors after the data are read from the device NVM. The alarm bits are set only at boot up.

7.4.3.4.1 NVM-CRC-FAIL-USER Bit

A logic 1 on the NVM-CRC-FAIL-USER bit indicates that the user-programmable NVM data are corrupt. During this condition, all registers in the DAC are initialized with factory reset values, and all DAC registers can be written to or read from. To reset the alarm bits to 0, issue a software reset command (see *セクション 7.4.3.2*), or cycle power to the DAC. A software reset or power-cycle also reloads the user-programmable NVM bits. In case the failure persists, reprogram the NVM.

7.4.3.4.2 NVM-CRC-FAIL-INT Bit

A logic 1 on NVM-CRC-FAIL-INT bit indicates that the internal NVM data are corrupt. During this condition, all registers in the DAC are initialized with factory reset values, and all DAC registers can be written to or read from. In case of a temporary failure, to reset the alarm bits to 0, issue a software reset command (see *セクション 7.4.3.2*) or cycle power to the DAC. A permanent failure in the NVM makes the device unusable.

7.4.4 Power-Down Mode

The DAC539G2-Q1 output amplifier and internal reference can be independently powered down through the EN-INT-REF and VOUT-PDN-X bits in the COMMON-CONFIG register (see 図 7-3). At power up, the DAC outputs are enabled and the internal reference is disabled by default. Use the VOUT-PDN-X bits to configure the DAC outputs (OUTx pins) as Hi-Z, 10 kΩ-A_{GND}, or 100 kΩ-A_{GND} power-down mode.

The DAC power-up state can be programmed to any state (power-down or normal mode) using the NVM. 表 7-2 shows the DAC power-down bits.

表 7-2. DAC Power-Down Bits

REGISTER	VOUT-PDN-X[1]	VOUT-PDN-X[0]	DESCRIPTION
COMMON-CONFIG	0	0	Power up VOUT-X.
	0	1	Power down VOUT-X with 10 kΩ to AGND.
	1	0	Power down VOUT-X with 100 kΩ to AGND.
	1	1	Power down VOUT-X to Hi-Z.

7.5 Programming

7.5.1 SPI Programming Mode

An SPI access cycle for the DAC539G2-Q1 is initiated by asserting the $\overline{\text{SYNC}}$ pin low. The serial clock, SCLK, can be continuous or gated. SDI data are clocked on the SCLK falling edges. The SPI frame for the DAC539G2-Q1 is 24 bits long. Therefore, the $\overline{\text{SYNC}}$ pin must stay low for at least 24 SCLK falling edges. The access cycle ends when the $\overline{\text{SYNC}}$ pin is deasserted high. If the access cycle contains less than the minimum clock edges, the communication is ignored. By default, the SDO pin is not enabled (three-wire SPI). In three-wire SPI mode, if the access cycle contains more than the minimum clock edges, only the first 24 bits are used by the device. When $\overline{\text{SYNC}}$ is high, the SCLK and SDI signals are blocked, and SDO becomes Hi-Z to allow data readback from other devices connected on the bus.

表 7-3 and 図 7-7 describe the format for the 24-bit SPI access cycle. The first byte input to SDI is the instruction cycle. The instruction cycle identifies the request as a read or write command and the 7-bit address that is to be accessed. The last 16 bits in the cycle form the data cycle.

表 7-3. SPI Read/Write Access Cycle

BIT	FIELD	DESCRIPTION
23	R/$\overline{\text{W}}$	Identifies the communication as a read or write command to the address register: R/$\overline{\text{W}}$ = 0 sets a write operation. R/$\overline{\text{W}}$ = 1 sets a read operation
22-16	A[6:0]	Register address: specifies the register to be accessed during the read or write operation
15-0	DI[15:0]	Data cycle bits: If a write command, the data cycle bits are the values to be written to the register with address A[6:0]. If a read command, the data cycle bits are *don't care* values.

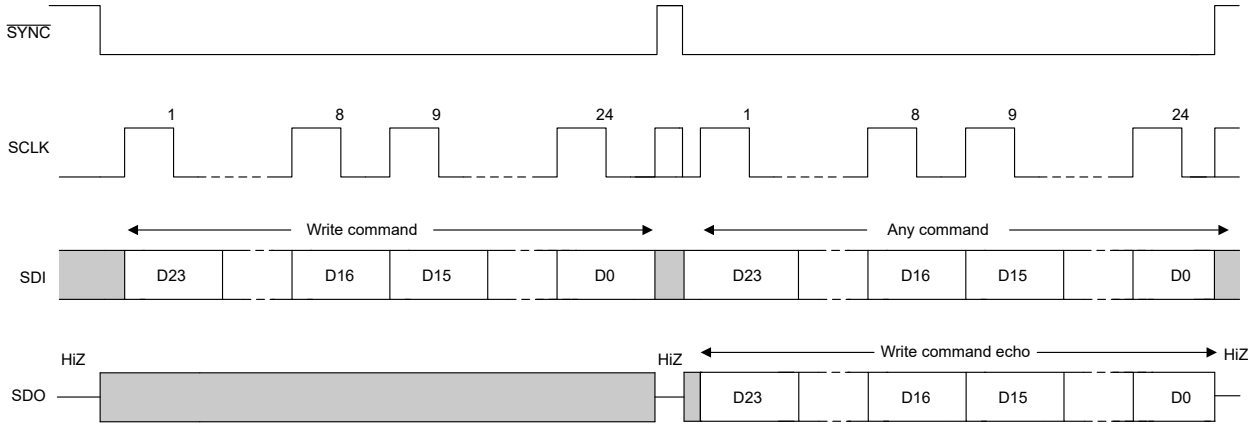


図 7-7. SPI Write Cycle

Read operations require that the SDO pin is first enabled by setting the SDO-EN bit in the INTERFACE-CONFIG register. This configuration is called four-wire SPI. A read operation is initiated by issuing a read command access cycle. After the read command, a second access cycle must be issued to get the requested data. 表 7-4 and 図 7-8 show the output data format. Data are clocked out on the SDO pin either on the falling edge or rising edge of SCLK according to the FSDO bit (see also 図 6-3).

表 7-4. SDO Output Access Cycle

BIT	FIELD	DESCRIPTION
23	R/$\overline{\text{W}}$	Echo R/$\overline{\text{W}}$ from previous access cycle
22-16	A[6:0]	Echo register address from previous access cycle
15-0	DI[15:0]	Readback data requested on previous access cycle

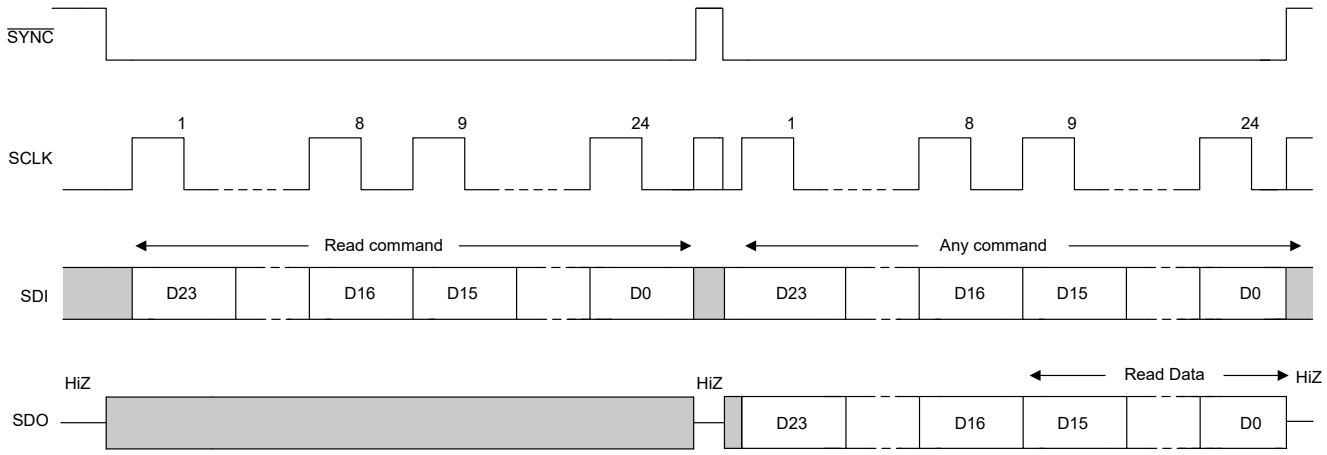


図 7-8. SPI Read Cycle

The daisy-chain operation is also enabled with the SDO pin. 図 7-9 shows that in daisy-chain mode, multiple devices are connected in a *chain* with the SDO pin of one device is connected to SDI pin of the following device. The SPI host drives the SDI pin of the first device in the chain. The SDO pin of the last device in the chain is connected to the POCI pin of the SPI host. In four-wire SPI mode, if the access cycle contains multiples of 24 clock edges, only the last 24 bits are used by the device first device in the chain. If the access cycle contains clock edges that are not in multiples of 24, the SPI packet is ignored by the device. 図 7-10 describes the packet format for the daisy-chain write cycle.

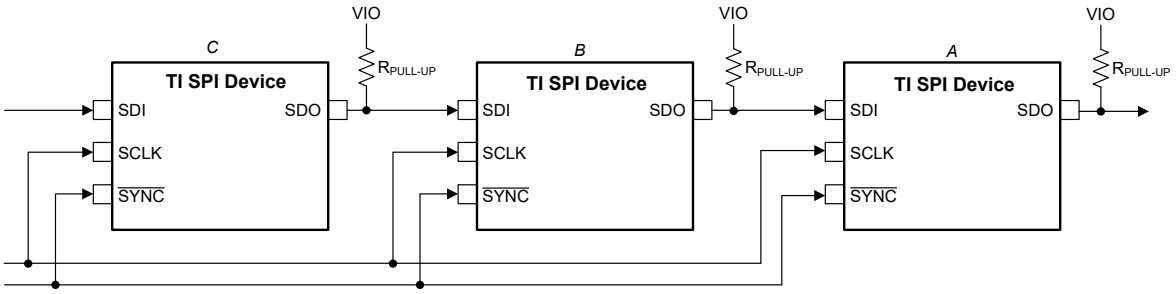


図 7-9. SPI Daisy-Chain Connection

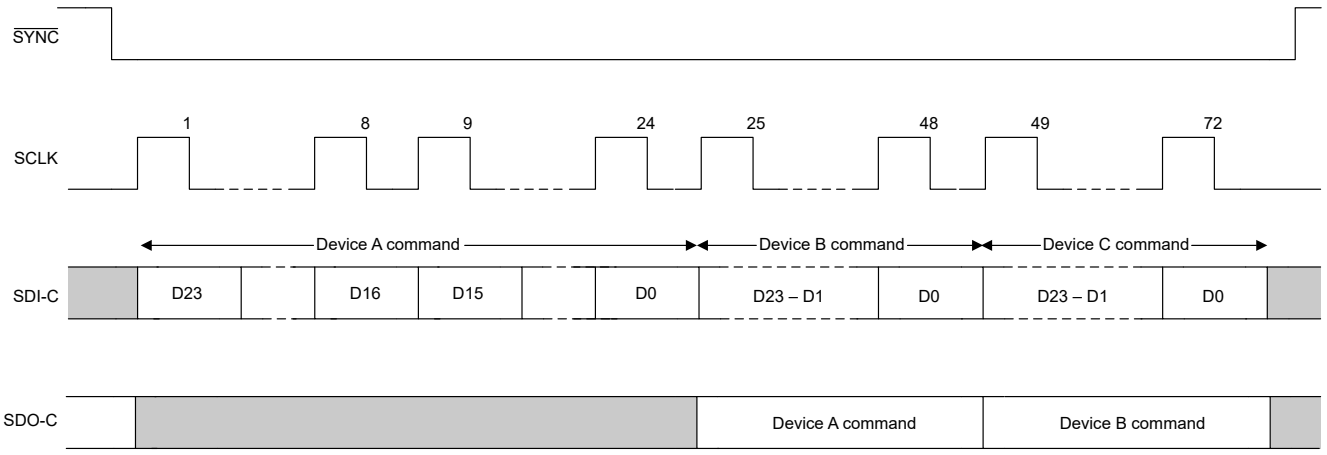


図 7-10. SPI Daisy-Chain Write Cycle

7.5.2 I²C Programming Mode

The DAC539G2-Q1 has a 2-wire serial interface (SCL and SDA), and one address pin (A0); see also 図 5-1. The I²C bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I²C-compatible devices connect to the I²C bus through the open drain I/O pins, SDA and SCL.

The I²C specification states that the device that controls communication is called a *controller*, and the devices that are controlled by the controller are called *targets*. The controller generates the SCL signal. The controller also generates special timing conditions (start condition, repeated start condition, and stop condition) on the bus to indicate the start or stop of a data transfer. Device addressing is completed by the controller. The controller on an I²C bus is typically a microcontroller or digital signal processor (DSP). The DAC539G2-Q1 operates as a target on the I²C bus. A target acknowledges controller commands, and upon controller control, receives or transmits data.

Typically, the DAC539G2-Q1 family operates as a target receiver. A controller writes to the DAC539G2-Q1, a target receiver. However, if a controller requires the DAC539G2-Q1 internal register data, the DAC539G2-Q1 operates as a target transmitter. In this case, the controller reads from the DAC539G2-Q1. According to I²C terminology, read and write refer to the controller.

The DAC539G2-Q1 supports the following data transfer modes:

- Standard mode (100Kbps)
- Fast mode (400Kbps)
- Fast mode plus (1.0Mbps)

The data transfer protocol for standard and fast modes is exactly the same; therefore, both modes are referred to as *F/S-mode* in this document. The fast mode plus protocol is supported in terms of data transfer speed, but not output current. The low-level output current is 3 mA; similar to the case of standard and fast modes. The DAC539G2-Q1 supports 7-bit addressing. The 10-bit addressing mode is not supported. The device supports the general call reset function. Sending the following sequence initiates a software reset within the device: start or repeated start, 0x00, 0x06, stop. The reset is asserted within the device on the rising edge of the ACK bit, following the second byte.

Other than specific timing signals, the I²C interface works with serial bytes. At the end of each byte, a ninth clock cycle generates and detects an acknowledge signal. An acknowledge is when the SDA line is pulled low during the high period of the ninth clock cycle. 図 7-11 depicts a not-acknowledge, when the SDA line is left high during the high period of the ninth clock cycle.

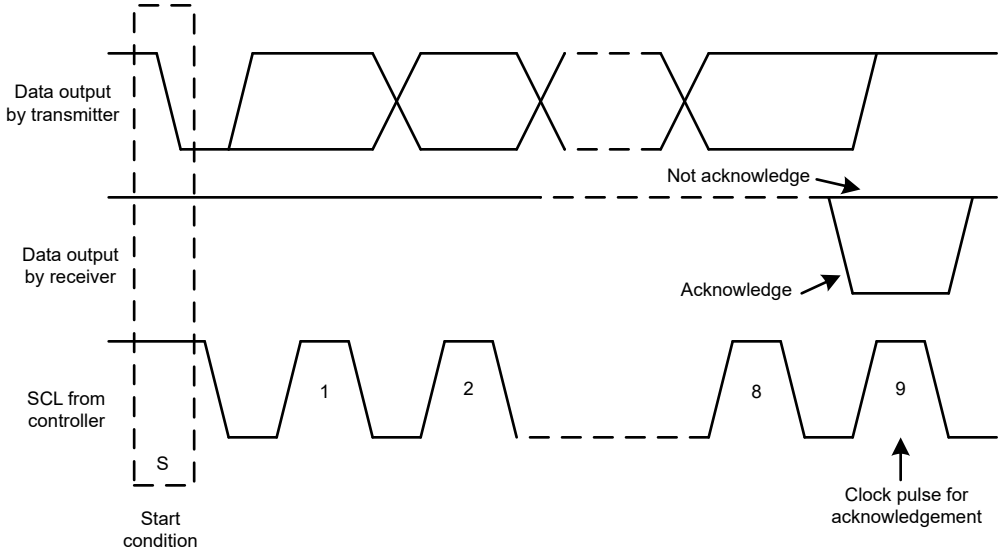


図 7-11. Acknowledge and Not Acknowledge on the I²C Bus

7.5.2.1 F/S Mode Protocol

The following steps explain a complete transaction in F/S mode.

1. The controller initiates data transfer by generating a start condition. 図 7-12 shows that the start condition is when a high-to-low transition occurs on the SDA line while SCL is high. All I^2C-compatible devices recognize a start condition.
2. The controller then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit (R/$\overline{W}$) on the SDA line. During all transmissions, the controller makes sure that data are valid. 図 7-13 shows that a valid data condition requires the SDA line to be stable during the entire high period of the clock pulse. All devices recognize the address sent by the controller and compare the address to the respective internal fixed address. Only the target device with a matching address generates an acknowledge by pulling the SDA line low during the entire high period of the 9th SCL cycle (see also 図 7-11). When the controller detects this acknowledge, the communication link with a target has been established.
3. The controller generates further SCL cycles to transmit (R/$\overline{W}$ bit 0) or receive (R/$\overline{W}$ bit 1) data to the target. In either case, the receiver must acknowledge the data sent by the transmitter. The acknowledge signal can be generated by the controller or by the target, depending on which is the receiver. The 9-bit valid data sequences consists of eight data bits and one acknowledge-bit, and can continue as long as necessary.
4. 図 7-12 shows that to signal the end of the data transfer, the controller generates a stop condition by pulling the SDA line from low-to-high while the SCL line is high. This action releases the bus and stops the communication link with the addressed target. All I^2C-compatible devices recognize the stop condition. Upon receipt of a stop condition, the bus is released, and all target devices then wait for a start condition followed by a matching address.

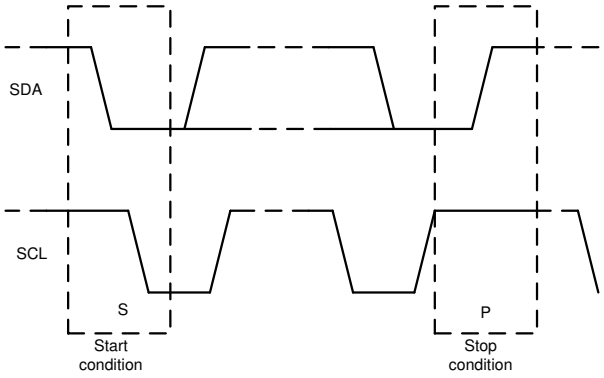


図 7-12. Start and Stop Conditions

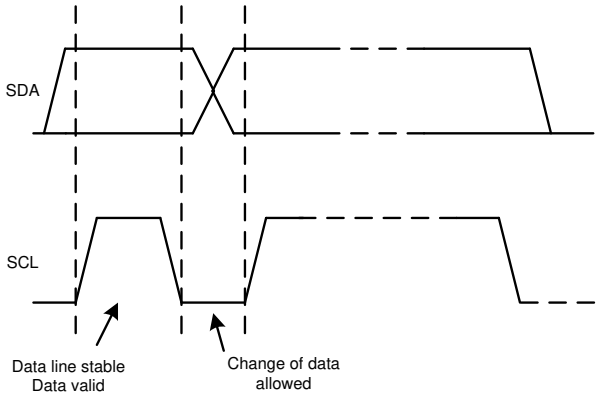


図 7-13. Bit Transfer on the I^2C Bus

7.5.2.2 I²C Update Sequence

表 7-5 shows that for a single update, the DAC539G2-Q1 requires a start condition, a valid I²C address byte, a command byte, and two data bytes.

表 7-5. Update Sequence

MSB	....	LSB	ACK	MSB	...	LSB	ACK	MSB	...	LSB	ACK	MSB	...	LSB	ACK
Address (A) byte セクション 7.5.2.2.1				Command byte セクション 7.5.2.2.2				Data byte - MSDB				Data byte - LSDB			
DB [31:24]				DB [23:16]				DB [15:8]				DB [7:0]			

図 7-14 shows that after each byte is received, the DAC539G2-Q1 acknowledges the byte by pulling the SDA line low during the high period of a single clock pulse. These four bytes and acknowledge cycles make up the 36 clock cycles required for a single update to occur. A valid I²C address byte selects the DAC539G2-Q1.

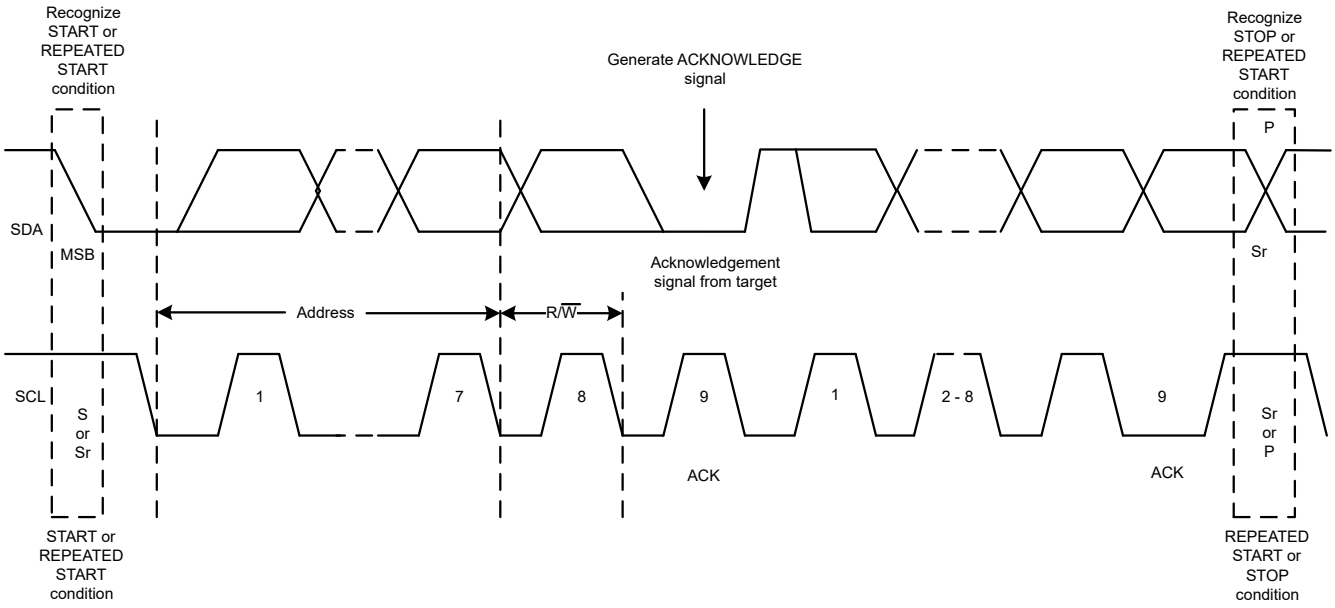


図 7-14. I²C Bus Protocol

The command byte sets the operating mode of the selected DAC539G2-Q1 device. For a data update to occur when the operating mode is selected by this byte, the DAC539G2-Q1 device must receive two data bytes: the most significant data byte (MSDB) and least significant data byte (LSDB). The DAC539G2-Q1 device performs an update on the falling edge of the acknowledge signal that follows the LSDB.

When using fast mode (clock = 400 kHz), the maximum DAC update rate is limited to 10 kSPS. Using fast mode plus (clock = 1 MHz), the maximum DAC update rate is limited to 25 kSPS. When a stop condition is received, the DAC539G2-Q1 device releases the I²C bus and awaits a new start condition.

7.5.2.2.1 Address Byte

表 7-6 depicts the address byte, the first byte received from the controller device following the start condition. The first four bits (MSBs) of the address are factory preset to 0b1001. The next three bits of the address are controlled by the A0 pin. The A0 pin input can be connected to VDD, AGND, SCL, or SDA. The A0 pin is sampled during the first byte of each data frame to determine the address. The device latches the value of the address pin, and consequently responds to that particular address according to 表 7-7.

表 7-6. Address Byte

COMMENT	MSB							LSB
—	AD6	AD5	AD4	AD3	AD2	AD1	AD0	R/$\overline{W}$
General address	1	0	0	1	See 表 7-7 (target address column)			0 or 1
Broadcast address	1	0	0	0	1	1	1	0

表 7-7. Address Format

TARGET ADDRESS	A0 PIN
000	AGND
001	VDD
010	SDA
011	SCL

The DAC539G2-Q1 supports broadcast addressing, which is used for synchronously updating or powering down multiple DAC539G2-Q1 devices. When the broadcast address is used, the DAC539G2-Q1 responds regardless of the address pin state. Broadcast is supported only in write mode.

7.5.2.2.2 Command Byte

表 7-10 lists the command byte in the ADDRESS column.

7.5.2.3 I^2C Read Sequence

To read any register the following command sequence must be used:

1. Send a start or repeated start command with a target address and the R/$\overline{W}$ bit set to 0 for writing. The device acknowledges this event.
2. Send a command byte for the register to be read. The device acknowledges this event again.
3. Send a repeated start with the target address and the R/$\overline{W}$ bit set to 1 for reading. The device acknowledges this event.
4. The device writes the MSDB byte of the addressed register. The controller must acknowledge this byte.
5. Finally, the device writes out the LSDB of the register.

The broadcast address cannot be used for reading.

表 7-8. Read Sequence

S	MSB	…	R/$\overline{W}$ (0)	ACK	MSB	…	LSB	ACK	Sr	MSB	…	R/$\overline{W}$ (1)	ACK	MSB	…	LSB	ACK	MSB	…	LSB	ACK
	Address byte セクション 7.5.2.2.1				Command byte セクション 7.5.2.2.2				Sr	Address byte セクション 7.5.2.2.1				MSDB				LSDB			
From controller				Target	From controller			Target	From controller				Target	From target			Controller	From target			Controller

7.6 Register Maps

表 7-9. Register Map

REGISTER	MOST SIGNIFICANT DATA BYTE (MSDB)								LEAST SIGNIFICANT DATA BYTE (LSDB)							
	BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
NOP	NOP															
DAC-X-VOUT-CMP-CONFIG	X			VOUT-X-GAIN			X					CMP-X-OD-EN	CMP-X-OUT-EN	CMP-X-HIZ-IN-DIS	CMP-X-INV-EN	CMP-X-EN
COMMON-CONFIG	RESERVED	DEV-LOCK	RESERVED	EN-INT-REF	VOUT-PDN-0		RESERVED							VOUT-PDN-1		RESERVED
COMMON-TRIGGER	DEV-UNLOCK				RESET		RESERVED								NVM-PROG	NVM-RELOAD
FUNCTION-TRIGGER	RESERVED															START-FUNCTION
GENERAL-STATUS	NVM-CRC-FAIL-INT	NVM-CRC-FAIL-USER	X	DAC-0-BUSY	X		DAC-1-BUSY	NVM-BUSY	DEVICE-ID							
DEVICE-MODE-CONFIG	RESERVED		DIS-MODE-IN	RESERVED						SM-IO-EN	RESERVED					
INTERFACE-CONFIG	X			TIMEOUT-EN	RESERVED									FAST-SDO-EN	X	SDO-EN
STATE-MACHINE-CONFIG	RESERVED													SM-ABORT	SM-START	SM-EN
SRAM-CONFIG	X								SRAM-ADDR							
SRAM-DATA	SRAM-DATA															
FUNCTION-CONFIG	RESERVED					FUNC-SELECT			RESERVED	CODE-STEP			TIME-STEP			
FUNCTION-MAX	FUNCTION-MAX										X					
FUNCTION-MIN	FUNCTION-MIN										X					
GPI-DEBOUNCE	DEBOUNCE-DELAY															
VOUT-DATA-X	VOUT-DATA-X										X					
PWM-FREQUENCY-ERROR	RESERVED										FREQUENCY-ERROR					

Note: Shaded cells indicate the register bits or fields that are stored in NVM.

Note: X = Don't care.

表 7-10. Register Names

I²C/SPI ADDRESS	SRAM ADDR	REGISTER NAME	SECTION
00h	--	NOP	セクション 7.6.1
15h	--	DAC-0-VOUT-CMP-CONFIG	セクション 7.6.2
03h	--	DAC-1-VOUT-CMP-CONFIG	セクション 7.6.2
1Fh	--	COMMON-CONFIG	セクション 7.6.3
20h	--	COMMON-TRIGGER	セクション 7.6.4
21h	--	FUNCTION-TRIGGER	セクション 7.6.5
22h	--	GENERAL-STATUS	セクション 7.6.6
25h	--	DEVICE-MODE-CONFIG	セクション 7.6.7
26h	--	INTERFACE-CONFIG	セクション 7.6.8
27h	--	STATE-MACHINE-CONFIG	セクション 7.6.9
2Bh	--	SRAM-CONFIG	セクション 7.6.10
2Ch	--	SRAM-DATA	セクション 7.6.11
--	20h	FUNCTION-CONFIG	セクション 7.6.12
--	21h	FUNCTION-MAX	セクション 7.6.13
--	22h	FUNCTION-MIN	セクション 7.6.14
--	23h	GPI-DEBOUNCE	セクション 7.6.15
--	24h	VOUT-DATA-0	セクション 7.6.16
--	25h	VOUT-DATA-1	セクション 7.6.16
--	26h	VOUT-DATA-2	セクション 7.6.16
--	27h	VOUT-DATA-3	セクション 7.6.16
--	28h	VOUT-DATA-4	セクション 7.6.16
--	29h	VOUT-DATA-5	セクション 7.6.16
--	2Ah	VOUT-DATA-6	セクション 7.6.16
--	2Bh	VOUT-DATA-7	セクション 7.6.16
--	9Eh	PWM-FREQUENCY-ERROR	セクション 7.6.17

7.6.1 NOP Register (address = 00h) [reset = 0000h]

図 7-15. NOP Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NOP															
R/W-0000h															

表 7-11. NOP Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	NOP	R/W	0000h	No operation

7.6.2 DAC-X-VOUT-CMP-CONFIG Register (address = 15h, 03h) [reset = 0400h]

図 7-16. DAC-X-VOUT-CMP-CONFIG Register (X = 0, 1)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X			VOUT-GAIN-X			X					CMP-X-OD-EN	CMP-X-OUT-EN	CMP-X-HIZ-IN-DIS	CMP-X-INV-EN	CMP-X-EN
X-0h			R/W-0h			X-00h					R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

表 7-12. DAC-X-VOUT-CMP-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	X	X	0h	Don't care.
12-10	VOUT-GAIN-X	R/W	001	001: Gain = 1 ×, VDD as reference. 010: Gain = 1.5 ×, internal reference. 011: Gain = 2 ×, internal reference. 100: Gain = 3 ×, internal reference. 101: Gain = 4 ×, internal reference. Others: NA.
9-5	X	X	0h	Don't care.
4	CMP-X-OD-EN	R/W	0	1: Set OUTx pin as open-drain in comparator mode (CMP-X-EN = 1 and CMP-X-OUT-EN = 1). 0: Set OUTx pin as push-pull.
3	CMP-X-OUT-EN	R/W	0	1: Bring comparator output to the respective OUTx pin. 0: Generate comparator output but consume internally.
2	CMP-X-HIZ-IN-DIS	R/W	0	0: FBx input has high-impedance. Input voltage range is limited. 1: FBx input is connected to resistor divider and has finite impedance. Input voltage range is same as full-scale.
1	CMP-X-INV-EN	R/W	0	1: Invert the comparator output. 0: Don't invert the comparator output.
0	CMP-X-EN	R/W	0	1: Enable comparator mode. 0: Disable comparator mode.

7.6.3 COMMON-CONFIG Register (address = 1Fh) [reset = 03F9h]

図 7-17. COMMON-CONFIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	DEV-LOCK	RESERVED	EN-INT-REF	VOUT-PDN-0		RESERVED							VOUT-PDN-1		RESERVED
R/W-0	R/W-0	R/W-0	R/W-0	R/W-00		R/W-7Fh							R/W-00		R/W-1

表 7-13. COMMON-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0	Always write 0.
14	DEV-LOCK	R/W	0	0: Device not locked 1: Device locked, the device locks all the registers. To set this bit back to 0 (unlock device), write to the unlock code to the DEV-UNLOCK field in the COMMON-TRIGGER register first, followed by a write to the DEV-LOCK bit as 0.
13	RESERVED	R/W	0	Always write 0.
12	EN-INT-REF	R/W	0	0: Disable internal reference 1: Enable internal reference. This bit must be set before using internal reference gain settings.
11-10	VOUT-PDN-0	R/W	00	00: Power-up VOUT-0. 01: Power-down VOUT-0 with 10 kΩ to AGND. 10: Power-down VOUT-0 with 100 kΩ to AGND. 11: Power-down VOUT-0 with Hi-Z to AGND.
9-3	RESERVED	R/W	7Fh	Always write 7Fh.
2-1	VOUT-PDN-1	R/W	00	00: Power-up VOUT-1. 01: Power-down VOUT-1 with 10 kΩ to AGND. 10: Power-down VOUT-1 with 100 kΩ to AGND. 11: Power-down VOUT-1 with Hi-Z to AGND.
0	RESERVED	R/W	1	Always write 1.

7.6.4 COMMON-TRIGGER Register (address = 20h) [reset = 0000h]

図 7-18. COMMON-TRIGGER Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEV-UNLOCK				RESET				RESERVED						NVM-PROG	NVM-RELOAD
R/W-0h				R/W-0h				R/W-00h						R/W-0h	R/W-0h

表 7-14. COMMON-TRIGGER Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	DEV-UNLOCK	R/W	0000	0101: Device unlocking password. Others: Don't care.
11-8	RESET	R/W	0000	1010: POR reset triggered. This field self-resets. Others: Don't care.
7-2	RESERVED	R/W	00h	Always write 00h.
1	NVM-PROG	R/W	0	0: NVM write not triggered. 1: NVM write triggered. This bit self-resets.
0	NVM-RELOAD	R/W	0	0: NVM reload not triggered. 1: Reload data from NVM to register map. This bit self-resets.

7.6.5 FUNCTION-TRIGGER Register (address = 21h) [reset = 0001h]

図 7-19. FUNCTION-TRIGGER Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															START-FUNCTION
R/W-0000h															R/W-0h

表 7-15. FUNCTION-TRIGGER Register Field Descriptions

Bit	Field	Type	Reset	Description
15-1	RESERVED	R/W	0000h	Always write 0.
0	START-FUNCTION	R/W	0	0: Stop function generation. 1: Start function generation as per the settings in the FUNCTION-CONFIG register.

7.6.6 GENERAL-STATUS Register (address = 22h) [reset = 2068h]

図 7-20. GENERAL-STATUS Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NVM-CRC-FAIL-INT	NVM-CRC-FAIL-USER	X	DAC-0-BUSY	X		DAC-1-BUSY	NVM-BUSY	DEVICE-ID						VERSION-ID	
R-0h	R-0h	X-1h	R-0h	X-0h		R-0h	R-0h	R-1Ah						R-0h	

表 7-16. GENERAL-STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	NVM-CRC-FAIL-INT	R	0	0: No CRC error in OTP. 1: Indicates a failure in OTP loading. A software reset or power-cycle brings the device out of this condition in case of temporary failure.
14	NVM-CRC-FAIL-USER	R	0	0: No CRC error in NVM loading. 1: Indicates a failure in NVM loading. The register settings are corrupted. The device allows all operations during this error condition. Reprogram the NVM to get the original state. A software reset brings the device out of this error condition.
13	X	X	1	Don't care.
12	DAC-0-BUSY	R	0	0: DAC-0 channel accepts commands. 1: DAC-0 channel does not accept commands.
11-10	X	X	0	Don't care.
9	DAC-1-BUSY	R	0	0: DAC-1 channel accepts commands. 1: DAC-1 channel does not accept commands.
8	NVM-BUSY	R	0	0: NVM is available for read and write. 1: NVM is not available for read or write.
7-2	DEVICE-ID	R	1Ah	Device identifier.
1-0	VERSION-ID	R	00	Version identifier.

7.6.7 DEVICE-MODE-CONFIG Register (address = 25h) [reset = 8040h]

図 7-21. DEVICE-MODE-CONFIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		DIS-MODE-IN	RESERVED						SM-IO-EN	RESERVED					
R/W-10		R/$\overline{W}$-0	R/W-00h						R/$\overline{W}$-1	R/W-00h					

表 7-17. DEVICE-MODE-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R/W	10	Always write 10.
13	DIS-MODE-IN	R/W	0	0: MODE function enabled. 1: MODE function disabled.
12-7	RESERVED	R/W	00h	Always write 00h.
6	SM-IO-EN	R/W	1	0: The state machine does not have control over the digital input-output. 1: Digital input-output controlled by the state machine.
5-0	RESERVED	R/W	00h	Always write 00h.

7.6.8 INTERFACE-CONFIG Register (address = 26h) [reset = 0000h]

図 7-22. INTERFACE-CONFIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X			TIMEOUT-EN	X									FSDO-EN	X	SDO-EN
X-0h			R/W-0h	X-0h									R/W-0h	X-0h	R/W-0h

表 7-18. INTERFACE-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	X	X	0h	Don't care.
12	TIMEOUT-EN	R/W	0	0: I^2C timeout disabled. 1: I^2C timeout enabled.
11-3	X	X	0h	Don't care.
2	FSDO-EN	R/W	0	0: Fast SDO disabled. 1: Fast SDO enabled.
1	X	X	0	Don't care.
0	SDO-EN	R/W	0	0: SDO disabled. 1: SDO enabled.

7.6.9 STATE-MACHINE-CONFIG Register (address = 27h) [reset = 0003h]

図 7-23. STATE-MACHINE-CONFIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													SM-ABORT	SM-START	SM-EN
R/W-0000h													R/W-0h	R/W-1	R/W-1

表 7-19. STATE-MACHINE-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-3	RESERVED	R/W	0000h	Always write 0000h.
2	SM-ABORT	R/W	0	0: State machine not aborted. 1: State machine aborted.
1	SM-START	R/W	1	0: State machine stopped. 1: State machine started. The state machine must be enabled using the SM-EN bit.
0	SM-EN	R/W	1	0: State machine disabled. 1: State machine enabled.

7.6.10 SRAM-CONFIG Register (address = 2Bh) [reset = 0000h]

図 7-24. SRAM-CONFIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X								SRAM-ADDR							
X-00h								R/ W-00h							

表 7-20. SRAM-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	X	X	00h	Don't care.
7-0	SRAM-ADDR	R/W	00h	8-bit SRAM address. Writing to this register field configures the SRAM address to be accessed next. This address automatically increments after a read or write from the SRAM.

7.6.11 SRAM-DATA Register (address = 2Ch) [reset = 0000h]

図 7-25. SRAM-DATA Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRAM-DATA															
R/ W-0000h															

表 7-21. SRAM-DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	SRAM-DATA	R/W	0000h	16-bit SRAM data. This data is written to or read from the address configured in the SRAM-CONFIG register.

7.6.12 FUNCTION-CONFIG Register (SRAM address = 20h) [reset = 007Ah]

注

This register address is mapped to SRAM. Use the SRAM-CONFIG and SRAM-DATA registers to read and write.

図 7-26. FUNCTION-CONFIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					FUNC-SELECT			RESERVED	CODE-STEP			TIME-STEP			
R/W-00h					R/W-000			R/W-0	R/W-111			R/W-Ah			

表 7-22. FUNCTION-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R/W	00h	Always write 0.
10-8	FUNC-SELECT	R/W	000	000: Triangular wave. 001: Sawtooth wave. 010: Inverse sawtooth wave. 111: Disable function generation. Others: Invalid.
7	RESERVED	R/W	0	Always write 0.
6-4	CODE-STEP	R/W	111	000: 1 LSB. 001: 2 LSB. 010: 3 LSB. 011: 4 LSB. 100: 6 LSB. 101: 8 LSB. 110: 16 LSB. 111: 32 LSB.
3-0	TIME-STEP	R/W	Ah	0000: Invalid. 0001: 4 µs/step. 0010: 8 µs/step. 0011: 12 µs/step. 0100: 18 µs/step. 0101: 27.04 µs/step. 0110: 40.48 µs/step. 0111: 60.72 µs/step. 1000: 91.12 µs/step. 1001: 136.72 µs/step. 1010: 239.2 µs/step. 1011: 418.64 µs/step. 1100: 732.56 µs/step. 1101: 1282 µs/step. 1110: 2563.92 µs/step. 1111: 5127.92 µs/step.

7.6.13 FUNCTION-MAX Register (SRAM address = 21h) [reset = B900h]

注

This register address is mapped to SRAM. Use the SRAM-CONFIG and SRAM-DATA registers to read and write.

図 7-27. FUNCTION-MAX Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FUNCTION-MAX										X					
R/W-2E4h										X-00h					

表 7-23. FUNCTION-MAX Register Field Descriptions

Bit	Field	Type	Reset	Description
15-6	FUNCTION-MAX	R/W	2E4h	Maximum DAC code for the function generator. Data are in straight-binary format.
5-0	X	X	00h	Don't care

7.6.14 FUNCTION-MIN Register (SRAM address = 22h) [reset = 1900h]

注

This register address is mapped to SRAM. Use the SRAM-CONFIG and SRAM-DATA registers to read and write.

図 7-28. FUNCTION-MIN Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FUNCTION-MIN										X					
R/W-064h										X-00h					

表 7-24. FUNCTION-MIN Register Field Descriptions

Bit	Field	Type	Reset	Description
15-6	FUNCTION-MIN	R/W	064h	Minimum DAC code for the function generator. Data are in straight-binary format.
5-0	X	X	00h	Don't care

7.6.15 GPI-DEBOUNCE Register (SRAM address = 23h) [reset = 0138h]

注

This register address is mapped to SRAM. Use the SRAM-CONFIG and SRAM-DATA registers to read and write.

図 7-29. GPI-DEBOUNCE Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEBOUNCE-DELAY															
R/W-0138h															

表 7-25. GPI-DEBOUNCE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	DEBOUNCE-DELAY	R/W	0138h	Debounce delay for the GPI pins. Set to 0 to disable the delay. Delay (sec) = (DEBOUNCE-DELAY) x 160 µs.

7.6.16 VOUT-DATA-X Register (SRAM address = 24h to 2Bh) [reset = see 表 7-26]

注

This register address is mapped to SRAM. Use the SRAM-CONFIG and SRAM-DATA registers to read and write.

図 7-30. VOUT-DATA-X Register (X = 0, 1, 2, 3, 4, 5, 6, 7)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VOUT-DATA-X										X					
R/W										X-0h					

表 7-26. VOUT-DATA-X Register Field Descriptions

Bit	Field	Type	Reset	Description
15-6	VOUT-DATA-X	R/W	VOUT-DATA-0: 0E4h VOUT-DATA-1: 265h VOUT-DATA-2: 164h VOUT-DATA-3: 1E5h VOUT-DATA-4: 0E4h VOUT-DATA-5: 265h VOUT-DATA-6: 164h VOUT-DATA-7: 1E5h	Look up table values for DAC output as per the GPI pins. Data are in straight-binary format.
5-0	X	X	0h	Don't care

7.6.17 PWM-FREQUENCY-ERROR Register (SRAM address = 9Eh) [reset = device-specific]

注

This register address is mapped to SRAM. Use the SRAM-CONFIG and SRAM-DATA registers to read and write.

図 7-31. PWM-FREQUENCY-ERROR Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										FREQUENCY-ERROR					
R-000h										R-00h					

表 7-27. PWM-FREQUENCY-ERROR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-6	RESERVED	R	000h	Reserved field. Readback value can depend on device revision.
5-0	FREQUENCY-ERROR	R	Device-specific	Oscillator frequency error for the given device. The error resolution is ±0.2%.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The DAC539G2-Q1 is a dual-channel, buffered, force-sense output, voltage-output smart DAC that includes an NVM and internal reference, and is available in a tiny 3-mm × 3-mm package. The FBx pins function as inputs in comparator mode. The device is configured as an application-specific, look-up table (LUT) based GPI-to-PWM converter. One DAC channel is configured in voltage-output mode, and the other is configured as a comparator for PWM output. Three digital inputs control an internal LUT to select between eight configurable 10-bit DAC codes on the voltage output. The comparator channel is configured for a triangle or sawtooth waveform that sets the threshold of the comparator. Connect the LUT output to the FB0 input of the comparator to achieve the PWM output from the comparator output. The PWM frequency error is stored in the device and is calibrated out by adjusting the triangle- or sawtooth-wave frequency. The LUT values are programed using I^2C or SPI and stored in the NVM. The GPIs are multiplexed with other digital pins. The MODE pin determines whether the device is in programming or standalone mode.

8.2 Typical Application

This design uses a dual-channel, buffered voltage output smart DAC to decode three GPIs into a constant-frequency PWM output with eight selectable duty-cycle levels. In this design, the integrated buffer acts as a comparator, and a triangle or sawtooth waveform generated by the device acts as the threshold for the comparator. The DAC539G2-Q1 output buffers have an exposed feedback path through the feedback pin (FBx), which acts as the voltage input to the comparator. The comparator generates a PWM output with the same frequency as the triangle or sawtooth wave, and a duty cycle that depends on the FBx input. Use this circuit in applications such as automotive rear lights, rear light fault indication, and fault communication in factory automation and control designs. 図 8-1 shows how to connect the two DAC outputs to achieve a PWM output.

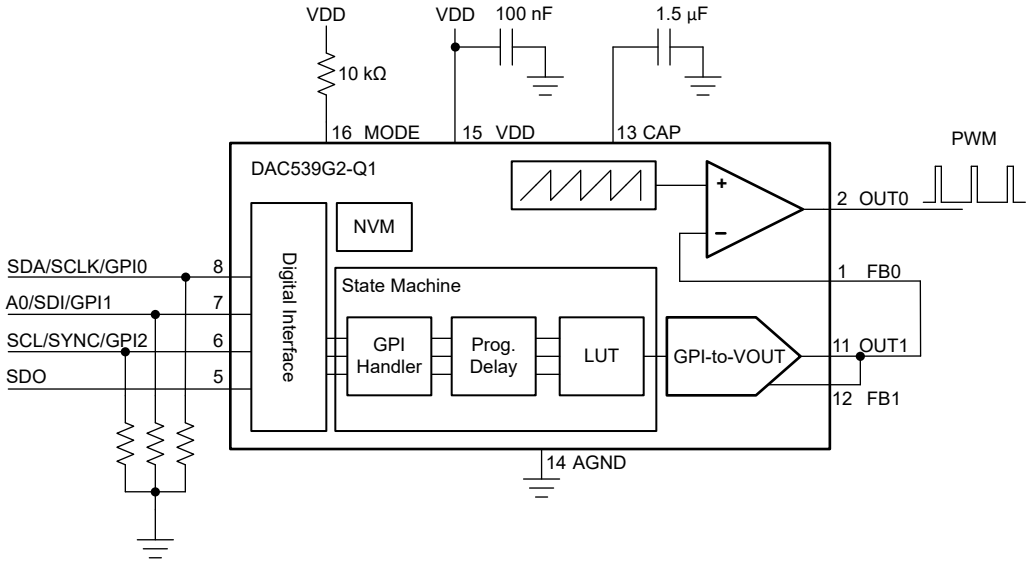


図 8-1. GPI to PWM

8.2.1 Design Requirements

表 8-1. Design Parameters

PARAMETER	VALUE
Frequency	100 Hz
Duty cycle	12.5%, 25%, 37.5%, 50%, 62.5%, 75%, 87.5%, 100%
Delay	50 ms

8.2.2 Detailed Design Procedure

Calculate the PWM frequency by using the time steps and code step from 表 7-22, either 式 4 for a triangle wave or 式 5 for a sawtooth wave, and the selected FUNCTION-MAX and FUNCTION-MIN DAC codes. セクション 7.4.2.1 describes the details on the function generation settings. The FUNCTION-MAX and FUNCTION-MIN DAC codes represent the peaks of the triangle or sawtooth waveforms. To achieve a frequency of 100 Hz, this example uses a triangle wave with a margin high of 725, a margin low of 100, slew rate of 8 µs, and code step of 1 LSB:

$$f_{TRIANGLE} = \frac{1}{2 \times 8\,\mu s \times CEILING\left(\frac{725-100}{1}\right)} = 100\,Hz \tag{7}$$

The DAC539G2-Q1 is a 10-bit device, which means the maximum DAC code is 1023d. Choose margin-high and -low values that are away from the endpoints to avoid effects from the zero-code and full-scale errors.

For small step sizes, the duty cycles can be estimated by:

$$Duty\_Cycle_{TRIANGLE} = \frac{FUNCTION\_MAX - VOUT\_DATA\_X}{CEILING\left(\frac{FUNCTION\_MAX - FUNCTION\_MIN}{CODE\_STEP}\right)} = 100\,Hz \tag{8}$$

Where VOUT_DATA_X is the DAC code set in the LUT for every combination of the GPI inputs (VOUT-DATA-X).

For a duty cycle duty cycle of 12.5%, the VOUT_DATA_X is calculated by:

$$VOUT\_DATA\_X_{TRIANGLE} = FUNCTION\_MAX - CEILING\left(\frac{FUNCTION\_MAX - FUNCTION\_MAX}{CODE\_STEP}\right) \times Duty\_Cycle = 725 - 2 \times CEILING\left(\frac{725-100}{1}\right) \times 0.125 = 646.88 \tag{9}$$

This result is rounded up to 647d (0x287). 表 8-2 lists the LUT table values for the remaining duty cycles.

表 8-2. LUT Codes

DUTY CYCLE	VOUT_DATA_X
12.5%	0x287
25%	0x239
37.5%	0x1EB
50%	0x19D
62.5%	0x14E
75%	0x100
87.5%	0x0B2
100%	0x064

The LUT codes are written to the DAC outputs depending on the state of the three GPI pins. The DAC codes do not have to increase chronologically with the GPIs. A programmable delay can be used so that the DAC output changes only after the GPIs have settled to avoid any switching noise on the output. The delay setting is 16 bits

with a step size of 160 µs, and is stored in the GPI-DEBOUNCE SRAM register. Set the delay code to 312d for a 50-ms delay.

The oscillator error is directly reflected on the output frequency of the PWM signal. This error can be compensated for by adjusting the margin-high and -low codes to adjust the frequency of the triangle wave generated on channel 0. The DAC539G2-Q1 oscillator error is stored in SRAM register 0x9E. This error is a 6-bit value with a code step of 0.2%, so the margin-high and -low codes can be modified to correct for –6.4% to +6.2% of error. For example, for code 0x2C, the oscillator error is –4%, or the frequency is 4% higher than the target. Increase the margin high – margin low differential value so that the calculated frequency is 4% lower than the target value.

Follow these guidelines to set up the registers on the DAC539G2-Q1:

- Stop the state machine before updating the application parameters by writing 0 to the STATE-MACHINE-CONFIG register.
- Set all of the application parameters shown in 表 8-3. These locations must be used to save the settings in the NVM. For example, the DAC register locations for FUNCTION-CONFIG, FUNCTION-MAX, and FUNCTION-MIN are not mapped to the NVM and are not saved when an NVM write is triggered.
- If the function generator is already running, the function generator must be stopped before any changes to the triangle wave take effect. Write a 0 to the START-FUNC field in the COMMON-DAC-TRIG register (0x21) to stop the function generator. The function generator is automatically started when the state machine is enabled.
- VOUT-DATA-0 and VOUT-DATA-7 correspond to the three GPIs being set to 0b000 and 0b111, respectively.
- Configure the reference for both channels in the DAC-X-VOUT-CMP-CONFIG register. Set the reference for channel 1 to the same reference chosen for channel 0.
- Configure DAC channel 0 in triangle-wave mode with the chosen slew rate and code step in the FUNCTION-CONFIG SRAM register.
- Set the margin-high and margin-low codes for the channel 0 triangle wave in the FUNCTION-MAX and FUNCTION-MIN SRAM registers, respectively.
- Power on the DAC outputs in voltage mode using the COMMON-CONFIG register.
- Set the DEVICE-MODE-CONFIG register to 0x8040.
- Start the state machine by writing 3d to the STATE-MACHINE-CONFIG.
- Trigger an NVM write by setting the NVM-PROG bit in the COMMON-TRIGGER register (0x20) to 1.

表 8-3. Application Parameters

REGISTER FIELD NAME	ADDRESS [FIELD]	ADDRESS LOCATION
FUNCTION-CONFIG	0x20[10:9][6:0]	SRAM
FUNCTION-MAX	0x21[15:6]	SRAM
FUNCTION-MIN	0x22[15:6]	SRAM
GPI-DEBOUNCE	0x23[15:0]	SRAM
VOUT-DATA-0	0x24[15:6]	SRAM
VOUT-DATA-1	0x25[15:6]	SRAM
VOUT-DATA-2	0x26[15:6]	SRAM
VOUT-DATA-3	0x27[15:6]	SRAM
VOUT-DATA-4	0x28[15:6]	SRAM
VOUT-DATA-5	0x29[15:6]	SRAM
VOUT-DATA-6	0x2A[15:6]	SRAM
VOUT-DATA-7	0x2B[15:6]	SRAM
DAC-0-VOUT-CMP-CONFIG	0x15[12:10][4:0]	Register
DAC-1-VOUT-CMP-CONFIG	0x03[12:10][4:0]	Register

表 8-3. Application Parameters (続き)

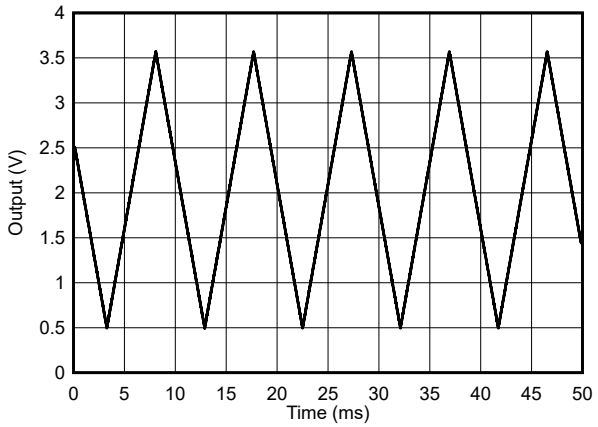
REGISTER FIELD NAME	ADDRESS [FIELD]	ADDRESS LOCATION
COMMON-CONFIG	0x1F[15:0]	Register
DEVICE-MODE-CONFIG	0x25[15:0]	Register
STATE-MACHINE-CONFIG	0x27[2:0]	Register

Only the bits listed in the address column of 表 8-3 are saved in NVM and used in the state machine. For example, only bits 12 to 10, and 4 to 0 are saved in NVM for the DAC-X-VOUT-CMP-CONFIG registers.

The pseudocode for this application example is as follows:

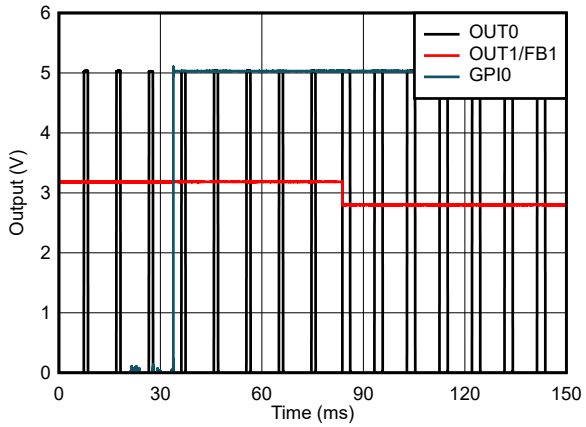
```
//SYNTAX: WRITE <REGISTER NAME(Hex Code)>, <MSB DATA>, <LSB DATA>
//Stop the state machine
WRITE STATE-MACHINE-CONFIG(0x27), 0x00, 0x03
//Stop the function generator
WRITE COMMON-DAC-TRIG(0x21), 0x00, 0x00
//Set the code step, slew rate, and waveform mode
WRITE FUNCTION-CONFIG(SRAM 0x20), 0x00, 0x02
WRITE FUNCTION-MAX(SRAM 0x21), 0xB5, 0x40
WRITE FUNCTION-MIN(SRAM 0x22), 0x19, 0x00
//Set the programmable debounce delay (this is the device default)
WRITE GPI-DEBOUNCE(SRAM 0x23), 0x01, 0x38
//Set the LUT values
WRITE VOUT-DATA-0(SRAM 0x24), 0xA1, 0xC0
WRITE VOUT-DATA-1(SRAM 0x25), 0x8E, 0x40
WRITE VOUT-DATA-2(SRAM 0x26), 0x7A, 0xC0
WRITE VOUT-DATA-3(SRAM 0x27), 0x67, 0x40
WRITE VOUT-DATA-4(SRAM 0x28), 0x53, 0x80
WRITE VOUT-DATA-5(SRAM 0x29), 0x40, 0x00
WRITE VOUT-DATA-6(SRAM 0x2A), 0x2C, 0x80
WRITE VOUT-DATA-7(SRAM 0x2B), 0x18, 0xC0
//Set the channel 0 reference to VDD (this is the device default)
WRITE DAC-0-VOUT-CMP-CONFIG(0x15), 0x04, 0x00
//Set channel 1 reference to VDD (this is the device default)
WRITE DAC-1-VOUT-CMP-CONFIG(0x03), 0x04, 0x00
//Power on the DAC channels (this is the device default)
WRITE COMMON-CONFIG(0x1F), 0x03, 0xF9
//Set the device mode (this is the device default)
WRITE DEVICE-MODE-CONFIG(0x25), 0x80, 0x40
//Start the state machine
WRITE STATE-MACHINE-CONFIG(0x27), 0x00, 0x03
//Save settings to NVM
WRITE COMMON-TRIGGER(0x20), 0x00, 0x02
```

8.2.3 Application Curves



The triangular waveform when OUT0 and FB0 are shorted

図 8-2. OUT0/FB0 Triangular Waveform



GPIs toggled from 000b to 001b

図 8-3. PWM Out: 12.5% to 25% Duty Cycle Transition

8.3 Power Supply Recommendations

The DAC539G2-Q1 does not require specific power-supply sequencing. These devices require a single power supply, V_{DD}. However, make sure the external voltage reference is applied after VDD. Use a 0.1-µF decoupling capacitor for the V_{DD} pin. Use a bypass capacitor with a value of approximately 1.5 µF for the CAP pin.

8.4 Layout

8.4.1 Layout Guidelines

The DAC539G2-Q1 pin configuration separates the analog, digital, and power pins for an optimized layout. For signal integrity, separate the digital and analog traces, and place decoupling capacitors close to the device pins.

8.4.2 Layout Example

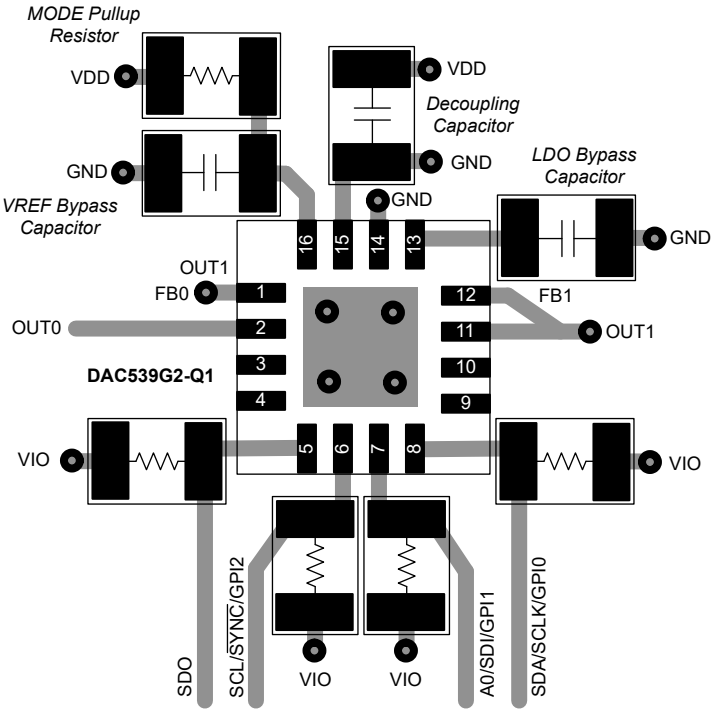


図 8-4. Layout Example

Note: The ground and power planes have been omitted for clarity. Connect the thermal pad to ground.

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

注

TI is transitioning to use more inclusive terminology. Some language may be different than what you would expect to see for certain technology areas.

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

9.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

9.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.6 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DAC539G2RTERQ1	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	539G2Q
DAC539G2RTERQ1.A	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	539G2Q
DAC539G2WRTERQ1	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	539G2Q
DAC539G2WRTERQ1.A	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	539G2Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

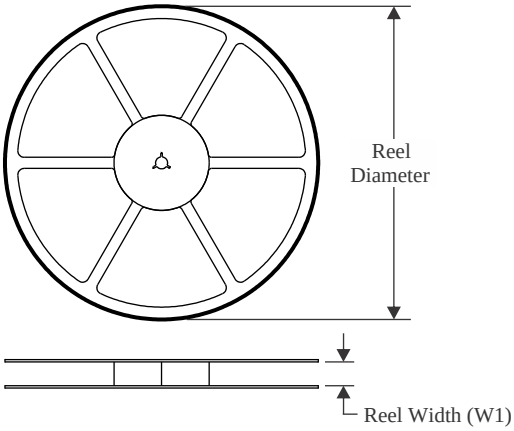
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

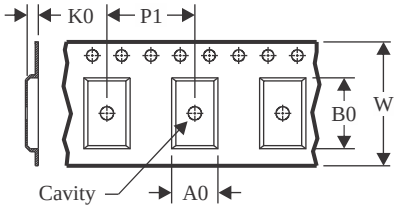
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

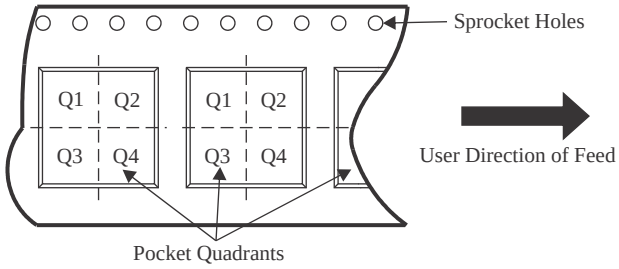


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

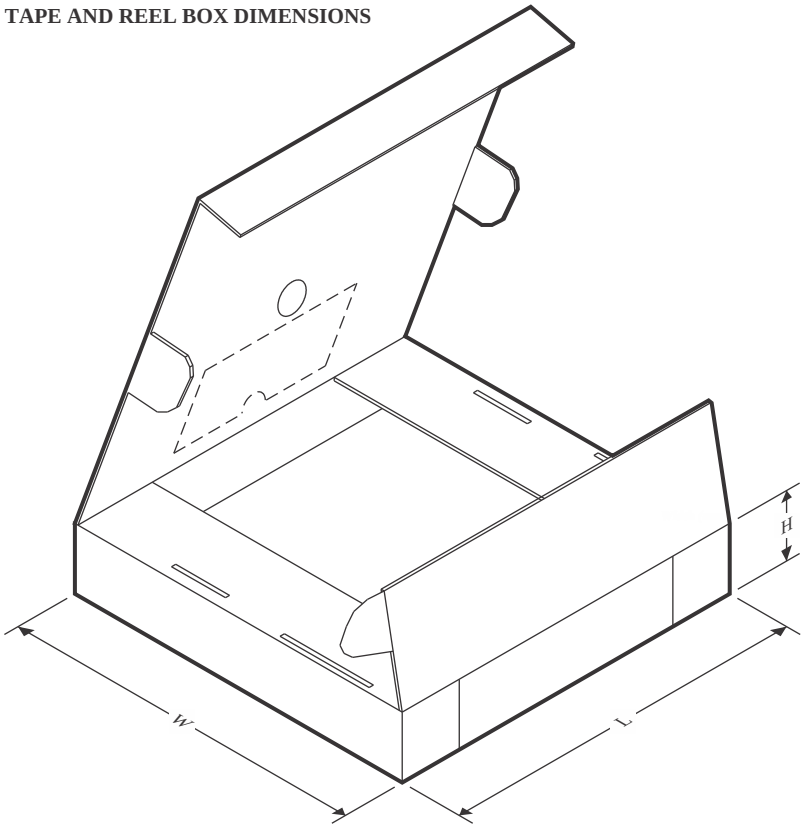
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC539G2RTERQ1	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
DAC539G2WRTERQ1	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC539G2RTERQ1	WQFN	RTE	16	3000	367.0	367.0	35.0
DAC539G2WRTERQ1	WQFN	RTE	16	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

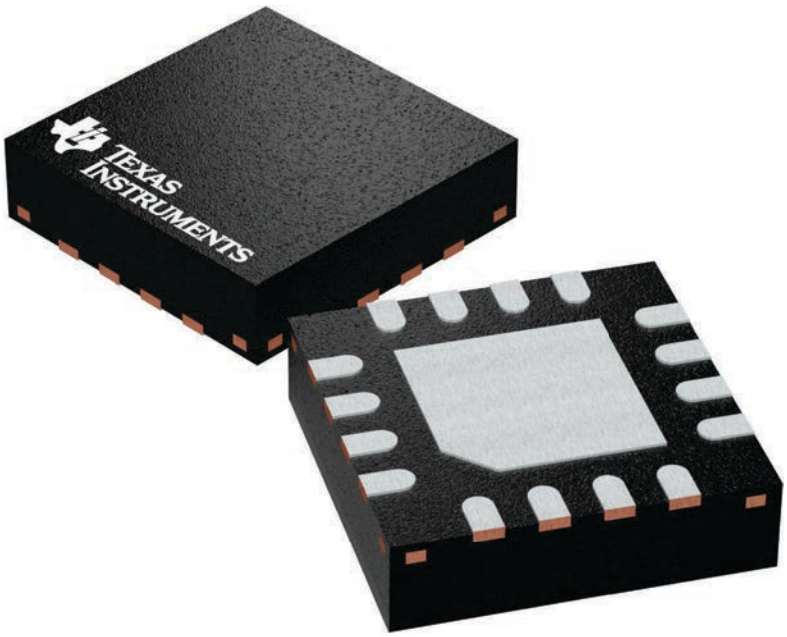
RTE 16

WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

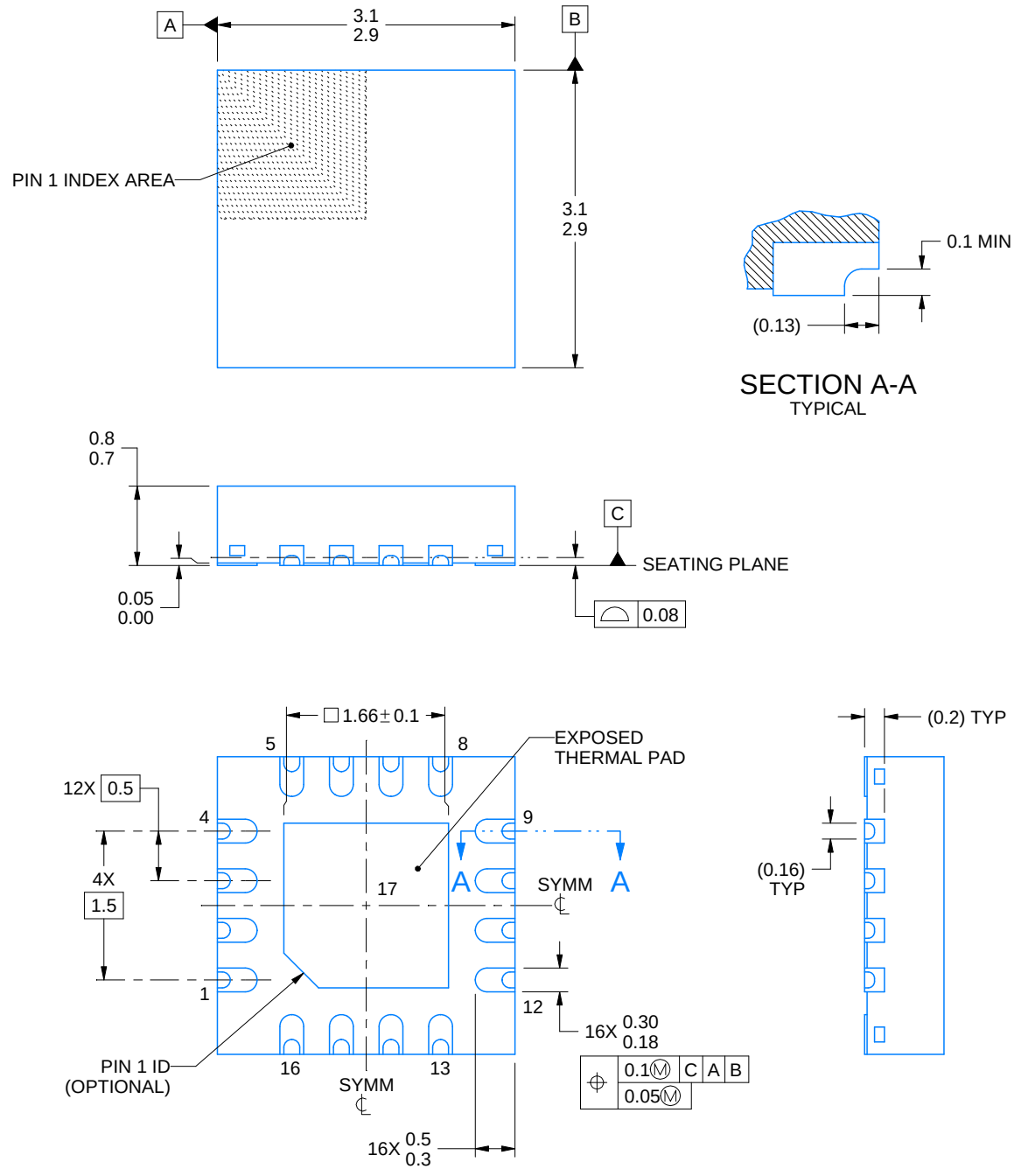


RTE0016K

PACKAGE OUTLINE

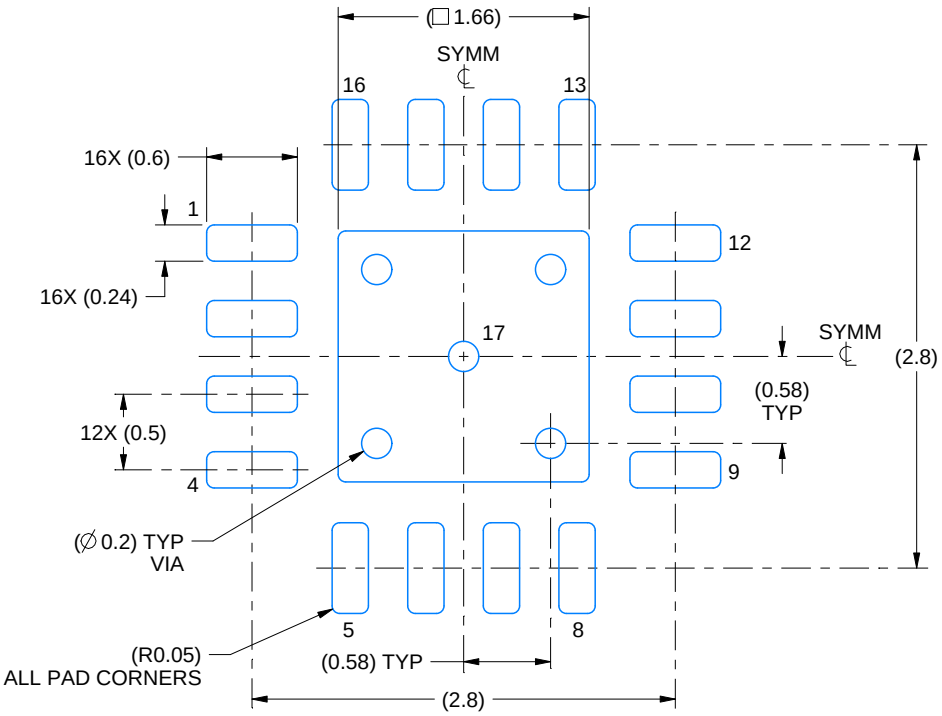
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

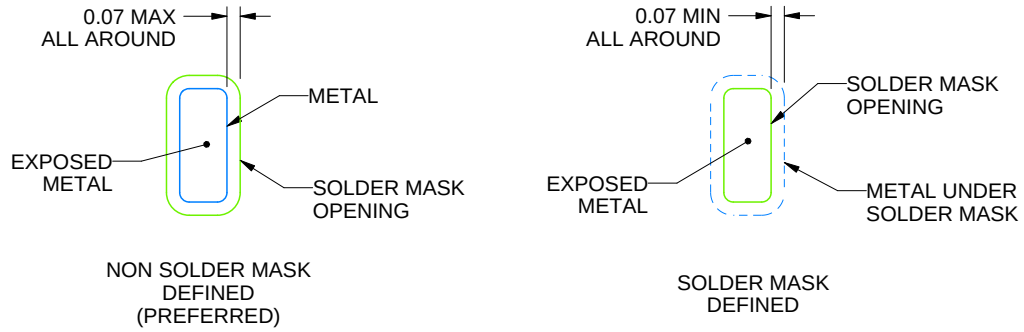


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

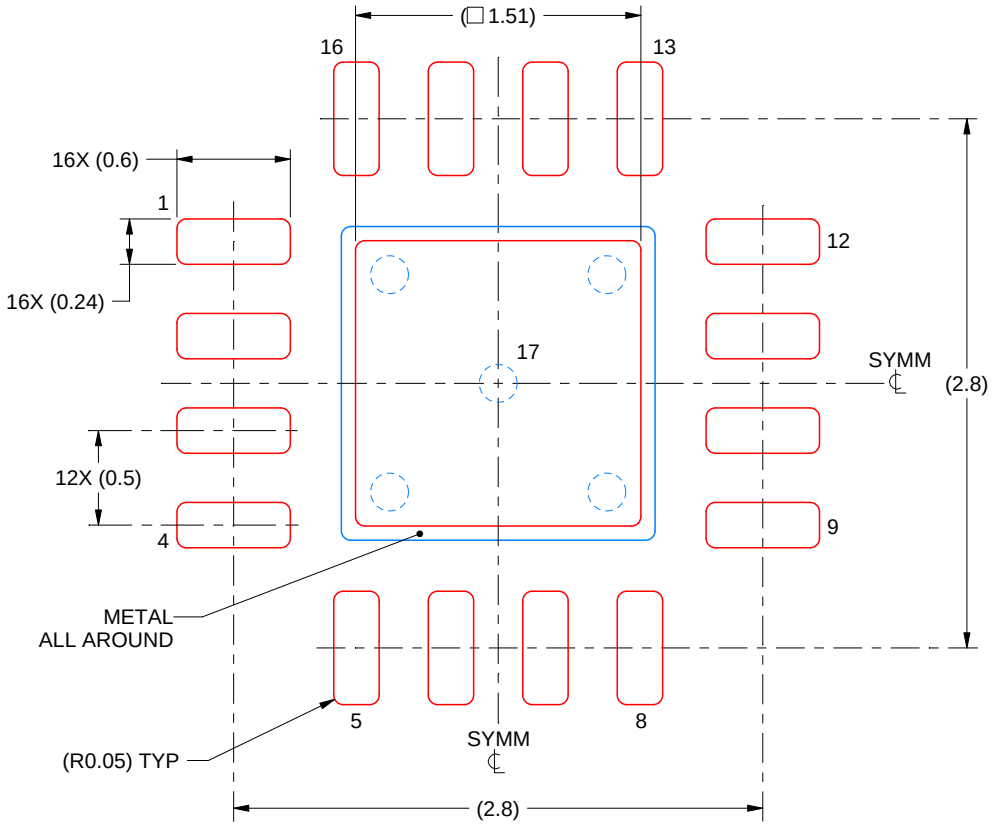


SOLDER MASK DETAILS

4224938/C 03/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
84% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4224938/C 03/2022

NOTES: (continued)

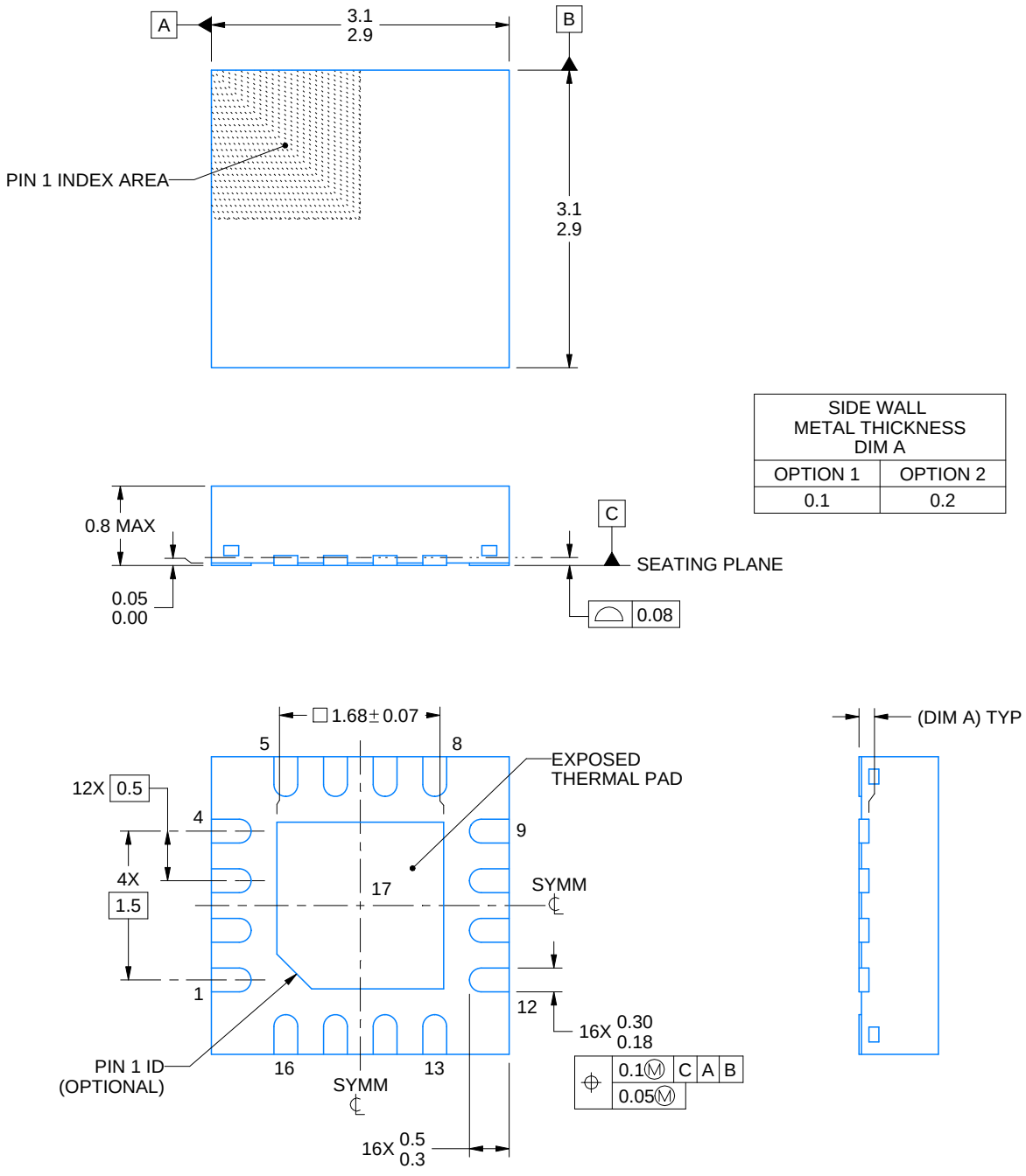
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

RTE0016C

PACKAGE OUTLINE

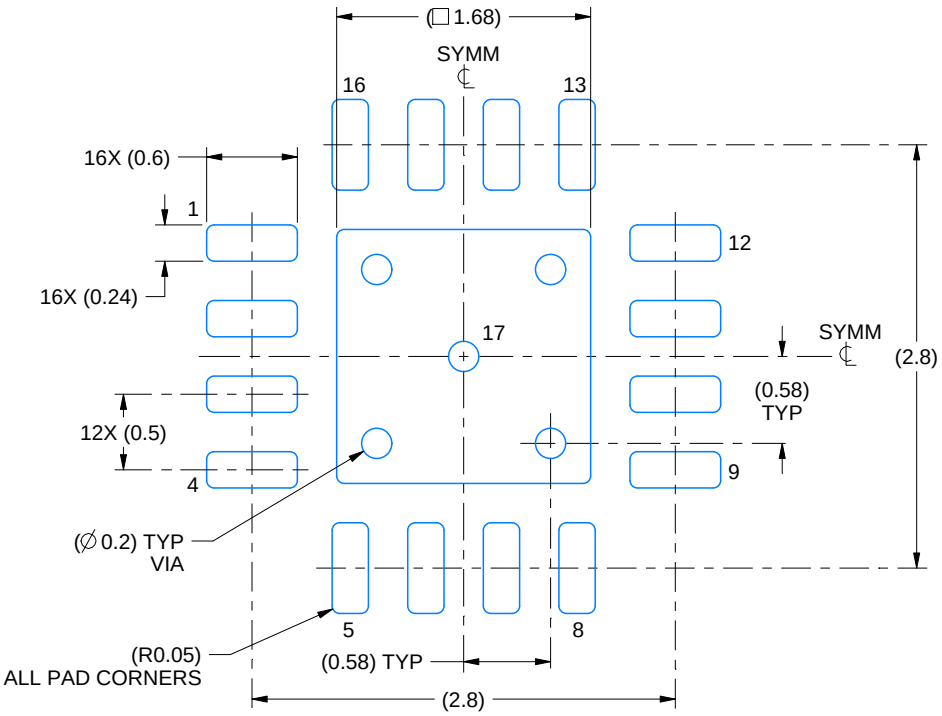
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

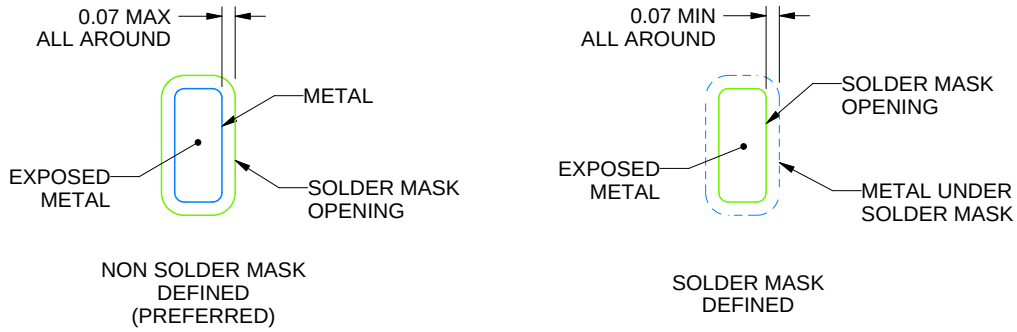


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

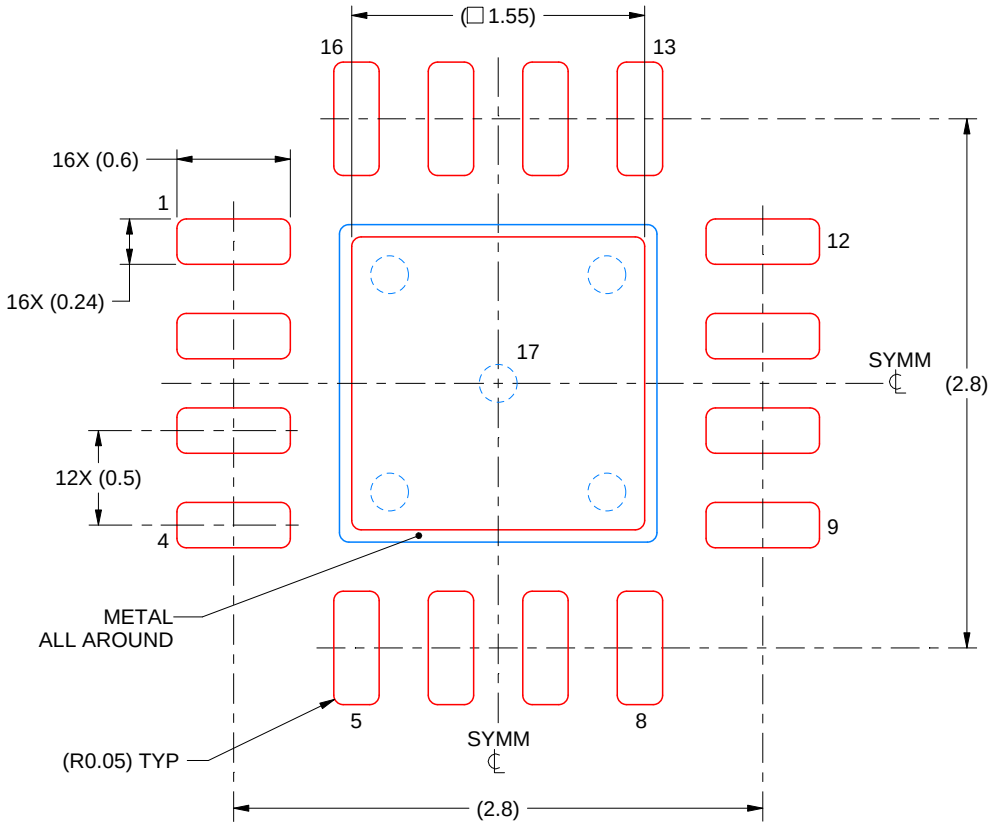


SOLDER MASK DETAILS

4219117/B 04/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219117/B 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、 TI の販売条件 、 TI の総合的な品質ガイドライン 、 ti.com または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。 TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

最終更新日：2025 年 10 月