DAC5662 デュアル、12 ビット、275MSPS D/A コンバータ

1 特長

- 12 ビットのデュアル伝送 DAC
- 更新速度:275MSPS
- 単電源:3V～3.6V
- 広い SFDR:85dBc (5MHz)
- 優れた IMD3 特性:78dBc (15.1MHz および 16.1MHz)
- WCDMA ACLR:70dB (30.72MHz)
- 独立または単一抵抗によるゲイン制御
- デュアル・データまたはインターリーブ・データ
- 1.2V のリファレンスを内蔵
- 低消費電力:330mW
- パワーダウン・モード:15mW
- パッケージ:48 ピン TQFP

2 アプリケーション

- 携帯電話基地局通信チャネル
  – CDMA:W-CDMA、CDMA2000、IS-95
  – TDMA:GSM、IS-136、EDGE/UWC-136
- 医療、テスト用計測機器
- 任意波形ジェネレータ (AWG)
- ダイレクト・デジタル・シンセシス (DDS)
- ケーブル・モデム終端システム (CMTS)

3 概要

DAC5662 は、オンチップの電圧リファレンスを内蔵したモノリシック、デュアル・チャネルの 12 ビット高速 D/A コンバータ (DAC) です。

最高 275MSPS の更新速度で動作し、抜群の動的性能、正確なゲイン、オフセット整合といった特性から、I/Q ベースバンドまたは直接 IF 通信アプリケーションに最適です。

各 DAC には、シングルエンドまたは差動アナログ出力構成に適した高インピーダンスの差動電流出力が備えられています。外部抵抗を使用して、各 DAC のフルスケール出力電流を別々に、または同時にスケーリングすることができます (一般的には 2mA～20mA)。高精度の内蔵電圧リファレンスは温度補償機能を備え、安定した 1.2V の電圧リファレンスを提供します。外部リファレンスも使用できます。

DAC5662 には、クロックとデータ・ラッチが異なる 12 ビットのパラレル入力ポートが 2 つあります。柔軟性を高めるため、インターリーブ・モードで動作する際には 1 ポートで各 DAC への多重化データもサポートされます。

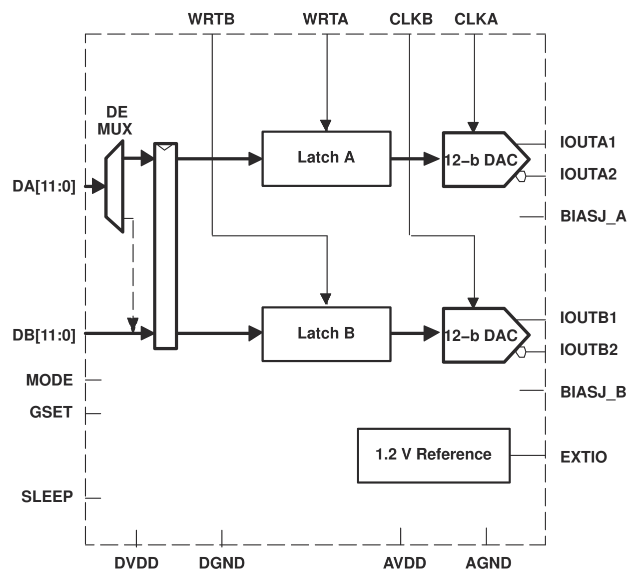
DAC5662 は、50Ω の二重終端負荷を接続した変圧器結合の差動出力用に設計されています。20mA のフルスケール出力電流の場合、インピーダンス比 4:1 (結果として出力 4dBm) と
インピーダンス比 1:1 の変圧器 (出力 -2dBm) をサポートします。

DAC5662 は、48 ピンの薄型クワッド・フラットパック (TQFP) で供給されます。ファミリ製品間にはピン互換性があり、12 ビット (DAC5662)、14 ビット (DAC5672) の分解能を選択できます。さらに、DAC5662 は DAC2902 および AD9765 デュアル DAC とピン互換です。このデバイスは、-40℃～85℃の工業用温度範囲で動作が規定されています。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
DAC5662	TQFP	7.00mm × 7.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



機能ブロック図

Table of Contents

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (October 2020) to Revision D (October 2021) **Page**

- 「*製品情報*」のデバイス番号を DAC566452 から DAC5662 に変更..1

Changes from Revision B (July 2004) to Revision C (October 2020) **Page**

- 「製品情報」表、「ESD 定格」表、「熱抵抗特性」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加..1

5 Pin Configurations and Functions

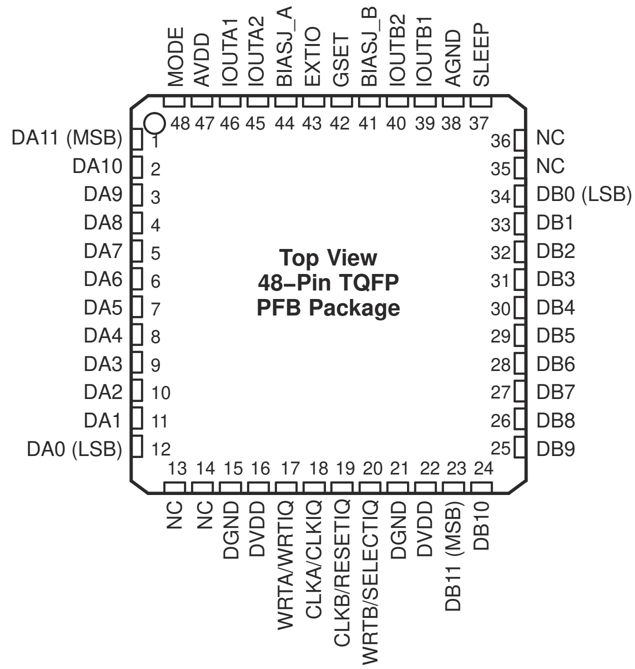


表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	38	I	Analog ground
AVDD	47	I	Analog supply voltage
BIASJ_A	44	O	Full-scale output current bias for DACA
BIASJ_B	41	O	Full-scale output current bias for DACB
CLKA/CLKIQ	18	I	Clock input for DACA, CLKIQ in interleaved mode.
CLKB/ RESETIQ	19	I	Clock input for DACB, RESETIQ in interleaved mode.
DA[11:0]	1-12	I	Data port A. DA11 is MSB and DA0 is LSB. Internal pulldown.
DB[11:0]	23-34	I	Data port B. DB11 is MSB and DB0 is LSB. Internal pulldown.
DGND	15, 21	I	Digital ground
DVDD	16, 22	I	Digital supply voltage
EXTIO	43	I/O	Internal reference output (bypass with 0.1 μF to AGND) or external reference input.
GSET	42	I	Gain-setting mode: H - 1 resistor, L - 2 resistors. Internal pullup.
IOUTA1	46	O	DACA current output. Full-scale with all bits of DA high.
IOUTA2	45	O	DACA complementary current output. Full-scale with all bits of DA low.
IOUTB1	39	O	DACB current output. Full-scale with all bits of DB high.
IOUTB2	40	O	DACB complementary current output. Full-scale with all bits of DB low.
MODE	48	I	Mode Select: H – Dual Bus, L – Interleaved. Internal pullup.
NC	13, 14, 35, 36	-	No connection
SLEEP	37	I	Sleep function control input: H – DAC in power-down mode, L – DAC in operating mode. Internal pulldown.
WRTA/WRTIQ	17	I	Input write signal for PORT A (WRTIQ in interleaving mode).
WRTB/ SELECTIQ	20	I	Input write signal for PORT B (SELECTIQ in interleaving mode).

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		Min	Max	UNIT
Supply voltage range	AVDD[2]	-0.5	4	V
	DVDD[3]	-0.5	4	V
Voltage between AGND and DGND		-0.5	0.5	V
Voltage between AVDD and DVDD		-0.5	0.5	V
Supply voltage range	DA[11:0] and DB[11:0][3]	-0.5	DVDD + 0.5	V
	MODE, SLEEP, CLKA, CLKB, WRTA, WRTB[3]	-0.5	DVDD + 0.5	V
	IOUTA1, IOUTA2, IOUTB1, IOUTB2[2]	-1	AVDD + 0.5	V
	EXTIO, BIASJ_A, BIASJ_B, GSET[2]	-0.5	AVDD + 0.5	V
Peak input current (any input)			+20	mA
Peak total input current (all inputs)			-30	mA
Operating free-air temperature range		-40	85	°C
Storage temperature range		-65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Measured with respect to AGND.
(3) Measured with respect to DGND.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

over operating free-air temperature range (unless otherwise noted)

6.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supplies				
AVDD	3	3.3	3.6	V
DVDD	3	3.3	3.6	V
$I_{(AVDD)}$ Analog supply current		75	90	mA
$I_{(DVDD)}$ Digital supply current		25	38	mA
Analog Output				
$I_{O(FS)}$ Full-Scale output current	2		20	mA
Output voltage compliance range	-1		1.25	V
Clock Interface (CLK, CLKC)				
CLKINPUT Frequency			275	MHz

6.4 Thermal Resistance Characteristics

THERMAL METRIC(1)		DAC5652 TQFP (PFB) 48-Pins	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	65.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	16.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	28.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	28.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

6.5 Electrical Characteristics

over operating free-air temperature range, AVDD = DVDD = 3.3 V, IOUTFS = 20 mA, independent gain set mode (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Specifications						
	Resolution		12			Bits
DC Accuracy(1)						
INL	Integral nonlinearity	1 LSB = $IOUT_{FS}/2^{12}$, T_A = 25°C	-2	±0.3	2	LSB
DNL	Differential nonlinearity	1 LSB = $IOUT_{FS}/2^{12}$, T_A = 25°C	-2	±0.2	2	LSB
Analog Output						
	Offset error			0.03		%FSR
	Gain error	With external reference		±0.25		%FSR
	Gain error	With internal reference		±0.5		%FSR
	Minimum full-scale output current(2)			2		mA
	Maximum full-scale output current(2)			20		mA
	Gain mismatch	With internal reference	-2	0.07	+2	%FSR
	Output voltage compliance range(3)		-1		1.25	V
R_O	Output resistance			300		kΩ
C_O	Output capacitance			5		pF
Reference Output						
	Reference voltage		1.14	1.2	1.26	V
	Reference output current(4)			100		nA
Reference Input						
V_{EXTIO}	Input voltage		0.1		1.25	V
R_I	Input resistance			1		MΩ
	Small signal bandwidth			300		kHz
C_I	Input capacitance			100		pF
Temperature Coefficients						
	Offset drift			0		ppm of FSR/°C
	Gain drift	With external reference		±50		ppm of FSR/°C
	Gain drift	With internal reference		±50		ppm of FSR/°C
	Reference voltage drift			±20		ppm/°C

(1) Measured differentially through 50 Ω to AGND.
(2) Nominal full-scale current, IOUTFS, equals 32x the IBIAS current.
(3) The lower limit of the output compliance is determined by the CMOS process. Exceeding this limit may result in transistor breakdown, resulting in reduced reliability of the DAC5662 device. The upper limit of the output compliance is determined by the load resistors and full-scale output current. Exceeding the upper limit adversely affects distortion performance and intergral nonlinearity.
(4) Use an external buffer amplifier with high impedance input to drive any external load.

6.6 Electrical Characteristics

over operating free-air temperature range, AVDD = DVDD = 3.3 V, IOUTFS = 20 mA, f_{DATA} = 200 MSPS, f_{OUT} = 1 MHz, independent gain set mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply						
AVDD	Analog supply voltage		3	3.3	3.6	V
DVDD	Digital supply voltage		3	3.3	3.6	V
I_{AVDD}	Supply current, analog	Including output current through load resistor		75	90	mA
		Sleep mode with clock		2.5	6	mA
		Sleep mode without clock		2.5		mA
I_{DVDD}	Supply current, digital			25	38	mA
		Sleep mode with clock		12.5	18	mA
		Sleep mode without clock		<10		μA
	Power dissipation			330	390	mW
		Sleep mode without clock		15		
		f_{DATA} = 275 MSPS, f_{OUT} = 20 MHz		350		
APSRR	Power supply rejection ratio		-0.2		0.2	%FSR/V
DPSRR			-0.2		0.2	
T_A	Operating free-air temperature		-40		85	°C

6.7 Electrical Characteristics, AC

AC specifications over operating free-air temperature range, AVDD = DVDD = 3.3 V, IOUTFS = 20 mA, independent gain set mode, differential 1:1 impedance ratio transformer coupled output, 50-Ω doubly terminated load (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analog Output						
f_{clk}	Maximum output update rate[(1)]		275			MSPS
t_s	Output settling time to 0.1% (DAC)	Mid-scale transition		20		ns
t_r	Output rise time 10% to 90% (OUT)			1.4		ns
t_f	Output fall time 90% to 10% (OUT)			1.5		ns
	Output noise	$IOUT_{FS}$ = 20 mA		55		pA/√Hz
		$IOUT_{FS}$ = 2 mA		30		pA/√Hz
AC Linearity						
SFDR	Spurious free dynamic range	1st Nyquist zone, T_A = 25°C, f_{DATA} = 50 MSPS, f_{OUT} = 1 MHz, IOUTFS = 0 dB		81		dBc
		1st Nyquist zone, T_A = 25°C, f_{DATA} = 50 MSPS, f_{OUT} = 1 MHz, IOUTFS = -6 dB		83		
		1st Nyquist zone, T_A = 25°C, f_{DATA} = 50 MSPS, f_{OUT} = 1 MHz, IOUTFS = -12 dB		81		
		1st Nyquist zone, T_A = 25°C, f_{DATA} = 100 MSPS, f_{OUT} = 5 MHz		85		
		1st Nyquist zone, T_A = 25°C, f_{DATA} = 100 MSPS, f_{OUT} = 20 MHz		78		
		1st Nyquist zone, T_{MIN} to T_{MAX}, f_{DATA} = 200 MSPS, f_{OUT} = 20 MHz	66	71		
		1st Nyquist zone, T_A = 25°C, f_{DATA} = 200 MSPS, f_{OUT} = 41 MHz		68		
		1st Nyquist zone, T_A = 25°C, f_{DATA} = 275 MSPS, f_{OUT} = 20 MHz		72		
SNR	Signal-to-noise ratio	1st Nyquist zone, T_A = 25°C, f_{DATA} = 100 MSPS, f_{OUT} = 5 MHz		73		dB
		1st Nyquist zone, T_A = 25°C, f_{DATA} = 200 MSPS, f_{OUT} = 20 MHz		67		
ACLR	Adjacent channel leakage ratio	W-CDMA signal with 3.84-MHz Bandwidth, f_{DATA} = 61.44 MSPS, IF = 15.360 MHz		70		dB
		W-CDMA signal with 3.84-MHz Bandwidth, f_{DATA} = 122.88 MSPS, IF = 30.72 MHz		70		
IMD3	Third-order two-tone intermodulation	Each tone at -6 dBFS, T_A = 25°C, f_{DATA} = 200 MSPS, f_{OUT} = 45.4 and 46.4 MHz		62		dBc
		Each tone at -6 dBFS, T_A = 25°C, f_{DATA} = 100 MSPS, f_{OUT} = 15.1 and 16.1 MHz		78		
IMD	Four-tone intermodulation	Each tone at -12 dBFS, T_A = 25°C, f_{DATA} = 100 MSPS, f_{OUT} = 15.6, 15.8, 16.2, and 16.4 MHz		77		dBc
		Each tone at -12 dBFS, T_A = 25°C, f_{DATA} = 165 MSPS, f_{OUT} = 68.8, 69.6, 71.2, and 72.0 MHz		56		
		Each tone at -12 dBFS, T_A = 25°C, f_{DATA} = 165 MSPS, f_{OUT} = 19.0, 19.1, 19.3, and 19.4 MHz		74		
	Channel isolation	T_A = 25°C, f_{DATA} = 165 MSPS, f_{OUT} (CH1) = 20 MHz, f_{OUT} (CH2) = 21 MHz		97		dBc

(1) Specified by design and bench characterization. Not production tested.

6.8 Electrical Characteristics, DC

Digital specifications over operating free-air temperature range, AVDD = DVDD = 3.3 V, IOUTFS = 20 mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Input						
V_{IH}	High-level input voltage		2		3.3	V
V_{IL}	Low-level input voltage		0		0.8	V
I_{IH}	High-level input current			±50		µA
I_{IL}	Low-level input current			±10		µA
$I_{IH(GSET)}$	High-level input current, GSET pin			7		µA
$I_{IL(GSET)}$	Low-level input current, GSET pin			-30		µA
$I_{IH(MODE)}$	High-level input current, MODE pin			-30		µA
$I_{IL(MODE)}$	Low-level input current, MODE pin			-80		µA
C_I	Input capacitance			5		pF

6.9 Switching Characteristics

Digital specifications over operating free-air temperature range, AVDD = DVDD = 3.3 V, IOUTFS = 20 mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Timing - Dual Bus Mode						
t_{su}	Input setup time		1			ns
t_h	Input hold time		1			ns
t_{LPH}	Input clock pulse high time			2		ns
t_{LAT}	Clock latency (WRTA/B to outputs)		4		4	clk
t_{PD}	Propagation delay time			1.5		ns
Timing - Single Bus Interleaved Mode						
t_{su}	Input setup time			0.5		ns
t_h	Input hold time			0.5		ns
t_{LAT}	Clock latency (WRTA/B to outputs)		4		4	clk
t_{PD}	Propagation delay time			1.5		ns

6.10 Typical Characteristics

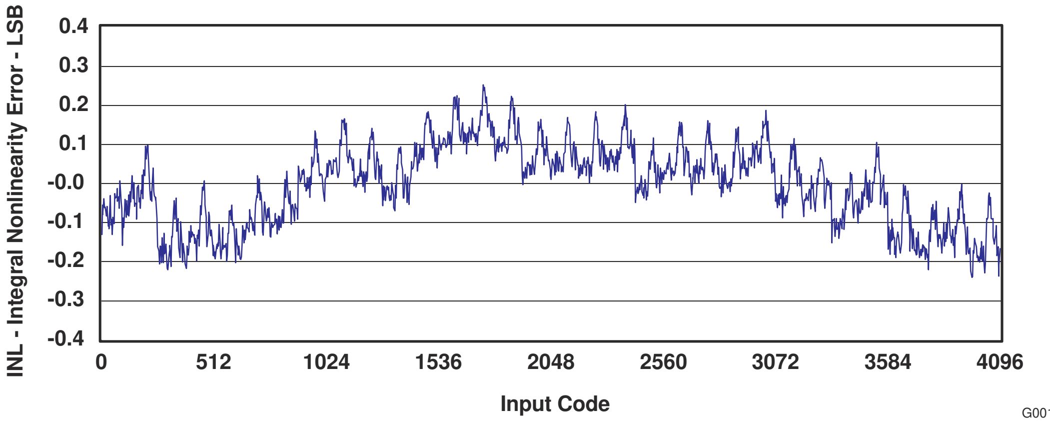


図 6-1. Integral Nonlinearity vs Input Code

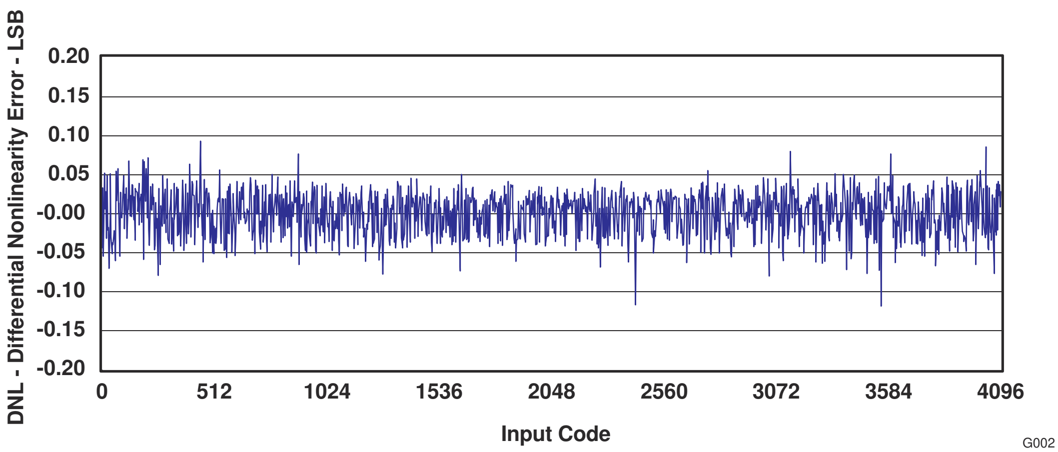


図 6-2. Differential Nonlinearity vs Input Code

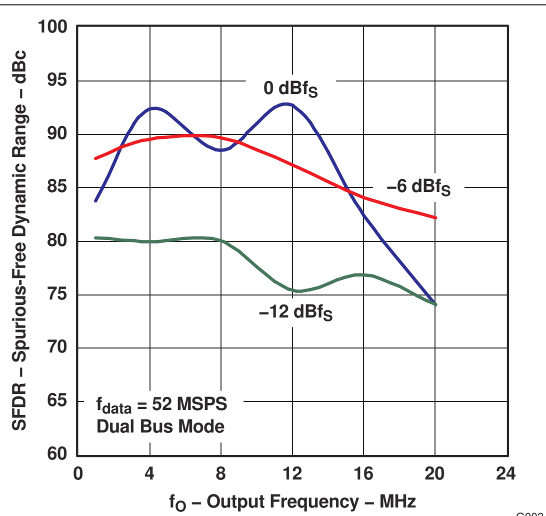


図 6-3. Spurious-Free Dynamic Range vs Output Frequency

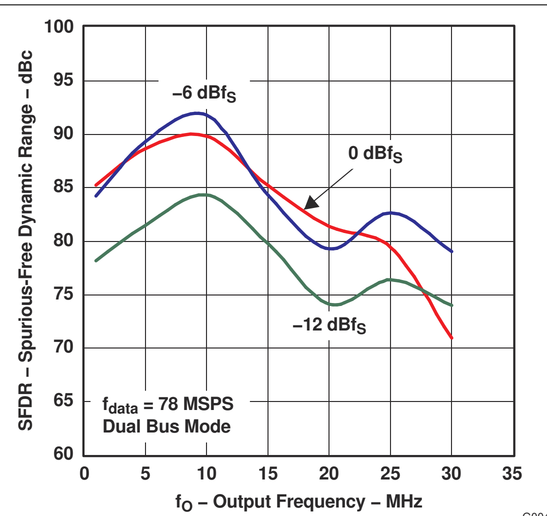


図 6-4. Spurious-Free Dynamic Range vs Output Frequency

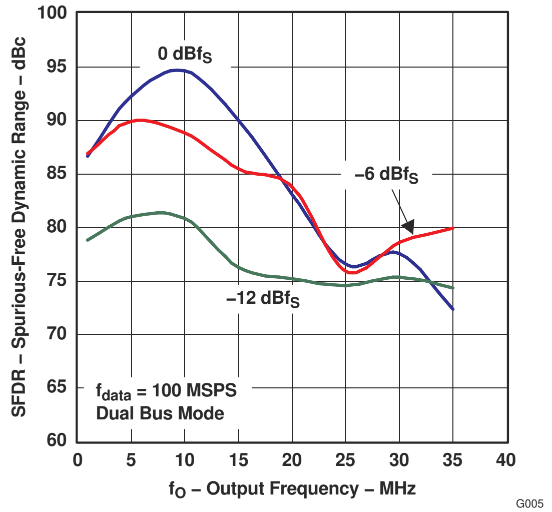


図 6-5. Spurious-Free Dynamic Range vs Output Frequency

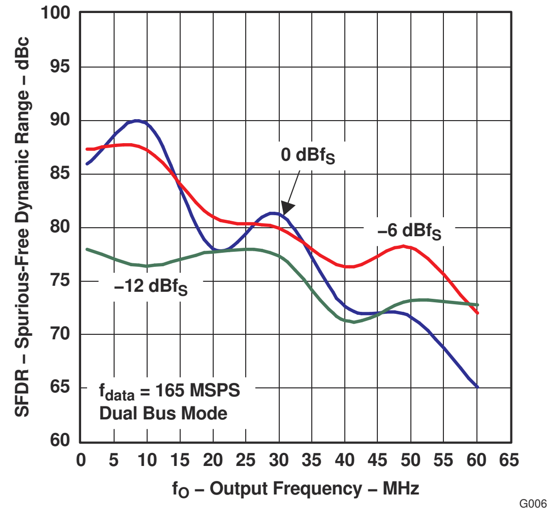


図 6-6. Spurious-Free Dynamic Range vs Output Frequency

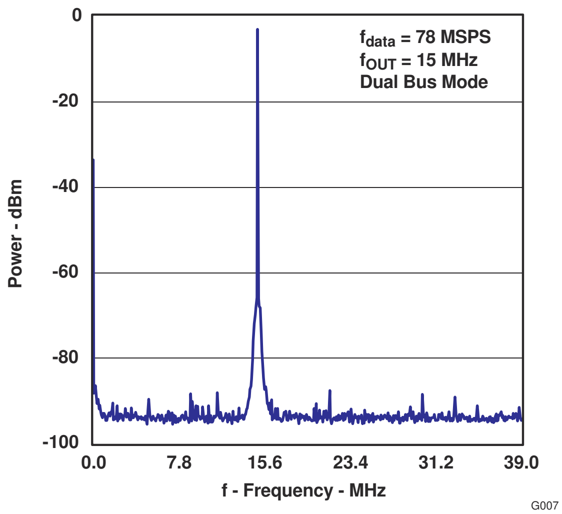


図 6-7. Single-Tone Spectrum

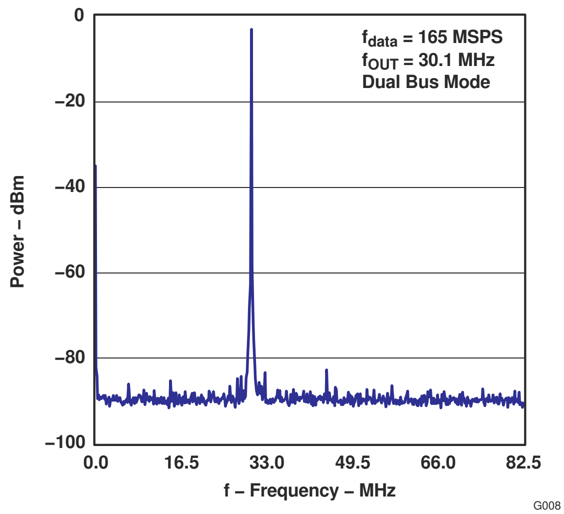


図 6-8. Single-Tone Spectrum

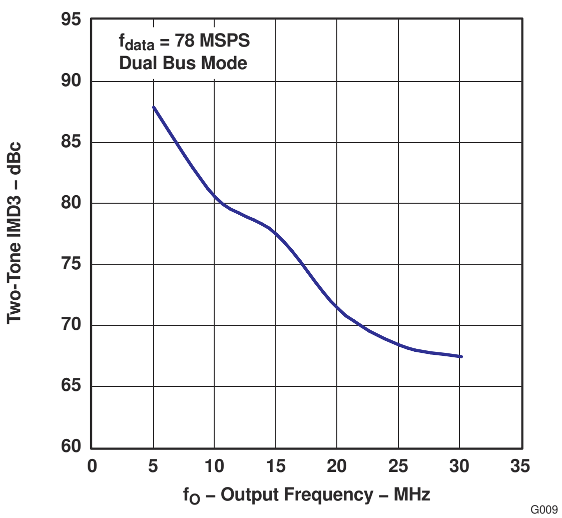


図 6-9. Two-Tone IMD3 vs Output Frequency

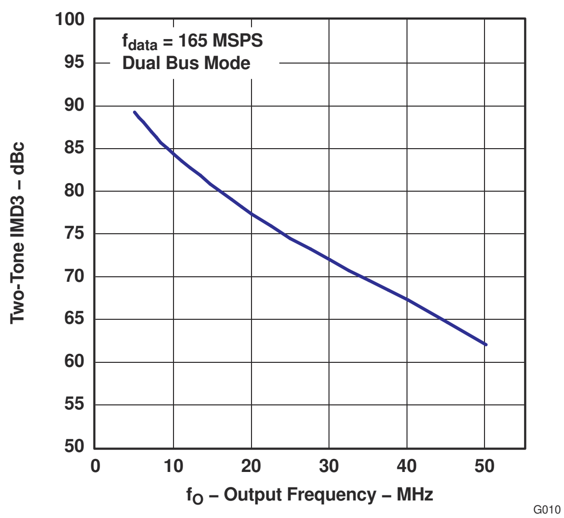


図 6-10. Two-Tone IMD3 vs Output Frequency

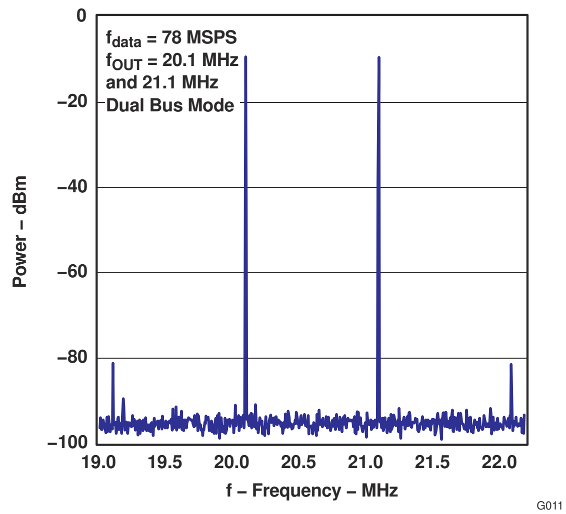


図 6-11. Two-Tone Spectrum

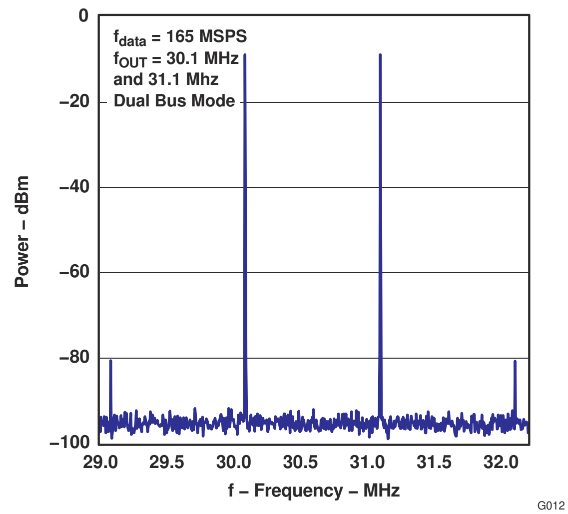


図 6-12. Two-Tone Spectrum

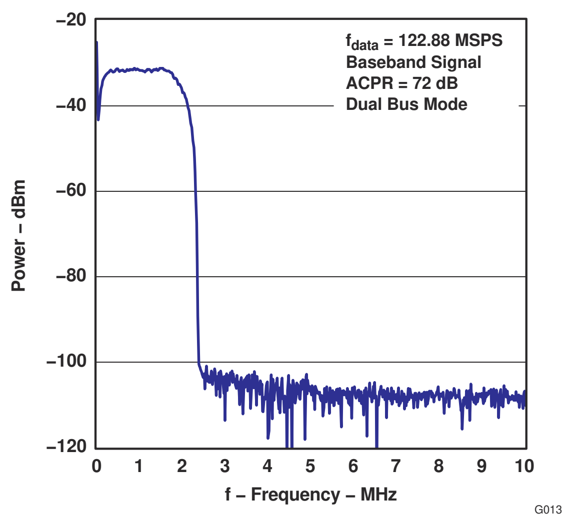


図 6-13. Power vs Frequency

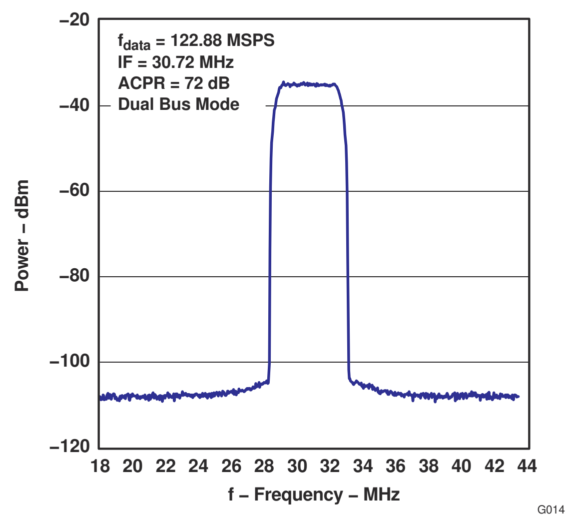


図 6-14. Power vs Frequency

7 Parameter Measurement Information

7.1 Digital Inputs and Timing

7.1.1 Digital Inputs

The data input ports of the DAC5662 accept a standard positive coding with data bit D11 being the most significant bit (MSB). The converter outputs support a clock rate of up to 275 MSPS. The best performance will typically be achieved with a symmetric duty cycle for write and clock; however, the duty cycle may vary as long as the timing specifications are met. Similarly, the setup and hold times may be chosen within their specified limits.

All digital inputs of the DAC5662 are CMOS compatible. 図 7-1 and 図 7-2 show schematics of the equivalent CMOS digital inputs of the DAC5662. The pullup and pulldown circuitry is approximately equivalent to 100kΩ. The 12-bit digital data input follows the offset positive binary coding scheme. The DAC5662 is designed to operate with a digital supply (DVDD) of 3 V to 3.6 V.

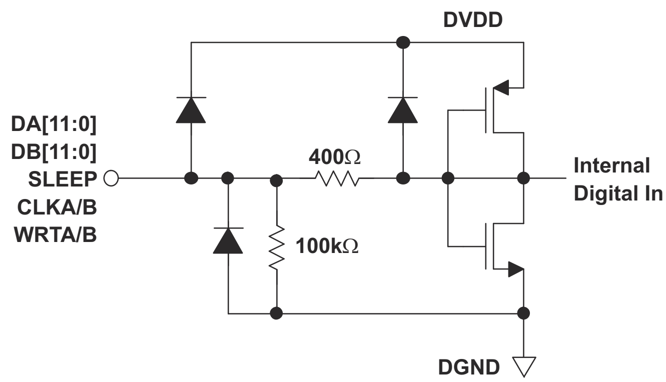


図 7-1. CMOS/TTL Digital Equivalent Input With Internal Pulldown Resistor

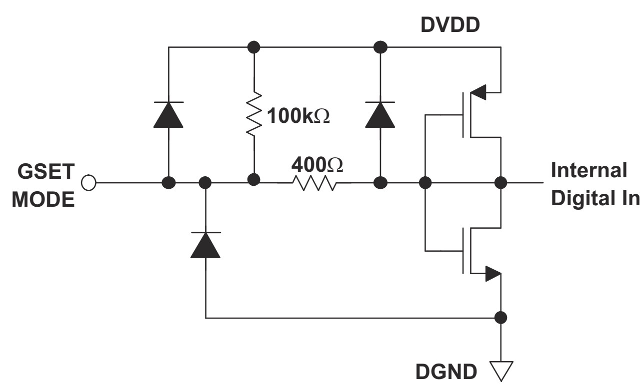


図 7-2. CMOS/TTL Digital Equivalent Input With Internal Pullup Resistor

7.1.2 Input Interfaces

The DAC5662 features two operating modes selected by the MODE pin, as shown in 表 7-1.

- For dual-bus input mode, the device essentially consists of two separate DACs. Each DAC has its own separate data input bus, clock input, and data write signal (data latch-in).
- In single-bus interleaved mode, the data should be presented interleaved at the I-channel input bus. The Q-channel input bus is not used in this mode. The clock and write input are now shared by both DACs.

表 7-1. Operating Modes

MODE PIN	Mode pin connected to DGND	Mode pin connected to DVDD
Bus input	Single-bus interleaved mode, clock and write input equal for both DACs	Dual-bus mode, DACs operate independently

7.1.3 Dual-Bus Data Interface and Timing

In dual-bus mode, the MODE pin is connected to DVDD. The two converter channels within the DAC5662 consist of two independent, 12-bit, parallel data ports. Each DAC channel is controlled by its own set of write (WRTA, WRTB) and clock (CLKA, CLKB) lines. The WRT lines control the channel input latches and the CLK lines control the DAC latches. The data is first loaded into the input latch by a rising edge of the WRT line

The internal data transfer requires a correct sequence of write and clock inputs, since essentially two clock domains having equal periods (but possibly different phases) are input to the DAC5662. This is defined by a minimum requirement of the time between the rising edge of the clock and the rising edge of the write inputs. This essentially implies that the rising edge of CLK must occur at the same time or before the rising edge of the WRT signal. A minimum delay of 2 ns should be maintained if the rising edge of the clock occurs after the rising edge of the write. Note that these conditions are satisfied when the clock and write inputs are connected externally. Note that all specifications were measured with the WRT and CLK lines connected together.

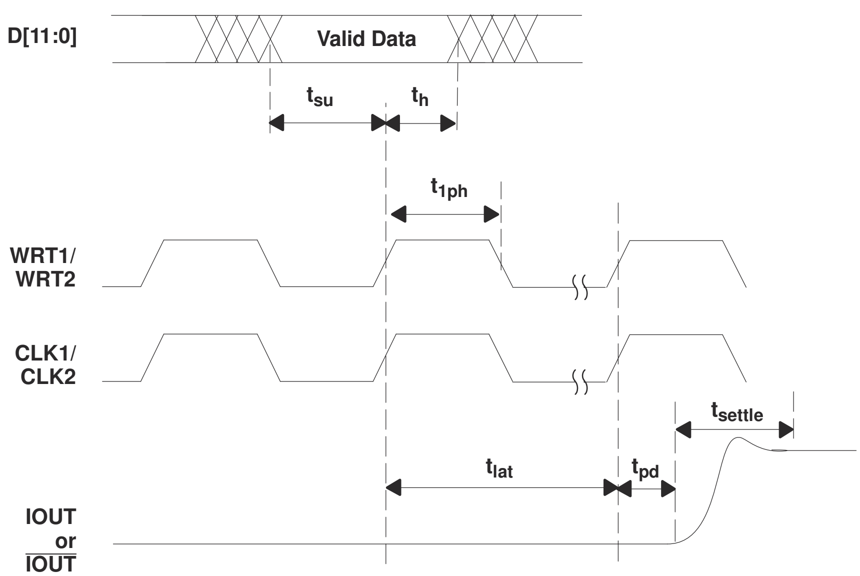


図 7-3. Dual Bus Mode Operation

7.1.4 Single-Bus Interleaved Data Interface and Timing

In single-bus interleaved mode, the MODE pin is connected to DGND. 図 7-4 shows the timing diagram. In interleaved mode, the I- and Q-channels share the write input (WRTIQ) and update clock (CLKIQ and internal CLKDACIQ). Multiplexing logic directs the input word at the I-channel input bus to either the I-channel input latch (SELECTIQ is high) or to the Q-channel input latch (SELECTIQ is low). When SELECTIQ is high, the data value in the Q-channel latch is retained by presenting the latch output data to its input again. When SELECTIQ is low, the data value in the I-channel latch is retained by presenting the latch output data to its input.

In interleaved mode, the I-channel input data rate is twice the update rate of the DAC core. As in dual-bus mode, it is important to maintain a correct sequence of write and clock inputs. The edge-triggered flip-flops latch the I- and Q-channel input words on the rising edge of the write input (WRTIQ). This data is presented to the I- and Q-DAC latches on the following falling edge of the write inputs. The DAC5662 clock input is divided by a factor of two before it is presented to the DAC latches.

Correct pairing of the I- and Q-channel data is done by RESETIQ. In interleaved mode, the clock input CLKIQ is divided by two, which would translate to a non-deterministic relation between the rising edges of the CLKIQ and CLKDACIQ. RESETIQ ensures, however, that the correct position of the rising edge of CLKDACIQ with respect to the data at the input of the DAC latch is determined. CLKDACIQ is disabled (low) when RESETIQ is high.

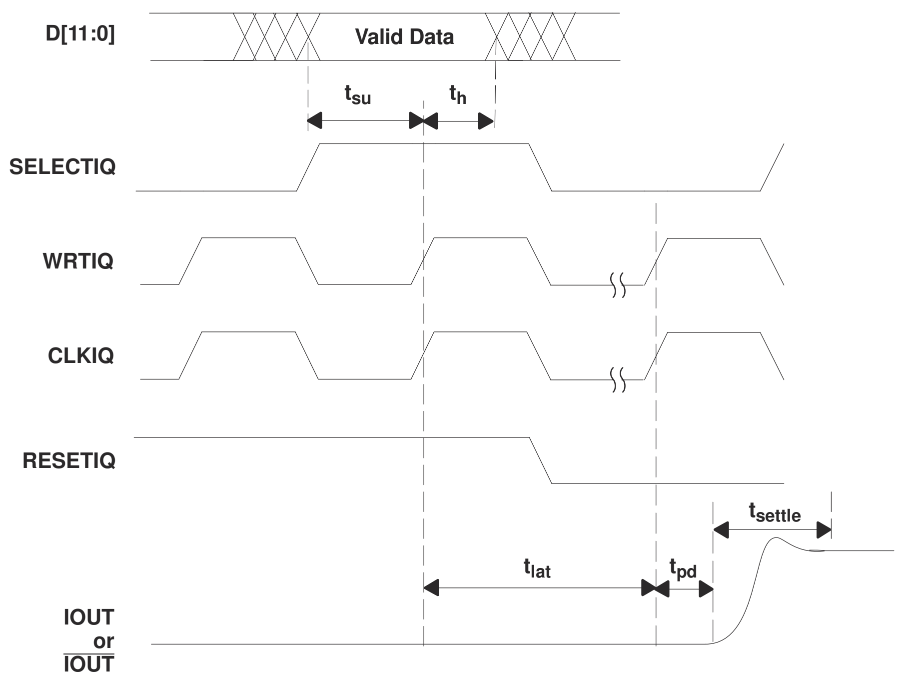


図 7-4. Single-Bus Interleaved Mode Operation

8 Detailed Description

8.1 Overview

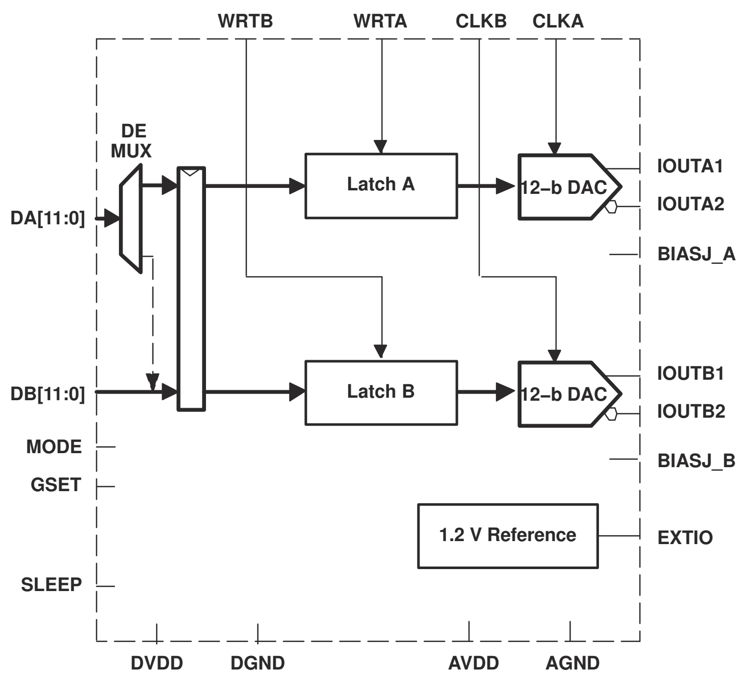
The architecture of the DAC5662 uses a current steering technique to enable fast switching and high update rate. The core element within the monolithic DAC is an array of segmented current sources that are designed to deliver a full-scale output current of up to 20 mA. An internal decoder addresses the differential current switches each time the DAC is updated and a corresponding output current is formed by steering all currents to either output summing node, IOUT1 and IOUT2. The complementary outputs deliver a differential output signal, which improves the dynamic performance through reduction of even-order harmonics, common-mode signals (noise), and double the peak-to-peak output signal swing by a factor of two, compared to single-ended operation.

The segmented architecture results in a significant reduction of the glitch energy, improves the dynamic performance (SFDR), and DNL. The current outputs maintain a high output impedance of greater than 300 kΩ.

When GSET is high (one resistor mode), the full-scale output current for both DACs is determined by the ratio of the internal reference voltage (1.2 V) and an external resistor RSET connected to BIASJ_A. When GSET is low (two resistor mode), the full-scale output current for each DACs is determined by the ratio of the internal reference voltage (1.2 V) and separate external resistors RSET connected to BIASJ_A and BIASJ_B. The resulting IREF is internally multiplied by a factor of 32 to produce an effective DAC output current that can range from 2 mA to 20 mA, depending on the value of RSET.

The DAC5662 is split into a digital and an analog portion, each of which is powered through its own supply pin. The digital section includes edge-triggered input latches and the decoder logic, while the analog section comprises the current source array with its associated switches, and the reference circuitry.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 DAC Transfer Function

Each of the DACs in the DAC5662 has a set of complementary current outputs, I_{OUT1} and I_{OUT2}. The full-scale output current, I_{OUTFS}, is the summation of the two complementary output currents:

$$I_{OUTFS} = I_{OUT1} + I_{OUT2} \quad (1)$$

The individual output currents depend on the DAC code and can be expressed as:

$$I_{OUT1} = I_{OUTFS} \times \left(\frac{Code}{4096}\right) \quad (2)$$

$$I_{OUT2} = I_{OUTFS} \times \left(\frac{4095 - Code}{4096}\right) \quad (3)$$

where Code is the decimal representation of the DAC data input word. Additionally, I_{OUTFS} is a function of the reference current I_{REF}, which is determined by the reference voltage and the external setting resistor (R_{SET}).

$$I_{OUTFS} = 32 \times I_{REF} = 32 \times \frac{V_{REF}}{R_{SET}} \quad (4)$$

In most cases, the complementary outputs drive resistive loads or a terminated transformer. A signal voltage develops at each output according to:

$$V_{OUT1} = I_{OUT1} \times R_{LOAD} \quad (5)$$

$$V_{OUT2} = I_{OUT2} \times R_{LOAD} \quad (6)$$

The value of the load resistance is limited by the output compliance specification of the DAC5662. To maintain specified linearity performance, the voltage for I_{OUT1} and I_{OUT2} should not exceed the maximum allowable compliance range.

The total differential output voltage is:

$$V_{OUTDIFF} = V_{OUT1} - V_{OUT2} \quad (7)$$

$$V_{OUTDIFF} = \frac{(2 \times Code - 4095)}{4096} \times I_{OUTFS} \times R_{LOAD} \quad (8)$$

8.3.1.1 Analog Outputs

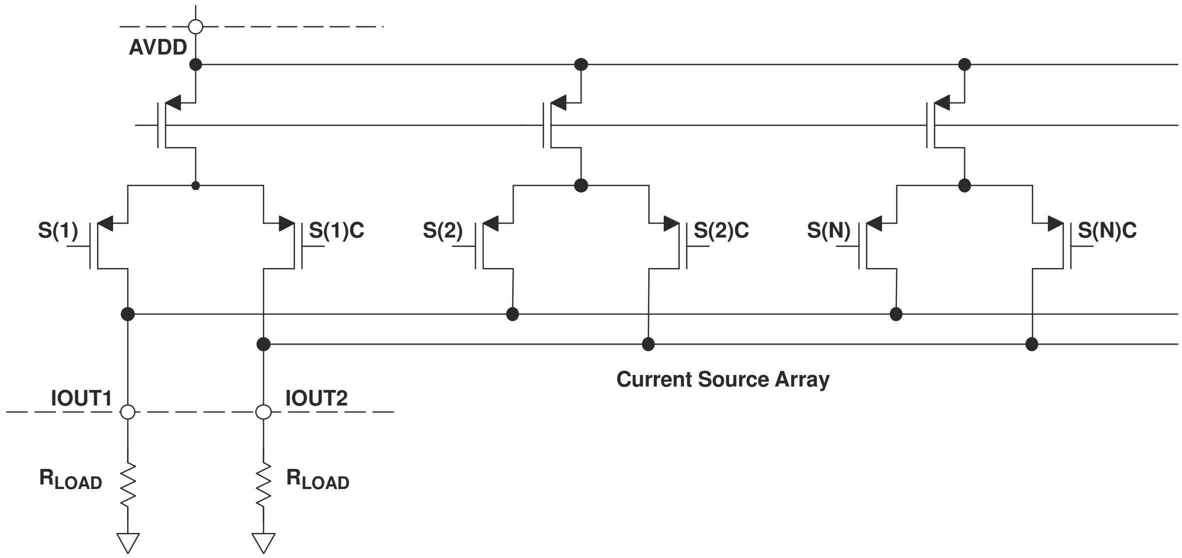


図 8-1. Analog Outputs

The DAC5662 provides two complementary current outputs, I_{OUT1} and I_{OUT2}. The simplified circuit of the analog output stage representing the differential topology is shown in 図 8-1. The output impedance of I_{OUT1} and I_{OUT2} results from the parallel combination of the differential switches, along with the current sources and associated parasitic capacitances.

The signal voltage swing that may develop at the two outputs, I_{OUT1} and I_{OUT2}, is limited by a negative and positive compliance. The negative limit of –1 V is given by the breakdown voltage of the CMOS process and exceeding it compromises the reliability of the DAC5662 or even causes permanent damage. With the full-scale output set to 20 mA, the positive compliance equals 1.2 V. Note that the compliance range decreases to about 1 V for a selected output current of I_{OUTFS} = 2 mA. Care should be taken that the configuration of DAC5662 does not exceed the compliance range to avoid degradation of the distortion performance and integral linearity.

Best distortion performance is typically achieved with the maximum full-scale output signal limited to approximately 0.5 Vpp. This is the case for a 50-Ω doubly terminated load and a 20-mA full-scale output current. A variety of loads can be adapted to the output of the DAC5662 by selecting a suitable transformer while maintaining optimum voltage levels at I_{OUT1} and I_{OUT2}. Furthermore, using the differential output configuration in combination with a transformer will be instrumental for achieving excellent distortion performance. Common-mode errors, such as even-order harmonics or noise, can be substantially reduced. This is particularly the case with high output frequencies.

For those applications requiring the optimum distortion and noise performance, it is recommended to select a full-scale output of 20 mA. A lower full-scale range of 2 mA may be considered for applications that require low power consumption, but can tolerate a slight reduction in performance level.

8.3.2 Output Configurations

The current outputs of the DAC5662 allow for a variety of configurations. As mentioned previously, utilizing the converter's differential outputs yield the best dynamic performance. Such a differential output circuit may consist of an RF transformer or a differential amplifier configuration. The transformer configuration is ideal for most applications with ac coupling, while op amps will be suitable for a dc-coupled configuration.

The single-ended configuration may be considered for applications requiring a unipolar output voltage. Connecting a resistor from either one of the outputs to ground converts the output current into a ground-referenced voltage signal. To improve on the dc linearity by maintaining a virtual ground, an I-to-V or op-amp configuration may be considered.

8.3.3 Differential With Transformer

Using an RF transformer provides a convenient way of converting the differential output signal into a single-ended signal while achieving excellent dynamic performance. The appropriate transformer should be carefully selected based on the output frequency spectrum and impedance requirements.

The differential transformer configuration has the benefit of significantly reducing common-mode signals, thus improving the dynamic performance over a wide range of frequencies. Furthermore, by selecting a suitable impedance ratio (winding ratio) the transformer can be used to provide optimum impedance matching while controlling the compliance voltage for the converter outputs.

図 8-2 and 図 8-3 show 50-Ω doubly terminated transformer configurations with 1:1 and 4:1 impedance ratios, respectively. Note that the center tap of the primary input of the transformer has to be grounded to enable a dc-current flow. Applying a 20-mA full-scale output current would lead to a 0.5-V_{PP} output for a 1:1 transformer and a 1-V_{PP} output for a 4:1 transformer. In general, the 1:1 transformer configuration will have slightly better output distortion, but the 4:1 transformer will have 6 dB higher output power.

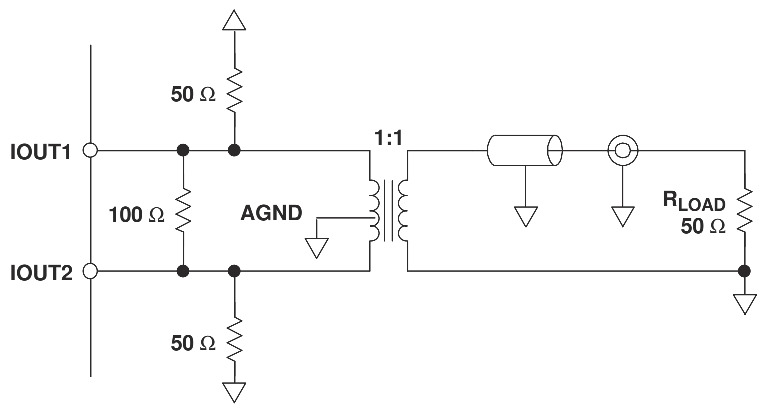


図 8-2. Driving a Doubly Terminated 50-Ω Cable Using a 1:1 Impedance Ratio Transformer

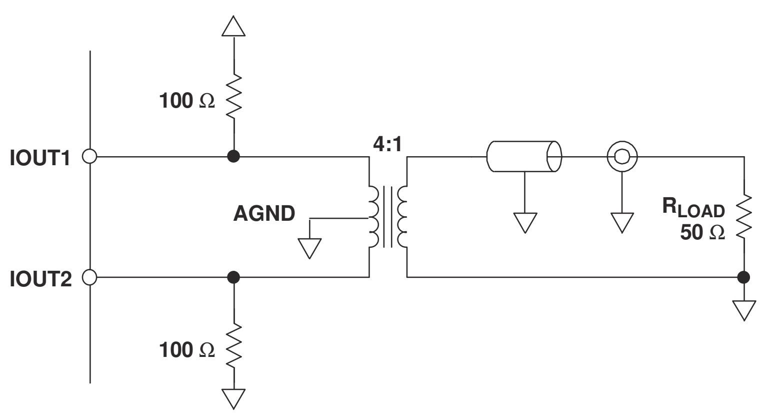


図 8-3. Driving a Doubly Terminated 50-Ω Cable Using a 4:1 Impedance Ratio Transformer

8.3.4 Single-Ended Configuration

図 8-4 shows the single-ended output configuration, where the output current I_{OUT1} flows into an equivalent load resistance of 25 Ω. Node IOUT2 should be connected to AGND or terminated with a resistor of 25 Ω to AGND. The nominal resistor load of 25 Ω gives a differential output swing of 1 V_{PP} when applying a 20-mA full-scale output current.

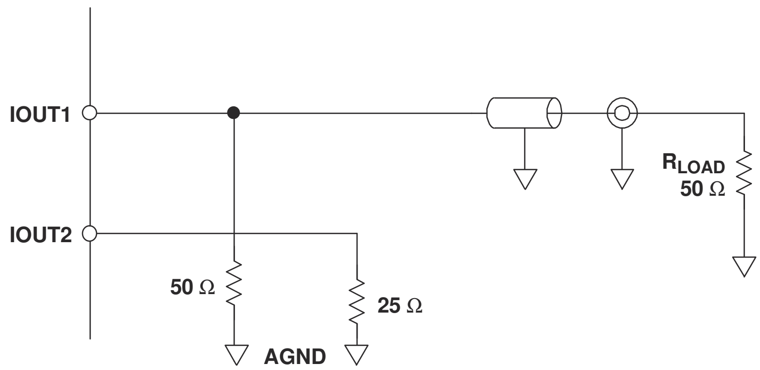


図 8-4. Driving a Doubly Terminated 50-Ω Cable Using a Single-Ended Output

8.3.5 Reference Operation

8.3.5.1 Internal Reference

The DAC5662 has an on-chip reference circuit which comprises a 1.2-V bandgap reference and two control amplifiers, one for each DAC. The full-scale output current, I_{OUTFS}, of the DAC5662 is determined by the reference voltage, V_{REF}, and the value of resistor R_{SET}. I_{OUTFS} can be calculated by:

$$I_{OUTFS} = 32 \times I_{REF} = 32 \times \frac{V_{REF}}{R_{SET}} \tag{9}$$

The reference control amplifier operates as a V-to-I converter producing a reference current, I_{REF}, which is determined by the ratio of V_{REF} and R_{SET} (see 式 9). The full-scale output current, I_{OUTFS}, results from multiplying IREF by a fixed factor of 32.

Using the internal reference, a 2-kΩ resistor value results in a full-scale output of approximately 20 mA. Resistors with a tolerance of 1% or better should be considered. Selecting higher values, the output current can be adjusted from 20 mA down to 2 mA. Operating the DAC5662 at lower than 20-mA output currents may be desirable for reasons of reducing the total power consumption, improving the distortion performance, or observing the output compliance voltage limitations for a given load condition.

It is recommended to bypass the EXTIO pin with a ceramic chip capacitor of 0.1 μF or more. The control amplifier is internally compensated and its small signal bandwidth is approximately 300 kHz.

8.3.5.2 External Reference

The internal reference can be disabled by simply applying an external reference voltage into the EXTIO pin, which in this case functions as an input. The use of an external reference may be considered for applications that require higher accuracy and drift performance or to add the ability of dynamic gain control.

While a 0.1-μF capacitor is recommended to be used with the internal reference, it is optional for the external reference operation. The reference input, EXTIO, has a high input impedance (1 MΩ) and can easily be driven by various sources. Note that the voltage range of the external reference should stay within the compliance range of the reference input.

8.3.6 Gain Setting Option

The full-scale output current on the DAC5662 can be set two ways: either for each of the two DAC channels independently or for both channels simultaneously. For the independent gain set mode, the GSET pin (pin 42) must be low (i.e. connected to AGND). In this mode, two external resistors are required — one RSET connected to the BIASJ_A pin (pin 44) and the other to the BIASJ_B pin (pin 41). In this configuration, the user has the flexibility to set and adjust the full-scale output current for each DAC independently, allowing for the compensation of possible gain mismatches elsewhere within the transmit signal path.

Alternatively, bringing the GSET pin high (i.e. connected to AVDD), the DAC5662 switches into the simultaneous gain set mode. Now the full-scale output current of both DAC channels is determined by only one external RSET resistor connected to the BIASJ_A pin. The resistor at the BIASJ_B pin may be removed, however this is not required since this pin is not functional in this mode and the resistor has no effect on the gain equation.

8.4 Device Functional Modes

8.4.1 Sleep Mode

The DAC5662 features a power-down function which can be used to reduce the total supply current to less than 3.5 mA over the specified supply range if no clock is present. Applying a logic high to the SLEEP pin initiates the power-down mode, while a logic low enables normal operation. When left unconnected, an internal active pulldown circuit enables the normal operation of the converter.

9 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Informmation

9.2 Typical Application

A typical application for the DAC5662 is as dual or single carrier transmitter. The DAC is provided with some input digital baseband signal and it outputs an analog carrier. A typical configuration is described below.

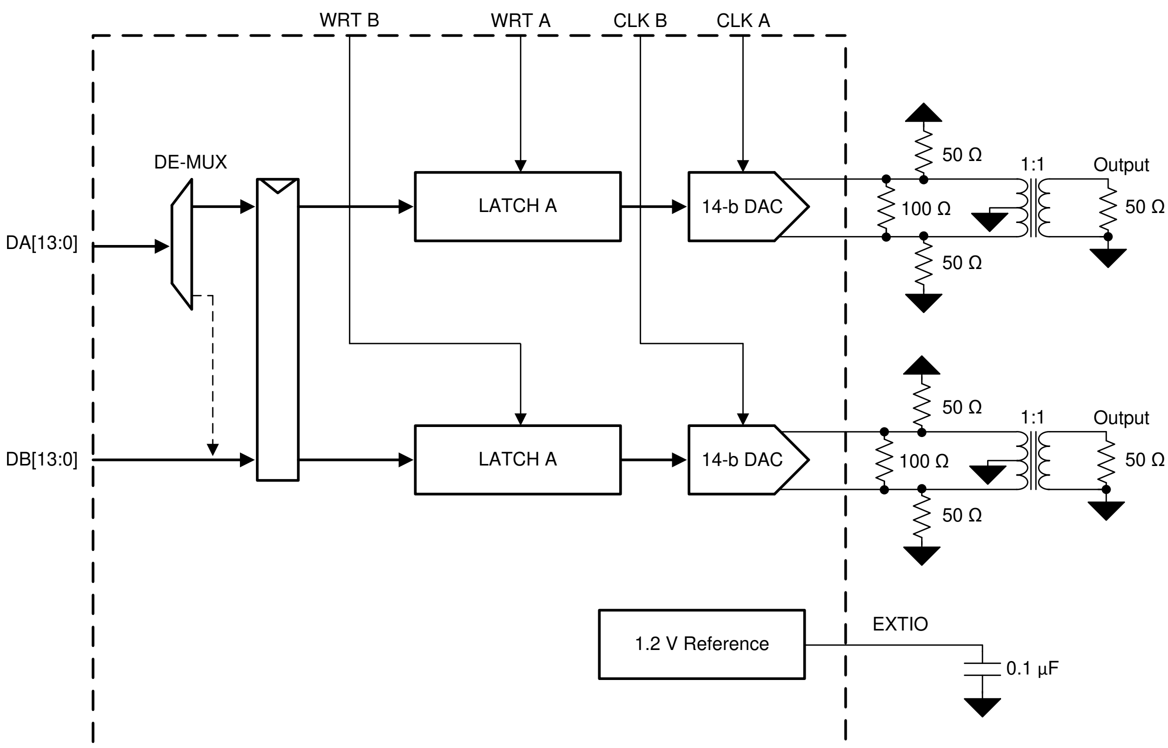


図 9-1. Typical Application Schematic

- Clock rate = 122.88 MHz
- Input data = WCDMA with IF frequency at 30.72 MH
- AVDD = DVDD = 3.3 V

9.2.1 Design Requirements

The requirements for this design were to generate a single WCDMA signal at an intermediate frequency of 30.72 MHz. The ACLR needs to be better than 72 dBc.

9.2.2 Detailed Design Procedure

The single carrier signal with an intermediate frequency of 30.72 MHz must be created in the digital processor at a sample rate of 122.88 Msps for DAC. These 12 bit samples are placed on the 12b CMOS input port of the DAC.

A CMOS DAC clock must be generated from a clock source at 122.88 MHz. This must be provided to the CLK pin of the DAC. The IOUTA and IOUTB differential connections must be connected to a transformer to provide a single ended output. A typical 1:1 impedance transformer is used on the device EVM. The DAC5662 EVM provides a good reference for this design example.

9.2.3 Application Curves

This spectrum analyzer plot shows the ACLR for the transformer output single carrier signal with intermediate frequency of 30.72 MHz. The results meet the system requirements for a minimum of 72 dBc ACLR.

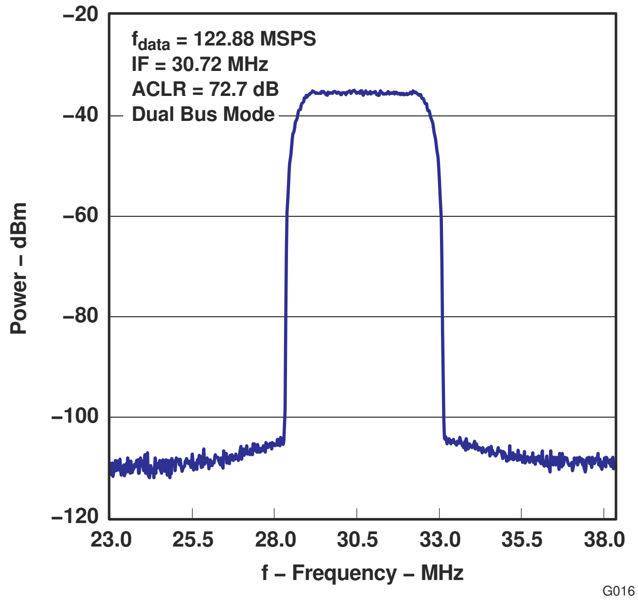


図 9-2. Power vs Frequency

10 Power Supply Recommendations

It is recommended that the device be powered with the nominal supply voltage as indicated in the Recommeneded Operating Conditions.

In most instances, the best performance is achieved with LDO supplies. However, the supplies may be driven with direct outputs from a DC-DC switcher as long as the noise performance of the switcher is acceptable

11 Layout

11.1 Layout Guidelines

The DAC5662 EVM layout should be used as a reference for the layout to obtain the best performance. A sample layout is shown in Figure 11-1 through Figure 11-4. Some important layout recommendations are:

1. Use a single ground plane. Keep the digital and analog signals on distinct separate sections of the board. This may be virtually divided down the middle of the device package when doing placement and layout.
2. Keep the analog outputs as far away from the switching clocks and digital signals as possible. This will keep coupling from the digital circuits to the analog outputs to a minimum.
3. Decoupling caps should be kept close to the power pins of the device.

11.2 Layout Example

The EVM is constructed on a 4-layer, 5.1-inch x 4.8-inch, 0.062-inch thick PCB using FR−4 material. 図 11-1 through 図 11-4 show the PCB layout for the EVM.

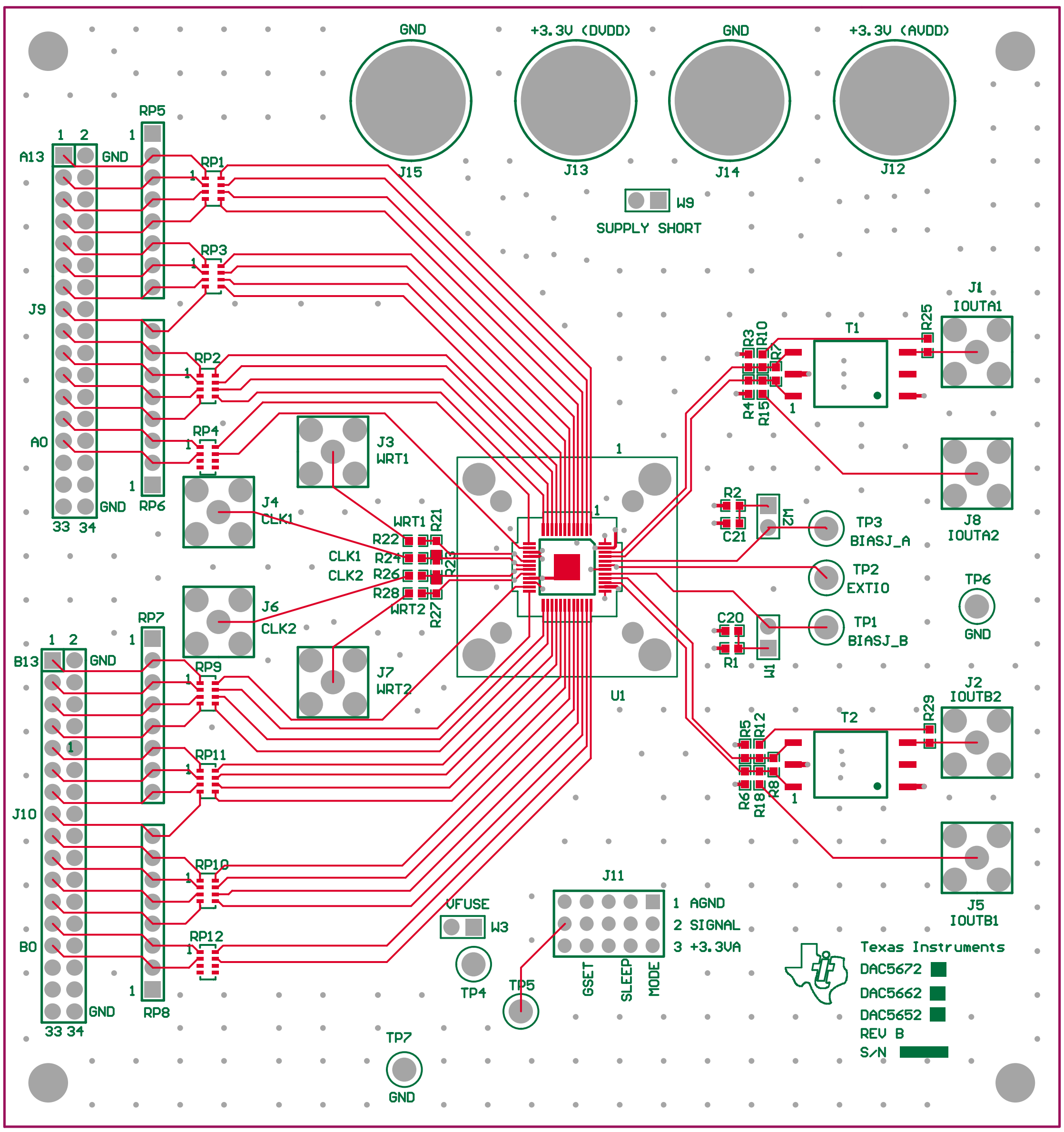


図 11-1. Top Layer 1

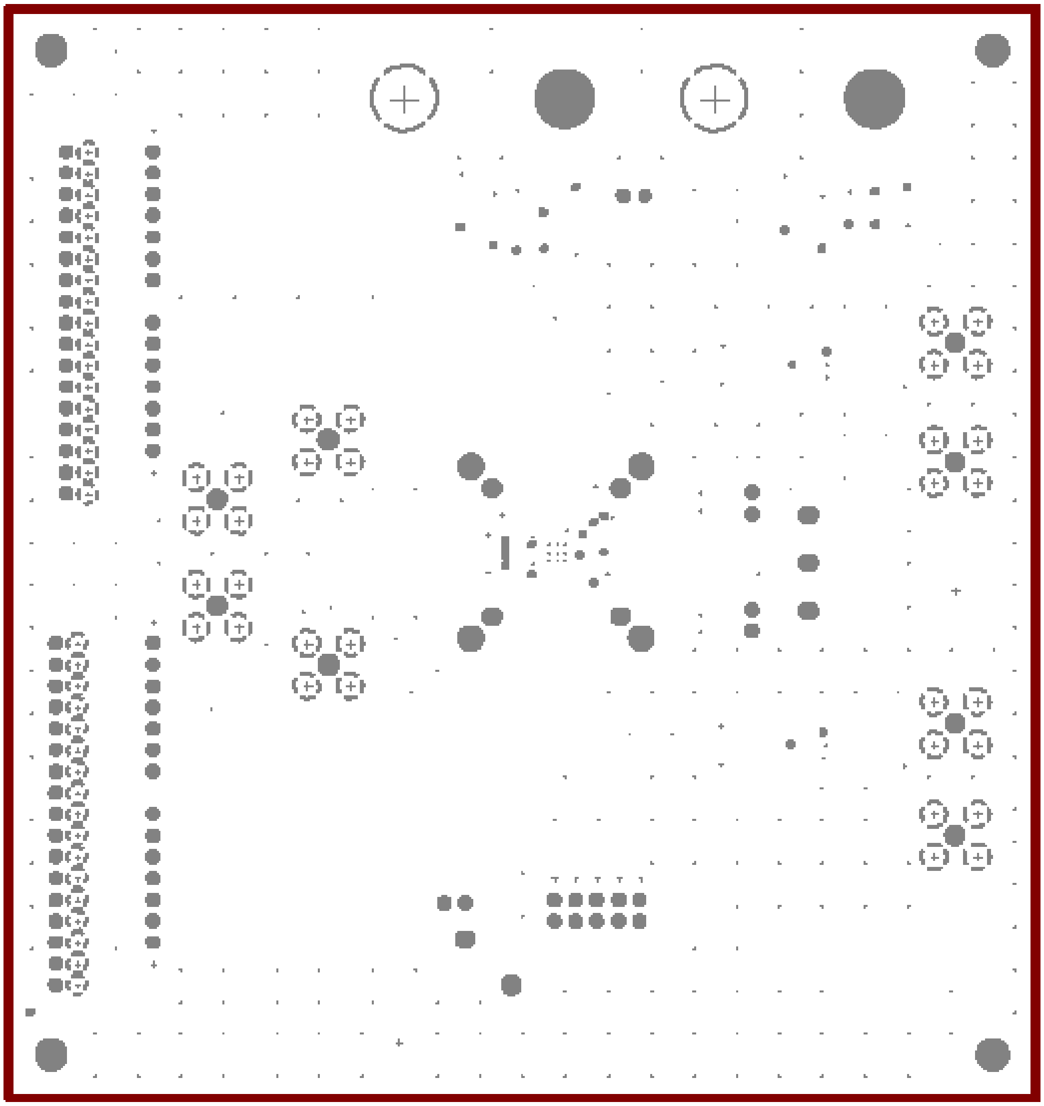


図 11-2. Ground Plane Layer 2

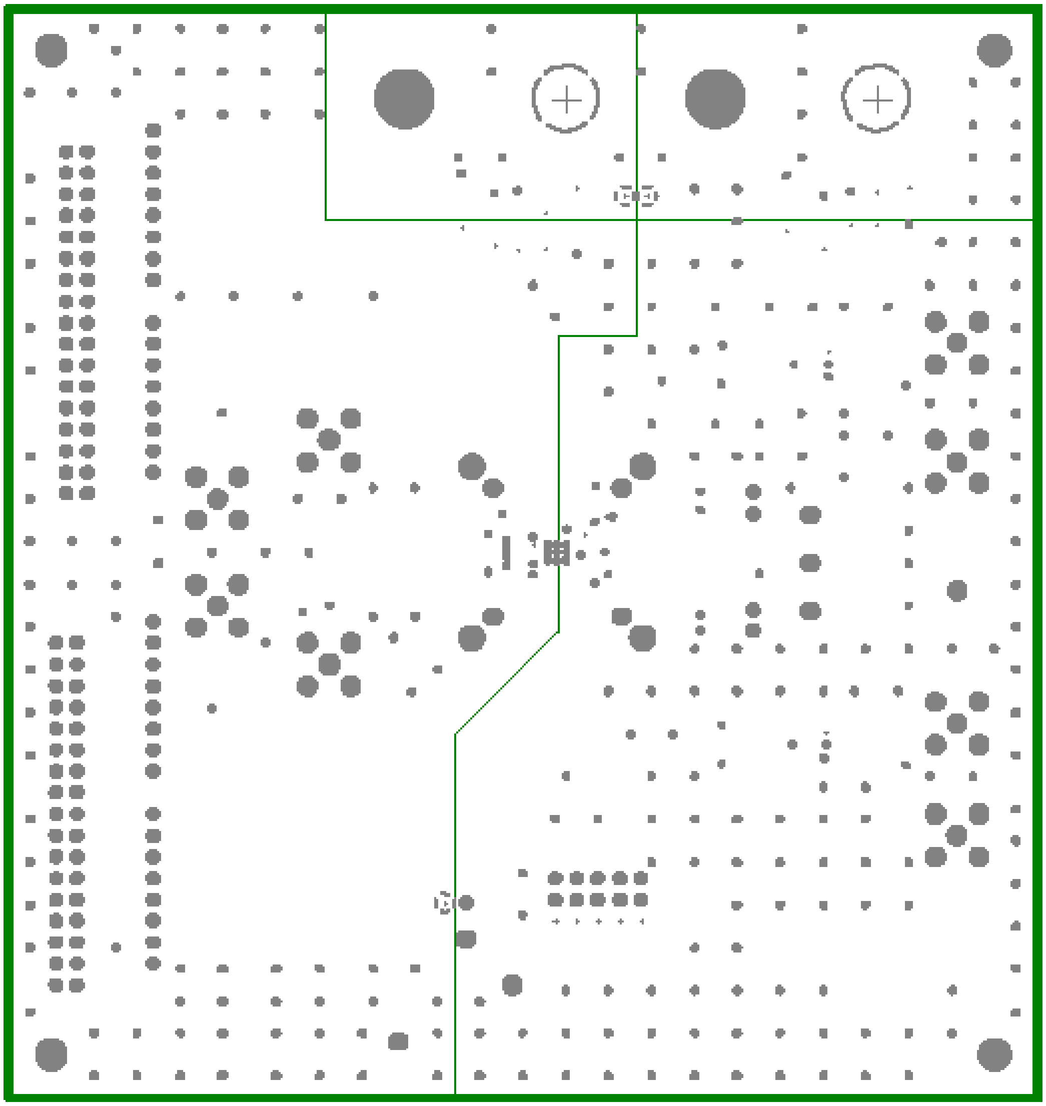


図 11-3. Power Plane Layer 3

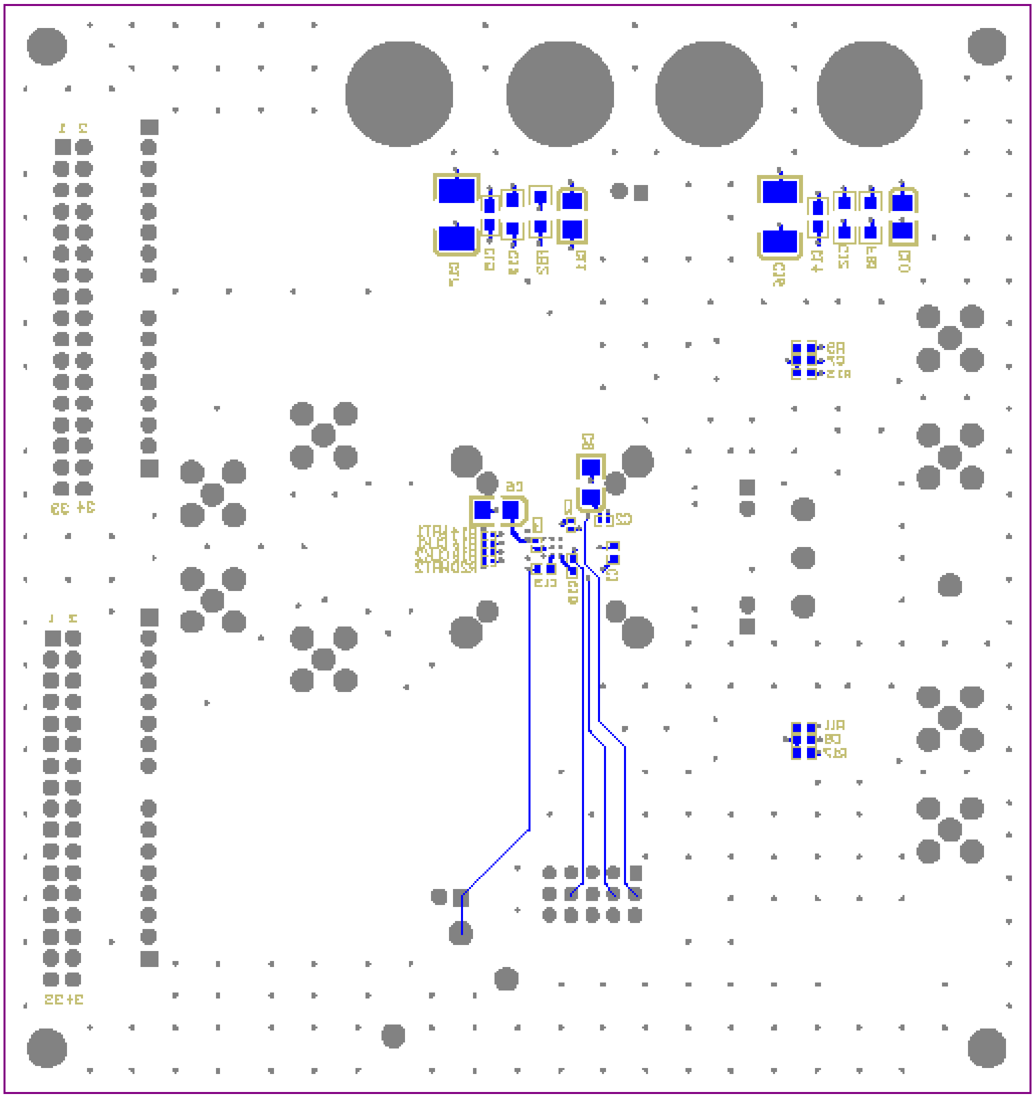


図 11-4. Bottom Layer 4

12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

12.1 Documentation Support

12.1.1 Related Documentation

12.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。*「更新の通知を受け取る」をクリック*して登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

12.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい ESD 対策をとらないと、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

12.6 用語集

TI 用語集	この用語集には、用語や略語の一覧および定義が記載されています。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DAC5662IPFB	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC5662I
DAC5662IPFB.A	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC5662I
DAC5662IPFBG4	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC5662I
DAC5662IPFBG4.A	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC5662I
DAC5662IPFBR	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC5662I
DAC5662IPFBR.A	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC5662I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

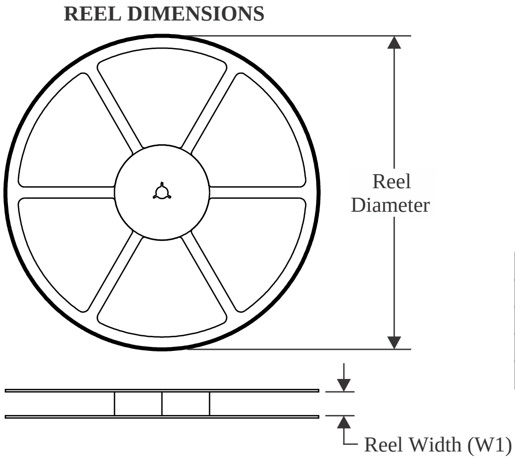
OTHER QUALIFIED VERSIONS OF DAC5662 :

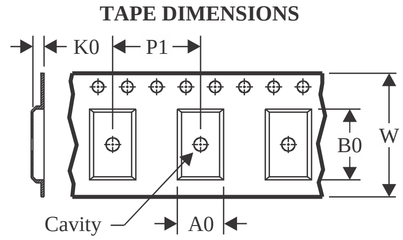
- Enhanced Product : DAC5662-EP

NOTE: Qualified Version Definitions:

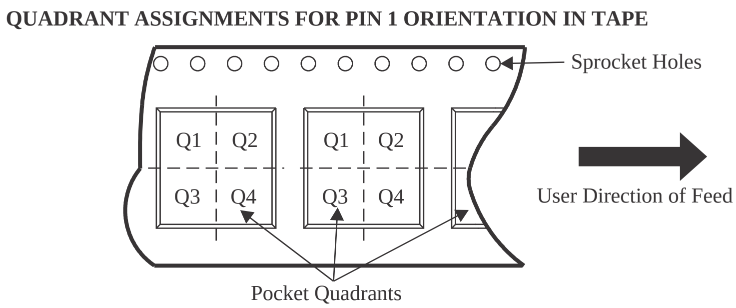
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION





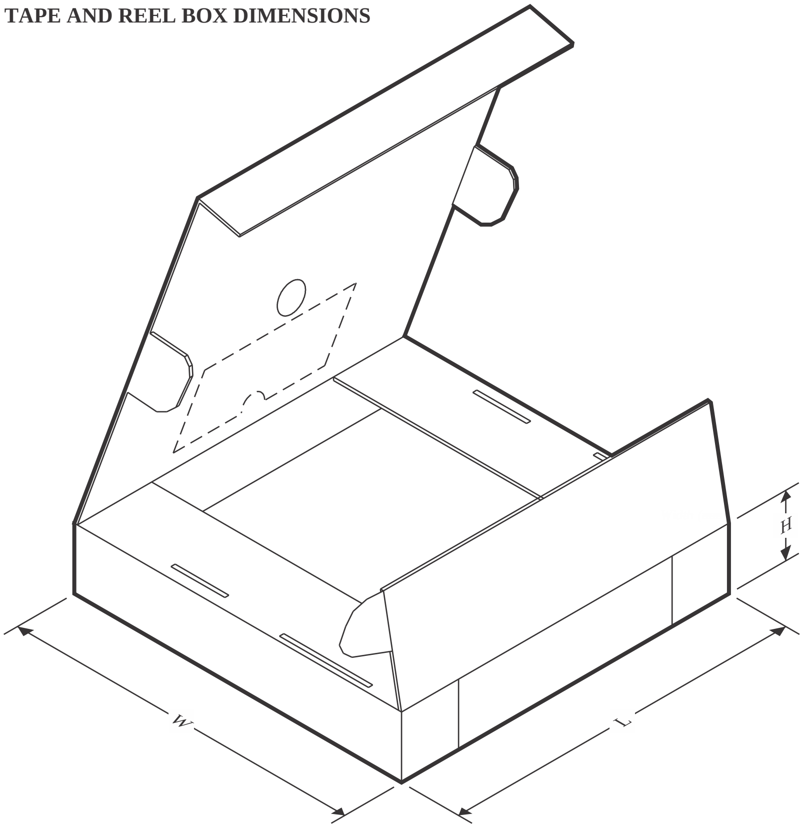
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC5662IPFBR	TQFP	PFB	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2

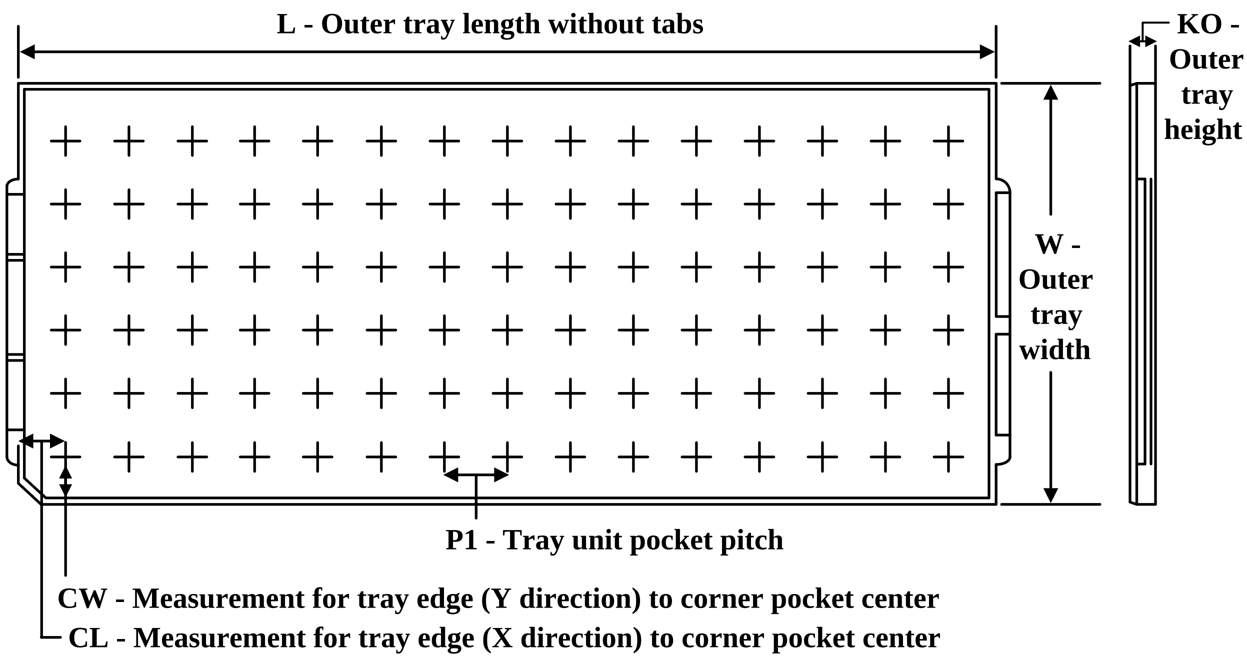
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC5662IPFBR	TQFP	PFB	48	1000	367.0	367.0	38.0

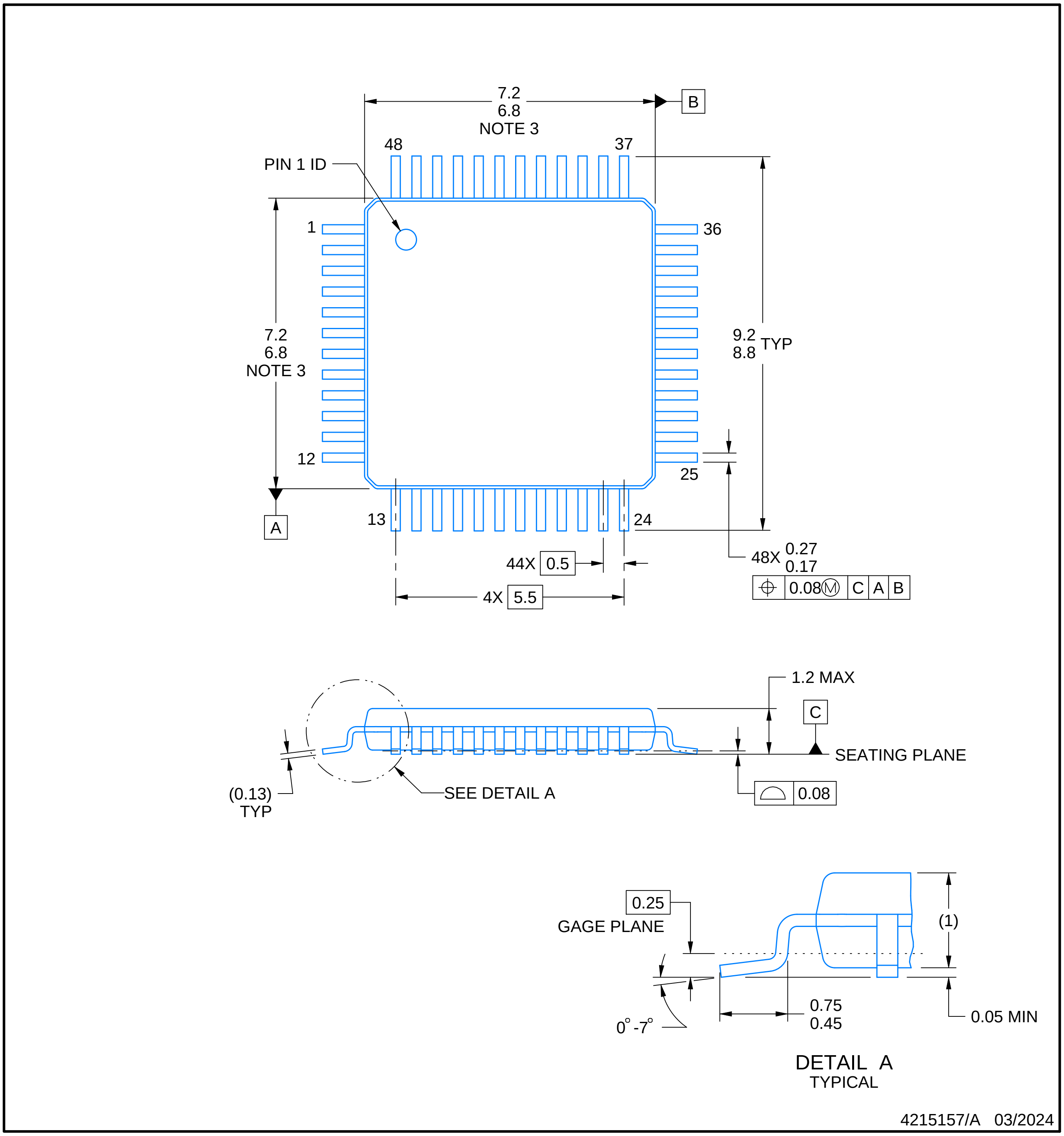
TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

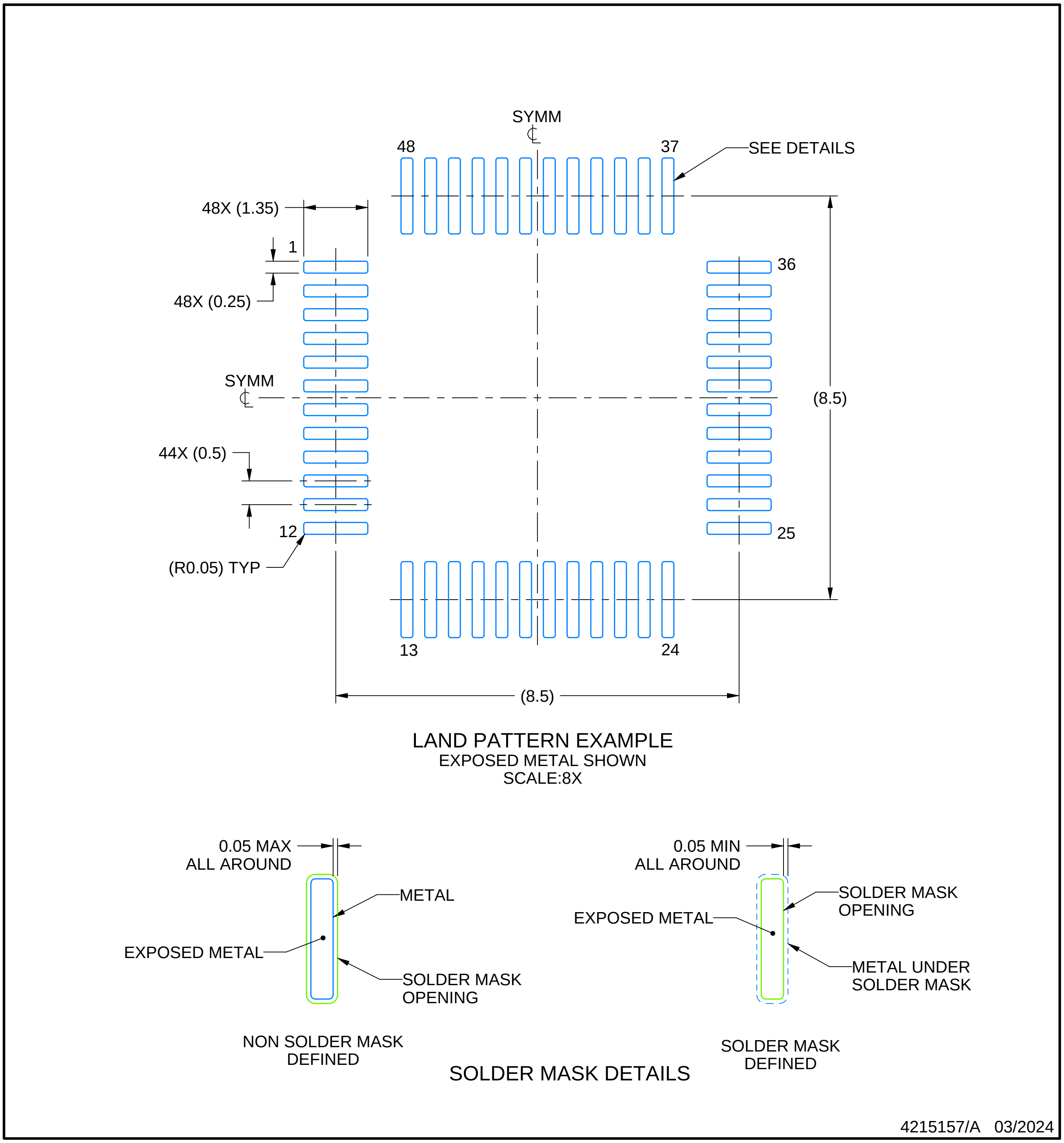
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
DAC5662IPFB	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.5	11.25
DAC5662IPFB.A	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.5	11.25
DAC5662IPFBG4	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.5	11.25
DAC5662IPFBG4.A	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.5	11.25



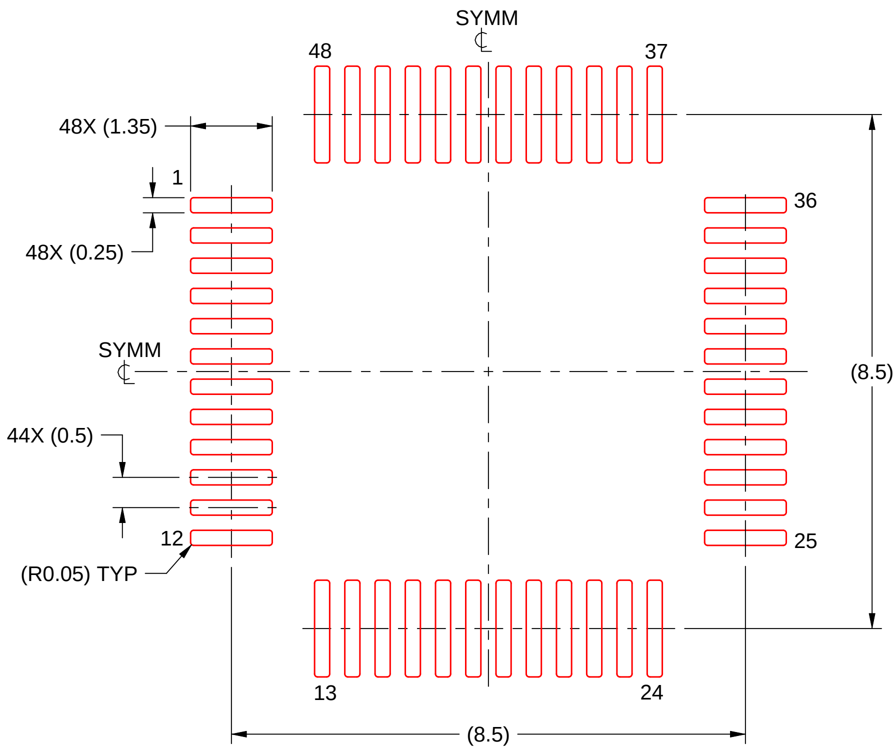
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.



NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
SCALE:8X

4215157/A 03/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、 TI の販売条件 、 TI の総合的な品質ガイドライン 、 ti.com または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。 TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

最終更新日：2025 年 10 月