DAC5672A 14ビット、275MSPS DAコンバータ

1 特長

- 14ビット、デュアル伝送DAコンバータ(DAC)
- 更新速度: 275MSPS
- 単一電源: 3V～3.6V
- 高SFDR (スプリアス・フリー・ダイナミック・レンジ): 5MHz時84dBc
- 高IMD3 (3次相互変調歪): 15.1MHzおよび16.1MHz時79dBc
- WCDMAのACLR (隣接チャネル漏洩電力比): ベースバンド時78dB
- WCDMAのACLR: 30.72MHz時73dB
- 独立または単一抵抗によるゲイン制御
- デュアル・データまたはインターリーブ・データ
- 1.2Vのリファレンスを内蔵
- 低消費電力: 330mW
- パワーダウン・モード: 9mW
- パッケージ: 48ピンTQFP (Thin-Quad Flat Pack)

2 アプリケーション

- 携帯電話基地局通信チャネル
  - CDMA: W-CDMA、CDMA2000、IS-95
  - TDMA: GSM、IS-136、EDGEおよびUWC-136
- 医療用および試験用機器
- 任意波形発生器(ARB)
- ダイレクト・デジタル・シンセシス(DDS)
- ケーブル・モデム・ターミネーション・システム(CMTS)

3 概要

DAC5672Aデバイスは、電圧リファレンスを内蔵したモノリシック、デュアル・チャネルの14ビット高速DACです。

最高275MSPSの更新速度で動作し、抜群の動的性能、正確なゲイン、オフセット整合といった特性を備えていることから、I/Qベースバンドまたはダイレクト IF通信アプリケーションに最適です。

各DACには、シングルエンドまたは差動アナログ出力構成に適した高インピーダンスの差動電流出力が備えられています。外部抵抗を使用して、各DACのフルスケール出力電流を別々に、または同時にスケーリングすることができます(一般的には2mA～20mA)。高精度の内蔵電圧リファレンスは温度補償機能を備え、安定した1.2Vのリファレンス電圧を提供します。外部リファレンスも使用できます。

DAC5672Aには、クロックとデータ・ラッチが異なる14ビットのパラレル入力ポートが2つあります。柔軟性を高めるために、インターリーブ・モードで動作する際には1ポートで各DACへの多重データもサポートされます。

DAC5672Aは、50Ωの二重終端負荷を接続した変圧器結合の差動出力用に設計されています。20mAのフルスケール出力電流の場合、インピーダンス比4:1 (結果として出力4dBm)とインピーダンス比1:1の変圧器(出力−2dBm)をサポートします。

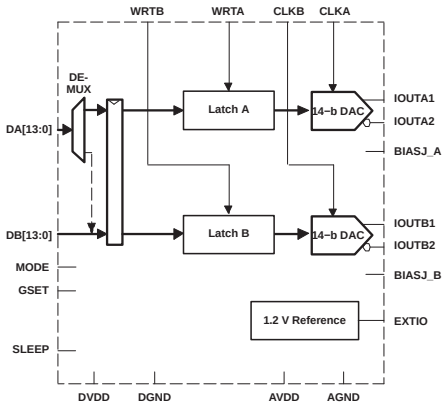
DAC5672Aは48ピンTQFPパッケージで供給されます。ファミリ製品間にはピン互換性があり、12ビット(DAC5662)および14ビット(DAC5672A)の分解能を提供します。さらに、DAC5672AはDAC2904およびAD9767のデュアルDACとピン互換です。このデバイスは、−40℃～85℃の工業用温度範囲で動作することを特長としています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
DAC5672A	TQFP (48)	7.00mm×7.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

機能ブロック図



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

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- 「*製品情報*」表 追加 ... 1
- 「*電気的特性*」セクションに温度係数オフセット・ドリフトおよびゲイン・ドリフトを 追加 ... 1
- 「*機能説明*」セクション 追加 ... 1
- 「*電気的特性*」セクションの電源にf_{DATA} = 200MSPS、f_{OUT}＝1MHzを 追加 ... 1
- 「*プログラミング*」セクションのデュアルバス・データ・インターフェイスおよびタイミング 変更 ... 1
- 「*電気的特性*」セクションのデジタル入力に3.3 (最大値)および0.8 (最大値)を 追加 ... 1
- 「*選択肢*」表 削除 ... 1
- 「*ピン構成および機能*」セクションのピン配置図およびピン表の形式を変更 ... 1
- 「*ESD定格*」表 追加 ... 1
- 「*推奨する動作条件*」表 追加 ... 1
- 「*熱条件*」表 追加 ... 1
- Table 1の形式 変更 ... 1
- 「*アプリケーション情報*」および「*代表的なアプリケーション*」セクション 追加 ... 1
- 「*電源に関する推奨事項*」セクション 追加 ... 1
- 「*レイアウト*」セクション 追加 ... 1

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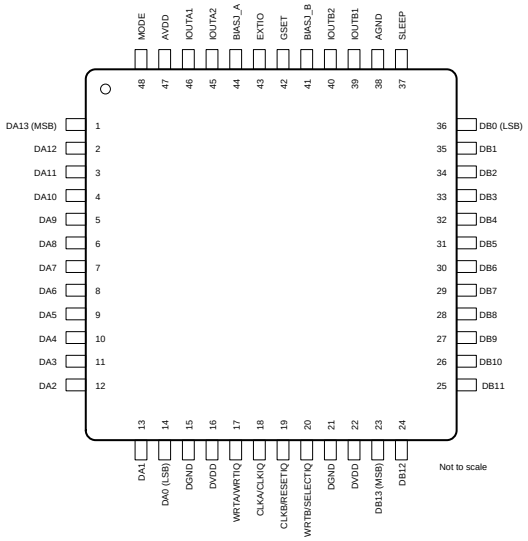
- Added Internal pulldown. ... 3
- Added Internal pulldown. ... 4
- Added The pullup and pulldown circuitry is approximately equivalent to 100 kΩ. ... 20
- Added resistor values ... 21
- Added resistor values ... 21

5 Pin Configuration and Functions

PFB Package
48-Pin TQFP
Top View



Pin Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AGND	38	I	Analog ground
AVDD	47	I	Analog supply voltage
BIASJ_A	44	O	Full-scale output current bias for DACA
BIASJ_B	41	O	Full-scale output current bias for DACB
CLKA/CLKIQ	18	I	Clock input for DACA, CLKIQ in interleaved mode
CLKB/RESETIQ	19	I	Clock input for DACB, RESETIQ in interleaved mode
DA[13:0]	1	I	Data port A. DA13 is MSB and DA0 is LSB. Internal pulldown.
	2		
	3		
	4		
	5		
	6		
	7		
	8		
	9		
	10		
	11		
	12		
	13		
	14		

Pin Functions (continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
DB[13:0]	23	I	Data port B. DB13 is MSB and DB0 is LSB. Internal pulldown.
	24		
	25		
	26		
	27		
	28		
	29		
	30		
	31		
	32		
	33		
	34		
	35		
	36		
DGND	15	I	Digital ground
	21		
DVDD	16	I	Digital supply voltage
	22		
EXTIO	43	I/O	Internal reference output (bypass with 0.1 μF to AGND) or external reference input
GSET	42	I	Gain-setting mode: H – 1 resistor, L – 2 resistors. Internal pullup.
IOUTA1	46	O	DACA current output. Full-scale with all bits of DA high.
IOUTA2	45	O	DACA complementary current output. Full-scale with all bits of DA low.
IOUTB1	39	O	DACB current output. Full-scale with all bits of DB high.
IOUTB2	40	O	DACB complementary current output. Full-scale with all bits of DB low.
MODE	48	I	Mode Select: H – Dual Bus, L – Interleaved. Internal pullup.
SLEEP	37	I	Sleep function control input: H – DAC in power-down mode, L – DAC in operating mode. Internal pulldown.
WRTA/WRTIQ	17	I	Input write signal for PORT A (WRTIQ in interleaving mode)
WRTB/SELECTIQ	20	I	Input write signal for PORT B (SELECTIQ in interleaving mode)

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	AVDD (2)	–0.5	4	V
	DVDD (3)			
Voltage between AGND and DGND		–0.5	0.5	V
Voltage between AVDD and DVDD		–4	4	V
Supply voltage	DA [13:0] and DB [13:0] (3)	–0.5	DVDD + 0.5	V
	MODE, SLEEP, CLKA, CLKB, WRTA, WRTB (3)	–0.5	DVDD + 0.5	V
	IOUTA1, IOUTA2, IOUTB1, IOUTB2 (2)	–1	AVDD + 0.5	V
	EXTIO, BIASJ_A, BIASJ_B, GSET (2)	–0.5	AVDD + 0.5	V
Peak input current (any input)		20		mA
Peak total input current (all inputs)		–30		mA
Operating free-air temperature range		–40	85	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Measured with respect to AGND.
(3) Measured with respect to DGND.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supplies				
AVDD	3.0	3.3	3.6	V
DVDD	3.0	3.3	3.6	V
$I_{(AVDD)}$ Analog supply current		75	90	mA
$I_{(DVDD)}$ Digital supply current		25	38	mA
Analog Output				
$I_{O(FS)}$ Full-scale output current	2		20	mA
Output voltage compliance range	–1		1.25	V
Clock Interface (CLK, CLKC)				
CLKINPUT Frequency			275	MHz

6.4 Thermal Information

THERMAL METRIC(1)		DAC5672A PFB (TQFP) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	64.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	16.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	27.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	27.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over T_A, AVDD = DVDD = 3.3 V, I_{OUTFS} = 20 mA, independent gain set mode, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC SPECIFICATIONS						
	Resolution		14			Bits
DC ACCURACY (1)						
INL	Integral nonlinearity	1 LSB = I_{OUTFS} / 2^{14}, T_{MIN} to T_{MAX}	–4	±1.1	4	LSB
DNL	Differential nonlinearity		–3	±0.75	3	LSB
ANALOG OUTPUT						
	Offset error	Midscale value		±0.03		%FSR
	Offset mismatch	Midscale value		±0.03		%FSR
	Gain error	With external reference		±0.25		%FSR
		With internal reference		±0.25		%FSR
	Minimum full-scale output current (2)			2		mA
	Maximum full-scale output current (2)			20		mA
	Gain mismatch	With external reference	–2	0.2	2	%FSR
		With internal reference	–2	0.2	2	%FSR
	Output voltage compliance range (3)		–1		1.25	V
R_O	Output resistance			300		kΩ
C_O	Output capacitance			5		pF
REFERENCE OUTPUT						
	Reference voltage		1.14	1.2	1.26	V
	Reference output current (4)			100		nA
REFERENCE INPUT						
V_{EXTIO}	Input voltage		0.1		1.25	V
R_I	Input resistance			1		MΩ
	Small signal bandwidth			300		kHz
C_I	Input capacitance			100		pF
TEMPERATURE COEFFICIENTS						
	Offset drift			2	10	ppm of FSR/°C

(1) Measured differently through 50 Ω to AGND.
(2) Nominal full-scale current (I_{OUTFS}) equals 32 times the I_{BIAS} current
(3) The lower limit of the output compliance is determined by the CMOS process. Exceeding this limit may result in transistor breakdown, resulting in reduced reliability of the DAC5672A device. The upper limit of the output compliance is determined by the load resistors and ful-scale output current. Exceeding the upper limit adversely affects distortion performance and integral nonlinearity.
(4) Use an external buffer amplifier with high-impedance input to drive any external load.

Electrical Characteristics (continued)

over T_A, AVDD = DVDD = 3.3 V, I_{OUTFS} = 20 mA, independent gain set mode, (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Gain drift	With external reference (DACA)		10	43	ppm of FSR/°C
	With external reference (DACB)		20	80	
	With internal reference		40	160	ppm of FSR/°C
Reference voltage drift			20		ppm /°C

6.6 Electrical Characteristics

over T_A, AVDD = DVDD = 3.3 V, I_{OUTFS} = 20 mA, f_{DATA} = 200 MSPS, f_{OUT} = 1 MHz, independent gain set mode, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
AVDD	Analog supply voltage		3	3.3	3.6	V
DVDD	Digital supply voltage		3	3.3	3.6	V
I_{AVDD}	Analog supply current	Including output current through load resistor		75	90	mA
		Sleep mode with clock		2.5	6	mA
		Sleep mode without clock		2.5		mA
I_{DVDD}	Digital supply current	f_{DATA} = 200 MSPS, f_{OUT} = 1 MHz		25	38	mA
		Sleep mode with clock		13.4	18	mA
		Sleep mode without clock		0.6		mA
	Power dissipation	f_{DATA} = 200 MSPS, f_{OUT} = 1 MHz		330	390	mW
		Sleep mode with clock		53		
		Sleep mode without clock		9.2		
		f_{DATA} = 275 MSPS, f_{OUT} = 20 MHz		350		
APSRR	Analog power supply rejection ratio		–0.2	–0.01	0.2	%FSR/V
DPSRR	Digital power supply rejection ratio		–0.2	0	0.2	%FSR/V
T_A	Operating free-air temperature		–40		85	°C

6.7 Electrical Characteristics: AC Characteristics

AC specifications over T_A , AVDD = DVDD = 3.3 V, I_{OUTFS} = 20 mA, differential 1:1 impedance ratio transformer coupled output, 50-Ω doubly terminated load (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG OUTPUT						
f_{clk}	Maximum output update rate (1)		275			MSPS
t_s	Output settling time to 0.1% (DAC)	Midscale transition		20		ns
t_r	Output rise time 10% to 90% (OUT)			1.4		ns
t_f	Output fall time 10% to 90% (OUT)			1.5		ns
	Output noise	I_{OUTFS} = 20 mA		55		pA/√Hz
		I_{OUTFS} = 2 mA		30		pA/√Hz
AC LINEARITY						

(1)

Electrical Characteristics: AC Characteristics (continued)

AC specifications over T_A , AVDD = DVDD = 3.3 V, I_{OUTFS} = 20 mA, differential 1:1 impedance ratio transformer coupled output, 50-Ω doubly terminated load (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SFDR	Spurious-free dynamic range	1st Nyquist zone: T_A = 25°C f_{DATA} = 50 MSPS f_{OUT} = 1 MHz I_{OUTFS} = 0 dB		83		dBc
		1st Nyquist zone: T_A = 25°C f_{DATA} = 50 MSPS f_{OUT} = 1 MHz I_{OUTFS} = –6 dB		80		
		1st Nyquist zone: T_A = 25°C f_{DATA} = 50 MSPS f_{OUT} = 1 MHz I_{OUTFS} = –12 dB		79		
		1st Nyquist zone: T_A = 25°C f_{DATA} = 100 MSPS f_{OUT} = 5 MHz		84		
		1st Nyquist zone, T_A = 25°C, f_{DATA} = 100 MSPS, f_{OUT} = 20 MHz		79		
		1st Nyquist zone, T_{MIN} to T_{MAX}, f_{DATA} = 200 MSPS, f_{OUT} = 20 MHz	68	75		
		1st Nyquist zone, T_A = 25°C, f_{DATA} = 200 MSPS, f_{OUT} = 41 MHz		72		
		1st Nyquist zone, TA = 25°C, f_{DATA} = 275 MSPS, f_{OUT} = 20 MHz		74		
SNR	Signal-to-noise ratio	1st Nyquist zone, T_A = 25°C, f_{DATA} = 100 MSPS, f_{OUT} = 5 MHz		77		dB
		1st Nyquist zone, T_A = 25°C, f_{DATA} = 160 MSPS, f_{OUT} = 20 MHz		70		dB
ACLR	Adjacent channel leakage ratio	W-CDMA signal with 3.84-MHz bandwidth, f_{DATA} = 61.44 MSPS, IF = 15.360 MHz		75		dB
		W-CDMA signal with 3.84-MHz bandwidth, f_{DATA} = 122.88 MSPS, IF = 30.72 MHz		73		dB
		W-CDMA signal with 3.84-MHz bandwidth, f_{DATA} = 61.44 MSPS, baseband		78		dB
		W-CDMA signal with 3.84-MHz bandwidth, f_{DATA} = 122.88 MSPS, baseband		78		dB
IMD3	Third-order two-tone intermodulation	Each tone at –6 dBFS, T_A = 25°C, f_{DATA} = 200 MSPS, f_{OUT} = 45.4 MHz and 46.4 MHz		65		dBc
		Each tone at –6 dBFS, T_A = 25°C, f_{DATA} = 100 MSPS, f_{OUT} = 15.1 MHz and 16.1 MHz		79		dBc
IMD	Four-tone intermodulation	Each tone at –12 dBFS, T_A = 25°C, f_{DATA} = 100 MSPS, f_{OUT} = 15.6, 15.8, 16.2, and 16.4 MHz		79		dBc
		Each tone at –12 dBFS, T_A = 25°C, f_{DATA} = 165 MSPS, f_{OUT} = 68.8, 69.6, 71.2, and 72 MHz		61		dBc
		Each tone at –12 dBFS, T_A = 25°C, f_{DATA} = 165 MSPS, f_{OUT} = 19, 19.1, 19.3, and 19.4 MHz		73		dBc

Electrical Characteristics: AC Characteristics (continued)

AC specifications over T_A , AVDD = DVDD = 3.3 V, I_{OUTFS} = 20 mA, differential 1:1 impedance ratio transformer coupled output, 50-Ω doubly terminated load (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Channel isolation	T_A = 25°C, f_{DATA} = 165 MSPS, f_{OUT} (CH1) = 20 MHz, f_{OUT} (CH2) = 21 MHz		95		dBc

6.8 Electrical Characteristics: Digital Characteristics

Digital specifications over T_A, AVDD = DVDD = 3.3 V, I_{OUTFS} = 20 mA, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUT						
V_{IH}	High-level input voltage		2		3.3	V
V_{IL}	Low-level input voltage		0		0.8	V
I_{IH}	High-level input current			±50	0.8	µA
I_{IL}	Low-level input current			±10		µA
$I_{IH(GSET)}$	High-level input current, GSET pin			7		µA
$I_{IL(GSET)}$	Low-level input current, GSET pin			–80		µA
$I_{IH(MODE)}$	High-level input current, MODE pin			–30		µA
$I_{IL(MODE)}$	Low-level input current, MODE pin			–80		µA
C_I	Input capacitance			5		pF

6.9 Switching Characteristics

digital specifications over T_A, AVDD = DVDD = 3.3 V, I_{OUTFS} = 20 mA, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{su}	Input setup time	Dual bus mode	1			ns
		Single-bus interleaved mode		0.5		
t_h	Input hold time	Dual bus mode	1			ns
		Single-bus interleaved mode		0.5		
t_{LPH}	Input clock pulse high time	Dual bus mode		1		ns
		Single-bus interleaved mode				
t_{LAT}	Clock latency (WRT A/B to outputs)	Dual bus mode	4		4	clk
		Single-bus interleaved mode	4		4	
t_{PD}	Propagation delay time	Dual bus mode		1.5		ns
		Single-bus interleaved mode		1.5		

6.10 Typical Characteristics

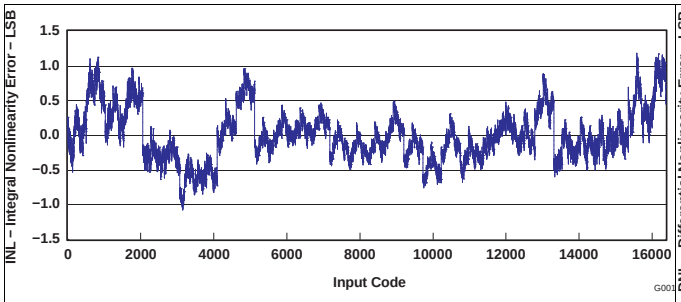


Figure 1. Integral Nonlinearity vs Input Code

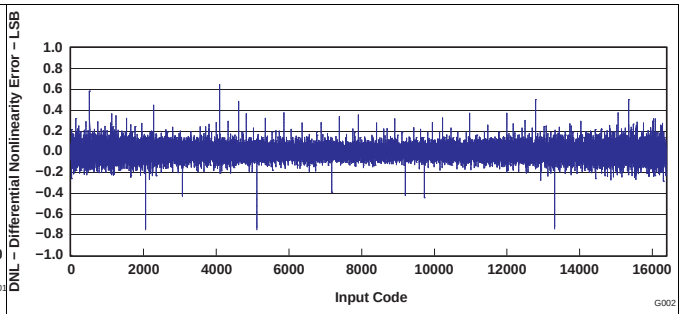


Figure 2. Differential Nonlinearity vs Input Code

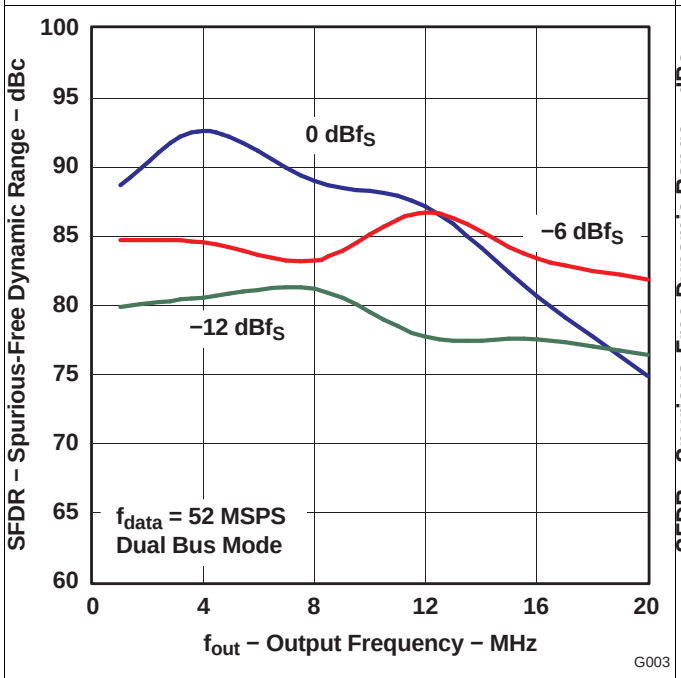


Figure 3. Spurious-Free Dynamic Range vs Output Frequency

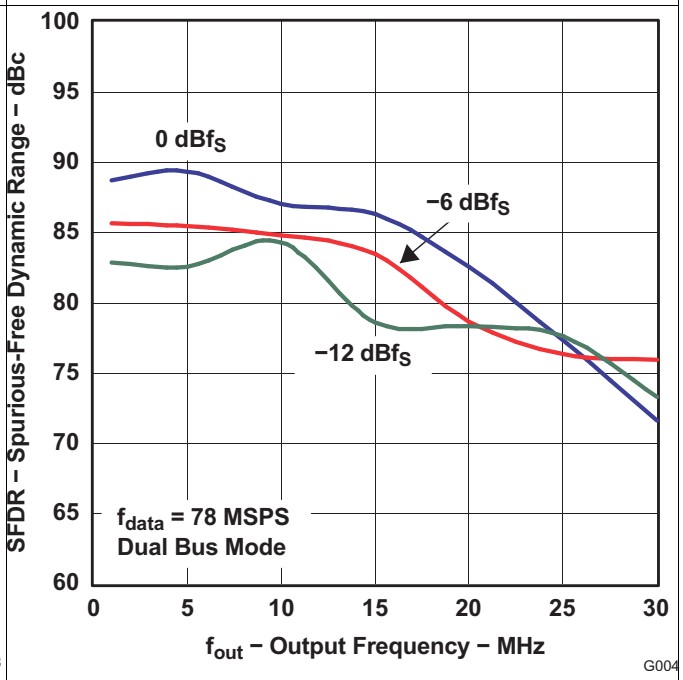


Figure 4. Spurious-Free Dynamic Range vs Output Frequency

Typical Characteristics (continued)

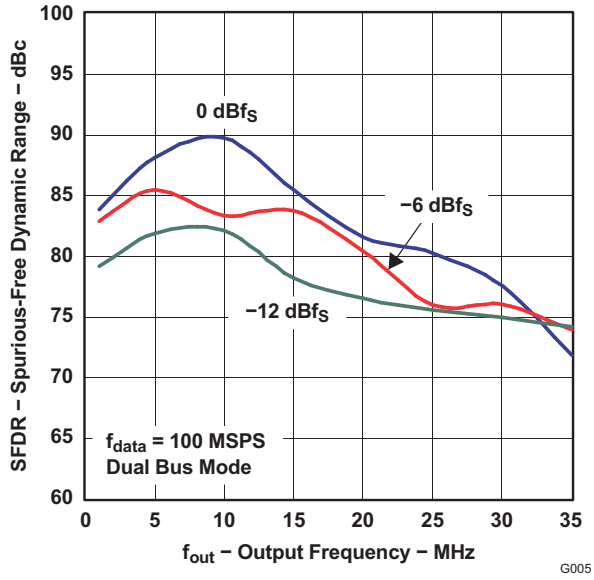


Figure 5. Spurious-Free Dynamic Range vs Output Frequency

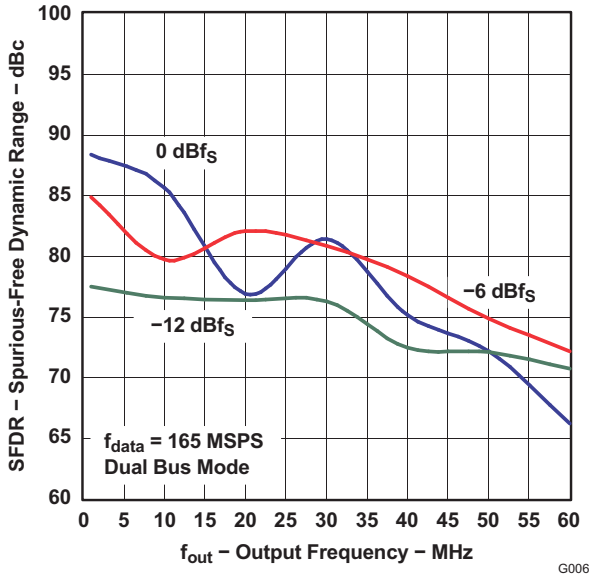


Figure 6. Spurious-Free Dynamic Range vs Output Frequency

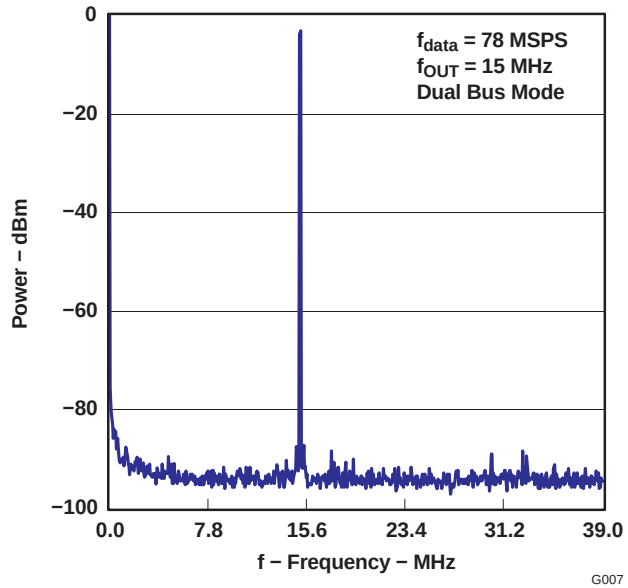


Figure 7. Single-Tone Spectrum

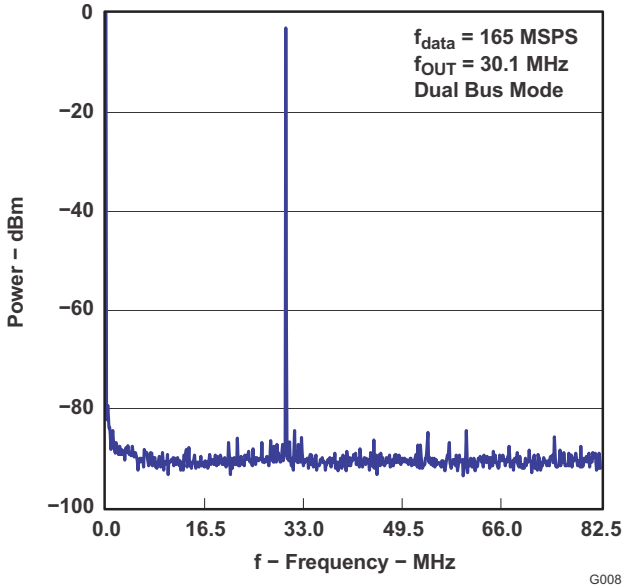


Figure 8. Single-Toned Spectrum

Typical Characteristics (continued)

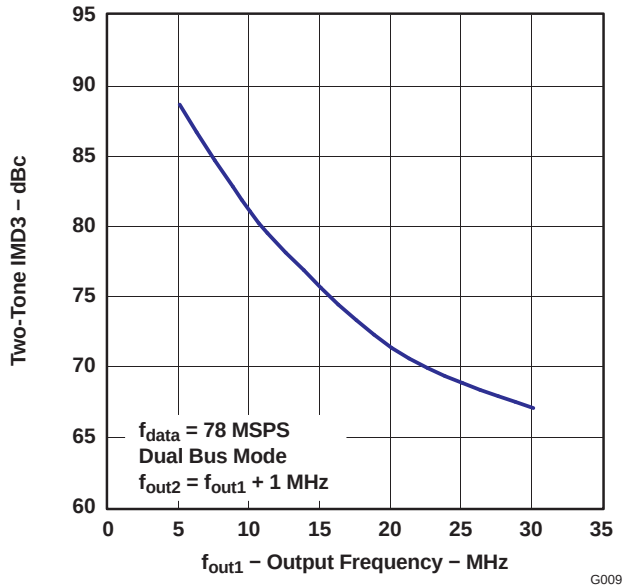


Figure 9. Two-Tone IMD3 vs Output Frequency

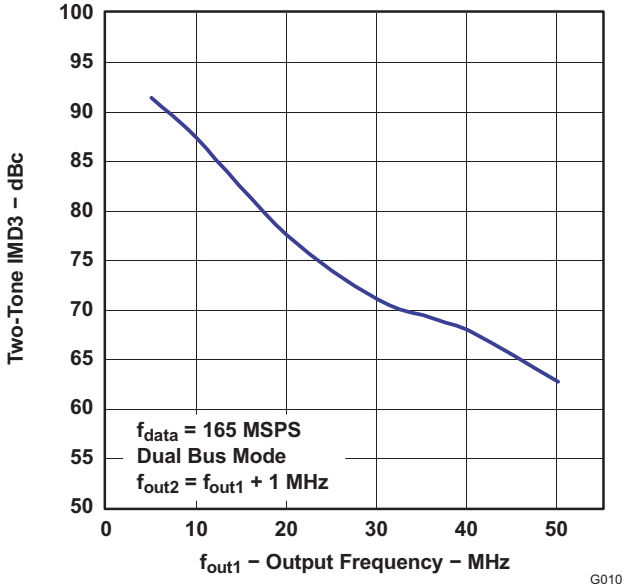


Figure 10. Two-Tone IMD3 vs Output Frequency

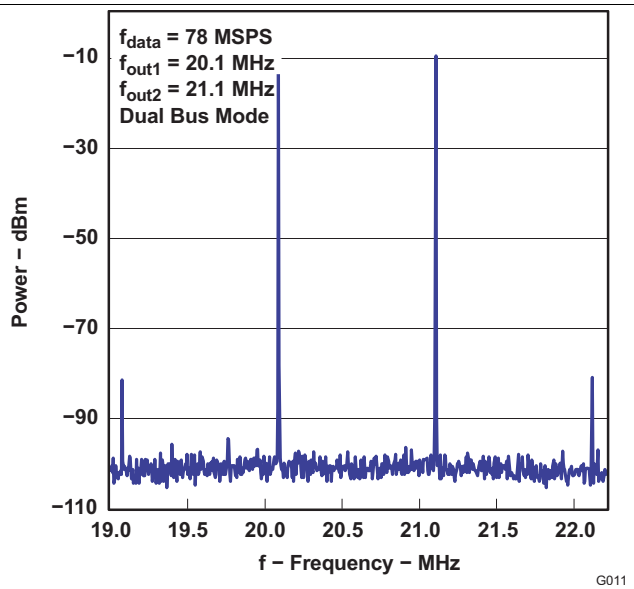


Figure 11. Two-Tone Spectrum

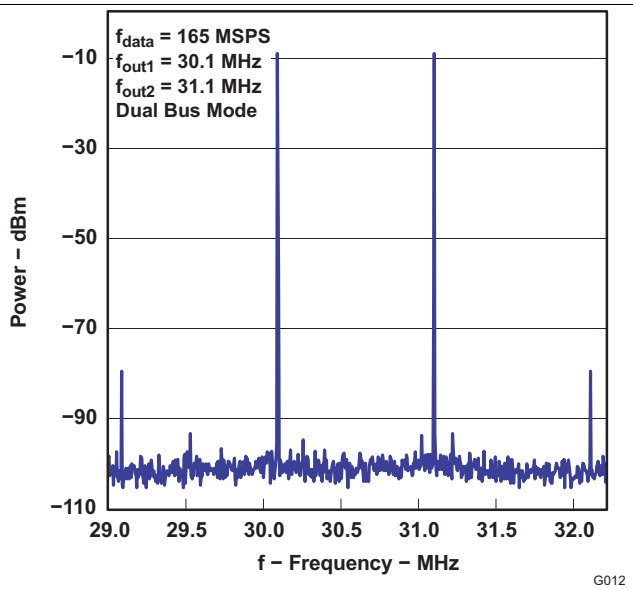


Figure 12. Two-Tone Spectrum

Typical Characteristics (continued)

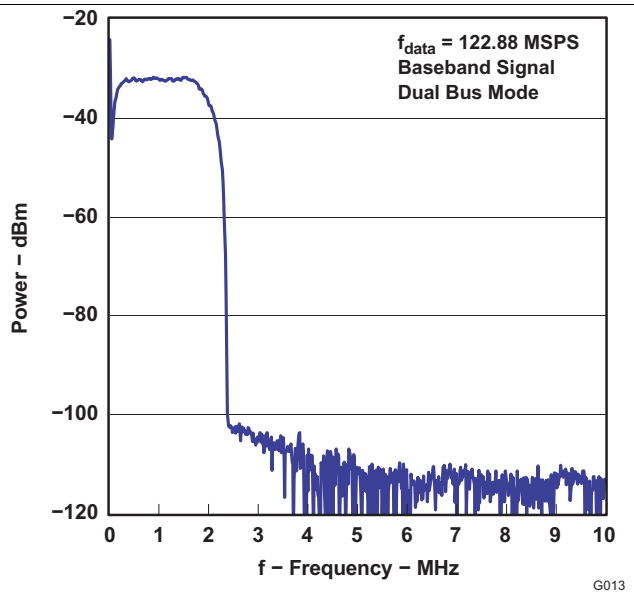


Figure 13. Power vs Frequency

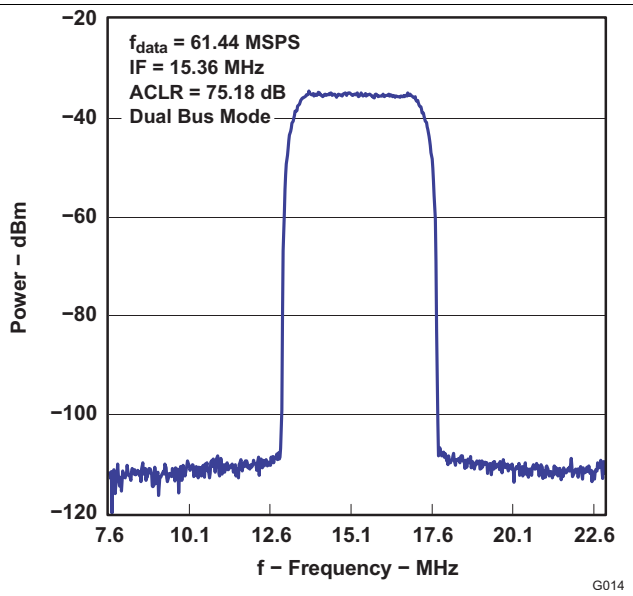


Figure 14. Power vs Frequency

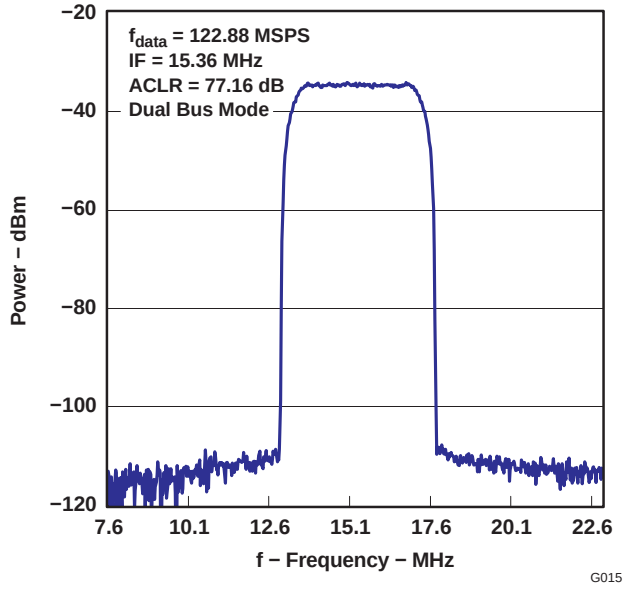


Figure 15. Power vs Frequency

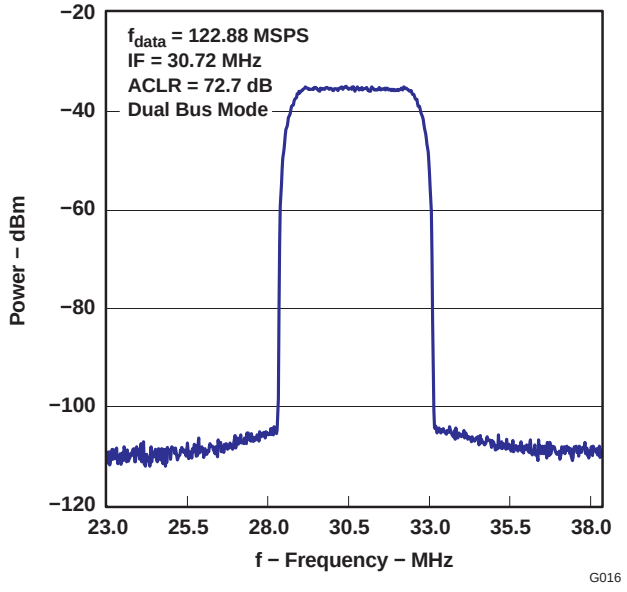


Figure 16. Power vs Frequency

7 Detailed Description

7.1 Overview

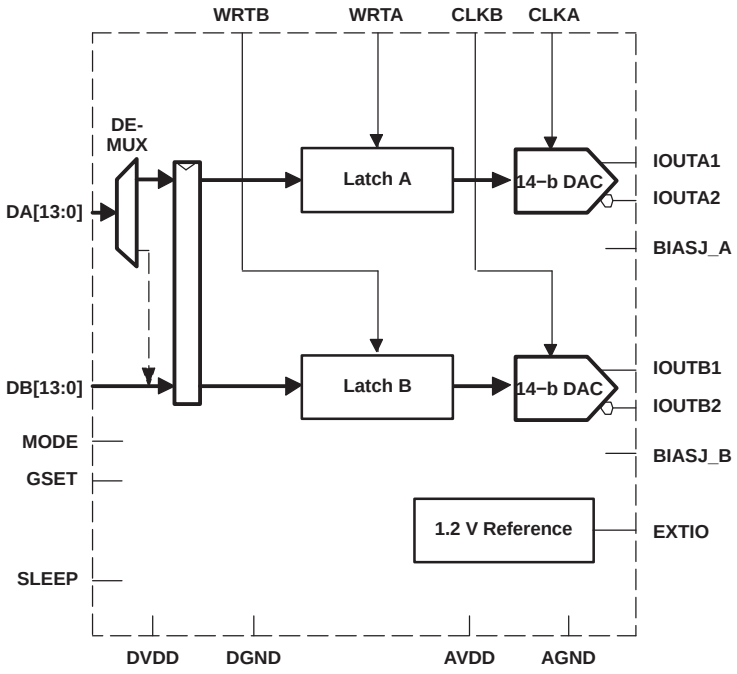
The architecture of the DAC5672A uses a current steering technique to enable fast switching and high update rate. The core element within the monolithic DAC is an array of segmented current sources that are designed to deliver a full-scale output current of up to 20 mA. An internal decoder addresses the differential current switches each time the DAC is updated and a corresponding output current is formed by steering all currents to either output summing node, IOUT1 or IOUT2. The complementary outputs deliver a differential output signal, which improves the dynamic performance through reduction of even-order harmonics, common-mode signals (noise), and double the peak-to-peak output signal swing by a factor of two, as compared to single-ended operation.

The segmented architecture results in a significant reduction of the glitch energy and improves the dynamic performance (SFDR) and DNL. The current outputs maintain a very high output impedance of greater than 300 kΩ.

When pin 42 (GSET) is high (simultaneous gain set mode), the full-scale output current for DACs is determined by the ratio of the internal reference voltage (1.2 V) and an external resistor (R_{SET}) connected to BIASJ_A. When GSET is low (independent gain set mode), the full-scale output current for each DAC is determined by the ratio of the internal reference voltage (1.2 V) and separate external resistors (R_{SET}) connected to BIASJ_A and BIASJ_B. The resulting I_{REF} is internally multiplied by a factor of 32 to produce an effective DAC output current that can range from 2 mA to 20 mA, depending on the value of R_{SET}.

The DAC5672A is split into a digital and an analog portion, each of which is powered through its own supply pin. The digital section includes edge-triggered input latches and the decoder logic, while the analog section comprises both the current source array with its associated switches, and the reference circuitry.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Interfaces

The DAC5672A features two operating modes selected by the MODE pin, as shown in Table 1.

- For dual-bus input mode, the device essentially consists of two separate DACs. Each DAC has its own separate data input bus, clock input, and data write signal (data latch-in).
- In single-bus interleaved mode, the data must be presented interleaved at the A-channel input bus. The B-channel input bus is not used in this mode. The clock and write input are now shared by both DACs.

Table 1. Operating Modes

MODE PIN	BUS INPUT
MODE pin connected to DGND	Single-bus interleaved mode, clock and write input equal for both DACs
MODE pin connected to DVDD	Dual-bus mode, DACs operate independently

7.3.2 Dual-Bus Data Interface and Timing

In dual-bus mode, the MODE pin is connected to DVDD. The two converter channels within the DAC5672A consist of two independent, 14-bit, parallel data ports. Each DAC channel is controlled by its own set of write (WRTA, WRTB) and clock (CLKA, CLKB) lines. The WRTA, WRTB lines control the channel input latches and the CLKA, CLKB lines control the DAC latches. The data is first loaded into the input latch by a rising edge of the WRTA, WRTB line.

The internal data transfer requires a correct sequence of write and clock inputs, since essentially two clock domains having equal periods (but possibly different phases) are input to the DAC5672A. The DAC5672A is defined by a minimum requirement of the time between the rising edge of the clock and the rising edge of the write inputs. The rising edge of CLKA, CLKB must occur at the same time or before the rising edge of the WRTA, WRTB signal. A minimum delay of 2 ns must be maintained if the rising edge of the clock occurs after the rising edge of the write. Note that these conditions are satisfied when the clock and write inputs are connected externally. Note that all specifications were measured with the WRTA, WRTB and CLKA, CLKB lines connected together.

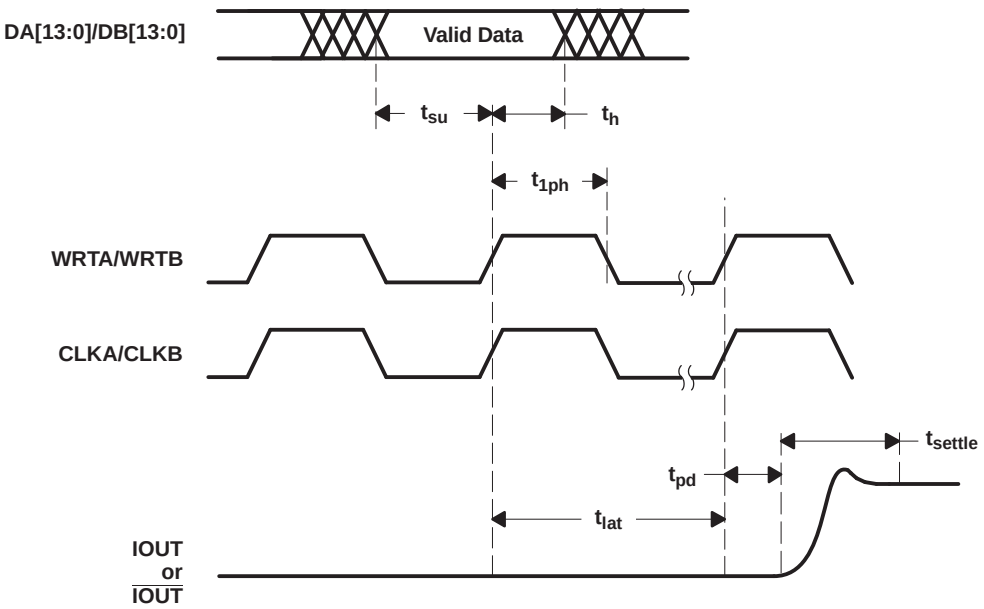


Figure 17. Dual-Bus Mode Operation

7.3.3 Single-Bus Interleaved Data Interface and Timing

In single-bus interleaved mode, the MODE pin is connected to DGND. Figure 18 shows the timing diagram. In interleaved mode, the A- and B-channels share the write input (WRTIQ) and update clock (CLKIQ and internal CLKDACIQ). Multiplexing logic directs the input word at the A-channel input bus to either the A-channel input latch (SELECTIQ is high) or to the B-channel input latch (SELECTIQ is low). When SELECTIQ is high, the data value in the B-channel latch is retained by presenting the latch output data to its input again. When SELECTIQ is low, the data value in the A-channel latch is retained by presenting the latch output data to its input.

In interleaved mode, the A-channel input data rate is twice the update rate of the DAC core. As in dual-bus mode, it is important to maintain a correct sequence of write and clock inputs. The edge-triggered flip-flops latch the A- and B-channel input words on the rising edge of the write input (WRTIQ). This data is presented to the A- and B-DAC latches on the following falling edge of the write inputs. The DAC5672A clock input is divided by a factor of two before it is presented to the DAC latches.

Correct pairing of the A- and B-channel data is done by RESETIQ. In interleaved mode, the clock input CLKIQ is divided by two, which would translate to a non-deterministic relation between the rising edges of the CLKIQ and CLKDACIQ. RESETIQ ensures, however, that the correct position of the rising edge of CLKDACIQ with respect to the data at the input of the DAC latch is determined. CLKDACIQ is disabled (low) when RESETIQ is high.

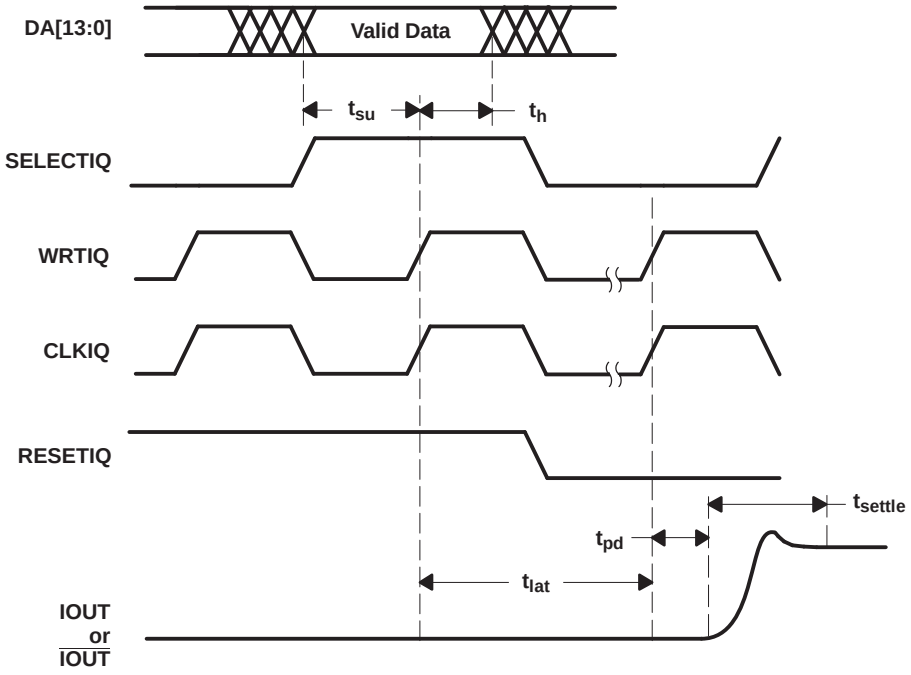


Figure 18. Single-Bus Interleaved Mode Operation

7.4 Device Functional Modes

7.4.1 DAC Transfer Function

Each of the DACs in the DAC5672A has a set of complementary current outputs, IOUT1 and IOUT2. The full-scale output current, I_{OUTFS}, is the summation of the two complementary output currents:

$$I_{OUTFS} = I_{OUT1} + I_{OUT2} \quad (1)$$

The individual output currents depend on the DAC code and can be expressed as:

$$I_{OUT1} = I_{OUTFS} \times \left(\frac{Code}{16384}\right) \quad (2)$$

$$I_{OUT2} = I_{OUTFS} \times \left(\frac{16383 - Code}{16384}\right) \quad (3)$$

Device Functional Modes (continued)

where Code is the decimal representation of the DAC data input word. Additionally, I_{OUTFS} is a function of the reference current I_{REF}, which is determined by the reference voltage and the external setting resistor (R_{SET}).

$$I_{OUTFS} = 32 \times I_{REF} = 32 \times \frac{V_{REF}}{R_{SET}} \quad (4)$$

In most cases, the complementary outputs drive resistive loads or a terminated transformer. A signal voltage develops at each output according to:

$$V_{OUT1} = I_{OUT1} \times R_{LOAD} \quad (5)$$

$$V_{OUT2} = I_{OUT2} \times R_{LOAD} \quad (6)$$

The value of the load resistance is limited by the output compliance specification of the DAC5672A. To maintain specified linearity performance, the voltage for IOUT1 and IOUT2 must not exceed the maximum allowable compliance range.

The total differential output voltage is:

$$V_{OUTDIFF} = V_{OUT1} - V_{OUT2} \quad (7)$$

$$V_{OUTDIFF} = \frac{(2 \times Code - 16383)}{16384} \times I_{OUTFS} \times R_{LOAD} \quad (8)$$

7.4.2 Analog Outputs

The DAC5672A provides two complementary current outputs, IOUT1 and IOUT2. The simplified circuit of the analog output stage representing the differential topology is shown in Figure 19. The output impedance of IOUT1 and IOUT2 results from the parallel combination of the differential switches, along with the current sources and associated parasitic capacitances.

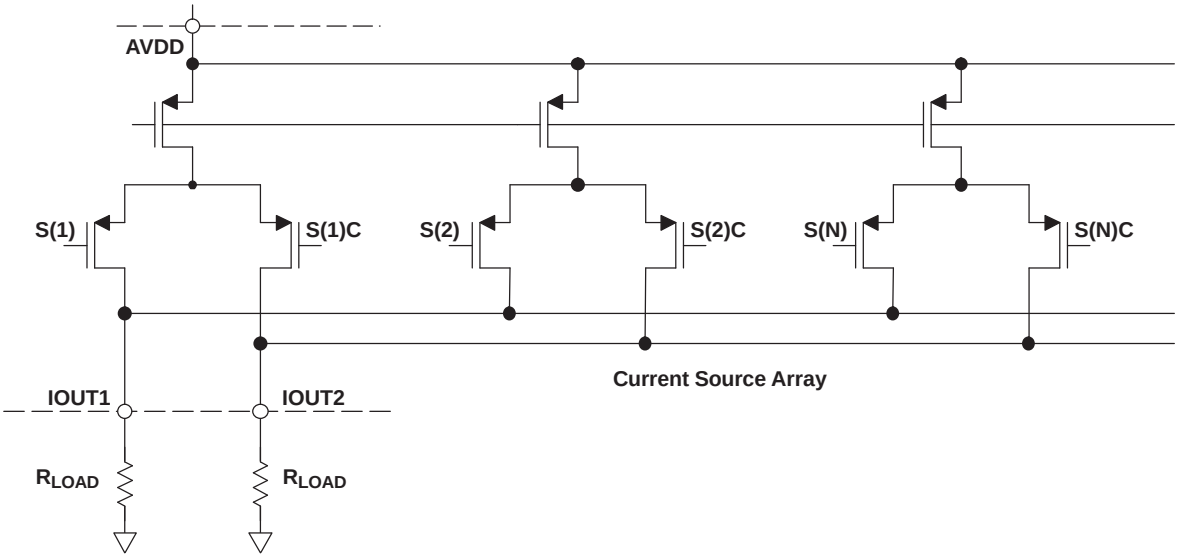


Figure 19. Analog Outputs

The signal voltage swing that may develop at the two outputs, IOUT1 and IOUT2, is limited by a negative and positive compliance. The negative limit of –1 V is given by the breakdown voltage of the CMOS process and exceeding it compromises the reliability of the DAC5672A (or even causes permanent damage). With the full-scale output set to 20 mA, the positive compliance equals 1.2 V. Note that the compliance range decreases to about 1 V for a selected output current of I_{OUTFS} = 2 mA. Care must be taken that the configuration of DAC5672A does not exceed the compliance range to avoid degradation of the distortion performance and integral linearity.

Device Functional Modes (continued)

Best distortion performance is typically achieved with the maximum full-scale output signal limited to approximately 0.5 V_{PP}. This is the case for a 50-Ω doubly-terminated load and a 20-mA full-scale output current. A variety of loads can be adapted to the output of the DAC5672A by selecting a suitable transformer while maintaining optimum voltage levels at IOUT1 and IOUT2. Furthermore, using the differential output configuration in combination with a transformer is instrumental for achieving excellent distortion performance. Common-mode errors, such as even-order harmonics or noise, can be substantially reduced. This is particularly the case with high output frequencies.

For those applications requiring the optimum distortion and noise performance, it is recommended to select a full-scale output of 20 mA. A lower full-scale range of 2 mA may be considered for applications that require low power consumption, but can tolerate a slight reduction in performance level.

7.4.3 Output Configurations

The current outputs of the DAC5672A allow for a variety of configurations. As mentioned previously, utilizing the converter's differential outputs yield the best dynamic performance. Such a differential output circuit may consist of an RF transformer or a differential amplifier configuration. The transformer configuration is ideal for most applications with ac coupling, while op amps are suitable for a dc-coupled configuration.

The single-ended configuration may be considered for applications requiring a unipolar output voltage. Connecting a resistor from either one of the outputs to ground converts the output current into a ground-referenced voltage signal. To improve on the dc linearity by maintaining a virtual ground, an I-to-V or op-amp configuration may be considered.

7.4.4 Differential With Transformer

Using an RF transformer provides a convenient way of converting the differential output signal into a single-ended signal while achieving excellent dynamic performance. The appropriate transformer must be carefully selected based on the output frequency spectrum and impedance requirements.

The differential transformer configuration has the benefit of significantly reducing common-mode signals, thus improving the dynamic performance over a wide range of frequencies. Furthermore, by selecting a suitable impedance ratio (winding ratio) the transformer can provide optimum impedance matching while controlling the compliance voltage for the converter outputs.

Figure 20 and Figure 21 show 50-Ω doubly-terminated transformer configurations with 1:1 and 4:1 impedance ratios, respectively. Note that the center tap of the primary input of the transformer has to be grounded to enable a dc-current flow. Applying a 20-mA full-scale output current would lead to a 0.5-V_{PP} output for a 1:1 transformer and a 1-V_{PP} output for a 4:1 transformer. In general, the 1:1 transformer configuration will have slightly better output distortion, but the 4:1 transformer will have 6 dB higher output power.

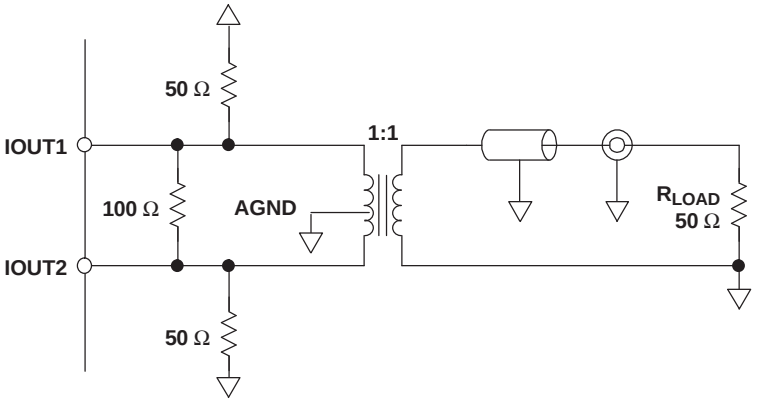


Figure 20. Driving a Doubly-Terminated 50-Ω Cable Using a 1:1 Impedance Ratio Transformer

Device Functional Modes (continued)

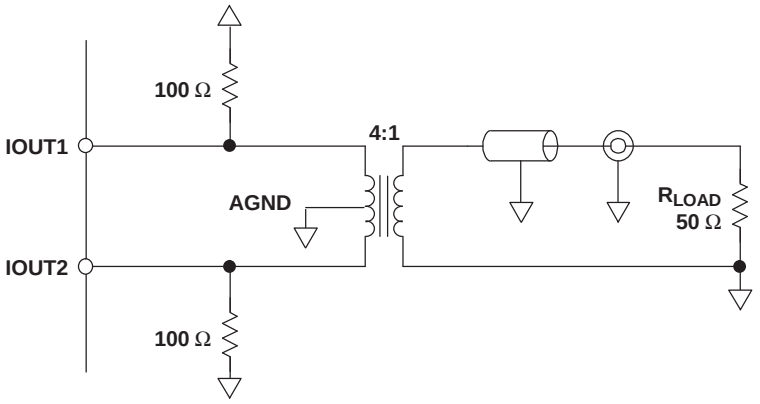


Figure 21. Driving a Doubly-Terminated 50-Ω Cable Using a 4:1 Impedance Ratio Transformer

7.4.5 Single-Ended Configuration

Figure 22 shows the single-ended output configuration, where the output current I_{OUT1} flows into an equivalent load resistance of 25 Ω. Node IOUT2 must be connected to AGND or terminated with a resistor of 25 Ω to AGND. The nominal resistor load of 25 Ω gives a differential output swing of 1 V_{PP} when applying a 20-mA full-scale output current.

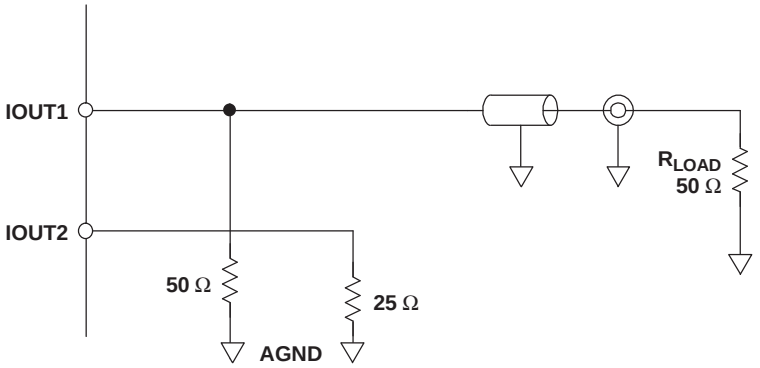


Figure 22. Driving a Doubly-Terminated 50-Ω Cable Using a Single-Ended Output

7.4.6 Reference Operation

7.4.6.1 Internal Reference

The DAC5672A has an on-chip reference circuit which comprises a 1.2-V bandgap reference and two control amplifiers, one for each DAC. The full-scale output current, I_{OUTFS}, of the DAC5672A is determined by the reference voltage, V_{REF}, and the value of resistor R_{SET}. I_{OUTFS} can be calculated by:

$$I_{OUTFS} = 32 \times I_{REF} = 32 \times \frac{V_{REF}}{R_{SET}} \quad (9)$$

The reference control amplifier operates as a V-to-I converter producing a reference current, I_{REF}, which is determined by the ratio of V_{REF} and R_{SET} (see Equation 9). The full-scale output current, I_{OUTFS}, results from multiplying I_{REF} by a fixed factor of 32.

Using the internal reference, a 2-kΩ resistor value results in a full-scale output of approximately 20 mA. Resistors with a tolerance of 1% or better should be considered. Selecting higher values, the output current can be adjusted from 20 mA down to 2 mA. Operating the DAC5672A at lower than 20-mA output currents may be desirable for reasons of reducing the total power consumption, improving the distortion performance, or observing the output compliance voltage limitations for a given load condition.

Device Functional Modes (continued)

It is recommended to bypass the EXTIO pin with a ceramic chip capacitor of 0.1 μF or more. The control amplifier is internally compensated and its small signal bandwidth is approximately 300 kHz.

7.4.6.2 External Reference

The internal reference can be disabled by simply applying an external reference voltage into the EXTIO pin, which in this case functions as an input. The use of an external reference may be considered for applications that require higher accuracy and drift performance or to add the ability of dynamic gain control.

While a 0.1-μF capacitor is recommended to be used with the internal reference, it is optional for the external reference operation. The reference input, EXTIO, has a high input impedance (1 MΩ) and can easily be driven by various sources. Note that the voltage range of the external reference must stay within the compliance range of the reference input.

7.4.6.3 Gain Setting Option

The full-scale output current on the DAC5672A can be set two ways: either for each of the two DAC channels independently or for both channels simultaneously. For the independent gain set mode, the GSET pin (pin 42) must be low (that is, connected to AGND). In this mode, two external resistors are required — one RSET connected to the BIASJ_A pin (pin 44) and the other to the BIASJ_B pin (pin 41). In this configuration, the user has the flexibility to set and adjust the full-scale output current for each DAC independently, allowing for the compensation of possible gain mismatches elsewhere within the transmit signal path.

Alternatively, bringing the GSET pin high (that is, connected to AVDD), the DAC5672A switches into the simultaneous gain set mode. Now the full-scale output current of both DAC channels is determined by only one external R_{SET} resistor connected to the BIASJ_A pin. The resistor at the BIASJ_B pin may be removed; however, this is not required since this pin is not functional in this mode and the resistor has no effect on the gain equation.

7.4.6.4 Sleep Mode

The DAC5672A features a power-down function which can reduce the total supply current to approximately 3.1 mA over the specified supply range if no clock is present. Applying a logic high to the SLEEP pin initiates the power-down mode, while a logic low enables normal operation. When left unconnected, an internal active pulldown circuit enables the normal operation of the converter.

7.5 Programming

7.5.1 Digital Inputs and Timing

7.5.1.1 Digital Inputs

The data input ports of the DAC5672A accept a standard positive coding with data bits DA13 and DB13 being the most significant bits (MSB). The converter outputs support a clock rate of up to 275 MSPS. The best performance is typically achieved with a symmetric duty cycle for write and clock; however, the duty cycle may vary as long as the timing specifications are met. Similarly, the setup and hold times may be chosen within their specified limits.

All digital inputs of the DAC5672A are CMOS compatible. Figure 23 and Figure 24 show schematics of the equivalent CMOS digital inputs of the DAC5672A. The pullup and pulldown circuitry is approximately equivalent to 100 kΩ. The 14-bit digital data input follows the offset positive binary coding scheme. The DAC5672A is designed to operate with a digital supply (DVDD) of 3 V to 3.6 V.

Programming (continued)

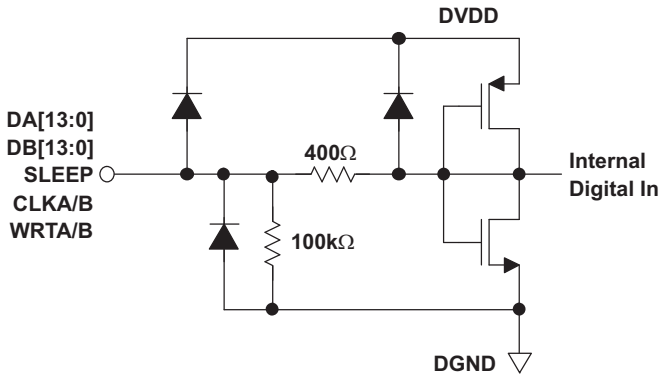


Figure 23. CMOS/TTL Digital Equivalent Input With Internal Pulldown Resistor

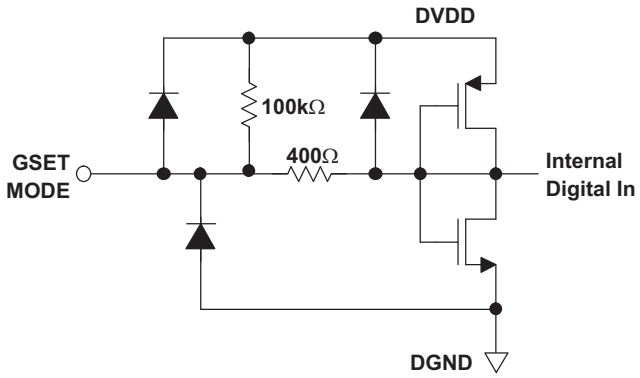


Figure 24. CMOS/TTL Digital Equivalent Input With Internal Pullup Resistor

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.2 Typical Application

A typical application for the DAC5672A is as dual or single carrier transmitter. The DAC is provided with some input digital baseband signal and it outputs an analog carrier. A typical configuration is described below.

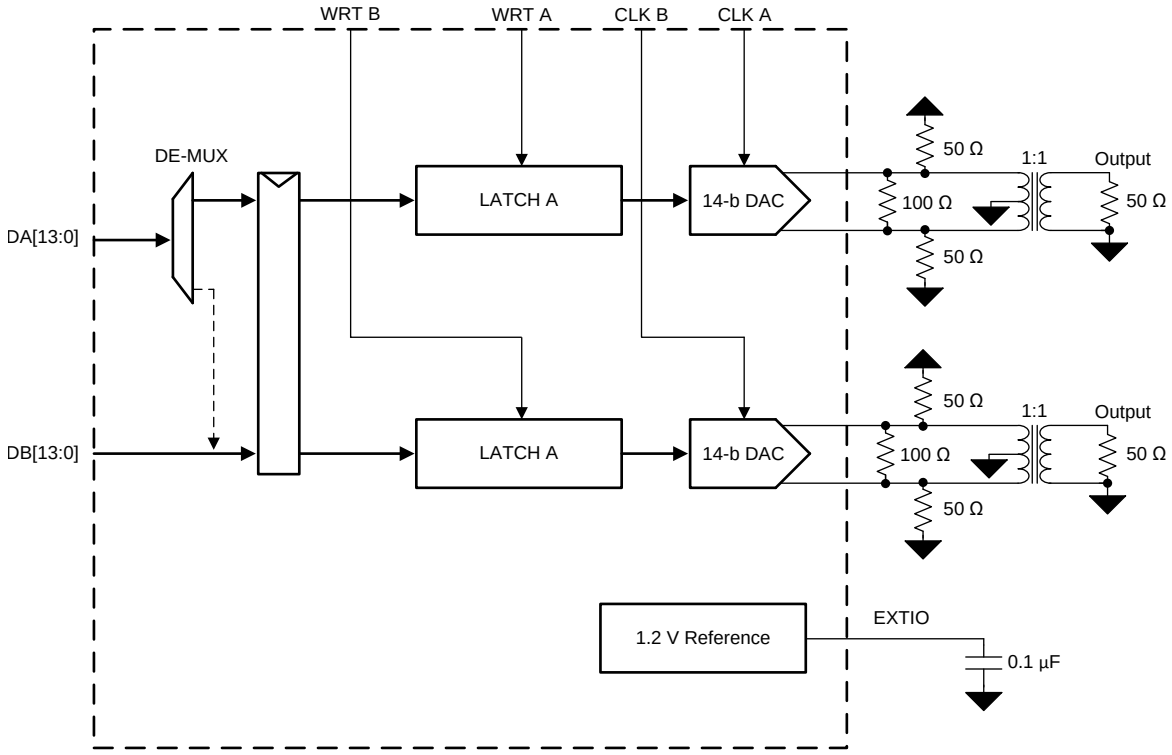


Figure 25. Typical Application Schematic

- Clock rate = 122.88 MHz
- Input data = WCDMA with IF frequency at 30.72 MHz
- AVDD= DVDD = 3.3 V

8.2.1 Design Requirements

The requirements for this design were to generate a single WCDMA signal at an intermediate frequency of 30.72 MHz. The ACLR needs to be better than 72 dBc.

8.2.2 Detailed Design Procedure

The single carrier signal with an intermediate frequency of 30.72 MHz must be created in the digital processor at a sample rate of 122.88 Msps for DAC. These 14 bit samples are placed on the 14b CMOS input port of the DAC.

Typical Application (continued)

A CMOS DAC clock must be generated from a clock source at 122.88 MHz. This must be provided to the CLK pin of the DAC.

The IOUTA and IOUTB differential connections must be connected to a transformer to provide a single ended output. A typical 1:1 impedance transformer is used on the device EVM. The DAC5672A EVM provides a good reference for this design example.

8.2.3 Application Curves

This spectrum analyzer plot shows the ACLR for the transformer output single carrier signal with intermediate frequency of 30.72 MHz. The results meet the system requirements for a minimum of 72 dBc ACLR.

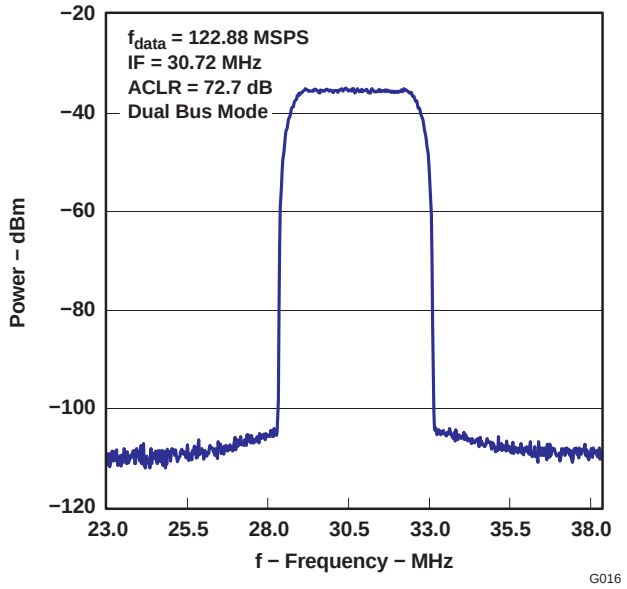


Figure 26. TBD

9 Power Supply Recommendations

It is recommended that the device be powered with the nominal supply voltages as indicated in the *Recommended Operating Conditions*.

In most instances the best performance is achieved with LDO supplies. However the supplies may be driven with direct outputs from a DC-DC switcher as long as the noise performance of the switcher is acceptable.

10 Layout

10.1 Layout Guidelines

The DAC5672A EVM layout should be used as a reference for the layout to obtain the best performance. A sample layout is shown in Figure 27 through Figure 30. Some important layout recommendations are:

1. Use a single ground plane. Keep the digital and analog signals on distinct separate sections of the board. This may be virtually divided down the middle of the device package when doing placement and layout.
2. Keep the analog outputs as far away from the switching clocks and digital signals as possible. This will keep coupling from the digital circuits to the analog outputs to a minimum.
3. Decoupling caps should be kept close to the power pins of the device.

10.2 Layout Example

The EVM is constructed on a 4-layer, 5.1-inch x 4.8-inch, 0.062-inch thick PCB using FR−4 material. Figure 27 through Figure 30 show the PCB layout for the EVM.

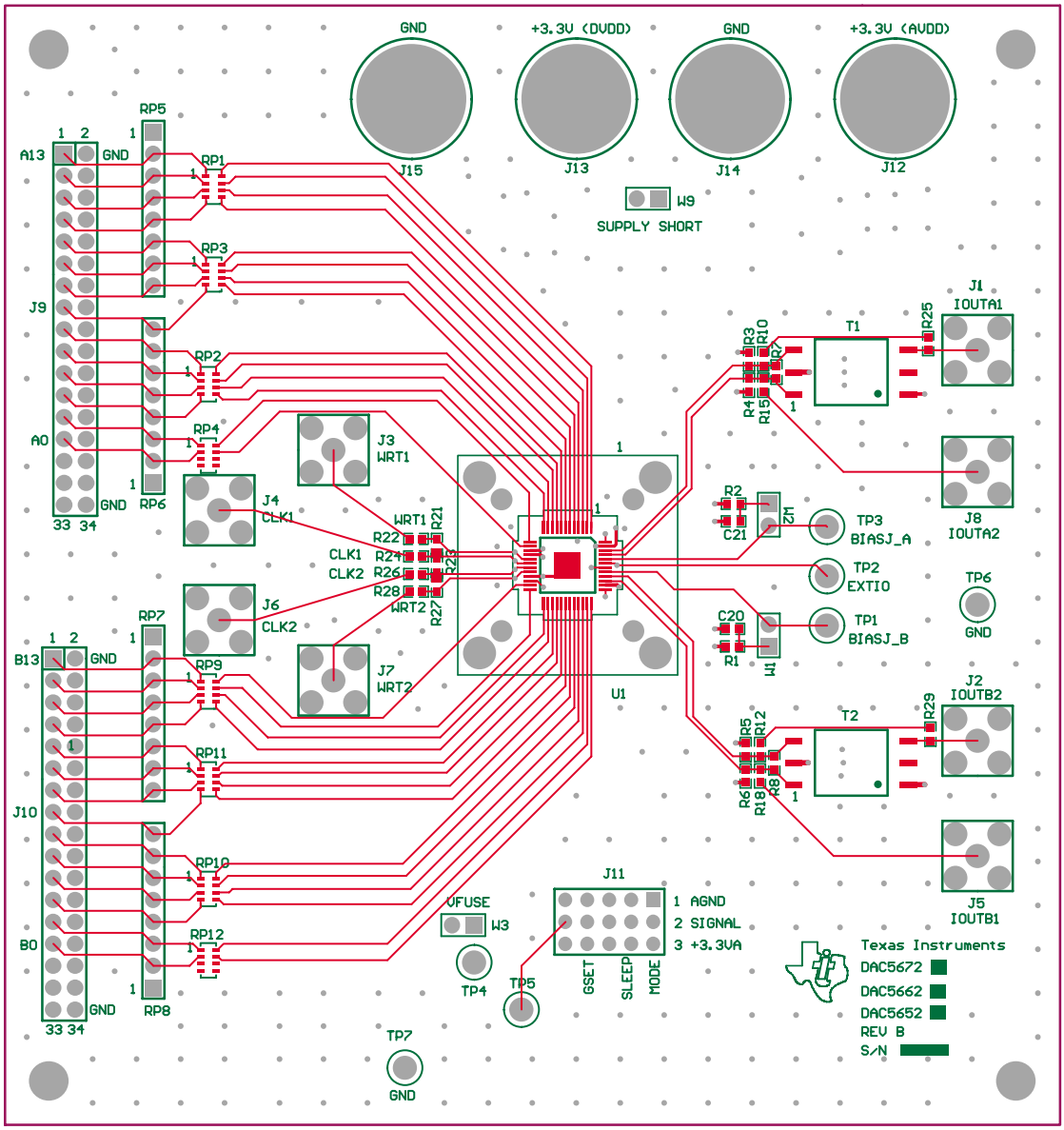


Figure 27. Top Layer 1

Layout Example (continued)

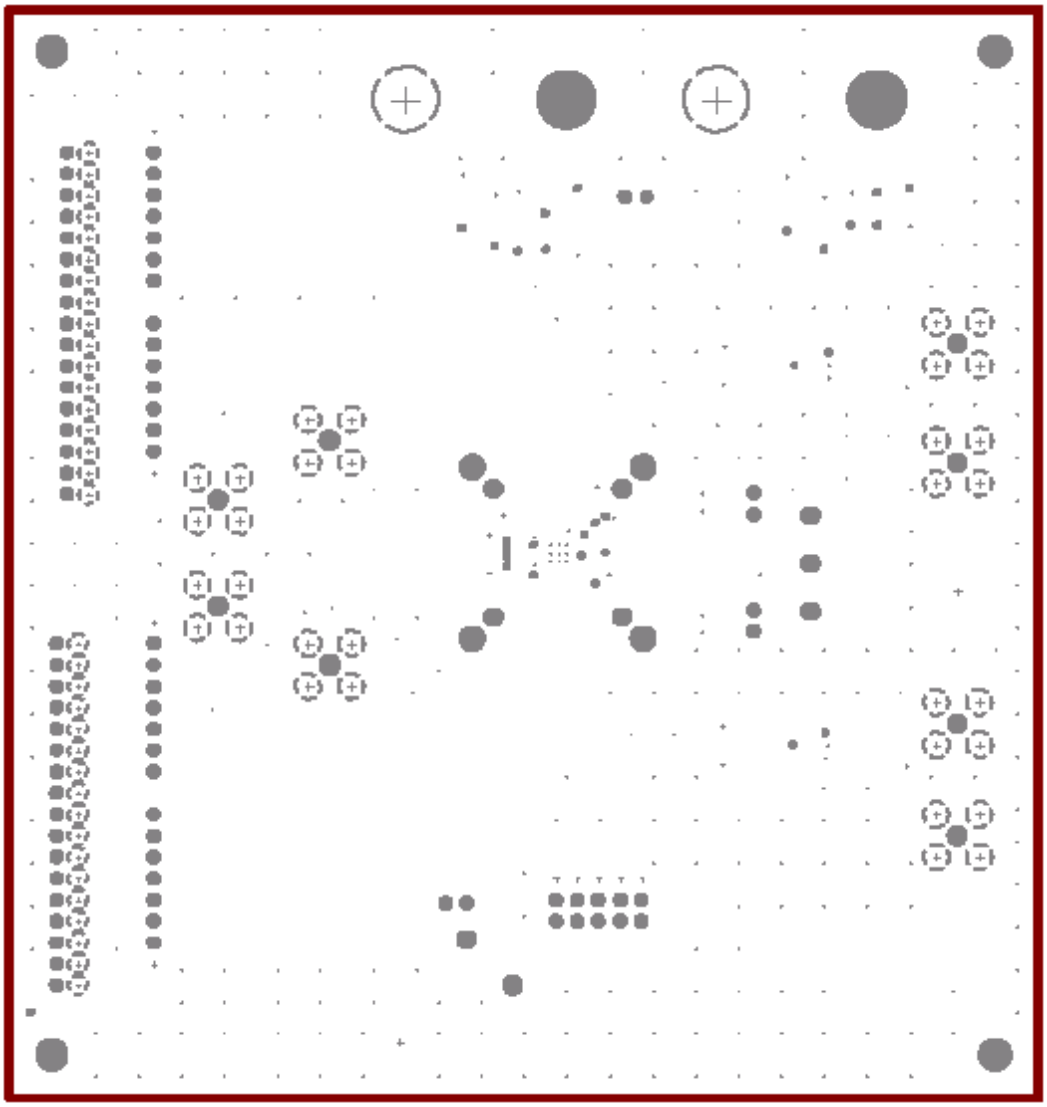


Figure 28. Ground Plane Layer 2

Layout Example (continued)

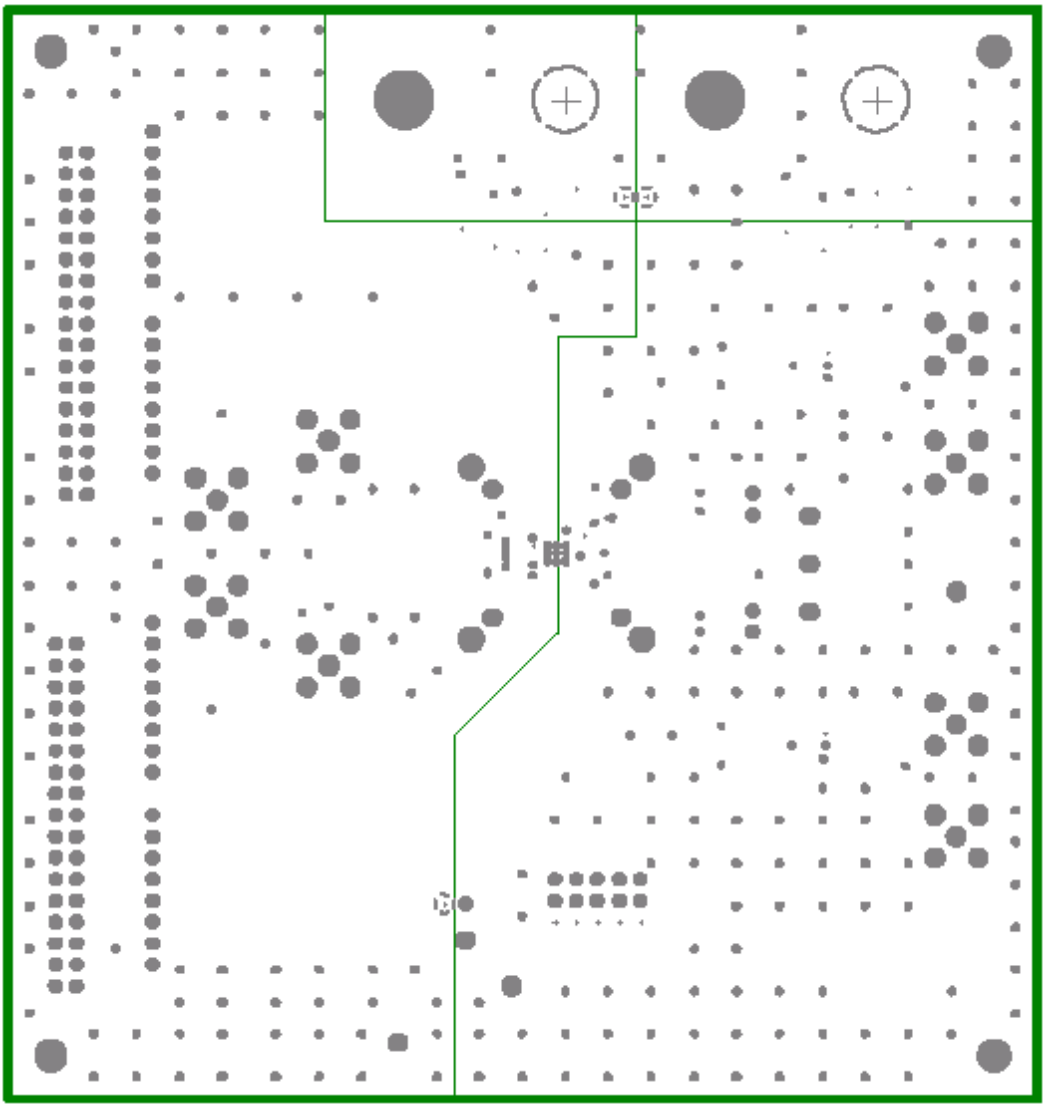


Figure 29. Power Plane Layer 3

Layout Example (continued)

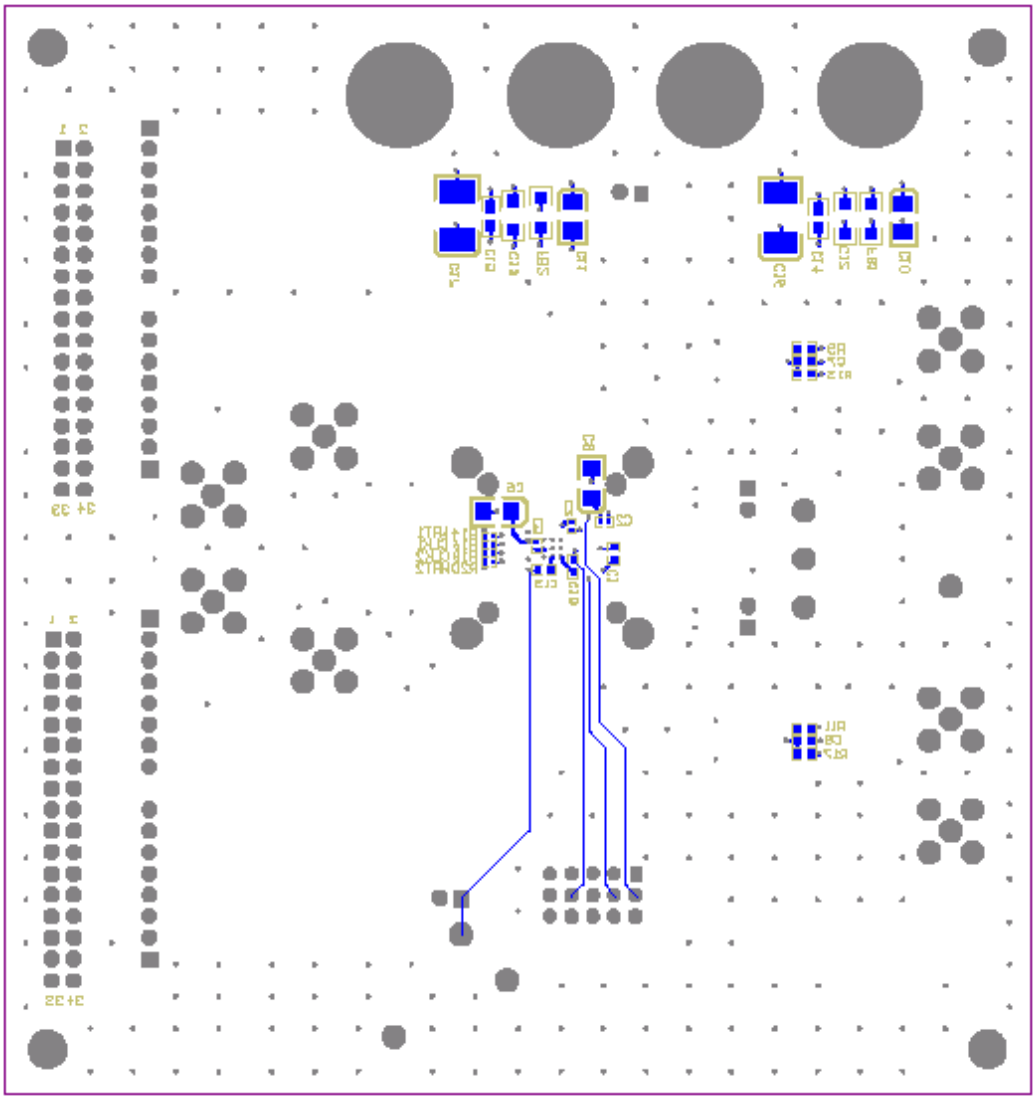


Figure 30. Bottom Layer 4

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.2 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™オンライン・コミュニティ ***TIのE2E（Engineer-to-Engineer）コミュニティ。*****エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。**

設計サポート ***TIの設計サポート*** **役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。**

11.3 商標

E2E is a trademark of Texas Instruments.

11.4 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DAC5672AIPFB	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC5672AI
DAC5672AIPFB.A	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC5672AI
DAC5672AIPFBG4	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC5672AI
DAC5672AIPFBR	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC5672AI
DAC5672AIPFBR.A	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC5672AI

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

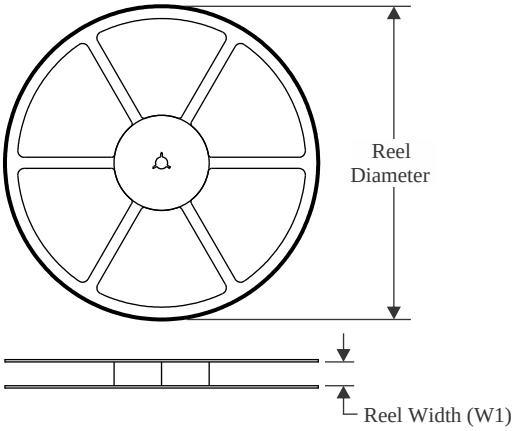
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

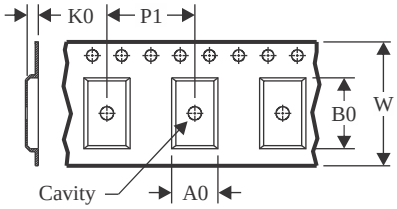
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

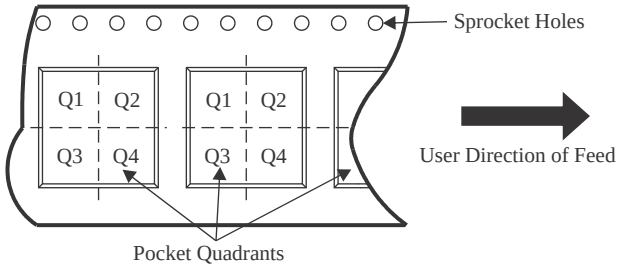


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

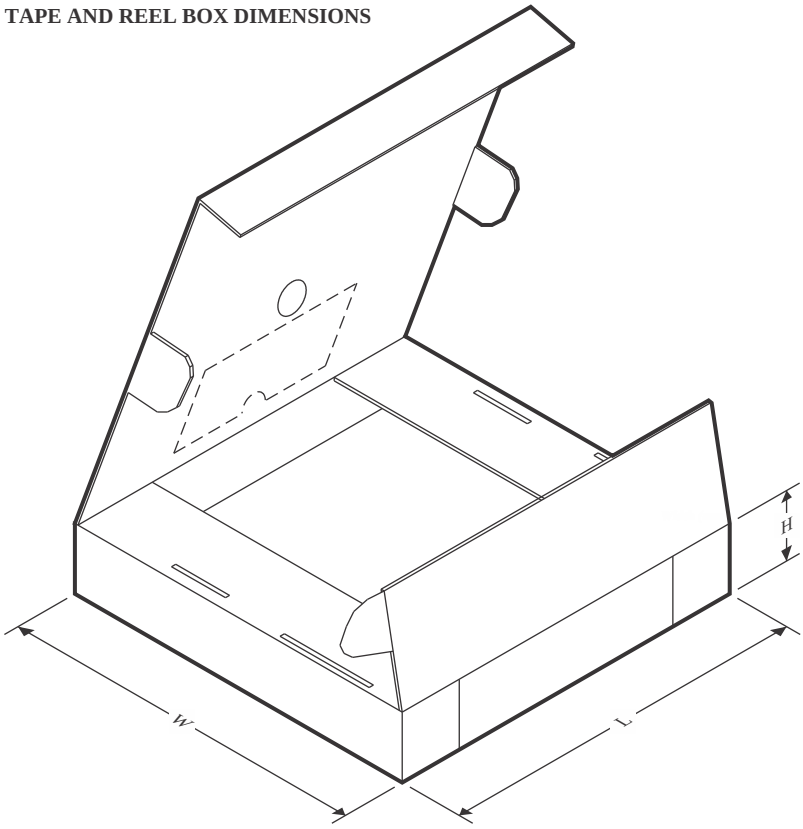
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC5672AIPFBR	TQFP	PFB	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2

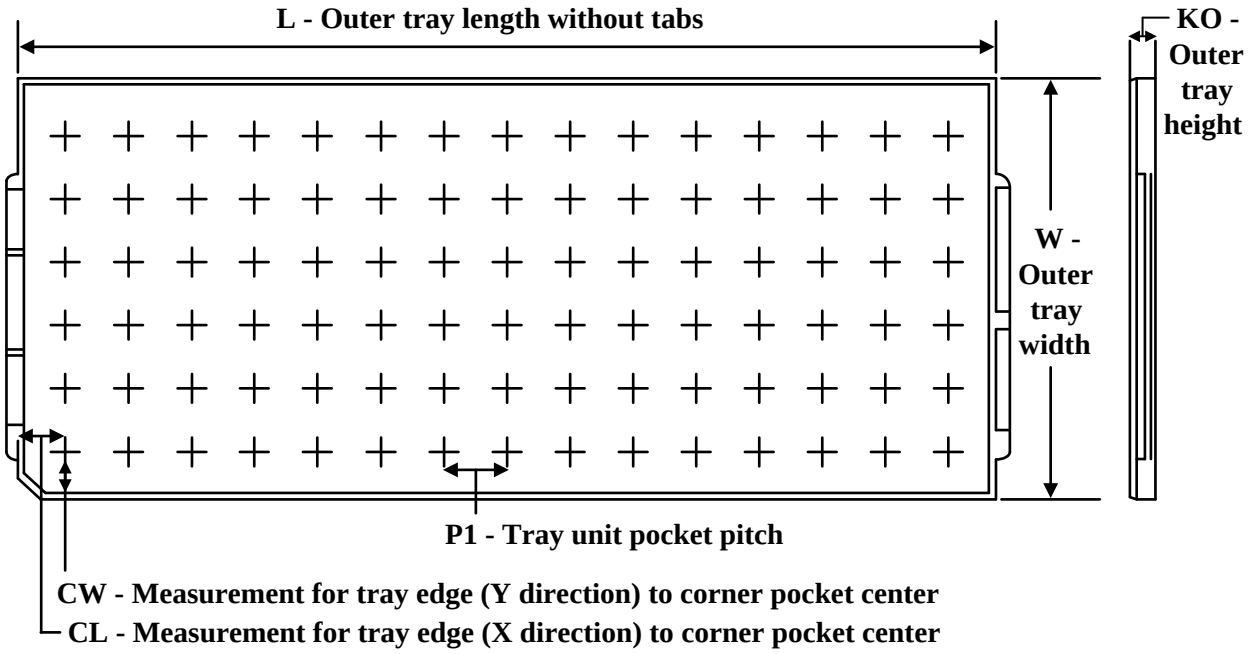
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC5672AIPFBR	TQFP	PFB	48	1000	367.0	367.0	38.0

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

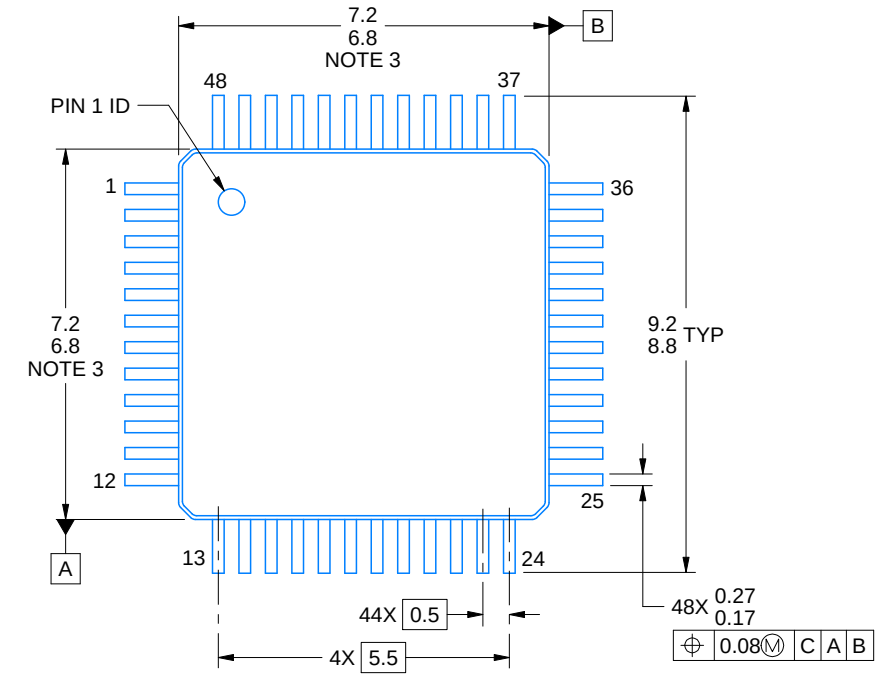
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
DAC5672AIPFB	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.5	11.25
DAC5672AIPFB.A	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.5	11.25
DAC5672AIPFBG4	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.5	11.25

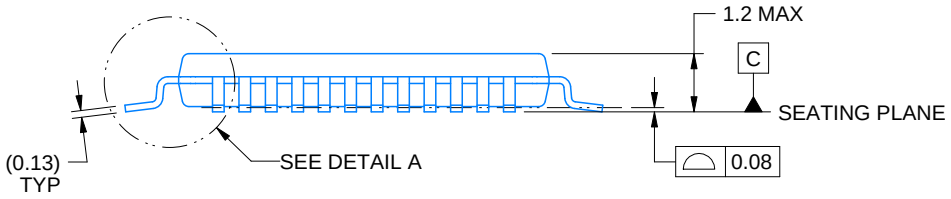
PACKAGE OUTLINE

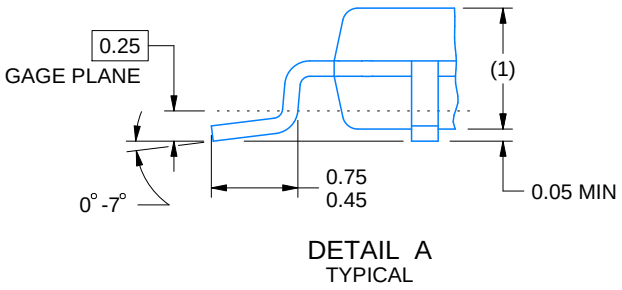
PFB0048A

TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK







DETAIL A
TYPICAL

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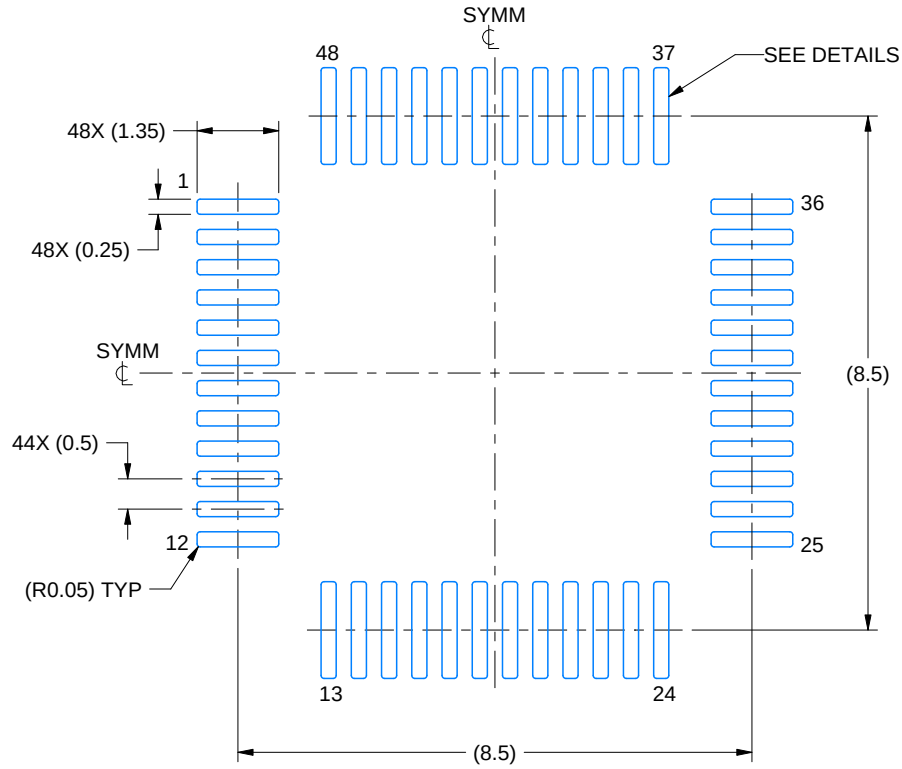
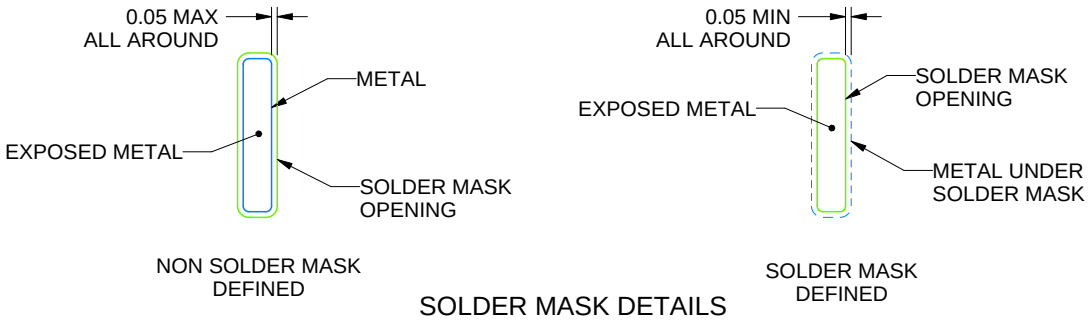
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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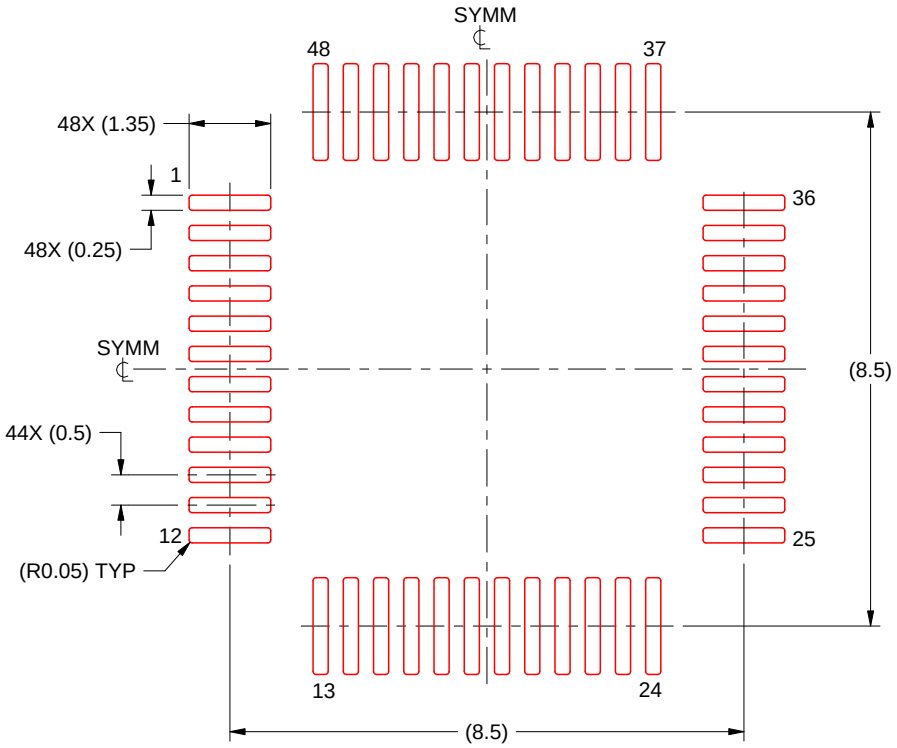
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
SCALE:8X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月