DACx750 シングル・チャネル、12 および 16 ビット、プログラム可能な電流出力、4mA～20mA 電流ループ・アプリケーション向け D/A コンバータ

1 特長

- 電流出力オプション:
  - 0mA～24mA
  - 4mA～20mA
  - 0mA～20mA
- 総合未調整誤差(TUE):±0.1% FSR (標準値)
- DNL:±1 LSB (最大値)
- 最大ループ・コンプライアンス電圧:AVDD – 2V
- 内部 5V 基準電圧:10ppm/℃ (最大値)
- 4.6V 電源出力を内蔵
- CRC フレーム・エラー・チェック
- ウォッチドッグ・タイマ
- サーマル・アラーム
- 断線アラーム
- 出力電流を監視する端子
- オンチップのフォルト・アラーム
- オフセットおよびゲインのユーザー較正
- 広い温度範囲:–40℃～+125℃
- パッケージ:6mm × 6mm 40 ピン VQFN および 24 ピン HTSSOP

2 アプリケーション

- アナログ出力モジュール
- CPU (PLC コントローラ)
- 流量トランスミッタ
- その他のセンサ・トランスミッタ
- アクチュエータ
- プロセス分析 (pH、ガス、濃度、力、湿度)

3 概要

DAC7750 および DAC8750 (DACx750) は、低コスト、高精度の完全統合型 12 ビットおよび 16 ビット D/A コンバータ (DAC) であり、産業用プロセス制御アプリケーションの要件を満たすよう設計されています。これらのデバイスは、4 mA～20mA、0mA～20 mA、または 0 mA～24mA の範囲の電流出力としてプログラムできます。DACx750 は、SPI フレームの CRC エラー・チェック、ウォッチドッグ・タイマ、断線検出、コンプライアンス電圧、サーマル・アラームなどの信頼性機能を備えています。さらに、内部の高精度抵抗にアクセスすることにより、出力電流を監視できます。

これらのデバイスは、パワーオン・リセット機能を備えており、電源オン時には既知の状態 (IOUT はディセーブルで Hi-Z 状態) になるように設計されています。CLR ピンは、出力が有効な場合に、電流出力を範囲の下限に設定します。ゼロ・レジスタおよびゲイン・レジスタをプログラムして、最終システムの中でデバイスをデジタル的に較正できます。出力のスルー・レートも、レジスタによりプログラム可能です。電流出力に外部の HART® 信号を重ね合わせることができます。これらのデバイスは、10V ~ 36V の電源電圧で動作します。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
DACx750	HTSSOP (24)	7.80mm × 4.40mm
	VQFN (40)	6.00mm × 6.00mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。

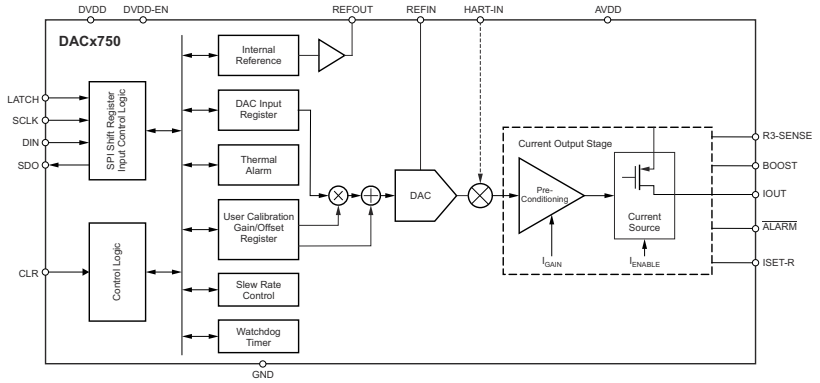

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Table of Contents

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (January 2018) to Revision D (December 2021)	Page
• 文書全体にわたって表、図、相互参照の採番方法を更新	1
• Changed *Loop compliance voltage* to *Reference input voltage*, and *Reference input voltage* to *External reference current* in *Recommended Operating Conditions*	5
• Changed *Digital input low voltage* test condition upper limit from 2.6 V to 3.6 V in *Recommended Operating Conditions*	5
• Deleted *Timing Requirements: Daisy-Chain Mode* section and *Daisy-Chain Mode Timing* figure	10
• Deleted *Power-Supply Sequence* section; content moved to *Power Supply Recommendations* section	21
• Deleted daisy-chain operation content from *Watchdog Timer* section	23
• Deleted *The DACx750 Shares the SPI Bus With Other Devices* subsection from *Watchdog Timer* section	23
• Deleted daisy-chain operation from *Frame Error Checking* section	23
• Added CRC fault reset command of 0x96 to *Frame Error Checking* section	23
• Deleted *The DACx750 Shares the SPI Bus With Other Devices* subsection	23
• Changed duplicated 010 step-size from 0.125 to 0.25 in Table 8-3, *Slew Rate Step-Size Options*	25
• Added CRC fault reset command to Table 8-8, *Write Address Functions*	30
• Deleted *Daisy-Chain Operation* section	31
• Added *Multiple Devices on the Bus* section	31
• Changed Table 8-11 to delete daisy-chain operation and add CRC fault reset	32
• Changed *DCEN* to *Reserved* for DB3 in *Control Register* table	32
• Deleted text stating CAP2 pin is only available for the 40-pin VQFN package	35
• Added series resistance for supply and corrected HART-IN capacitance for Figure 9-3	37
• Added content from deleted *Power-Supply Sequence* section to *Power Supply Recommendations* section	40
• Added fast supply ramp and series resistance content to *Power-Supply Recommendations*	40
• Added power supply series resistance to Figure 11-1, *Layout Example*	41

Changes from Revision B (June 2016) to Revision C (January 2018)	Page
• Added last paragraph to *User Calibration* section	24
• Added last paragraph to *Programmable Slew Rate* section	25

5 Device Comparison Table

PRODUCT	RESOLUTION	TUE (FSR)	DIFFERENTIAL NONLINEARITY (LSB)
DAC8750	16	0.2%	±1
DAC7750	12	0.2%	±1

6 Pin Configuration and Functions

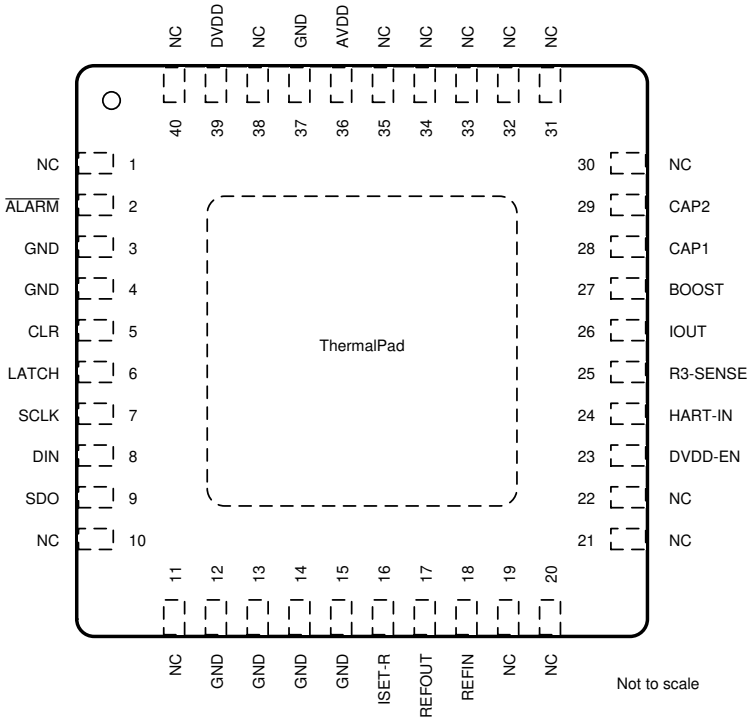


図 6-1. RHA Package, 40-Pin VQFN, Top View

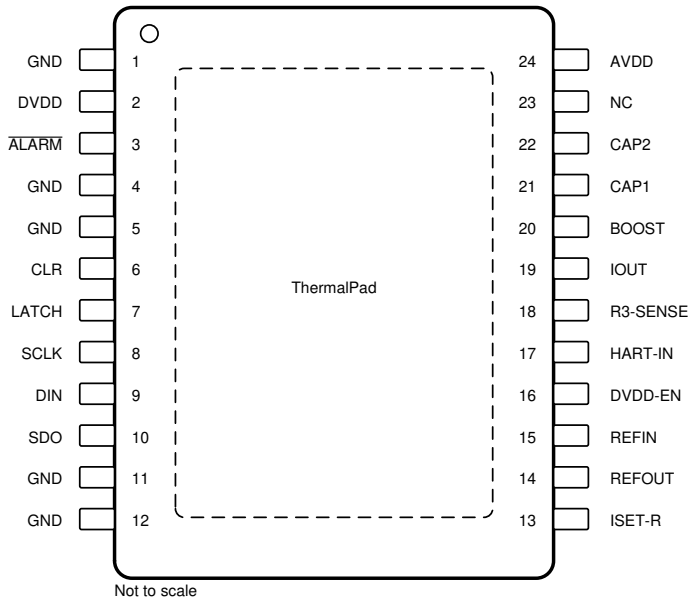


図 6-2. PWP Package, 24-Pin HTSSOP, Top View

表 6-1. Pin Functions

PIN			TYPE	DESCRIPTION
NAME	RHA (VQFN)	PWP (HTSSOP)		
$\overline{\text{ALARM}}$	2	3	Digital output	Alarm pin. Open drain output. External pullup resistor required (10 kΩ). The pin goes low (active) when the $\overline{\text{ALARM}}$ condition is detected (open circuit, over temperature, timeout, and so on).
AVDD	36	24	Supply input	Positive analog power supply.
BOOST	27	20	Analog output	Boost pin. External transistor connection (optional).
CAP1	28	21	Analog input	Connection for output filtering capacitor (optional).
CAP2	29	22	Analog input	Connection for output filtering capacitor (optional).
CLR	5	6	Digital input	Clear input. Logic high on this pin causes the part to enter CLEAR state. Active high.
DIN	8	9	Digital input	Serial data input. Data are clocked into the 24-bit input shift register on the rising edge of the serial clock input. Schmitt-Trigger logic input.
DVDD	39	2	Supply input or output	Digital power supply. Can be input or output, depending on DVDD-EN pin.
DVDD-EN	23	16	Digital input	Internal power-supply enable pin. Connect this pin to GND to disable the internal supply, or leave this pin unconnected to enable the internal supply. When this pin is connected to GND, an external supply must be connected to the DVDD pin.
GND	12, 13, 14, 15, 37	1, 11, 12	Supply input	Ground reference point for all analog circuitry of the device.
GND	3, 4	4, 5	Supply input	Ground reference point for all digital circuitry of the device.
HART-IN	24	17	Analog input	Input pin for HART modulation.
IOUT	26	19	Analog output	Current output pin
ISET-R	16	13	Analog input	Connection pin for external precision resistor (15 kΩ). See *セクション 8* of this data sheet.
LATCH	6	7	Digital input	Load DAC registers input. A rising edge on this pin loads the input shift register data into the DAC data and control registers and updates the DAC output.
NC	1, 10, 11, 19, 20, 21, 22, 30, 31, 32, 33, 34, 35, 38, 40	23	—	No connection.
R3-SENSE	25	18	Analog output	This pin is used as a monitoring feature for the output current. The voltage measured between the R3-SENSE pin and the BOOST pin is directly proportional to the output current.
REFOUT	17	14	Analog output	Internal reference output. Connects to REFIN when using internal reference.
REFIN	18	15	Analog input	Reference input
SCLK	7	8	Digital input	Serial clock input of the SPI. Data can be transferred at rates up to 30 MHz. Schmitt-Trigger logic input.
SDO	9	10	Digital output	Serial data output. Data are valid on the rising edge of SCLK.
Thermal Pad	—	—	Supply input	The thermal pad is internally connected to GND. For enhanced thermal performance, thermally connect the pad to a copper plane. The pad can be electrically connected to the same potential as the GND pin or left electrically unconnected provided a supply connection is made at the GND pin.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
	AVDD to GND	–0.3	40	V
	DVDD to GND	–0.3	6	V
	IOUT to GND	–0.3	AVDD	V
	REFIN to GND	–0.3	6	V
	REFOUT to GND	–0.3	6	V
	$\overline{\text{ALARM}}$ to GND	–0.3	6	V
	Digital input voltage to GND	–0.3	DVDD + 0.3	V
	SDO to GND	–0.3	DVDD + 0.3	V
	Current into REFOUT		10	mA
	Operating temperature	–40	125	°C
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

7.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge(1)	Human body model (HBM) ESD stress voltage(2)	±3000	V
		Charged device model (CDM) ESD stress voltage(3)	±1000	

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

7.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
AVDD	Analog supply voltage		10		36	V
DVDD	Digital supply voltage		2.7		5.5	V
	Reference input voltage		4.95		5.05	V
	External reference current			30		µA
	Loop compliance voltage (output = 24 mA)(1)				AVDD – 2	V
VIH	Digital input high voltage		2			V
VIL	Digital Input low voltage	3.6 V < AVDD < 5.5 V			0.8	V
		2.7 V < AVDD < 3.6 V			0.6	
	Specified performance temperature		–40		125	°C

(1) Loop compliance voltage is defined as the voltage at the IOUT pin

7.4 Thermal Information

THERMAL METRIC[1]		DAC7750, DAC8750		UNIT
		RHA (VQFN)	PWP (HTSSOP)	
		40 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.9	32.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	17.2	14.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.5	12.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.5	12	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.4	0.63	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

at AVDD = 10 V to 36 V, GND = 0 V, REFIN = 5 V external, DVDD = 2.7 V to 5.5 V, and all specifications are from –40°C to +125°C (unless otherwise noted); for IOUT, R_L = 300 Ω; typical specifications are at 25°C

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
CURRENT OUTPUT						
Current output	RANGE bits = 111		0		24	mA
	RANGE bits = 110		0		20	
	RANGE bits = 101		4		20	
Resolution	DAC8750		16			Bits
	DAC7750		12			
CURRENT OUTPUT ACCURACY (0 mA TO 20 mA AND 0 mA TO 24 mA)[1]						
Total unadjusted error, TUE	T_A = –40°C to +125°C		–0.2%		0.2%	FSR
	T_A = –40°C to +85°C		–0.16%		0.16%	
	T_A = 25°C		–0.08%	±0.02%	0.08%	
Differential nonlinearity, DNL	Monotonic				±1	LSB
Relative accuracy, INL[3]	T_A = –40°C to +125°C				±0.08%	FSR
	T_A = –40°C to +85°C				±0.024%	
Offset error	T_A = –40°C to +125°C		–0.17%		0.17%	FSR
	T_A = –40°C to +85°C		–0.1%		0.1%	
	T_A = 25°C		–0.07%	±0.01%	0.07%	
Offset error temperature coefficient				±5		ppm FSR/°C
Full-scale error	T_A = –40°C to +125°C		–0.2%		0.2%	FSR
	T_A = –40°C to +85°C		–0.16%		0.16%	
	T_A = 25°C		–0.08%	±0.015%	0.08%	
Full-scale error temperature coefficient	Internal R_{SET}			±5		ppm FSR/°C
	External R_{SET}			±10		
Gain error	Internal R_{SET}	T_A = –40°C to +125°C	–0.2%		0.2%	FSR
		T_A = –40°C to +85°C	–0.15%		0.15%	
		T_A = 25°C	–0.08%	±0.01%	0.08%	
	External R_{SET}	T_A = –40°C to +125°C	–0.17%		0.17%	
		T_A = –40°C to +85°C	–0.12%		0.12%	
		T_A = 25°C	–0.05%	±0.01%	0.05%	
Gain error temperature coefficient	Internal R_{SET}			±3		ppm FSR/°C
	External R_{SET}			±8		
Output current drift vs time	T_A = 125°C, 1000 hrs	Internal R_{SET}		±50		ppm FSR
		External R_{SET}		±25		

7.5 Electrical Characteristics (continued)

at AVDD = 10 V to 36 V, GND = 0 V, REFIN = 5 V external, DVDD = 2.7 V to 5.5 V, and all specifications are from –40°C to +125°C (unless otherwise noted); for IOUT, R_L = 300 Ω; typical specifications are at 25°C

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
CURRENT OUTPUT ACCURACY (4 mA TO 20 mA)(1)						
Total unadjusted error, TUE	Internal R_{SET}	T_A = –40°C to +125°C	–0.25%		0.25%	FSR
		T_A = 25°C	–0.08%	±0.02%	0.08%	
	External R_{SET}	T_A = –40°C to +125°C	–0.29%		0.29%	
		T_A = –40°C to +85°C	–0.25%		0.25%	
		T_A = 25°C	–0.1%	±0.02%	0.1%	
Differential nonlinearity, DNL	Monotonic				±1	LSB
Relative accuracy, INL(3)	T_A = –40°C to +125°C				±0.08%	FSR
	T_A = –40°C to +85°C				±0.024%	
Offset error	Internal R_{SET}	T_A = –40°C to +125°C	–0.22%		0.22%	FSR
		T_A = –40°C to +85°C	–0.2%		0.2%	
	External R_{SET}	T_A = –40°C to +125°C	–0.2%		0.2%	
		T_A = –40°C to +85°C	–0.18%		0.18%	
	Internal and external R_{SET}, T_A = 25°C		–0.07%	±0.01%	0.07%	
Offset error temperature coefficient				±3		ppm FSR/°C
Full-scale error	Internal R_{SET}	T_A = –40°C to +125°C	–0.25%		0.25%	FSR
		T_A = 25°C	–0 .08%	±0.015%	0.08%	
	External R_{SET}	T_A = –40°C to +125°C	–0.29%		0.29%	
		T_A = –40°C to +85°C	–0.25%		0.25%	
		T_A = 25°C	–0 .1%	±0.015%	0.1%	
Full-scale error temperature coefficient	Internal R_{SET}			±5		ppm FSR/°C
	External R_{SET}			±10		
Gain error	Internal R_{SET}	T_A = –40°C to +125°C	–0.2%		0.2%	FSR
		T_A = –40°C to +85°C	–0.15%		0.15%	
		T_A = 25°C	–0.08%	±0.01%	0.08%	
	External R_{SET}	T_A = –40°C to +125°C	–0.16%		0.16%	
		T_A = –40°C to +85°C	–0.12%		0.12%	
		T_A = 25°C	–0.05%	±0.01%	0.05%	
Gain error temperature coefficient	Internal R_{SET}			±3		ppm FSR/°C
	External R_{SET}			±8		
Output current drift vs time	T_A = 125°C, 1000 hrs	Internal R_{SET}		±50		ppm FSR
		External R_{SET}		±75		
CURRENT OUTPUT STAGE(2)						
Loop compliance voltage(4)	Output = 24 mA				AVDD – 2	V
Inductive load(5)				50		mH
DC PSRR					1	µA/V
Output impedance	Code = 0x8000			50		MΩ
R3 RESISTOR						
R3 resistor value			36	40	44	Ω
R3 resistor temperature coefficient				40		ppm/°C
EXTERNAL REFERENCE INPUT						
Reference input voltage			4.95	5	5.05	V
External reference current	REFIN = 5.0 V			30		µA
Reference input capacitance				10		pF

7.5 Electrical Characteristics (continued)

at AVDD = 10 V to 36 V, GND = 0 V, REFIN = 5 V external, DVDD = 2.7 V to 5.5 V, and all specifications are from –40°C to +125°C (unless otherwise noted); for IOUT, R_L = 300 Ω; typical specifications are at 25°C

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
INTERNAL REFERENCE OUTPUT						
Reference output	T_A = 25°C		4.995		5.005	V
Reference temperature coefficient(2)	T_A = –40°C to +85°C				±10	ppm/°C
Output noise (0.1 Hz to 10 Hz)	T_A = 25°C			14		μV_{PP}
Noise spectral density	T_A = 25°C, 10 kHz			185		nV/√Hz
Capacitive load				600		nF
Load current				±5		mA
Short-circuit current	REFOUT shorted to GND			25		mA
Load regulation	AVDD = 24 V, T_A = 25°C, sourcing			55		µV/mA
	AVDD = 24 V, T_A = 25°C, sinking			120		
Line regulation				±1.2		µV/V
DVDD INTERNAL REGULATOR						
Output voltage	AVDD = 24 V			4.6		V
Output load current(2)					10	mA
Load regulation				3.5		mV/mA
Line regulation				1		mV/V
Short-circuit current	AVDD = 24 V, to GND			35		mA
Capacitive load stability(2)					2.5	µF
DIGITAL INPUTS						
High-level input voltage, V_{IH}			2			V
Low-level input voltage, V_{IL}	3.6 V < AVDD < 5.5 V				0.8	V
	2.7 V < AVDD < 3.6 V				0.6	
Hysteresis voltage				0.4		V
Input current	DVDD-EN, V_{IN} ≤ 5 V		–2.7			µA
	All pins other than DVDD-EN				±1	
Pin capacitance	Per pin			10		pF
DIGITAL OUTPUTS						
SDO	Low-level output voltage, V_{OL}, sinking 200 µA				0.4	V
	HIgh-level output voltage, V_{OH}, sourcing 200 µA		DVDD – 0.5			
	High-impedance leakage				±1	µA
$\overline{ALARM}$	Low-level output voltage, V_{OL}	10-kΩ pullup resistor to DVDD			0.4	V
		2.5 mA			0.6	
	High-impedance leakage				±1	µA
High-impedance output capacitance				10		pF
POWER SUPPLY						
AVDD			10		36	V
DVDD	Internal regulator disabled		2.7		5.5	V
AIDD	Outputs disabled, external DVDD				3	mA
	Outputs disabled, internal DVDD				4	
	Code = 0x0000, IOUT enabled				3	
DIDD	V_{IH} = DVDD, V_{IL} = GND, interface idle				1	mA
Power dissipation	AVDD = 36 V, IOUT = 0 mA, DVDD = 5 V			95	115	mW
TEMPERATURE						
Thermal alarm				142		°C
Thermal alarm hysteresis				18		°C

(1) DAC8750 and DAC7750 current output range is set by writing to RANGE bits in control register at address 0x55.
(2) Specified by design and characterization; not production tested.

(3) For 0-mA to 20-mA and 0-mA to 24-mA ranges, INL is calculated beginning from code 0x0100 for DAC8750 and from code 0x0010 for DAC7750.
(4) Loop compliance voltage is defined as the voltage at the IOUT pin.
(5) For stability, use slew rate limit feature or add a capacitor between IOUT and GND

7.6 Electrical Characteristics: AC

At AVDD = 10 V to 36 V, GND = 0 V, REFIN= 5 V external and DVDD = 2.7 V to 5.5 V. For IOUT, R_L = 300 Ω. All specifications –40°C to 125°C (unless otherwise noted). Typical specifications are at 25°C.

PARAMETER(1)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE					
Output current settling time	16-mA step, to 0.1% FSR, no L (inductance)		10		µs
	16-mA step, to 0.1% FSR, L < 1 mH		25		µs
AC PSRR	200-mV, 50-Hz or 60-Hz sine wave superimposed on power-supply voltage		–75		dB

(1) Specified by characterization, not production tested.

7.7 Timing Requirements: Write Mode

at T_A = –40°C to 125°C and DVDD = 2.7 V to 5.5 V (unless otherwise noted)(1)

		MIN	MAX	UNIT
t_1	SCLK cycle time	33		ns
t_2	SCLK low time	13		ns
t_3	SCLK high time	13		ns
t_4	LATCH delay time	13		ns
t_5	LATCH high time(2)	40		ns
t_6	Data setup time	5		ns
t_7	Data hold time	7		ns
t_8	LATCH low time	40		ns
t_9	CLR pulse duration	20		ns
t_{10}	CLR activation time		5	µs

(1) Specified by design, not production tested.
(2) Based on digital interface circuitry only. When writing to DAC control and configuration registers, consider the analog output specifications in *セクション 7.6*.

7.8 Timing Requirements: Readback Mode

at T_A = –40°C to 125°C and DVDD = 2.7 V to 5.5 V (unless otherwise noted)(1)

		MIN	MAX	UNIT
t_{11}	SCLK cycle time	60		ns
t_{12}	SCLK low time	25		ns
t_{13}	SCLK high time	25		ns
t_{14}	LATCH delay time	13		ns
t_{15}	LATCH high time	40		ns
t_{16}	Data setup time	5		ns
t_{17}	Data hold time	7		ns
t_{18}	LATCH low time	40		ns
t_{19}	Serial output delay time ($C_{L, SDO}$ = 15 pF)		35	ns
t_{20}	LATCH rising edge to SDO 3-state ($C_{L, SDO}$ = 15 pF)		35	ns

(1) Specified by design, not production tested.

7.9 Timing Diagrams

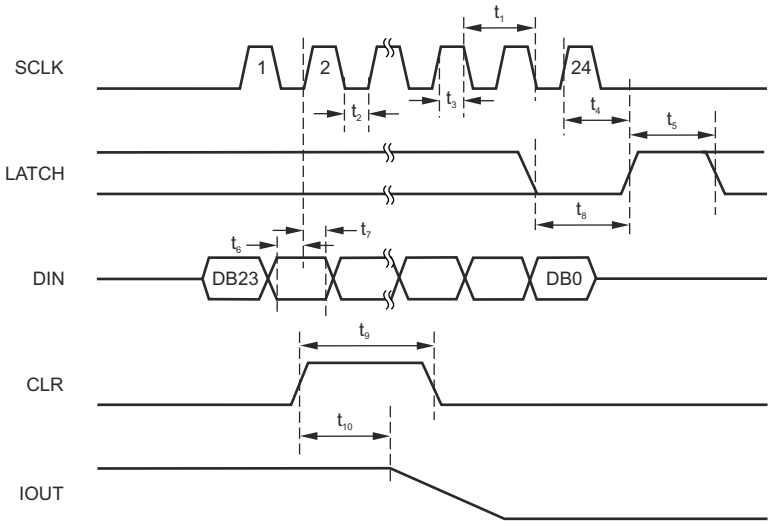


図 7-1. Write Mode Timing

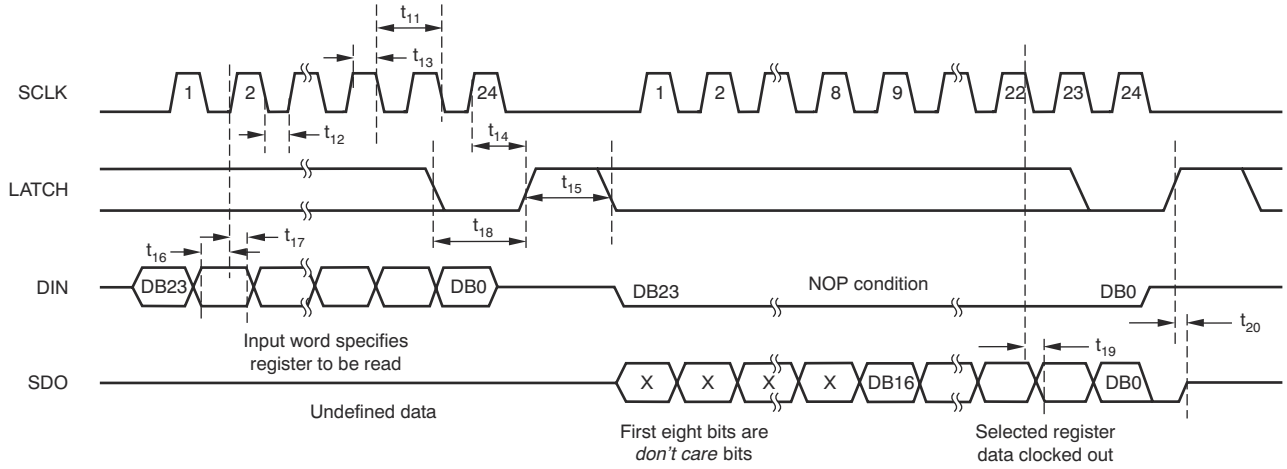
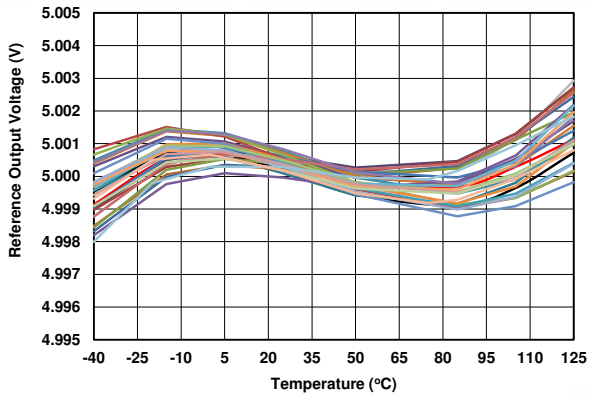


図 7-2. Readback Mode Timing

7.10 Typical Characteristics

at T_A = 25°C (unless otherwise noted)



30 units shown AVDD = 24 V

図 7-3. REFOUT vs Temperature

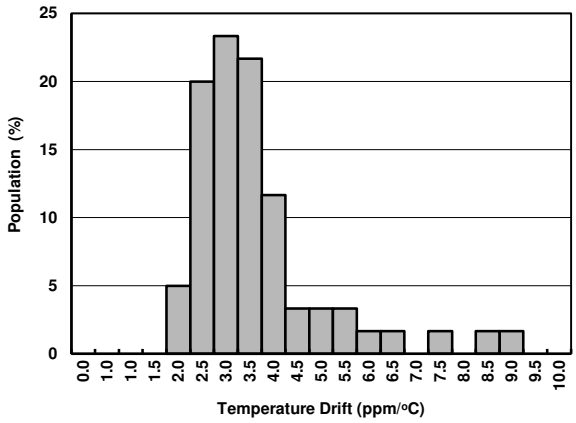
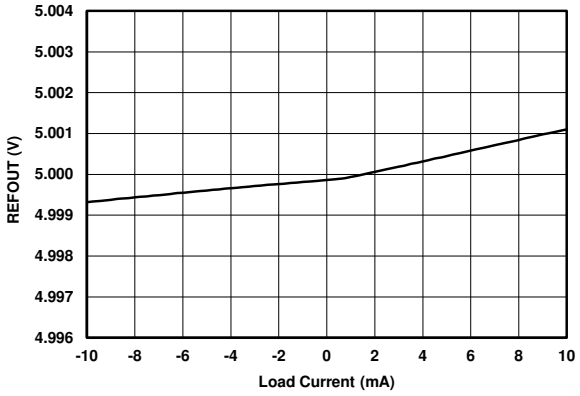
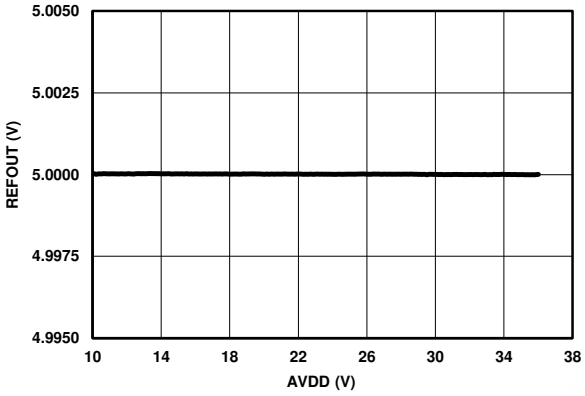


図 7-4. Internal Reference Temperature Drift Histogram



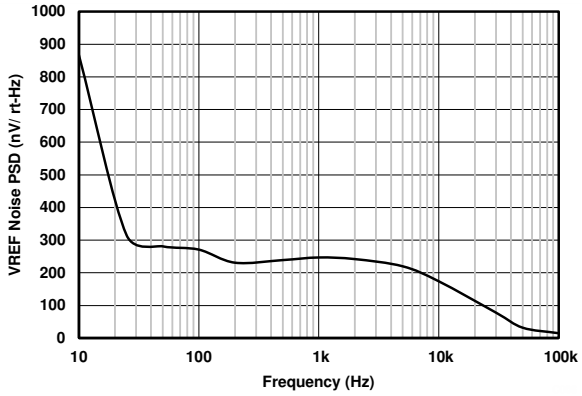
AVDD = 24 V

図 7-5. REFOUT vs Load Current



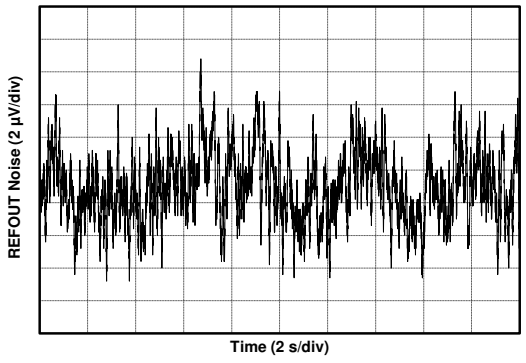
T_A = 25°C

図 7-6. REFOUT vs AVDD



AVDD = 24 V

図 7-7. REFOUT Noise PSD vs Frequency

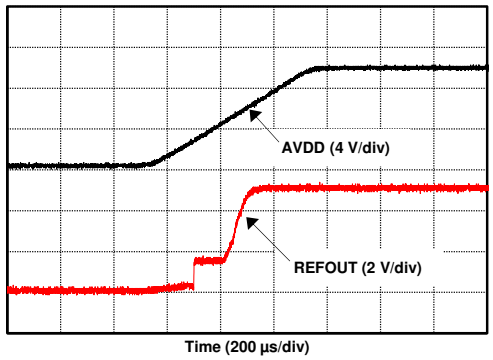


AVDD = 24 V

図 7-8. Internal Reference, Peak-to-Peak Noise (0.1 Hz to 10 Hz)

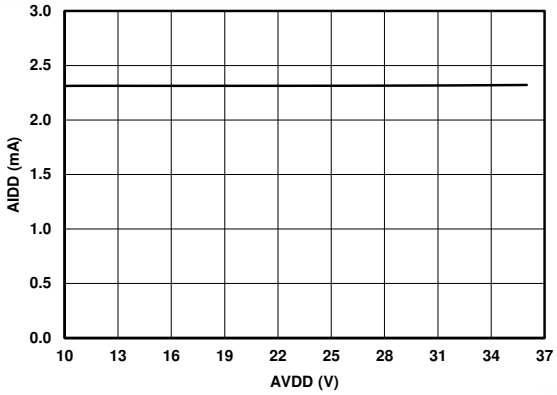
7.10 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)



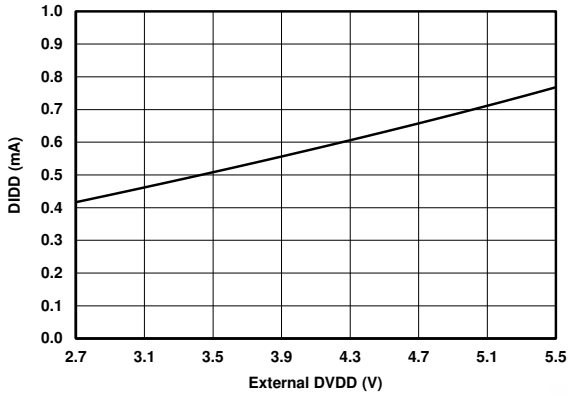
AVDD = 10 V

図 7-9. REFOUT Transient vs Time



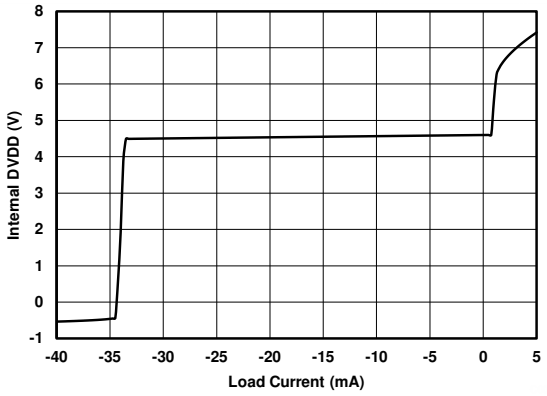
External DVDD IOUT = 0 mA

図 7-10. AIDD vs AVDD



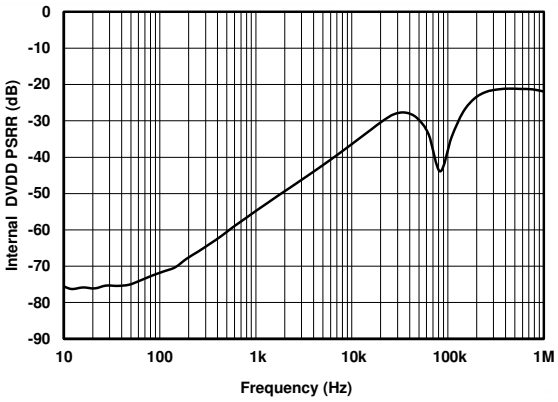
T_A = 25°C External DVDD

図 7-11. DIDD vs External DVDD



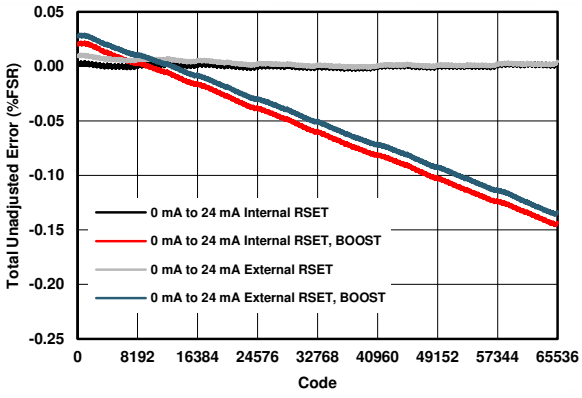
T_A = 25°C Internal DVDD

図 7-12. Internal DVDD vs Load Current



AVDD = 18 V C_{LOAD} = 100 nF

図 7-13. Internal DVDD PSRR vs Frequency

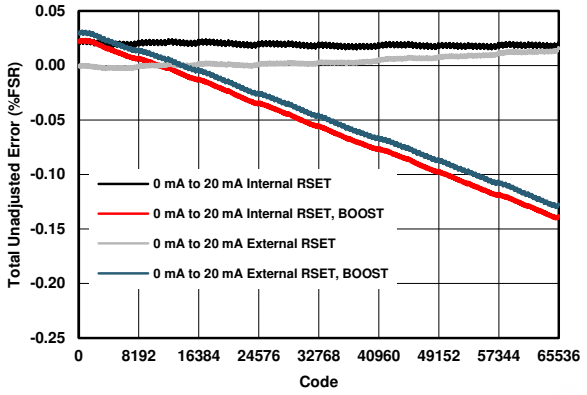


AVDD = 24 V R_{LOAD} = 300 Ω

図 7-14. IOUT TUE vs Code (0 mA to 24 mA)

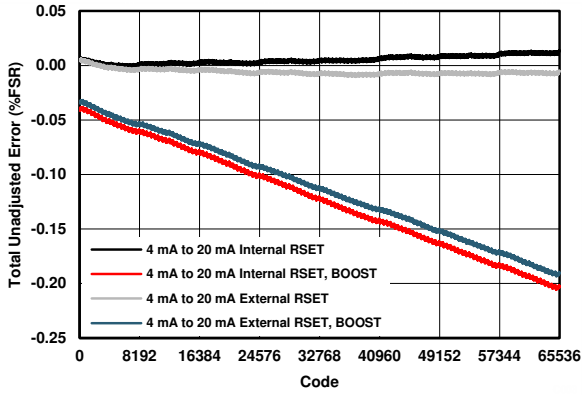
7.10 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)



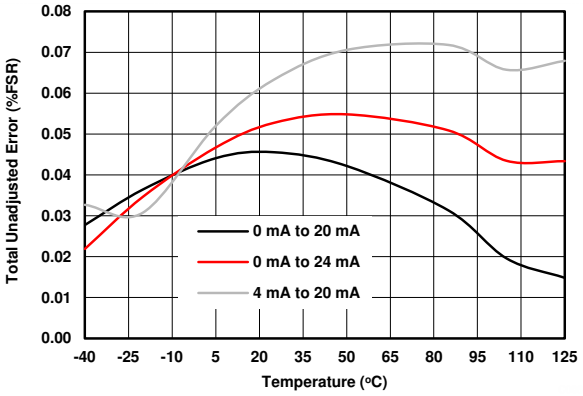
AVDD = 24 V R_{LOAD} = 300 Ω

図 7-15. IOUT TUE vs Code (0 mA to 20 mA)



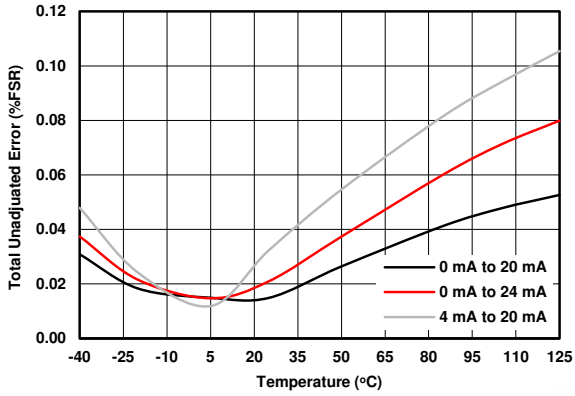
AVDD = 24 V R_{LOAD} = 300 Ω

図 7-16. IOUT TUE vs Code (4 mA to 20 mA)



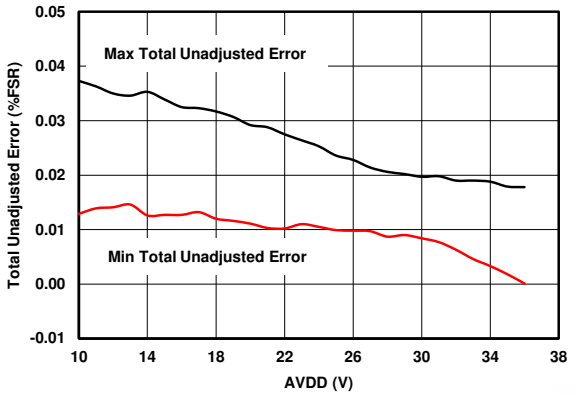
AVDD = 10 V R_{LOAD} = 300 Ω

図 7-17. IOUT TUE vs Temperature (Internal R_{SET})



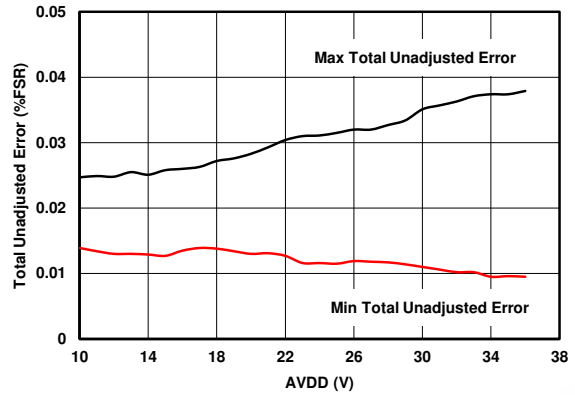
AVDD = 10 V R_{LOAD} = 300 Ω

図 7-18. IOUT TUE vs Temperature (External R_{SET})



R_{LOAD} = 300 Ω 0-mA to 24-mA range

図 7-19. IOUT TUE vs Supply (Internal R_{SET})

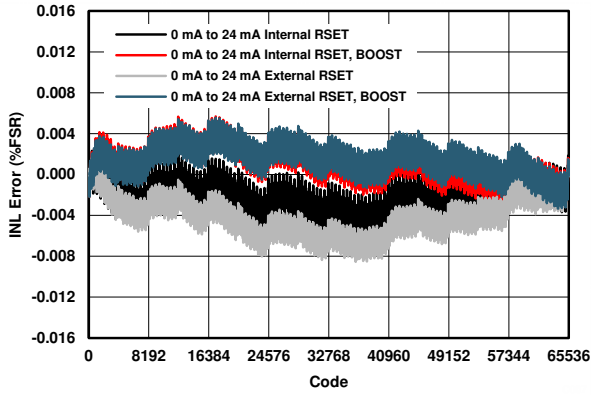


R_{LOAD} = 300 Ω 0-mA to 24-mA range

図 7-20. IOUT TUE vs Supply (External R_{SET})

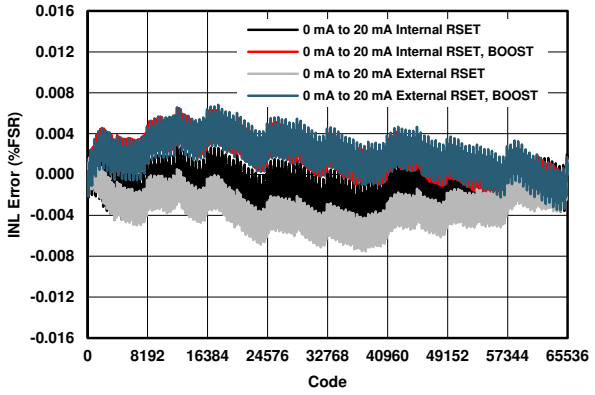
7.10 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)



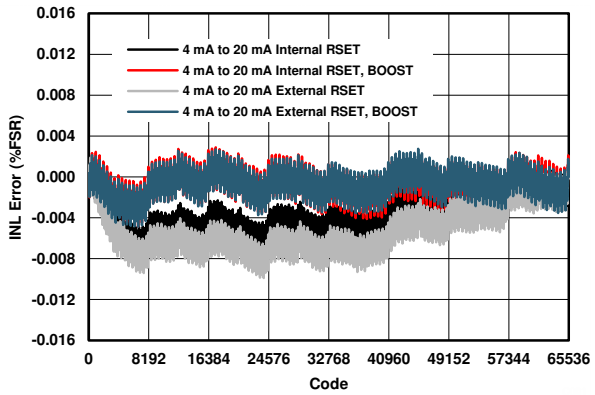
AVDD = 24 V R_{LOAD} = 300 Ω

図 7-21. IOUT INL vs Code (0 mA to 24 mA)



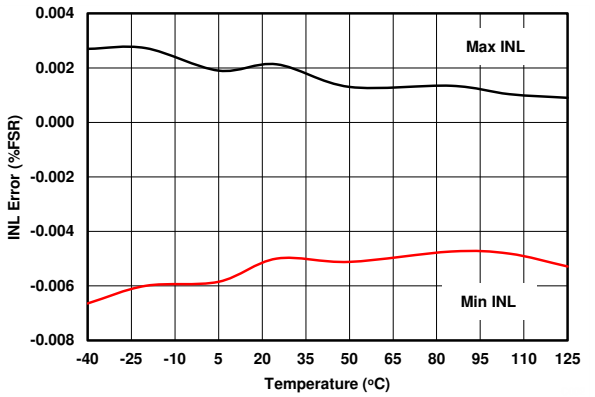
AVDD = 24 V R_{LOAD} = 300 Ω

図 7-22. IOUT INL vs Code (0 mA to 20 mA)



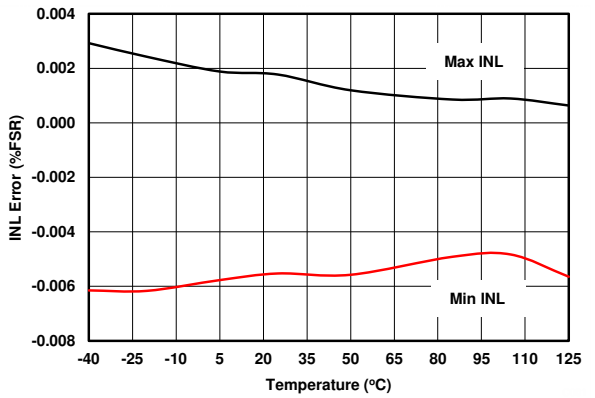
AVDD = 24 V R_{LOAD} = 300 Ω

図 7-23. IOUT INL vs Code (4 mA to 20 mA)



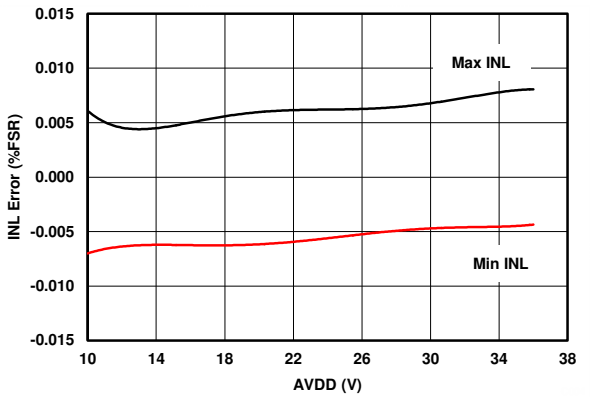
AVDD = 10 V R_{LOAD} = 300 Ω All IOUT ranges

図 7-24. IOUT INL vs Temperature (Internal R_{SET})



AVDD = 10 V R_{LOAD} = 300 Ω All IOUT ranges

図 7-25. IOUT INL vs Temperature (External R_{SET})

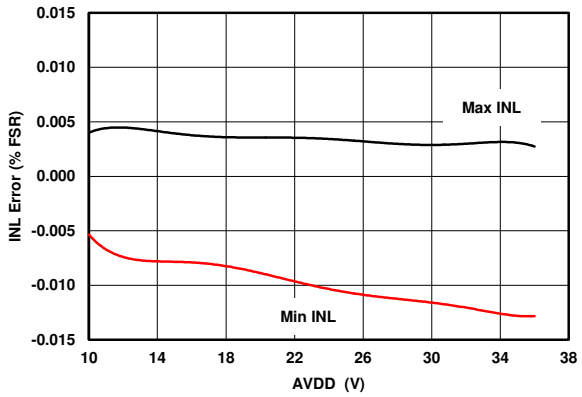


R_{LOAD} = 300 Ω 0-mA to 24-mA range

図 7-26. IOUT INL vs Supply (Internal R_{SET})

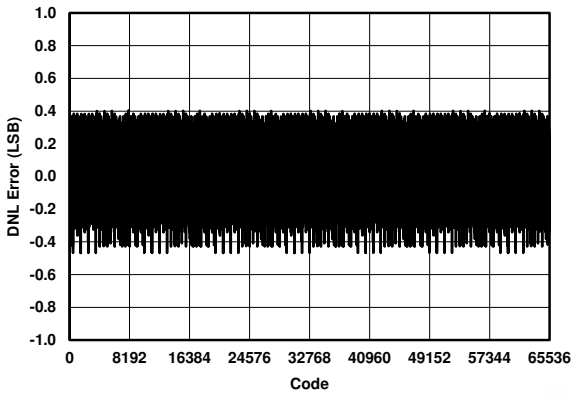
7.10 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)



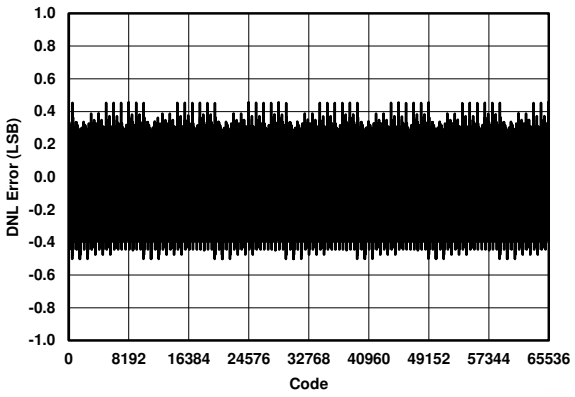
R_{LOAD} = 300 Ω 0-mA to 24-mA range

図 7-27. IOUT INL vs Supply (External R_{SET})



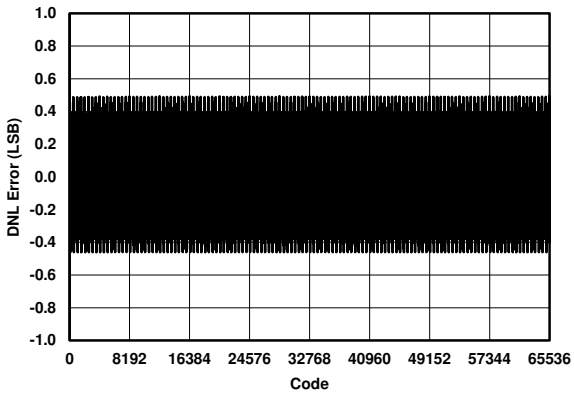
AVDD = 24 V 0-mA to 24-mA range
R_{LOAD} = 300 Ω

図 7-28. IOUT DNL vs Code (0 mA to 24 mA)



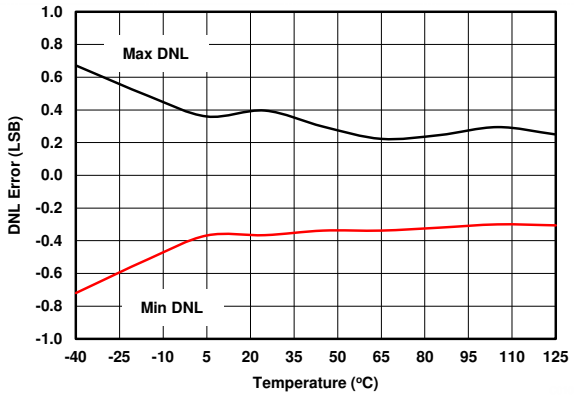
AVDD = 24 V 0-mA to 24-mA range
R_{LOAD} = 300 Ω

図 7-29. IOUT DNL vs Code (0 mA to 20 mA)



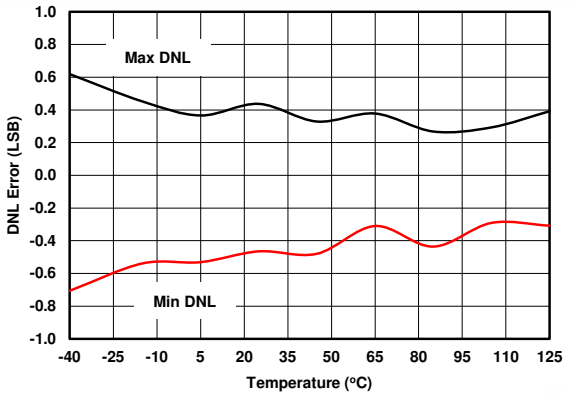
AVDD = 24 V 4-mA to 24-mA range
R_{LOAD} = 300 Ω

図 7-30. IOUT DNL vs Code (4 mA to 20 mA)



AVDD = 10 V R_{LOAD} = 300 Ω All IOUT ranges

図 7-31. IOUT DNL vs Temperature (Internal R_{SET})

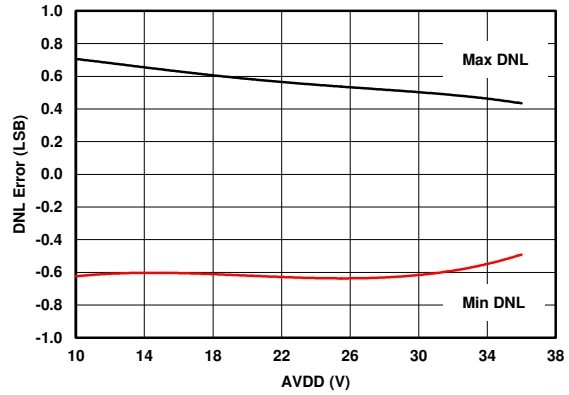


AVDD = 10 V R_{LOAD} = 300 Ω All IOUT ranges

図 7-32. IOUT DNL vs Temperature (External R_{SET})

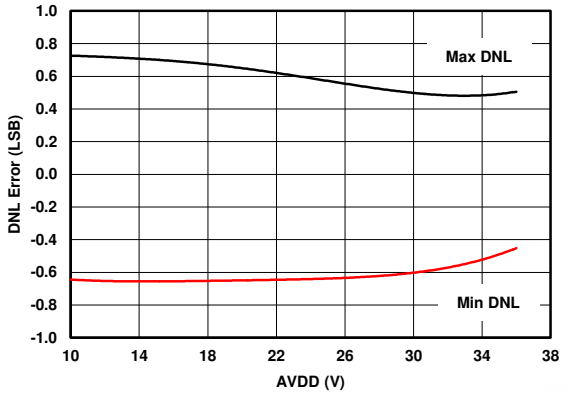
7.10 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)



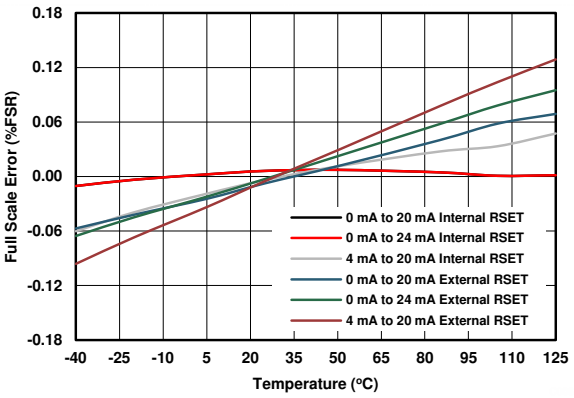
R_{LOAD} = 300 Ω 0-mA to 24-mA range

図 7-33. IOUT DNL vs Supply (Internal R_{SET})



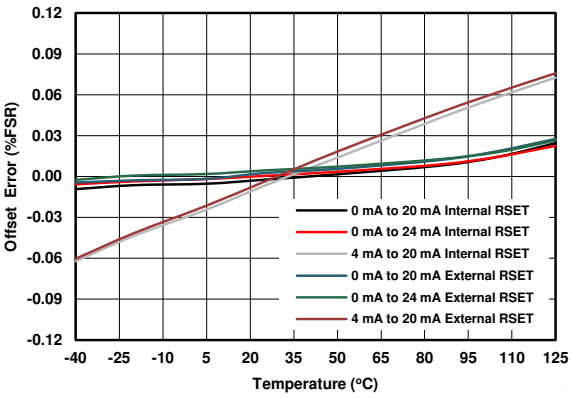
R_{LOAD} = 300 Ω 0-mA to 24-mA range

図 7-34. IOUT DNL vs Supply (External R_{SET})



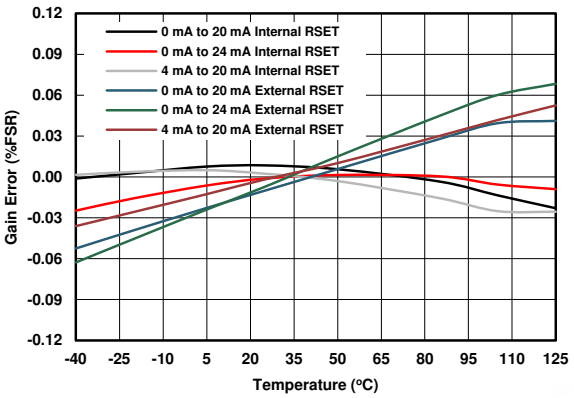
AVDD = 10 V R_{LOAD} = 300 Ω

図 7-35. IOUT Full-Scale Error vs Temperature



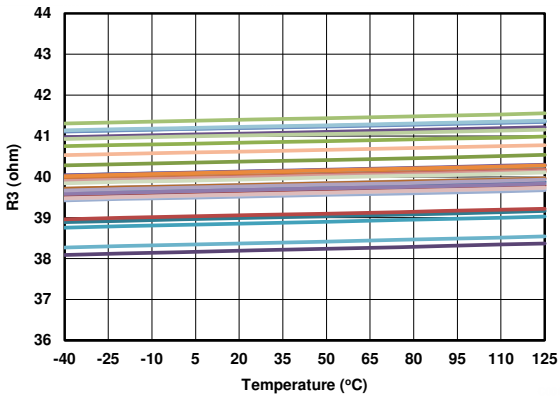
AVDD = 10 V R_{LOAD} = 300 Ω

図 7-36. IOUT Offset Error vs Temperature



AVDD = 10 V R_{LOAD} = 300 Ω

図 7-37. IOUT Gain Error vs Temperature



33 units shown

図 7-38. R3 Resistance vs Temperature

7.10 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)

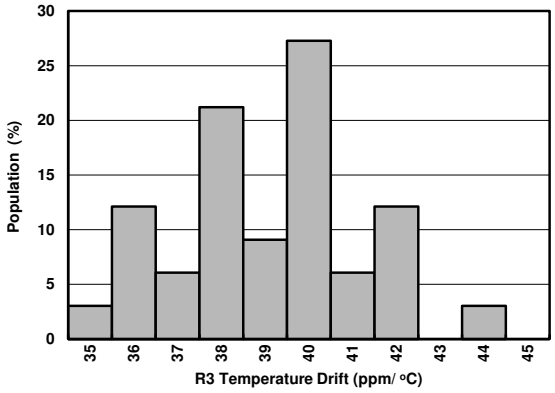
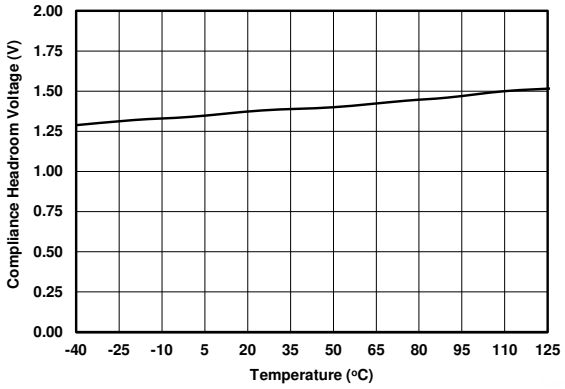


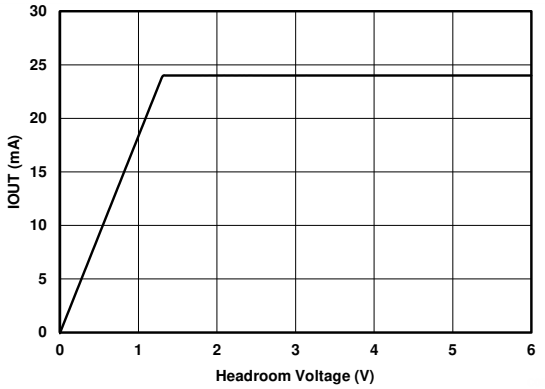
図 7-39. R3 Resistance Temperature Drift Histogram



AVDD = 36 V IOUT = 24 mA R_{LOAD} = 300 Ω

NOTE: Compliance voltage headroom is defined as the drop from the AVDD pin to the IOUT pin.

図 7-40. Compliance Headroom Voltage vs Temperature

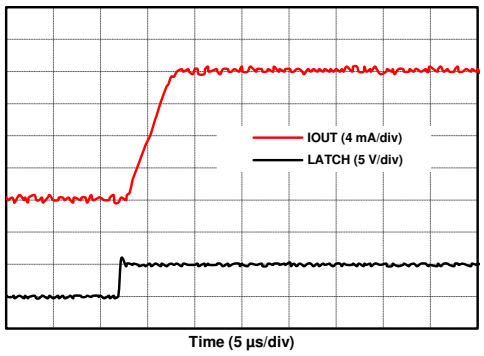


AVDD = 36 V R_{LOAD} = 300 Ω

DAC configured to deliver 24 mA

NOTE: Compliance voltage headroom is defined as the drop from the AVDD pin to the IOUT pin.

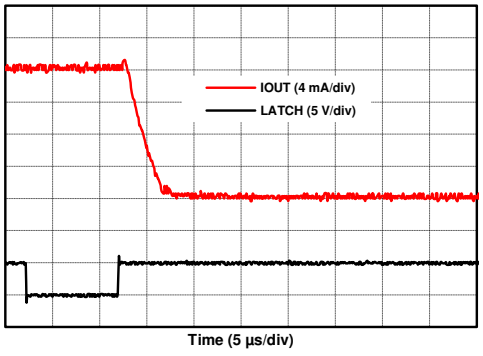
図 7-41. IOUT vs Compliance Headroom Voltage



AVDD = 24 V 4-mA to 20-mA range

R_{LOAD} = 300 Ω From code: 0x0000 To code: 0xFFFF

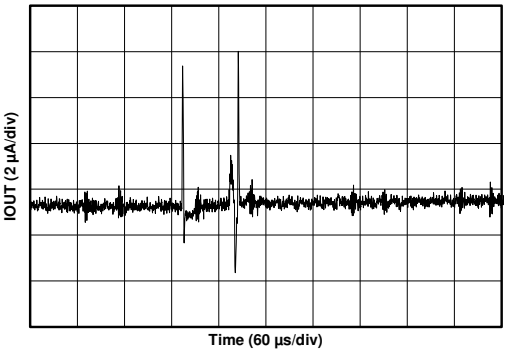
図 7-42. 4-mA to 20-mA Rising



AVDD = 24 V 4-mA to 20-mA range

R_{LOAD} = 300 Ω From code: 0xFFFF To code: 0x0000

図 7-43. 4-mA to 20-mA Falling

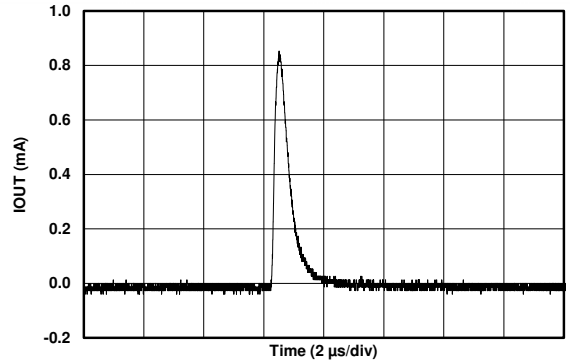


AVDD = 24 V R_{LOAD} = 300 Ω

図 7-44. IOUT Power-On Glitch

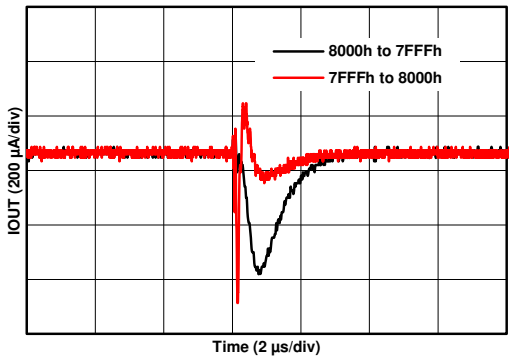
7.10 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)



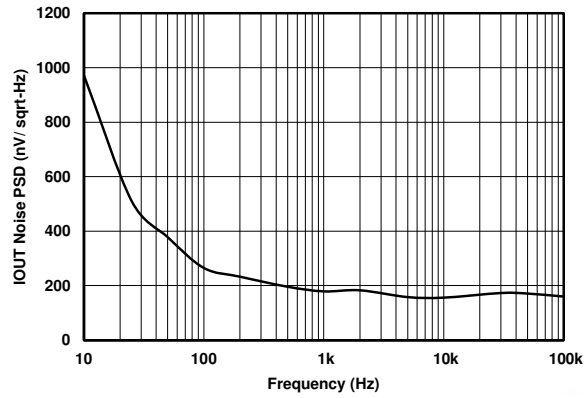
AVDD = 24 V R_{LOAD} = 300 Ω

図 7-45. IOUT Output Enable Glitch



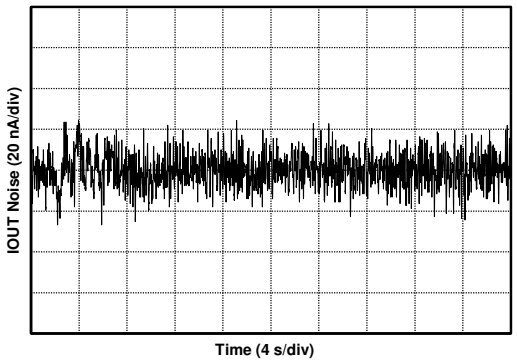
AVDD = 24 V R_{LOAD} = 250 Ω

図 7-46. IOUT Digital-to-Analog Glitch



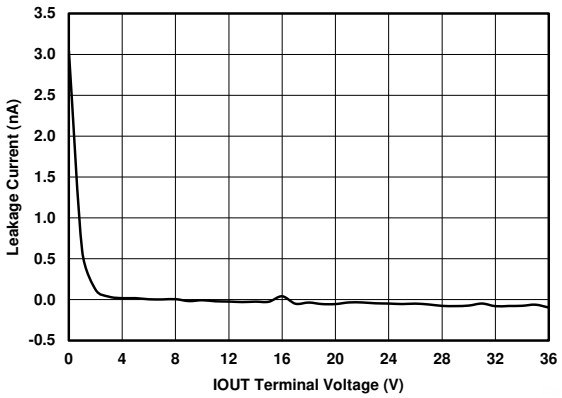
AVDD = 24 V R_{LOAD} = 300 Ω All IOUT ranges

図 7-47. IOUT Noise PSD vs Frequency



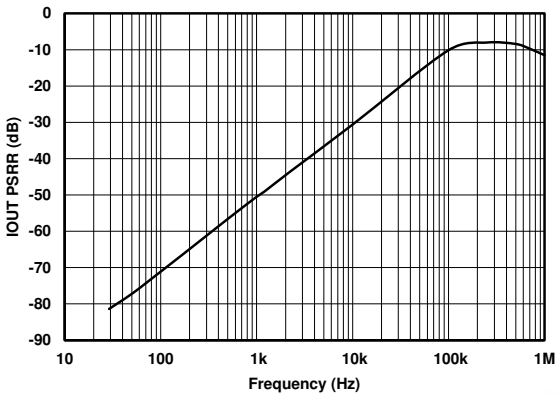
AVDD = 24 V 0-mA to 20-mA range
DAC = midscale

図 7-48. IOUT Peak-to-Peak Noise vs Time (0.1 Hz to 10 Hz)



AVDD = 36 V Output disabled

図 7-49. IOUT Hi-Z Leakage Current vs Voltage



AVDD = 24 V R_{LOAD} = 250 Ω All IOUT ranges

図 7-50. IOUT PSRR vs Frequency

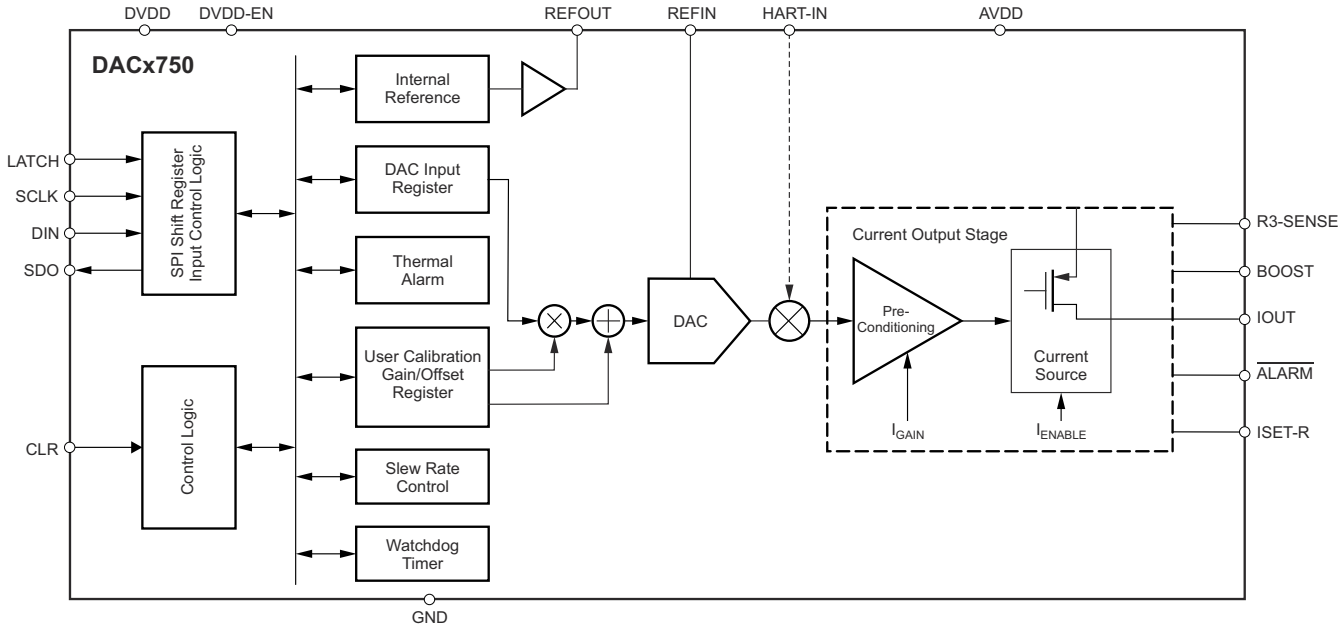
8 Detailed Description

8.1 Overview

The DAC8750 and DAC7750 are low-cost, precision, fully-integrated, 16-bit and 12-bit digital-to-analog converters (DACs) designed to meet the requirements of industrial process control applications. These devices can be programmed as a current output with a range of 4 mA to 20 mA, 0 mA to 20 mA, or 0 mA to 24 mA. The DAC8750 and DAC7750 include reliability features such as CRC error checking on the serial peripheral interface (SPI) frame, a watchdog timer, an open circuit, compliance voltage, and thermal alarm. In addition the output current can be monitored by accessing an internal precision resistor.

These devices include a power-on-reset function to ensure powering up in a known state (both IOUT is disabled and in a high-impedance state). The CLR pin sets the current output to the low-end of the range if the output is enabled. Zero code error and gain error calibration registers can be programmed to digitally calibrate the device in the end system. The output slew rate is also programmable. These devices can AC couple an external HART signal on the current output and can operate with either a 10-V to 36-V supply.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 DAC Architecture

The resistor-string section is simply a string of resistors, each with the same value, from REFIN to GND, as 図 8-1 shows. This type of architecture makes sure the DAC is monotonic. The 16-bit (DAC8750) or 12-bit (DAC7750) binary digital code loaded to the DAC register determines at which node on the string the voltage is tapped off before it is fed into the voltage-to-current conversion stage. The current-output stage converts the voltage output from the string to current. When the output is disabled, it is in a high-impedance (Hi-Z) state. After power-on, the output is disabled.

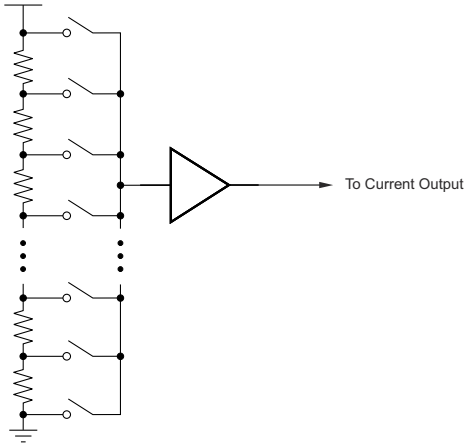


図 8-1. DAC Structure: Resistor String

8.3.2 Current Output Stage

The current output stage consists of a preconditioner and a current source, as shown in 図 8-2. This stage provides a current output according to the DAC code. The output range can be programmed as 0 mA to 20 mA, 0 mA to 24 mA, or 4 mA to 20 mA. Use an external transistor to reduce the power dissipation of the device. The maximum compliance voltage on IOUT equals (AVDD – 2 V). In single power-supply mode, the maximum AVDD is 36 V, and the maximum compliance voltage is 34 V. After power on, the IOUT pin is in a Hi-Z state.

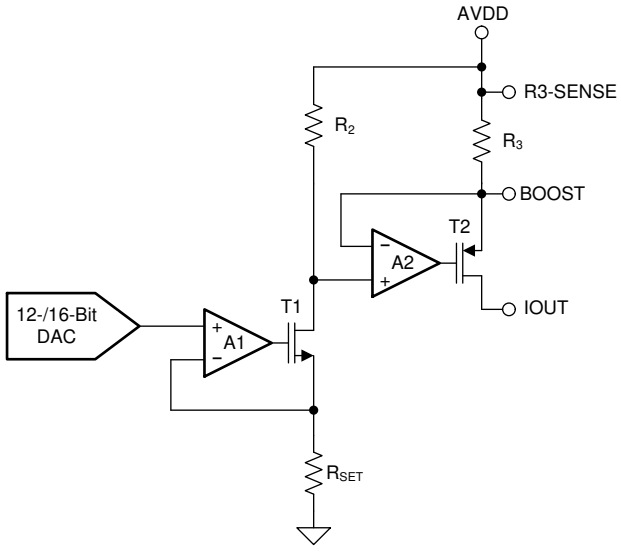


図 8-2. Current Output

For a 5-V reference, the output can be expressed as shown in 式 1 through 式 3.

For a 0-mA to 20-mA output range, use 式 1.

$$IOUT = 20mA \bullet \frac{CODE}{2^N} \quad (1)$$

For a 0-mA to 24-mA output range, use 式 2.

$$IOUT = 24mA \bullet \frac{CODE}{2^N} \quad (2)$$

For a 4-mA to 20-mA output range, use 式 3.

$$IOUT = 16mA \bullet \frac{CODE}{2^N} + 4mA \quad (3)$$

where

- *CODE* is the decimal equivalent of the code loaded to the DAC
- *N* is the bits of resolution; 16 for DAC8750, and 12 for DAC7750

The current-output range is normally set according to the value of the RANGE bits in the *Control Register* (see *セクション 8.4.1* for more details).

8.3.3 Internal Reference

The DACx750 includes an integrated 5-V reference with a buffered output (REFOUT) capable of driving up to 5 mA (source or sink) with an initial accuracy of ±5 mV maximum and a temperature drift coefficient of 10 ppm/°C maximum.

8.3.4 Digital Power Supply

An internally generated 4.6-V supply capable of driving up to 10 mA can be output on DVDD by leaving the DVDD-EN pin unconnected. This configuration simplifies the system power-supply design when an isolation barrier is required to generate the digital supply. The internally generated supply can be used to drive isolation components used for the digital data lines and other miscellaneous components, such as references and temperature sensors; see 図 9-3 for an example application.

If an external supply is preferred, the DVDD pin (which can be driven up to 5.5 V in this case) can become an input by tying DVDD-EN to GND. See *セクション 7.5* for detailed specifications.

8.3.5 DAC Clear

The DAC has an asynchronous clear function through the CLR pin that is active-high and allows the current output to be cleared to zero-scale code. When the CLR signal returns to low, the output remains at the cleared value. The preclear value can be restored by pulsing the LATCH signal without clocking any data. A new value cannot be programmed until the CLR pin returns to low. To avoid glitches on the output, disable the output by writing a 0 to the OUTEN bit of the *Control Register* before changing the current range.

8.3.6 Power-On Reset

The DACx750 incorporates two internal POR circuits for the DVDD and AVDD supplies. The DVDD and AVDD POR signals are ANDed together so that both supplies must be at their minimal specified values for the device to *not* be in a reset condition. These POR circuits initialize internal logic and registers, as well as set the analog outputs to a known state while the device supplies are ramping. All registers are reset to their default values. Typically the POR function can be ignored, as long as the device supplies power-up and maintains the specified minimum voltage levels. However, in the case of a supply drop or brownout, the DACx750 can have an internal POR reset event or lose digital memory integrity. 図 8-3 represents the threshold levels for the internal POR for both the DVDD and AVDD supplies.

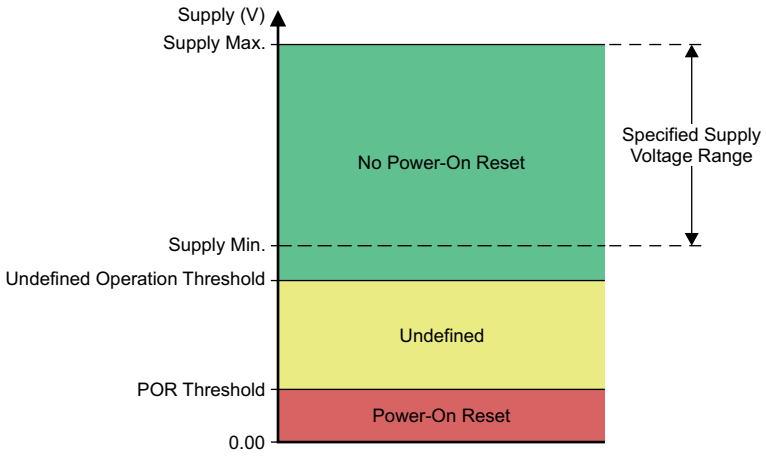


図 8-3. Relevant Voltage Levels for POR Circuit

For the DVDD supply, no internal POR occurs for nominal supply operation from 2.7 V (supply min) to 5.5 V (supply max). For the DVDD supply region between 2.4 V (undefined operation threshold) and 0.8 V (POR threshold), the internal POR circuit may or may not provide a reset over all temperature conditions. For the DVDD supply below 0.8 V (POR threshold), the internal POR resets if the supply voltage remains less than 0.8 V for approximately 1 ms.

For the AVDD supply, no internal POR occurs for nominal supply operation from 10 V (supply min) to 36 V (supply max). For AVDD supply voltages between 8 V (undefined operation threshold) and 1 V (POR threshold), the internal POR circuit may or may not provide a reset over all temperature conditions. For the AVDD supply below 1 V (POR threshold), the internal POR resets if the supply voltage remains less than 1 V for approximately 1 ms. In case the DVDD or AVDD supply drops to a level where the internal POR signal is indeterminate, either power cycle the device, or toggle the LATCH pin and then perform a software reset. Both options initialize the internal circuitry to a known state and provide proper operation.

8.3.7 Alarm Detection

These devices also provide an alarm detection feature. When one or more of following events occur, the $\overline{\text{ALARM}}$ pin goes low:

- The current output load is in open circuit,
- The voltage at IOUT reaches a level where accuracy of the output current is compromised. This condition is detected by monitoring internal voltage levels of the IOUT circuitry and is typically below the specified compliance voltage headroom (defined as the voltage drop between the AVDD and IOUT pins) minimum of 2 V,
- The die temperature exceeds 142°C,
- The SPI watchdog timer exceeds the timeout period (if enabled), or
- The SPI frame error CRC check encounters an error (if enabled).

When the $\overline{\text{ALARM}}$ pins of multiple DACx750 devices are connected together to form a wired-AND function, the host processor must read the status register of each device to know all the fault conditions that are present. Note that the thermal alarm has hysteresis of approximately 18°C. After being set, the alarm only resets when the die temperature drops below 124°C.

8.3.8 Watchdog Timer

This feature is useful to make sure that communication between the host processor and the DACx750 has not been lost. The feature can be enabled by setting the WDEN bit of the *Configuration Register* to 1. The watchdog timeout period can be set using the WDPD bits of the configuration register, as shown in 表 8-1. The timer period is based off an internal oscillator with a typical value of 8 MHz.

表 8-1. Watchdog Timeout Period

WDPD BITS	WATCHDOG TIMEOUT PERIOD (Typical)
00	10 ms
01	51 ms
10	102 ms
11	204 ms

If the watchdog timer is enabled, these devices must have an SPI frame with 0x95 as the write address byte written to the device within the programmed timeout period. Otherwise, the $\overline{\text{ALARM}}$ pin asserts low and the WD-FLT bit of the status register is set to 1. The $\overline{\text{ALARM}}$ pin can be asserted low for any of the different conditions explained in *セクション 8.3.7*. To reset the WD-FLT bit to 0, use a software reset, disable the watchdog timer, or power down the device.

8.3.9 Frame Error Checking

In noisy environments, error checking can be used to check the integrity of SPI data communication between the DACx750 and the host processor. To enable this feature, set the CRCEN bit of the *Configuration Register* to 1. The frame error checking scheme is based on the CRC-8-ATM (HEC) polynomial $x^8 + x^2 + x + 1$ (that is, *100000111*). When error checking is enabled, the SPI frame width is 32 bits, as shown in 表 8-2. Start with the default 24-bit frame, enable frame error checking, and then switch to the 32-bit frame. The normal 24-bit SPI data are appended with an 8-bit CRC polynomial by the host processor before feeding to the device. For a register readback, the CRC polynomial is output on the SDO pins by the device as part of the 32-bit frame.

表 8-2. SPI Frame with Frame Error Checking Enabled

BIT 31:BIT 8	BIT 7:BIT 0
Normal SPI frame data	8-bit CRC polynomial

When in CRC mode, the DACx750 calculates CRC words every 32 clocks, unconditional of when the LATCH pin toggles. The DACx750 decodes the 32-bit input frame data to compute the CRC remainder. If no error exists in the frame, the CRC remainder is zero. When the remainder is non-zero (that is, the input frame has single- or multiple-bit errors), the $\overline{\text{ALARM}}$ pin asserts low and the CRC-FLT bit of the status register is set to 1. The $\overline{\text{ALARM}}$ pin can be asserted low for any of the different conditions explained in *セクション 8.3.7*. To reset the CRC-FLT bit to 0, either issue software reset command of 0x96, disable the frame error checking, or power down the device. In the case of a CRC error, the specific SPI frame is blocked from writing to the device.

If CRC mode is enabled on the first frame issued to the device after power up, issue a no operation, or NOOP, command to the device in order to reset the SPI clock and SPI frame alignment in the event that any transients on the SCLK line are interpreted as SCLK periods. A NOOP command can be issued to the device by simply toggling the LATCH pin without any SCLK periods.

8.3.10 User Calibration

The device implements a user-calibration function (enabled by the CALEN bit in the *Configuration Register*) to trim system gain and zero errors. The DAC output is calibrated according to the value of the gain calibration and zero calibration registers. The range of gain adjustment is typically ±50% of full-scale with 1 LSB per step. The gain register must be programmed to 0x8000 to achieve the default gain of 1 because the power-on value of the register is 0x0000, equivalent to a gain of 0.5. The zero code adjustment is typically ±32,768 LSBs with 1 LSB per step. The input data format of the gain register is unsigned straight binary, and the input data format of the zero register is 2's complement. The gain and offset calibration is described by 式 4.

$$CODE\_OUT = CODE \bullet \frac{User\_GAIN + 2^{15}}{2^{16}} + User\_ZERO \tag{4}$$

where

- *CODE* is the decimal equivalent of the code loaded to the DAC data register at address 0x01
- *N* is the bits of resolution (16 for DAC8750 and 12 for DAC7750)
- *User_ZERO* is the signed 16-bit code in the zero register
- *User_GAIN* is the unsigned 16-bit code in the gain register
- *CODE_OUT* is the decimal equivalent of the code loaded to the DAC (limited between 0x0000 to 0xFFFF for DAC8750 and 0x000 to 0xFFF for DAC7750)

This is a purely digital implementation and the output is still limited by the programmed value at both ends of the current output range (set by the RANGE bits, as described in *セクション 8.4.1*). In addition, the correction only makes sense for endpoints inside of the true device end points. To correct more than just the actual device error (for example, a system offset), the valid range for the adjustment changes accordingly and must be taken into account.

New calibration codes are only applied to subsequent writes to the DAC data register. Updating the calibration codes does not automatically update the DAC output. Additionally, before applying new DAC data, configure the calibration codes along with the slew rate control.

8.3.11 Programmable Slew Rate

The slew rate control feature controls the rate at which the output current changes. With the slew rate control feature disabled, the output changes smoothly at a rate limited by the output drive circuitry and the attached load.

To reduce the slew rate, enable the slew rate control feature through bit 4 of the *Control Register*. With this feature enabled, the output does not slew directly between the two values. Instead, the output steps digitally at a rate defined by bits [7:5] (SRSTEP) and bits [11:8] (SRCLK) of the *Control Register*. SRCLK defines the rate at which the digital slew updates, and SRSTEP defines the amount by which the output value changes at each update. If the DAC data register is read while the DAC output is still changing, the instantaneous value is read. 表 8-3 lists the slew rate step-size options. 表 8-4 summarizes the slew rate update clock options.

表 8-3. Slew Rate Step-Size (SRSTEP) Options

SRSTEP	STEP SIZE (LSB)	
	DAC7750	DAC8750
000	0.0625	1
001	0.125	2
010	0.25	4
011	0.5	8
100	1	16
101	2	32
110	4	64
111	8	128

表 8-4. Slew Rate Update Clock (SRCLK) Options

SRCLK	DAC UPDATE FREQUENCY (Hz)
0000	258,065
0001	200,000
0010	153,845
0011	131,145
0100	115,940
0101	69,565
0110	37,560
0111	25,805
1000	20,150
1001	16,030
1010	10,295
1011	8,280
1100	6,900
1101	5,530
1110	4,240
1111	3,300

The time required for the output to slew over a given range is expressed as 式 5.

$$\text{Slew Time} = \frac{\text{Output Change}}{\text{Step Size} \cdot \text{Update Clock Frequency} \cdot \text{LSB Size}} \quad (5)$$

where

- *Slew Time* is expressed in seconds
- *Output Change* is expressed in amps (A) for IOUT or volts (V) for VOUT

When the slew rate control feature is enabled, all output changes happen at the programmed slew rate. This configuration results in a staircase formation at the output. If the CLR pin is asserted, the output slews to the zero-scale value at the programmed slew rate. Read bit 1 (SR-ON) of the *Status Register* to verify that the slew operation has completed. The update clock frequency for any given value is the same for all output ranges. The step size, however, varies across output ranges for a given value of step size because the LSB size is different for each output range. 図 8-4 shows an example of IOUT slewing at a rate set by the previously described parameters. In this example for the DAC8750 (LSB size of 305 nA for the 0-mA to 20-mA range), the settings correspond to an update clock frequency of 6.9 kHz and a step size of 128 LSB. As shown in the case with no capacitors on CAP1 or CAP2, the steps occur at the update clock frequency (6.9 kHz corresponds to a period close to 150 µs), and the size of each step is approximately 38 µA (128 × 305 nA). Calculate the slew time for a specific code change by using 式 5.

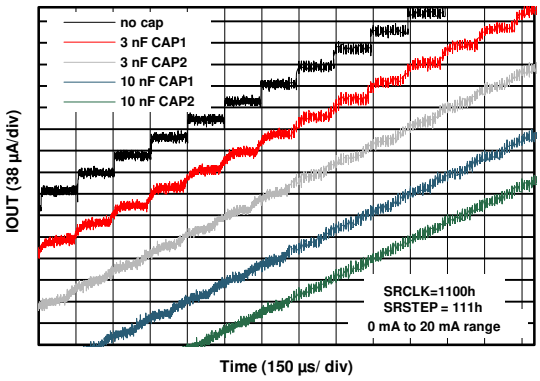


図 8-4. IOUT vs Time With Digital Slew Rate Control

Apply the desired programmable slew rate control setting before updating the DAC data register because updates to the DAC data register in tandem with updates to the slew rate control registers can create race conditions that may result in unexpected DAC data.

8.4 Device Functional Modes

8.4.1 Setting Current-Output Ranges

The current output range is set according to 表 8-5.

表 8-5. RANGE Bits vs Output Range

RANGE	OUTPUT RANGE
101	4 mA to 20 mA
110	0 mA to 20 mA
111	0 mA to 24 mA

Note that changing the RANGE bits at any time causes the DAC data register to be cleared.

8.4.2 Current-Setting Resistor

Resistor R_{SET} (used to convert the DAC voltage to current) illustrated in 図 8-2 determines the stability of the output current over temperature. If desired, an external, low-drift, precision 15-kΩ resistor can be connected to the ISET-R pin and used instead of the internal R_{SET} resistor.

8.4.3 BOOST Configuration for IOUT

図 8-5 illustrates an external NPN transistor used to reduce power dissipation on the die. Most of the load current flows through the NPN transistor with a small amount flowing through the on-chip PMOS transistor based on the gain of the NPN transistor. This configuration reduces the temperature induced drift on the die and internal reference and is an option for use cases at the extreme end of the supply, load current, and ambient temperature ranges.

The inclusion of the bipolar junction transistor (BJT) adds an additional open loop gain to internal amplifier A2 (see 図 8-2) and thus, can cause possible instability. Adding series emitter resistor R2 decreases the gain of the stage created by the BJT and internal R3 resistor (see 図 8-2) especially for cases where R_{LOAD} is a short or a very small load, such as a multimeter. Recommended values for R_1, R_2, and C_1 in this circuit are 1 kΩ, 30 Ω and 22 nF, respectively. An equivalent solution is to place R_2 (with a recommended value of 3 kΩ instead of 30 Ω) in series with the base of the transistor instead of the configuration provided in 図 8-5. Note that there is some gain error introduced by this configuration; see 図 7-14, 図 7-15 and 図 7-16. Use the internal transistor in most cases because the values in *セクション 7.5* are based on the configuration with the internal on-chip PMOS transistor.

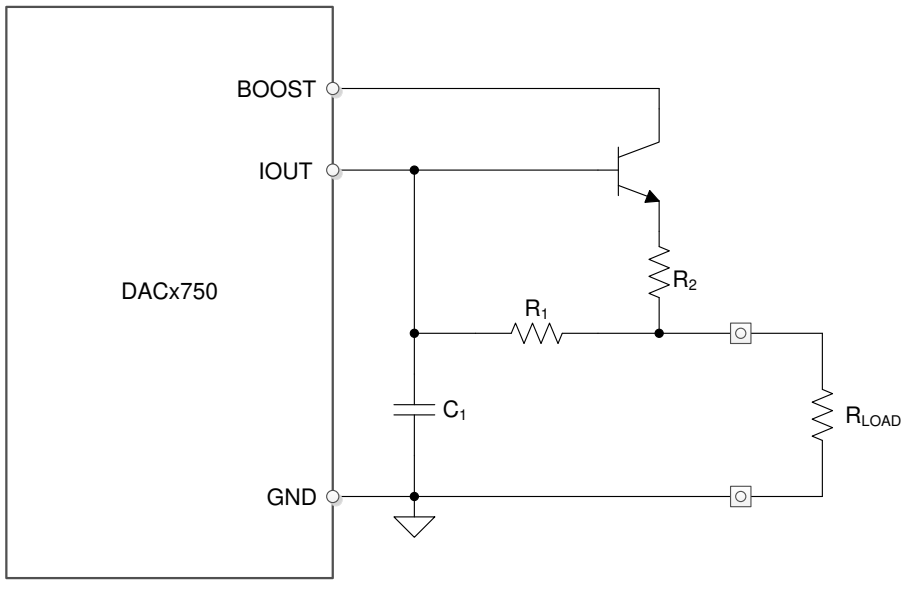


図 8-5. Boost Mode Configuration

8.4.4 Filtering The Current Output

The DACx750 provides access to internal nodes of the circuit; see 図 9-2. Place capacitors on these pins and AVDD to form a filter on the output current, reducing bandwidth and the slew rate of the output, especially useful for driving inductive loads. However, to achieve large reductions in slew rate, use the programmable slew rate to avoid having to use large capacitors. Even in that case, use the capacitors on CAP1 and CAP2 to smooth out the stairsteps caused by the digital code changes as shown in 図 8-6. However, note that power supply ripple also couples into the devices through these capacitors.

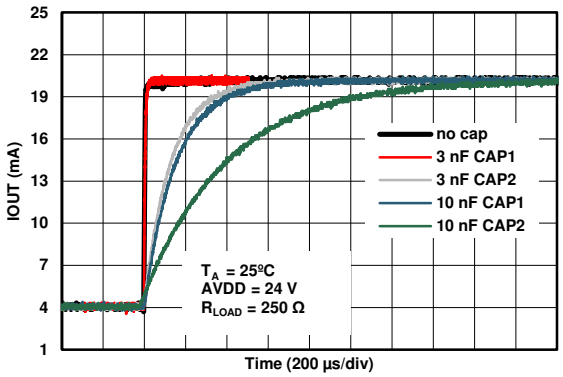


図 8-6. IOUT vs Time for Different Cap Values on CAP1 and CAP2

8.4.5 Output Current Monitoring

Many applications, especially for functional safety, require monitoring to make sure that the output current stays close to the programmed value. To monitor the output current, place a sense resistor in series with the output and measure the voltage across the resistor. However, this resistor reduces the compliance voltage available for the load. The DACx750 provide access to an internal precision resistor (R3 in 図 8-2) through the R3-SENSE and BOOST pins to perform analog readback for monitoring the output current. Measure the voltage between the R3-SENSE and BOOST pins and divide by the value of the R3 resistor to determine the magnitude of the output current. The R3 resistor has a typical value of 40 Ω (see 図 7-38 for a plot of resistance vs temperature) with a temperature drift coefficient of 40 ppm/°C (see 図 7-39 for a histogram of R3 resistance temperature drift). The R3 resistor is tested to stay within the minimum (36 Ω) and maximum (44 Ω) resistance values shown in the *R3 Resistor* portion of *セクション 7.5*. To remove the tolerance error, perform a simple calibration by programming a certain value of output current, measuring the voltage across R3-SENSE and BOOST, and calculating the exact value of R3.

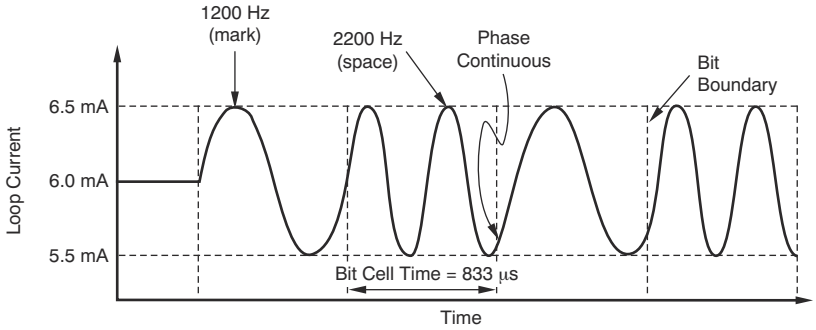
8.4.6 HART Interface

For the DACx750, HART digital communication can be modulated onto the input signal by the methods shown in the following subsections. For more detail, see *Implementing HART Communication with the DAC8760 Family*.

8.4.6.1 Implementing HART in 4-mA to 20-mA Mode

This method is limited to the case where the RANGE bits of the *Control Register* are programmed to the 4-mA to 20-mA range. Some applications require going beyond the 4-mA to 20-mA range. In those cases, see the methods described in the next subsection.

The external HART signal (ac voltage; 500 mV_{PP}, 1200 Hz, and 2200 Hz) can be capacitively coupled in through the HART-IN pin and transferred to a current that is superimposed on the 4-mA to 20-mA current output. The HART-IN pin has a typical input impedance of 35 kΩ that together with the input capacitor used to couple the external HART signal, forms a filter to attenuate frequencies beyond the HART band-pass region. In addition to this filter, an external passive filter is recommended to complete the filtering requirements of the HART specifications. 図 8-7 shows the output current versus time operation for a typical HART signal. 表 8-6 specifies the performance of the HART-IN pin.



DC current = 6 mA.

図 8-7. Output Current vs Time

表 8-6. HART-IN Pin Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input impedance	HART signal ac-coupled into pin		35		kΩ
Output current (peak-to-peak)	Input signal of 500 mV (peak-to-peak)	0.9	1	1.1	mA

8.4.6.2 Implementing HART in All Current Output Modes

The use of the HART-IN pin to implement HART modulation is limited to the case where the RANGE bits of the *セクション 8.6.1.1* are set to the 4-mA to 20-mA range. If it is desirable to implement HART in all current-output modes, see セクション 9.1.1.

8.5 Programming

表 8-11 describes the available commands and registers on the DACx750 devices. *No operation*, *read operation*, and *watchdog timer* refer to commands and are not explicit registers. For more information on these commands, see *セクション 8.5.1.3* and *セクション 8.3.8*.

8.5.1 Serial Peripheral Interface (SPI)

The device is controlled over a versatile four-wire serial interface (SDI, SDO, SCLK, and LATCH) that operates at clock rates of up to 30 MHz and is compatible with SPI, QSPI, Microwire, and digital signal processing (DSP) standards. The SPI communication command consists of a write address byte and a data word for a total of 24 bits. The timing for the digital interface is illustrated in 図 7-1 and 図 7-2.

8.5.1.1 SPI Shift Register

The default frame is 24 bits wide (see *セクション 8.3.9* for 32-bit frame mode) and begins with the rising edge of SCLK that clocks in the MSB. The subsequent bits are latched on successive rising edges of SCLK. The default 24-bit input frame consists of an 8-bit address byte followed by a 16-bit data word as shown in 表 8-7.

表 8-7. Default SPI Frame

BIT 23:BIT 16	BIT 15:BIT 0
Address byte	Data word

The host processor must issue 24 bits before it issues a rising edge on the LATCH pin. Input data bits are clocked in regardless of the LATCH pin and are unconditionally latched on the rising edge of LATCH. By default, the SPI shift register resets to 0x000000 at power on or after a reset.

8.5.1.2 Write Operation

A write operation is accomplished when the address byte is set according to 表 8-8. For more information on the DACx750 registers, see *セクション 8.6*.

表 8-8. Write Address Functions

ADDRESS BYTE (HEX)	FUNCTION
00	No operation (NOP)
01	Write DAC Data register
02	Register read
55	Write control register
56	Write reset register
57	Write configuration register
58	Write DAC gain calibration register
59	Write DAC zero calibration register
95	Watchdog timer reset
96	CRC error reset

8.5.1.3 Read Operation

A read operation is accomplished when the address byte is 0x02. Follow the read operation with a no-operation (NOP) command to clock out an addressed register; see 図 7-2. To read from a register, the address byte and data word is as shown in 表 8-9. The read register value is output MSB first on SDO on successive falling edges of SCLK.

表 8-9. Default SPI Frame for Register Read

ADDRESS BYTE (HEX)	DATA WORD	
	BIT 15:BIT 6	BIT 5:BIT 0
02	X (*don't care*)	Register read address (see 表 8-10)

表 8-10 shows the register read addresses available on the DACx750 devices.

表 8-10. Register Read Address Functions

READ ADDRESS(1)	FUNCTION
XX XX00	Read status register
XX XX01	Read DAC data register
XX XX10	Read control register
00 1011	Read configuration register
01 0011	Read DAC gain calibration register
01 0111	Read DAC zero calibration register

(1) X denotes *don't care* bits.

8.5.1.4 Stand-Alone Operation

SCLK can operate in either continuous or burst mode, as long as the LATCH rising edge occurs after the appropriate number of SCLK cycles. Providing more than or less than 24 SCLK cycles before the rising edge of LATCH results in incorrect data being programmed into the device registers, and incorrect data sent out on SDO. The rising edge of SCLK that clocks in the MSB of the 24-bit input frame marks the beginning of the write cycle, and data are written to the addressed registers on the rising edge of LATCH.

8.5.1.5 Multiple Devices on the Bus

Communication with the device is not directly gated by LATCH; therefore, do not connect multiple devices in parallel without gating SCLK. 図 8-8 shows two devices with SCLK gated for each device.

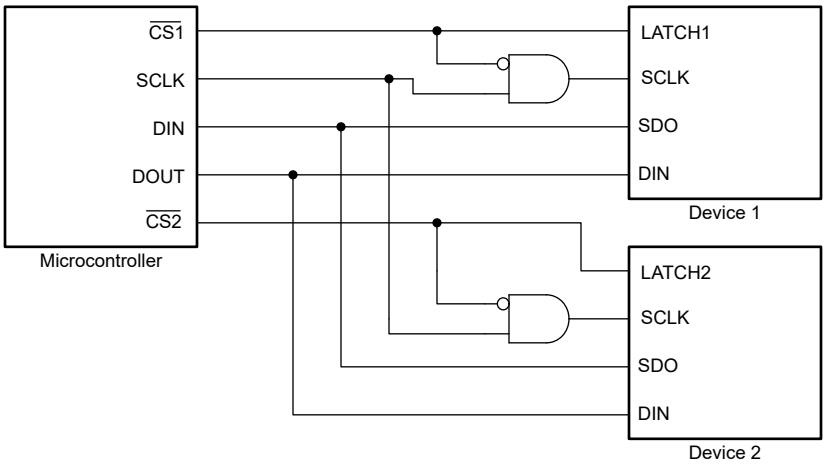


図 8-8. Multiple Devices on the Bus Using Gated SCLK

The microcontroller uses two chip select lines, one for each LATCH pin. Each line is used to gate the SCLK for communication for each device.

8.6 Register Maps

表 8-11 shows the available registers on the DACx750 devices. See セクション 8.6.1 for descriptions of all DACx750 registers.

表 8-11. Command and Register Map

REGISTER OR COMMAND	READ AND WRITE ACCESS	DATA BITS (DB15:DB0)													
		15:14	13	12	11	10:9	8	7	6	5	4	3	2	1	0
Control	RW	X	REXT	OUTEN	SRCLK			SRSTEP			SREN	Reserved	RANGE		
Configuration	RW	X(1)								CALEN	HARTEN	CRCEN	WDEN	WDPD	
DAC Data(2)	RW	D15:D0													
No operation(3)	—	X													
Read Operation (3)	—	X								READ ADDRESS					
Reset	W														RESET
Status	R	Reserved									CRC-FLT	WD-FLT	I-FLT	SR-ON	T-FLT
DAC Gain Calibration (2)	RW	G15:G0, unsigned													
DAC Zero Calibration (2)	RW	Z15:Z0, signed													
Watchdog Timer Reset (3)	—	X													
CRC Fault Reset (3)	—	X													

(1) X denotes *don't care* bits.
(2) DAC8750 (16-bit version) shown. DAC7750 (12-bit version) contents are located in DB15:DB4. For DAC7750, DB3:DB0 are *don't care* bits when writing and zeros when reading.
(3) *No operation*, *read operation*, *watchdog timer reset*, and *CRC fault reset* are commands and not registers.

8.6.1 DACx750 Register Descriptions

8.6.1.1 Control Register

The DACx750 control register is written to at address 0x55. 表 8-12 shows the description for the control register bits.

表 8-12. Control Register

DATA BIT(S)	NAME	DEFAULT	DESCRIPTION
DB15:DB14	Reserved	00	Reserved. Do not write any value other than zero to these bits.
DB13	REXT	0	External current setting resistor enable.
DB12	OUTEN	0	Output enable. Bit = 1: Output is determined by RANGE bits. Bit = 0: Output is disabled. IOUT is Hi-Z.
DB11:DB8	SRCLK[3:0]	0000	Slew rate clock control. Ignored when bit SREN = 0.
DB7:DB5	SRSTEP[2:0]	000	Slew rate step size control. Ignored when bit SREN = 0.
DB4	SREN	0	Slew Rate Enable. Bit = 1: Slew rate control is enabled, and the ramp speed of the output change is determined by SRCLK and SRSTEP. Bit = 0: Slew rate control is disabled. Bits SRCLK and SRSTEP are ignored. The output changes to the new level immediately.
DB3	Reserved	0	Reserved. Must be set to 0.
DB2:DB0	RANGE[2:0]	000	Output range bits.

8.6.1.2 Configuration Register

The DACx750 configuration register is written to at address 0x57. 表 8-13 summarizes the description for the configuration register bits.

表 8-13. Configuration Register

DATA BIT(S)	NAME	DEFAULT	DESCRIPTION
DB15:DB6	Reserved	00 0000 0000	Reserved. Do not write any value other than zero to these bits.
DB5	CALEN	0	User calibration enable. When user calibration is enabled, the DAC data are adjusted according to the contents of the gain and zero calibration registers. See the *セクション 8.3.10* section.
DB4	HARTEN	0	Enable interface through HART-IN pin (only valid for IOUT set to 4-mA to 20-mA range through RANGE bits). Bit = 1: HART signal is connected through internal resistor and modulates output current. Bit = 0: HART interface is disabled.
DB3	CRCEN	0	Enable frame error checking.
DB2	WDEN	0	Watchdog timer enable.
DB1:DB0	WDPD[1:0]	00	Watchdog timeout period.

8.6.1.3 DAC Registers

The DAC registers consist of a DAC data register (表 8-14), a DAC gain calibration register (表 8-15), and a DAC zero calibration register (表 8-16). User calibration as described in *セクション 8.3.10* is a feature that allows for trimming the system gain and zero errors. 表 8-14 through 表 8-16 show the DAC8750, 16-bit version of these registers. The DAC7750 (12-bit version) register contents are located in DB15:DB4. For DAC7750, DB3:DB0 are *don't care* bits when writing and zeros when reading.

表 8-14. DAC Data Register

DATA BITS	NAME	DEFAULT	DESCRIPTION
DB15:DB0	D15:D0	0x0000	DAC data register. Format is unsigned straight binary.

表 8-15. DAC Gain Calibration Register

DATA BITS	NAME	DEFAULT	DESCRIPTION
DB15:DB0	G15:G0	0x0000	Gain calibration register for user calibration. Format is unsigned straight binary.

表 8-16. DAC Zero Calibration Register

DATA BITS	NAME	DEFAULT	DESCRIPTION
DB15:DB0	Z15:Z0	0x0000	Zero calibration register for user calibration. Format is twos complement.

8.6.1.4 Reset Register

The DACx750 reset register is written to at address 0x56. 表 8-17 provides the description.

表 8-17. Reset Register

DATA BIT(S)	NAME	DEFAULT	DESCRIPTION
DB15:DB1	Reserved	000 0000 0000 0000	Reserved. Writing to these bits does not cause any change.
DB0	RESET	0	Software reset bit. Writing 1 to the bit performs a software reset that resets all registers and the $\overline{\text{ALARM}}$ status to the respective power-on reset default value. After reset completes, the RESET bit clears itself.

8.6.1.5 Status Register

This read-only register consists of four $\overline{\text{ALARM}}$ status bits (CRC-FLT, WD-FLT, I-FLT, and T-FLT) and the SR-ON bit that shows the slew rate status, as shown in 表 8-18.

表 8-18. Status Register

DATA BIT(S)	NAME	DEFAULT	DESCRIPTION
DB15:DB5	Reserved	000 0000 0000	Reserved. Reading these bits returns 0.
DB4	CRC-FLT	0	Bit = 1 indicates CRC error on SPI frame. Bit = 0 indicates normal operation.
DB3	WD-FLT	0	Bit = 1 indicates watchdog timer timeout. Bit = 0 indicates normal operation.
DB2	I-FLT	0	Bit = 1 indicates an open circuit or a compliance voltage violation in IOUT loading. Bit = 0 indicates IOUT load is at normal condition.
DB1	SR-ON	0	Bit = 1 when DAC code is slewing as determined by SRCLK and SRSTEP. Bit = 0 when DAC code is not slewing.
DB0	T-FLT	0	Bit = 1 indicates die temperature is over 142°C. Bit = 0 indicates die temperature is not over 142°C.

These devices continuously monitor the current output and die temperature. When an alarm occurs, the corresponding $\overline{\text{ALARM}}$ status bit is set (1). Whenever an $\overline{\text{ALARM}}$ status bit is set, it remains set until the event that caused it is resolved. The $\overline{\text{ALARM}}$ bit can only be cleared by performing a software reset, a power-on reset (by cycling power), or by having the error condition resolved. These bits are reasserted if the alarm condition continues to exist in the next monitoring cycle.

The $\overline{\text{ALARM}}$ bit goes to 0 when the error condition is resolved.

9 Application and Implementation

Note

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9.1 Application Information

9.1.1 HART Implementation

If desirable, the following subsections show two methods to implement HART, irrespective of the RANGE bit settings.

9.1.1.1 Using the CAP2 Pin

The first method to implement HART is to couple the signal through the CAP2 pin, as shown in 図 9-1.

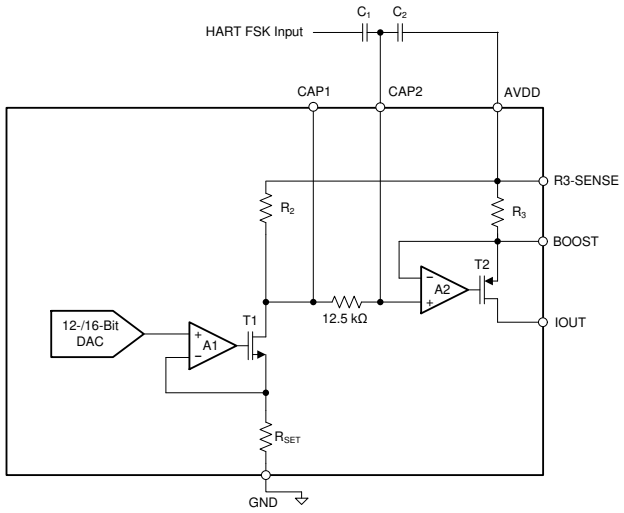

図 9-1. Implementing HART on IOUT Using the CAP2 Pin

In 図 9-1, R_3 is nominally 40 Ω, and R_2 depends on the current output range (set by the RANGE bits), described as follows:

- 4-mA to 20-mA range: R_2 = 2.4 kΩ (typical)
- 0-mA to 20-mA range: R_2 = 3 kΩ (typical)
- 0-mA to 24-mA range: R_2 = 3.6 kΩ (typical)

The purpose of the 12.5-kΩ resistor is to create a filter when CAP1 and CAP2 are used.

To insert the external HART signal on the CAP2 pin, an external ac-coupling capacitor is typically connected to CAP2. The high-pass filter 3-dB frequency is determined by the resistive impedance looking into CAP2 (R_2 + 12.5 kΩ) and the coupling-capacitor value. The 3-dB frequency is 1 / (2 × π × [R_2 + 12.5 kΩ] × [Coupling Capacitor Value]).

When the input HART frequency is greater than the 3-dB frequency, the ac signal is seen at the plus input of amplifier A2, and is therefore seen across the 40-Ω resistor. To generate a 1-mA signal on the output therefore requires a 40-mV peak-to-peak signal on CAP2. Most HART modems do not output a 40-mV signal; therefore, a capacitive divider is used in 図 9-1 to attenuate the FSK signal from the modem. In 図 9-1, the high-pass cutoff frequency is 1 / (2 × π × [R_2+ 12.5 kΩ] × [C_1 + C_2]). There is one disadvantage to this approach: if the AVDD supply is not clean, any ripple on the supply could couple into the device.

9.1.1.2 Using the ISET-R Pin

The second method to implement HART is to couple the HART signal through the ISET-R pin when IOUT is operated using an external R_{SET} resistor. The FSK signal from the modem is ac-coupled into the pin through a series combination of Rin and Cin as shown in 図 9-2.

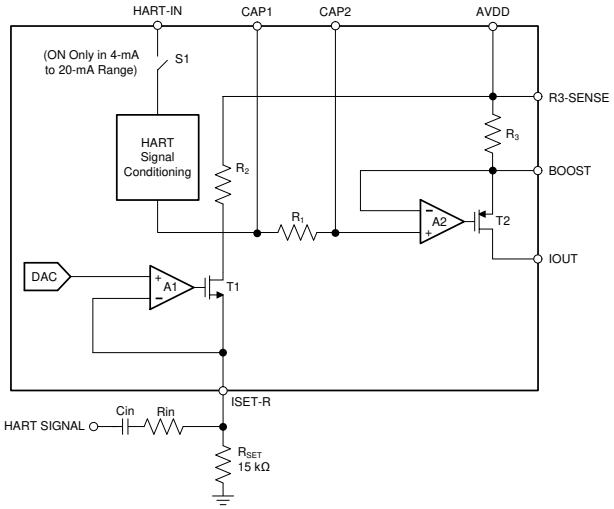

図 9-2. Implementing HART with the ISET-R pin

The magnitude of the ac-current output is calculated with 式 6.

$$(V_{HART} \times k) / Rin \quad (6)$$

where

- V_{HART} is the amplitude of the HART FSK signal from the modem
- k is a constant that represents the gain transfer function from the ISET-R pin to the IOUT pin and depends on the selected current output range as follows:
  - k = 60 for the 4-mA to 20-mA range
  - k = 75 for the 0-mA to 20-mA range
  - k = 90 for the 0-mA to 24-mA range

The series input resistor and capacitor form a high-pass filter at the ISET-R pin. Select Cin to make sure that all signals in the HART extended-frequency band pass through unattenuated.

9.2 Typical Application

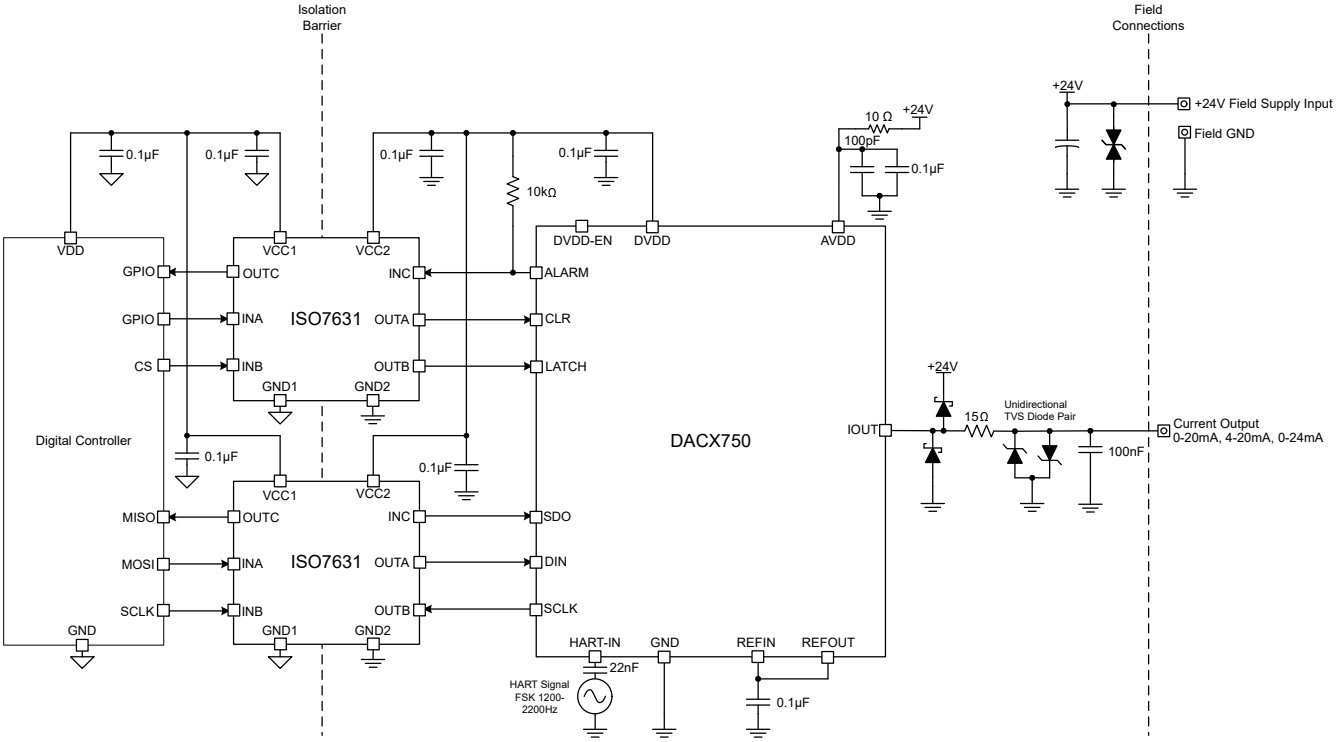

図 9-3. DACx750 in a Voltage and Current Output Driver for Factory Automation and Control, EMC and EMI Protected - DACx750 in an Analog Output (AO) Module

9.2.1 Design Requirements

Analog I/O modules are used by programmable logic controllers (PLCs) and distributed control systems (DCSs) to interface to sensors, actuators, and other field instruments. These modules must meet stringent electrical specifications for both performance as well as protection. These outputs are typically current loops based on the 4-mA to 20-mA range. Common error budgets accommodate 0.1% full-scale range total unadjusted error (%FSR TUE) at room temperature. Designs which desire stronger accuracy over temperature frequently implement calibration. Often times the PLC back-plane provides access to a 12-V to 36-V analog supply, from which a majority of supply voltages are derived.

9.2.2 Detailed Design Procedure

図 9-4 illustrates a common generic solution for realizing these desired voltage and current output spans.

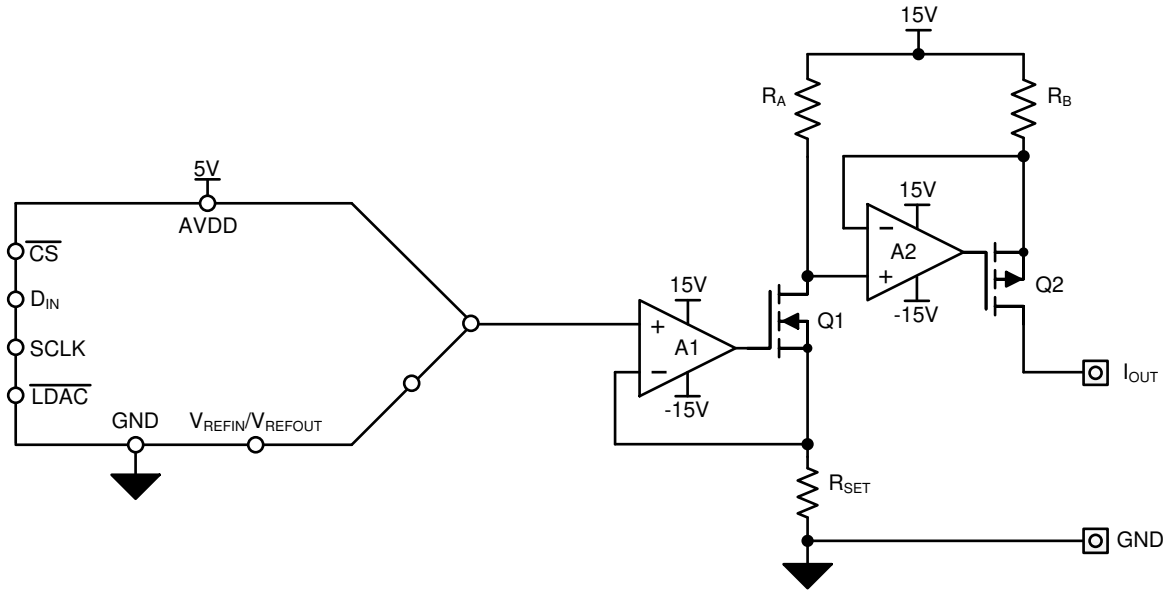

図 9-4. Generic Design for Typical PLC Current and Voltage Outputs

The current output circuit is comprised of amplifiers A1 and A2, MOSFETs Q1 and Q1, and the three resistors R_{SET}, R_A, and R_B. This two-stage current source enables the ground-referenced DAC output voltage to drive the high-side amplifier required for the current-source.

The high-level of integration of the DACx750 family lends itself very well to the design of analog output modules, offering simplicity of design and reducing solution size. The DACx750 integrates all of the components shown in 図 9-4 allowing a software configurable current output driver. 図 9-3 illustrates an example circuit design for such an application using the DACx750 for the current output driver.

The design uses two triple channel isolators (ISO7631FC) to provide galvanic isolation for the digital lines to communicate to the main controller. Note that these isolators can be driven by the internally-generated supply (DVDD) from the DACx750 to save components and cost. The DACx750 supplies up to 10 mA that meets the supply requirements of the two isolators running at up to 10 Mbps. Note that additional cost savings are possible if noncritical digital signals such as CLR and ALARM are tied to GND or left unconnected. Finally, a protection scheme with transient voltage suppressors and other components is placed on all pins which connect to the field.

The protection circuitry is designed to provide immunity to the IEC61000-4 test suite which includes system-level industrial transient tests. The protection circuit includes transient voltage suppressor (TVS) diodes, clamp-to-rail steering diodes, and pass elements in the form of resistors and ferrite beads. For more detail about selecting these components, see the *Single-Channel Industrial Voltage and Current Output Driver, Isolated, EMC/EMI Tested Reference Design*.

9.2.3 Application Curve

The current output circuit was measured in 0-mA to 24-mA mode using an 8.5 digit digital multimeter to measure the output while driving a 300-Ω load at 25°C. The measured results are illustrated in 図 9-5. The current output remains within the data sheet specified performance.

The design was also exposed to IEC61000-4 electrostatic discharge, electrically fast transient, conducted immunity, and radiated immunity tests on both the current and voltage outputs. During each of these tests a 6.5 digit digital multimeter, set in fast 5.5 digit acquisition mode, was used to monitor the output. Complete data sets for the voltage and current outputs during these tests are available in the *Single-Channel Industrial Voltage and Current Output Driver, Isolated, EMC/EMI Tested Reference Design*.

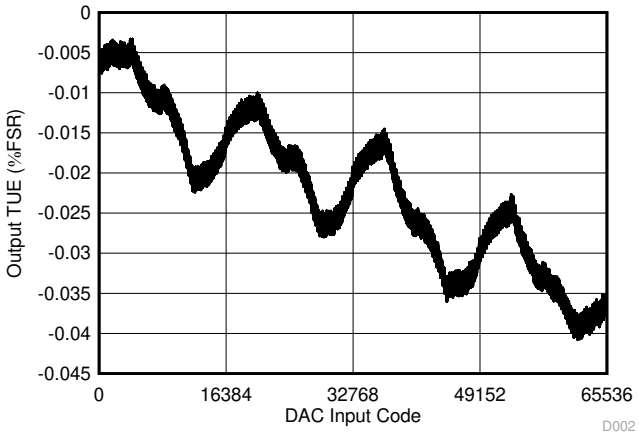

図 9-5. Current Output TUE vs Code

10 Power Supply Recommendations

The DACx750 family operates within the specified single-supply range of 10 V to 36 V applied to the AVDD pin. The digital supply, DVDD, operates within the specified supply range of 2.7 V to 5.5 V or powered by the internal 4.6-V LDO, as described in セクション 8.3.4.

Switching power supplies and DC/DC converters often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes. This noise can be easily coupled into the DAC output voltage or current through various paths between the power connections and analog output. To further reduce noise, include bulk and local decoupling capacitors.

CAUTION

Do not ramp the supplies for the DACx750 faster than 1 V/ns or damage may result to the device. A 10-Ω series resistor from the analog supply to the device AVDD connection helps reduce the supply ramp.

The DACx750 has internal power on reset (POR) circuitry for both the digital DVDD and analog AVDD supplies. This circuitry makes sure that the internal logic and power-on state of the DAC power up to the proper state independent of the supply sequence. The recommended power-supply sequence is to first have the analog AVDD supply come up, followed by the digital DVDD supply. DVDD can come up first as long as AVDD ramps to at least 5 V within 50 µs. If neither condition can be satisfied, issue a software reset command using the SPI bus after both AVDD and DVDD are stable.

The current consumption on the AVDD pin and current ranges for the current output are listed in *セクション 7.5*. The power supply must meet the requirements listed in *セクション 7.5*.

11 Layout

11.1 Layout Guidelines

To maximize the performance of the DACx750 in any application, good layout practices and proper circuit design must be followed. A few recommendations specific to the DACx750 are:

- As illustrated in 図 9-1, CAP2 is directly connected to the input of the final IOUT amplifier. Any noise or unwanted ac signal routed near the CAP1 and CAP2 pins could capacitively couple onto internal nodes and affect IOUT. Therefore, make sure to avoid routing any digital or HART signal traces over the CAP1 and CAP2 traces.
- Connect the thermal PAD to the lowest potential in the system.
- Make sure that AVDD has decoupling capacitors local to the respective pins.
- Place the reference capacitor close to the reference input pin.
- Avoid routing switching signals near the reference input.
- For designs that include protection circuits:
  - Place diversion elements, such as TVS diodes or capacitors, close to off-board connectors to make sure that return current from high-energy transients does not cause damage to sensitive devices.
  - Use large, wide traces to provide a low-impedance path to divert high-energy transients away from I/O pins.

11.1.1 Thermal Considerations

The DACx750 is designed for a maximum junction temperature of 150°C. In cases where the maximum AVDD is driving maximum current into ground, this junction temperature can be exceeded. Use 式 7 to determine the maximum junction temperature that can be reached.

$$\text{Power dissipation} = (T_J \text{ max} - T_A) / \theta_{JA} \quad (7)$$

where

- T_J max = 150°C
- T_A is the ambient temperature
- θ_{JA} is the package-dependent, junction-to-ambient thermal resistance, found in *セクション 7.4*.

The power dissipation is calculated by multiplying all the supply voltages with the currents supplied, which are found in the *Power Requirements* subsection of *セクション 7.5*.

Consider an example: IOUT is enabled, supplying 24 mA into GND with a 25°C ambient temperature, AVDD of 24 V, and DVDD is generated internally. From the *セクション 7.5*, the max value of AIDD = 3 mA when IOUT is enabled and DAC code = 0x0000. Also, the max value of DIDD = 1 mA. Accordingly, the worst-case power dissipation is 24 V × (24 mA + 3 mA + 1 mA) = 672 mW. Using the θ_{JA} value for the TSSOP package, we get T_J max = 25°C + (32.3 × 0.672)°C = 46.7°C. At 85°C ambient temperature, the corresponding value of T_J max is 106.7°C. Using this type of analysis, the system designer can both specify and design for the equipment operating conditions. Note that for enhanced thermal performance, connect the thermal pad in both packages to a copper plane.

11.2 Layout Example

図 11-1 shows an example layout for the DACx750 device based on a similar layout for the DACx760 from TIPD153.

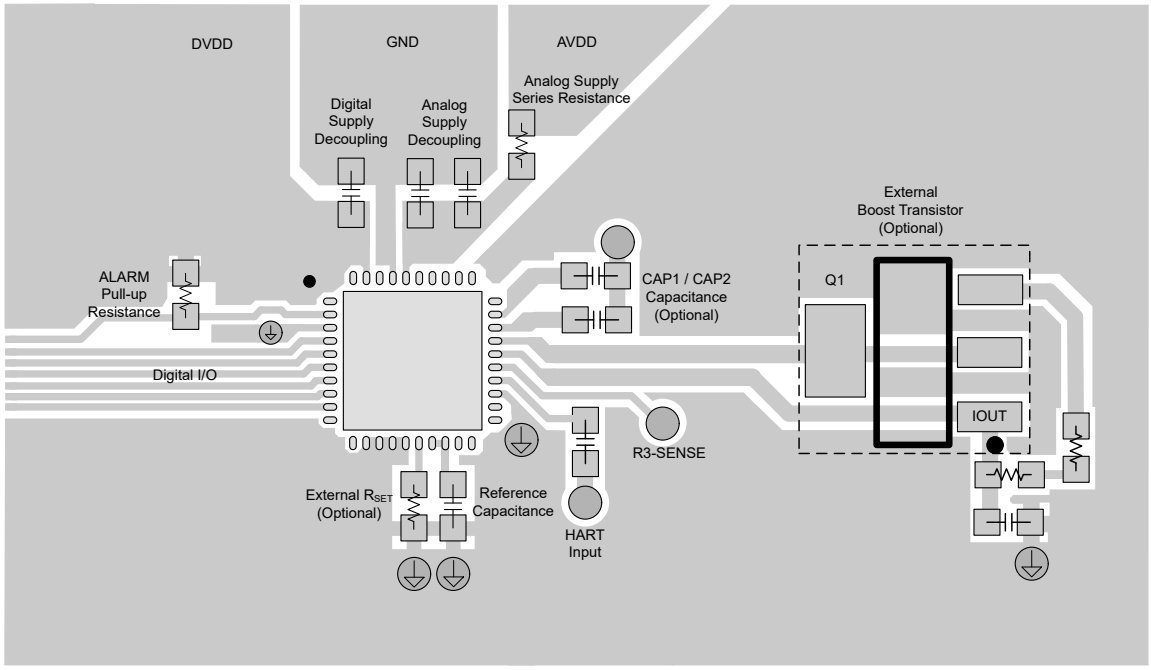

図 11-1. Example Layout

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Single-Channel Industrial Voltage & Current Output Driver, Isolated, EMC/EMI Tested Reference Design*
- Texas Instruments, *Implementing HART™ Communication with the DAC8760 Family*

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 サポート・リソース

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12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DAC7750IPWP	Active	Production	HTSSOP (PWP) | 24	60 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC7750
DAC7750IPWP.A	Active	Production	HTSSOP (PWP) | 24	60 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC7750
DAC7750IPWP.B	Active	Production	HTSSOP (PWP) | 24	60 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC7750
DAC7750IPWPR	Active	Production	HTSSOP (PWP) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC7750
DAC7750IPWPR.A	Active	Production	HTSSOP (PWP) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC7750
DAC7750IPWPR.B	Active	Production	HTSSOP (PWP) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC7750
DAC7750IRHAR	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC7750
DAC7750IRHAR.A	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC7750
DAC7750IRHAR.B	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC7750
DAC7750IRHAT	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC7750
DAC7750IRHAT.A	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC7750
DAC7750IRHAT.B	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC7750
DAC8750IPWP	Active	Production	HTSSOP (PWP) | 24	60 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC8750
DAC8750IPWP.A	Active	Production	HTSSOP (PWP) | 24	60 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC8750
DAC8750IPWP.B	Active	Production	HTSSOP (PWP) | 24	60 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC8750
DAC8750IPWPR	Active	Production	HTSSOP (PWP) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC8750
DAC8750IPWPR.A	Active	Production	HTSSOP (PWP) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC8750
DAC8750IPWPR.B	Active	Production	HTSSOP (PWP) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC8750
DAC8750IPWPRG4	Active	Production	HTSSOP (PWP) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC8750
DAC8750IPWPRG4.A	Active	Production	HTSSOP (PWP) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC8750
DAC8750IPWPRG4.B	Active	Production	HTSSOP (PWP) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC8750
DAC8750IRHAR	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC8750
DAC8750IRHAR.A	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC8750
DAC8750IRHAR.B	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC8750
DAC8750IRHARG4	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC8750
DAC8750IRHARG4.A	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC8750
DAC8750IRHARG4.B	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC8750
DAC8750IRHAT	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC8750
DAC8750IRHAT.A	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC8750

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DAC8750IRHAT.B	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC8750

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

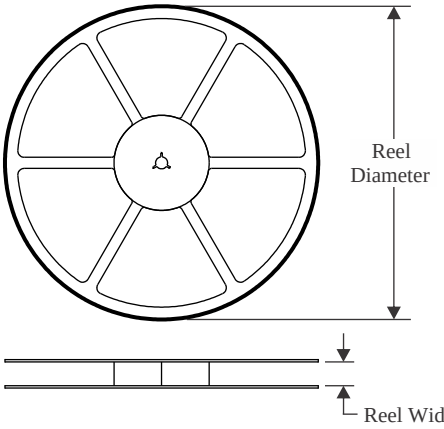
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

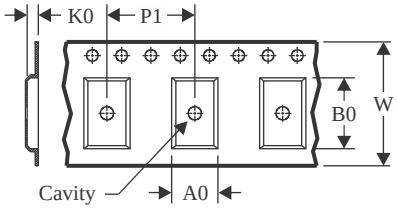
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

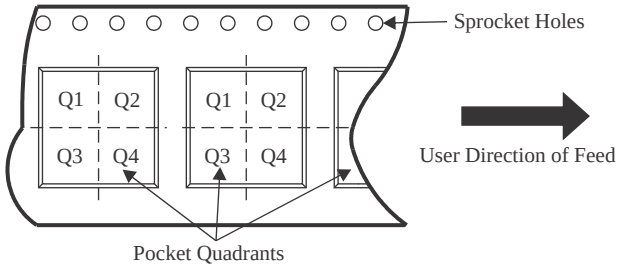


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

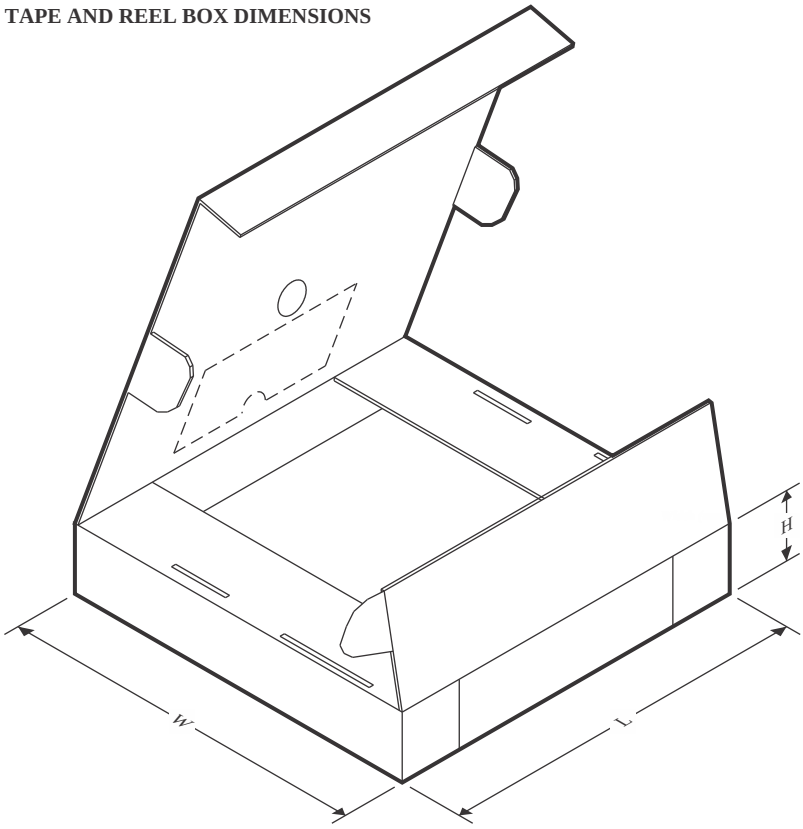
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC7750IPWPR	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
DAC7750IRHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
DAC8750IPWPR	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
DAC8750IPWPRG4	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
DAC8750IRHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
DAC8750IRHARG4	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
DAC8750IRHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

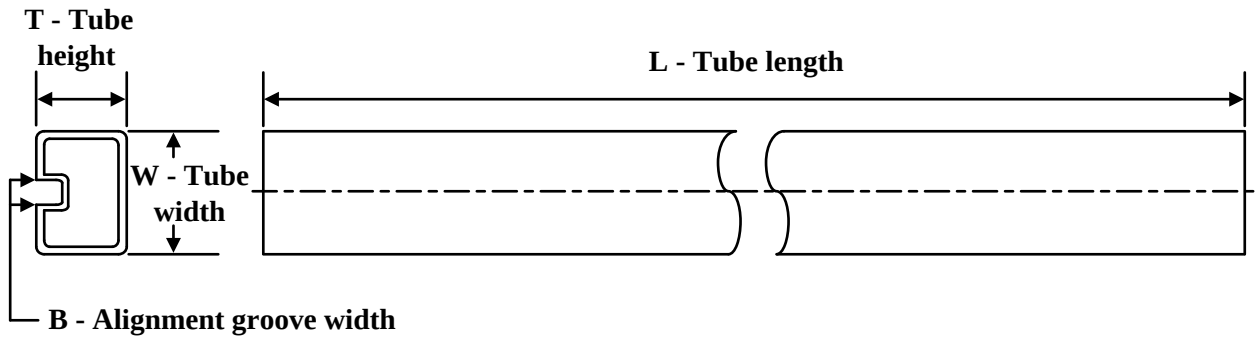
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC7750IPWPR	HTSSOP	PWP	24	2000	350.0	350.0	43.0
DAC7750IRHAT	VQFN	RHA	40	250	210.0	185.0	35.0
DAC8750IPWPR	HTSSOP	PWP	24	2000	350.0	350.0	43.0
DAC8750IPWPRG4	HTSSOP	PWP	24	2000	350.0	350.0	43.0
DAC8750IRHAR	VQFN	RHA	40	2500	367.0	367.0	38.0
DAC8750IRHARG4	VQFN	RHA	40	2500	367.0	367.0	38.0
DAC8750IRHAT	VQFN	RHA	40	250	210.0	185.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DAC7750IPWP	PWP	HTSSOP	24	60	530	10.2	3600	3.5
DAC7750IPWP.A	PWP	HTSSOP	24	60	530	10.2	3600	3.5
DAC7750IPWP.B	PWP	HTSSOP	24	60	530	10.2	3600	3.5
DAC8750IPWP	PWP	HTSSOP	24	60	530	10.2	3600	3.5
DAC8750IPWP.A	PWP	HTSSOP	24	60	530	10.2	3600	3.5
DAC8750IPWP.B	PWP	HTSSOP	24	60	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

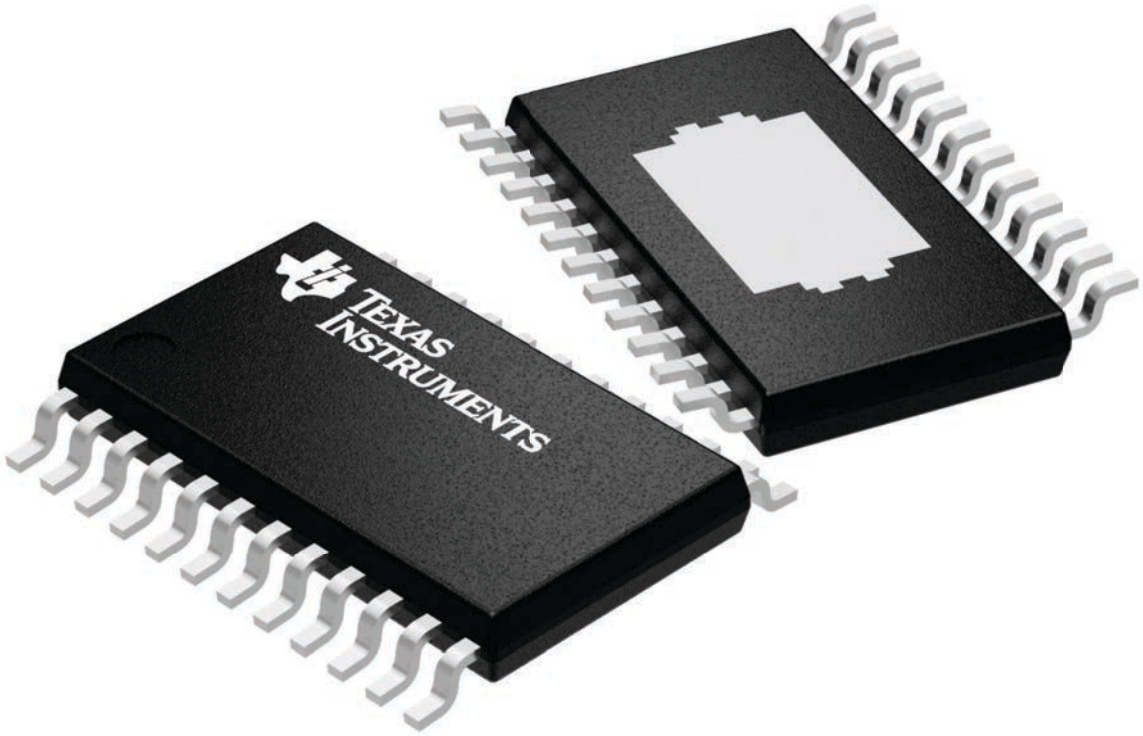
PWP 24

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 7.6, 0.65 mm pitch

PLASTIC SMALL OUTLINE

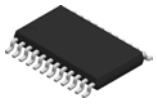
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224742/B

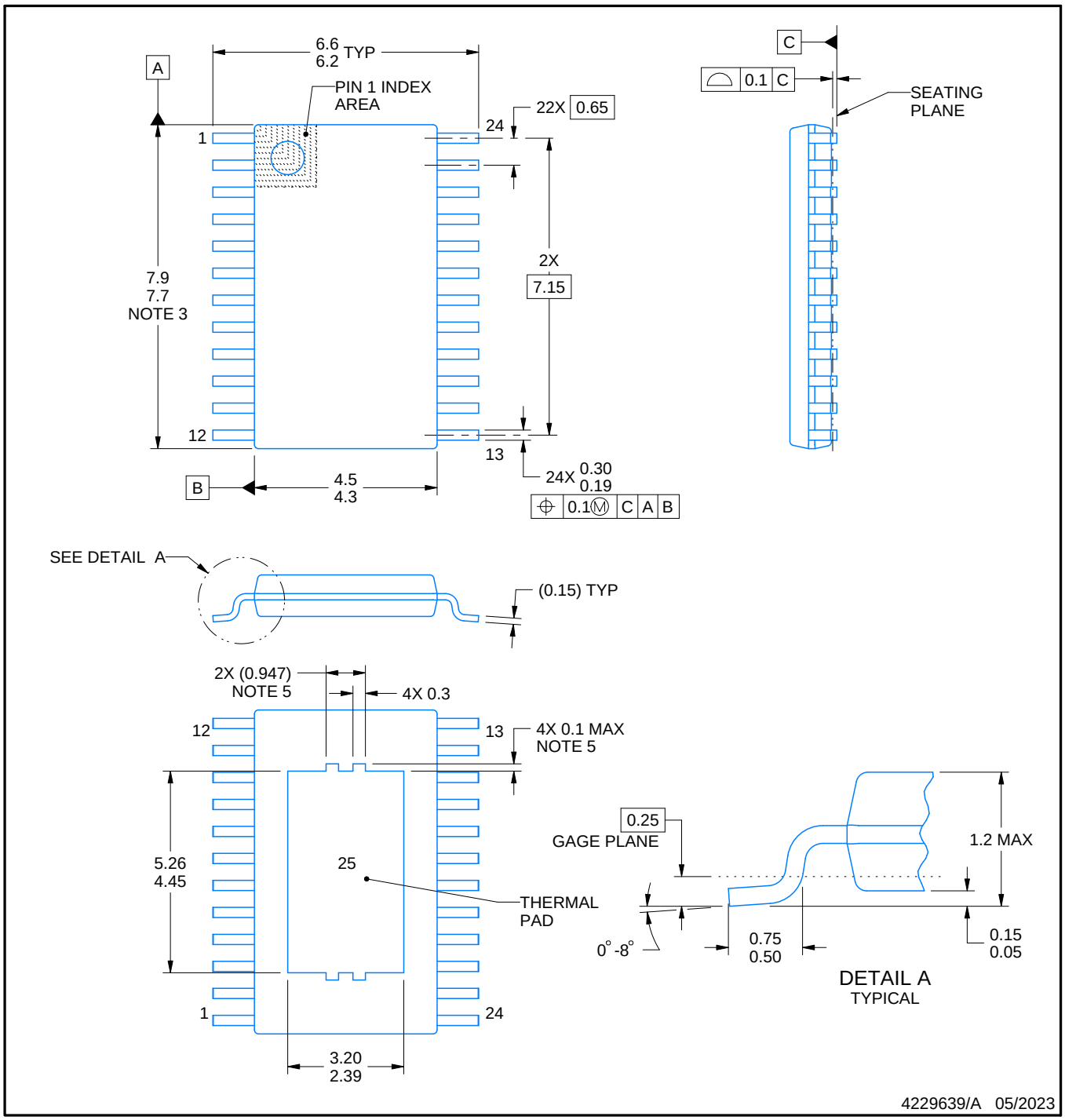
PACKAGE OUTLINE

PWP0024R



PowerPAD™ TSSOP - 1.2 mm max height

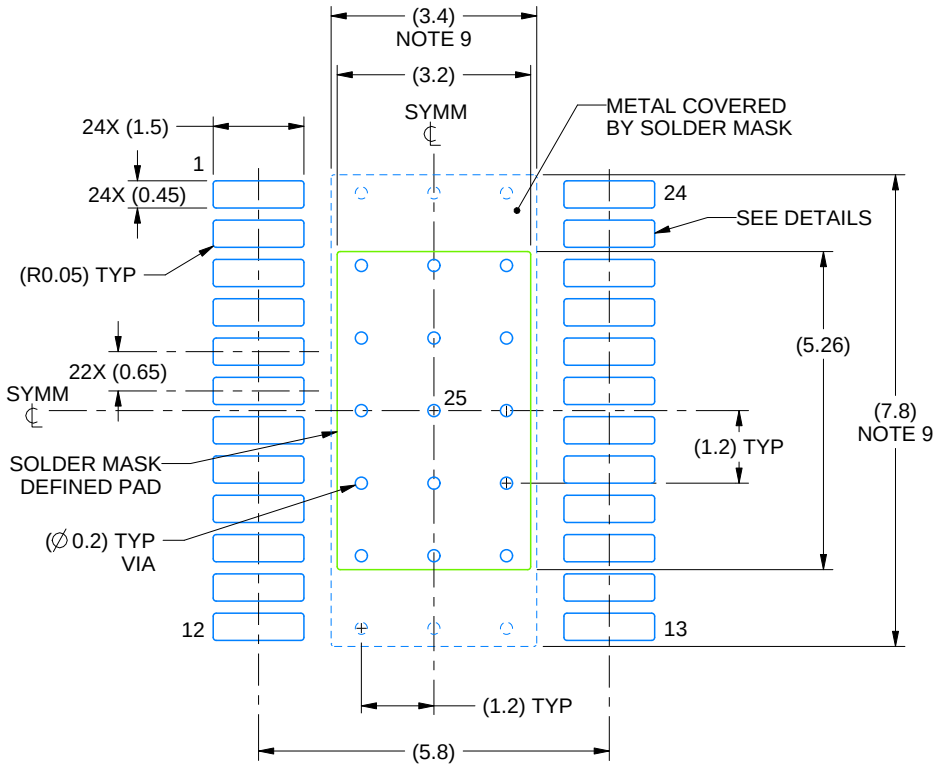
SMALL OUTLINE PACKAGE



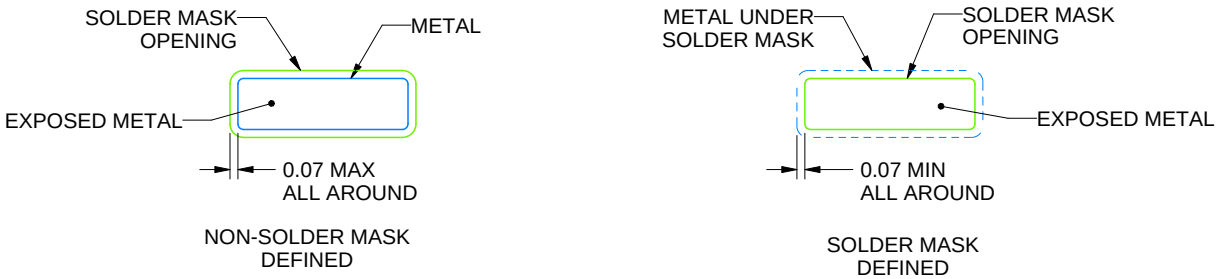
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

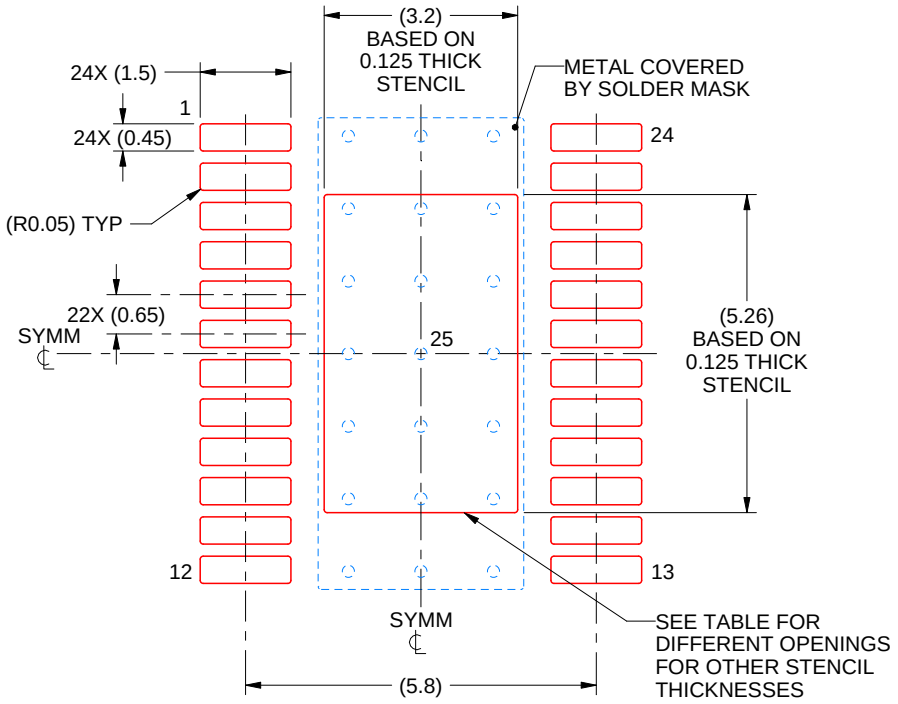


SOLDER MASK DETAILS

4229639/A 05/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.58 X 5.88
0.125	3.20 X 5.26 (SHOWN)
0.15	2.92 X 4.80
0.175	2.70 X 4.45

4229639/A 05/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

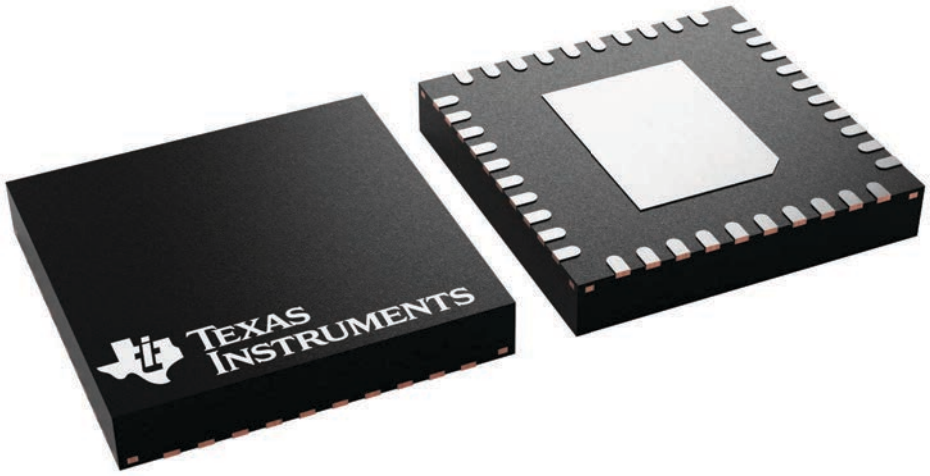
RHA 40

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



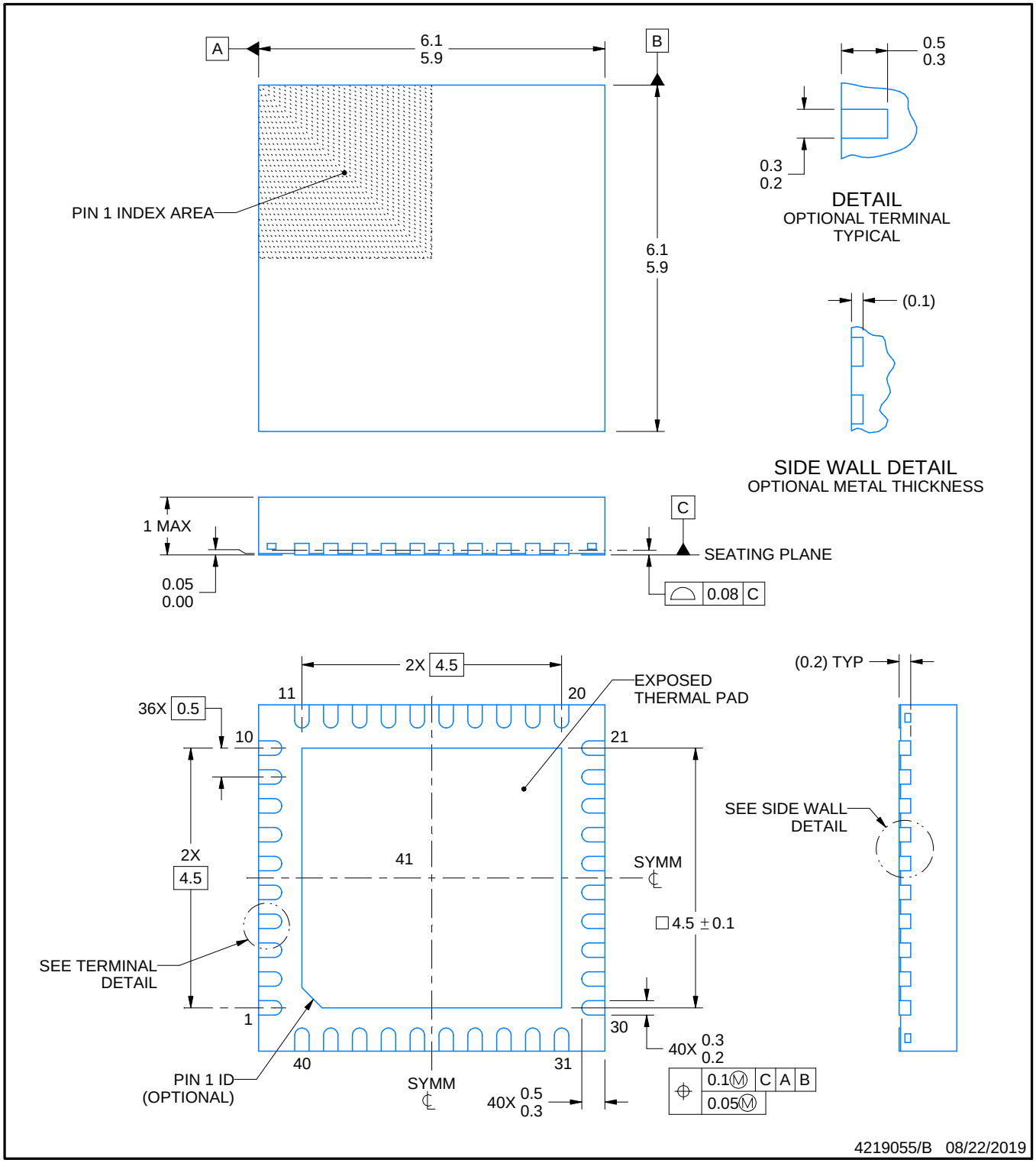
4225870/A

PACKAGE OUTLINE

RHA0040H

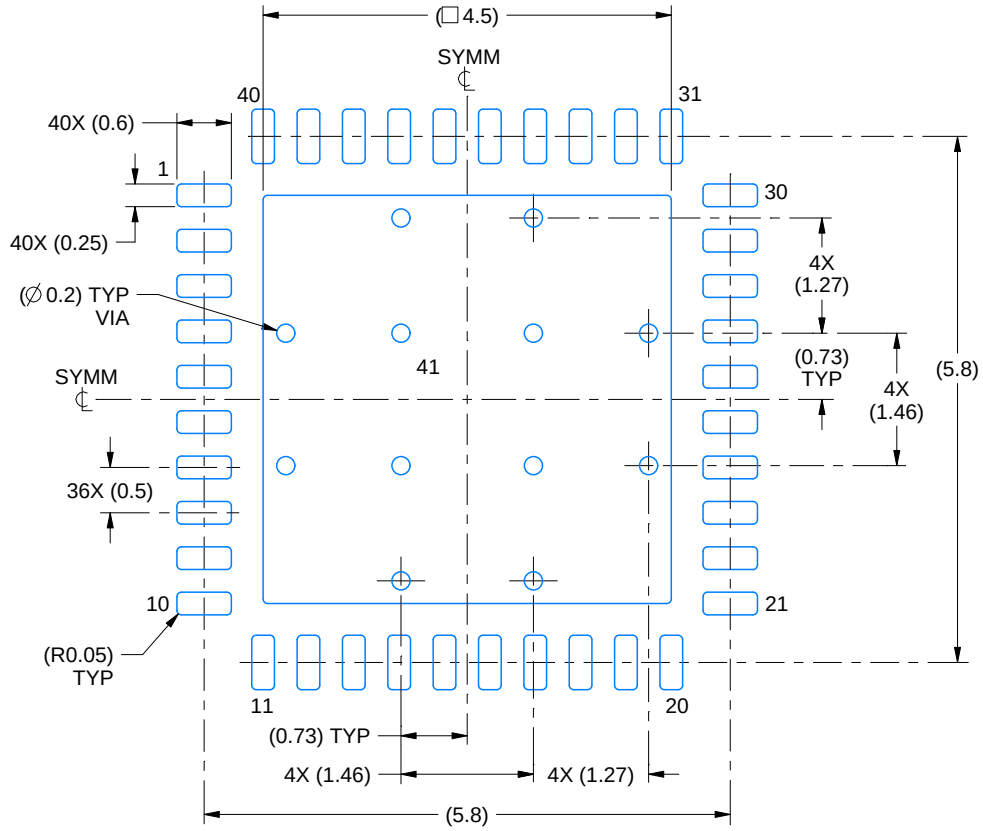
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

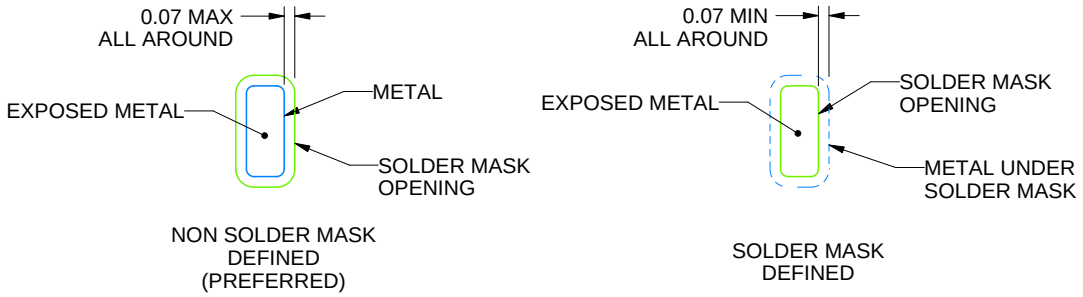


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X

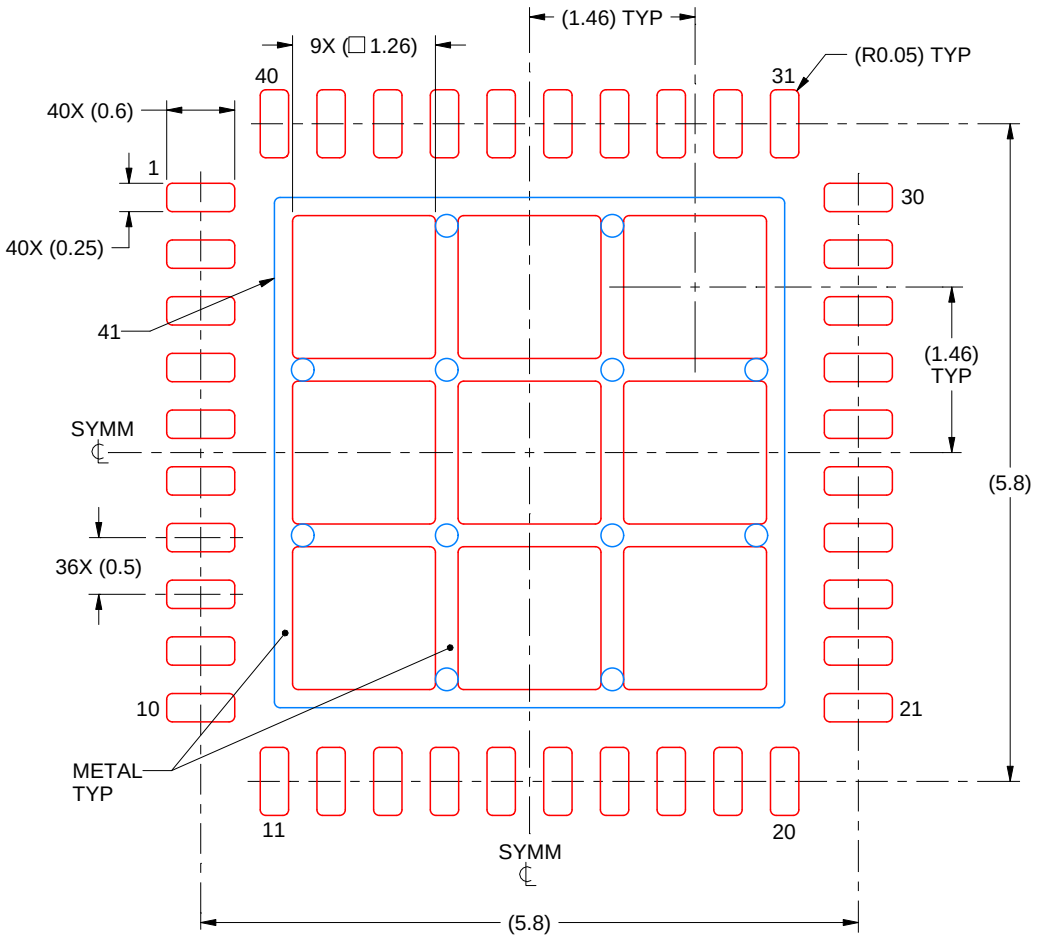


SOLDER MASK DETAILS

4219055/B 08/22/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 41:
70% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

4219055/B 08/22/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月