参考資料

Texas Instruments

DLP472TP
JAJSQF9 – AUGUST 2024

DLP472TP 0.47 インチ 4K UHD デジタル マイクロミラー デバイス

1 特長

- 対角 0.47 インチのマイクロミラー アレイ
  - ディスプレイ解像度:4K UHD (3840 × 2160)
  - 5.4µm のマイクロミラー ピッチ
  - マイクロミラー傾斜角:±17° (平面に対して)
  - 下部光源
- SubLVDS 入力データ バス
- 4K UHD、60Hz (60fps) の動画をサポート
- 1080p、最大 240Hz をサポート
- DLPC8445 ディスプレイ コントローラ、DLPA3085 パワー マネージメント IC (PMIC) および LED ドライバにより、LED の動作をサポート

2 アプリケーション

- モバイル スマート TV
- モバイル プロジェクタ
- デジタル サイネージ

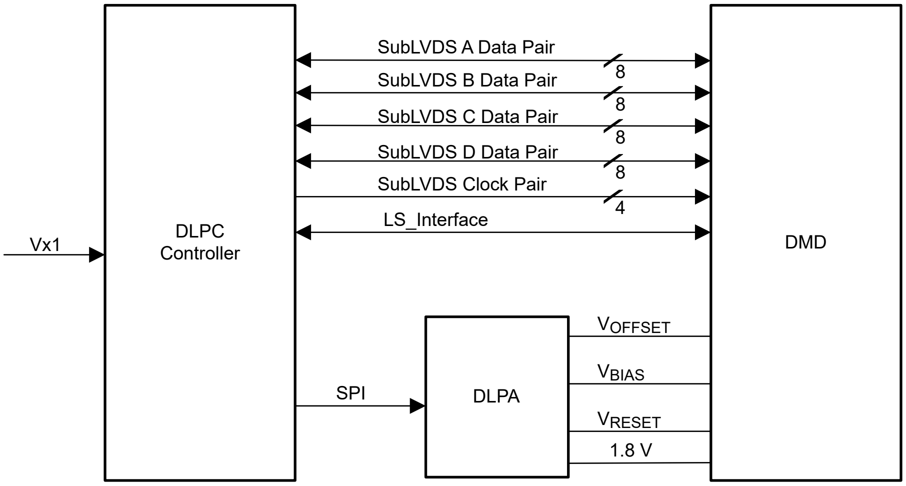
3 概要

DLP472TP デジタル マイクロミラー デバイス (DMD) は、デジタル制御の MEMS (micro-electromechanical system) 空間光変調器 (SLM) で、色鮮やかな 4K UHD ディスプレイ システムを実現します。テキサス・インスツルメンツの DLP® 製品である 0.47 インチ 4K UHD チップセットは、DLP472TP DMD、DLPC8445 ディスプレイ コントローラ、DLPA3085 PMIC および LED ドライバで構成されています。このコンパクトなチップセットは、小型の 4K UHD ディスプレイを実現する完全なシステム ソリューションを提供します。

製品情報

部品番号	パッケージ(1)	パッケージ サイズ
DLP472TP	FQY (166)	24.50mm × 11.00 mm

(1) 詳細については、セクション 12 を参照してください。



アプリケーション概略図

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4 Pin Configuration and Functions

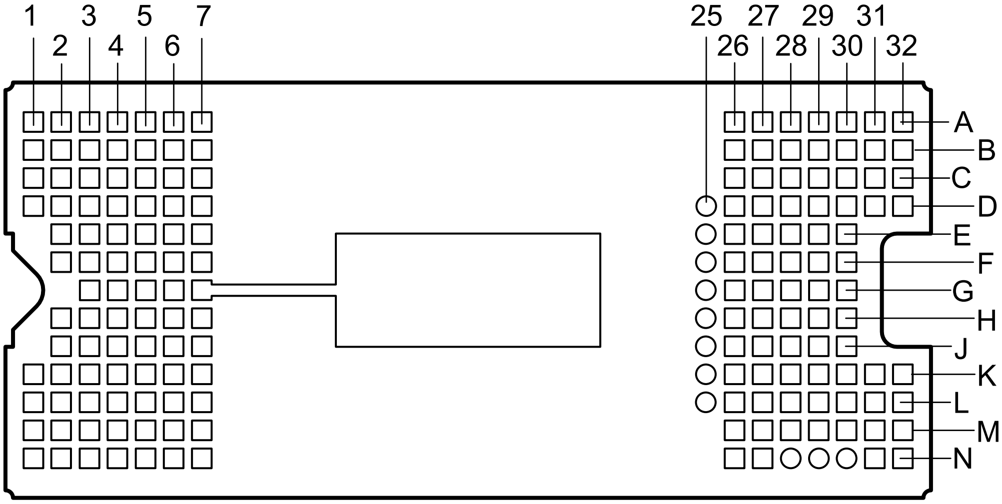


図 4-1. FQY Package 166-Pin LGA (Bottom View)

> 注意
>
> The layout and operation of signals identified in the Pin Functions table must be properly managed to make sure there is reliable operation of the 0.47” 4K UHD S321 DMD. Refer to the Layout Guidelines for the DMD and Controller before designing the board.

4.1 Pin Functions

PIN(2)		TYPE(1)	DESCRIPTION	TERMINATION	TRACE LENGTH (mm)
NAME	PAD ID				
D_AP(0)	A2	I	High-speed Differential Data Pair lane A0	Differential 100Ω	3.75497
D_AN(0)	B2	I	High-speed Differential Data Pair lane A0	Differential 100Ω	3.75482
D_AP(1)	A6	I	High-speed Differential Data Pair lane A1	Differential 100Ω	4.62509
D_AN(1)	B6	I	High-speed Differential Data Pair lane A1	Differential 100Ω	4.625
D_AP(2)	C1	I	High-speed Differential Data Pair lane A2	Differential 100Ω	3.59503
D_AN(2)	C2	I	High-speed Differential Data Pair lane A2	Differential 100Ω	3.59513
D_AP(3)	C6	I	High-speed Differential Data Pair lane A3	Differential 100Ω	5.12758
D_AN(3)	C7	I	High-speed Differential Data Pair lane A3	Differential 100Ω	5.12745
D_AP(4)	G3	I	High-speed Differential Data Pair lane A4	Differential 100Ω	1.60057
D_AN(4)	G4	I	High-speed Differential Data Pair lane A4	Differential 100Ω	1.6004
D_AP(5)	F7	I	High-speed Differential Data Pair lane A5	Differential 100Ω	3.64067
D_AN(5)	F6	I	High-speed Differential Data Pair lane A5	Differential 100Ω	3.64091
D_AP(6)	F4	I	High-speed Differential Data Pair lane A6	Differential 100Ω	1.58206
D_AN(6)	F5	I	High-speed Differential Data Pair lane A6	Differential 100Ω	1.58187
D_AP(7)	H6	I	High-speed Differential Data Pair lane A7	Differential 100Ω	2.70067
D_AN(7)	G6	I	High-speed Differential Data Pair lane A7	Differential 100Ω	2.70086
DCLK_AP	E5	I	High-speed Differential Clock A	Differential 100Ω	2.96493
DCLK_AN	D5	I	High-speed Differential Clock A	Differential 100Ω	2.9653
D_BP(0)	B30	I	High-speed Differential Data Pair lane B0	Differential 100Ω	3.57087

PIN(2)		TYPE(1)	DESCRIPTION	TERMINATION	TRACE LENGTH (mm)
NAME	PAD ID				
D_BN(0)	A30	I	High-speed Differential Data Pair lane B0	Differential 100Ω	3.57064
D_BP(1)	C32	I	High-speed Differential Data Pair lane B1	Differential 100Ω	4.2546
D_BN(1)	B32	I	High-speed Differential Data Pair lane B1	Differential 100Ω	4.25425
D_BP(2)	A28	I	High-speed Differential Data Pair lane B2	Differential 100Ω	4.97968
D_BN(2)	B28	I	High-speed Differential Data Pair lane B2	Differential 100Ω	4.97953
D_BP(3)	C31	I	High-speed Differential Data Pair lane B3	Differential 100Ω	3.12736
D_BN(3)	C30	I	High-speed Differential Data Pair lane B3	Differential 100Ω	3.12743
D_BP(4)	C27	I	High-speed Differential Data Pair lane B4	Differential 100Ω	5.44353
D_BN(4)	B27	I	High-speed Differential Data Pair lane B4	Differential 100Ω	5.4433
D_BP(5)	D28	I	High-speed Differential Data Pair lane B5	Differential 100Ω	3.32124
D_BN(5)	D27	I	High-speed Differential Data Pair lane B5	Differential 100Ω	3.32115
D_BP(6)	F30	I	High-speed Differential Data Pair lane B6	Differential 100Ω	2.99334
D_BN(6)	E30	I	High-speed Differential Data Pair lane B6	Differential 100Ω	2.99374
D_BP(7)	G27	I	High-speed Differential Data Pair lane B7	Differential 100Ω	3.14865
D_BN(7)	G28	I	High-speed Differential Data Pair lane B7	Differential 100Ω	3.14902
DCLK_BP	D29	I	High-speed Differential Clock B	Differential 100Ω	5.03976
DCLK_BN	D30	I	High-speed Differential Clock B	Differential 100Ω	5.0395
D_CP(0)	J4	I	High-speed Differential Data Pair lane C0	Differential 100Ω	2.06577
D_CN(0)	H4	I	High-speed Differential Data Pair lane C0	Differential 100Ω	2.06568
D_CP(1)	J7	I	High-speed Differential Data Pair lane C1	Differential 100Ω	4.87119
D_CN(1)	J6	I	High-speed Differential Data Pair lane C1	Differential 100Ω	4.87131
D_CP(2)	K5	I	High-speed Differential Data Pair lane C2	Differential 100Ω	4.69951
D_CN(2)	J5	I	High-speed Differential Data Pair lane C2	Differential 100Ω	4.69926
D_CP(3)	L4	I	High-speed Differential Data Pair lane C3	Differential 100Ω	3.27735
D_CN(3)	L5	I	High-speed Differential Data Pair lane C3	Differential 100Ω	3.27722
D_CP(4)	L2	I	High-speed Differential Data Pair lane C4	Differential 100Ω	4.65167
D_CN(4)	M2	I	High-speed Differential Data Pair lane C4	Differential 100Ω	4.6513
D_CP(5)	M3	I	High-speed Differential Data Pair lane C5	Differential 100Ω	5.70359
D_CN(5)	N3	I	High-speed Differential Data Pair lane C5	Differential 100Ω	5.70352
D_CP(6)	M5	I	High-speed Differential Data Pair lane C6	Differential 100Ω	2.57704
D_CN(6)	M6	I	High-speed Differential Data Pair lane C6	Differential 100Ω	2.57727
D_CP(7)	N7	I	High-speed Differential Data Pair lane C7	Differential 100Ω	3.77278
D_CN(7)	M7	I	High-speed Differential Data Pair lane C7	Differential 100Ω	3.77317
DCLK_CP	K2	I	High-speed Differential Clock C	Differential 100Ω	2.3747
DCLK_CN	J2	I	High-speed Differential Clock C	Differential 100Ω	2.37429
D_DP(0)	G29	I	High-speed Differential Data Pair lane D0	Differential 100Ω	3.67925
D_DN(0)	F29	I	High-speed Differential Data Pair lane D0	Differential 100Ω	3.6794
D_DP(1)	F27	I	High-speed Differential Data Pair lane D1	Differential 100Ω	4.73751
D_DN(1)	E27	I	High-speed Differential Data Pair lane D1	Differential 100Ω	4.73796
D_DP(2)	K30	I	High-speed Differential Data Pair lane D2	Differential 100Ω	2.76933
D_DN(2)	K29	I	High-speed Differential Data Pair lane D2	Differential 100Ω	2.76936
D_DP(3)	J27	I	High-speed Differential Data Pair lane D3	Differential 100Ω	3.07794
D_DN(3)	K27	I	High-speed Differential Data Pair lane D3	Differential 100Ω	3.07804
D_DP(4)	M30	I	High-speed Differential Data Pair lane D4	Differential 100Ω	3.60026

PIN[2]		TYPE[1]	DESCRIPTION	TERMINATION	TRACE LENGTH (mm)
NAME	PAD ID				
D_DN(4)	L30	I	High-speed Differential Data Pair lane D4	Differential 100Ω	3.60028
D_DP(5)	M27	I	High-speed Differential Data Pair lane D5	Differential 100Ω	3.24012
D_DN(5)	L27	I	High-speed Differential Data Pair lane D5	Differential 100Ω	3.24002
D_DP(6)	N26	I	High-speed Differential Data Pair lane D6	Differential 100Ω	4.69564
D_DN(6)	M26	I	High-speed Differential Data Pair lane D6	Differential 100Ω	4.69594
D_DP(7)	M31	I	High-speed Differential Data Pair lane D7	Differential 100Ω	3.97347
D_DN(7)	M32	I	High-speed Differential Data Pair lane D7	Differential 100Ω	3.97352
DCLK_DP	H29	I	High-speed Differential Clock D	Differential 100Ω	1.7593
DCLK_DN	J29	I	High-speed Differential Clock D	Differential 100Ω	1.75933
LS_WDATA	D4	I	LVDS Data		2.29224
LS_CLK	C4	I	LVDS CLK		1.73951
LS_RDATA_A	C5	O	LVCMOS Output		2.72344
LS_RDATA_B	D3	O	LVCMOS Output		2.22814
LS_RDATA_C	E3	O	LVCMOS Output		3.22863
LS_RDATA_D	F3	O	LVCMOS Output		4.90151
DMD_DEN_ARSTZ	D2	I	ARSTZ		1.80911
TEMP_N	N1	I	Temp Diode N		1.84006
TEMP_P	M1	I	Temp Diode P		2.62822
VDD	A3, A4, C26, D1, D6, D7, D26, E2, E6, E7, E26, F2, G30, H28, H30, J26, J30, K1, K6, K26, K31, K32, L1, L31, L32, N2	P	Digital Core Supply Voltage		14.26561
VDDI	A5, B5, F26, G26, H26, H27, K7, L7	P	SubLVDS supply voltage		3.72532
VRESET	B3, B26	P	Supply voltage for negative bias of micromirror reset signal		25.57603
VBIAS	A27, B4	P	Supply voltage for positive bias of micromirror reset signal		24.70004
VOFFSET	A26, C3, L6, L26	P	Supply voltage for HVCMOS logic, stepped up logic level		8.73417

PIN[2]		TYPE[1]	DESCRIPTION	TERMINATION	TRACE LENGTH (mm)
NAME	PAD ID				
VSS	A1, A7, A29, A31, A32, B1, B7, B29, B31, C28, C29, D31, D32, E4, E28, E29, F28, G5, G7, H2, H3, H5, H7, J3, J28, K3, K4, K28, L3, L28, L29, M4, M28, M29, N4, N5, N6, N27, N31, N32	G	Ground		24.6246
N/C	N28, N29, N30, L25, K25, J25, H25, G25, F25, E25, D25	NC	No Connect Pin		None

(1) I=Input, O=Output, P=Power, G=Ground, NC=No Connect
(2) Only 163 pins are electrically connected for functional use

5 Specifications

5.1 Absolute Maximum Ratings

Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

		MIN	MAX	UNIT
SUPPLY VOLTAGE				
V_{DD}	Supply voltage for LVCMOS core logic and LPSDR low speed interface (1)	-0.5	2.3	V
V_{DDI}	Supply voltage for SubLVDS receivers(1)	-0.5	2.3	V
V_{OFFSET}	Supply voltage for HVCMOS and micromirror electrode(1) (2)	-0.5	11	V
V_{BIAS}	Supply voltage for micromirror electrode(1)	-0.5	19	V
V_{RESET}	Supply voltage for micromirror electrode(1)	-15	0.5	V
$\|V_{DDI} - V_{DD}\|$	Supply voltage delta, absolute value(3)		0.3	V
$\|V_{BIAS} - V_{OFFSET}\|$	Supply voltage delta, absolute value(4)		11	V
$\|V_{BIAS} - V_{RESET}\|$	Supply voltage delta, absolute value(5)		34	V
INPUT VOLTAGE				
	Input voltage for other inputs -- LSIF and LVCMOS(1)	-0.5	V_{DD} + 0.5	V
	Input voltage for other inputs -- SubLVDS(1) (6)	-0.5	V_{DDI} + 0.5	V
SUBLVDS INTERFACE				
$\|V_{ID}\|$	SubLVDS input differential voltage (absolute value)(1) (6)		810	mV
I_{ID}	SubLVDS input differential current		10	mA
CLOCK FREQUENCY				
f_{clock}	Clock frequency for low speed interface LS_CLK	100	130	MHz
TEMPERATURE DIODE				
I_{TEMP_DIODE}	Max current source into temperature diode		120	µA
ENVIRONMENTAL				
T_{WINDOW} and T_{ARRAY}	Temperature, operating(7)	0	90	°C
	Temperature, non-operating(7)	-40	90	°C
$\|T_{DELTA}\|$	Absolute temperature delta between any point on the window edge and theceramic test point TP1(8)		30	°C
T_{DP}	Dew point temperature, operating and non–operating (noncondensing)		81	°C

(1) All voltage values are with respect to the ground terminals (V_{SS}). The following required power supplies must be connected for proper DMD operation: V_{DD}, V_{DDI}, V_{OFFSET}, V_{BIAS}, and V_{RESET}. All V_{SS} connections are also required.
(2) V_{OFFSET} supply transients must fall within specified voltages.
(3) Exceeding the recommended allowable absolute voltage difference between V_{DDI} and V_{DD} may result in excessive current draw and permanent damage to the device.
(4) Exceeding the recommended allowable absolute voltage difference between V_{BIAS} and V_{OFFSET} may result in excessive current draw and permanent damage to the device.
(5) Exceeding the recommended allowable absolute voltage difference between V_{BIAS} and V_{RESET} may result in excessive current draw and permanent damage to the device.
(6) This maximum input voltage rating applies when each input of a differential pair is at the same voltage potential. Sub-LVDS differential inputs must not exceed the specified limit or damage may result to the internal termination resistors.
(7) The highest temperature of the active array (as calculated using the Micromirror Array Temperature Calculation) or of any point along the window edge. The locations of thermal test points TP2, TP3, TP4, and TP5 are intended to measure the highest window edge temperature. If a particular application causes another point on the window edge to be at a higher temperature, that point should be used.
(8) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge. The window test points TP2, TP3, TP4, and TP5 are intended to result in the worst case delta. If a particular application causes another point on the window edge to result in a larger delta temperature, that point should be used.

5.2 Storage Conditions

Applicable for the DMD as a component or non-operating in a system.

		MIN	MAX	UNIT
T_{DMD}	DMD temperature	-40	85	°C
$T_{DP\text{-}AVG}$	Average dew point temperature, non-condensing(1)		24	°C
$T_{DP\text{-}ELR}$	Elevated dew point temperature range, non-condensing(2)	28	36	°C
CT_{ELR}	Cumulative time in elevated dew pointt temperature range		6	months

(1) The average temperature over time (including storage and operating temperatures) that the device is not in the elevated dew point temperature range.
(2) Exposure to dew point temperatures in the elevated range during storage and operation should be limited to less than a total cumulative time of CT_{ELR}.

5.3 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic Discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged device model (CDM), per JEDEC specification ANSI/ESDA/JEDEC JS-002(2)	±250	V

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

5.4 Recommended Operating Conditions

Over operating free-air temperature range and supply voltages (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by the Recommended Operating Conditions. No level of performance is implied when operating the device above or below the Recommended Operating Conditions limits.

		MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE RANGE					
VDD	Supply voltage for LVCMOS core logic(1) (2) Supply voltage for LPSDR low-speed interface(1) (2)	1.71	1.8	1.95	V
VDDI	Supply voltage for SubLVDS receivers(1) (2)	1.71	1.8	1.95	V
VOFFSET	Supply voltage for HVCMOS and micromirror electrode(1) (2) (3)	9.5	10	10.5	V
VBIAS	Supply voltage for mirror electrode(1) (2)	17.5	18	18.5	V
VRESET	Supply voltage for micromirror electrode(1) (2)	–14.5	–14	–13.5	V
|VDDI- VDD|	Supply voltage delta (absolute value)(1) (2) (4)			0.3	V
|VBIAS-VOFFSET|	Supply voltage delta (absolute value)(1) (2) (5)			10.5	V
|VBIAS- VRESET|	Supply voltage delta (absolute value)(1) (2) (6)			33	V
CLOCK FREQUENCY					
f_{clock}	Clock frequency for low speed interface LS_CLK(7)	108		120	MHz
	Clock frequency for high-speed interface DCLK (8)			720	MHz
DCD_{IN}	Duty cycle distortion	44		56	%
SUBLVDS INTERFACE					
$\|V_{ID}\|$	LVDS differential input voltage magnitude(8)	150	250	350	mV
V_{CM}	Common mode voltage(8)	700	900	1100	mV
$V_{SUBLVDS}$	SubLVDS voltage(8)	525		1275	mV
Z_{LINE}	Line differential impedance (PWB/trace)	90	100	110	Ω
Z_{IN}	Internal differential termination resistance(10)	80	100	120	Ω
	100Ω differential PCB trace	6.35		152.4	mm
ENVIRONMENTAL					
T_{ARRAY}	Array temperature, long-term operation(9) (10) (11) (12)	10		40 to 70	°C
	Array temperature, short-term operation, 500 hr max(10) (13)	0		10	°C
T_{Window}	Window temperature, operational(14)			85	°C
$\|T_{DELTA}\|$	Absolute Temperature difference between any point on the window edge and the ceramic test point TP1(16)			15	°C
$T_{DP\text{-}AVG}$	Average dew point temperature, (non-condensing)(15)			24	°C
$T_{DP\text{-}ELR}$	Elevated dew point temperature range, (non-condensing)(16)		28	36	°C
CT_{ELR}	Cumulative time in elevated dew point temperature range			6	Months
ILLUMINATION					
ILL_{UV}	Illumination, wavelength < 410nm(9)			10	mW/cm^2
ILL_{VIS}	Illumination power at wavelengths ≥ 410nm and ≤ 800nm(17)			20.5	W/cm^2
ILL_{IR}	Illumination, wavelength between > 800nm			10	mW/cm^2
ILL_{BLU}	Illumination power at wavelengths ≥ 410nm and ≤ 475nm(17)			6.5	W/cm^2
ILL_{BLU1}	Illumination power at wavelengths ≥ 410nm and ≤ 445nm(17)			1.2	W/cm^2
ILL_{θ}	Illumination marginal ray angle(18)			55	deg

(1) The following power supplies are all required to operate the DMD: V_{DD}, V_{DDI}, V_{OFFSET}, V_{BIAS}, and V_{RESET}. All V_{SS} connections are required to operate the DMD.
(2) All voltage values are with respect to the V_{SS} ground pins.
(3) V_{OFFSET} supply transients must fall within specified max voltages.
(4) To prevent excess current, the supply voltage delta $|V_{DDI} – V_{DD}|$ must be less than the specified limit.
(5) To prevent excess current, the supply voltage delta $|V_{BIAS} – V_{OFFSET}|$ must be less than the specified limit.

(6) To prevent excess current, the supply voltage delta $|V_{BIAS} – V_{RESET}|$ must be less than the specified limit.
(7) LS_CLK must run as specified to ensure internal DMD timing for reset waveform commands.
(8) Refer to the SubLVDS timing requirements in セクション 5.8.
(9) Simultaneous exposure of the DMD to the maximum Recommended Operating Conditions for temperature and UV illumination will reduce device lifetime.
(10) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point (TP1) and the package thermal resistance using the Micromirror Array Temperature Calculation.
(11) Per Maximum Recommended Array Temperature—Derating Curve, the maximum operational array temperature should be derated based on the micromirror landed duty cycle that the DMD experiences in the end application. Refer to Micromirror Landed-On/Landed-Off Duty Cycle for a definition of micromirror landed duty cycle.
(12) Long-term is defined as the usable life of the device.
(13) Short-term is the total cumulative time over the useful life of the device.
(14) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge. The window test points TP2, TP3, TP4, and TP5 are intended to result in the worst case delta temperature. If a particular application causes another point on the window edge to result in a larger delta temperature, that point should be used.
(15) The average over time (including storage and operating) that the device is not in the ‘elevated dew point temperature range'.
(16) Exposure to dew point temperatures in the elevated range during storage and operation should be limited to less than a total cumulative time of CT_{ELR}.
(17) The maximum allowable optical power incident on the DMD is limited by the maximum optical power density for each wavelength range specified and the micromirror array temperature (T_{ARRAY}).
(18) The maximum marginal ray angle of the incoming illumination light at any point in the micromirror array, including Pond of Micromirrors (POM), should not exceed 55 degrees from the normal to the device array plane. The device window aperture has not necessarily been designed to allow incoming light at higher maximum angles to pass to the micromirrors, and the device performance has not been tested nor qualified at angles exceeding this. Illumination light exceeding this angle outside the micromirror array (including POM) will contribute to thermal limitations described in this document, and may negatively affect lifetime.

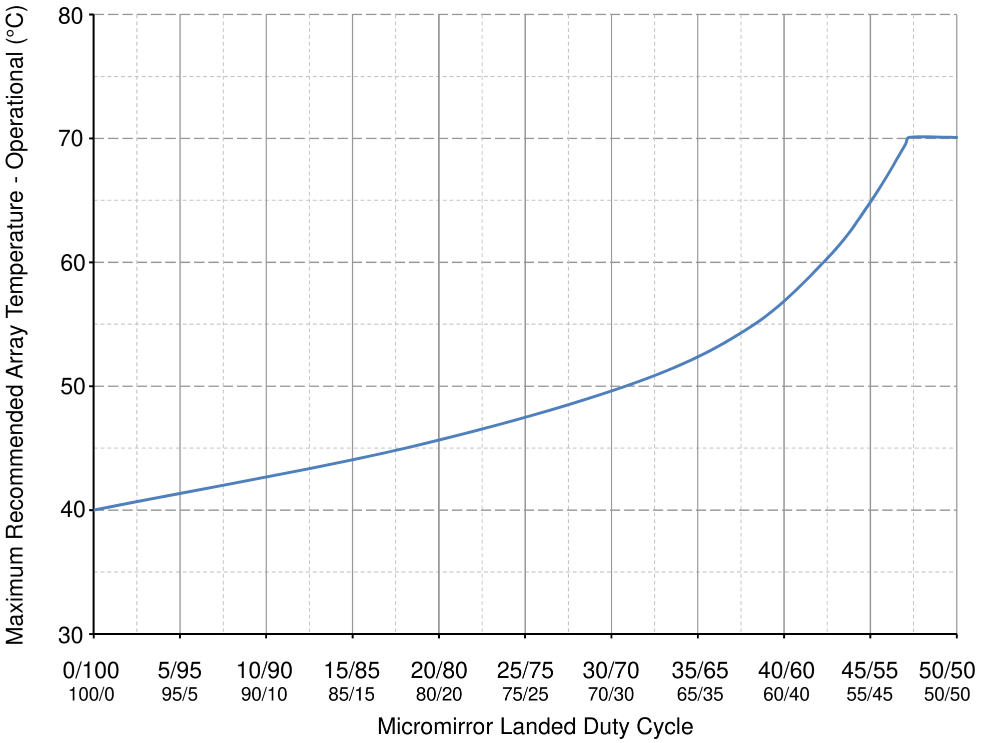


図 5-1. Maximum Recommended Array Temperature—Derating Curve

5.5 Thermal Information

THERMAL METRIC	DLP472TP	UNIT
	FQY	
	163 PIN	
THERMAL INFORMATION		

5.5 Thermal Information (続き)

THERMAL METRIC	DLP472TP	UNIT
	FQY	
	163 PIN	
Thermal Resistance, active area to test point 1 (TP1)(1)	1.2	°C/W

(1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package. The cooling system must be capable of maintaining the DMD within the temperature range specified in the Recommended Operating Conditions. The total heat load on the DMD is largely driven by the incident light absorbed by the active area; although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array. Optical systems should be designed to minimize the light energy falling outside the window clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

5.6 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted) (1)

PARAMETER(7)		TEST CONDITIONS (2)	MIN	TYP	MAX	UNIT
CURRENT						
I_{DD}	Supply current: V_{DD} (3) (4)	Typical			140	mA
I_{DDI}	Supply current: V_{DDI} (3) (4)	Typical			45	mA
I_{OFFSET}	Supply current: V_{OFFSET} (5) (6)	Typical			6	mA
I_{BIAS}	Supply current: V_{BIAS} (5) (6)	Typical			.5	mA
I_{RESET}	Supply current: V_{RESET} (6)	Typical	-1.8			mA
POWER						
P_{DD}	Supply power dissipation: V_{DD} (3) (4)	Typical			252	mW
P_{DDI}	Supply power dissipation: V_{DDI} (3) (4)	Typical			81	mW
P_{OFFSET}	Supply power dissipation: V_{OFFSET} (5) (6)	Typical			60	mW
P_{BIAS}	Supply power dissipation: V_{BIAS} (5) (6)	Typical			9	mW
P_{RESET}	Supply power dissipation: V_{RESET} (6)	Typical			25.2	mW
P_{TOTAL}	Supply power dissipation Total	Typical			427.2	mW
LPSDR INPUT						
V_{IH}	High-level input voltage(8) (9)		0.7 x V_{DD}		V_{DD} + 0.3	x VDD
V_{IL}	Low-level input voltage(8) (9)		–0.3		0.3 x V_{DD}	x VDD
$V_{IH(AC)}$	AC input high voltage(8) (9)		0.8 × V_{DD}		V_{DD} + 0.3	x VDD
$V_{IL(AC)}$	AC input low voltage(8) (9)		–0.3		0.2 × V_{DD}	x VDD
VHyst	Input Hysteresis ($V_{T+} – V_{T–}$)(11)		0.1 × V_{DD}		0.4 × V_{DD}	V
I_{IL}	Low level input current	V_{DD} = 1.95 V, V_I = 0V	-100			nA
I_{IH}	High level input current	V_{DD} = 1.95 V, V_I = 1.95V			135	uA
LPSDR OUTPUT						
V_{OH}	DC output high voltage(10)	I_{OH} = -2 mA	0.8 x V_{DD}			X VDD
V_{OL}	DC output low voltage(10)	I_{OL} = 2 mA			0.2 x V_{DD}	X VDD
CAPACITANCE						
C_{IN}	Input capacitance LVCMOS	F = 1 MHz			10	pF
C_{IN}	Input capacitance SubLVDS	F = 1 MHz			20	pF
C_{OUT}	Output capacitance	F = 1 MHz			10	pF

(1) Device electrical characteristics are over セクション 5.4 unless otherwise noted.
(2) All voltage values are with respect to the ground pins (V_{SS}).
(3) To prevent excess current, the supply voltage delta | V_{DDI} – V_{DD} | must be less than the specified limit.
(4) Supply power dissipation based on non–compressed commands and data.

(5) To prevent excess current, the supply voltage delta | V_{BIAS} – V_{OFFSET} | must be less than the specified limit.
(6) Supply power dissipation based on 3 global resets in 200 µs.
(7) All power supply connections are required to operate the DMD: V_{DD}, V_{DDI}, V_{OFFSET}, V_{BIAS}, V_{RESET}. All V_{SS} connections are also required.
(8) LPSDR specifications are for pins LS_CLK and LS_WDATA.
(9) Low-speed interface is LPSDR and adheres to the Electrical Characteristics and AC/DC Operating Conditions table in JEDEC Standard No. 209B, Low-Power Double Data Rate (LPDDR) JESD209B.
(10) LPSDR output specification is for pins LS_RDATA_A, LS_RDATA_B, LS_RDATA_C, LS_RDATA_D.
(11) Refer to Figure 6-10

5.7 Switching Characteristics

Over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PD}	Output propagation, clock to Q, rising edge of LS_CLK input to LS_RDATA output.	C_L = 45 pF			15	ns
	Slew rate, LS_RDATA		0.3			V/ns
	Output duty cycle distortion, LS_RDATA		40		60	%

(1) Device electrical characteristics are over セクション 5.4 unless otherwise noted.

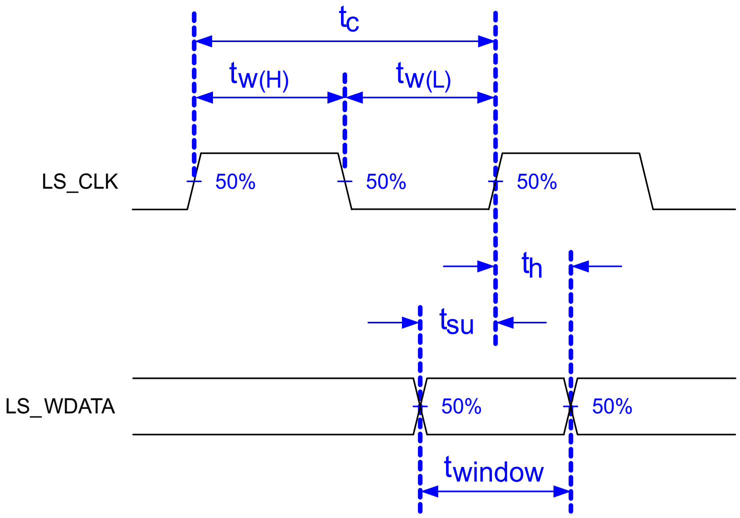
5.8 Timing Requirements

Over operating free-air temperature range (unless otherwise noted) (1)

			MIN	NOM	MAX	UNIT
LPSDR						
t_f	Fall slew rate (2)	(80% to 20%) × V_{DD} (5)	0.25			V/ns
t_c	Cycle time LS_CLK(5)	50% to 50% reference points(5)	7.7	8.3		ns
t_r	Rise slew rate (1)	(30% to 80%) × V_{DD} (6)	1		3	V/ns
t_f	Fall slew rate (1)	(70% to 20%) x V_{DD} (6)	1		3	V/ns
t_r	Rise slew rate (2)	(20% to 80%) × V_{DD} (6)	0.25			V/ns
$t_{W(H)}$	Pulse duration LS_CLK high	50% to 50% reference points(5)	3.1			ns
$t_{W(L)}$	Pulse duration LS_CLK low	50% to 50% reference points(5)	3.1			ns
t_{WINDOW}	Window time(1) (3)	Setup time + Hold time(5)	3			ns
$t_{DERATING}$	Window time derating(1) (3)	For each 0.25 V/ns reduction in slew rate below 1 V/ns(8)		0.35		ns
t_{su}	Setup time	LS_WDATA valid before LS_CLK(5)			1.5	ns
t_h	Hold time	LS_WDATA valid after LS_CLK(5)			1.5	ns
SubLVDS						
t_r	Rise slew rate	20% to 80% reference points(7)	0.7	1		V/ns
t_f	Fall slew rate	80% to 20% reference points(7)	0.7	1		V/ns
t_c	Cycle time D_CLK(9)	50% to 50% reference points(9)	1.35	1.39		ns
$t_{W(H)}$	Pulse duration DCLK high	50% to 50% reference points(9)	0.7			ns
$t_{W(L)}$	Pulse duration DCLK low	50% to 50% reference points(9)	0.7			ns
t_{su}	Setup time	DATA valid before D_CLK(9)			0.17	ns
t_h	Hold time	DATA valid after D_CLK(9)			0.17	ns
t_{WINDOW}	Window time	Setup time + Hold time(9) (10)			0.25	ns
t_{POWER}	Power-up receiver(4)				200	ns

(1) Specification is for LS_CLK and LS_WDATA pins. Refer to LPSDR input rise and fall slew rate in Figure 6-3
(2) Specification is for DMD_DEN_ARSTZ pin. Refer to LPSDR input rise and fall slew rate in Figure 6-3
(3) Window time derating example: 0.5-V/ns slew rate increases the window time by 0.7 ns, from 3 to 3.7 ns.
(4) Specification is for SubLVDS receiver time only and does not take into account commanding and latency after commanding.
(5) See Figure 6-2 .
(6) See Figure 6-3 .
(7) See Figure 6-4.
(8) See Figure 6-5.

(9) See Figure 6-6.
(10) See Figure 6-7.



The low-speed interface is LPSDR and adheres to the Electrical Characteristics and AC/DC Operating Conditions table in JEDEC Standard No. 209B, *Low Power Double Data Rate (LPDDR)* JESD209B.

図 5-2. LPSDR Switching Parameters

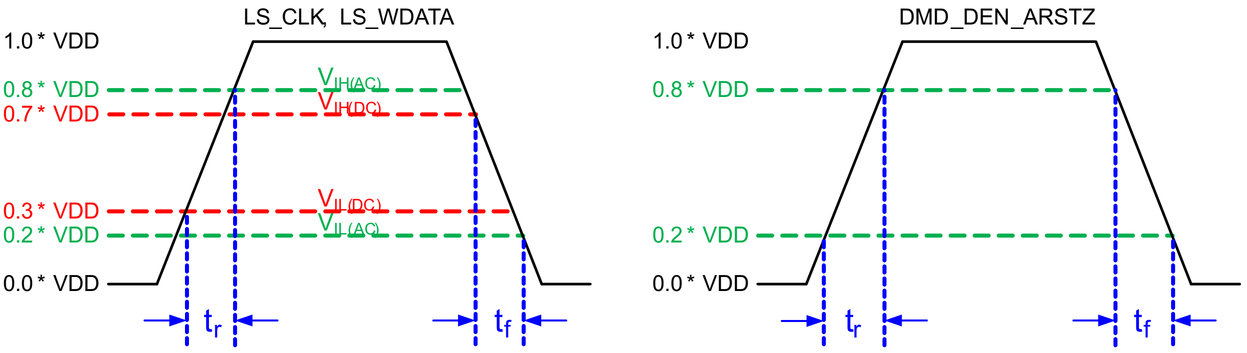


図 5-3. LPSDR Input Rise and Fall Slew Rate

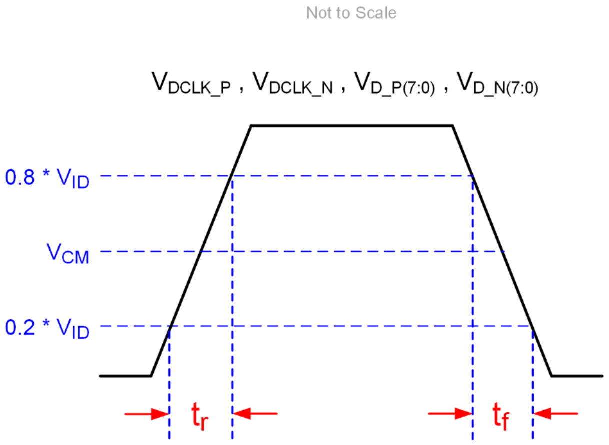


図 5-4. SubLVDS Input Rise and Fall Slew Rate

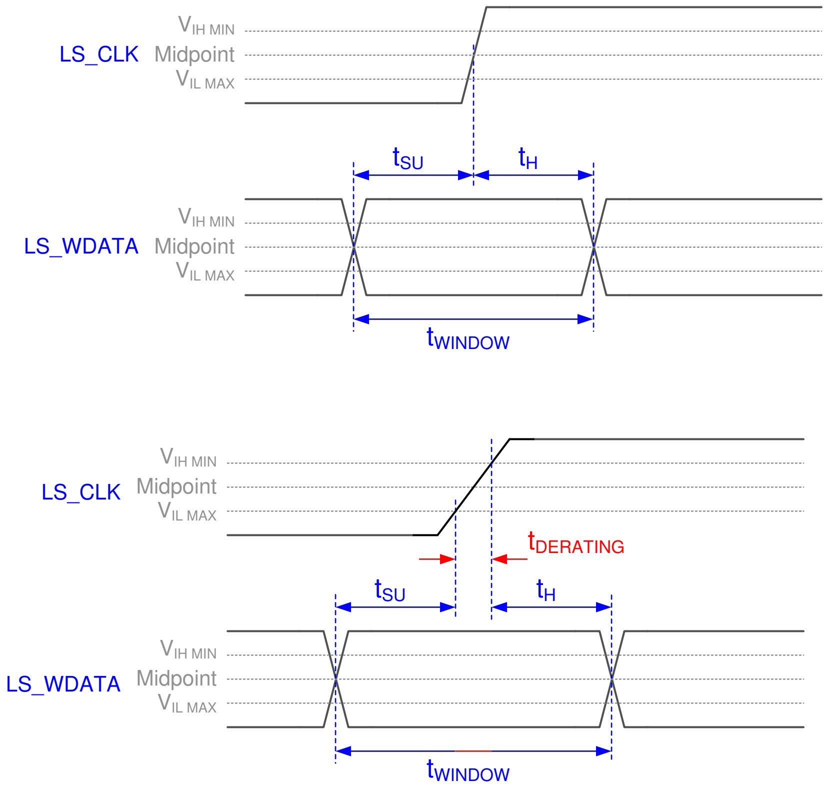


図 5-5. Window Time Derating Concept

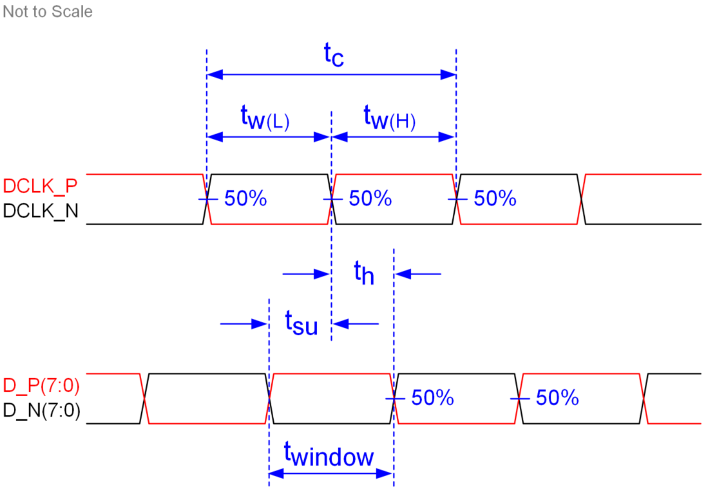
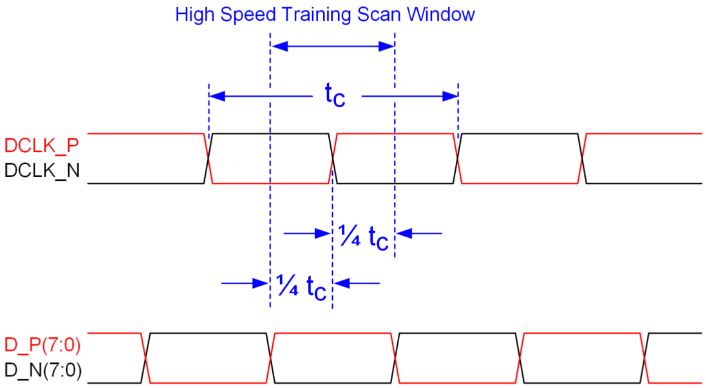


図 5-6. SubLVDS Switching Parameters



Note: Refer to セクション 5.8 for details.

図 5-7. High-Speed Training Scan Window

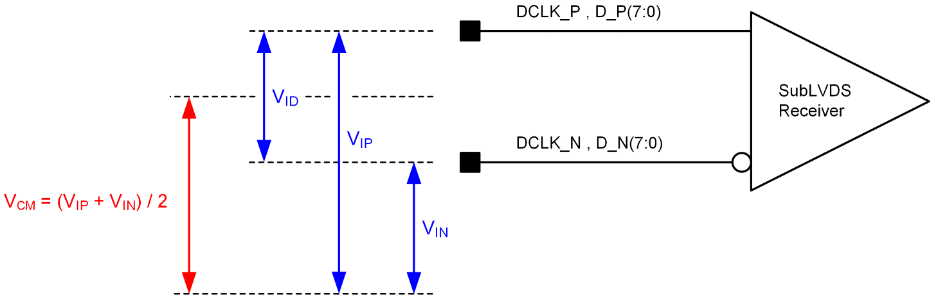


図 5-8. SubLVDS Voltage Parameters

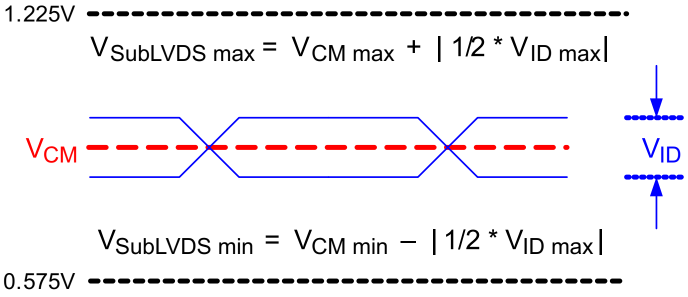


図 5-9. SubLVDS Waveform Parameters

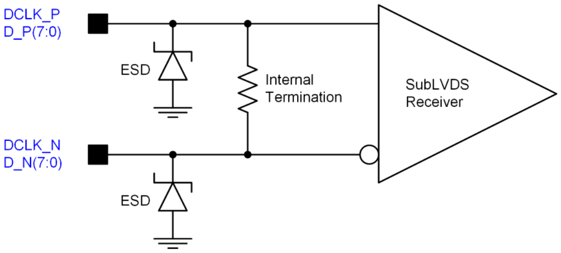


図 5-10. SubLVDS Equivalent Input Circuit

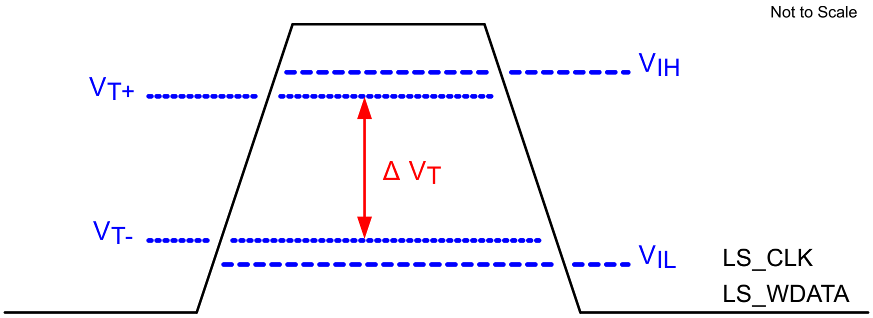


図 5-11. LPSDR Input Hysteresis

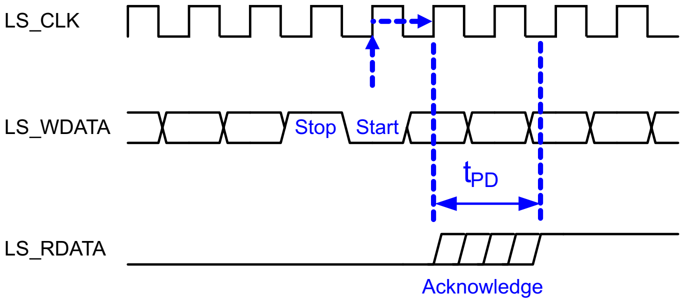
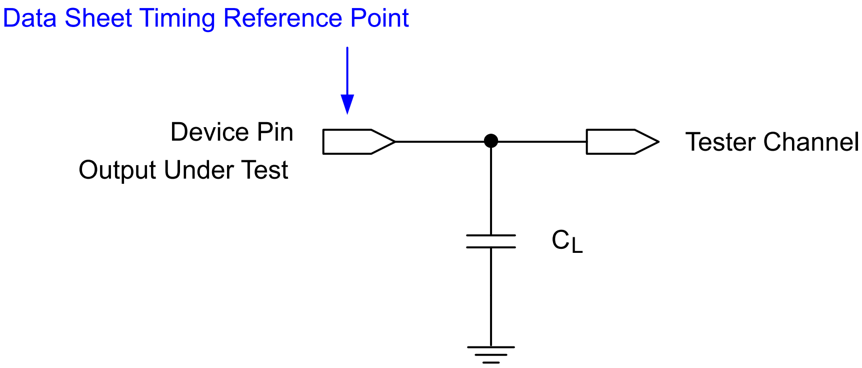


図 5-12. LPSDR Read Out



See セクション 5.6 for more information.

図 5-13. Test Load Circuit for Output Propagation Measurement

5.9 System Mounting Interface Loads

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Thermal Interface Area	Maximum load evenly distributed within each area (1)			73.5	N
Electrical Interface Area	Maximum load evenly distributed within each area (1)			150	

(1) See Figure 6-14.

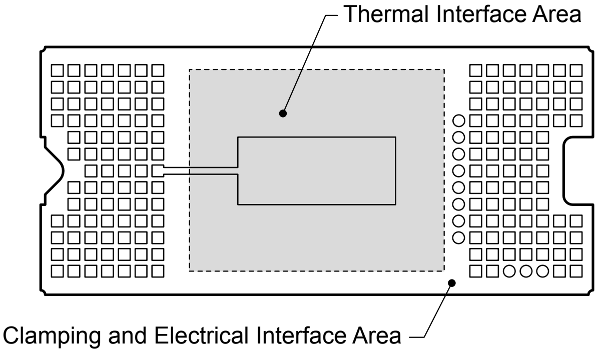


図 5-14. System Mounting Interface Loads

5.10 Micromirror Array Physical Characteristics

PARAMETER DESCRIPTION		VALUE	UNIT
Number of active columns (1) (2)	M	1920	micromirrors
Number of active rows (1) (2)	N	1080	micromirrors
Micromirror (pixel) pitch (1)	P	5.4	µm
Micromirror active array width (1)	Micromirror pitch × number of active columns	10.368	mm
Micromirror active array height (1)	Micromirror pitch × number of active columns	5.832	mm
Micromirror active border (3)	Pond of micromirror (POM)	20	micromirrors/side

(1) See Figure 6-15

(2) The fast switching speed of the DMD micromirrors combined with advanced DLP image processing algorithms enables each micromirror to display four distinct pixels on the screen during every frame, resulting in a full 3840 x 2160 pixel image being displayed.

(3) The structure and qualities of the bordere around the active array includes a band of partially functional micromirrors referred to as the i{Pond of Micromirrors} (POM). These micromirrors are structurally and/or electrically prevented from tilting toward the bright or ON state but still require an electrical bias to tilt toward the OFF state.

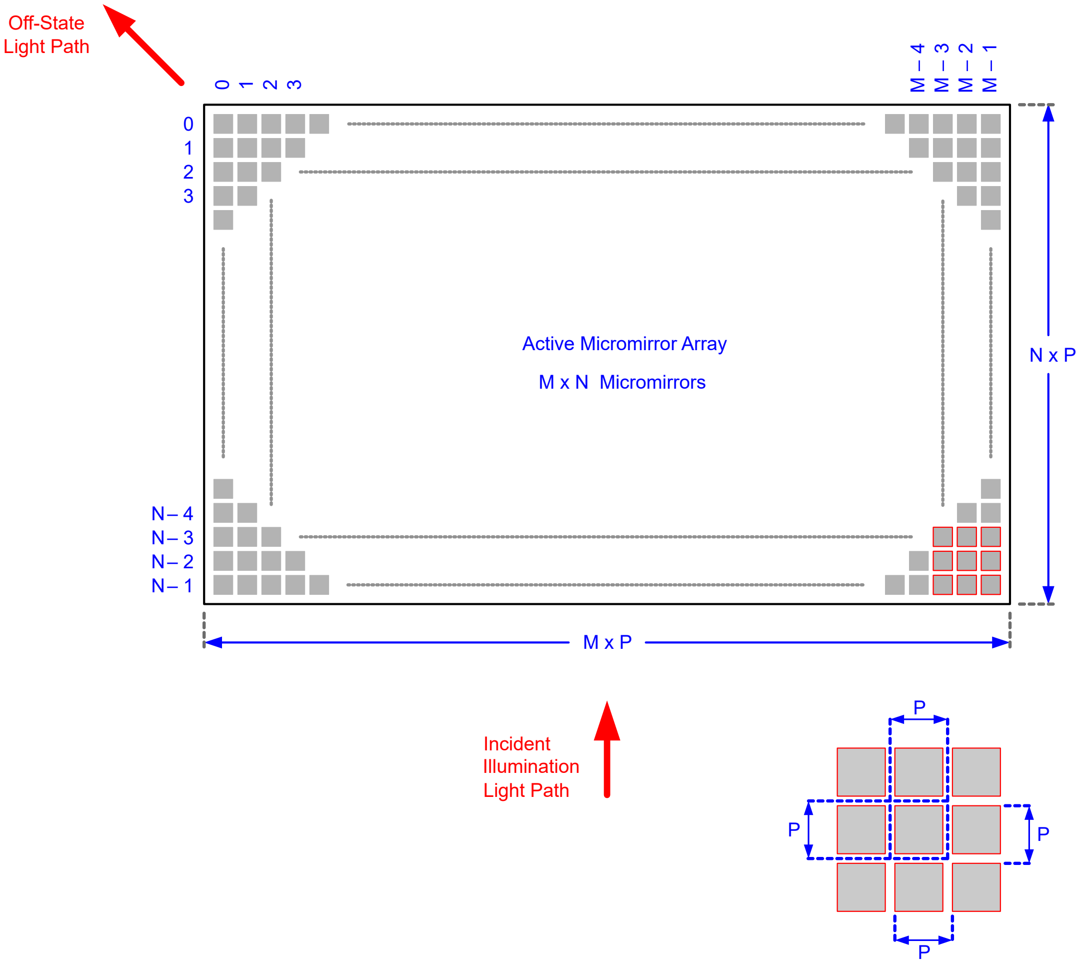


図 5-15. Micromirror Array Physical Characteristics

5.11 Micromirror Array Optical Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Micromirror tilt angle		Landed state (1)		17		°
Micromirror tilt angle tolerance (2) (3) (4) (5)			-1.4		1.4	°
Micromirror tilt direction (6) (7)		Landed ON state		270		°
Micromirror tilt direction (6) (7)		Landed OFF state		180		°
Micromirror crossover time (8)		Typical Performance		1	3	μs
Micromirror switching time (9)		Typical Performance	6			
Image Performance (10)	Bright pixel(s) in active area (11)	Gray 10 Screen (12)			0	micromirrors
	Bright pixel(s) in the POM (13)	Gray 10 Screen (12)			1	
	Dark pixel(s) in the active area (14)	White Screen			4	
	Adjacent pixel(s) (15)	Any Screen			0	
	Unstable pixel(s) in active area (16)	Any Screen			0	

(1) Measured relative to the plane formed by the overall micromirror array.
(2) Additional variation exists between the micromirror array and the package datums.
(3) Represents the landed tilt angle variation relative to the nominal landed tilt angle.
(4) Represents the variation that can occur between any two individual micromirrors, located on the same device or located on different devices.

(5) For some applications, it is critical to account for the micromirror tilt angle variation in the overall system optical design. With some system optical designs, the micromirror tilt angle variation within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some system optical designs, the micromirror tilt angle variation between devices may result in colorimetry variations, system efficiency variations or system contrast variations.

(6) When the micromirror array is landed (not parked), the tilt direction of each individual micromirror is dictated by the binary contents of the CMOS memory cell associated with each individual micromirror. A binary value of 1 results in a micromirror landing in the ON State direction. A binary value of 0 results in a micromirror landing in the OFF State direction. See the Micromirror Landed Orientation and Tilt Figure 6-16.

(7) Micromirror tilt direction is measured as in a typical polar coordinate system: Measuring counter-clockwise from a 0° degree reference which is aligned with the +X Cartesian axis.

(8) The time required for a micromirror to nominally transition from one landed state to the opposite landed state.

(9) The minimum time between successive transitions of a micromirror.

(10) Conditions of Acceptance: All DMD image quality returns will be evaluated using the following projected image test conditions:
Test set degamma shall be linear
Test set brightness and contrast shall be set to nominal
The diagonal size of the projected image shall be a minimum of 20 inches
The projections screen shall be 1X gain
The projected image shall be inspected from a 38 inch minimum viewing distance
The image shall be in focus during all image quality tests

(11) Bright pixel definition: A single pixel or mirror that is stuck in the ON position and is visibly brighter than the surrounding pixels

(12) Gray 10 screen definition: All areas of the screen are colored with the following settings:
Red = 10/255
Green = 10/255
Blue = 10/255

(13) POM definition: Rectangular border of off-state mirrors surrounding the active area

(14) Dark pixel definition: A single pixel or mirror that is stuck in the OFF position and is visibly darker than the surrounding pixels

(15) Adjacent pixel definition: Two or more stuck pixels sharing a common border or common point, also referred to as a cluster

(16) Unstable pixel definition: A single pixel or mirror that does not operate in sequence with parameters loaded into memory. The unstable pixel appears to be flickering asynchronously with the image

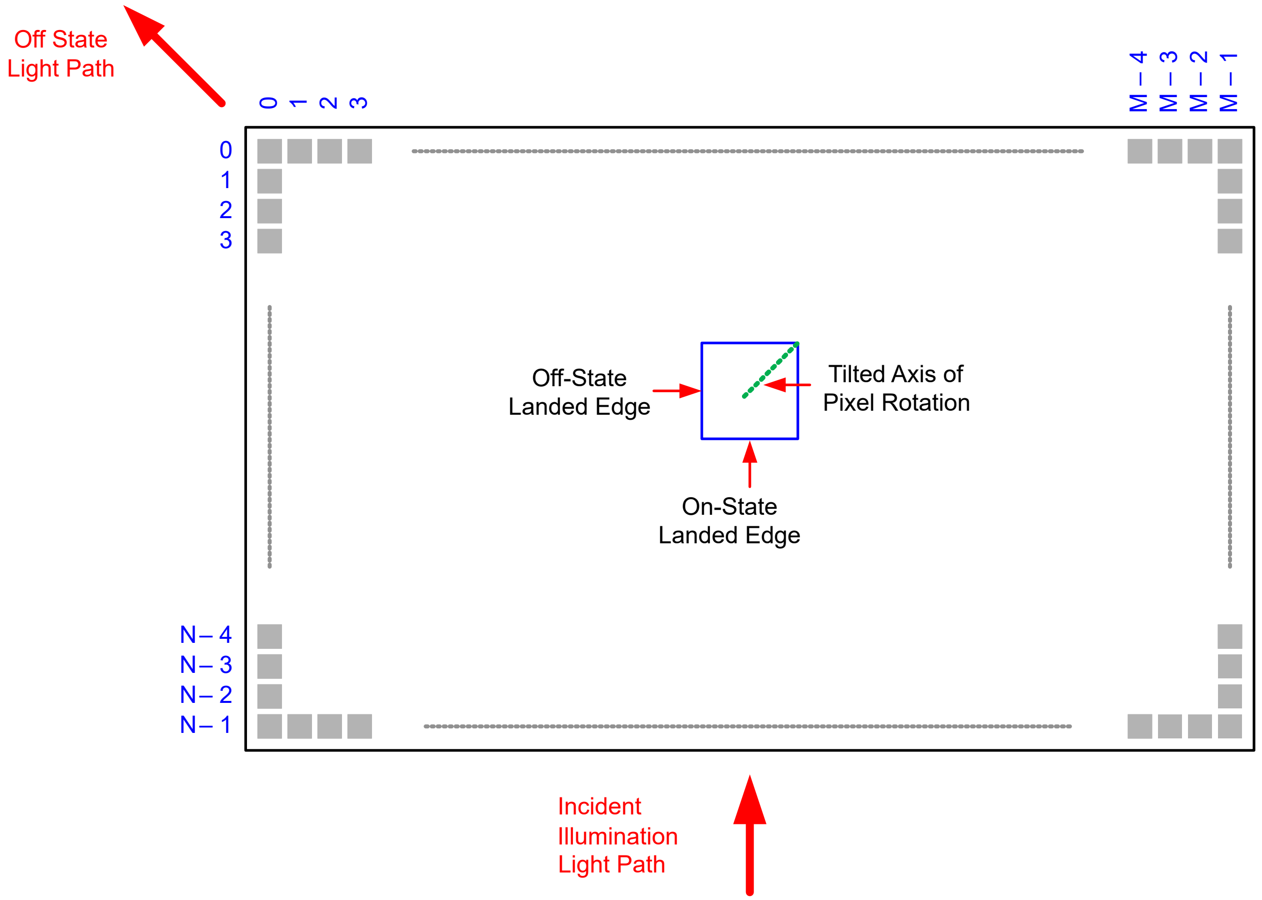


図 5-16. Micromirror Landed Orientation and Tilt

5.12 Window Characteristics

DESCRIPTION(1)		MIN	TYP	MAX
Window material			Corning Eagle XG	
Window refractive index	At wavelength 546.1 nm		1.5119	
Window aperture (2)			See (2).	
Illumination overfill(3)			See (3).	
Window transmittance, single-pass through both surfaces and glass	Minimum within the wavelength range 420 nm to 680 nm. Applies to all angles 0° to 30° AOI. (4)	97%		
	Average over the wavelength range 420 nm to 680 nm. Applies to all angles 30° to 45° AOI. (4)	97%		

(1) See Section 7.5
(2) See the package mechanical characteristics for details regarding the size and location of the window aperture.
(3) The active area of the DMD device is surrounded by an aperture on the inside of the window surface that masks structures of the DMD device assembly from normal view. The aperture is sized to anticipate several optical conditions. Overfill light illuminating the area outside the active array can scatter and create adverse effects to the performance of an end application using the DMD. The illumination optical system should be designed to limit light flux incident outside the active array to less than 10% of the average flux level in the active area. Depending on the particular system"s optical architecture and assembly tolerances, the amount of overfill light on the outside of the active array may cause system performance degradation.
(4) Angle of incidence (AOI) is the angle between an incident ray and the normal to a reflecting or refracting surface.

5.13 Chipset Component Usage Specification

Reliable function and operation of the DLP472TP DMD requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology consists of the TI technology and devices used for operating or controlling a DLP DMD.

注

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously.

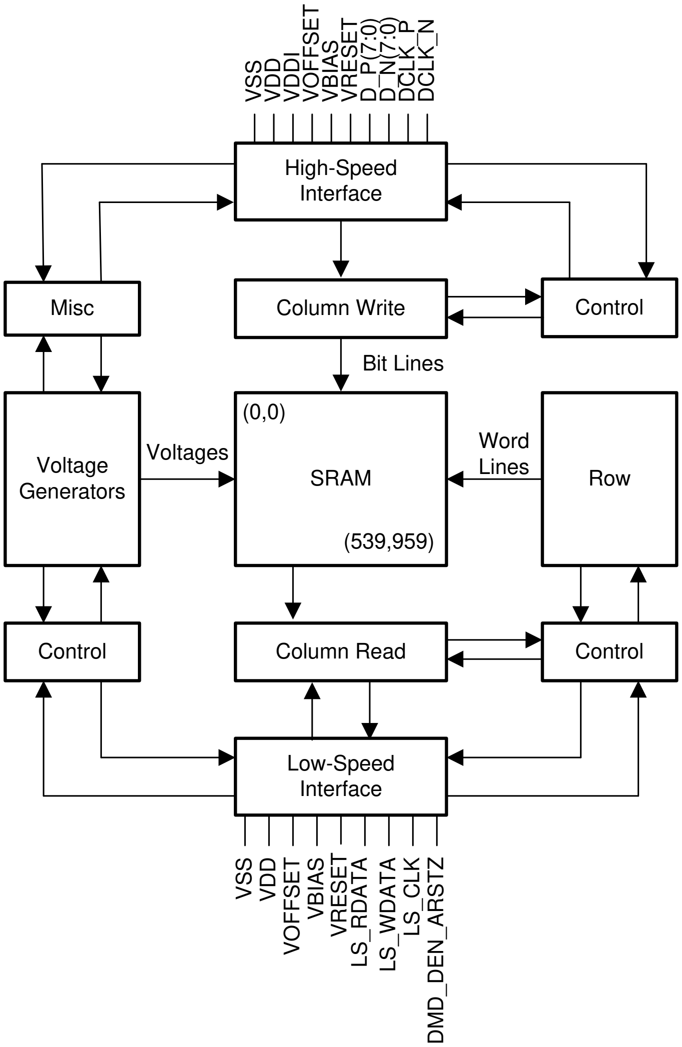
6 Detailed Description

6.1 Overview

The DLP472TP DMD is a 0.47-inch diagonal spatial light modulator which consists of an array of highly reflective aluminum micromirrors. The DMD is an electrical input, optical output micro-optical-electrical-mechanical system (MOEMS). The fast switching speed of the DMD micromirrors combined with advanced DLP image processing algorithms enables each micromirror to display four distinct pixels on the screen during every frame, resulting in a full 3840 × 2160 pixel image being displayed. The electrical interface is low voltage differential signaling (LVDS). The DMD consists of a two-dimensional array of 1-bit CMOS memory cells. The array is organized in a grid of M memory cell columns by N memory cell rows. Refer to the Functional Block Diagram. The positive or negative deflection angle of the micromirrors can be individually controlled by changing the address voltage of underlying CMOS addressing circuitry and micromirror reset signals (MBRST).

The DLP 0.47” 4K UHD chipset is comprised of the DLP472TP DMD, DLPC8445 display controller, and the DLPA3085 PMIC driver. To ensure reliable operation, the DLP472TP DMD must always be used with the DLP display controller and the PMIC specified in the chipset.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Power Interface

The DMD requires 4 DC voltages: 1.8V source, V_{OFFSET}, V_{RESET}, and V_{BIAS}. In a typical LED-based system, 1.8V, V_{OFFSET}, V_{RESET}, and V_{BIAS} is managed by the DLPA3085 PMIC and LED driver.

6.3.2 LPSDR Low-Speed Interface

The Low Speed Interface handles instructions that configure the DMD and control reset operation. LS_CLK is the low-speed clock, and LS_WDATA is the low speed data input.

6.3.3 High-Speed Interface

The purpose of the high-speed interface is to transfer pixel data rapidly and efficiently, making use of high speed DDR transfer and compression techniques to save power and time. The high-speed interface is composed of differential SubLVDS receivers for inputs, with a dedicated clock.

6.3.4 Timing

The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be considered. 図 5-13 shows an equivalent test load circuit for the output under test. Timing reference loads are not intended to be precise representations of any particular system environment or depiction of the actual load presented by a production test. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

6.4 Device Functional Modes

DMD functional modes are controlled by the DLPC8445 display controller. See the DLPC8445 display controller data sheet or contact a TI applications engineer.

6.5 Optical Interface and System Image Quality Considerations

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. Optimizing system optical performance and image quality strongly relate to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance to the optical system operating conditions described in the following sections.

6.5.1 Numerical Aperture and Stray Light Control

The angle defined by the numerical aperture of the illumination and projection optics at the DMD optical area should be the same. This angle should not exceed the nominal device micromirror tilt angle unless appropriate apertures are added in the illumination and projection pupils to block out flat-state and stray light from the projection lens. The micromirror tilt angle defines DMD capability to separate the "ON" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the micromirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle (and vice versa), contrast degradation and objectionable artifacts in the display border and active area could occur.

6.5.2 Pupil Match

TI’s optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within 2° of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display border and active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

6.5.3 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD chip assembly from normal view, and is sized to anticipate several optical operating conditions. Overfill light illuminating the window aperture can create artifacts from the edge of the window aperture opening and other surface anomalies that may be visible on the screen. The illumination optical system should be designed to limit light flux incident anywhere on the window aperture from exceeding approximately 10% of the average flux level in the active area. Depending on the particular system optical architecture, overfill light may have to be further reduced below the suggested 10% level in order to be acceptable.

6.6 Micromirror Array Temperature Calculation

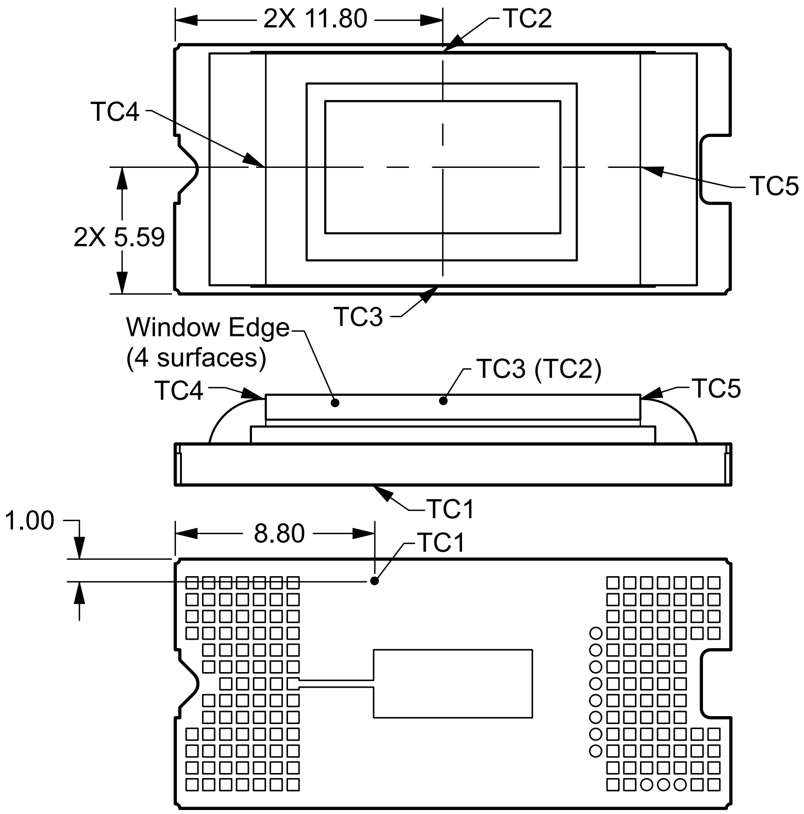


図 6-1. DMD Thermal Test Points

Micromirror array temperature cannot be measured directly, therefore it must be computed analytically from measurement points on the outside of the package, the package thermal resistance, the electrical power, and the illumination heat load. The relationship between array temperature and the reference ceramic temperature (thermal test TC1/TP1 in 図 6-1) is provided by the following equations:

$$T_{ARRAY} = T_{CERAMIC} + (Q_{ARRAY} \times R_{ARRAY\text{-}TO\text{-}CERAMIC})$$

$$Q_{ARRAY} = Q_{ELECTRICAL} + Q_{ILLUMINATION}$$

where

- T_{ARRAY} = Computed array temperature (°C)
- $T_{CERAMIC}$ = Measured ceramic temperature (°C) (TP1 location)
- $R_{ARRAY\text{-}TO\text{-}CERAMIC}$ = Thermal resistance of package specified in 図 6-1 from array to ceramic TP1 (°C/Watt)
- Q_{ARRAY} = Total DMD power on the array (W) (electrical + absorbed)
- $Q_{ELECTRICAL}$ = Nominal electrical power (W)
- $Q_{INCIDENT}$ = Incident illumination optical power (W)
- $Q_{ILLUMINATION}$ = (DMD average thermal absorptivity × $Q_{INCIDENT}$) (W)
- DMD average thermal absorptivity = 0.4

The electrical power dissipation of the DMD is variable and depends on the voltages, data rates, and operating frequencies. A nominal electrical power dissipation to use when calculating array temperature is 1.0 Watts. The absorbed power from the illumination source is variable and depends on the operating state of the micromirrors and the intensity of the light source. The equations shown above are valid for a single chip or multichip DMD system. It assumes an illumination distribution of 83.7% on the active array and 16.3% on the array border.

The sample calculation for a typical projection application is as follows:

$$Q_{INCIDENT} = 9.4\text{W (measured)}$$

$$T_{CERAMIC} = 55.0°\text{C (measured)}$$

$$Q_{ELECTRICAL} = 1.0\text{W}$$

$$Q_{ARRAY} = 1.0\text{W} + (0.40 \times 9.4\text{W}) = 4.76\text{W}$$

$$T_{ARRAY} = 55.0°\text{C} + (4.76\text{ W} \times 1.2°\text{C/W}) = 60.7°\text{C}$$

6.7 Micromirror Power Density Calculation

The calculation of the optical power density of the illumination on the DMD in the different wavelength bands uses the total measured optical power on the DMD, percent illumination overfill, area of the active array, and ratio of the spectrum in the wavelength band of interest to the total spectral optical power.

- $ILL_{UV} = [OP_{UV\text{-}RATIO} \times Q_{INCIDENT}] \times 1000 \div A_{ILL}$ (mW/cm^2)
- $ILL_{VIS} = [OP_{VIS\text{-}RATIO} \times Q_{INCIDENT}] \div A_{ILL}$ (W/cm^2)
- $ILL_{IR} = [OP_{IR\text{-}RATIO} \times Q_{INCIDENT}] \times 1000 \div A_{ILL}$ (mW/cm^2)
- $ILL_{BLU} = [OP_{BLU\text{-}RATIO} \times Q_{INCIDENT}] \div A_{ILL}$ (W/cm^2)
- $ILL_{BLU1} = [OP_{BLU1\text{-}RATIO} \times Q_{INCIDENT}] \div A_{ILL}$ (W/cm^2)

- $A_{ILL} = A_{ARRAY} \div (1 - OV_{ILL})$ (cm^2)

where:

- ILL_{UV} = UV illumination power density on the DMD (mW/cm^2)
- ILL_{VIS} = VIS illumination power density on the DMD (W/cm^2)
- ILL_{IR} = IR illumination power density on the DMD (mW/cm^2)
- ILL_{BLU} = BLU illumination power density on the DMD (W/cm^2)
- ILL_{BLU1} = BLU1 illumination power density on the DMD (W/cm^2)
- A_{ILL} = illumination area on the DMD (cm^2)
- $Q_{INCIDENT}$ = total incident optical power on DMD (W) (measured)
- A_{ARRAY} = area of the array (cm^2) (data sheet)
- OV_{ILL} = percent of total illumination on the DMD outside the array (%) (optical model)
- $OP_{UV\text{-}RATIO}$ = ratio of the optical power for wavelengths <410nm to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{VIS\text{-}RATIO}$ = ratio of the optical power for wavelengths ≥410nm and ≤800nm to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{IR\text{-}RATIO}$ = ratio of the optical power for wavelengths >800nm to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{BLU\text{-}RATIO}$ = ratio of the optical power for wavelengths ≥410nm and ≤475nm to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{BLU1\text{-}RATIO}$ = ratio of the optical power for wavelengths ≥410nm and ≤445nm to the total optical power in the illumination spectrum (spectral measurement)

The illumination area varies and depends on the illumination overfill. The total illumination area on the DMD is the array area and the overfill area around the array. The optical model is used to determine the percent of the total illumination on the DMD that is outside the array (OV_{ILL}) and the percent of the total illumination that is on the active array. From these values, the illumination area (A_{ILL}) is calculated. The illumination is assumed to be uniform across the entire array.

From the measured illumination spectrum, the ratio of the optical power in the wavelength bands of interest to the total optical power is calculated.

Sample calculation:

$Q_{INCIDENT}$ = 9.40 W (measured)

A_{ARRAY} = ((10.368mm × 5.832mm) ÷ 100) = 0.6047cm^2 (data sheet)

OV_{ILL} = 16.3% (optical model)

$OP_{UV\text{-}RATIO}$ = 0.00021 (spectral measurement)

$OP_{VIS\text{-}RATIO}$ = 0.99977 (spectral measurement)

$OP_{IR\text{-}RATIO}$ = 0.00002 (spectral measurement)

$OP_{BLU\text{-}RATIO}$ = 0.28100 (spectral measurement)

$OP_{BLU1\text{-}RATIO}$ = 0.03200 (spectral measurement)

A_{ILL} = 0.6047cm^2 ÷ (1 - 0.163) = 0.7224cm^2

ILL_{UV} = [0.00021 × 9.40 W] × 1000 ÷ 0.7224cm^2 = 2.732mW/cm^2

ILL_{VIS} = [0.99977 × 9.40 W] ÷ 0.7224cm^2 = 13.01mW/cm^2

ILL_{IR} = [0.00002 × 9.40 W] × 1000 ÷ 0.7224cm^2 = 0.260mW/cm^2

ILL_{BLU} = [0.28100 × 9.40 W] ÷ 0.7224cm^2 = 3.66mW/cm^2

ILL_{BLU1} = [0.03200 × 9.40 W] ÷ 0.7224cm^2 = 0.42mW/cm^2

6.8 Micromirror Landed-On/Landed-Off Duty Cycle

6.8.1 Definition of Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the percentage of time that an individual micromirror is landed in the ON state versus the amount of time the same micromirror is landed in the OFF state.

For example, a landed duty cycle of 100/0 indicates that the referenced pixel is in the ON state 100% of the time (and in the OFF state 0% of the time); whereas 0/100 would indicate that the pixel is in the OFF state 100% of the time. Likewise, 50/50 indicates that the pixel is ON for 50% of the time (and OFF for 50% of the time).

Note that when assessing the landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (ON or OFF), the two numbers (percentages) always add to 100.

6.8.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the DMD micromirror array (also called the active array) to an asymmetric landed duty cycle for a prolonged period of time can reduce the DMD useful life.

Note that it is the symmetry/asymmetry of the landed duty cycle that is of relevance. The symmetry of the landed duty cycle is determined by how close the two numbers (percentages) are to being equal. For example, a landed duty cycle of 50/50 is perfectly symmetrical whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

6.8.3 Landed Duty Cycle and Operational DMD Temperature

Operational DMD temperature and landed duty cycle interact to affect DMD useful life, and this interaction can be exploited to reduce the impact that an asymmetrical landed duty cycle has on the DMD useful life. This is quantified in the derating curve shown in 図 5-1. The importance of this curve is that:

- All points along this curve represent the same useful life.
- All points above this curve represent lower useful life (and the further away from the curve, the lower the useful life).
- All points below this curve represent higher useful life (and the further away from the curve, the higher the useful life).

This curve specifies the maximum operating DMD temperature that the DMD should be operated at for a given long-term average landed duty cycle.

6.8.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given period of time, the landed duty cycle of a given pixel follows from the image content being displayed by that pixel.

For example, in the simplest case, when displaying pure-white on a given pixel for a given time period, that pixel operates under a 100/0 landed duty cycle during that time period. Likewise, when displaying pure-black, the pixel operates under a 0/100 landed duty cycle.

Between the two extremes (ignoring for the moment color and any image processing that may be applied to an incoming image), the landed duty cycle tracks one-to-one with the gray scale value, as shown in 表 6-1.

表 6-1. Grayscale Value and Landed Duty Cycle

GRAYSCALE VALUE	LANDED DUTY CYCLE
0%	0/100
10%	10/90
20%	20/80
30%	30/70
40%	40/60
50%	50/50
60%	60/40
70%	70/30
80%	80/20
90%	90/10
100%	100/0

Accounting for color rendition (but still ignoring image processing) requires knowing both the color intensity (from 0% to 100%) for each constituent primary color (red, green, and/or blue) for the given pixel as well as the color cycle time for each primary color, where “color cycle time” is the total percentage of the frame time that a given primary must be displayed in order to achieve the desired white point.

Use 式 1 to calculate the landed duty cycle of a given pixel during a given time period.

$$\text{Landed Duty Cycle} = (\text{Red\_Cycle\_\%} \times \text{Red\_Scale\_Value}) + (\text{Green\_Cycle\_\%} \times \text{Green\_Scale\_Value}) + (\text{Blue\_Cycle\_\%} \times \text{Blue\_Scale\_Value}) \tag{1}$$

where

- Red_Cycle_%, represents the percentage of the frame time that red is displayed to achieve the desired white point
- Green_Cycle_% represents the percentage of the frame time that green is displayed to achieve the desired white point
- Blue_Cycle_%, represents the percentage of the frame time that blue is displayed to achieve the desired white point

For example, assume that the red, green, and blue color cycle times are 30%, 50%, and 20% respectively (in order to achieve the desired white point), then the landed duty cycle for various combinations of red, green, blue color intensities would be as shown in 表 6-2 and 表 6-3.

表 6-2. Example Landed Duty Cycle for Full-Color, Color Percentage

CYCLE PERCENTAGE		
RED	GREEN	BLUE
30%	50%	20%

表 6-3. Example Landed Duty Cycle for Full-Color

SCALE VALUE			LANDED DUTY CYCLE
RED	GREEN	BLUE	
0%	0%	0%	0/100

表 6-3. Example Landed Duty Cycle for Full-Color (続き)

SCALE VALUE			LANDED DUTY CYCLE
RED	GREEN	BLUE	
100%	0%	0%	50/50
0%	100%	0%	20/80
0%	0%	100%	30/70
12%	0%	0%	6/94
0%	35%	0%	7/93
0%	0%	60%	18/82
100%	100%	0%	70/30
0%	100%	100%	50/50
100%	0%	100%	80/20
12%	35%	0%	13/87
0%	35%	60%	25/75
12%	0%	60%	24/76
100%	100%	100%	100/0

The last factor to account for in estimating the landed duty cycle is any applied image processing. Within the controller, the gamma function affects the landed duty cycle.

Gamma is a power function of the form $\text{Output\_Level} = A \times \text{Input\_Level}^{\text{Gamma}}$, where A is a scaling factor that is typically set to 1.

In the controller, gamma is applied to the incoming image data on a pixel-by-pixel basis. A typical gamma factor is 2.2, which transforms the incoming data as shown in 図 6-2.

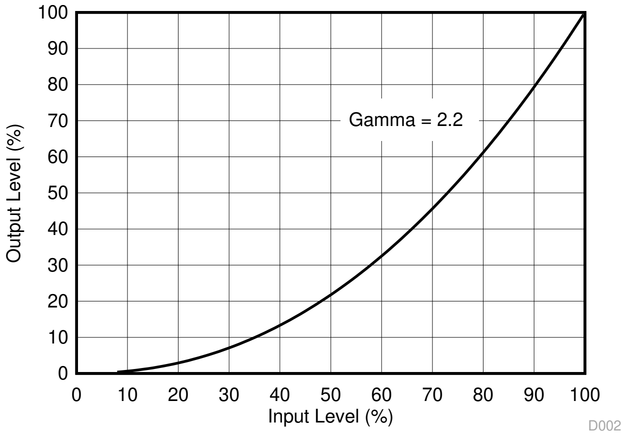


図 6-2. Example of Gamma = 2.2

From 図 6-2, if the gray scale value of a given input pixel is 40% (before gamma is applied), then gray scale value will be 13% after gamma is applied. Therefore, it can be seen that since gamma has a direct impact displayed gray scale level of a pixel, it also has a direct impact on the landed duty cycle of a pixel.

Consideration must also be given to any image processing which occurs before the controller.

7 Application and Implementation

注

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7.1 Application Information

DMDs are spatial light modulators that reflect incoming light from an illumination source to one of two directions, with the primary direction being into a projection or collection optic. Each application is derived primarily from the optical architecture of the system and the format of the data coming into the DLPC8445 controller. The high tilt pixel in the bottom-illuminated DMD increases brightness performance and enables a smaller system footprint for thickness-constrained applications. Typical applications using the DLP472TP include mobile smart TVs and digital signage.

DMD power-up and power-down sequencing is strictly controlled by the DLPA3085 . Refer to セクション 8 for power-up and power-down specifications. To ensure reliable operation, the DLP472TP DMD must always be used with the DLPC8445 controller and a DLPA3085 PMIC.

7.2 Typical Application

The DLP472TP DMD, combined with DLPC8445 digital controller and a power management device, provides full 4K UHD resolution for bright, colorful display applications. See 図 7-1, which shows the system components needed along with the LED configuration of the DLP 0.47” 4K UHD chipset. The components include the DLP472TP DMD, the DLPC8445 display controller, and the DLPA3085 PMIC and LED driver.

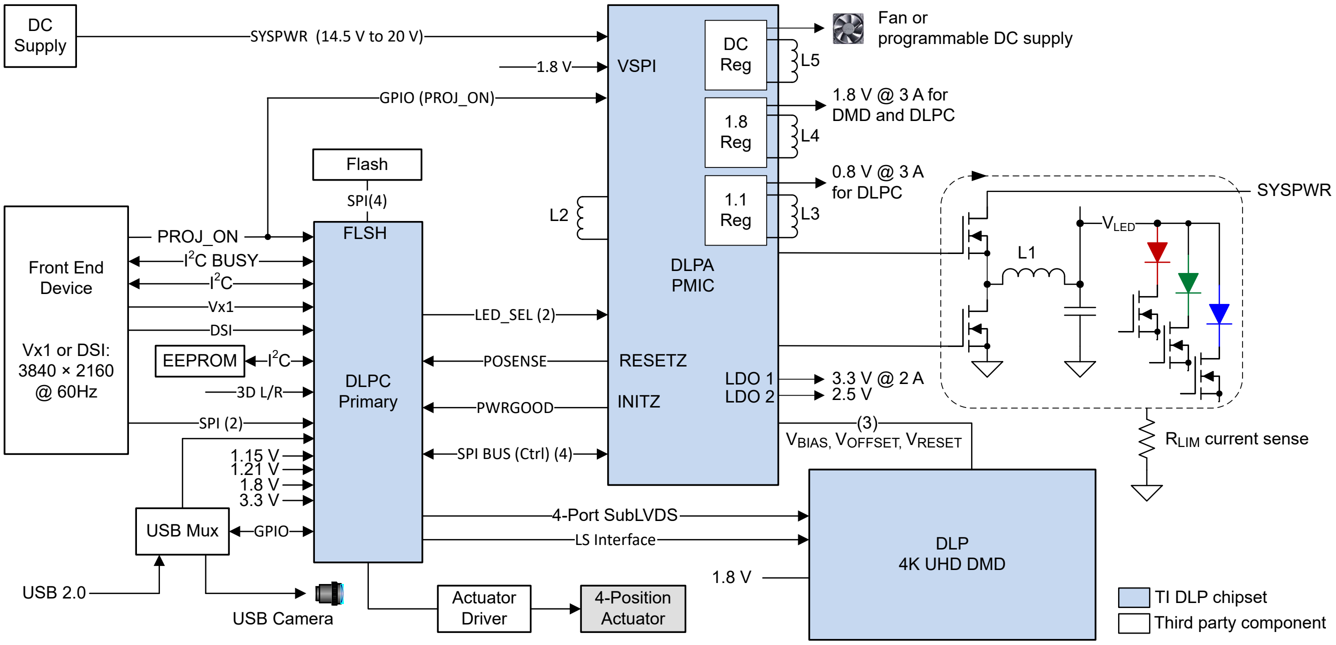


図 7-1. Typical 4K UHD LED Application Diagram

7.2.1 Design Requirements

Other core components of the display system include an illumination source, an optical engine for the illumination and projection optics, other electrical and mechanical components, and software. The type of illumination used and the desired brightness have a major effect on the overall system design and size.

The display system uses the DLP472TP as the core imaging device and contains a 0.47-inch array of micromirrors. The DLPC8445 controller is the digital interface between the DMD and the rest of the system, taking digital input from the front-end receiver and driving the DMD over a high-speed interface. The DLPA3085 PMIC serves as a voltage regulator for the DMD, controller, and LED illumination functionality.

7.2.2 Detailed Design Procedure

For a complete DLP system, an optical module or light engine is required that contains the DLP472TP DMD, associated illumination sources, optical elements, and necessary mechanical components.

To ensure reliable operation, the DMD must always be used with the DLPC8445 display controller and the DLPA3085 PMIC driver.

7.2.3 Application Curve

The typical LED-current-to-luminance relationship when LED illumination is used is shown in 図 7-2.

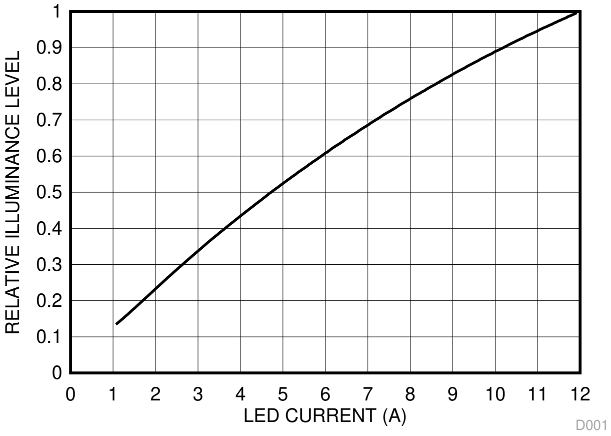


図 7-2. Luminance vs. Current

7.3 Temperature Sensor Diode

The software application provides functions to configure the TMP411 to read the DLP472TP DMD temperature sensor diode. Use this data to incorporate additional functionality in the overall system design, such as adjusting illumination, fan speeds, and so on. All communication between the TMP411 and the DLPC8445 controller is completed using the I^2C interface. The TMP411 connects to the DMD through the pins outlined in セクション 4.

8 Power Supply Recommendations

The following power supplies are all required to operate the DMD:

- V_{SS}
- V_{BIAS}
- V_{DD}
- V_{DDI}
- V_{OFFSET}
- V_{RESET}

DMD power-up and power-down sequencing is strictly controlled by the DLP display controller.

> 注意
>
> For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to any of the prescribed power-up and power-down requirements may affect device reliability. See the DMD power supply sequencing requirements in 図 8-1.
>
> V_{BIAS}, V_{DD}, V_{DDI}, V_{OFFSET}, and V_{RESET} power supplies must be coordinated during power-up and power-down operations. Failure to meet any of the below requirements result in a significant reduction in the DMD reliability and lifetime. Common ground V_{SS} must also be connected.

表 8-1. Power Supply Sequence Requirements

SYMBOL	PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{DELAY}	Delay requirement	from V_{OFFSET} power up to V_{BIAS} power up	2			ms
V_{OFFSET}	Supply voltage level	at beginning of power-up sequence delay(1)			6	V
V_{BIAS}	Supply voltage level	at end of power-up sequence delay(1)			6	V

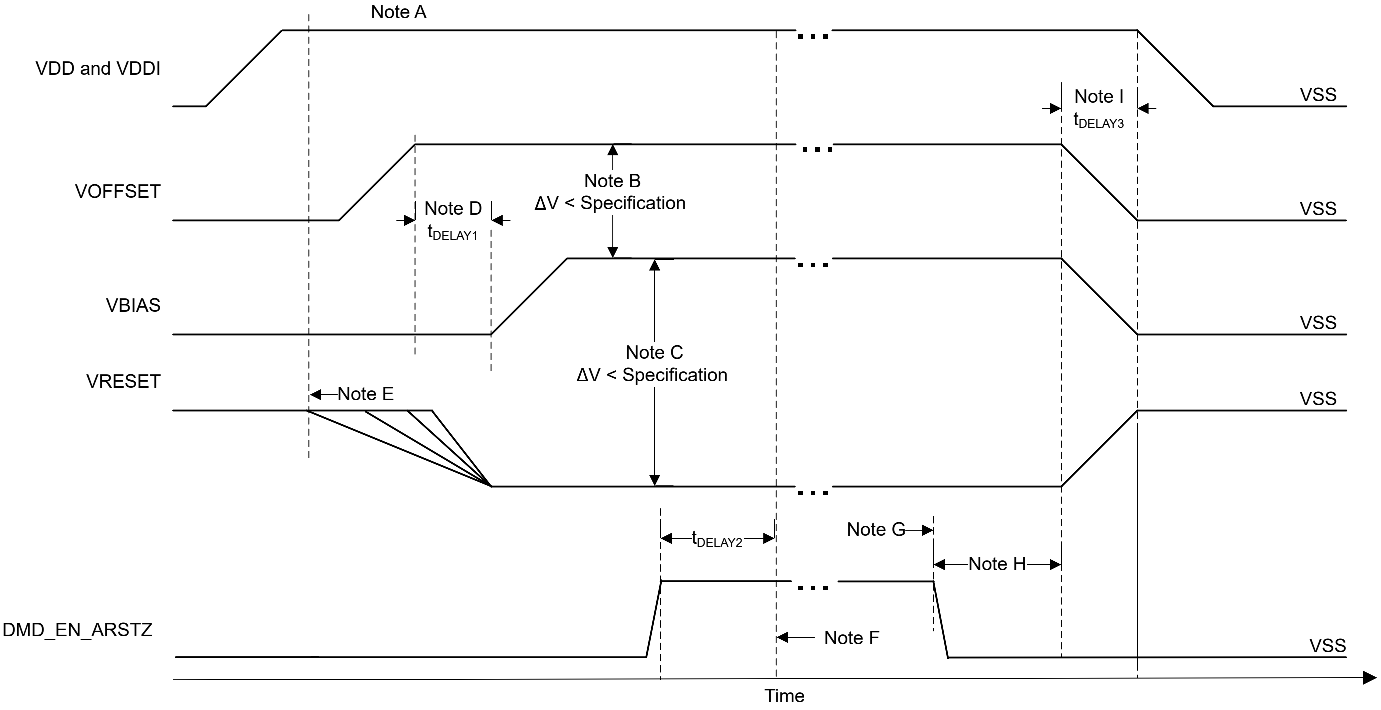
(1) See 図 8-1, Power-Up Sequence Delay Requirement.

8.1 DMD Power Supply Power-Up Procedure

- During power-up, V_{DD} and V_{DDI} must always start and settle before V_{OFFSET} plus Delay1 specified in 表 8-2, V_{BIAS}, and V_{RESET} voltages are applied to the DMD.
- During power-up, it is a strict requirement that the voltage difference between V_{BIAS} and V_{OFFSET} must be within the specified limit shown in セクション 5.4.
- During power-up, there is no requirement for the relative timing of V_{RESET} with respect to V_{BIAS}.
- Power supply slew rates during power-up are flexible, provided that the transient voltage levels follow the requirements specified in セクション 5.1, in セクション 5.4, and in 図 8-1.
- During power-up, LVCMOS input pins must not be driven high until after V_{DD} have settled at operating voltages listed in セクション 5.4.

8.2 DMD Power Supply Power-Down Procedure

- During power-down, V_{DD} and V_{DDI} must be supplied until after V_{BIAS}, V_{RESET}, and V_{OFFSET} are discharged to within the specified limit of ground. See 表 8-2.
- During power-down, it is a strict requirement that the voltage difference between V_{BIAS} and V_{OFFSET} must be within the specified limit shown in セクション 5.4.
- During power-down, there is no requirement for the relative timing of V_{RESET} with respect to V_{BIAS}.
- Power supply slew rates during power-down are flexible, provided that the transient voltage levels follow the requirements specified in セクション 5.1, in セクション 5.4, and in 図 8-1.
- During power-down, LVCMOS input pins must be less than specified in セクション 5.4.



A. See セクション 4 for the *Pin Functions Table*.

B. To prevent excess current, the supply voltage difference $|V_{OFFSET} – V_{BIAS}|$ must be less than the specified limit in セクション 5.4.

C. To prevent excess current, the supply difference $|V_{BIAS} – V_{RESET}|$ must be less than the specified limit in セクション 5.4.

D. V_{BIAS} should power up after V_{OFFSET} has powered up, per the Delay1 specification in 表 8-2.

E. DLP controller software initiates the global V_{BIAS} command.

F. After the DMD micromirror park sequence is complete, the DLP controller software initiates a hardware power-down that activates DMD_EN_ARSTZ and disables V_{BIAS}, V_{RESET}, and V_{OFFSET}.

G. Under power-loss conditions where emergency DMD micromirror park procedures are being enacted by the DLP controller hardware DMD_EN_ARSTZ will go low.

H. V_{DD} must remain high until after V_{OFFSET}, V_{BIAS}, and V_{RESET} go low, per Delay2 specification in 表 8-2.

I. To prevent excess current, the supply voltage delta $|V_{DDI} – V_{DD}|$ must be less than the specified limit in セクション 5.4.

図 8-1. DMD Power Supply Requirements

表 8-2. DMD Power-Supply Requirements

PARAMETER	DESCRIPTION	MIN	NOM	MAX	UNIT
Delay1(1)	Delay from V_{OFFSET} settled at recommended operating voltage to V_{BIAS} and V_{RESET} power up	1	2		ms
Delay2(1)	Delay V_{DD} must be held high from V_{OFFSET}, V_{BIAS}, and V_{RESET} powering down.	50			µs

(1) See 図 8-1.

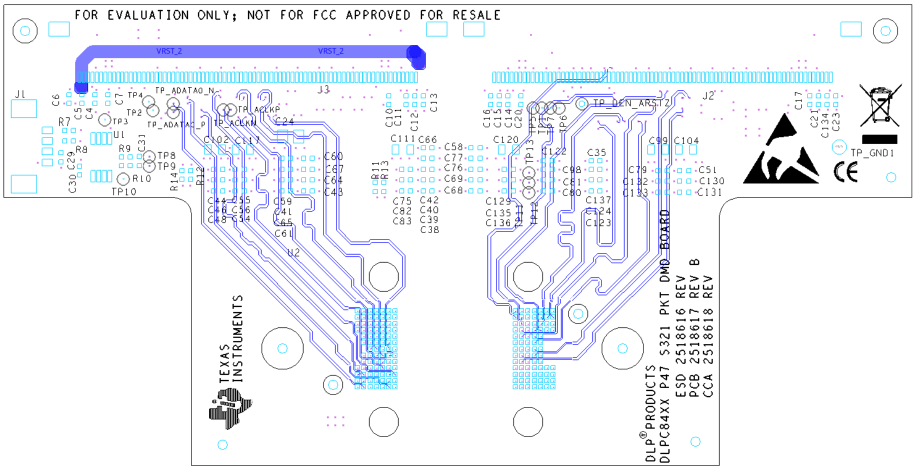
9 Layout

9.1 Layout Guidelines

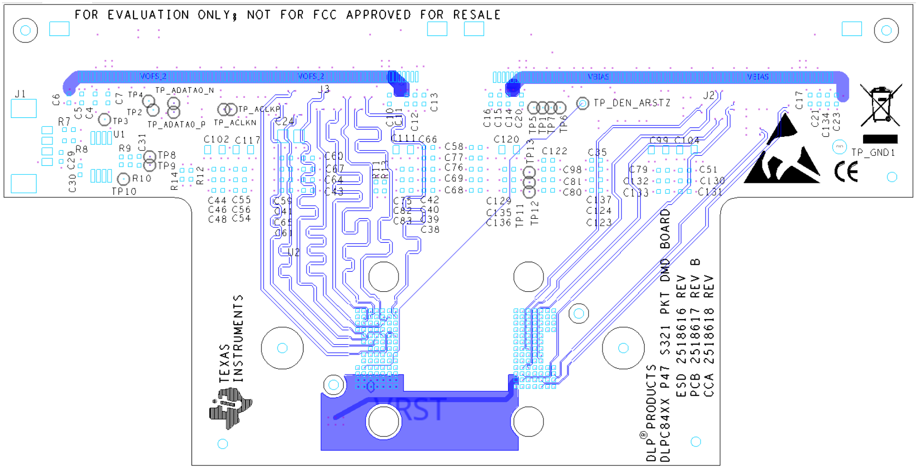
The DLP472TP DMD connects to a PCB or a flex circuit using an interposer. For additional layout guidelines regarding length matching and impedance, see the DLPC8445 controller data sheet. For a detailed layout example, refer to the layout design files. Some layout guidelines for routing to the DLP472TP DMD are:

- Match lengths for the LS_WDATA and LS_CLK signals, as specified in the DLPC8445 controller data sheet.
- Match lengths for the HS_bus differential signals as specified in the DLPC8445 controller data sheet.
- Minimize vias, layer changes, and turns for the HS bus signals. Refer to 図 9-1.
- Supply capacitance needs can vary per design. Refer to the layout design file for a general guideline. Supplies need to be verified on the design to ensure all supplies are operating in the recommended operating range at the DMD.

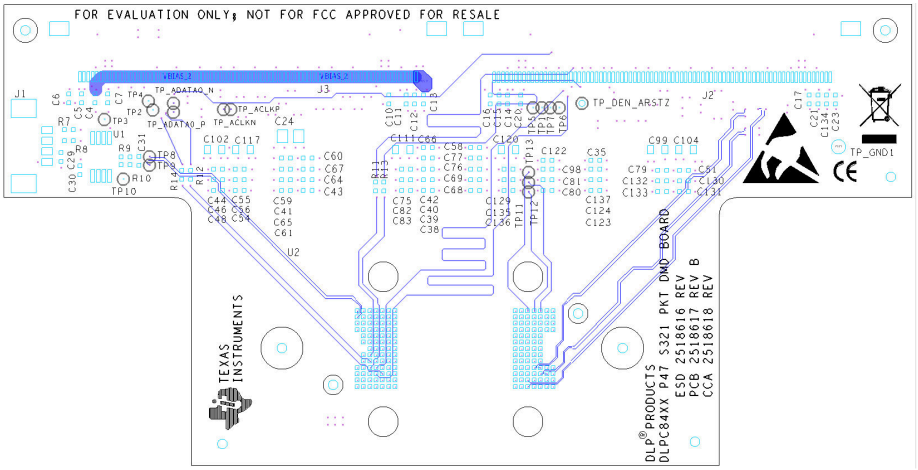
9.2 Layout Example



Layer 4



Layer 7



Layer 9

図 9-1. Routing Example

10 Device and Documentation Support

10.1 サード・パーティ製品に関する免責事項

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10.2 Device Support

10.2.1 Device Nomenclature

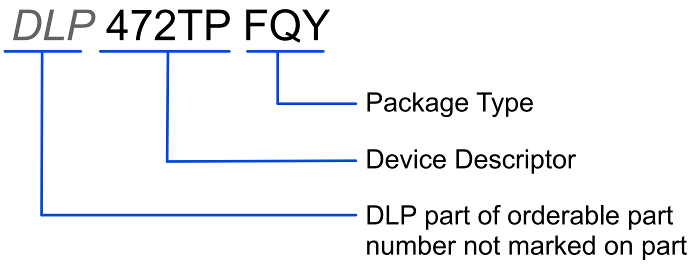

図 10-1. Part Number Description

10.2.2 Device Markings

The device marking includes both human-readable information and a 2-dimensional matrix code. The human-readable information is described in 図 10-2 and includes the legible character string GHJJJJK 472TPFQY. GHJJJJK is the lot trace code and 472TPFQY is the device marking.

Example: GHJJJJK DLP472TPFQY

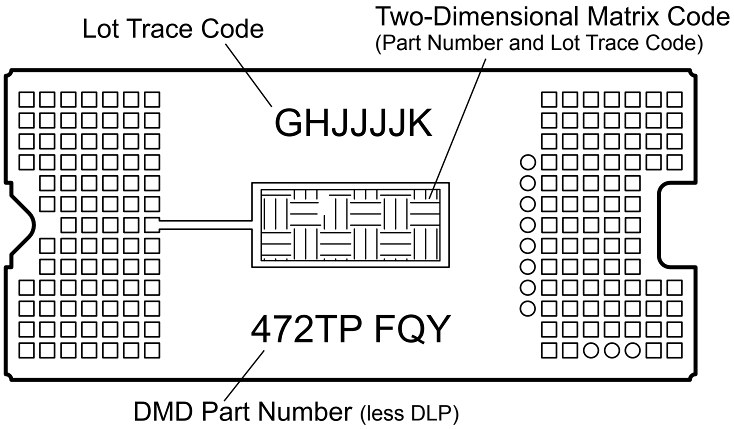

図 10-2. DMD Marking Locations

10.3 Documentation Support

10.3.1 Related Documentation

The following documents contain additional information related to the chipset components used with the DMD.

- *DLPC8445 High Resolution Controller Data Sheet*
- *DLPA3085 PMIC and High-Current LED Driver IC Data Sheet*

10.4 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

10.5 Trademarks

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10.7 用語集

テキサス・インスツルメンツ用語集	この用語集には、用語や略語の一覧および定義が記載されています。

11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
August 2024	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DLP472TPFQY	Active	Production	CLGA (FQY) | 174	80 | JEDEC TRAY (5+1)	In-Work	NIAU	N/A for Pkg Type	0 to 70	
DLP472TPFQY.B	Active	Production	CLGA (FQY) | 174	80 | JEDEC TRAY (5+1)	In-Work	NIAU	N/A for Pkg Type	0 to 70	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

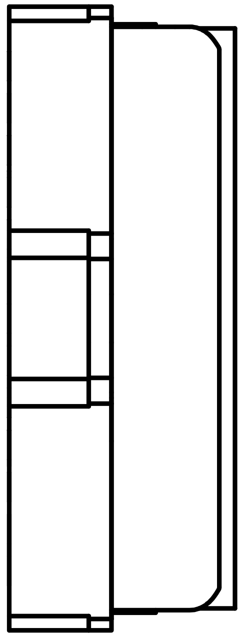
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

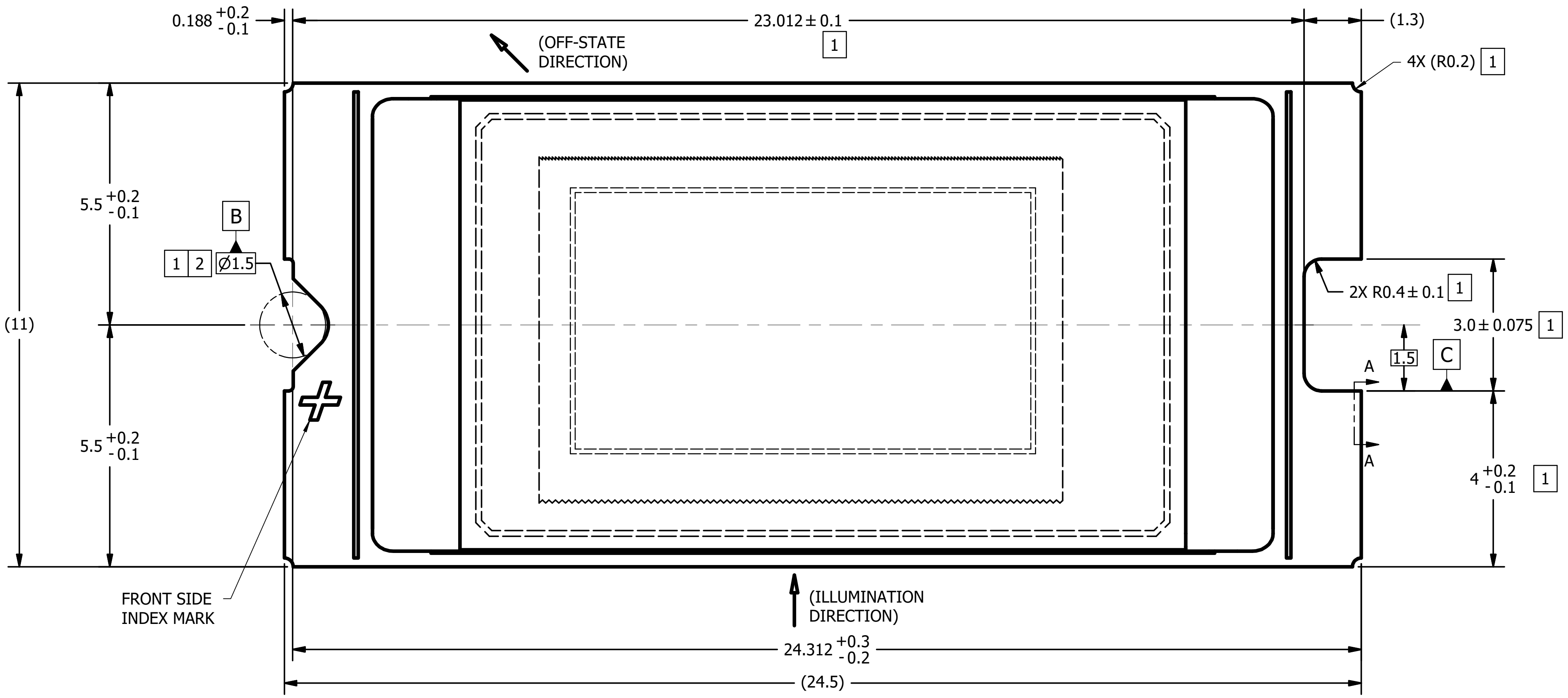
NOTES UNLESS OTHERWISE SPECIFIED:

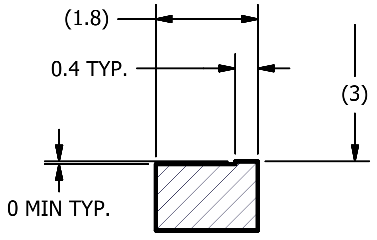
1. NOTCH DIMENSIONS ARE DEFINED BY UPPERMOST LAYERS OF CERAMIC, AS SHOWN IN SECTION A-A.
2. SEE DETAIL B FOR "V-NOTCH" DIMENSIONS.
3. DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY.
4. WHILE ONLY THE THREE DATUM A TARGET AREAS A1, A2, AND A3 ARE USED FOR MEASUREMENT, ALL 4 CORNERS SHOULD BE CONTACTED, INCLUDING E1, TO SUPPORT MECHANICAL LOADS.
5. ENCAPSULANT TO BE CONTAINED WITHIN DIMENSIONS SHOWN IN VIEW D (SHEET 2). NO ENCAPSULANT IS ALLOWED ON TOP OF THE WINDOW.
6. ENCAPSULANT NOT TO EXCEED THE HEIGHT OF THE WINDOW.
7. ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND HAS A MAXIMUM ALLOWED VALUE OF 0.6 DEGREES.
8. BOUNDARY MIRRORS SURROUNDING THE DMD ACTIVE ARRAY.

REVISIONS

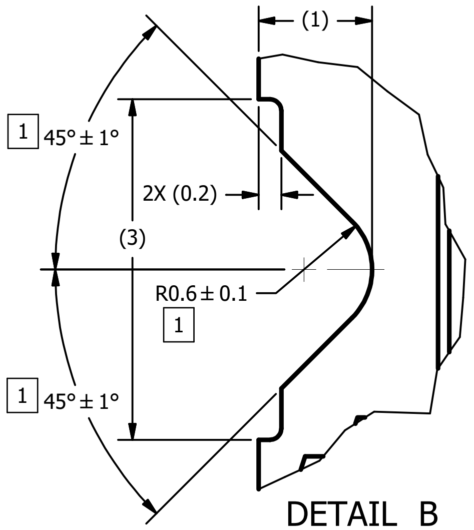
REV	DESCRIPTION	DATE	BY
A	ECO 2202674: INITIAL RELEASE	12/22/22	HG



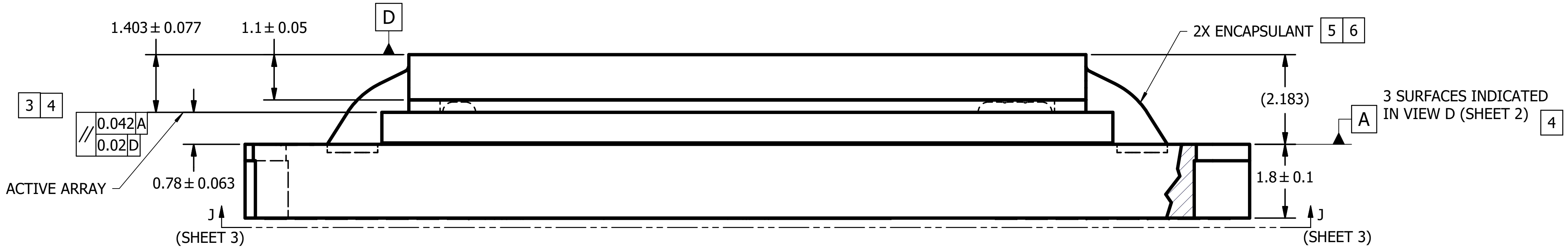




SECTION A-A
NOTCH OFFSET



DETAIL B
V-NOTCH
SCALE 30 : 1



NEXT ASSY	USED ON
	0314DA
APPLICATION	

THIRD ANGLE PROJECTION

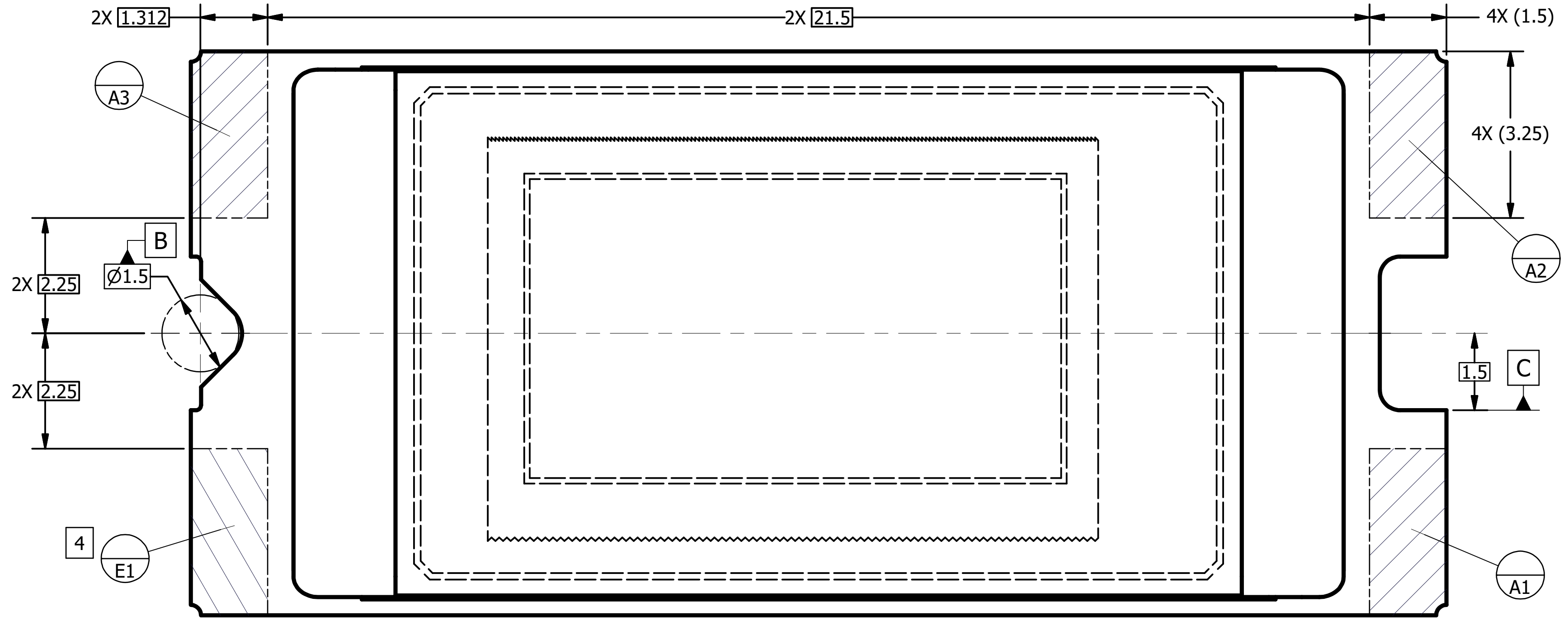
UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN MILLIMETERS
- TOLERANCES:
  - ANGLES ± 1°
  - 2 PLACE DECIMALS ± 0.25
  - 1 PLACE DECIMALS ± 0.50
- ~~DIMENSIONAL LIMITS APPLY BEFORE PROCESSES~~
- INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5M-1994
- ~~REMOVE ALL BURRS AND SHARP EDGES~~
- PARENTHETICAL INFORMATION FOR REFERENCE ONLY

		DATE
DRAWN	H. GAGLIARDI	1/22/2023
ENGINEER	H. GAGLIARDI	12/22/2022
QA/CE	P. KONRAD	12/27/2022
CM	B. HASKETT	12/22/2022
	J. McKINLEY	12/22/2022
APPROVED	M. GARCIA	1/3/2023

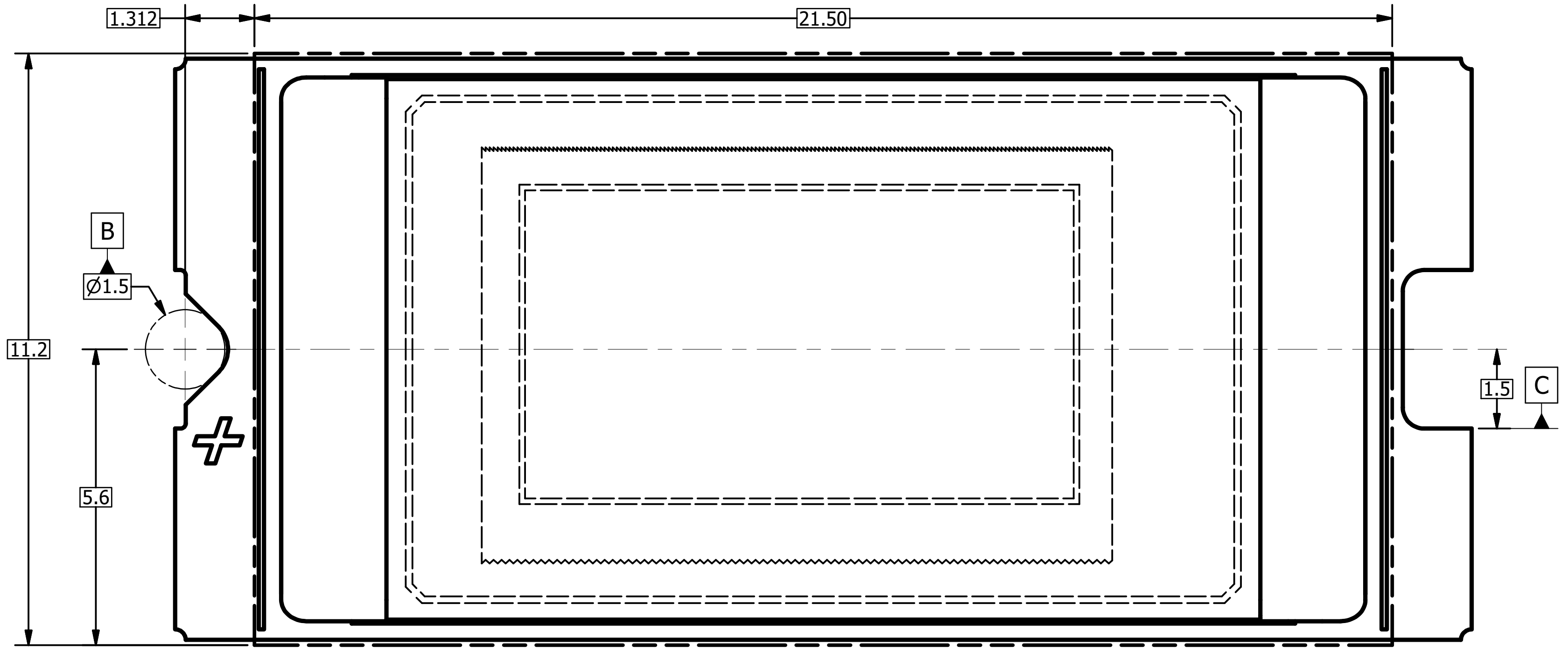
TEXAS INSTRUMENTS
Dallas Texas

TITLE
ICD, MECHANICAL, DMD,
.47 4K PKT-LVDS3 SERIES 321,
(FQY PACKAGE)

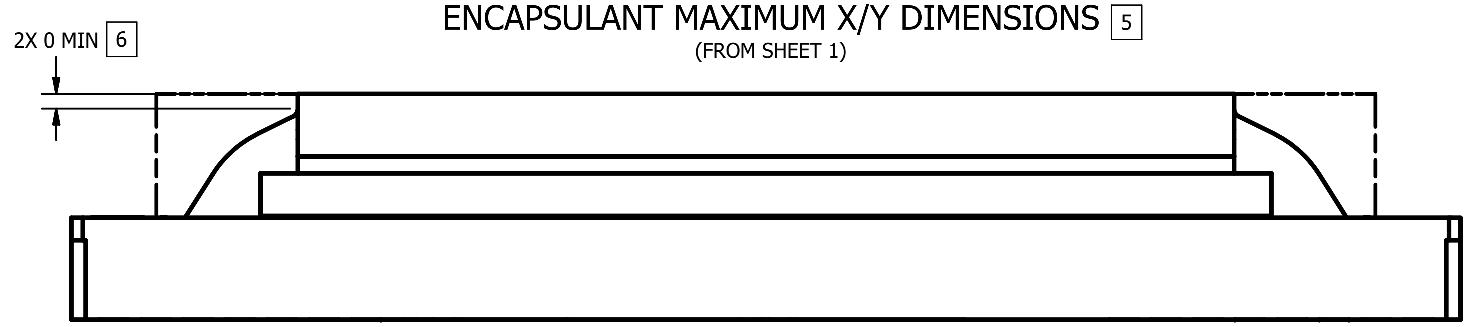
SIZE D | DWG NO 2518523 | REV A
SCALE 15:1 | SHEET 1 OF 3



VIEW C
DATUMS A AND E
(SUBSTRATE METALLIZATION OMITTED FOR CLARITY)
(FROM SHEET 1)



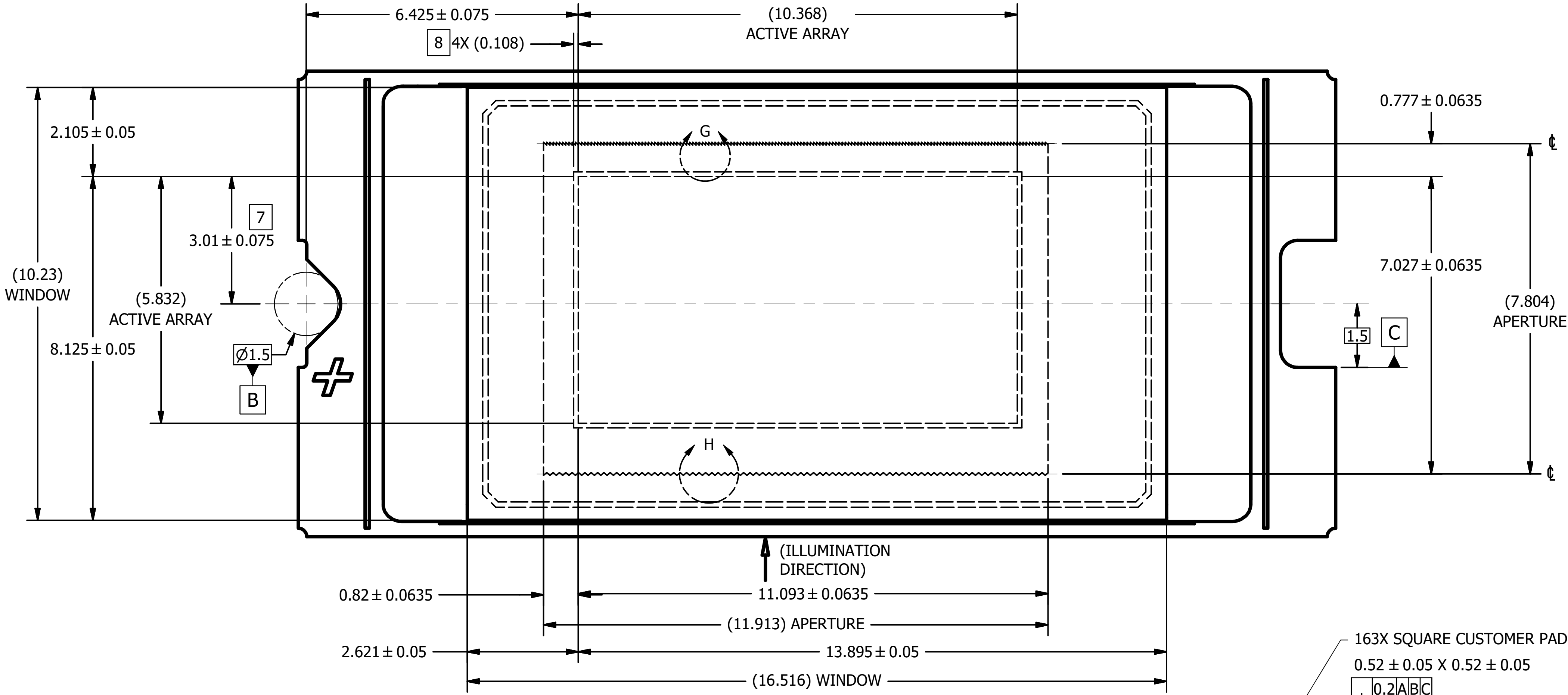
VIEW D
ENCAPSULANT MAXIMUM X/Y DIMENSIONS 5
(FROM SHEET 1)



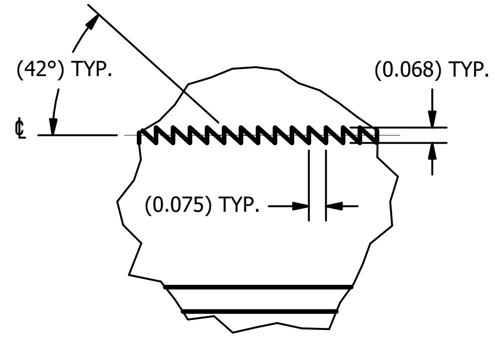
VIEW E
ENCAPSULANT MAXIMUM HEIGHT

TEXAS INSTRUMENTS
Dallas Texas

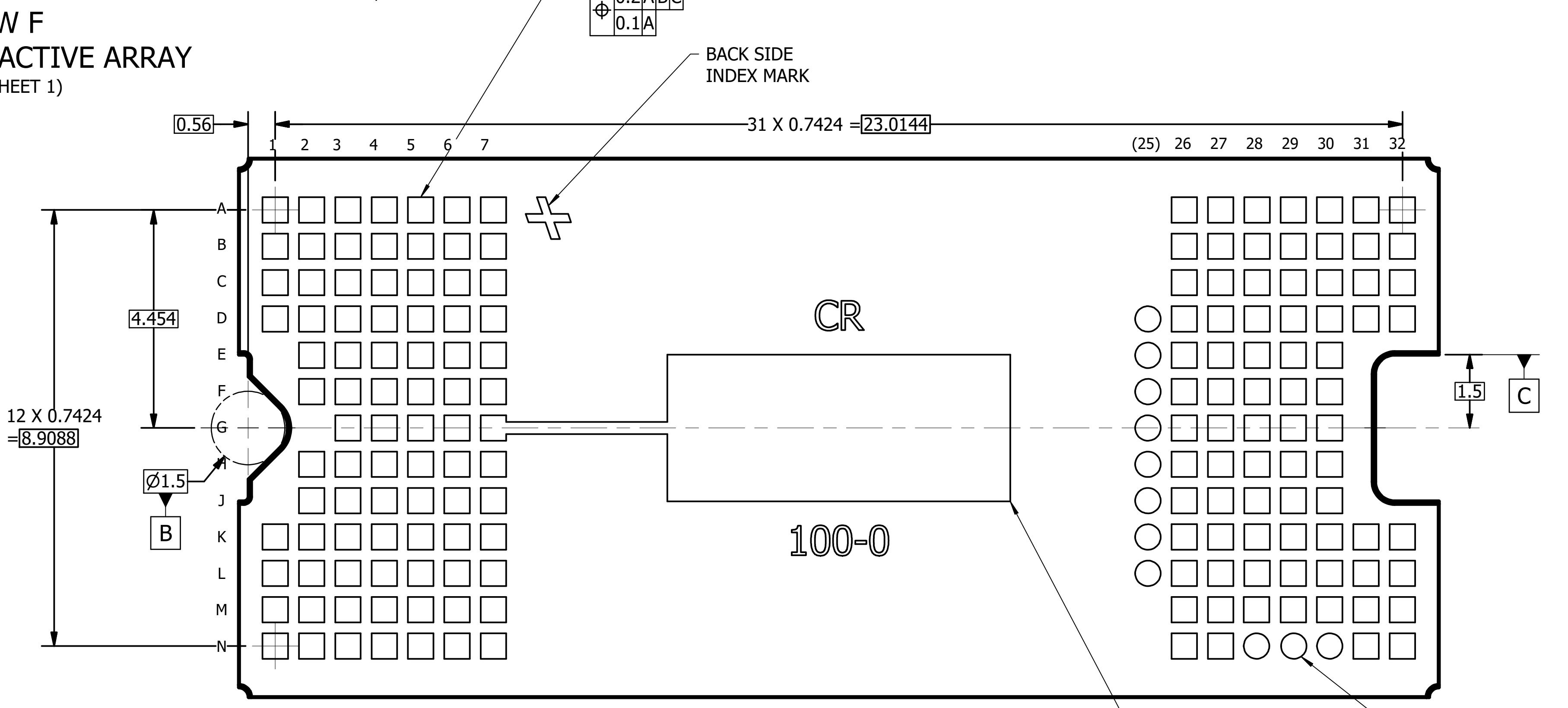
DRAWN H. GAGLIARDI	DATE 1/22/2023	SIZE D	DWG NO 2518523	REV A
		SCALE	SHEET 2 OF 3	



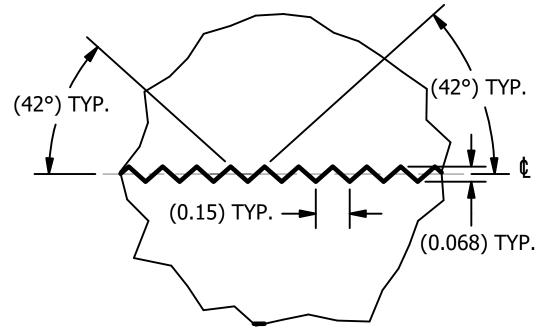
VIEW F
WINDOW AND ACTIVE ARRAY
(FROM SHEET 1)



DETAIL G
APERTURE TOP EDGE
SCALE 60 : 1



VIEW J-J
BACK SIDE METALLIZATION
(FROM SHEET 1)



DETAIL H
APERTURE BOTTOM EDGE
SCALE 60 : 1

TEXAS INSTRUMENTS Dallas Texas	DRAWN H. GAGLIARDI	DATE 1/22/2023	SIZE D	DWG NO 2518523	REV A
			SCALE	SHEET 3 OF 3	

重要なお知らせと免責事項

最終更新日：2025 年 10 月