TEXAS INSTRUMENTS
DRV8213
JAJSOH4 – AUGUST 2023

DRV8213 電流センス、電流レギュレーション、ストール検出機能を内蔵した 4A ブラシ付き DC モーター・ドライバ

1 特長

- N チャネル、H ブリッジ、ブラシ付き DC モーター・ドライバ
- 動作電源電圧範囲:**1.65V～11V**
- **240mΩ** の $R_{DS(on)}$ (ハイサイド+ローサイド)
- 高い出力電流能力:4A (ピーク)
- PWM 制御インターフェイス、最大 100kHz のスイッチング
- 1.8V、3.3V、5V のロジック入力電圧をサポート
- 電流センスおよび電流レギュレーション機能を内蔵
- アナログ電流センス出力 (**IPROPI**)
- ゲイン選択 (**GAINSEL**) 機能:
  - 最小 **10mA** までの高精度電流センス
  - さまざまな電流範囲に合わせて最適化された $R_{DS(on)}$ および過電流制限
- 設定可能な突入時間 (RTE パッケージのみ)
- **内蔵**チャージ・ポンプ
- 低消費電力のスリープ・モードによる長いバッテリ寿命
  - **60nA 未満**の最大スリープ電流
- 小さいパッケージ占有面積
- 保護機能内蔵
  - VM 低電圧誤動作防止 (UVLO)
  - 自動リトライ過電流保護 (OCP)
  - サーマル・シャットダウン (TSD)
  - **ストール検出** (RTE パッケージのみ)

2 アプリケーション

- ブラシ付き DC モーター、ソレノイド、リレー駆動
- 水道およびガス・メーター
- 電子スマート・ロック
- 電子 / ロボット玩具
- 輸液ポンプおよびその他のポータブル医療機器
- 電動歯ブラシ
- 美容と化粧
- 携帯プリンタ
- POS (販売時点情報管理) デバイス
- その他のバッテリ駆動 DC モーター・アプリケーション

3 概要

DRV8213 は、N チャネル H ブリッジ、チャージ・ポンプ、電流センス出力、電流レギュレーション、保護回路を備えた統合型モーター・ドライバです。3 段のチャージ・ポンプにより、最低 1.65V で動作し、1.8V の電源レールとバッテリの低電圧に対応できます。チャージ・ポンプにはすべてのコンデンサが内蔵されており、100% のデューティ・サイクル動作が可能です。

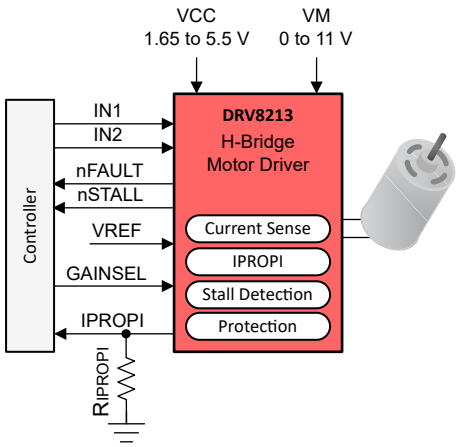
内部カレント・ミラーは、電流センスとレギュレーションを実装しています。そのため、大電力シャント抵抗を使う必要がなく、基板面積を節約しシステム・コストを低減できます。IPROPI 電流センス出力を使うと、マイコンはモーターのストールまたは負荷条件の変化を検出できます。ゲイン選択 (GAINSEL) 機能により、平均モーター電流 10mA までの高精度の電流センスが可能です。VREF ピンを使うことで、起動および高負荷イベント中もマイコンを使わずにモーター電流をレギュレーションできます。RTE パッケージは、センサレス・モーター・ストール検出とマイコンへのレポートをサポートしています。

低消費電力スリープ・モードは、内部回路の多くをシャットダウンすることで非常に小さい静止電流を実現します。低電圧誤動作防止、過電流、過熱に対する内部保護機能を備えています。

製品情報 (1)

部品番号	パッケージ	本体サイズ (公称)
DRV8213DSG	WSON (8)	2.00mm × 2.00mm
DRV8213RTE	WQFN (16)	3.00mm × 3.00mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。



概略回路図 (RTE パッケージ)

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
August 2023	*	Initial Release

5 Device Comparison

表 5-1. Device Comparison Table

Part Number	Package	Supply (VM, Volts)	$R_{DS(on)}$ (mΩ)	Current Regulation	Current Sense Output	Stall Detection	Package Size
DRV8213	RTE	1.65 to 11	240	**Yes**	**Yes**	**Yes**	3 mm x 3 mm
DRV8213	DSG	1.65 to 11	240	**Yes**	**Yes**	No	2 mm x 2 mm
DRV8212/P	DSG	1.65 to 11	280	No	No	No	2 mm x 2 mm
DRV8210/P	DSG	1.65 to 11	1000	No	No	No	2 mm x 2 mm
DRV8837	DSG	0 to 11	280	No	No	No	2 mm x 2 mm
DRV8837C	DSG	0 to 11	1000	No	No	No	2 mm x 2 mm

6 Pin Configuration and Functions

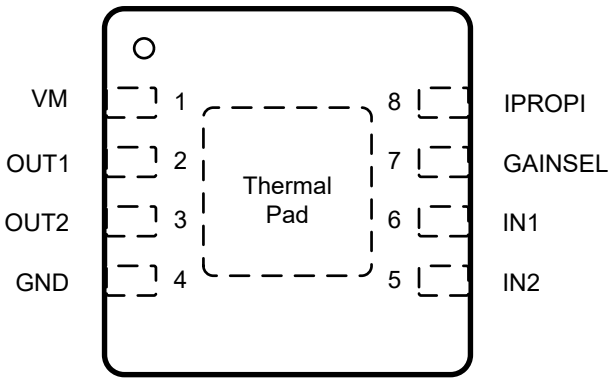


図 6-1. DSG Package (WSON) Top View

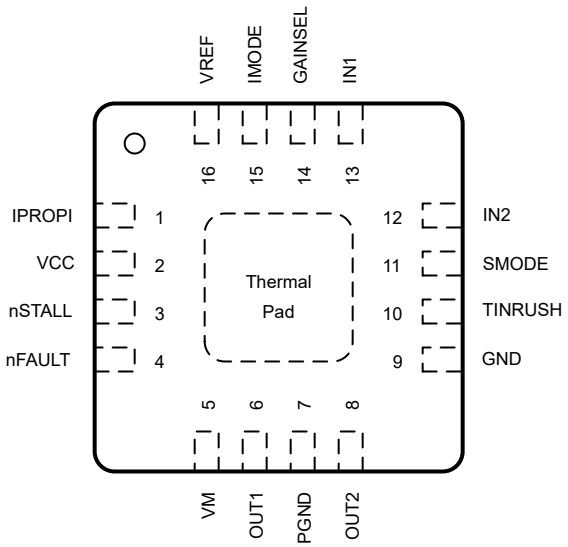


図 6-2. RTE Package (WQFN) Top View

表 6-1. Pin Functions

PIN			TYPE	DESCRIPTION
NAME	DSG	RTE		
GND	4	9	PWR	Device ground. Connect to system ground.
IMODE	—	15	I	Current regulation mode configuration. Tri-level input. See 表 8-4.
IN1	6	13	I	Controls the H-bridge output. Has internal pulldown. Logic input. See 表 8-2.
IN2	5	12	I	Controls the H-bridge output. Has internal pulldown. Logic input. See 表 8-2.
IPROPI	8	1	PWR	Analog current output proportional to load current. See セクション 8.4.2.1.
nFAULT	—	4	OD	Fault indicator output. Pulled low during a fault condition. Connect an external pullup resistor for open-drain operation. Connect to nSTALL pin to reduce number of external components. See セクション 8.4.4.
nSTALL	—	3	OD	Stall detection enable and stall indicator output. Pulled low during a stall condition. Connect an external pullup resistor for open-drain operation. Connect to nFAULT pin to reduce number of external components. Connect to GND to disable stall detection. See セクション 8.4.3.
OUT1	2	6	O	H-bridge output. Connect directly to the motor or other inductive load.
OUT2	3	8	O	H-bridge output. Connect directly to the motor or other inductive load.
PGND	—	7	PWR	Device power ground. Connect to system ground.
SMODE	—	11	I	Stall detection response configuration. Tri-level input. See 表 8-6.
TINRUSH	—	10	O	Sets timing for stall detection to ignore motor inrush current. Connect to a ceramic capacitor to system ground. See セクション 8.4.3.
VCC	—	2	PWR	Logic power supply. Bypass this pin to the GND pin with a 0.1-µF ceramic capacitor rated for VCC.
VM	1	5	PWR	Motor power supply. Bypass this pin to the GND pin with a 0.1-µF ceramic capacitor as well as sufficient bulk capacitance rated for VM.
VREF	—	16	I	Analog input to set current regulation and stall detection level. For the DSG package, VREF is internally fixed at 510 mV. For information on current regulation, see セクション 8.4.2.2. For more information on stall detection, see セクション 8.4.3.
GAINSEL	7	14	I	Configures IPROPI gain factor depeding on the output current range. Tri-level input.
PAD	—	—	—	Thermal pad. Connect to board ground. For good thermal dissipation, use large ground planes on multiple layers, and multiple nearby vias connecting those planes.

7 Specifications

7.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Power supply pin voltage	VM	-0.5	12	V
Logic power supply pin voltage	VCC	-0.5	5.75	V
Power supply transient voltage ramp	VM, VCC	0	2	V/µs
Voltage difference between ground pins	GND, PGND	-0.6	0.6	V
Logic pin voltage	IN1, IN2, GAINSEL, nSLEEP, IMODE, SMODE	-0.3	5.75	V
Open-drain output pin voltage	nFAULT, nSTALL	-0.3	5.75	V
Timing capacitor current output pin voltage	TINRUSH	-0.3	V_{VCC}	V
Proportional current output pin voltage, VM ≥ 5.45 V	IPROPI	-0.3	5.75	V
Proportional current output pin voltage, VM < 5.45 V		-0.3	V_{VM} + 0.3	V
Reference input pin voltage	VREF	0.3	5.75	V
Output pin voltage	OUTx	$-V_{SD}$	$V_{VM}+V_{SD}$	V
Output current	OUTx	Internally Limited	Internally Limited	A
Ambient temperature, T_A		–40	125	°C
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ± 2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ± 500 V may actually have higher performance.

7.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{VM}	Power supply voltage, DSG	VM	1.65		11	V
V_{VM}	Power supply voltage, RTE	VM	0		11	V
V_{VCC}	Power supply voltage, RTE	VCC	1.65		5.5	V
V_{IN}	Logic input voltage	IN1, IN2, nSLEEP, IMODE, SMODE, GAINSEL	0		5.5	V
f_{PWM}	PWM frequency	IN1, IN2	0		100	kHz
V_{OD}	Open drain pullup voltage	nFAULT, nSTALL	0		5.5	V
I_{OD}	Open drain output current	nFAULT, nSTALL	0		5	mA
I_{OUT} (1)	Peak output current	OUTx	0		4	A
I_{IPROPI}	Current sense output current	IPROPI	0		1	mA

over operating temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{VREF}	Current limit reference voltage	VREF	0		min (3.3, V_{VM} - 1.25)	V
T_A	Operating ambient temperature		–40		125	°C
T_J	Operating junction temperature		–40		150	°C

(1) Power dissipation and thermal limits must be observed

7.4 Thermal Information

THERMAL METRIC(1)		DEVICE DSG (WSON) 8 PINS	DEVICE RTE (WQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	65.9	50.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	75.2	52.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	28.7	25.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.0	1.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	28.7	25.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	12.0	11.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

DSG: 1.65 V ≤ V_{VM} ≤ 11 V, RTE: 0 V ≤ V_{VM} ≤ 11 V and 1.65 V ≤ V_{VCC} ≤ 5.5 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical values are at T_J = 27°C, V_{VM} = 5 V, V_{VCC} = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES, DSG (VM)						
I_{VMQ}	VM sleep mode current	IN1 = IN2 = 0 V, after waiting $t_{AUTOSLEEP}$, V_{VM} = 5 V, T_J = 27°C		20	60	nA
I_{VM}	VM active mode current	IN1 = 3.3 V, IN2 = 0 V		1.2	1.9	mA
t_{WAKE}	Turnon time	Sleep mode to active mode delay			250	µs
$t_{AUTOSLEEP}$	Autosleep turnoff time	Active mode to autosleep mode delay	0.7	1	1.3	ms
f_{VCP}	Charge pump switching frequency			6000		kHz
POWER SUPPLIES, RTE (VM, VCC)						
I_{VMQ}	VM sleep mode current	IN1 = IN2 = 0 V, after waiting $t_{AUTOSLEEP}$, V_{VM} = 5 V, V_{VCC} = 3.3 V, T_J = 27°C		10	20	nA
I_{VM}	VM active mode current	IN1 = 3.3 V, IN2 = 0 V, V_{VM} = 5 V, V_{VCC} = 3.3 V		0.83	1	mA
I_{VCCQ}	VCC sleep mode current	IN1 = IN2 = 0 V, after waiting $t_{AUTOSLEEP}$, V_{VM} = 5 V, V_{VCC} = 3.3 V, T_J = 27°C		6	12	nA
I_{VCC}	VCC active mode current	IN1 = 3.3 V, IN2 = 0 V, V_{VM} = 5 V, V_{VCC} = 3.3 V		0.46	0.6	mA
t_{WAKE}	Turnon time	Sleep mode to active mode delay			250	µs
$t_{AUTOSLEEP}$	Autosleep turnoff time	Active mode to autosleep mode delay	0.75	0.9	1.05	ms
LOGIC-LEVEL INPUTS (IN1, IN2)						
V_{IL}	Input logic low voltage		0		0.4	V
V_{IH}	Input logic high voltage		1.45		5.5	V
V_{HYS}	Input hysteresis		40			mV
I_{IL}	Input logic low current	V_I = 0 V	-1		1	µA

DSG: 1.65 V ≤ V_{VM} ≤ 11 V, RTE: 0 V ≤ V_{VM} ≤ 11 V and 1.65 V ≤ V_{VCC} ≤ 5.5 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical values are at T_J = 27°C, V_{VM} = 5 V, V_{VCC} = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	Input logic high current	V_{INx} = 5 V	15		35	µA
		V_{nSTALL} = VCC			40	nA
R_{PD}	Input pulldown resistance, INx			200		kΩ
$t_{DEGLITCH}$	Input logic deglitch, INx			50		ns
TRI-LEVEL INPUTS (IMODE, SMODE)						
V_{THYS}	Tri-level input logic low voltage		0		0.4	V
I_{TIL}	Tri-level input Hi-Z voltage		0.75		1.05	V
I_{TIZ}	Tri-level input logic high voltage		1.45		5.5	V
R_{TPD}	Tri-level pulldown resistance	to GND		83		kΩ
I_{TPU}	Tri-level pullup current	to VCC		10.5		µA
OPEN-DRAIN OUTPUTS (nFAULT, nSTALL)						
V_{OL}	Output logic low voltage	I_{OD} = 5 mA			0.4	V
I_{OZ}	Output logic high current	V_{OD} = VCC	-1		1	µA
DRIVER OUTPUTS (OUTx)						
$R_{DS(ON)\_HS}$	High-side MOSFET on resistance	I_{OUTx} = 1 A		120	280	mΩ
$R_{DS(ON)\_LS}$	Low-side MOSFET on resistance, 350mA to 2A	GAINSEL = Low		120	260	mΩ
$R_{DS(ON)\_LS}$	Low-side MOSFET on resistance, 60mA to 350mA	GAINSEL = High-Z		460	900	mΩ
$R_{DS(ON)\_LS}$	Low-side MOSFET on resistance, 10mA to 60mA	GAINSEL = High		2100	4000	mΩ
V_{SD}	Body diode forward voltage	I_{OUTx} = -1 A		0.9		V
t_{RISE}	Output rise time	V_{OUTx} rising from 10% to 90% of V_{VM}		70		ns
t_{FALL}	Output fall time	V_{OUTx} falling from 90% to 10% of V_{VM}		40		ns
t_{PDR}	Input high to output high propagation delay	Input to OUTx		450		ns
t_{PDF}	Input low to output low propagation delay	Input to OUTx		450		ns
t_{DEAD}	Output dead time			500		ns
CURRENT SENSE AND REGULATION (IPROPI, VREF)						
V_{REF_INT}	Internal reference voltage	SMODE = Open for RTE package and for DSG package	470	510	550	mV
A_{IPROPI_H}	Current scaling factor	GAINSEL = Low		205		µA/A
A_{IPROPI_M}	Current scaling factor	GAINSEL = High-Z		1050		µA/A
A_{IPROPI_L}	Current scaling factor	GAINSEL = High		4900		µA/A
A_{ERR_H}	Current mirror total error, 350 mA to 2 A	GAINSEL = Low, V_{IPROPI} ≤ min(VM-1.25 V, 3.3 V), 3.3 V ≤ V_{VM} ≤ 11 V	-6		6	%
A_{ERR_H}	Current mirror total error, 350 mA to 2 A	GAINSEL = Low, V_{IPROPI} ≤ min(VM-1.25 V, 3.3 V), 1.65 V ≤ V_{VM} ≤ 3.3 V	-6		6	%
A_{ERR_M}	Current mirror total error, 60 mA to 350 mA	GAINSEL = High-Z, V_{IPROPI} ≤ min(VM-1.25 V, 3.3 V), 3.3 V ≤ V_{VM} ≤ 11 V	-6		6	%
		GAINSEL = High-Z, V_{IPROPI} ≤ min(VM-1.25 V, 3.3 V), 1.65 V ≤ V_{VM} ≤ 3.3 V	-6		6	%
A_{ERR_L}	Current mirror total error, 10 mA to 60 mA	GAINSEL = High, V_{IPROPI} ≤ min(VM-1.25 V, 3.3 V), 3.3 V ≤ V_{VM} ≤ 11 V	-6		6	%
		GAINSEL = High, V_{IPROPI} ≤ min(VM-1.25 V, 3.3 V), 1.65 V ≤ V_{VM} ≤ 3.3 V	-6		6	%

DSG: 1.65 V ≤ V_{VM} ≤ 11 V, RTE: 0 V ≤ V_{VM} ≤ 11 V and 1.65 V ≤ V_{VCC} ≤ 5.5 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical values are at T_J = 27°C, V_{VM} = 5 V, V_{VCC} = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{OFF}	Current regulation off time			20		µs
t_{BLANK}	Current regulation blanking time			1.8		µs
t_{DELAY}	Current sense delay time			1.5		µs
t_{DEG}	Current regulation and stall detection deglitch time			2		µs
HARDWARE STALL DETECTION (TINRUSH)						
$V_{TINRUSH\_trip}$	Threshold voltage for setting t_{INRUSH} timing		0.97	1	1.03	V
$I_{TINRUSH}$	Current sourced out of the TINRUSH pin	Inputs transition to a state other than IN1=IN2=0, $V_{TINRUSH}$ < $V_{TINRUSH\_trip}$	8	10	12	µA
$t_{discharge}$	TINRUSH capacitor discharge time	0.8 nF ≤ $C_{TINRUSH}$ ≤ 0.8 µF			100	µs
t_{STALL_RETRY}	IN1/IN2 = 0/0 duration to recover from Stall (retry type)		350		900	µs
PROTECTION CIRCUITS						
V_{UVLO_VM}	VM supply undervoltage lockout (UVLO), DSG	Supply rising			1.65	V
		Supply falling	1.30			V
V_{UVLO_VCC}	VCC supply undervoltage lockout (UVLO), RTE	Supply rising			1.65	V
		Supply falling	1.30			V
V_{UVLO_HYS}	Supply UVLO hysteresis	Rising to falling threshold		150		mV
t_{UVLO}	Supply undervoltage deglitch time	V_{VM} falling (DSG) or V_{VCC} falling (RTE) to OUTx disabled		10		µs
I_{OCP}	Overcurrent protection trip point, 350mA to 2A		4			A
I_{OCP}	Overcurrent protection trip point, 60mA to 350mA		0.8			A
I_{OCP}	Overcurrent protection trip point, 10mA to 60mA		0.16			A
t_{OCP}	Overcurrent protection deglitch time			4.2		µs
t_{RETRY}	Fault retry time			1.5		ms
T_{TSD}	Thermal shutdown temperature		165	175	185	°C
T_{HYS}	Thermal shutdown hysteresis			17		°C

7.6 Timing Diagrams

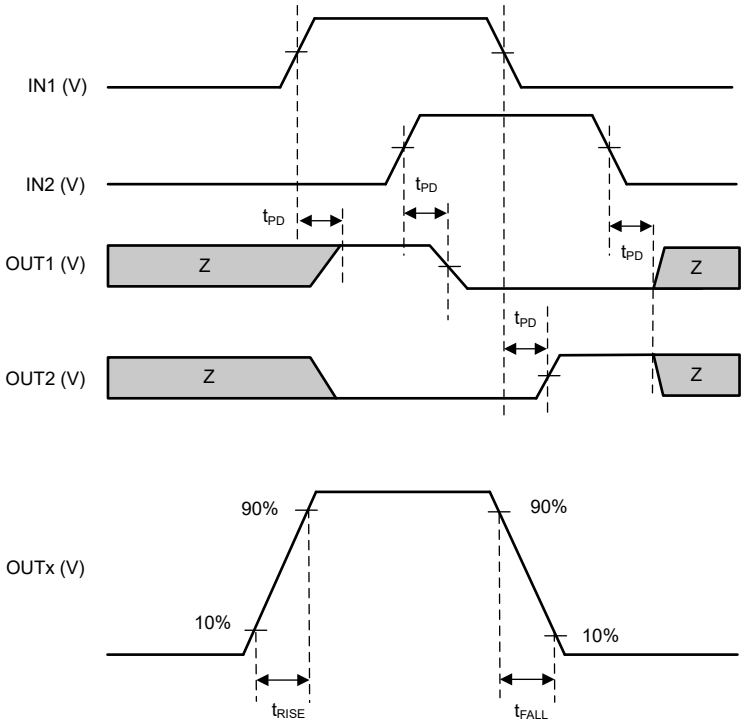


図 7-1. Input-to-Output Timing

7.7 Typical Operating Characteristics

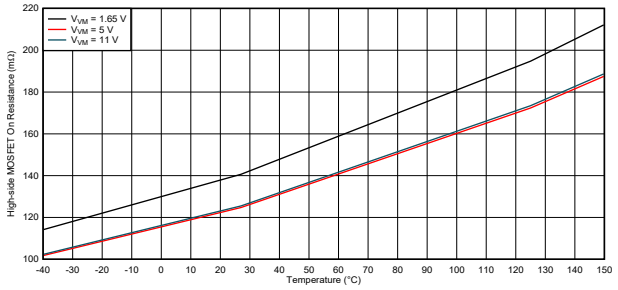


図 7-2. High-Side MOSFET ON Resistance (DSG Package)

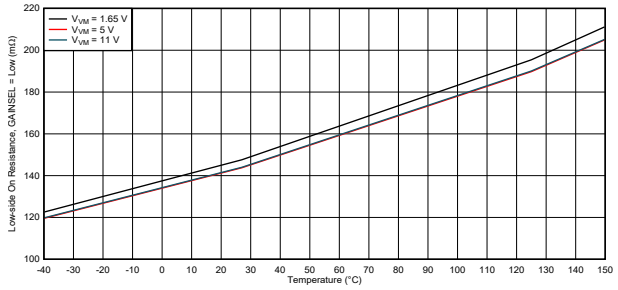


図 7-3. Low-Side MOSFET ON Resistance with GAINSEL = Low (DSG Package)

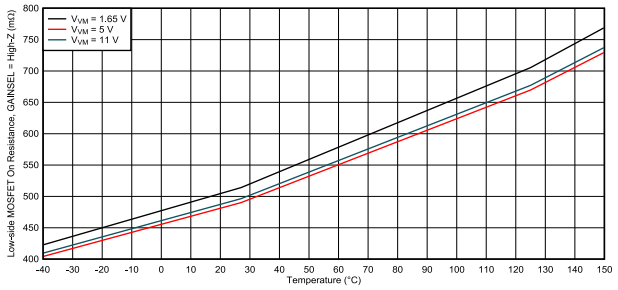


図 7-4. Low-Side MOSFET ON Resistance with GAINSEL = High-Z (DSG Package)

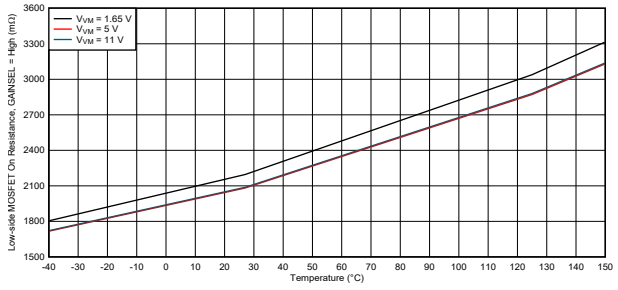


図 7-5. Low-Side MOSFET ON Resistance with GAINSEL = High (DSG Package)

7.7 Typical Operating Characteristics (continued)

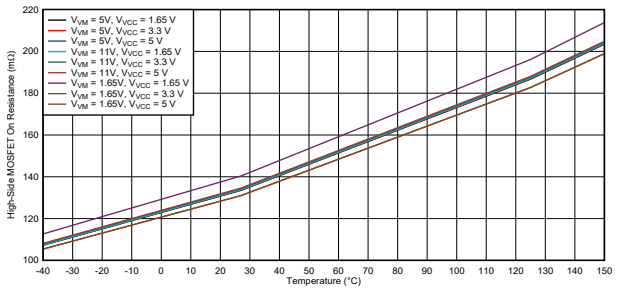


図 7-6. High-Side MOSFET ON Resistance (RTE Package)

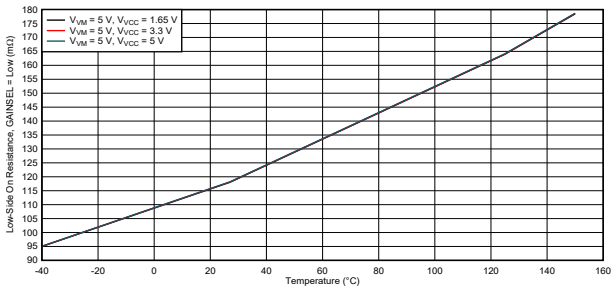


図 7-7. Low-Side MOSFET ON Resistance with GAINSEL = Low (RTE Package)

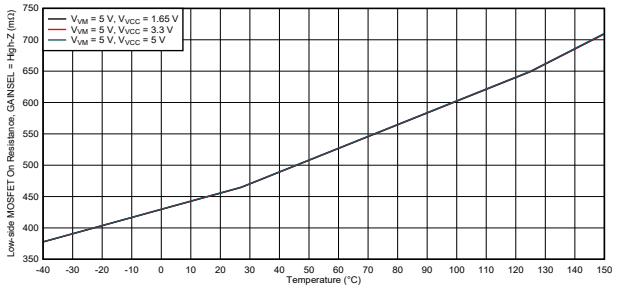


図 7-8. Low-Side MOSFET ON Resistance with GAINSEL = High-Z (RTE Package)

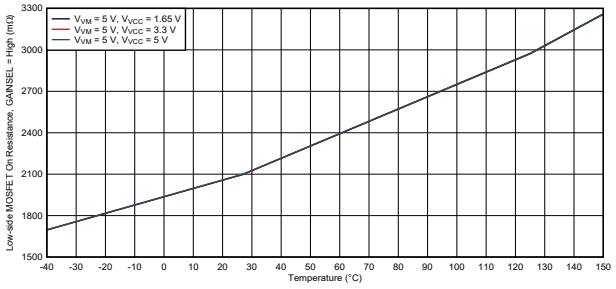


図 7-9. Low-Side MOSFET ON Resistance with GAINSEL = High (RTE Package)

8 Detailed Description

8.1 Overview

DRV8213 is a full-bridge driver with integrated current sense, current regulation, and current sense output. To reduce area and external components on a printed circuit board, the device integrates a charge pump regulator and capacitors. In the WQFN (RTE) package, the separate full-bridge (VM) and logic (VCC) supplies allow the full-bridge supply voltage to drop to 0 V without significant impact to $R_{DS(ON)}$ and without triggering UVLO as long as the VCC supply is stable. In the WSON (DSG) package, a single power input (VM) serves as both device power and the full-bridge supply for small design size. An auto-sleep mode reduces microcontroller GPIO connections by eliminating a disable/sleep pin and automatically putting the device into a low-power sleep mode when the PWM inputs remain low for $t_{AUTOSLEEP}$.

The DRV8213 uses a standard 2-pin (IN1/IN2) PWM interface. The IN1/IN2 pins control the full bridge, which consists of four N-channel MOSFETs that have a typical $R_{DS(ON)}$ of 240 mΩ (including one high-side and one low-side FET). Motor speed can be controlled with pulse-width modulation (PWM), at frequencies between 0 to 100 kHz.

The integrated current regulation feature limits motor current to a predefined maximum based on the VREF and IPROPI settings. The IPROPI signal can provide current feedback to a microcontroller during both the drive and brake/slow-decay states of the H-bridge.

The gain select (GAINSEL) feature allows high accuracy current sensing down to 10 mA average motor current. The $R_{DS(ON)}$ of the low-side MOSFET and the overcurrent protection limit changes according to the GAINSEL setting, thereby leading to optimized answers for different applications and different values of motor current.

In the WQFN package (RTE), the DRV8213 has additional pins to configure a hardware stall detection feature based on the IPROPI current sensing signal.

The integrated protection features protect the device in the case of a system fault. These include undervoltage lockout (UVLO), overcurrent protection (OCP), and overtemperature shutdown (TSD).

8.2 Functional Block Diagram

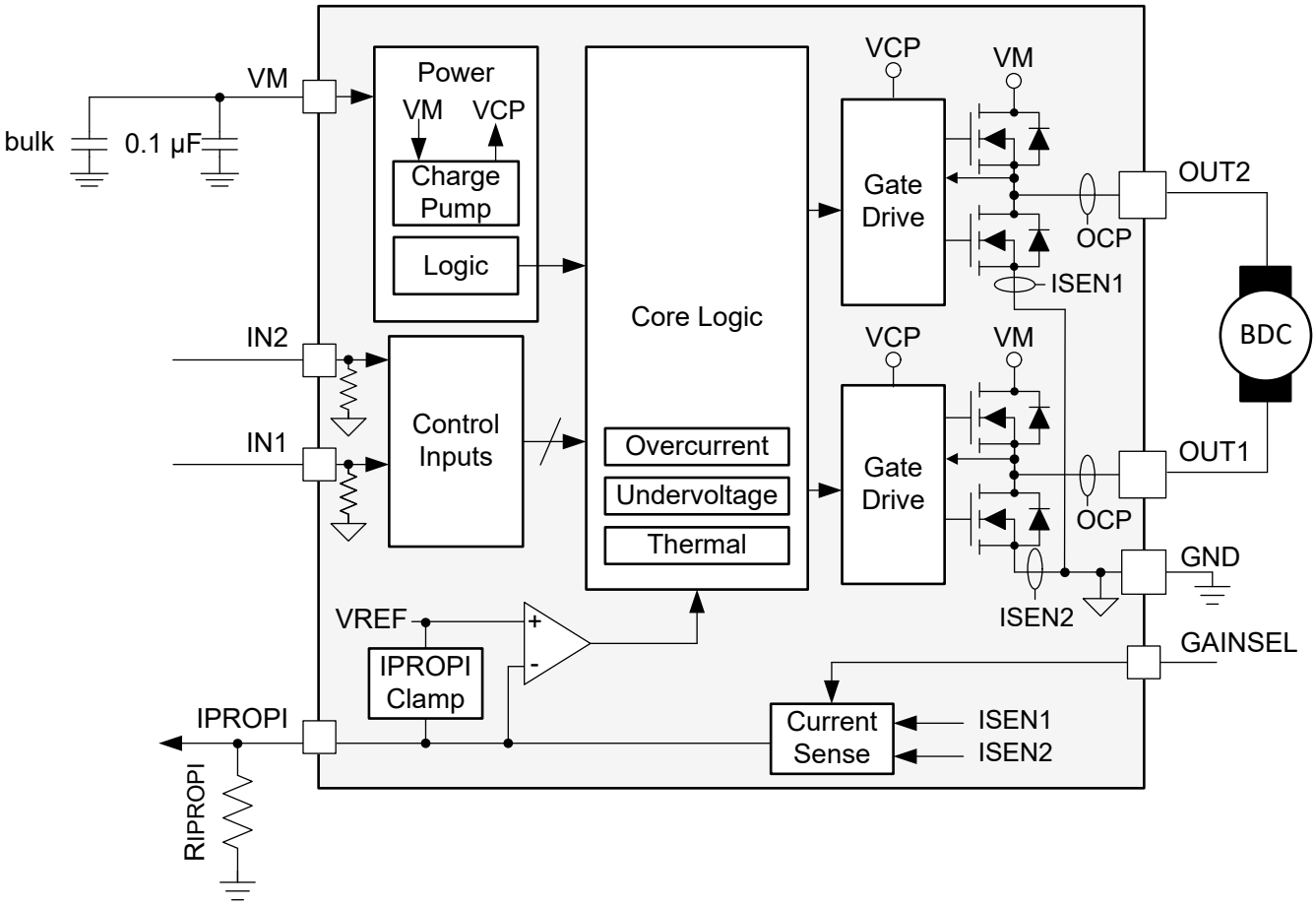


図 8-1. DRV8213 in WSON (DSG) package with single supply pin

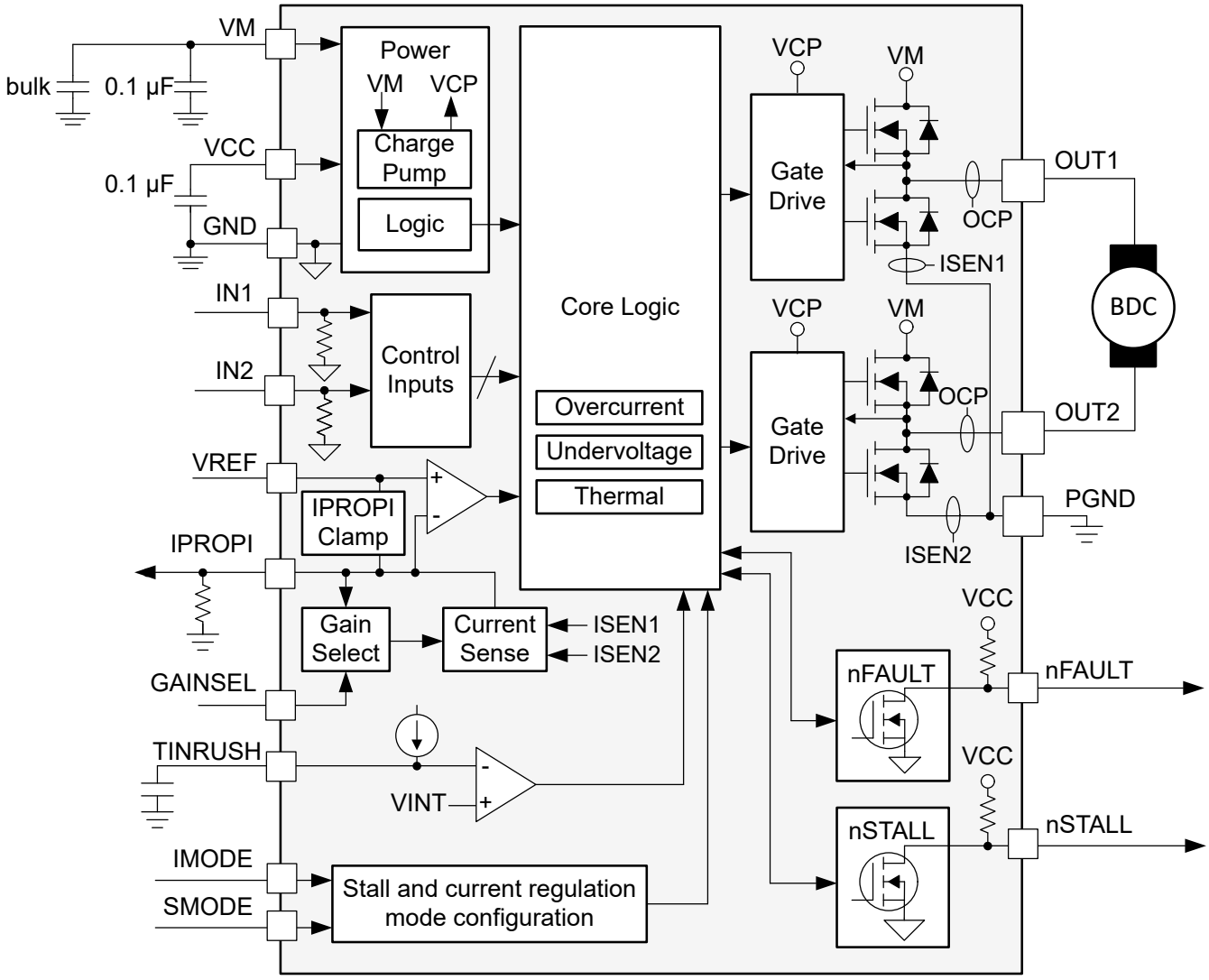


図 8-2. DRV8213 in WQFN (RTE) package with stall detection and dual supply pins

8.3 External Components

表 8-1 lists the recommended external components for the device.

表 8-1. Recommended external components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_{VM1}	VM	GND	0.1-µF, low ESR ceramic capacitor, VM-rated
C_{VM2}	VM	GND	セクション 10.1, VM-rated
C_{VCC}	VCC	GND	0.1-µF, low ESR ceramic capacitor, VM-rated
R_{IPROPI}	IPROPI	GND	Resistor from IPROPI pin to GND, sets the current regulation level
C_{INRUSH}	TINRUSH	GND	Sets the inrush current blanking time
R_{nFAULT}	VCC	nFAULT	10 kΩ
R_{nSTALL}	VCC	nSTALL	10 kΩ

8.4 Feature Description

8.4.1 Bridge Control

The DRV8213 output consists of four N-channel MOSFETs designed to drive high current. These outputs are controlled by the two PWM inputs IN1 and IN2 as listed in 表 8-2.

表 8-2. H-Bridge Control

IN1	IN2	OUT1	OUT2	DESCRIPTION
0	0	High-Z	High-Z	Coast; H-bridge disabled to High-Z (sleep entered after $t_{AUTOSLEEP}$)
0	1	L	H	Reverse (Current OUT2 → OUT1)
1	0	H	L	Forward (Current OUT1 → OUT2)
1	1	L	L	Brake; low-side slow decay

The inputs can be set to static voltages for 100% duty cycle drive, or they can be pulse-width modulated (PWM) for variable motor speed. When using PWM, switching between driving and braking typically works best. For example, to drive a motor forward with 50% of the maximum RPM, IN1 = 1 and IN2 = 0 during the driving period, and IN1 = 1 and IN2 = 1 during the other period. Alternatively, the coast mode (IN1 = 0, IN2 = 0) for *fast current decay* is also available. 図 8-3 shows how the motor current flows through the H-bridge. The input pins can be powered before VM or VCC are applied.

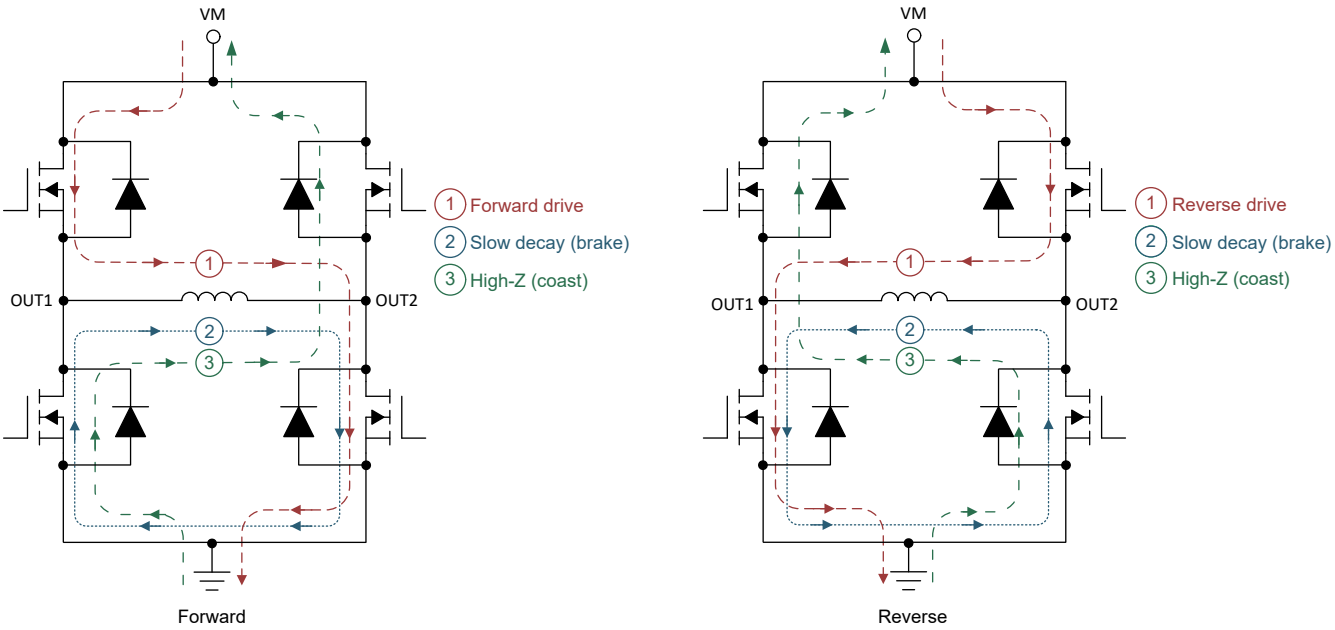


図 8-3. H-Bridge Current Paths

When an output changes from driving high to driving low, or driving low to driving high, dead time is automatically inserted to prevent shoot-through. The t_{DEAD} time is the time in the middle when the output is High-Z. If the output pin is measured during t_{DEAD}, the voltage depends on the direction of current. If the current is leaving the pin, the voltage is a diode drop below ground. If the current is entering the pin, the voltage is a diode drop above VM. This diode is the body diode of the high-side or low-side FET.

The propagation delay time (t_{PD}) is measured as the time between an input edge to output change. This time accounts for input deglitch time and other internal logic propagation delays. The input deglitch time prevents noise on the input pins from affecting the output state. Additional output slew delay timing accounts for FET turn on or turn off times (t_{RISE} and t_{FALL}).

8.4.2 Current Sense and Regulation (IPROPI)

The DRV8213 device integrates current sensing, regulation, and current sense feedback. The internal current mirror allows the device to sense the output current without an external sense resistor or sense circuitry, thereby reducing system size, cost, and complexity. The current regulation feature allows for the device to limit the output current in the case of motor stall or high torque events and give detailed feedback to the controller about the load current using the IPROPI output. 図 8-4 shows the IPROPI timings specified in the Electrical Characteristics table.

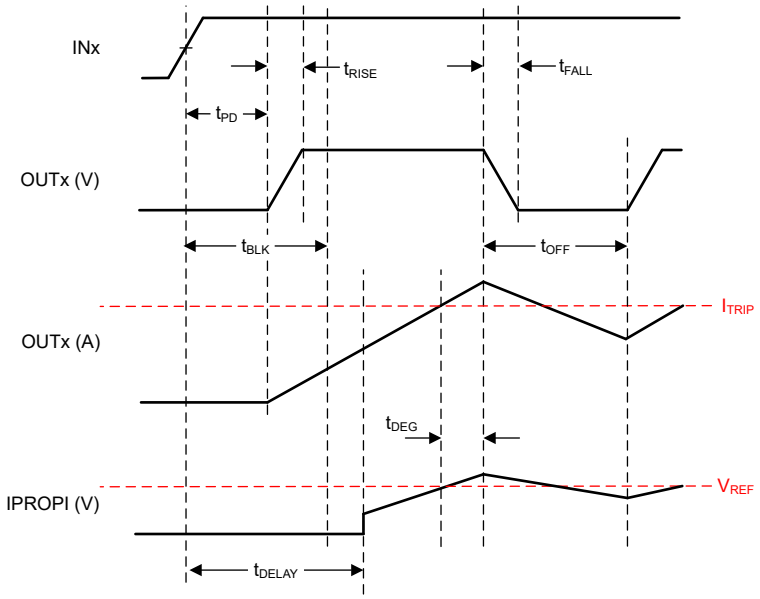


図 8-4. Detailed IPROPI Timing Diagram

8.4.2.1 Current Sensing and Current Mirror Gain Selection

The IPROPI pin outputs an analog current proportional to the current flowing through the low-side power MOSFETs in the H-bridge and scaled by the current mirror gain (A_{IPROPI}). The IPROPI output current can be calculated by 式 1. The I_{LSx} in 式 1 is only valid when the current flows from drain to source in the low-side MOSFET. If current flows from source to drain or through the body diode, the value of I_{LSx} for that channel is zero. For instance, if the bridge is in the brake, slow-decay state, then the current out of IPROPI is only proportional to the current in one of the low-side MOSFETs.

$$I_{PROPI}\ (\mu A) = (I_{LS1} + I_{LS2})\ (A) \times A_{IPROPI}\ (\mu A/A) \quad (1)$$

The A_{ERR} parameter in the Electrical Characteristics table is the error associated with the A_{IPROPI} gain. A_{ERR} indicates the combined effect of offset error added to the I_{OUT} current and gain error.

Depending on the application, high accuracy current sense output is required down to 10 mA current. The GAINSEL feature allows optimizing the design for different end applications by reducing OCP limit and increasing current mirror gain at lower motor currents. The current mirror gain A_{IPROPI} depends on the GAINSEL pin setting, as shown in 表 8-3.

表 8-3. GAINSEL Setting

GAINSEL	A_{IPROPI}	Recommended Current Range	Low-side FET $R_{DS(ON)}$	Minimum OCP Limit
Low	205 µA/A	350 mA to 2 A	120 mΩ	4 A
High-Z	1050 µA/A	60 mA to 350 mA	460 mΩ	800 mA
High	4900 µA/A	10 mA to 60 mA	2100 mΩ	160 mA

The motor current is measured by an internal current mirror architecture on the low-side FETs which removes the need for an external power sense resistor as shown in 図 8-5. The current mirror architecture senses motor winding current in both the drive and brake low-side slow-decay periods, therefore allowing continuous current monitoring in typical bidirectional brushed DC motor applications. In coast mode, the current is freewheeling and cannot be sensed because the current flows from source to drain. However, the current can be sampled by briefly reenabling the driver in either drive or slow-decay modes and measuring the current before switching back to coast mode again.

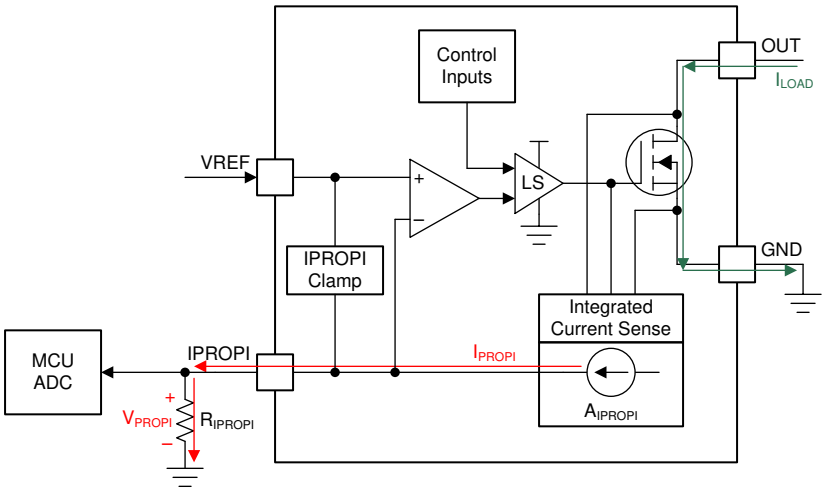


図 8-5. Integrated Current Sensing

The IPROPI pin is connected to an external resistor (R_{IPROPI}) to ground to generate a proportional voltage (V_{IPROPI}) on the IPROPI pin with the I_{IPROPI} analog current output. This allows for the load current to be measured as the voltage drop across the R_{IPROPI} resistor with a standard analog to digital converter (ADC). The R_{IPROPI} resistor can be sized based on the expected load current in the application so that the full range of the controller ADC is utilized.

Additionally, the DRV8213 device implements an internal IPROPI voltage clamp circuit to limit V_{IPROPI} with respect to V_{VREF} on the VREF pin and protect the external ADC in case of output overcurrent or unexpected high current events. For the DSG package, V_{VREF} is set at 510 mV internally. TI recommends designing for at least 1.25 V of headroom between V_{VM} and the maximum V_{IPROPI} voltage to be measured by the ADC, V_{IPROPI_MAX}. This maintains good accuracy across the range of VIPROPI voltages measured by the ADC. For instance, if V_{VM} is 4.55 V to 11 V, V_{IPROPI_MAX} can be as high as 3.3 V. However, if V_{VM} is 3.3 V, then VIPROPI has good accuracy up to 2.05 V.

The corresponding IPROPI voltage to the output current can be calculated by 式 2.

$$V_{IPROPI}\ (V) = I_{PROPI}\ (A) \times R_{IPROPI}\ (\Omega) \quad (2)$$

The IPROPI output bandwidth is limited by the sense delay time (t_{DELAY}) of the internal current sensing circuit. This time is the delay from the low-side MOSFET enable command (from the INx pins) to the IPROPI output being ready.

If the device is alternating between drive and slow-decay (brake) in an H-bridge PWM pattern then the low-side MOSFET sensing the current is continuously on and the sense delay time has no impact to the IPROPI output. If a command on the INx pins disables the low-side MOSFETs (according to the logic tables in セクション 8.4.1), the IPROPI output disables with the input logic signal. Although the low-side MOSFETs still conduct current as the MOSFETs disable according to the device slew rate (noted in the Electrical Characteristics table by t_{RISE} time), IPROPI does not represent the current in the low-side MOSFETs during this turnoff time.

8.4.2.2 Current Regulation

The DRV8213 device integrates current regulation using a fixed off-time current chopping scheme, as shown in 図 8-6. This allows the device to limit the output current in case of motor stall, high torque, or other high current load events without involvement from the external controller.

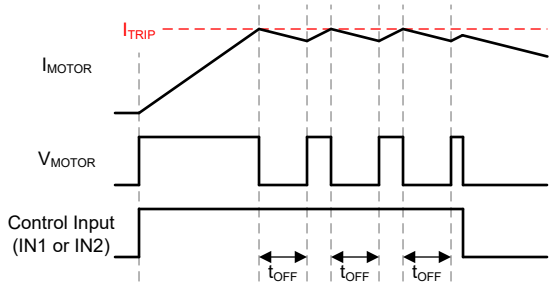


図 8-6. Off-Time Current-Regulation

The current chopping threshold (I_{TRIP}) is set through a combination of the VREF voltage (V_{VREF}) and IPROPI output resistor (R_{IPROPI}). This is done by comparing the voltage drop across the external R_{IPROPI} resistor to V_{VREF} with an internal comparator.

$$I_{TRIP}\ (A) \times A_{IPROPI}\ (\mu A/A) = V_{VREF}\ (V) / R_{IPROPI}\ (\Omega) \quad (3)$$

For example, if V_{VREF} = 3.3 V, R_{IPROPI} = 8.06 kΩ, and A_{IPROPI} = 205 µA/A, then I_{TRIP} will be approximately 2 A.

V_{VREF} must be lower than V_{VM} by at least 1.25 V. The maximum recommended value of V_{VREF} is 3.3 V.

As mentioned before, for DSG package, V_{VREF} is internally fixed at 510 mV. For RTE package as well, if SMODE is left OPEN, V_{VREF} is internally fixed at 510 mV.

The fixed off-time current chopping scheme supports up to 100% duty cycle current regulation since the H-bridge automatically enables after the t_{OFF} period and does not require a new control input edge on the INx pins to reset the outputs. When the motor current exceeds the I_{TRIP} threshold, the outputs will enter a current chopping mode with a fixed off time (t_{OFF}). During t_{OFF}, the H-bridge enters a brake/low-side slow decay state (both low-side MOSFETs ON) for t_{OFF} duration after I_{OUT} exceeds I_{TRIP}. After t_{OFF}, the outputs re-enable according to the control inputs if I_{OUT} is less than I_{TRIP}. If I_{OUT} is still greater than I_{TRIP}, the H-bridge enters another period of brake/low-side slow decay for t_{OFF} after a drive time of t_{BLANK}.. If the state of the INx control pins changes during the t_{OFF} time, the remainder of the t_{OFF} time is ignored, and the outputs will again follow the inputs.

The I_{TRIP} comparator has both a blanking time (t_{BLK}) and a deglitch time (t_{DEG}). The internal blanking time helps to prevent voltage and current transients during output switching from effecting the current regulation. These transients may be caused by a capacitor inside the motor or on the connections to the motor terminals. The internal deglitch time ensures that transient conditions do not prematurely trigger the current regulation. In certain cases where the transient conditions are longer than the deglitch time, placing a 10-nF capacitor on the IPROPI pin, close to the device, will help filter the transients on IPROPI output so current regulation does not prematurely trigger. The capacitor value can be adjusted as needed, however large capacitor values may slow down the response time of the current regulation circuitry.

The IMODE pin determines the behavior of current regulation in the motor driver. When IMODE is logic low (IMODE = 0), current regulation is disabled. When IMODE is floating (IMODE =Z), the device only performs current regulation during the t_{INRUSH} time when stall detection is enabled. This functionality relates to the hardware stall detection feature described in セクション 8.4.3. When IMODE is logic high (IMODE = 1), current regulation is enabled at all times. 表 8-4 summarizes the IMODE pin settings.

表 8-4. IMODE configuration

IMODE	nSTALL	Description
Low	X	No current regulation at any time

表 8-4. IMODE configuration (continued)

IMODE	nSTALL	Description
High-Z	Low	Current regulation at all times
High-Z	High	Current regulation during t_{INRUSH} only
High	X	Current regulation at all times

8.4.3 Hardware Stall Detection

The DRV8213 integrates a hardware stall detection feature available in the RTE package variant. The principle of the stall detection scheme relies on the fact that motor current increases during stall conditions. The DRV8213 compares the voltage on the IPROPI pin to the voltage on the VREF pin (or 510 mV as applicable) to determine whether a stall condition has occurred. The following paragraphs describe how to configure the device pins for the desired stall detection response. For information on implementing stall detection in the DSG package variant, see セクション 9.2.1.3.1.2.

The nSTALL output is pulled low when stall is detected. The nSTALL pin status is latched at power-up. It requires a pull-up resistor to VCC and pulls low when a stall condition occurs. This pin can be connected to the nFAULT pin so both pins share the same pullup resistor. Combining nFAULT and nSTALL signals reduces board area needed by external components and number of input pins on the controller to detect fault and stall conditions. By having separate pullup resistors for the nSTALL and nFAULT, the microcontroller can detect a device fault separate from a stall condtition using two input pins. Connecting nSTALL directly to GND disables stall detection. 表 8-5 summarizes the nSTALL pin settings.

表 8-5. nSTALL configuration

nSTALL	Description
0 V	Stall detection disabled. Float TINRUSH. If IMODE = High-Z, current regulation will occur at all times when $V_{IPROPI} \geq V_{VREF}$.
Pull-up resistor to VCC	Stall detection enabled. Pin pulls low to indicate a stall.

The **IPROPI** pin provides the current sense signal for the hardware stall detection feature. The **VREF** pin sets the I_{TRIP} current level at which a stall condition is detected. For DSG package, or RTE package and SMODE = High-Z, V_{VREF} is internally fixed at 510 mV. When $V_{IPROPI} \geq V_{VREF}$, then $I_{OUT} \geq I_{TRIP}$, and the device will detect a stall condition if the t_{INRUSH} time has passed. The IPROPI and VREF pins are also responsible for current regulation, as described in セクション 8.4.2.

The **TINRUSH** pin sets the amount of time that the stall detection scheme will ignore the inrush current during motor startup (t_{INRUSH}). When the input pins transition from the state IN1 = IN2 = logic low to any other logic combination, the TINRUSH pin sources 10 µA of current into the capacitor (C_{INRUSH}) connected from TINRUSH pin to ground. Once the voltage of the TINRUSH pin exceeds 1 V, the device discharges the capacitor in less than 100 µs. The capacitor charging time is internally multiplied by 65 to determine the t_{INRUSH} time. After t_{INRUSH} time expires, the DRV8213 indicates a stall condition the next time V_{IPROPI} is greater than or equal to V_{VREF}.

The following conditions cause the stall detection scheme to ignore the inrush current for t_{INRUSH} time -

- Power-up of the DRV8213
- Recovering from faults
- After device exits from sleep mode
- After recovering from stall, as explained in 表 8-6

Use the following formula to select the C_{INRUSH} capacitor -

$t_{INRUSH} = 6.5 \times 10^6 \times C_{INRUSH}$

The **SMODE** pin sets the device's response to a stall condition. The device decides that a stall condtion has occurred when V_{IPROPI} is greater than or equal to V_{VREF} and the t_{INRUSH} time has elapsed. When SMODE = logic low, the outputs disable, and the nSTALL pin latches low. When SMODE = logic high, the nSTALL pin still latches low, but the outputs continue to drive current into the motor. When SMODE = Hi-z, the device uses

internal V_{VREF} (510 mV) for stall detection, the nSTALL pin still latches low, but the outputs continue to drive current into the motor. 表 8-6 summarizes the SMODE pin settings.

表 8-6. SMODE configuration

SMODE	Description	Recovery from Stall Condition
0	Latched disable with indication: the OUTx pins disable and the nSTALL pin pulls low.	To recover from this condition, device needs to enter sleep mode. nSTALL will go high after IN1 and IN2 are both low for t_{SLEEP}. After waking up from sleep mode, the stall detection scheme ignores the inrush current for t_{INRUSH} time.
1	Indication only: the OUTx pins remain active and the nSTALL pin pulls low.	nSTALL goes high if stall condition is not observed and if IN1 and IN2 are both low for stall retry time (t_{STALL_RETRY}). After t_{INRUSH} time, if motor current is still higher than I_{TRIP}, nSTALL pin is pulled low again.
Hi-z	Indication only: the OUTx pins remain active and the nSTALL pin pulls low. Device uses internal V_{VREF} (510 mV) for stall detection.	

The stall retry time (t_{STALL_RETRY}) is implemented such that it is always lower than the autosleep turnoff time ($t_{AUTOSLEEP}$).

The **IMODE** pin determines the behavior of current regulation in the motor driver. When IMODE is floating (IMODE = High-Z), the device only performs current regulation during the t_{INRUSH} time. 表 8-4 summarizes the IMODE pin settings. For more details on current regulation, see セクション 8.4.2.2.

The following diagrams show example timing diagrams for different configurations of the hardware stall detection feature.

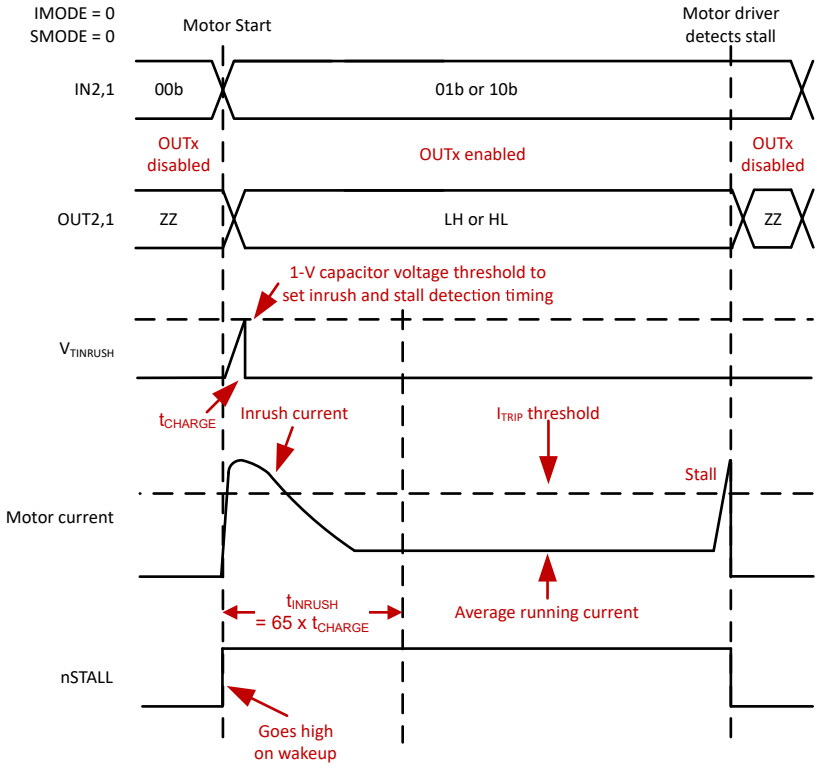


図 8-7. Stall Detection with Latched Disable

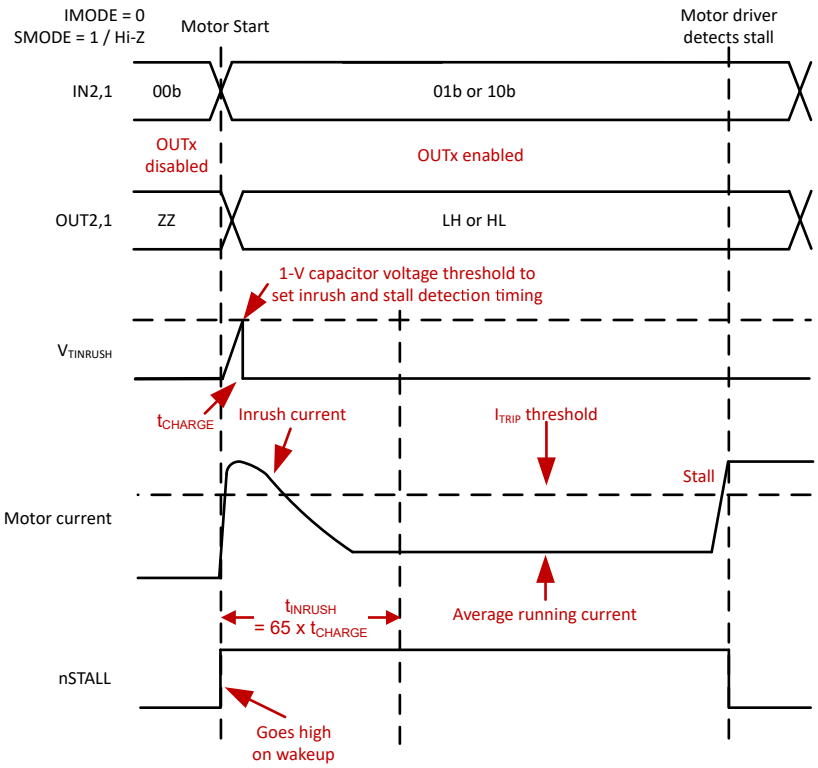


図 8-8. Stall Detection with nSTALL indication only

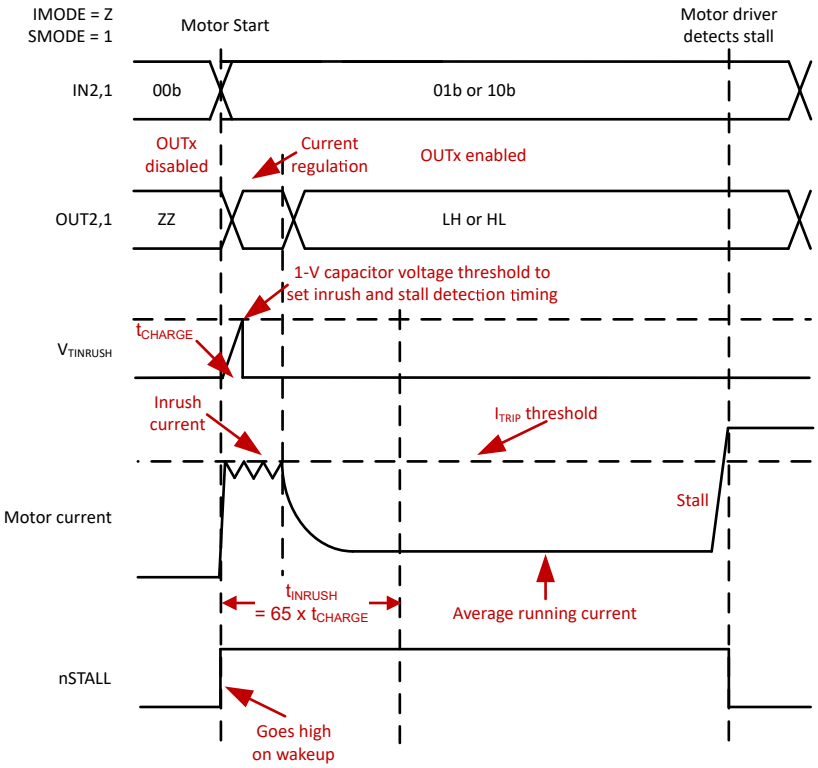


図 8-9. Stall regulation with current regulation during inrush

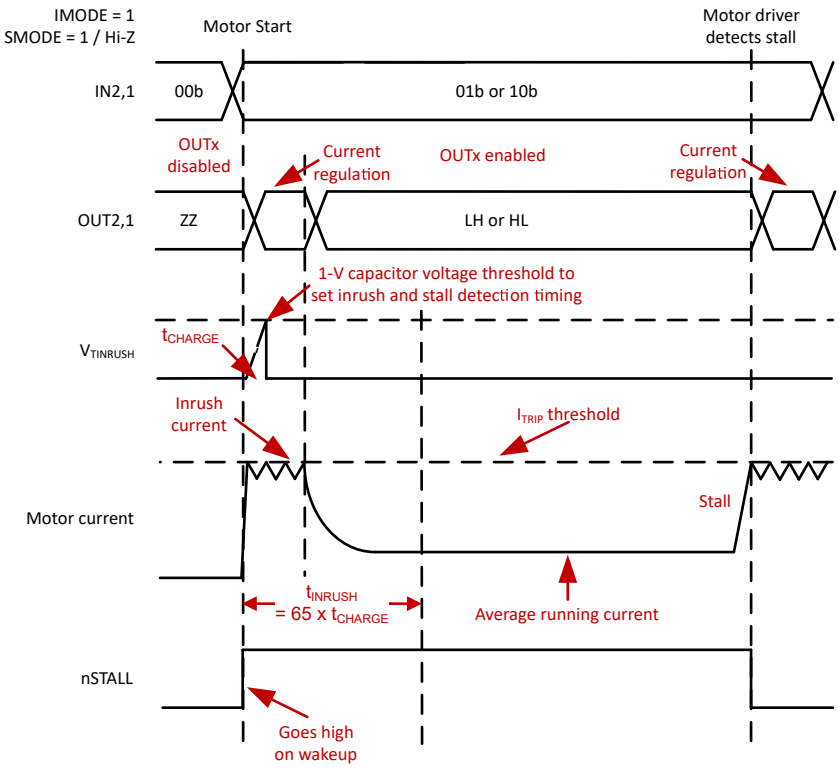


図 8-10. Stall detection with current regulation

8.4.4 Protection Circuits

The DRV8213 device is fully protected against supply undervoltage, overcurrent, and overtemperature events.

8.4.4.1 Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by limiting the gate drive internally. If this analog current limit persists for longer than the OCP deglitch time (t_{OCP}), all FETs in the H-bridge will disable and nFAULT is pulled low. The driver re-enables after the fault retry period (t_{RETRY}) has passed. If the fault condition is still present, the cycle repeats as shown in 図 8-11.

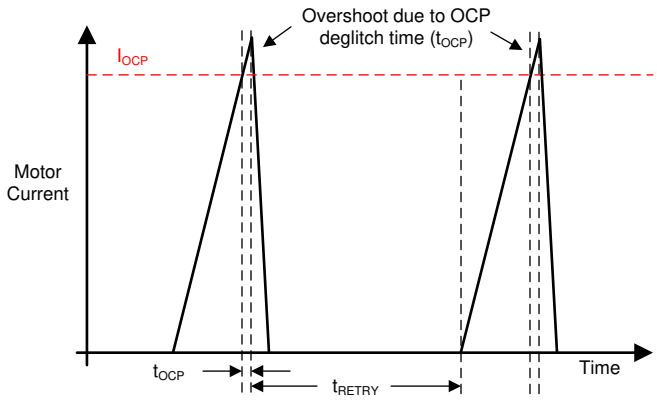


図 8-11. OCP Operation

Overcurrent conditions are detected independently on both high- and low-side FETs. This means that a short to ground, supply, or across the motor winding will all result in an overcurrent shutdown. Overcurrent protection does not use the current sense circuitry used for current regulation, so it functions regardless of VREF and IPROPI settings.

8.4.4.2 Thermal Shutdown (TSD)

If the die temperature exceeds the thermal shutdown temperature threshold (T_{TSD}), all FETs in the H-bridge are disabled and nFAULT is pulled low. The driver re-enables after the fault retry period (t_{RETRY}) has passed. If the fault condition is still present, the cycle repeats.

8.4.4.3 VM Undervoltage Lockout (UVLO)

Whenever the supply voltage falls below the UVLO falling threshold voltage, V_{UVLO}, all circuitry in the device is disabled, the output FETS are disabled, all internal logic is reset and nFAULT is pulled low. When powered by split supplies (RTE package only), the UVLO triggers when the VCC pin voltage drops below V_{UVLO_VCC} falling threshold. This allows the VM supply to dip all the way to 0 V. When operating from a single supply (DSG package only), the UVLO triggers when the VM pin voltage drops below V_{UVLO_VM} falling threshold. Normal operation resumes when the supply voltage rises above the V_{UVLO} rising threshold as shown in 図 8-12. 表 8-7 summarizes the conditions when the device enters UVLO.

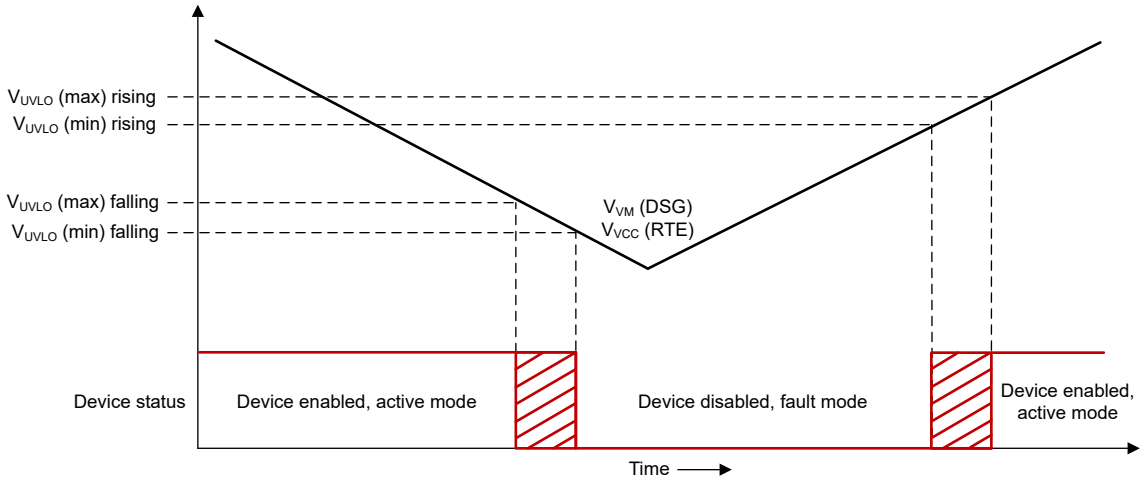


図 8-12. UVLO Operation

表 8-7. UVLO response conditions

Package variant	V_{VM}	V_{VCC}	Device Response	IPROPI
RTE	0 V to V_{VM_MAX}	<1.65 V	UVLO	Not available
	0 V to V_{VM_MAX}	>1.65 V	Normal Operation	Available for V_{VM} > 1.65 V
DSG	<1.65 V	N/A	UVLO	Not available
	1.65 V to V_{VM_MAX}	N/A	Normal Operation	Available

8.5 Device Functional Modes

表 8-8 summarizes the DRV8213 functional modes described in this section.

表 8-8. Modes of Operation

MODE	CONDITION	H-BRIDGE	INTERNAL CIRCUITS
Active Mode	IN1 or IN2 = logic high	Operating	Operating
Low-Power Sleep Mode	IN1 = IN2 = logic low	Disabled	Disabled
Fault Mode	Any fault condition met	Disabled	See 表 8-9

8.5.1 Active Mode

After the supply voltage on the VM pin (DSG package) or VCC pin (RTE package) has crossed the rising undervoltage threshold V_{UVLO}, the INx pins are in a state other than IN1 = 0 & IN2 = 0, and t_{WAKE} has elapsed, the device enters active mode. In this mode, the full-bridge, charge pump, and internal logic are active and the device is ready to receive inputs.

In the RTE package, when V_{VCC} < V_{VM}, the DRV8213 draws active current from the VM pin rather than the VCC pin (I_{VM}). During this operating condition, I_{VCC} is typically less than 500 nA. When V_{VCC} > V_{VM}, the device draws active current from the VCC pin, and the VM pin will only draw current required by the load. When V_{VCC} = V_{VM}, the active current may be drawn from either supply pin. The active current is typically less than 1.9 mA.

8.5.2 Low-Power Sleep Mode

When the IN1 and IN2 pins are both low for time t_{SLEEP}, the DRV8213 device enters a low-power sleep mode. In sleep mode, the outputs remain High-Z and the device draws minimal current from the supply pin (I_{VMQ} or I_{VCCQ}). After any of the input pins are set high for longer than the duration of t_{WAKE}, the device becomes fully operational. 図 8-13 shows an example timing diagram for entering and leaving sleep mode.

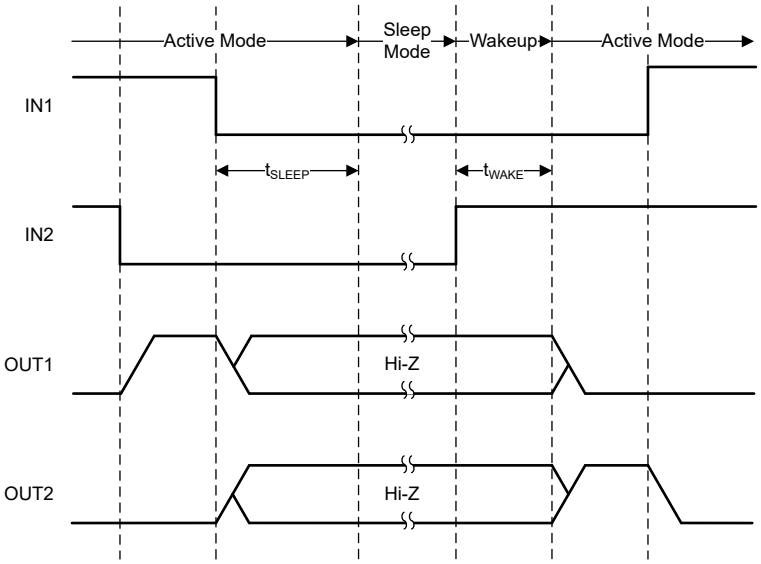


図 8-13. Sleep Mode Entry and Wakeup Timing Diagram

8.5.3 Fault Mode

The DRV8213 device enters fault mode when it encounters a fault condition. This protects the device and the load on the outputs. 表 8-9 describes the device behavior in the fault mode which depends on the fault condition. The device will leave the fault mode and re-enter the active mode when the system meets the recovery condition.

表 8-9. Fault Conditions Summary

FAULT	FAULT CONDITION	ERROR REPORT	FULL-BRIDGE	INTERNAL CIRCUITS	RECOVERY CONDITION
VM undervoltage (UVLO), DSG	$V_{VM} < V_{UVLO\_VM}$ Falling	nFAULT	Disabled	Disabled	$V_{VM} > V_{UVLO\_VM}$ Rising
VCC undervoltage (UVLO), RTE	$V_{VCC} < V_{UVLO\_VCC}$ Falling	nFAULT	Disabled	Disabled	$V_{VCC} > V_{UVLO\_VCC}$ Rising
Overcurrent (OCP)	$I_{OUT} > I_{OCP}$	nFAULT	Disabled	Operating	$I_{OUT} < I_{OCP}$
Thermal Shutdown (TSD)	$T_J > T_{TSD}$	nFAULT	Disabled	Operating	$T_J < T_{TSD} – T_{HYS}$

8.6 Pin Diagrams

8.6.1 Logic-Level Inputs

図 8-14 shows the input structure for the logic-level input pins IN1 and IN2.

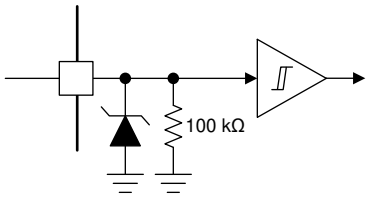


図 8-14. Logic-level input

8.6.2 Tri-Level Input

図 8-15 shows the input structure for the tri-level input pins, GAINSEL, IMODE and SMODE.

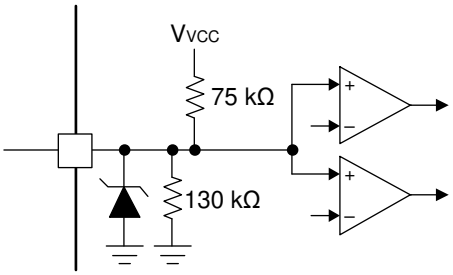


図 8-15. Tri-level input

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DRV8213 is intended to drive one brushed DC motor.

9.2 Typical Application

9.2.1 Brushed DC Motor

A typical application for the DRV8213 is to drive a brushed DC motor using the full-bridge outputs. 図 9-1 shows an example schematic using the DSG package for driving a motor and controlling the driver from a microcontroller (MCU). 図 9-2 shows a schematic example using the RTE package with stall detection disabled. The resistor on the IPROPI pin can provide a voltage signal to the microcontroller analog-to-digital converter (ADC).

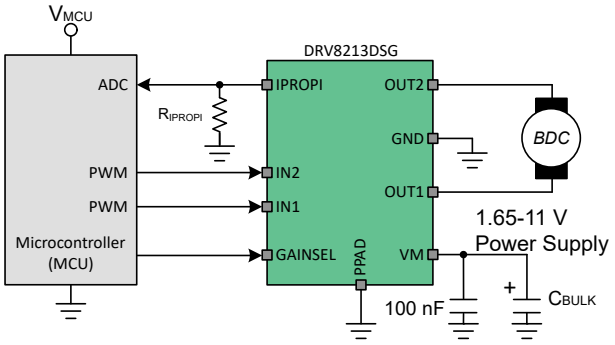


図 9-1. Typical Connections for DSG variant

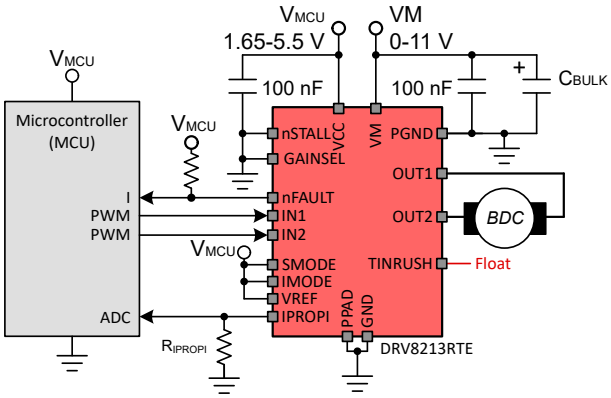


図 9-2. Typical Connections for RTE variant with stall detection disabled

9.2.1.1 Design Requirements

表 9-1 lists example design parameters.

表 9-1. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Motor voltage	V_{VM}	8 V
Average motor current	I_{AVG}	0.8 A
Motor inrush (startup) current	I_{INRUSH}	2.1 A
Motor stall current	I_{STALL}	2.1 A
Motor current trip point	I_{TRIP}	1.9 A
VREF voltage	VREF	3.3 V
IPROPI resistance	R_{IPROPI}	8.45 kΩ
PWM frequency	f_{PWM}	20 kHz

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Motor Voltage

The motor voltage to use depends on the ratings of the motor selected and the desired RPM. A higher voltage spins a brushed DC motor faster with the same PWM duty cycle applied to the power FETs. A higher voltage also increases the rate of current change through the inductive motor windings.

9.2.1.2.2 Motor Current

Motors experience large currents at low speed, initial startup, and stalled rotor conditions. The large current at motor startup is sometimes called inrush current. The current regulation feature in the DRV8213 can help to limit these large currents. Alternatively, the microcontroller may limit the inrush current by ramping the PWM duty cycle during the startup time.

9.2.1.3 Stall Detection

Some applications require stall detection to notify the microcontroller of a locked-rotor/stall condition. A stall could be caused by one of two things: unintended mechanical blockage or the load reaching an end-stop in a constrained travel path. The DRV8213 supports two methods for determing a stall conditions: hardware stall detection and software stall detection. The RTE package supports hardware stall detection by providing additional pins to configure the response of the device to a stall condition as shown in 図 9-3. Both DSG and RTE packages support software stall detection by providing the IPROPI analog current sense feedback to the ADC of a microcontroller as shown in 図 9-1 and 図 9-2.

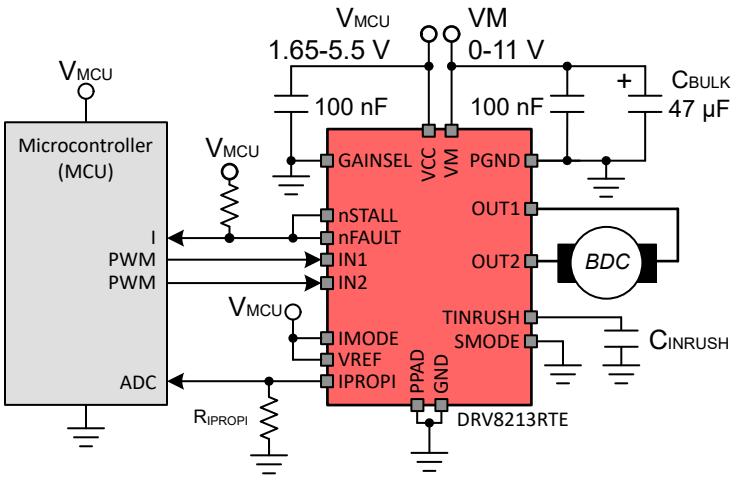


図 9-3. Typical Connections for RTE variant with stall detection enabled

9.2.1.3.1 Detailed Design Procedure

9.2.1.3.1.1 Hardware Stall Detection Application Description

The principle of this stall detection scheme relies on the fact that motor current increases during stall conditions as shown in 図 9-5. The DRV8213 compares the voltage on the IPROPI pin to the voltage on the VREF pin to determine whether a stall condition has occurred. The capacitor on the TINRUSH pin sets the timing, t_{INRUSH}, so the DRV8213 ignores the inrush current at motor startup. The SMODE pin configures how the DRV8213 responds to a stall condition. The IMODE pin configures whether the device regulates current during inrush and stall currents. When a stall condition occures, nSTALL pulls low to indicate the stall event to the microcontroller. セクション 8.4.3 provides full details for configuring the stall detection feature.

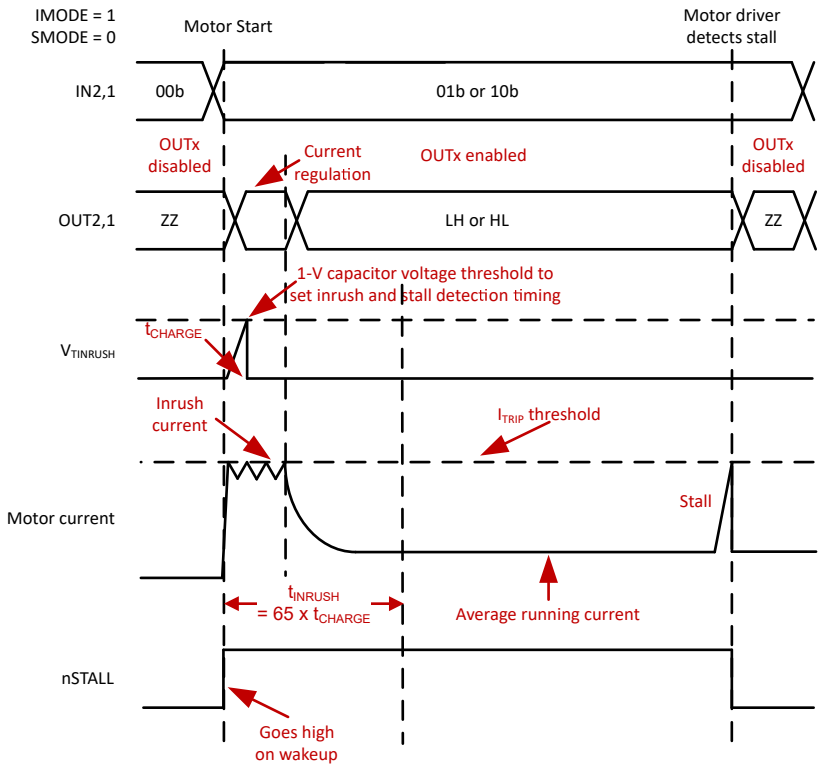


図 9-4. Example timing diagram for hardware stall detection

表 9-2 summarizes stall detection configuration.

表 9-2. Summary table for hardware stall detection pin configuration

nSTALL	TINRUSH	SMODE	Description
GND	Z	X	Stall detection disabled. Float TINRUSH. If IMODE = Z, current regulation occurs at all times when $V_{IPROPI} \geq V_{VREF}$.
Pull-up resistor to VCC	GND	X	TI does not recommend this configuration. t_{INRUSH} corresponds to approximately 6.7s. Device continuously sources 10 uA out of TINRUSH pin into GND. If IMODE = Z, current regulation occurs when $V_{IPROPI} \geq V_{VREF}$.
	Capacitor to GND	0	Latched disable with indication: the OUTx pins disable and the nSTALL pin pulls low after t_{INRUSH} when $V_{IPROPI} \geq V_{VREF}$.
		1 / Z	Indication only: the OUTx pins remain active and the nSTALL pin pulls low after t_{INRUSH} when $V_{IPROPI} \geq V_{VREF}$.
	Z	X	TI does not recommend this configuration. Floating TINRUSH pin effectively sets t_{INRUSH} = 0 seconds. The device responds according to the settings of SMODE and IMODE at all times when $V_{IPROPI} \geq V_{VREF}$.
	VCC	X	TI does not recommend this configuration. Tying TINRUSH to a voltage higher than 1 V effectively sets t_{INRUSH} = 0 seconds. The device draws excessive current from the voltage source due to the TINRUSH discharge path being on.

9.2.1.3.1.1.1 Hardware Stall Detection Timing

Large inrush current occurs during motor start up because motor speed is low. As the motor accelerates, the motor current drops to an average level because the back electromotive force (EMF) in the motor increases with speed. The inrush current should not be mistaken for a stall condition, so the DRV8213 integrates a timing circuit in the RTE package variant to ignore the inrush current during the startup time, t_{INRUSH}. The timing circuit is configured using a capactior, C_{INRUSH}, on the TINRUSH pin. セクション 8.4.3 describes the overall details for using the stall detection feature.

When designing for the t_{INRUSH} time, it is important to include enough margin to account for tolerances and variation in the DRV8213 and the system overall. 式 4 defines the minimum t_{INRUSH} time, t_{INRUSH_min}. The timing t_{INRUSH_motor} should be determined experimentally because it depends on motor parameters, supply voltage, temperature, and mechanical load response times. The $\epsilon_{TINRUSH}$ term accounts for tolerances in the TINRUSH timing circuit and the C_{INRUSH} capacitor.

$$t_{INRUSH\_min} = t_{INRUSH\_motor} \times (1 + \epsilon_{TINRUSH}) \quad (4)$$

式 5 shows the expression for finding $\epsilon_{TINRUSH}$. The tolerance of the 1-V reference on the TINRUSH pin is $\epsilon_{VTINRUSH\_trip}$. This tolerance is 3%, as defined by the minimum and maximum specifications for $V_{TINRUSH\_trip}$ in the Electrical Characteristics table. The tolerance of the 10-µA current source on the TINRUSH pin is $\epsilon_{ITINRUSH}$. This tolerance is 20%, as defined by the minimum and maximum specifications for $I_{TINRUSH}$ in the Electrical Characteristics table. The tolerance of the C_{INRUSH} capacitor is $\epsilon_{CINRUSH}$. This is a percentage defined by the tolerance of the selected C_{INRUSH} capacitor.

$$\epsilon_{TINRUSH} = \sqrt{\epsilon_{VTINRUSH\_trip}^2 + \epsilon_{ITINRUSH}^2 + \epsilon_{CINRUSH}^2} \quad (5)$$

For example, assume t_{INRUSH_motor} = 100 ms and a capacitor with 1% tolerance will be used for C_{INRUSH}. In this case, it can be calculated that the C_{INRUSH} capacitor should be larger than 18.5 nF, so a 22 nF capacitor will be sufficient in this application.

9.2.1.3.1.1.2 Hardware Stall Threshold Selection

The voltage on the VREF pin selects I_{TRIP} threshold which sets the current level for stall detection and current regulation. This threshold should be chosen such that I_{TRIP} is less than the stall current of the motor when current regulation is not used. It should also be set low enough to account for variation in the stall current due to changes in the motor supply voltage, V_{VM}, and temperature. セクション 8.4.2.2 and セクション 8.4.3 provide more details for configuring the voltage on the VREF pin.

9.2.1.3.1.2 Software Stall Detection Application Description

The principle of this stall detection scheme relies on the fact that motor current increases during stall conditions as shown in 図 9-5. To implement stall detection, the microcontroller reads the voltage on the IPROPI pin using an ADC and compares it to a stall threshold set in firmware. Alternatively, a comparator peripheral may be used to set this threshold.

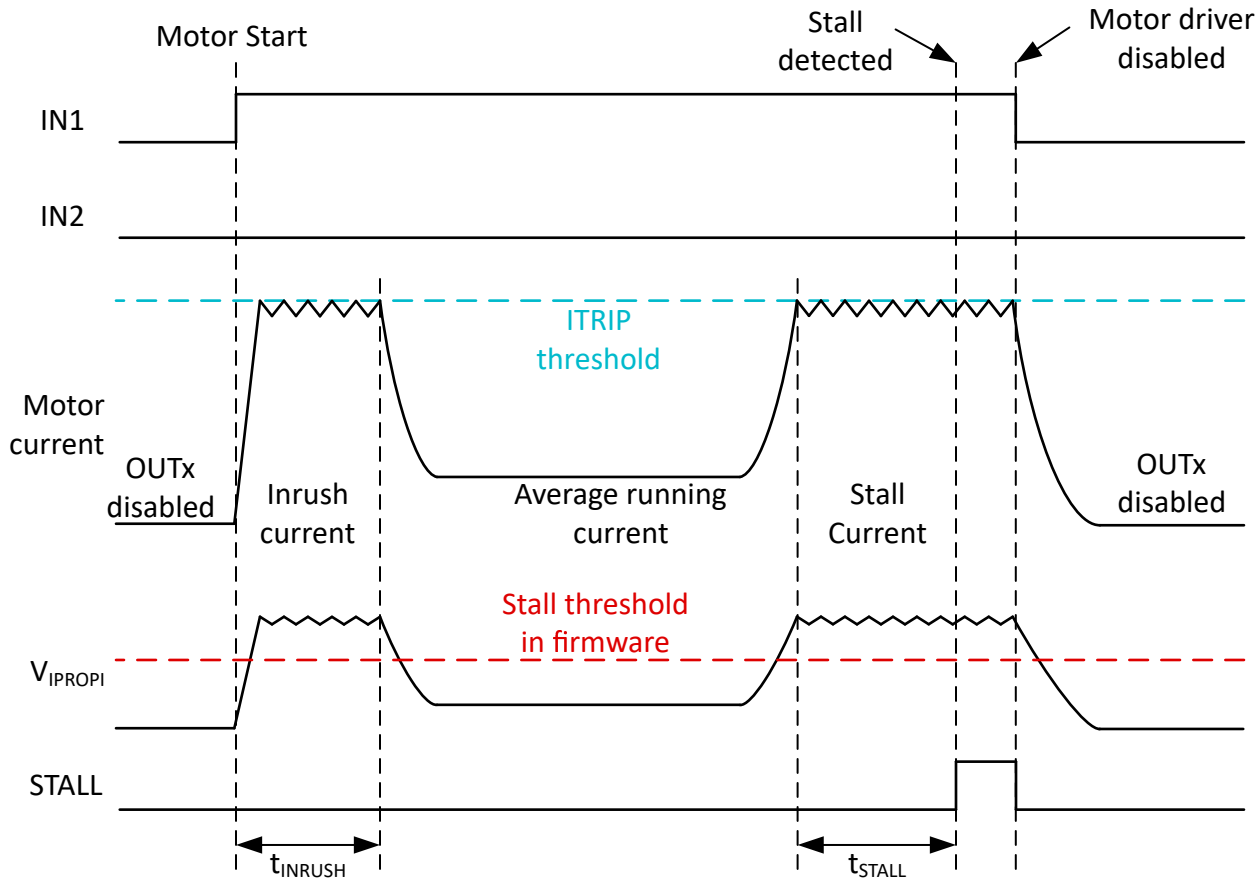


図 9-5. Motor Current Profile with STALL Signal

9.2.1.3.1.2.1 Software Stall Detection Timing

The microcontroller needs to decide whether or not the IPROPI signal indicates a motor stall. Large inrush current occurs during motor start up because motor speed is low. As the motor accelerates, the motor current drops to an average level because the back electromotive force (EMF) in the motor increases with speed. Do not mistake the inrush current for a stall condition. One way to do this is for the microcontroller to ignore the IPROPI signal above the firmware stall threshold for the duration of the inrush current, t_{INRUSH}, at startup. The t_{INRUSH} timing is determined experimentally using the motor parameters, supply voltage, and mechanical load response times.

When a stall condition occurs, the motor current increases from the average running current level because the back EMF is now 0 V. In some cases, it may be desirable to drive at the stall curent for some time in case the motor can clear the blockage on its own. This might be useful for an unintended stall or high-torque condition on the motor. In this case, the system designer can choose a long stall detection time, t_{STALL}, before the microcontroller decides to take action. In other cases, like end-stop detection, a faster response might be desired to reduce power or minimize strong motor torque on the gears or end-stop. This corresponds to setting a shorter t_{STALL} time in the microcontroller.

図 9-5 illustrates the t_{INRUSH} and t_{STALL} timings and how they relate to the motor current waveform.

9.2.1.3.1.2.2 Software Stall Threshold Selection

The stall detection threshold in firmware should be chosen at a current level between the maximum stall current and the average running current of the motor as shown in 図 9-5.

9.2.1.4 Application Curves

Traces from top to bottom: IN1 (6 V/div), OUT2 (5 V/div), V_{IPROPI} (600 mV/div), Motor Current (100 mA/div)

図 9-6. PWM Operation at VM = 1.65 V

Traces from top to bottom: OUT1 (10 V/div), OUT2 (10 V/div), Motor Current (1 A/div), V_{IPROPI} (50 mV/div)

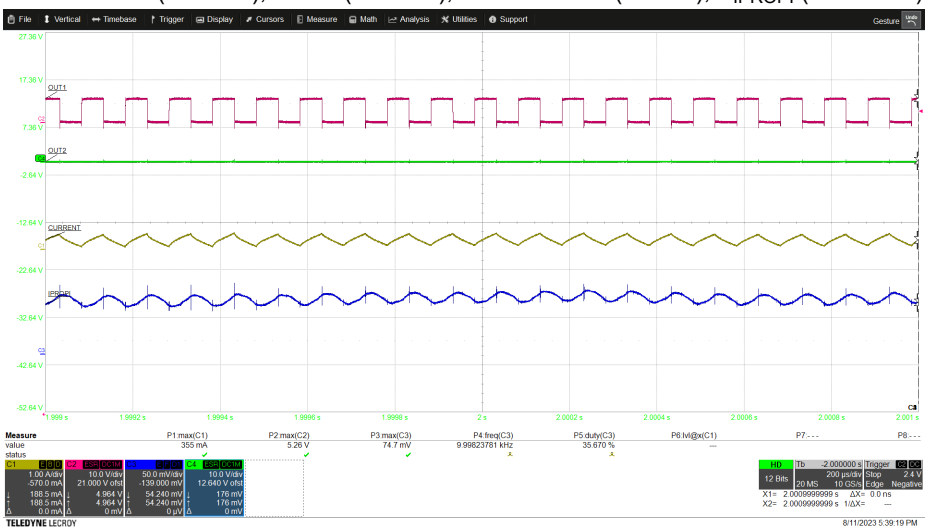


図 9-7. PWM Operation at VM = 5 V

Traces from top to bottom: IN1 (7 V/div), OUT2 (6 V/div), Motor Current (200 mA/div), V_{IPROPI} (2 V/div)

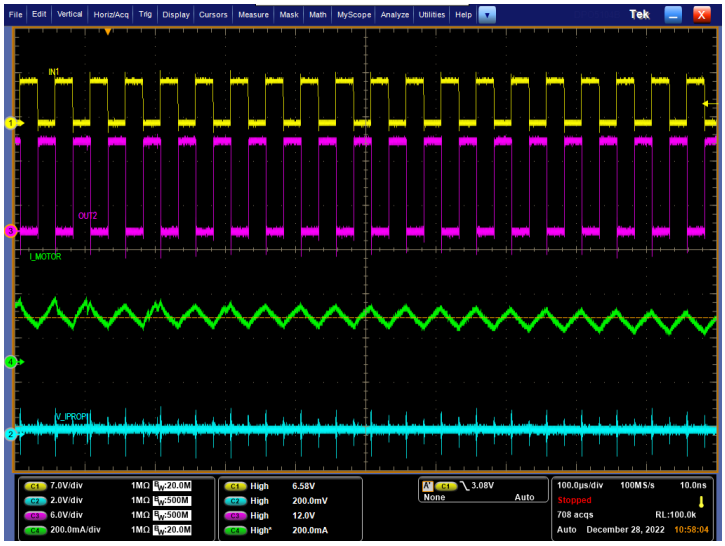


図 9-8. PWM Operation at VM = 11 V

Traces from top to bottom: nSTALL (4 V/div), TINRUSH (1 V/div), OUT2 (5 V/div), Motor Current (600 mA/div)

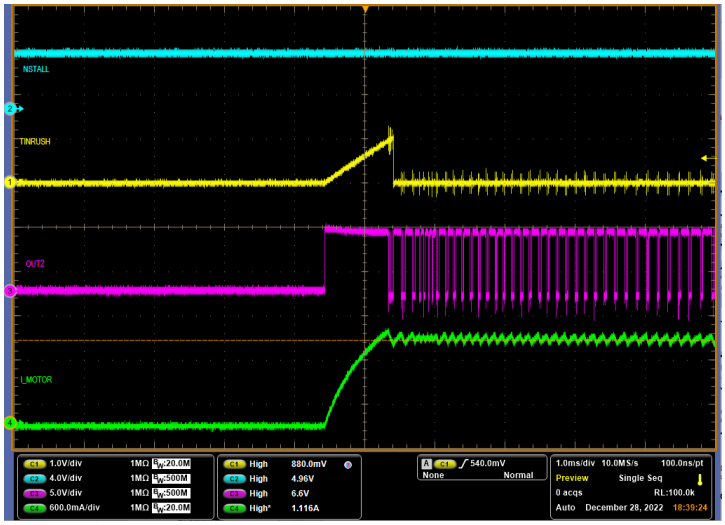


図 9-9. Stall Detection with IMODE = Hi-Z, SMODE = 1

9.2.1.5 Thermal Performance

The datasheet-specified junction-to-ambient thermal resistance, $R_{\theta JA}$, is primarily useful for comparing various drivers or approximating thermal performance. However, the actual system performance may be better or worse than this value depending on PCB stackup, routing, number of vias, and copper area around the thermal pad. The length of time the driver drives a particular current will also impact power dissipation and thermal performance. This section considers how to design for steady-state and transient thermal conditions.

The data in this section was simulated using the following criteria:

WSON (DSG package)

- 2-layer PCB (size 114.3 x 76.2 x 1.6 mm), standard FR4, 1-oz (35 mm copper thickness) or 2-oz copper thickness. Thermal vias are only present under the thermal pad (2 vias, 1.2mm spacing, 0.3 mm diameter, 0.025 mm Cu plating).

  - Top layer: DRV8213 WSON package footprint and copper plane heatsink. Top layer copper area is varied in simulation.
  - Bottom layer: ground plane thermally connected through vias under the thermal pad for DRV8213. Bottom layer copper area varies with top copper area.
- 4-layer PCB (size 114.3 x 76.2 x 1.6 mm), standard FR4. Outer planes are 1-oz (35 mm copper thickness) or 2-oz copper thickness. Inner planes are kept at 1-oz. Thermal vias are only present under the thermal pad (2 vias, 1.2mm spacing, 0.3 mm diameter, 0.025 mm Cu plating).
  - Top layer: DRV8213 WSON package footprint and copper plane heatsink. Top layer copper area is varied in simulation.
  - Mid layer 1: GND plane thermally connected to DRV8213 thermal pad through vias. The area of the ground plane is 74.2 mm x 74.2 mm.
  - Mid layer 2: power plane, no thermal connection. The area of the power plane is 74.2 mm x 74.2 mm.
  - Bottom layer: ground plane thermally connected through via stitching from the TOP and internal GND planes. Bottom layer copper area varies with top copper area.

図 9-10 shows an example of the simulated board for the DSG package. 表 9-3 shows the dimensions of the board that were varied for each simulation.

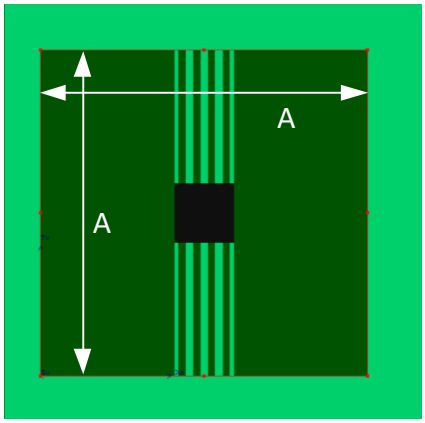


図 9-10. WSON PCB model top layer

表 9-3. Dimension A for 8-pin DSG package

Cu area (mm^2)	Dimension A (mm)
2	15.11
4	20.98
8	29.27
16	40.99

WQFN (RTE package)

- 2-layer PCB (size 114.3 x 76.2 x 1.6 mm), standard FR4, 1-oz (35 mm copper thickness) or 2-oz copper thickness. Thermal vias are only present under the package footprint (5 vias, 1 mm pitch, 0.2 mm diameter, 0.025 mm Cu plating).
  - Top layer: WQFN package footprint and traces.
  - Bottom layer: ground plane thermally connected through vias under the package footprint. Bottom layer copper area is varied in simulation.
- 4-layer PCB (size 114.3 x 76.2 x 1.6 mm), standard FR4. Outer planes are 1-oz (35 mm copper thickness) or 2-oz copper thickness. Inner planes are kept at 1-oz. Thermal vias are only present under the package footprint (5 vias, 1 mm pitch, 0.2 mm diameter, 0.025 mm Cu plating).
  - Top layer: WQFN package footprint and traces.
  - Mid layer 1: GND plane thermally connected under package footprint through vias. The area of the ground plane is 74.2 mm x 74.2 mm.

– Mid layer 2: power plane, no thermal connection. The area of the power plane is 74.2 mm x 74.2 mm.
– Bottom layer: signal layer with small copper pad underneath the driver and thermally connected through via stitching from the TOP and internal GND plane. Bottom layer thermal pad is the same size as the package (3 mm x 3 mm). Bottom pad size remains constant.

図 9-11 shows an example of the simulated board for the WQFN package. 表 9-4 shows the dimensions of the board that were varied for each simulation.

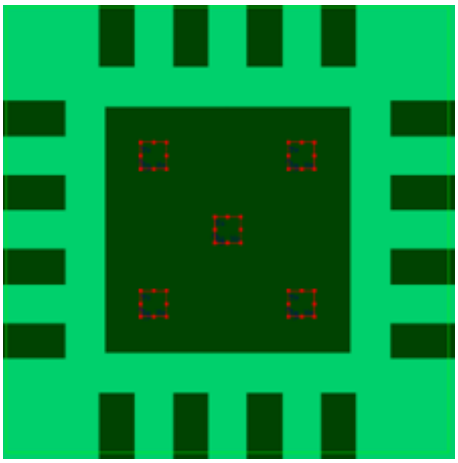


図 9-11. WQFN PCB model top layer

表 9-4. Dimension A for 16-pin RTE package

Cu area (cm^2)	Dimension A (mm)
2	14.14
4	20.00
8	28.28
16	40.00

9.2.1.5.1 Steady-State Thermal Performance

"Steady-state" conditions assume that the motor driver operates with a constant RMS current over a long period of time. The figures in this section show how $R_{\theta JA}$ and Ψ_{JB} (junction-to-board characterization parameter) change depending on copper area, copper thickness, and number of layers of the PCB. More copper area, more layers, and thicker copper planes decrease $R_{\theta JA}$ and Ψ_{JB}, which indicate better thermal performance from the PCB layout.

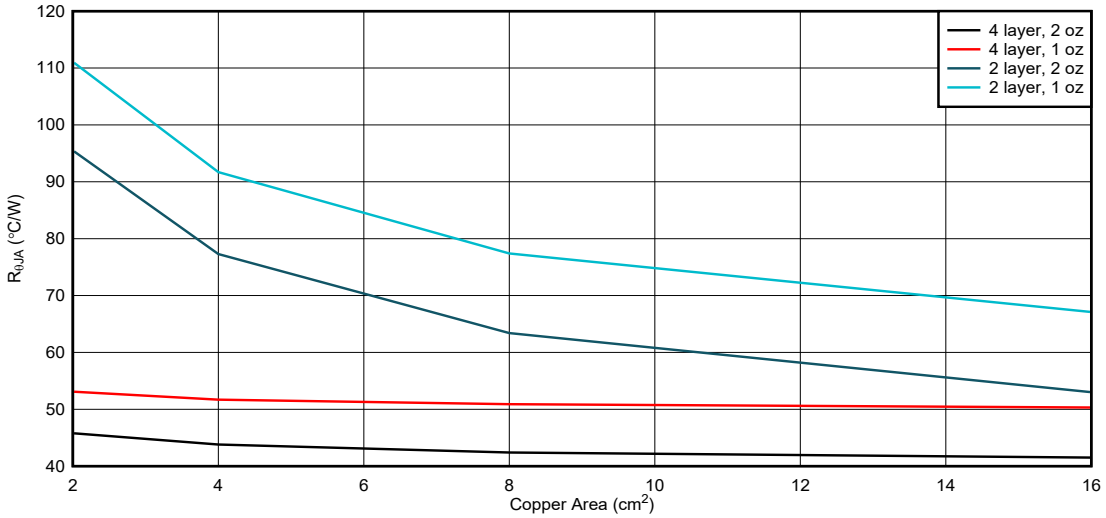


図 9-12. WSON, PCB junction-to-ambient thermal resistance vs copper area

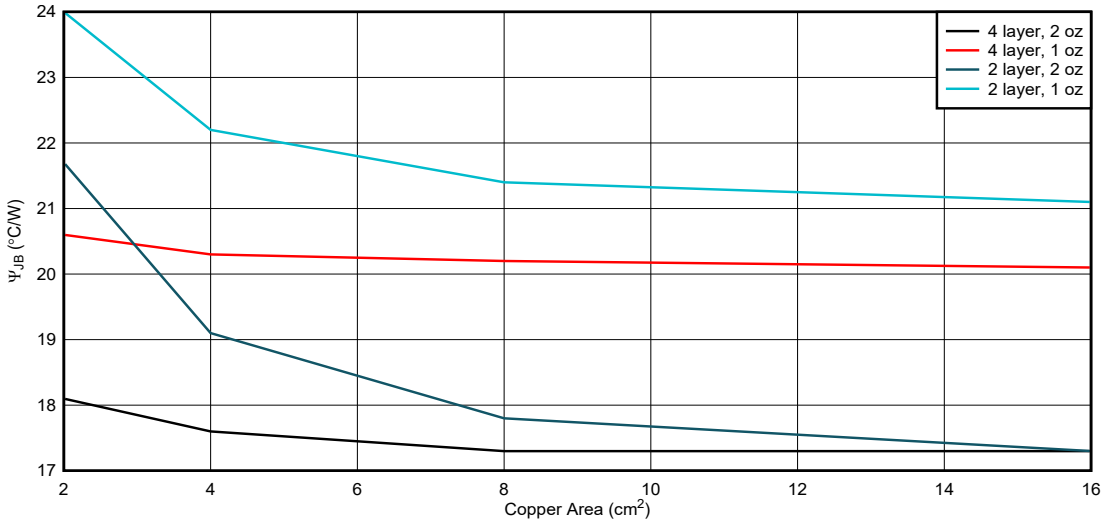


図 9-13. WSON, junction-to-board characterization parameter vs copper area

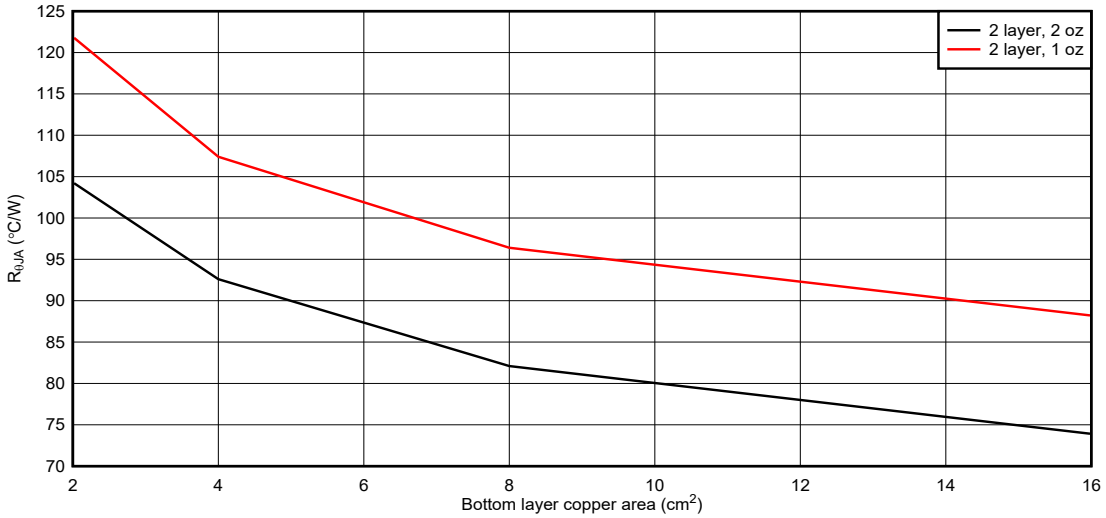


図 9-14. WQFN, PCB junction-to-ambient thermal resistance vs copper area

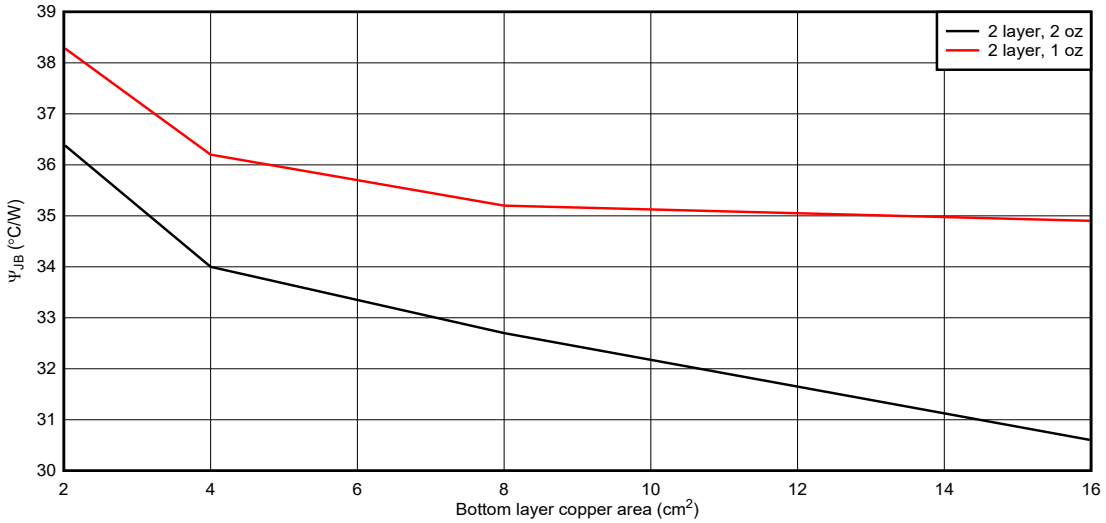


図 9-15. WQFN, junction-to-board characterization parameter vs copper area

9.2.1.5.2 Transient Thermal Performance

The motor driver may experience different transient driving conditions that cause large currents to flow for a short duration of time. These may include -

- Motor start-up when the rotor is initially stationary.
- Fault conditions when there is a supply or ground short to one of the motor outputs, and the overcurrent protection triggers.
- Briefly energizing a motor or solenoid for a limited time, then de-energizing.

For these transient cases, the duration of drive time is another factor that impacts thermal performance in addition to copper area and thickness. In transient cases, the thermal impedance parameter $Z_{\theta JA}$ denotes the junction-to-ambient thermal performance. The figures in this section show the simulated thermal impedances for 1-oz and 2-oz copper layouts for the WSON and WQFN packages. These graphs indicate better thermal performance with short current pulses. For short periods of drive time, the device die size and package dominates the thermal performance. For longer drive pulses, board layout has a more significant impact on thermal performance. Both graphs show the curves for thermal impedance split due to number of layers and copper area as the duration of the drive pulse duration increases. Long pulses can be considered steady-state performance.

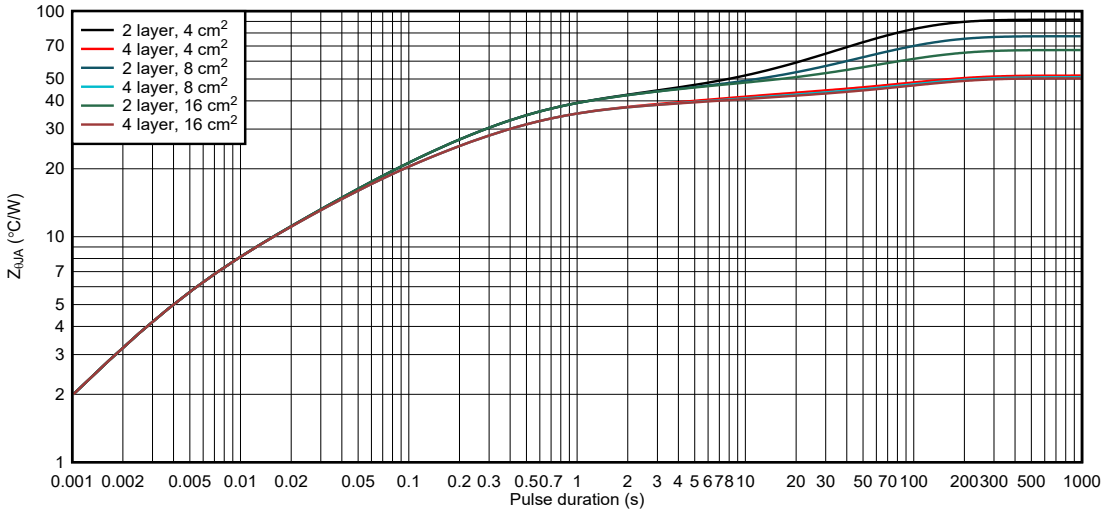


図 9-16. WSON package junction-to-ambient thermal impedance for 1-oz copper layouts

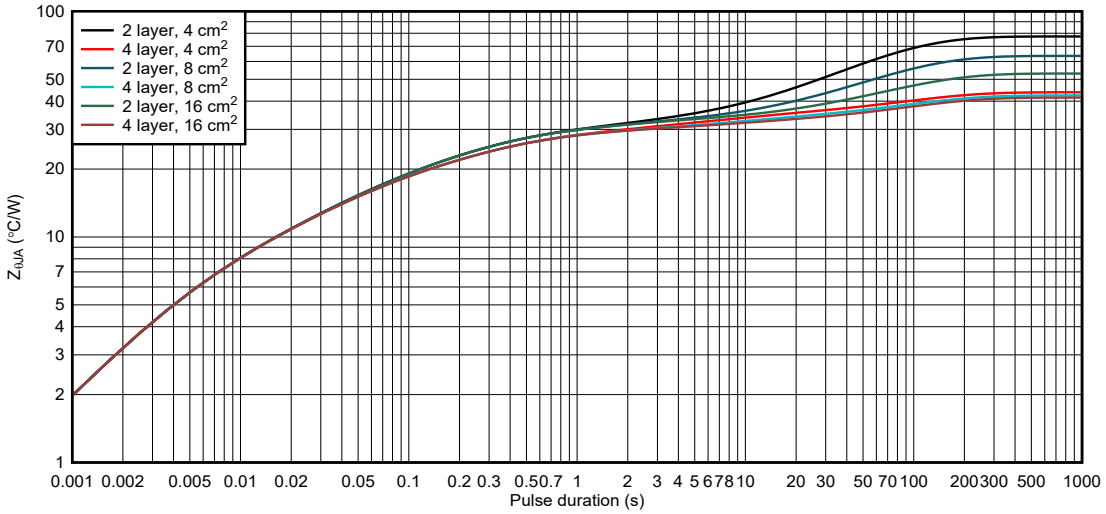


図 9-17. WSON package junction-to-ambient thermal impedance for 2-oz copper layouts

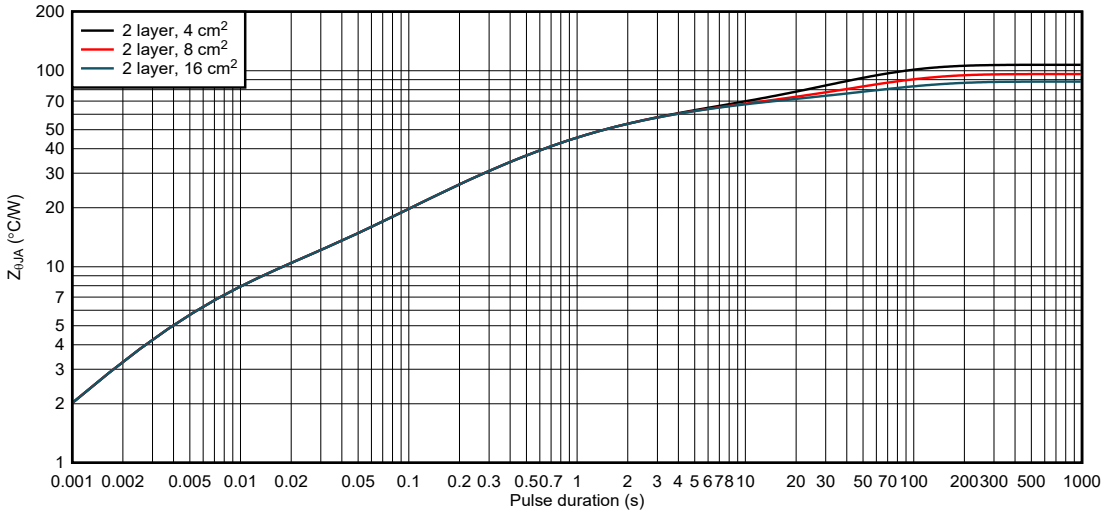


図 9-18. WQFN package junction-to-ambient thermal impedance for 1-oz copper layouts

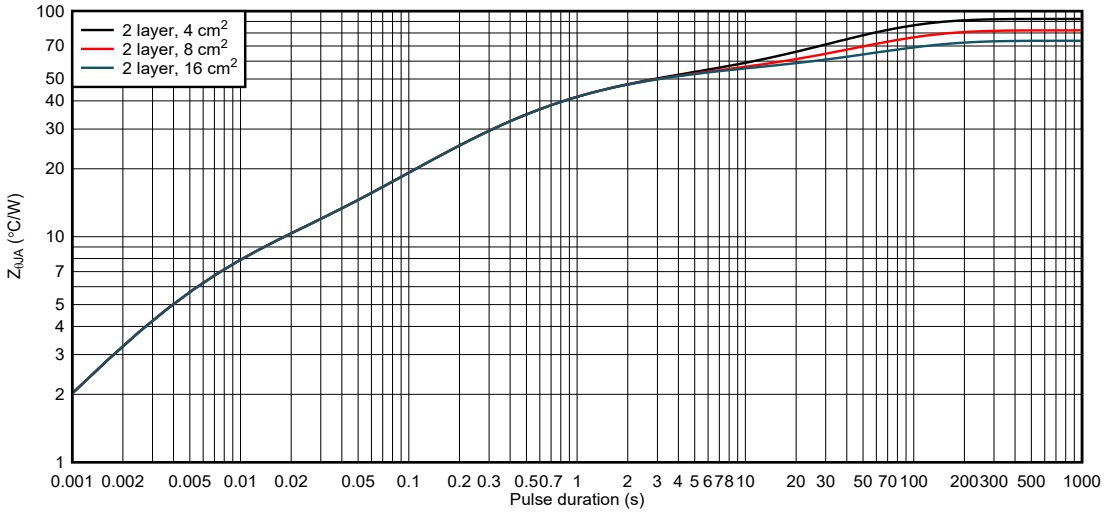


図 9-19. WQFN package junction-to-ambient thermal impedance for 2-oz copper layouts

10 Power Supply Recommendations

10.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. Having more bulk capacitance is generally beneficial, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The capacitance of the power supply and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and motor drive system limits how the rate current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

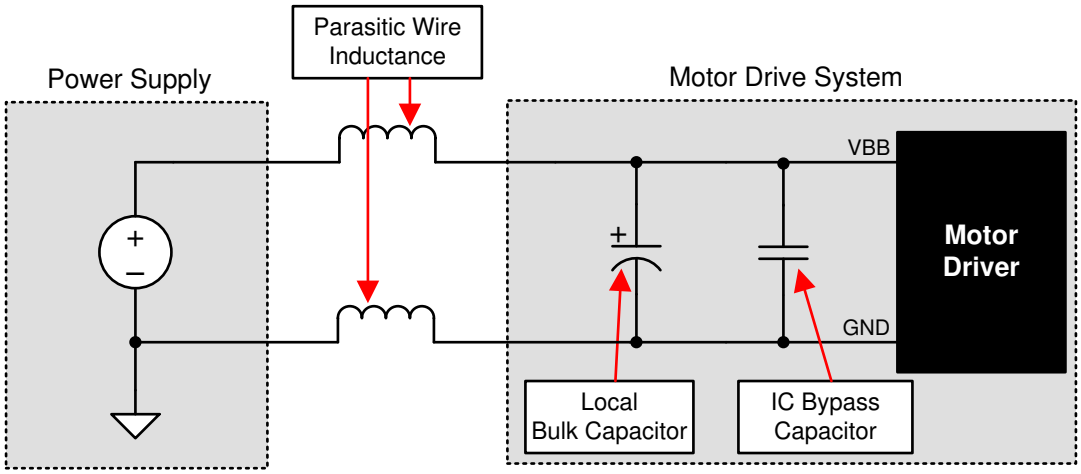


図 10-1. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

11 Layout

11.1 Layout Guidelines

Since the DRV8213 integrates power MOSFETs capable of driving high current, careful attention should be paid to the layout design and external component placement. Some design and layout guidelines are provided below.

- Low ESR ceramic capacitors should be utilized for the VM to GND bypass capacitor. X5R and X7R types are recommended.
- The VM power supply capacitors should be placed as close to the device as possible to minimize the loop inductance.
- The VM power supply bulk capacitor can be of ceramic or electrolytic type, but should also be placed as close as possible to the device to minimize the loop inductance.
- VM, OUT1, OUT2, and GND carry the high current from the power supply to the outputs and back to ground. Thick metal routing should be utilized for these traces as is feasible.
- The device thermal pad should be attached to the PCB top layer ground plane and internal ground plane (when available) through thermal vias to maximize the PCB heat sinking.
- A recommended land pattern for the thermal vias is provided in the package drawing section.
- The copper plane area attached to the thermal pad should be maximized to ensure optimal heat sinking.

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Calculating Motor Driver Power Dissipation* application report
- Texas Instruments, *Current Recirculation and Decay Modes* application report
- Texas Instruments, *PowerPAD™ Made Easy* application report
- Texas Instruments, *PowerPAD™ Thermally Enhanced Package* application report
- Texas Instruments, *Understanding Motor Driver Current Ratings* application report

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

12.4 Trademarks

すべての商標は、それぞれの所有者に帰属します。

13 Mechanical, Packaging, and Orderable Information

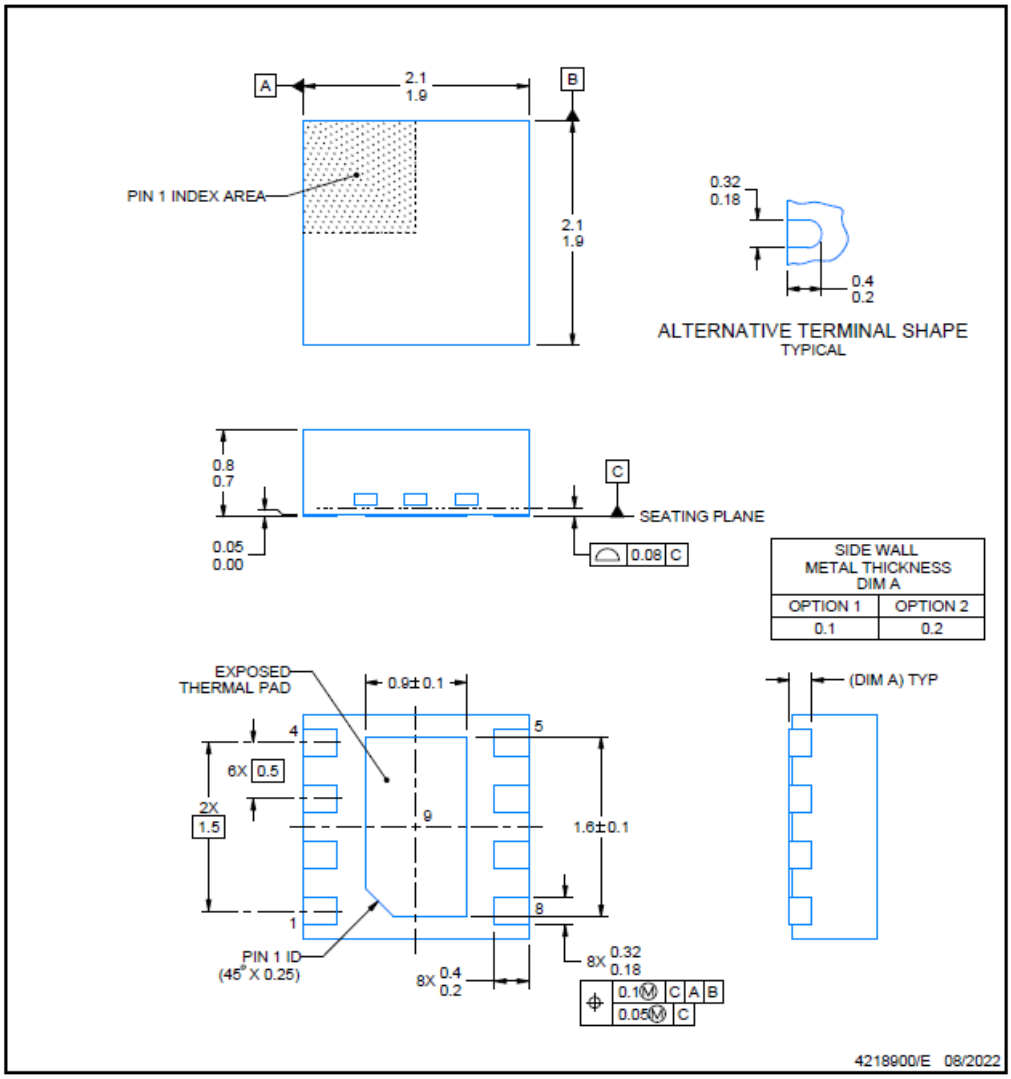
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



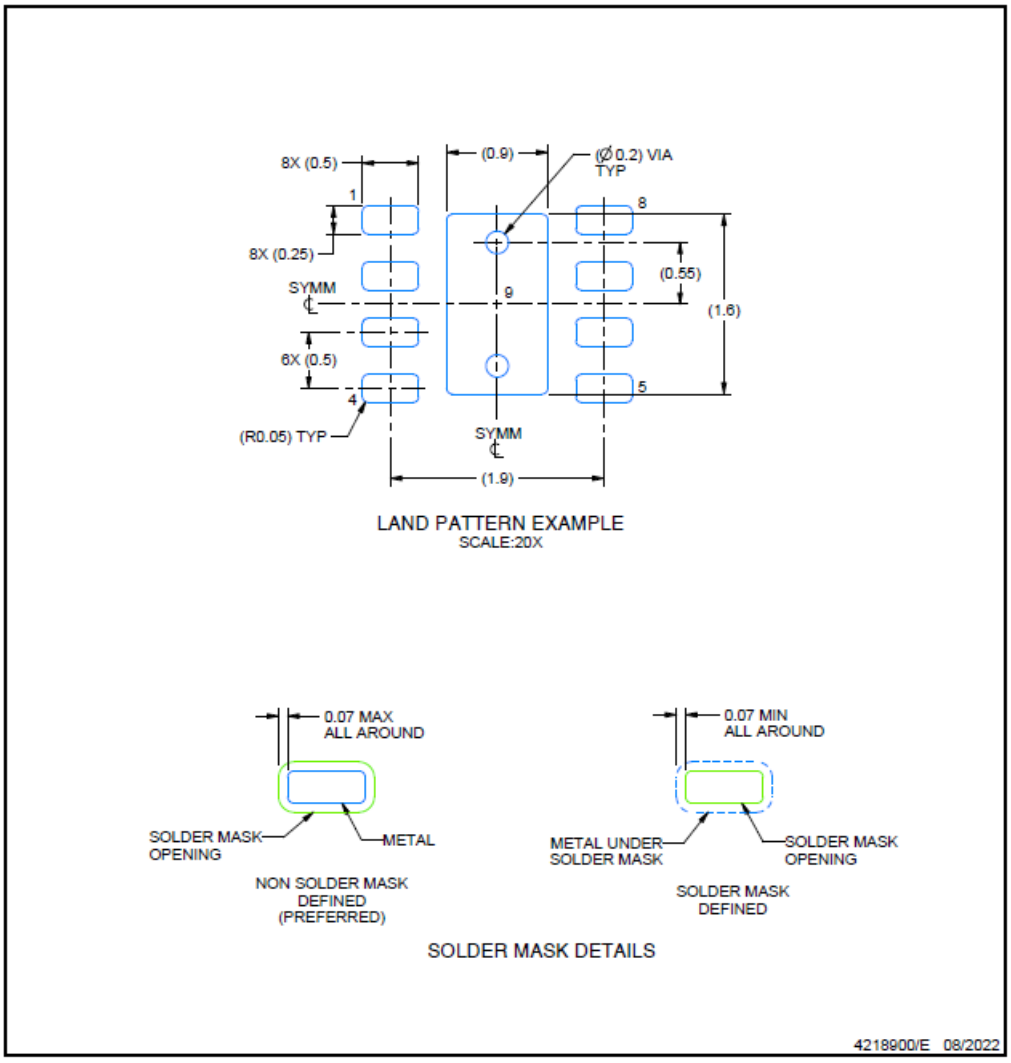
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

DSG0008A — **WSON - 0.8 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



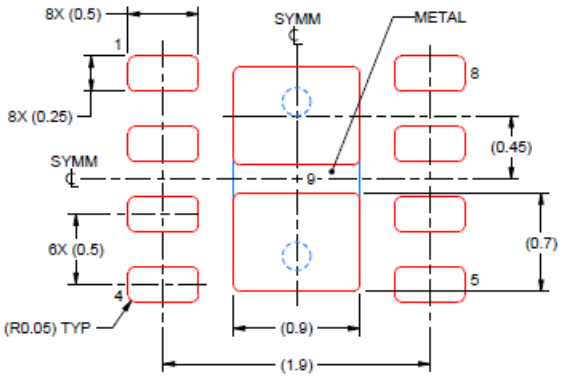
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DSG0008A — **WSON - 0.8 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/E 08/2022

NOTES: (continued)

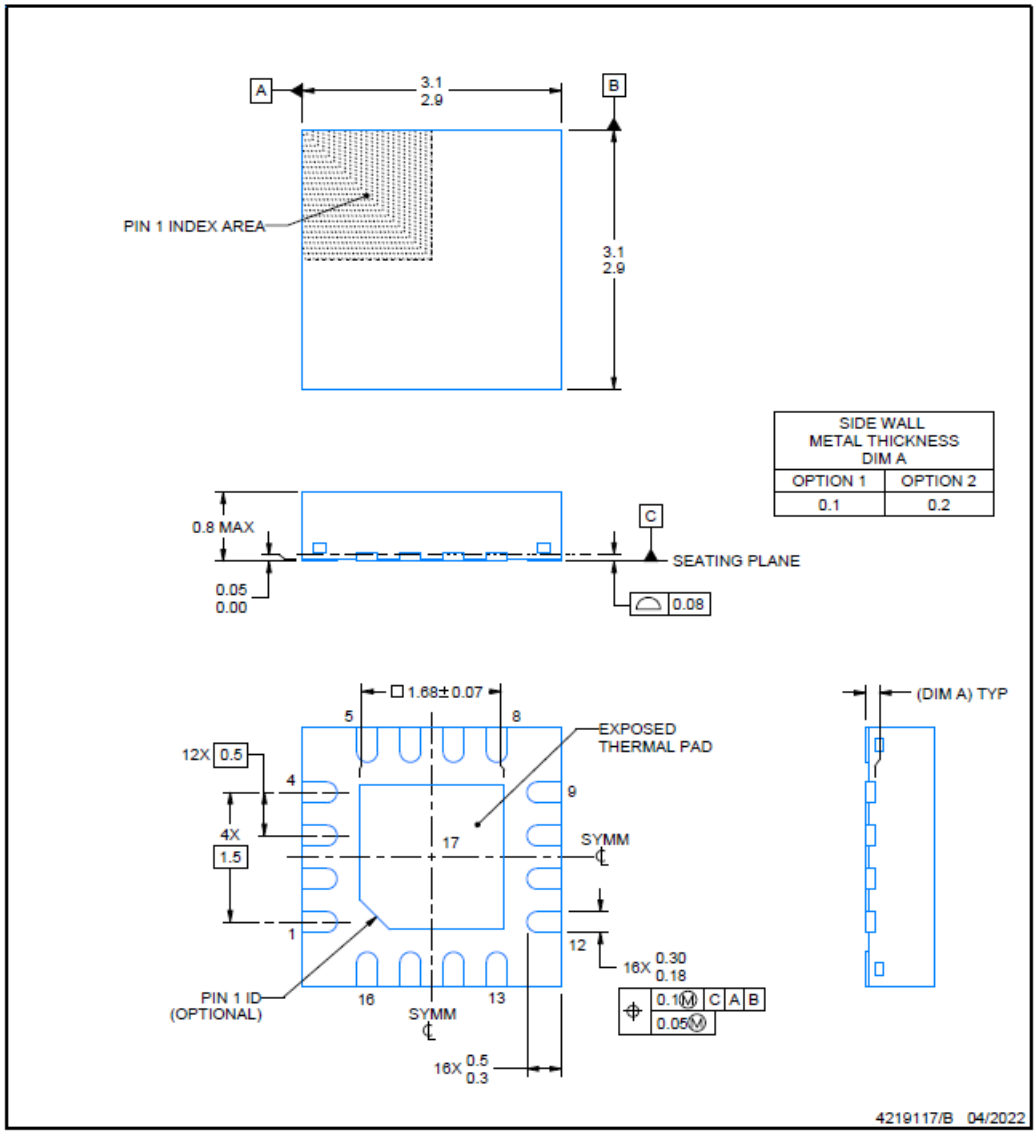
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

RTE0016C

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



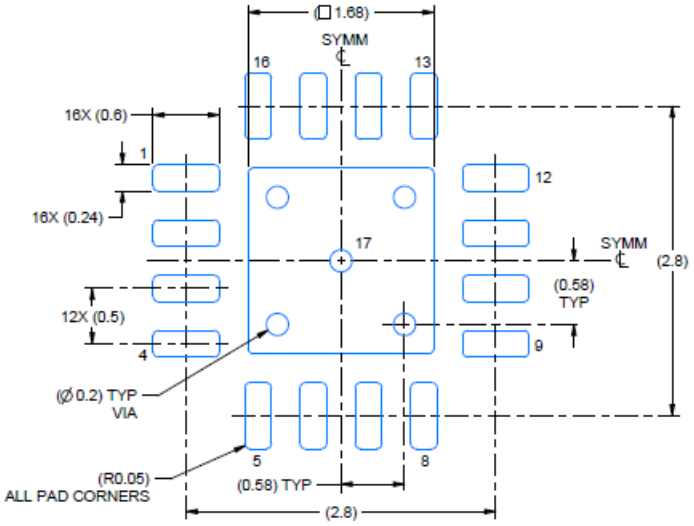
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

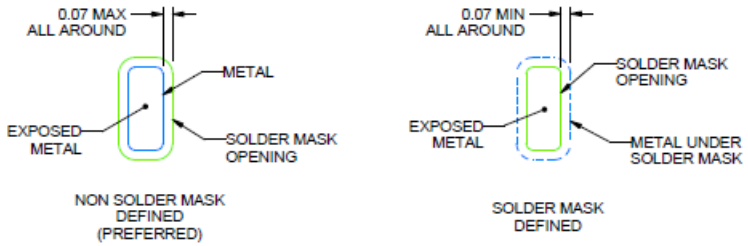
EXAMPLE BOARD LAYOUT

RTE0016C — **WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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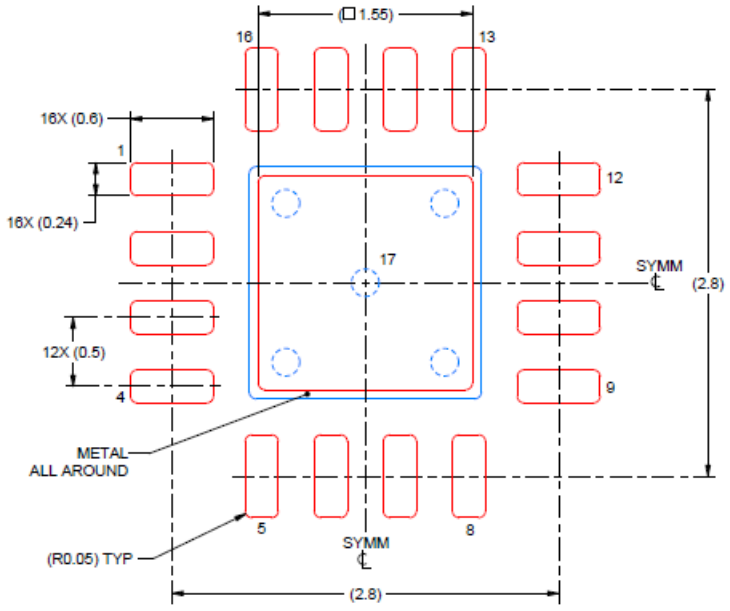
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RTE0016C — **WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

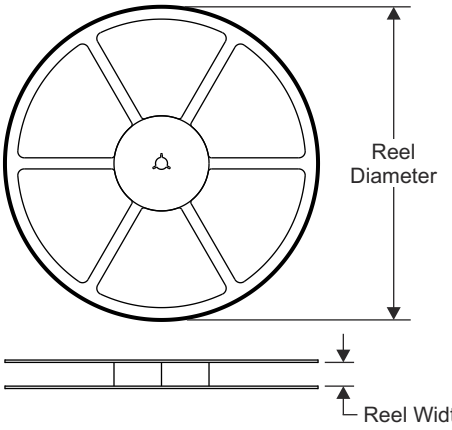
4219117/B 04/2022

NOTES: (continued)

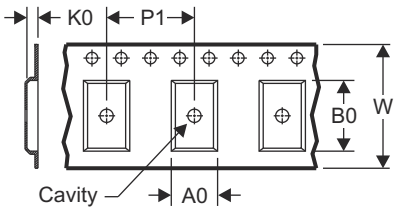
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

13.1 Tape and Reel Information

REEL DIMENSIONS

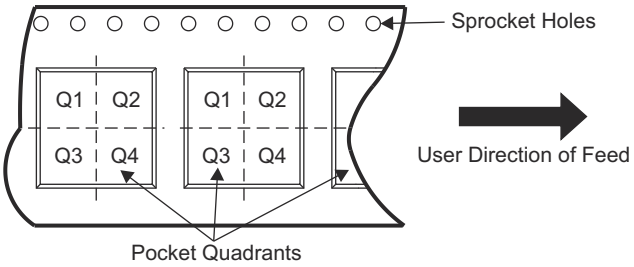


TAPE DIMENSIONS



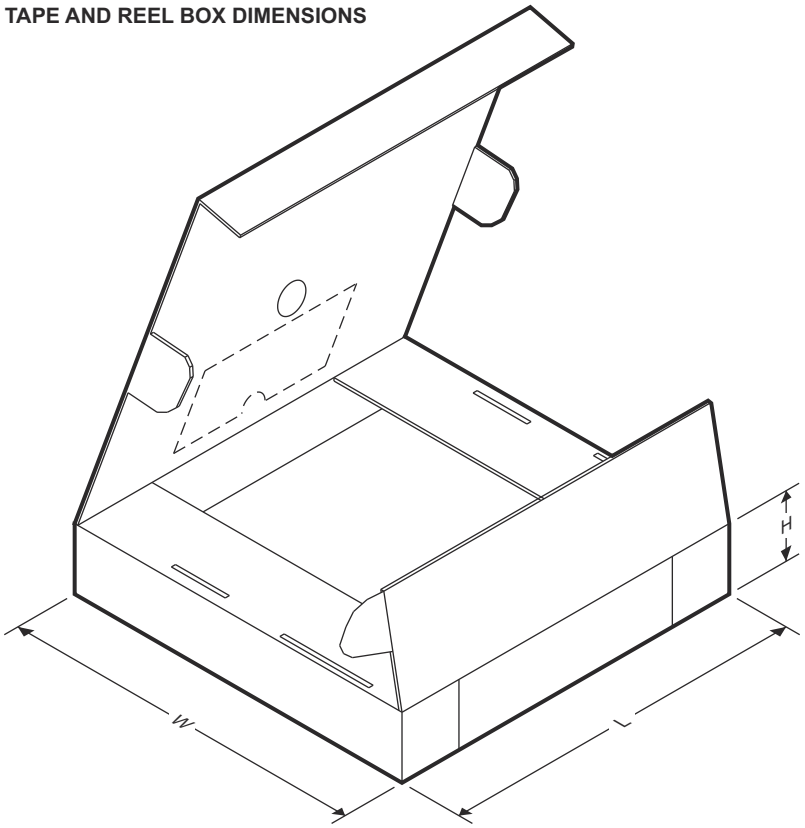
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8213DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
DRV8213RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8213DSGR	WSON	DSG	8	3000	2.0	2.0	0.8
DRV8213RTER	WQFN	RTE	16	3000	3.0	3.0	0.8

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV8213DSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8213
DRV8213DSGR.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8213
DRV8213RTER	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8213
DRV8213RTER.A	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8213

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

GENERIC PACKAGE VIEW

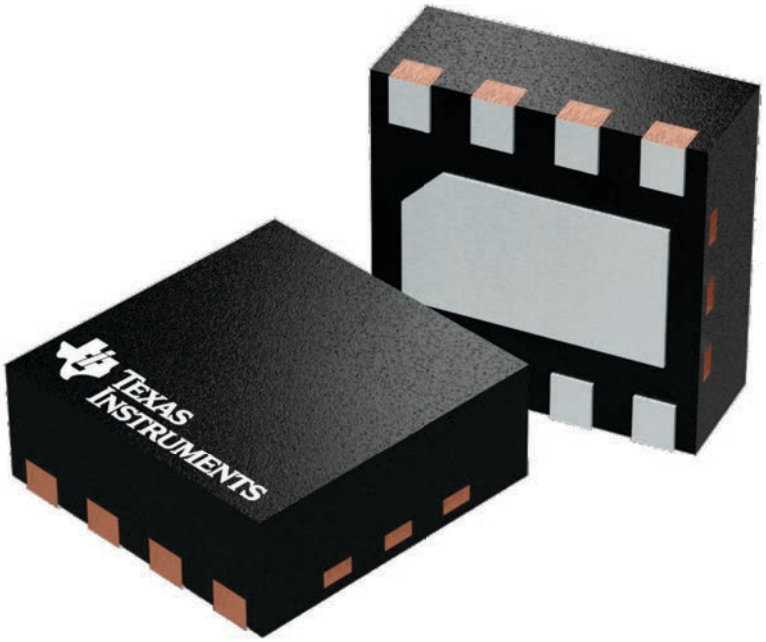
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



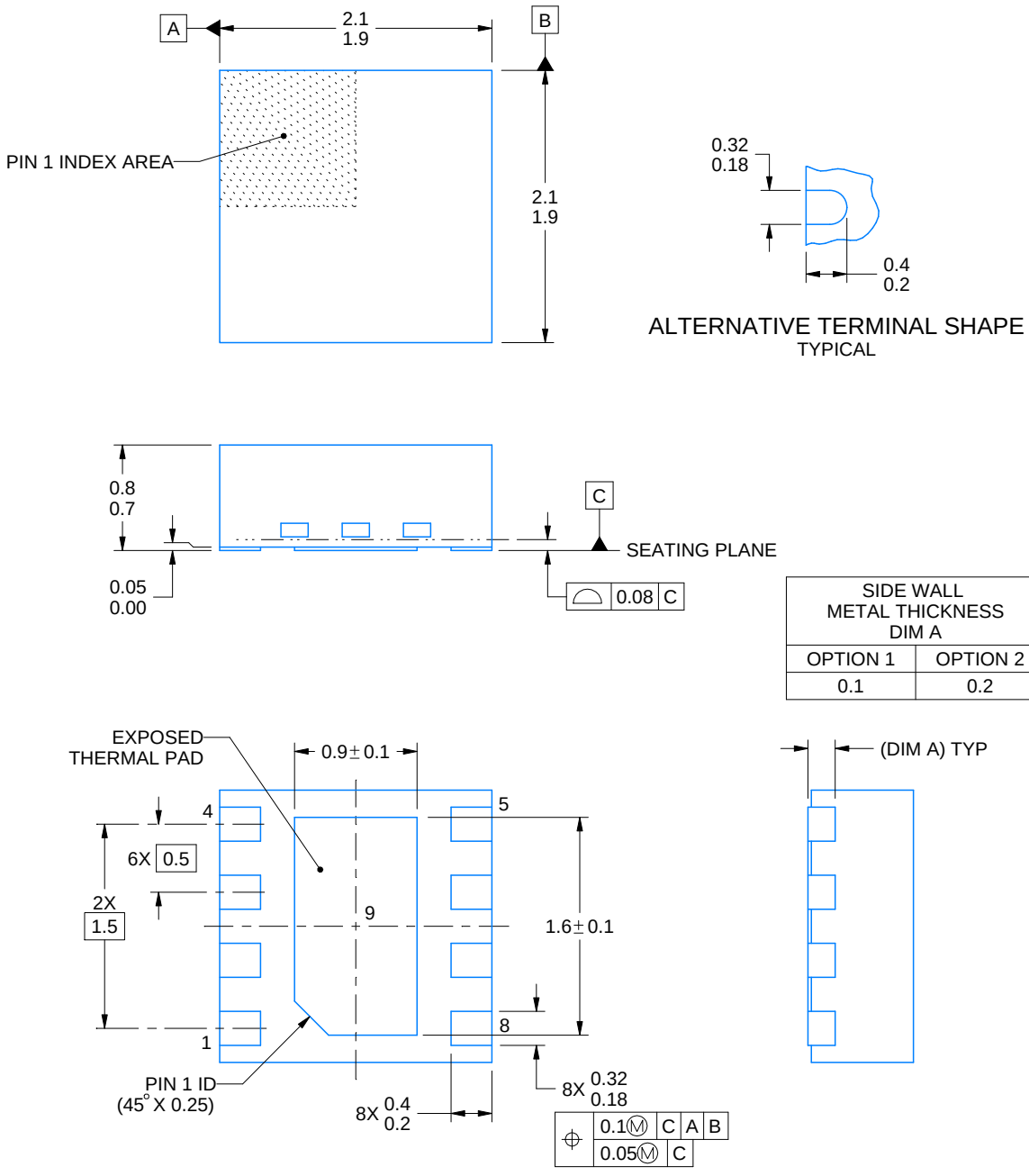
4224783/A

PACKAGE OUTLINE

DSG0008A

WSON - 0.8 mm max height

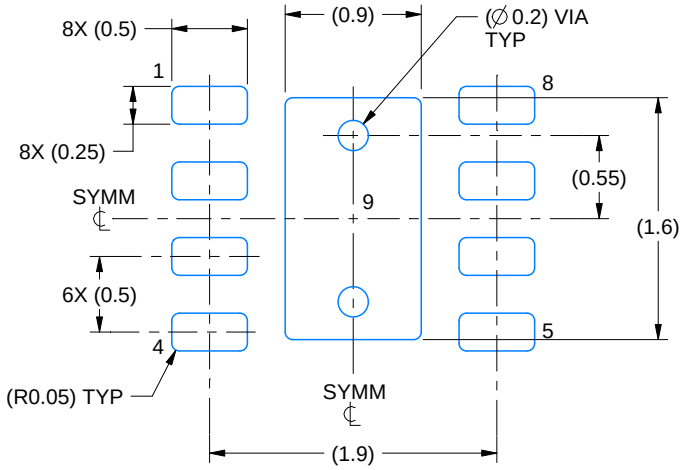
PLASTIC SMALL OUTLINE - NO LEAD



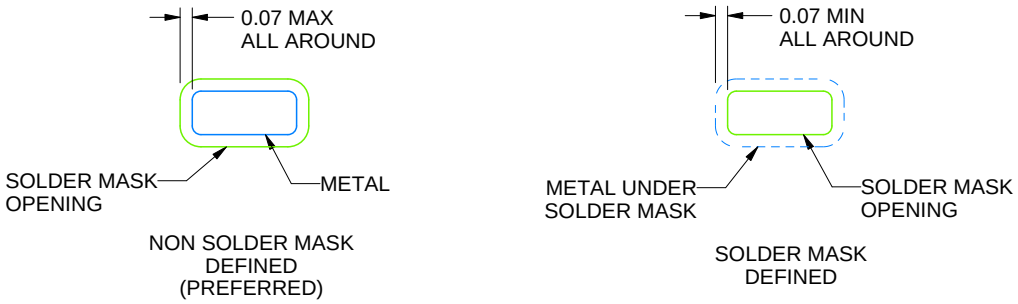
4218900/E 08/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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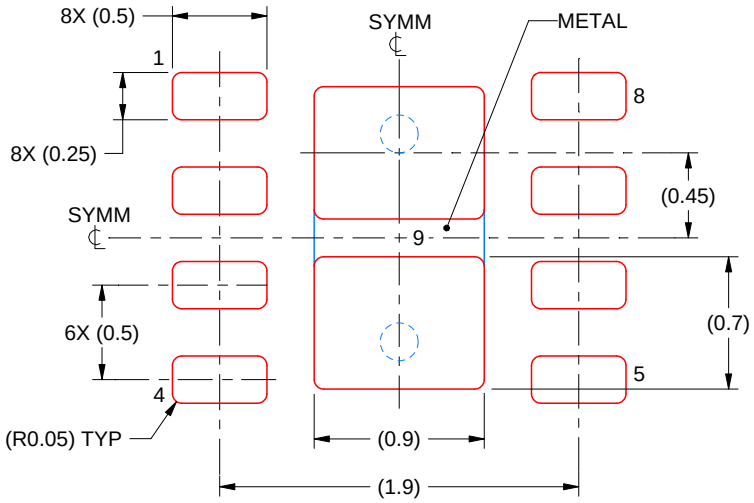
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/E 08/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

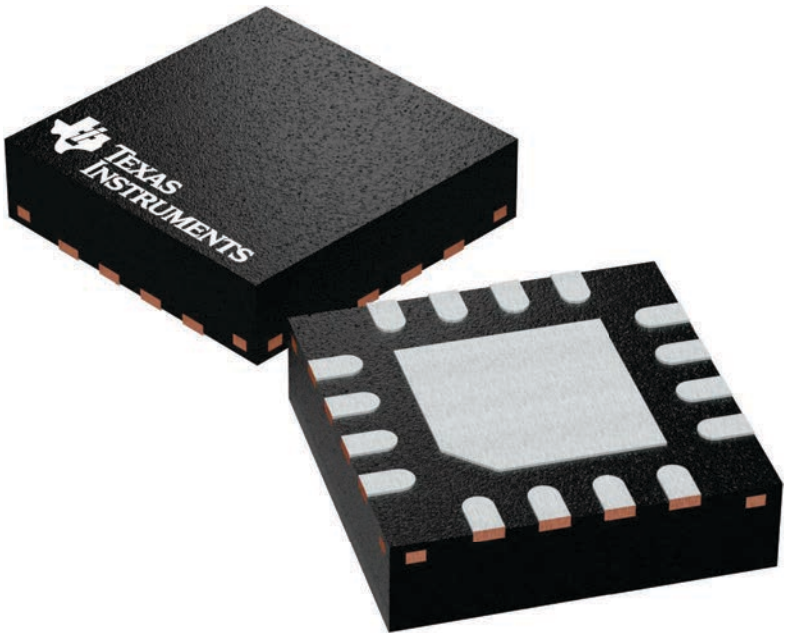
RTE 16

WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

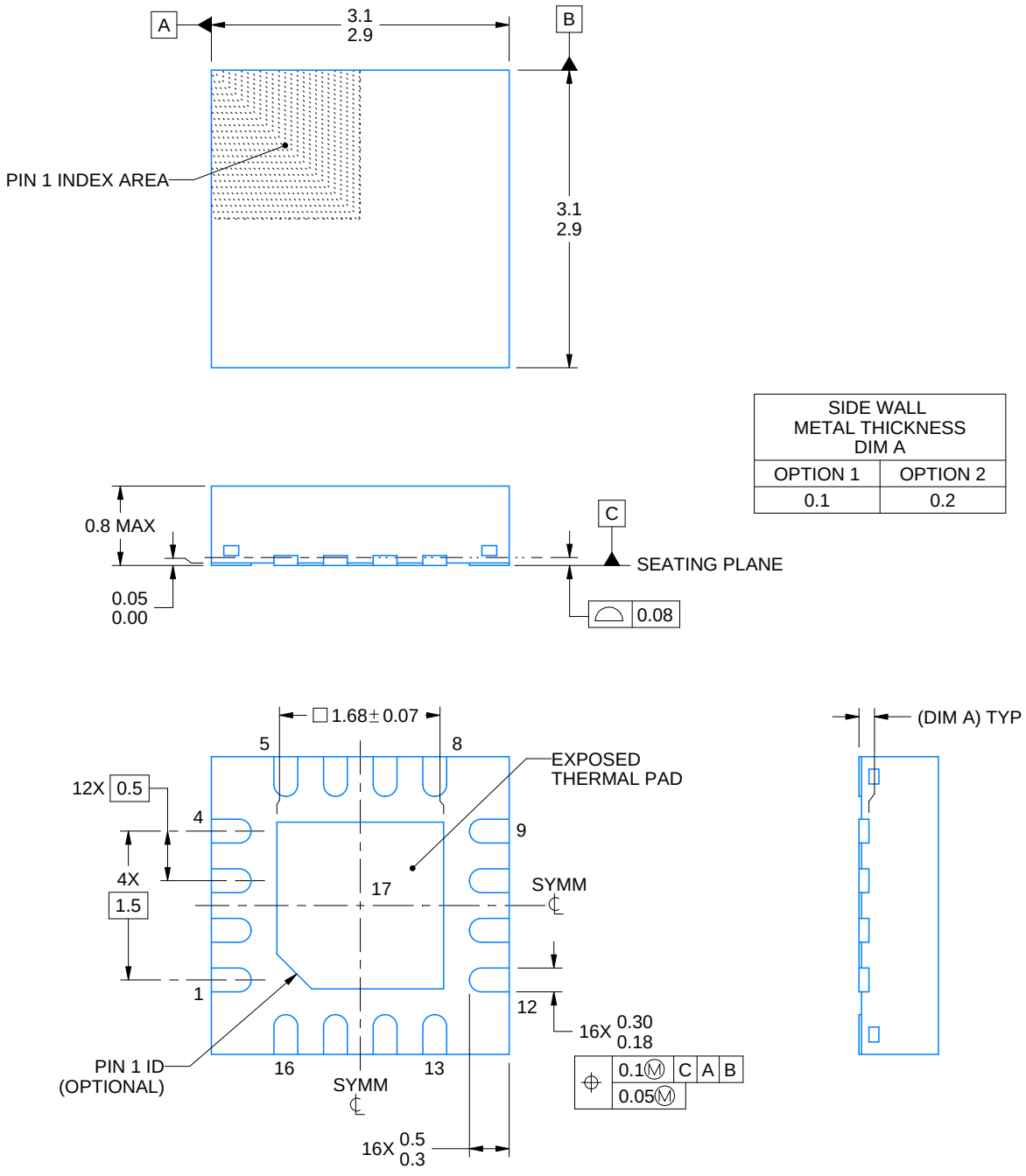


RTE0016C

PACKAGE OUTLINE

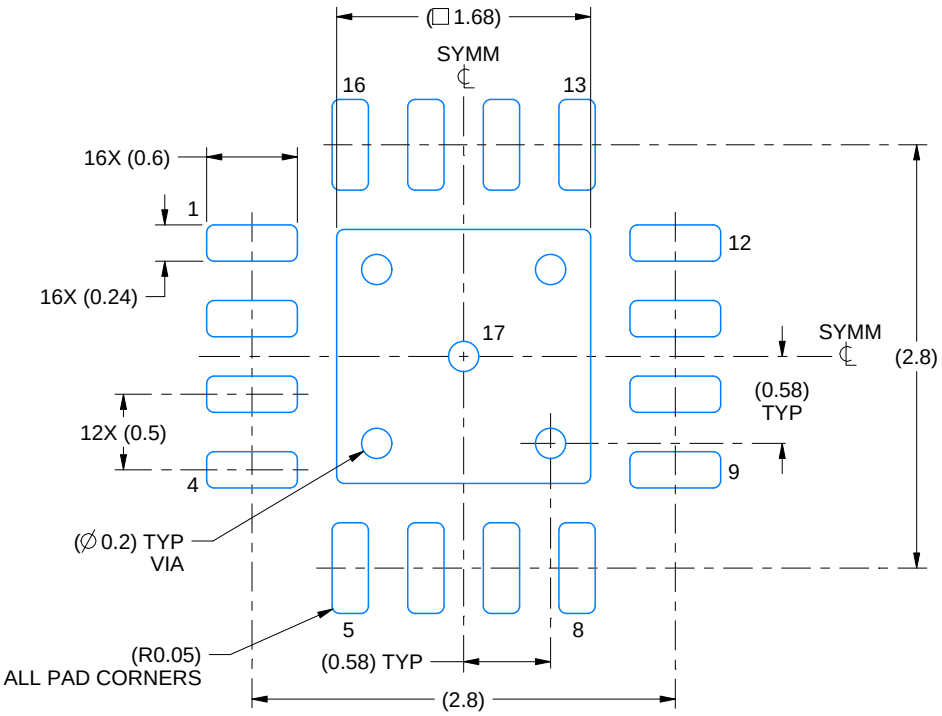
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

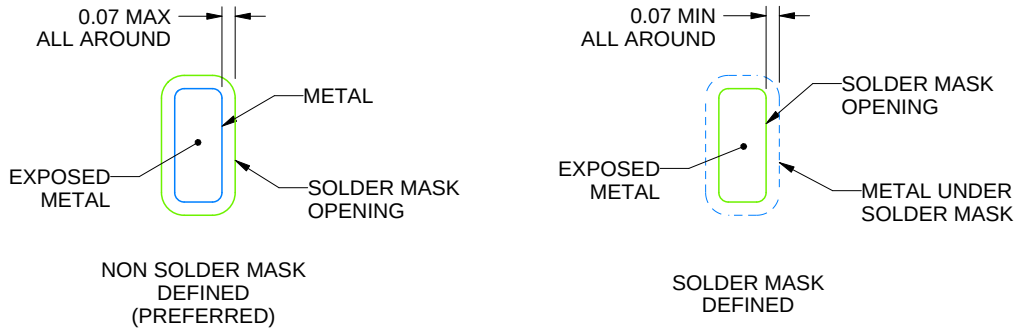


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

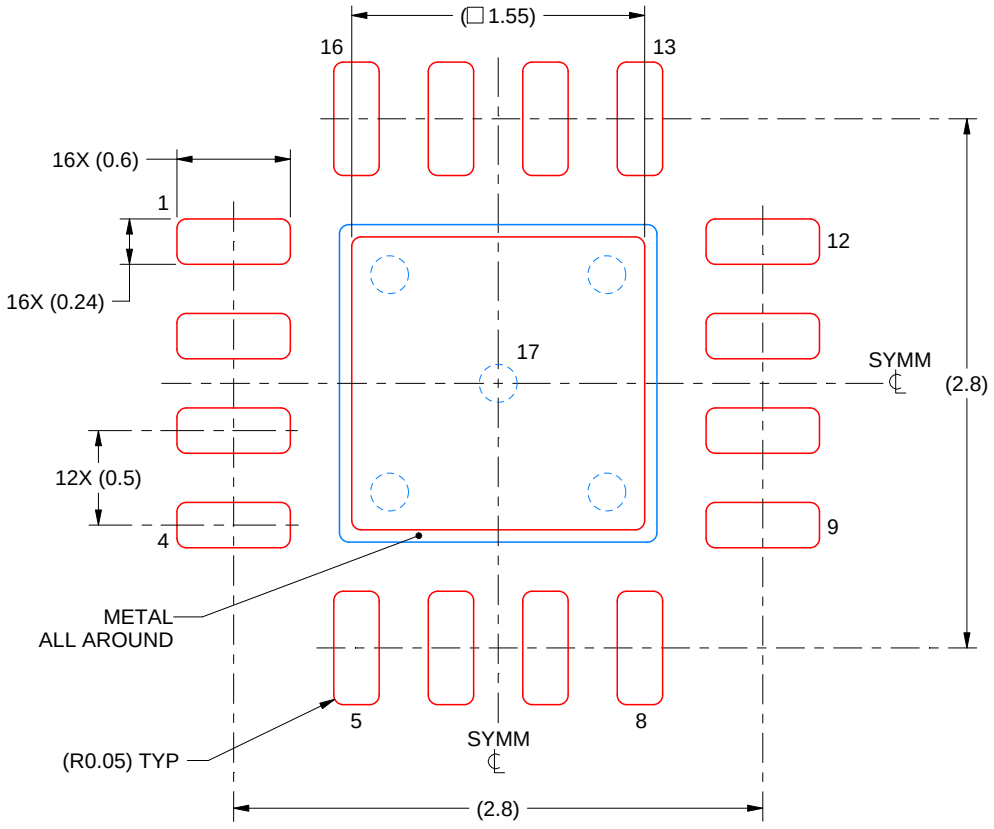


SOLDER MASK DETAILS

4219117/B 04/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219117/B 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

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