TEXAS INSTRUMENTS
DRV8215
JAJSU38 – APRIL 2024

DRV8215 速度調整機能およびストール検出機能内蔵、11V、4A、ブラシ付き DC モーター ドライバ

1 特長

- N チャネル、H ブリッジ、ブラシ付き DC モーター ドライバ
- 動作電源電圧範囲:**1.65V～11V**
- **電圧**および**速度レギュレーション**を内蔵
- **ソフト スタートおよびストップ**機能による突入電流からの保護
- **240mΩ** の $R_{DS(on)}$ (ハイサイド+ローサイド)
- 高い出力電流能力:4A ピーク、2A RMS
- I^2C 制御インターフェイス搭載 PWM
  - I^2C レジスタでの構成と診断
  - マルチフォロア動作のサポート
  - 標準およびファースト I^2C モードをサポート
- 1.8V、3.3V、5V のロジック入力をサポート
- 電流センスおよび電流レギュレーション機能を内蔵
- アナログ電流センス出力 (IPROPI)
- ゲイン選択機能:
  - 最小 10mA までの高精度電流センス
  - $R_{DS\ (ON)}$ と過電流制限を最適化
- 100% デューティ サイクルの内部チャージ ポンプ
- 低消費電力のスリープ モードによる長いバッテリ寿命
  - < 100nA の最大スリープ電流
- 小さなパッケージと占有面積
  - PowerPAD™ 付き 16 ピン WQFN、3 × 3mm
- 保護機能内蔵
  - VCC 低電圧誤動作防止 (UVLO)
  - 過電流保護 (OCP)
  - サーマル シャットダウン (TSD)
  - ストール検出
  - 過電圧保護 (OVP)

2 アプリケーション

- 電子スマート ロック
- 電子 / ロボット玩具
- 水道およびガス メーター
- 輸液ポンプおよびその他のポータブル医療機器
- 電動歯ブラシ、美容 & 身だしなみ
- ポータブル プリンタおよび POS (販売時点管理) デバイス

3 概要

DRV8215 は、速度および電圧レギュレーション機能に加えて、ストール検出、電流検出出力、電流レギュレーション、保護回路などの追加機能を内蔵した高性能統合型 H ブリッジ モータードライバです。

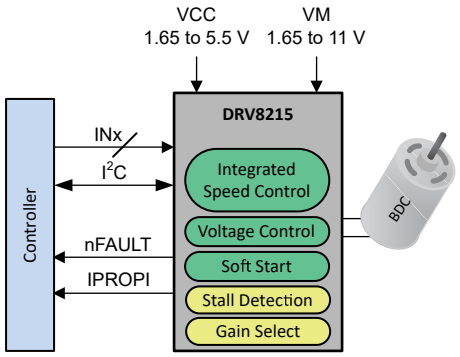
この内蔵された速度および電圧レギュレーション機能は、モーター電圧および電流情報を使用してモーターの速度または電圧を制御するため、速度を検出するための外部センサは不要です。これにより、基板のサイズと設計の複雑さが低減し、システム全体のコストが削減されます。内蔵の速度レギュレーション機能により、入力電源電圧が変化してもモータ速度が一定に保たれるため、消費電流が最小限に抑えられ、長期的に電力が節約されます。これは、さまざまな負荷条件を持つアプリケーションや、入力電圧が一定ではない操作に対してバッテリ電源に依存するアプリケーションで重要です。ソフト スタートおよびストップにより、制御されたターンオンおよびターンオフ時間が可能になり、大きな突入電流を低減してモータ巻線を損傷から保護することで、システムの信頼性と耐用期間が向上します。

内部カレント ミラーは、電流センスとレギュレーションを実装しています。そのため、大電力シャント抵抗を使う必要がなく、基板面積を節約しシステム コストを低減できます。IPROPI 電流センス出力を使うと、マイコンはモーターのストールまたは負荷条件の変化を検出できます。ゲイン選択機能により、平均モーター電流 10mA までの高精度の電流センスが可能です。VREF ピンを使うことで、起動および高負荷イベント中もマイコンを使わずにモーター電流をレギュレーションできます。デバイスは、センサレス モータストール検出とマイコンへのレポートをサポートしています。

製品情報

部品番号	パッケージ (1)	パッケージ サイズ (公称) (2)
DRV8215	WQFN (16)	3.00mm × 3.00mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



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4 Device Comparison

表 4-1. Device Comparison Table

Part Number	Package	Supply VM (V)	$R_{DS(ON)}$ (mΩ)	RMS Current Capacity (A)	Sensorless Position Sensing	Speed Regulation	Stall Detection	Package Size
DRV8214	RTE	1.65 to 11	240	2	Yes	Yes	Yes	3 mm × 3 mm
DRV8215	**RTE**	**1.65 to 11**	**240**	**2**	**No**	**Yes**	**Yes**	**3 mm × 3 mm**
DRV8234	RTE	4.5 to 38	600	2	Yes	Yes	Yes	3 mm × 3 mm
DRV8235	RTE	4.5 to 38	600	2	No	Yes	Yes	3 mm × 3 mm
DRV8213	RTE	1.65 to 11	240	2	No	No	Yes	3 mm × 3 mm
DRV8213	DSG	1.65 to 11	240	2	No	No	No	2 mm × 2 mm

5 Pin Configuration and Functions

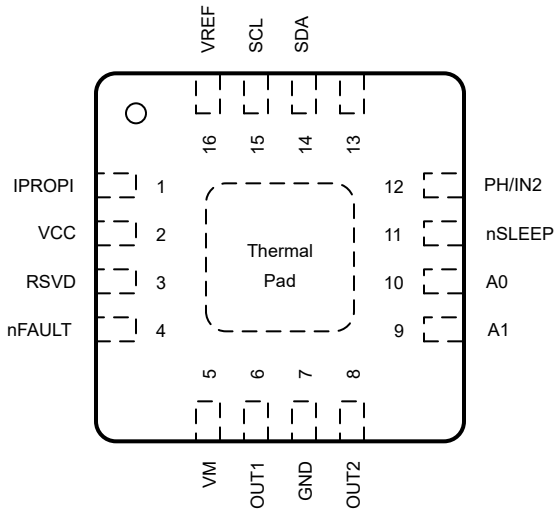


図 5-1. RTE Package 16-Pin WQFN Top View

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	RTE		
IPROPI	1	PWR	Analog current output proportional to load current. Connect a resistor from IPROPI to ground.
VCC	2	PWR	Logic power supply. Bypass this pin to the GND pin with a 0.1-µF ceramic capacitor rated for VCC.
RSVD	3	—	Reserved. Leave this pin unconnected.
nFAULT	4	OD	Fault indicator output. Pulled low during a fault condition. Connect an external pullup resistor for open-drain operation.
VM	5	PWR	Motor power supply. Bypass this pin to the GND pin with a 0.1-µF ceramic capacitor as well as sufficient bulk capacitance rated for VM.
OUT1	6	O	H-bridge output. Connect directly to the motor.
GND	7	PWR	Device ground. Connect to system ground.
OUT2	8	O	H-bridge output. Connect directly to the motor.
A1	9	I	I^2C base address select pin. Tri-level input.
A0	10	I	I^2C base address select pin. Tri-level input.
nSLEEP	11	I	Sleep mode input. Logic high to enable device. Logic low to enter low-power sleep mode. Internal pulldown resistor.
PH/IN2	12	I	Controls the H-bridge output. Has internal pulldown.
EN/IN1	13	I	Controls the H-bridge output. Has internal pulldown.
SDA	14	I	I^2C data signal. The SDA pin requires a pullup resistor.
SCL	15	I	I^2C clock signal.
VREF	16	I	Analog input to set current regulation and stall detection level.
PAD	—	—	Thermal pad. Connect to board ground. For good thermal dissipation, use large ground planes on multiple layers, and multiple nearby vias connecting those planes.

(1) I = Input, O = Output, PWR = Power, OD = Open-Drain Output

6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Power supply pin voltage	VM	-0.5	12	V
Logic power supply pin voltage	VCC	-0.5	5.75	V
Power supply transient voltage ramp	VM, VCC	0	2	V/µs
Logic pin voltage	EN/IN1, PH/IN2, A1, A0, SDA, SCL, nSLEEP	-0.3	5.75	V
Open-drain output pin voltage	nFAULT	-0.3	5.75	V
Proportional current output pin voltage, VM ≥ 5.45 V	IPROPI	-0.3	5.75	V
Proportional current output pin voltage, VM < 5.45 V		-0.3	V_{VM} + 0.3	V
Reference input pin voltage	VREF	-0.3	5.75	V
Output pin voltage	OUTx	$-V_{SD}$	$V_{VM}+V_{SD}$	V
Output current	OUTx	Internally Limited	Internally Limited	A
Ambient temperature, T_A		–40	125	°C
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ± 2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ± 500 V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{VM}	Power supply voltage	VM	0		11	V
V_{VCC}	Power supply voltage	VCC	1.65		5.5	V
V_{IN}	Logic input voltage	EN/IN1, PH/IN2,A1, A0, SDA, SCL,nSLEEP	0		5.5	V
f_{PWM}	PWM frequency	INx	0		200	kHz
V_{OD}	Open drain pullup voltage	nFAULT	0		5.5	V
I_{OD}	Open drain output current	nFAULT	0		5	mA
I_{OUT} (1)	Peak output current	OUTx	0		4	A
I_{IPROPI}	Current sense output current	IPROPI	0		1	mA
V_{VREF}	Current limit reference voltage	VREF	0		min (3.3, V_{VM} - 1.25)	V
T_A	Operating ambient temperature		–40		125	°C

over operating temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_J	Operating junction temperature	–40		150	°C

(1) Power dissipation and thermal limits must be observed

6.4 Thermal Information

THERMAL METRIC(1)		DEVICE RTE (WQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	22.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	8.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

0 V ≤ V_{VM} ≤ 11 V and 1.65 V ≤ V_{VCC} ≤ 11 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted).
Typical values are at T_J = 27°C, V_{VM} = 5 V, V_{VCC} = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VM, VCC)						
I_{VMQ}	VM sleep mode current	nSLEEP = 0 V, V_{VM} = 5 V, V_{VCC} = 3.3 V, T_J = 27°C, OVP disabled		100	170	nA
I_{VMQ_OVP}	VM sleep mode current	nSLEEP = 0 V, V_{VM} = 5 V, V_{VCC} = 3.3 V, T_J = 27°C, OVP enabled		0.1	1	µA
I_{VM}	VM active mode current	nSLEEP = 3.3 V, EN/IN1 = 3.3 V, PH/IN2 = 0 V, V_{VM} = 5 V, V_{VCC} = 3.3 V		1.3	1.9	mA
I_{VCCQ}	VCC sleep mode current	nSLEEP = 0 V, V_{VM} = 5 V, V_{VCC} = 3.3 V, T_J = 27°C		1	3.0	nA
I_{VCC}	VCC active mode current	nSLEEP = 3.3 V, EN/IN1 = 3.3 V, PH/IN2 = 0 V, V_{VM} = 5 V, V_{VCC} = 3.3 V		1.5	2	mA
t_{WAKE}	Turnon time	nSLEEP = 1 to I^2C ready			410	µs
LOGIC-LEVEL INPUTS (EN/IN1, PH/IN2, SDA, SCL, nSLEEP)						
V_{IL}	Input logic low voltage		0		0.4	V
V_{IH}	Input logic high voltage		1.45		5.5	V
V_{HYS}	Input hysteresis		49			mV
I_{IL}	Input logic low current	V_I = 0 V	-1		1	µA
I_{IH}	Input logic high current	V_I = 5 V	15		35	µA
R_{PD}	Input pulldown resistance, INx			200		kΩ
$t_{DEGLITCH}$	Input logic deglitch, INx			50		ns
TRI-LEVEL INPUTS (A1, A0)						
V_{THYS}	Tri-level input logic low voltage		0		0.4	V
I_{TIL}	Tri-level input Hi-Z voltage		0.75		1.05	V
I_{TIZ}	Tri-level input logic high voltage		1.45		5.5	V
R_{TPD}	Tri-level pulldown resistance	to GND		90		kΩ
I_{TPU}	Tri-level pullup current	to VCC		10		µA

0 V ≤ V_{VM} ≤ 11 V and 1.65 V ≤ V_{VCC} ≤ 11 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted).
Typical values are at T_J = 27°C, V_{VM} = 5 V, V_{VCC} = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPEN-DRAIN OUTPUTS (nFAULT, SDA)						
V_{OL}	Output logic low voltage	I_{OD} = 5 mA			0.4	V
I_{OZ}	Output logic high current	V_{OD} = VCC	-1		1	µA
t_{PW_nFAULT}	nFAULT low pulse width	RC Count overflow, RC_REP = 11b	30	50	70	µs
C_B	SDA capacitive load for each bus line				400	pF
DRIVER OUTPUTS (OUTx)						
$R_{DS(ON)\_HS}$	High-side MOSFET on resistance	I_{OUTx} = 1 A; T_J = 25 °C		120	155	mΩ
$R_{DS(ON)\_HS}$	High-side MOSFET on resistance	I_{OUTx} = 1 A; T_J = 125 °C		180	220	mΩ
$R_{DS(ON)\_HS}$	High-side MOSFET on resistance	I_{OUTx} = 1 A; T_J = 150 °C		200	250	mΩ
$R_{DS(ON)\_LS}$	Low-side MOSFET on resistance, CS_GAIN_SEL = 00Xb	I_{OUTx} = -1 A; T_J = 25 °C		120	145	mΩ
$R_{DS(ON)\_LS}$	Low-side MOSFET on resistance, CS_GAIN_SEL = 00Xb	I_{OUTx} = -1 A; T_J = 125 °C		180	220	mΩ
$R_{DS(ON)\_LS}$	Low-side MOSFET on resistance, CS_GAIN_SEL = 00Xb	I_{OUTx} = -1 A; T_J = 150 °C		200	250	mΩ
$R_{DS(ON)\_LS}$	Low-side MOSFET on resistance, CS_GAIN_SEL = 01Xb	I_{OUTx} = -250 mA; T_J = 25 °C		440	530	mΩ
$R_{DS(ON)\_LS}$	Low-side MOSFET on resistance, CS_GAIN_SEL = 01Xb	I_{OUTx} = -250 mA; T_J = 125 °C		660	800	mΩ
$R_{DS(ON)\_LS}$	Low-side MOSFET on resistance, CS_GAIN_SEL = 01Xb	I_{OUTx} = -250 mA; T_J = 150 °C		750	900	mΩ
$R_{DS(ON)\_LS}$	Low-side MOSFET on resistance, CS_GAIN_SEL = 11Xb	I_{OUTx} = -50 mA; T_J = 25 °C		2040	2450	mΩ
$R_{DS(ON)\_LS}$	Low-side MOSFET on resistance, CS_GAIN_SEL = 11Xb	I_{OUTx} = -50 mA; T_J = 125 °C		3050	3650	mΩ
$R_{DS(ON)\_LS}$	Low-side MOSFET on resistance, CS_GAIN_SEL = 11Xb	I_{OUTx} = -50 mA; T_J = 150 °C		3450	4150	mΩ
V_{SD}	Body diode forward voltage	I_{OUTx} = -1 A		0.9		V
t_{RISE}	Output rise time	V_{OUTx} rising from 10% to 90% of V_{VM}		100		ns
t_{FALL}	Output fall time	V_{OUTx} falling from 90% to 10% of V_{VM}		50		ns
t_{PD}	Input to output propagation delay	Input to OUTx		650		ns
t_{DEAD}	Output dead time			500		ns
CURRENT SENSE AND REGULATION (IPROPI, VREF)						
V_{REF_INT}	Internal reference voltage	INT_VREF = 1b	480	500	520	mV
A_{IPROPI_H}	Current scaling factor	CS_GAIN_SEL = 000b, 350 mA to 2A		244		µA/A
A_{IPROPI_M}	Current scaling factor	CS_GAIN_SEL = 010b, 60 mA to 350 mA		1156		µA/A
A_{IPROPI_L}	Current scaling factor	CS_GAIN_SEL = 110b, 10 mA to 60 mA		5320		µA/A
A_{ERR_H}	Current mirror total error, CS_GAIN_SEL = 000b	I_{OUT} = 1 A, V_{IPROPI} ≤ min(VM-1.25 V, 3.3 V), 3.3 V ≤ V_{VM} ≤ 11 V	-5		5	%
		I_{OUT} = 1 A, V_{IPROPI} ≤ min(VM-1.25 V, 3.3 V), 1.65 V ≤ V_{VM} ≤ 3.3 V	-5		5	%
A_{ERR_M}	Current mirror total error, CS_GAIN_SEL = 010b	I_{OUT} = 250 mA, V_{IPROPI} ≤ min(VM-1.25 V, 3.3 V), 3.3 V ≤ V_{VM} ≤ 11 V	-5		5	%
		I_{OUT} = 250 mA, V_{IPROPI} ≤ min(VM-1.25 V, 3.3 V), 1.65 V ≤ V_{VM} ≤ 3.3 V	-5		5	%

0 V ≤ V_{VM} ≤ 11 V and 1.65 V ≤ V_{VCC} ≤ 11 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted).
Typical values are at T_J = 27°C, V_{VM} = 5 V, V_{VCC} = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
A_{ERR_L}	Current mirror total error, CS_GAIN_SEL = 110b	I_{OUT} = 50 mA, V_{IPROPI} ≤ min(VM-1.25 V, 3.3 V), 3.3 V ≤ V_{VM} ≤ 11 V	-6.5		6.5	%
		I_{OUT} = 50 mA, V_{IPROPI} ≤ min(VM-1.25 V, 3.3 V), 1.65 V ≤ V_{VM} ≤ 3.3 V	-6.5		6.5	%
t_{OFF}	Current regulation off time			20		µs
t_{BLANK}	Current sense blanking time	TBLANK = 0b		1.8		µs
t_{BLANK}	Current sense blanking time	TBLANK = 1b		1		µs
t_{DEG}	Current regulation and stall detection deglitch time	TDEG = 0b		2		µs
t_{DEG}	Current regulation and stall detection deglitch time	TDEG = 1b		1		µs
t_{INRUSH}	Inrush time blanking for stall detection		5		6716	ms
Voltage regulation						
ΔV_{LINE}	Line regulation	4 V ≤ V_{VM} ≤ 11 V, V_{VCC} = 3.3 V, V_{OUT} = 3.3 V, I_{OUT} = 2 A		±1%		
ΔV_{LOAD}	Load regulation	V_{VM} = 5 V, V_{VCC} = 3.3 V, V_{OUT} = 3.3 V, I_{OUT} = 100 mA to 2 A		±3%		
PROTECTION CIRCUITS						
V_{UVLO_VCC}	VCC supply undervoltage lockout (UVLO)	Supply rising			1.65	V
		Supply falling	1.30			V
V_{UVLO_HYS}	Supply UVLO hysteresis	Rising to falling threshold		120		mV
t_{UVLO}	Supply undervoltage deglitch time	V_{VCC} falling to OUTx disabled		10		µs
V_{OVP_TH}	Overvoltage protection threshold	V_{OUT} - V_{VM}		200		mV
t_{OVP_ON}	Overvoltage protection turn-on time			13		µs
t_{OVP_OFF}	Overvoltage protection turn-off time			250		µs
I_{OCP}	Overcurrent protection trip point, CS_GAIN_SEL = 000b		4			A
I_{OCP}	Overcurrent protection trip point, CS_GAIN_SEL = 010b		0.8			A
I_{OCP}	Overcurrent protection trip point, CS_GAIN_SEL = 110b		0.16			A
t_{OCP}	Overcurrent protection deglitch time			2		µs
t_{RETRY}	Retry time			1.7		ms
T_{TSD}	Thermal shutdown temperature		157	175	193	°C
T_{HYS}	Thermal shutdown hysteresis			18		°C

6.6 I2C Timing Requirements

		MIN	NOM	MAX	UNIT
STANDARD MODE					
f_{SCL}	SCL Clock frequency	0		100	kHz
$t_{HD,STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4			µs
t_{LOW}	LOW period of the SCL clock	4.7			µs
t_{HIGH}	HIGH period of the SCL clock	4			µs
$t_{SU,STA}$	Setup time for a repeated START condition	4.7			µs
$t_{HD,DAT}$	Data hold time: For I2C bus devices	0.035		3.45	µs
$t_{SU,DAT}$	Data set-up time	250			ns

		MIN	NOM	MAX	UNIT
t_R	SDA and SCL rise time			1000	ns
t_F	SDA and SCL fall time			300	ns
$t_{SU,STO}$	Set-up time for STOP condition	4			µs
t_{BUF}	Bus free time between a STOP and START condition	4.7			µs
FAST MODE					
f_{SCL}	SCL Clock frequency	0		400	kHz
$t_{HD,STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	0.6			µs
t_{LOW}	LOW period of the SCL clock	1.3			µs
t_{HIGH}	HIGH period of the SCL clock	0.6			µs
$t_{SU,STA}$	Setup time for a repeated START condition	0.6			µs
$t_{HD,DAT}$	Data hold time: For I2C bus devices	0.035		0.9	µs
$t_{SU,DAT}$	Data set-up time	250			ns
t_R	SDA and SCL rise time			300	ns
t_F	SDA and SCL fall time			300	ns
$t_{SU,STO}$	Set-up time for STOP condition	0.6			µs
t_{BUF}	Bus free time between a STOP and START condition	1.3			µs
t_{SP}	Pulse width of spikes to be supressed by input noise filter		50		ns

6.7 Timing Diagrams

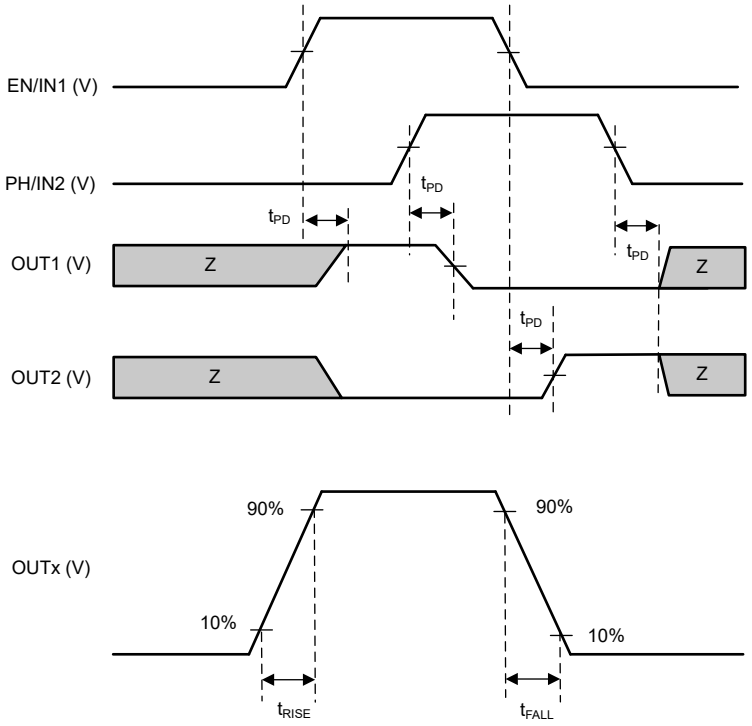


図 6-1. Input-to-Output Timing Diagram

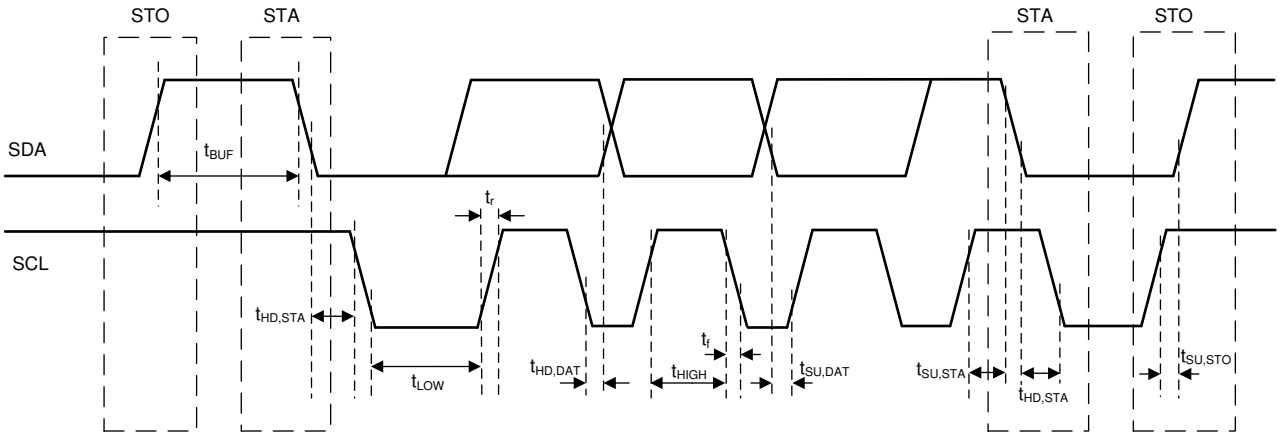


図 6-2. I²C Timing Diagram

6.8 Typical Operating Characteristics

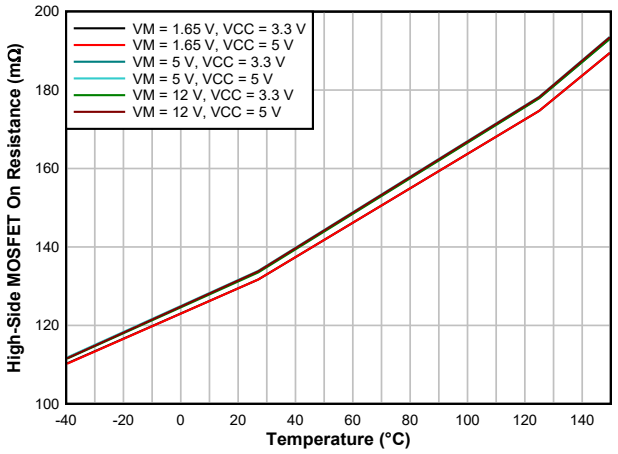


図 6-3. High-Side MOSFET On Resistance (mΩ)

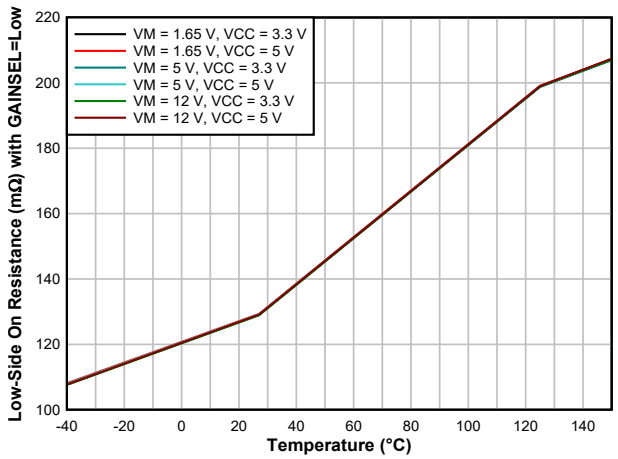


図 6-4. Low-Side MOSFET On Resistance (mΩ) with GAINSEL=Low (000b)

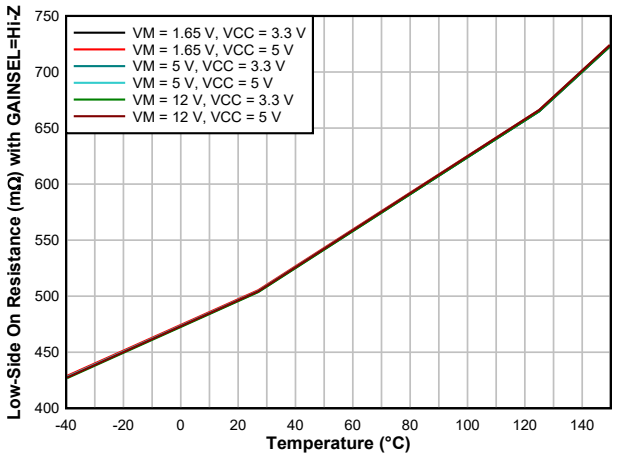


図 6-5. Low-Side MOSFET On Resistance (mΩ) with GAINSEL=Hi-Z (010b)

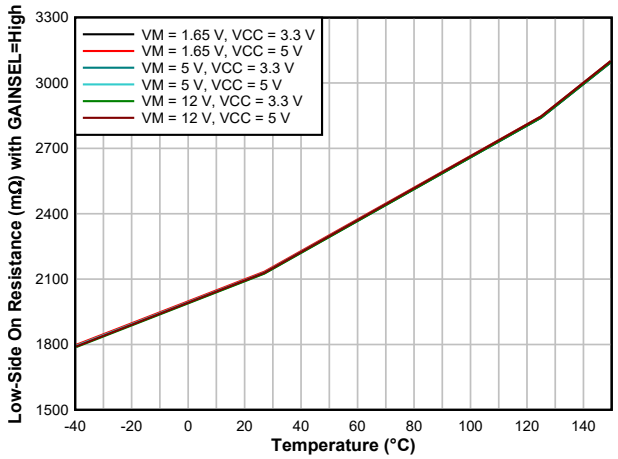


図 6-6. Low-Side MOSFET On Resistance (mΩ) with GAINSEL=High (110b)

7 Detailed Description

7.1 Overview

The DRV8215 is a high-performance integrated H-bridge motor driver with integrated speed and voltage regulation along with additional integrated features like stall detection, current sense output, current regulation, and protection circuitry.

The integrated speed regulation feature maintains maintains constant motor speed over varying battery voltages. The voltage regulation feature saves energy by driving the motor with a programmable lower terminal voltage. control in the device thereby reducing external components on a PCB and saving cost. The principle is based on counting the number of current ripples appearing in the motor current waveform due to commutations.

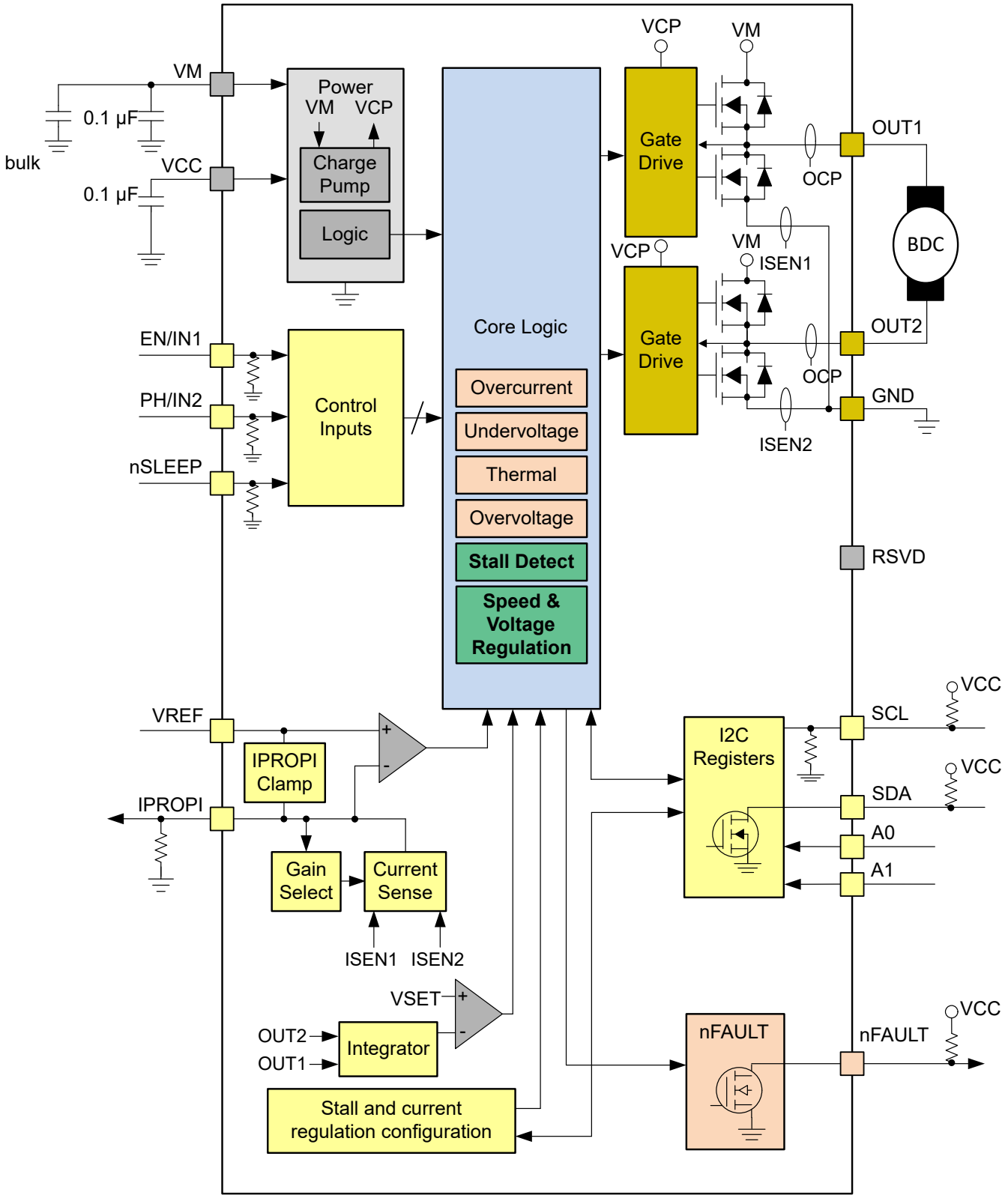
The DRV8215 contains PWM and PH/EN interfaces along with an I^2C interface for configuration and detailed diagnostics. The EN/IN1 & PH/IN2 pins control the full bridge, which consists of four N-channel MOSFETs that have a typical $R_{DS(ON)}$ of 240mΩ (including one high-side and one low-side FET). Motor speed can be controlled with pulse-width modulation (PWM), at frequencies between 0 to 200kHz. The PMODE bit in I^2C registers allows to control the H-bridge solely through I^2C commands, reducing the number of GPIO inputs.

The integrated current regulation feature limits motor current to a predefined maximum based on the VREF and IPROPI settings. The IPROPI signal can provide current feedback to a microcontroller during both the drive and brake/slow-decay states of the H-bridge. The gain select bits allow high accuracy current sensing down to 10 mA average motor current. The $R_{DS(ON)}$ of the low-side MOSFET and the overcurrent protection limit changes according to the gain select bits, thereby leading to optimized solutions for different values of motor current. The DRV8215 also has I^2C programmable registers to configure a hardware stall detection feature based on the IPROPI current sensing signal.

The integrated protection features protect the device in case of a system fault. These include undervoltage lockout (UVLO), overcurrent protection (OCP), and overtemperature shutdown (TSD). Fault conditions are indicated on the nFAULT pin. Additionally, the overvoltage protection (OVP) feature puts the driver into the brake state when the motor is spun manually while the device is in sleep mode or when the H-bridge is disabled. This prevents the back EMF induced high voltages on the supply rail that could potentially damage the driver and other circuits in the system.

To reduce area and external components on a printed circuit board, the device integrates a charge pump regulator and the corresponding capacitors. The separate full-bridge (VM) and logic (VCC) supplies allow the full-bridge supply voltage to drop to 0V without significant impact to $R_{DS(ON)}$ and without triggering UVLO as long as the VCC supply is stable. The nSLEEP pin provides an ultra-low power mode to minimize current draw during system inactivity.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 External Components

表 7-1 lists the recommended external components for the device.

表 7-1. Recommended External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_{VM1}	VM	GND	0.1-µF, low ESR ceramic capacitor, VM-rated.
C_{VM2}	VM	GND	Bulk Capacitance, VM-rated.
C_{VCC}	VCC	GND	0.1-µF, low ESR ceramic capacitor, VM-rated.
R_{IPROPI}	IPROPI	GND	Resistor from IPROPI pin to GND, sets the current regulation level.
R_{nFAULT}	VCC	nFAULT	10 kΩ
$R_{Pull-up}$	SDA, SCL, A0, A1	VM	2.2 kΩ

7.3.2 Summary of Features

This section includes a summary of the key and advanced features of DRV8215.

1. DRV8215 Functional Block Diagram
2. Current Sense and Regulation (IPROPI)
3. Bridge Control
4. Protection
5. Advanced: Stall Detection
6. Advanced: Speed and Voltage Regulation
7. Advanced: Soft-Start and Soft-Stop using t_{INRUSH}

7.3.3 Bridge Control

The DRV8215 output consists of four N-channel MOSFETs designed to drive high current. These outputs are controlled by the two inputs EN/IN1 and PH/IN2 or the I^2C bits I2C_EN_IN1 and I2C_PH_IN2.

The I2C_BC bit determines whether the bridge is controlled by the EN/IN1 and PH/IN2 pins or the I2C_EN_IN1 and I2C_PH_IN2 bits, as shown below.

表 7-2. H-Bridge Control Interface

I2C_BC	Description
0b	Bridge control configured by using the EN/IN1 and PH/IN2 pins.
1b	Bridge control configured by using the I2C_EN_IN1 and I2C_PH_IN2 bits.

The control interface is selected by the PMODE bit. DRV8215 allows users to choose either Phase-Enable mode or PWM mode, as described below.

表 7-3. PMODE Functions

PMODE	Control Mode
0b	PH/EN
1b	PWM

The inputs can be set to static voltages for 100% duty cycle drive, or they can be pulse-width modulated (PWM) for variable motor speed. Following diagram shows how the motor current flows through the H-bridge. The input pins can be powered before VM or VCC are applied.

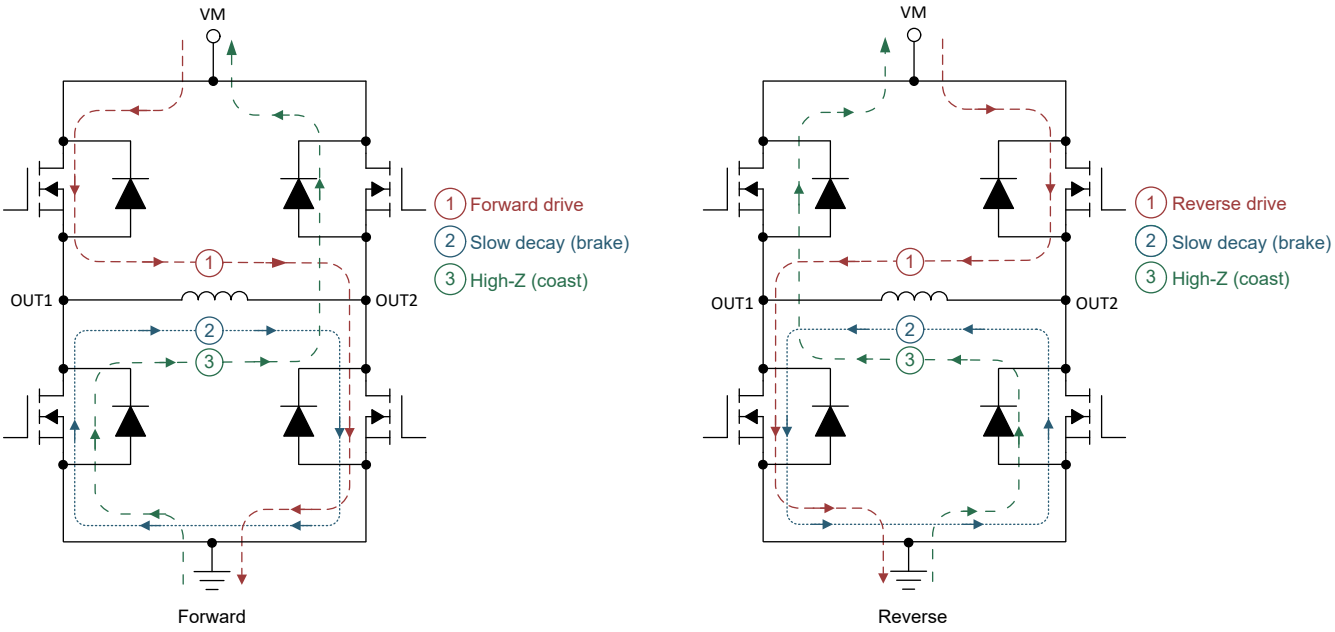


図 7-1. H-Bridge Current Paths

The truth tables for each control mode are shown below. Note that these tables do not take into account the internal current regulation feature. Additionally, when an output changes from driving high to driving low (or driving low to driving high), dead time is automatically inserted to prevent shoot-through.

PH/EN mode allows for the H-bridge to be controlled with a speed and direction type of interface. The truth table for PH/EN mode is shown below.

表 7-4. PH/EN Control Mode (PMODE = 0b)

nSLEEP	Enable	Phase	OUT1	OUT2	Description
0	X	X	High-Z	High-Z	Sleep Mode (H-bridge High-Z)
1	1	0	L	H	Reverse (Current OUT2 → OUT1)
1	1	1	H	L	Forward (Current OUT1 → OUT2)
1	0	X	L	L	Brake; low-side slow decay

注

Enable refers to the EN pin when bridge control is external (I2C_BC=0b), and the I2C_EN_IN1 bit when bridge control is internal (I2C_BC=1b).

Phase refers to the PH pin when bridge control is external (I2C_BC=0b), and the I2C_PH_IN2 bit when bridge control is internal (I2C_BC=1b).

PWM mode allows for the H-bridge to enter the High-Z state while the device is awake. The truth table for PWM mode is shown below.

表 7-5. PWM Control Mode (PMODE = 1b)

nSLEEP	Input1	Input2	OUT1	OUT2	Description
0	X	X	High-Z	High-Z	Sleep Mode (H-bridge High-Z)
1	0	0	High-Z	High-Z	Coast (H-bridge High-Z)
1	0	1	L	H	Reverse (Current OUT2 → OUT1)
1	1	0	H	L	Forward (Current OUT1 → OUT2)
1	1	1	L	L	Brake; low-side slow decay

注

Input1 refers to the IN1 pin when bridge control is external (I2C_BC=0b), and the I2C_EN_IN1 bit when bridge control is internal (I2C_BC=1b).

Input2 refers to the IN2 pin when bridge control is external (I2C_BC=0b), and the I2C_PH_IN2 bit when bridge control is internal (I2C_BC=1b).

The following timing diagram shows the timing of the inputs and outputs of the motor driver.

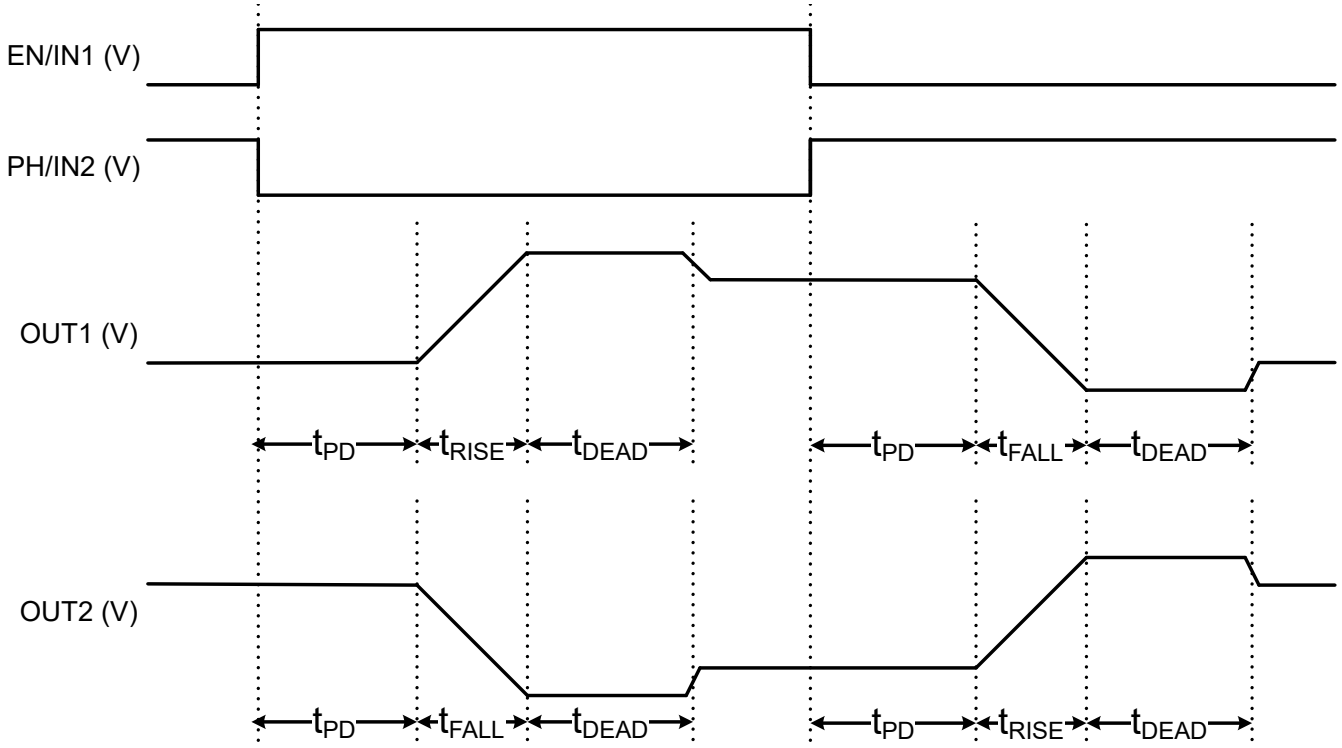


図 7-2. H-Bridge Timing Diagram

The t_{DEAD} time is the time in the middle when the output is High-Z. The output pin voltage during t_{DEAD} depends on the direction of the output current. If the current is sourced from the pin, the voltage is a diode voltage drop below ground. If the current is sunk to pin, the voltage is a diode voltage drop above VM. This diode is the body diode of the high-side or low-side FET.

The propagation delay time (t_{PD}) is measured as the time between an input edge to output change. This time accounts for input deglitch time and other internal logic propagation delays. The input deglitch time prevents noise on the input pins from affecting the output state. Additional output slew delay timing accounts for FET turn on or turn off times (t_{RISE} and t_{FALL}).

7.3.4 Current Sense and Regulation (IPROPI)

The DRV8215 integrates current sensing, regulation, and current sense feedback. The internal current mirror allows the device to sense the output current without an external sense resistor or sense circuitry, thereby reducing system size, cost, and complexity. The current regulation feature allows for the device to limit the output current in case of motor stall or high load torque events. The IPROPI output provides a current output proportional to the load current. This I_{IPROPI} current can be converted to a V_{IPROPI} output voltage by connecting a suitable resistor R_{IPROPI} from this pin to the circuit ground.. The following diagram shows the IPROPI timings specified in the Electrical Characteristics table.

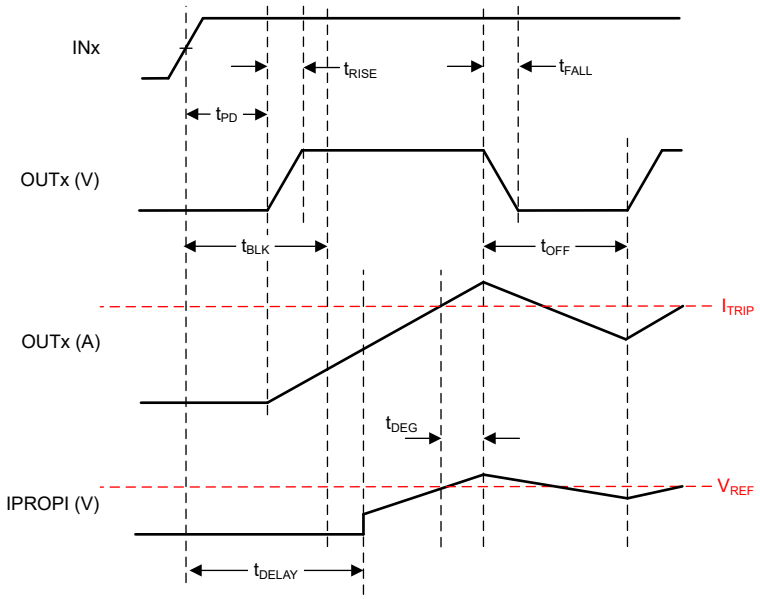


図 7-3. Detailed IPROPI Timing Diagram

7.3.4.1 Current Sensing and Current Mirror Gain Selection

The IPROPI pin outputs an analog current proportional to the current flowing through the low-side power MOSFETs in the H-bridge and scaled by the current mirror gain (A_{IPROPI}). The IPROPI output current can be calculated by the following equation. The I_{LSx} in the equation is only valid when the current flows from drain to source in the low-side MOSFET. If current flows from source to drain or through the body diode, the value of I_{LSx} for that channel is zero. For instance, if the bridge is in the brake, slow-decay state, then the current out of IPROPI is only proportional to the current in one of the low-side MOSFETs.

$$I_{PROPI}\ (\mu A) = (I_{LS1} + I_{LS2})\ (A) \times A_{IPROPI}\ (\mu A/A) \quad (1)$$

The A_{ERR} parameter in the Electrical Characteristics table is the error associated with the A_{IPROPI} gain. It indicates the combined effect of offset error added to the I_{OUT} current and gain error.

The current mirror gain A_{IPROPI} depends on the CS_GAIN_SEL bit setting, as shown in the table below -

表 7-6. Recommended settings for CS_GAIN_SEL

CS_GAIN_SEL	A_{IPROPI}	Recommended Current Range	Low-side FET $R_{DS(ON)}$	Minimum OCP Limit
000b	244 µA/A	350 mA to 2A	120 mΩ	4 A
010b	1156 µA/A	60 mA to 350 mA	440 mΩ	800 mA
110b	5320 µA/A	10 mA to 60 mA	2040 mΩ	160 mA

CS_GAIN_SEL bits therefore allows optimizing the design for various applications by reducing OCP limit and increasing current mirror gain at lower motor currents.

The motor current is measured by an internal current mirror architecture on the low-side FETs which removes the need for an external power sense resistor as shown below. The current mirror architecture senses motor winding current in both the drive and brake low-side slow-decay periods, therefore allowing continuous current monitoring in typical bidirectional brushed DC motor applications. In coast mode, the current is freewheeling and cannot be sensed because it flows from source to drain. However, the current can be sampled by briefly reenabling the driver in either drive or slow-decay modes and measuring the current before switching back to coast mode again.

表 7-7 lists the overall CS_GAIN_SEL settings with the maximum current values.

表 7-7. CS_GAIN_SEL Settings

Bit	Maximum Current Value	A_{IPROPI}
000b	4 A	244 µA/A
001b	2 A	244 µA/A
010b	1 A	1156 µA/A
011b	0.5 A	1156 µA/A
1X0b	0.25 A	5320 µA/A
1X1b	0.125 A	5320 µA/A

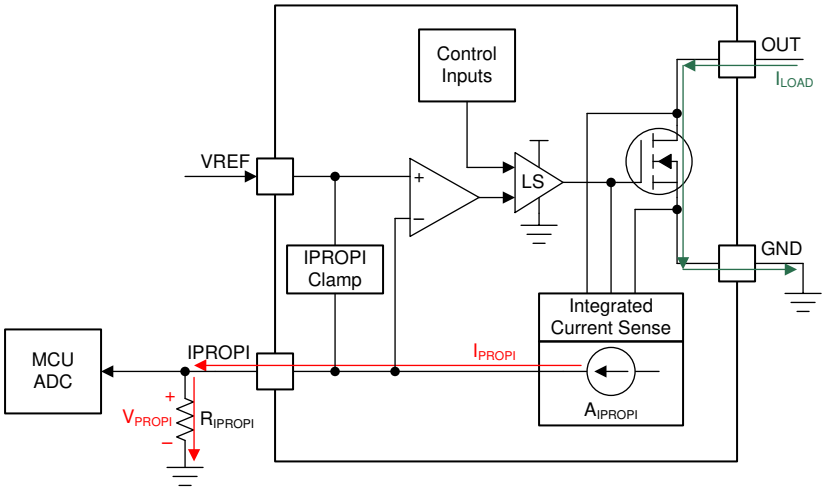


図 7-4. Integrated Current Sensing

The IPROPI pin should be connected to an external resistor (R_{IPROPI}) to ground in order to generate a proportional voltage (V_{IPROPI}) on the IPROPI pin with the I_{IPROPI} analog current output. This allows for the load current to be measured as the voltage drop across the R_{IPROPI} resistor with a standard analog to digital converter (ADC). The R_{IPROPI} resistor can be sized based on the expected load current in the application so that the full range of the controller ADC is utilized.

Additionally, the DRV8215 implements an internal IPROPI voltage clamp circuit to limit V_{IPROPI} with respect to V_{VREF} on the VREF pin and protect the external ADC in case of output overcurrent or unexpected high current events. TI recommends designing for at least 1.25 V of headroom between V_{VM} and the maximum V_{IPROPI} voltage to be measured by the ADC, V_{IPROPI_MAX}. This ensures good accuracy across the range of VIPROPI voltages measured by the ADC. For instance, if V_{VM} is 4.55 V to 11 V, V_{IPROPI_MAX} can be as high as 3.3 V. However, if V_{VM} is 3.3 V, then VIPROPI will have good accuracy up to 2.05 V.

The corresponding IPROPI voltage to the output current can be calculated as shown below -

$$V_{IPROPI}\ (V) = I_{PROPI}\ (A) \times R_{IPROPI}\ (\Omega) \quad (2)$$

The IPROPI output bandwidth is limited by the sense delay time (t_{DELAY}) of the internal current sensing circuit. This time is the delay from the low-side MOSFET enable command (from the INx pins) to the IPROPI output being ready.

If the device is alternating between drive and slow-decay (brake) in an H-bridge PWM pattern then the low-side MOSFET sensing the current is continuously on and the sense delay time has no impact to the IPROPI output. If a command on the INx pins disables the low-side MOSFETs (according to the truth tables), the IPROPI output will disable with the input logic signal. Although the low-side MOSFETs may still conduct current as they disable according to the device slew rate (specified in the Electrical Characteristics table by t_{RISE} time), IPROPI will not represent the current in the low-side MOSFETs during this turnoff time.

7.3.4.2 Current Regulation

The DRV8215 integrates current regulation using either a fixed off-time or a cycle-by-cycle PWM current regulation scheme. This allows the device to limit the output current in case of a motor stall, high torque, or other high current load events autonomously. The current regulation scheme is selectable by the REG_CTRL bit in I^2C.

The internal current regulation can be disabled by tying IPROPI to GND and setting the VREF pin voltage greater than GND if current feedback is not required. Additionally, current regulation can also be disabled by setting IMODE to 00b as explained below. If current feedback is required and current regulation is not required, set V_{VREF} and R_{IPROPI} such that V_{IPROPI} never reaches the V_{VREF} threshold. For proper operation of the current regulation circuit, V_{VREF} must be within the range of the VREF pin voltage specified in the Recommended Operating Conditions table.

表 7-8. REG_CTRL Functions

Bit*	Current Regulation Mode
00b	Fixed Off-Time
01b	Cycle-By-Cycle

注

*Additional REG_CTRL options 10b and 11b allow selection between motor voltage or speed regulation described in セクション 7.3.6.2.1.

The current regulation threshold (I_{TRIP}) is set through a combination of the VREF voltage (V_{VREF}) and IPROPI output resistor (R_{IPROPI}). This is done by comparing the voltage drop across the external R_{IPROPI} resistor to V_{VREF} with an internal comparator.

$$I_{TRIP}\ (A) \times A_{IPROPI}\ (\mu A/A) = V_{VREF}\ (V) / R_{IPROPI}\ (\Omega) \quad (3)$$

For example, if V_{VREF} = 3.3 V, R_{IPROPI} = 7500 Ω and A_{IPROPI} = 225 µA/A, then I_{TRIP} will be approximately 1.96 A.

V_{VREF} must be lower than V_{VM} by at least 1.25 V. The maximum recommended value of V_{VREF} is 3.3 V. If INT_VREF bit is set to 1b, V_{VREF} is internally selected with a fixed value of 500 mV.

The I_{TRIP} comparator has both a blanking time (t_{BLANK}) and a deglitch time (t_{DEG}). The internal blanking time helps to prevent voltage and current transients during output switching from affecting the current regulation. These transients may be caused by a capacitor inside the motor or motor terminals. The internal deglitch time ensures that transient conditions do not prematurely trigger the current regulation. In certain cases where the transient conditions are longer than the deglitch time, placing a 10-nF capacitor on the IPROPI pin, close to the device, helps filter the transients on IPROPI output so current regulation does not prematurely trigger. The capacitor value can be modified as needed, however large capacitor values may slow down the response time of the current regulation circuit.

The IMODE bits determine the behavior of current regulation for the motor driver.

- When IMODE is 00b, current regulation is disabled.
- When IMODE is 01b, the device performs current regulation only during the t_{INRUSH} time when stall detection is enabled.
- When IMODE is 10b, current regulation is enabled at all times.

The following table summarizes the IMODE bit settings.

表 7-9. IMODE configuration

IMODE	EN_STALL	Description
00b	X	No current regulation at any time
01b	0b	Current regulation at all times
	1b	Current regulation during t_{INRUSH} only
1Xb	X	Current regulation at all times

7.3.4.2.1 Fixed Off-Time Current Regulation

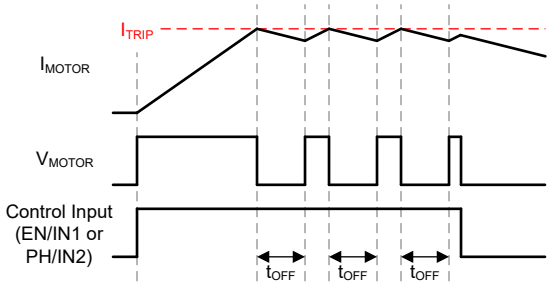


図 7-5. Fixed Off-Time Current Regulation

In the fixed off-time mode, the H-bridge enters a brake/low-side slow decay state (both low-side MOSFETs ON) for t_{OFF} duration after I_{OUT} exceeds I_{TRIP}. After t_{OFF} the outputs are re-enabled according to the control inputs unless I_{OUT} is still greater than I_{TRIP}. If I_{OUT} is still greater than I_{TRIP}, the H-bridge will enter another period of brake/low-side slow decay for t_{OFF}. If the state of the EN/IN1 or PH/IN2 control pin inputs or I2C_EN_IN1 or I2C_PH_IN2 bits changes during the t_{OFF} time, the remainder of the t_{OFF} time is ignored, and the outputs will again follow the inputs.

The fixed off-time mode allows for a simple current regulation scheme independent of the external controller. Fixed off-time mode will support 100% duty cycle current regulation since the H-bridge automatically enables after the t_{OFF} period and does not require a new control input edge on the control input pins or bits to reset the outputs.

7.3.4.2.2 Cycle-By-Cycle Current Regulation

In cycle-by-cycle mode, the H-bridge enters a brake, low-side slow decay state (both low-side MOSFETs ON) after I_{OUT} exceeds I_{TRIP} until the next control input edge on either the EN/IN1 or PH/IN2 pins or 0 to 1 transitions on the I2C_EN_IN1 or I2C_PH_IN2 bits. This allows for additional control of the current regulation by the external controller. This is shown in the diagram below. Cycle-by-cycle mode will not support 100% duty cycle current regulation as a new control input edge is required to reset the outputs after the brake, low-side slow decay state has been entered.

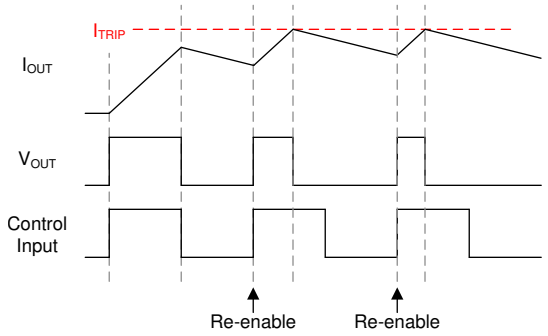


図 7-6. Cycle-By-Cycle Current Regulation

In cycle-by-cycle mode, the device can indicate whenever the H-bridge enters internal current regulation by pulling the nFAULT pin low. This can be used to determine when the device outputs will differ from the control inputs or the load has reached the I_{TRIP} threshold. This behavior is controlled by the CBC_REP bit. This is shown in the following diagram. In cycle-by-cycle mode, if the CBC_REP bit is 1b, nFAULT will be pulled low when the H-bridge enters internal current regulation and nFAULT will be released whenever the next control input edge is received by the device and the outputs are reset.

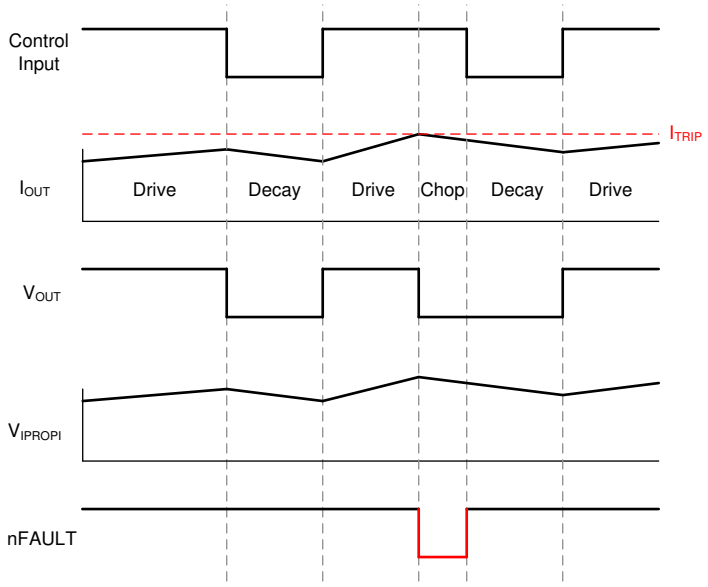


図 7-7. Cycle-By-Cycle Current Regulation, CBC_REP = 1b

No device functionality is affected when the nFAULT pin is pulled low for the current regulation indicator. The nFAULT pin is only used as an indicator and the device will continue normal operation. To distinguish a device fault from the current regulation indicator, the nFAULT pin can be compared with the control inputs. The current regulation indicator can only assert when the control inputs are commanding a forward or reverse drive state. If the nFAULT pin is pulled low and the control inputs are commanding the high-Z or slow-decay states, then a device fault has occurred.

7.3.5 Stall Detection

The DRV8215 integrates a stall detection feature. The principle of the stall detection scheme relies on the fact that motor current increases during stall conditions. The DRV8215 compares the voltage on the IPROPI pin to the voltage on the VREF pin or 500 mV to determine whether a motor stall condition has occurred. The setting is deterimed by the INT_VREF register. 表 7-10 shows the configurable options for INT_VREF. The following paragraphs describe how to configure the I^2C registers for the desired stall detection response.

表 7-10. Settings for INT_VREF

Bit	Description
0b	V_{VREF} not fixed
1b	V_{VREF} fixed internally at 500 mV

The STALL bit in status register changes to 1b when a motor stall is detected. The EN_STALL bit is used to enable or disable stall detection. The following table summarizes the EN_STALL bit settings.

表 7-11. EN_STALL configuration

EN_STALL	Description
0b	Stall detection disabled. If IMODE = 01b, current regulation occurs at all times when $V_{IPROPI} \geq V_{VREF}$.
1b	Stall detection enabled.

The IPROPI pin provides the current sense signal to the stall detection module. The VREF pin sets the I_{TRIP} current level at which a stall condition is detected. As shown in 表 7-10, V_{VREF} is internally fixed at 500mV when INT_VREF = 1b. When $V_{IPROPI} \geq V_{VREF}$, it implies $I_{OUT} \geq I_{TRIP}$. The device detects a stall condition here. Stall detection is blanked for a period of time, t_{INRUSH}, to avoid false detection due to high inrush currents during motor startup. The IPROPI and VREF pins also support current regulation, as described earlier.

The TINRUSH[15:0] bits set the period of time the stall detection logic will ignore the inrush current during motor startup (t_{INRUSH}). After t_{INRUSH} time expires, the DRV8215 indicates a stall condition the next instant V_{IPROPI} is greater than or equal to V_{VREF}.

When voltage or speed soft-start is disabled, the t_{INRUSH} time directly reflects the setting of the TINRUSH bits. The t_{INRUSH} can be set to a value between 5ms (corresponding to 0000h) and 6.7s (corresponding to FFFFh), with a default value of 1s. Each increment of LSB corresponds to 102.4µs of the inrush time.

When voltage or speed soft-start is enabled, target motor voltage or speed is soft-started and soft-stopped for the duration of t_{INRUSH} time. The TINRUSH bits should be setup such that the t_{INRUSH} = TINRUSH bit setting x WSET_VSET. For example, if WSET_VSET = 10 and intended inrush time is 1s, then TINRUSH bit setting should correspond to 100ms.

The following conditions cause the stall detection scheme to ignore the inrush current for t_{INRUSH} time -

- Power-up of the DRV8215
- Recovering from faults
- After device exits from sleep mode
- After recovering from stall, as explained in 表 7-12

The SMODE bit programs the device's response to a stall condition. When SMODE = 0b, the outputs disable, and the STALL bit becomes 1b. When SMODE = 1b, the STALL bit becomes 1b, but the outputs continue to drive current into the motor. 表 7-12 summarizes the SMODE bit settings.

表 7-12. SMODE configuration

SMODE	Description	Recovery from Stall Condition
0b	Latched disable with indication: the OUTx pins disable and the STALL bit becomes 1b.	A clear fault must be issued by writing 1b to the CLR_FLT bit. STALL bit changes to 0b after a clear fault is issued. After waking up from stall, the stall detection scheme ignores the inrush current for t_{INRUSH} time as described earlier. After t_{INRUSH} time, if motor current is still higher than I_{TRIP}, a stall condition is detected again.
1b	Indication only: the OUTx pins remain active and the STALL bit becomes 1b.	A clear fault must be issued by writing 1b to the CLR_FLT bit to make STALL bit 0b. After t_{INRUSH} time, if motor current is still higher than I_{TRIP}, a stall condition is detected again.

The **IMODE** bits determine the behavior of current regulation in the motor driver. 表 7-9 summarizes the IMODE pin settings. For more details on current regulation, see セクション 7.3.4.2.

The STALL_REP bit determines whether stall is reported on nFAULT pin. When STALL_REP bit is 1b, nFAULT is pulled low whenever stall is detected and STALL bit is 1b. If STALL_REP bit is 0b, stall is not reported on nFAULT output.

The following diagrams show example timing diagrams for different configurations of the hardware stall detection feature.

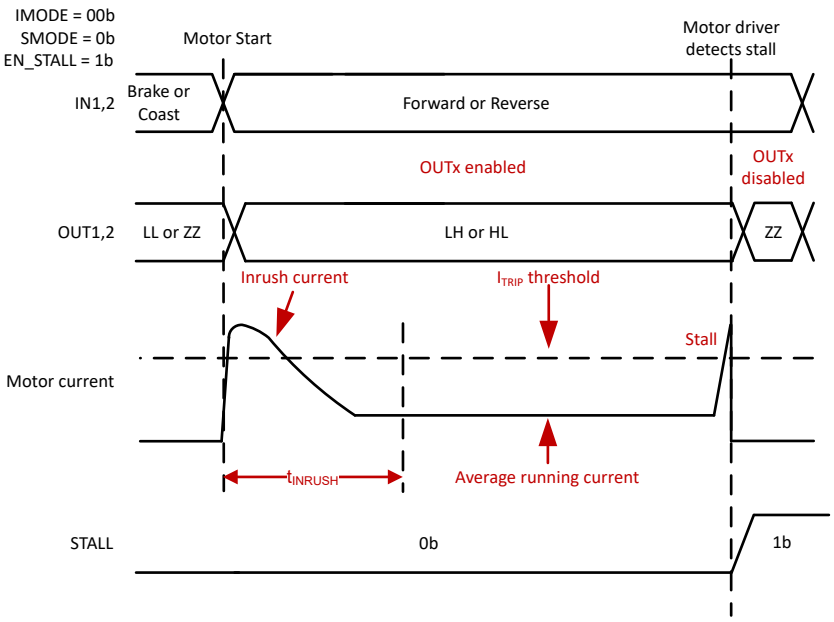


図 7-8. Stall Detection with Latched Disable

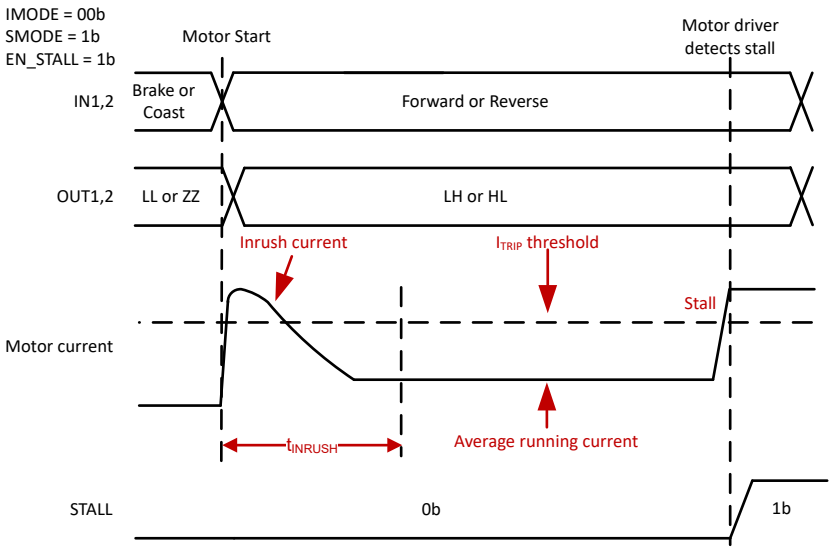


図 7-9. Stall Detection with STALL indication only

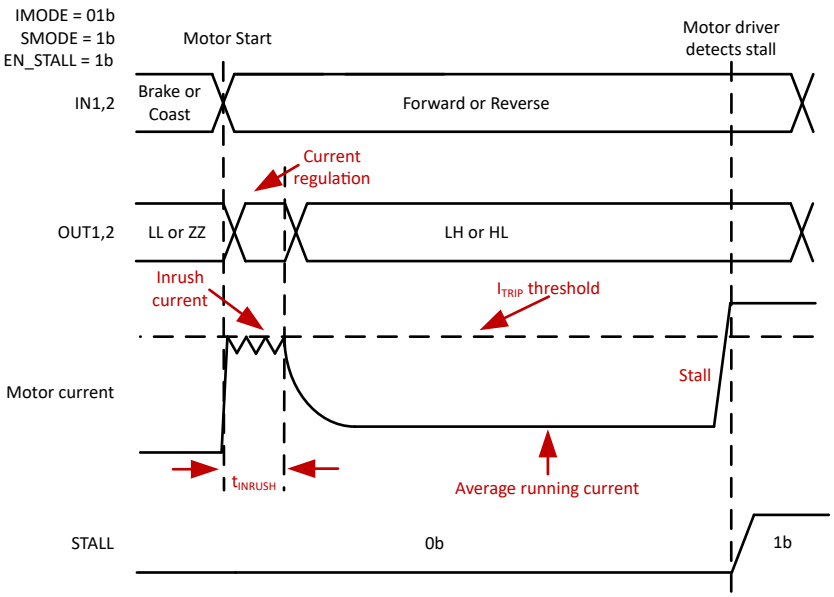


図 7-10. Stall Detection with current regulation during inrush

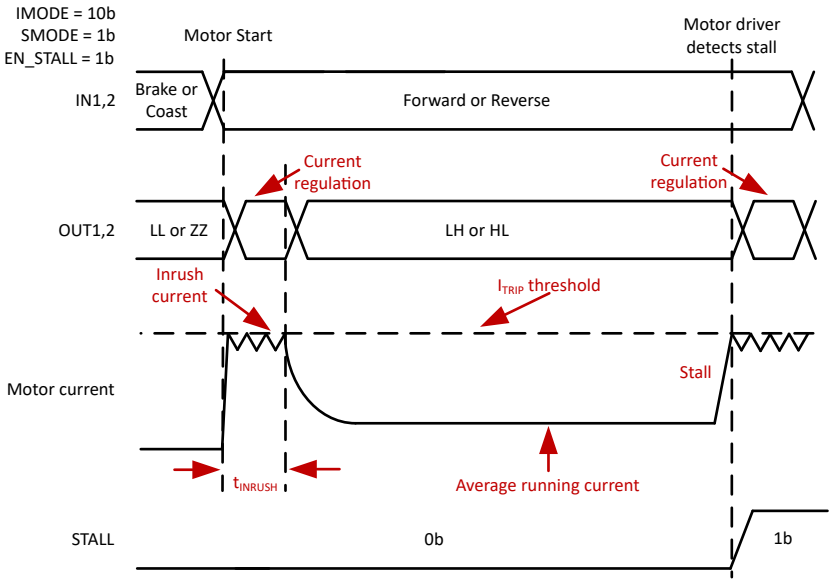


図 7-11. Stall Detection with current regulation

7.3.6 Motor Voltage and Speed Regulation

The DRV8215 provides the ability to regulate the voltage applied to the motor winding or to regulate the speed of the motor. This feature allows constant motor speed to be maintained even when operating from a varying supply voltage such as a discharging battery. The DRV8215 uses a pulse-width modulation (PWM) technique instead of a linear circuit to minimize current consumption and maximize battery life.

The intended voltage or speed can be programmed by the WSET_VSET bits. Refer to セクション 7.3.6.2.1 for further explanation.

Four ranges of motor speed can be selected using the W_SCALE bits to support low, moderate and high speed applications. The speed regulation loop compares the motor speed estimated by the speed estimator with the

user definded target speed. The following section describes the internal bridge control logic taking voltage regulation as an example, but is also applicable for speed regulation.

図 7-12 shows the closed loop PI control for regulating speed and voltage.

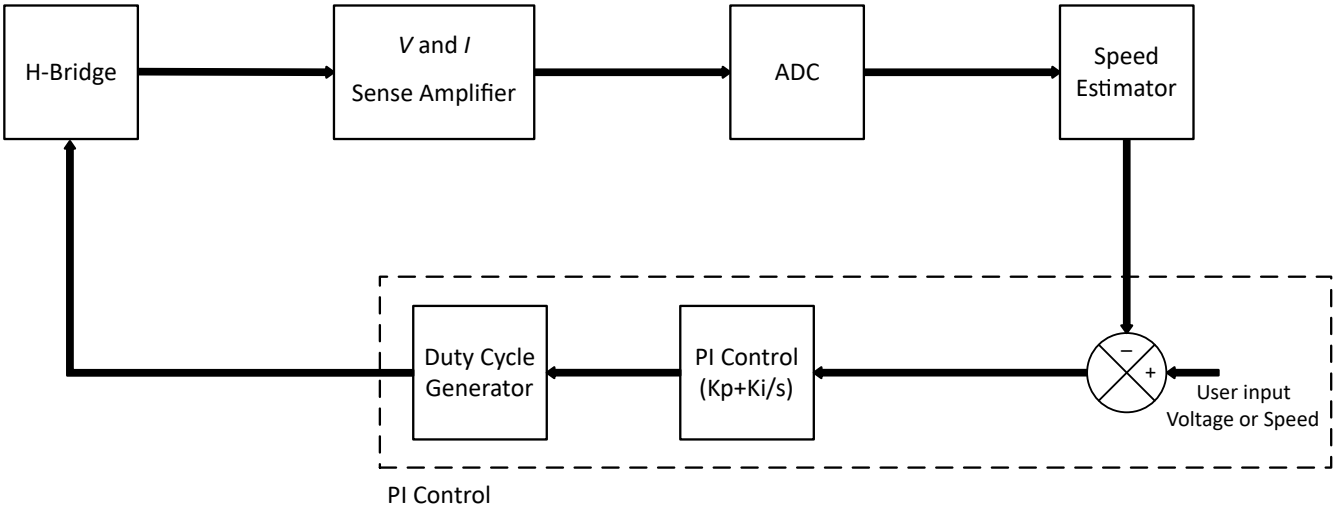


図 7-12. Speed and Voltage Regulation with PI Control

注

Please note that the sampling frequency of the ADC is 80kHz.

7.3.6.1 Internal Bridge Control

For voltage regulation, an internal circuit monitors the voltage difference between the output pins. This voltage difference is integrated over time to get an average DC voltage value. The time depends on the cut-off frequency of the output filter which can be set by the OUT_FLT register. For best results, choose a cut-off frequency equal to a value at least 20 times lower than the PWM frequency. Eg, if you PWM at 20kHz, OUT_FLT=11b (1000Hz) is sufficient.

The DC voltage value is compared to the target motor voltage programmed by the I^2C register, WSET_VSET.

When speed/voltage regulation mode is active, an internal bridge control scheme is employed. DUTY_CTRL must be set to 0b. The duty cycle cannot be manually programmed by the user.

- If the averaged output voltage is lower than VSET, the duty cycle of the internal bridge control output is increased.
- If the averaged output voltage is higher than VSET, the duty cycle of the internal bridge control output is decreased.
- During PWM regulation, the H-bridge is enabled to drive current through the motor winding during the PWM on time. The current flow direction depends on the EN/IN1 and PH/IN2 polarity.
- During the PWM off time, winding current is recirculated by enabling both of the low-side FETs in the bridge.
- If the programmed output voltage (VSET) is greater than the VM supply voltage, the device operates at 100% duty cycle and the voltage regulation feature is disabled. In this mode, the device behaves like a conventional H-bridge driver.

注

1. During Speed/Voltage regulation, the duty cycle can be read from the DUTY_READ register.
2. PWM_FREQ sets the PWM frequency for internal PWM generation. Variation around the value of PWM_FREQ is ±30%.

表 7-13. PWM_FREQ Settings

Bit	Value
0b	50 kHz
1b	25 kHz

注

In voltage regulation mode, the motor speed can vary slightly because the voltage drop across the motor coil resistance introduces a small error. The speed regulation mode eliminates this error by directly regulating the target motor speed. To enable speed regulation, the REG_CTRL bit must be set to 10b.

注

When Speed/Voltage regulation is inactive, the user can still PWM internally. To do this, set DUTY_CTRL to 1b and program the duty cycle value into PROG_DUTY. Please note that in this case, I2C_BC is used to decide if the information about the direction or rotation (Forward/Reverse/Coast/Brake/Sleep) is extracted:

1. Externally, from the EN/IN1 and PH/IN2 pins; I2C_BC=0b), or
2. Internally (from the I2C_EN_IN1 and I2C_PH_IN2 bits; I2C_BC=1b)

Please note that the setting for PMODE does not matter in this case.

As an example, if the settings in 表 7-14 are followed, the device PWMs at 50kHz with approximately 50% duty cycle in the forward direction.

表 7-14. Example settings

Bit	Value
I2C_BC	1b
DUTY_CTRL	1b
PMODE	1b
PWM_FREQ	0b
PROG_DUTY	011111b
I2C_EN_IN1	1b
I2C_PH_IN2	0b

7.3.6.2 Setting Speed/Voltage Regulation Parameters

For obtaining an accurate output from speed and voltage regulation, the following parameters need to be set (for an in-depth explanation, refer to セクション 8).

7.3.6.2.1 Speed and Voltage Set

Denoted by WSET_VSET, this parameter helps set the target speed or voltage, based on the REG_CTRL register setting.

When REG_CTRL is set to 10b, the speed regulation mode is enabled. WSET_VSET is an 8-bit register and can be set to a value between 00h (corresponds to 0 rad/s) and FFh (corresponds to the maximum speed allowable by W_SCALE). The speed control loop matches the value of the SPEED register to the target speed set by WSET_VSET. Please note that the maximum value of the SPEED register is 255.

When REG_CTRL is set to 11b, the motor voltage regulation mode is enabled. VM_GAIN_SEL is used to select the voltage range for a smaller or larger range of voltages.

表 7-15. VM_GAIN_SEL Settings

VM_GAIN_SEL	Voltage range	Corresponding WSET_VSET range	Approximate WSET_VSET Resolution	Formula for WSET_VSET setting
0b	0V - 15.7V	0V: 0 15.7V: 255	61.56mV/bit	WSET_VSET = Target Output Voltage x (255/15.7)
1b	0V - 3.92V	0V: 0 3.92V: 255	15.38mV/bit	WSET_VSET = Target Output Voltage x (255/3.92)

As mentioned in 表 7-15 setting VM_GAIN_SEL to 1b allows the user to increase the resolution for voltage regulation at lower voltages.

When set to 0b, the motor voltage can be set to a value between 0 for 0V and 255 for approximately 15.7V drive output voltage. Please note that the maximum value of WSET_VSET is 255. Each bit corresponds to approximately a 61.56mV resolution of the output voltage setting. Setting WSET_VSET to 255 sets the target voltage to 15.7V. The formula to calculate the decimal value is represented by the equation:

$$\text{Register Setting Value} = \text{Desired Target Voltage} \times \left(\frac{255}{15.7}\right) \quad (4)$$

For example, if desired target voltage is 5V, Register Setting Value = 5*(255/15.7) = 81. Hence, setting a value of 81 (or 51h) outputs approximately 5V.

注

1. In practice, the driver's Over Voltage Protection shuts the device down before 15.7V.
2. The maximum voltage for VM under セクション 6.3 is 11V.
   a. Recommended to set the target voltage below 11V for better accuracy.
3. To set the target voltage to 11V, set WSET_VSET to 179.

7.3.6.2.2 Speed Scaling Factor

Denoted by W_SCALE, this is a scaling factor which helps in setting the target ripple speed when speed regulation mode is enabled. Settings for W_SCALE are shown below. This register also sets the maximum value of ripple speed under each setting of W_SCALE.

表 7-16. Settings for W_SCALE

Bit	W_SCALE	Maximum Ripple Speed
00b	16	4080 rad/s
01b	32	8160 rad/s
10b	64	16320 rad/s
11b	128	32640 rad/s

Example setting for W_SCALE: If SPEED register = 15, W_SCALE = 01b, then the actual ripple speed = 15*32=480 rad/s.

注

Explanation for Maximum Ripple Speed: W_SCALE inadvertently sets the upper limit for the target ripple speed under that setting of W_SCALE. For example, if W_SCALE = 00b, then the maximum ripple speed under this setting = 255*16 rad/s = 4080 rad/s. Hence, the maximum target speed achievable under this setting is 4080 rad/s. Furthermore, under this setting of W_SCALE, FFh corresponds to 4080 rad/s for WSET_VSET when speed regulation mode is activated (REG_CTRL=10b).

7.3.6.2.2.1 Target Speed Setting Example

To set a target speed in rpm, you need to know the following information:

- Gear ratio of the system, GR
- Number of current ripples per motor revolution, N_R. This can be found by taking the lowest common multiple, LCM, of the number of brushes (N_B) and the number of commutator segments (N_C). LCM can easily be calculated using an online calculator.
- Choose an appropriate W_SCALE value.

As an example, if desired target speed is 10000rpm, WSET_VSET value can be calculated using the following equation :

$$\text{WSET\_VSET} = \frac{\text{rpm}}{\text{W\_SCALE}} \times \frac{2\pi}{60} \times N_R \times \text{Gear Ratio} \tag{5}$$

Assuming:

- N_R=6
- W_SCALE = 00b (16 rad/s)
- Gear ratio = 50:1

$$\text{WSET\_VSET} = \frac{10000\text{rpm}}{16} \times \frac{2\pi}{60} \times 6 \times \frac{1}{50} = 7.86 \tag{6}$$

Thus, set WSET_VSET to 0x08.

7.3.6.2.3 Motor Resistance Inverse

Denoted by INV_R, this is the equivalent of the conductance (inverse of resistance) of the motor scaled by a scaling factor, INV_R_SCALE. Scaling allows a wide range of motor resistance values to be accepted using the combination of INV_R and INV_R_SCALE.

7.3.6.2.4 Motor Resistance Inverse Scale

Denoted by INV_R_SCALE, this is the scaling factor for the inverse of motor resistance (INV_R). Since the inverse of a motor resistance is generally not an integer, the value must be rounded off to the nearest integer. Settings are described in 表 7-17.

表 7-17. Settings for INV_R_SCALE

Bit	Value of INV_R_SCALE
00b	2
01b	64
10b	1024
11b	8192

INV_R is represented by the equation:

$$\text{INV\_R} = \frac{1}{\text{Motor Resistance}} \times \text{INV\_R\_SCALE} \tag{7}$$

Please note that the maximum value of INV_R is 255. Please refer to セクション 9.2.3.1.1 for an example on how to select the appropriate INV_R_SCALE for a given value of motor resistance.

7.3.6.2.5 KMC Scaling Factor

Denoted by KMC_SCALE, this is a scaling factor for the parameter KMC. KMC is represented by the following equation:

$$\text{KMC} = \frac{K_V}{N_R} \times \text{KMC\_SCALE} \tag{8}$$

Where, K_V is the motor back emf constant and N_R is the number of ripples per revolution. N_R is calculated by taking the LCM (Least Common Multiple) of the number of brushes, N_B, and the number of commutators, N_C:

$$N_R = LCM(N_B, N_C) \quad (9)$$

Please note that LCM can be easily calculated by using any online LCM calculator.

Tuning KMC appropriately is critical for the speed and voltage regulation algorithm to perform accurately. Scaling is done because the value of motor back emf constant is generally small. Scaling allows integer values to be written on to registers.

表 7-18. Settings for KMC_SCALE

Bit	Value of KMC_SCALE
00b	24 x 2^8
01b	24 x 2^9
10b	24 x 2^{12}
11b	24 x 2^{13}

7.3.6.2.6 KMC

This register is a motor constant representing a proportional value of the motor back emf constant. See KMC Tuning for a detailed tuning procedure.

7.3.6.2.7 VSNS_SEL

This parameter is used to select the motor voltage output filtering method (analog or digital) during PWM. The analog filter (0b) filters out the noise based on the voltage difference between the output pins. The digital filter (1b) multiplies the PWM duty cycle with VM to render an average output voltage. Settings are shown in 表 7-19. When analog filter is selected, the cut-off frequency can be selected using the OUT_FLT register. Recommended setting is the analog filter (0b).

表 7-19. Settings for VSNS_SEL

Bit	Description
0b	Analog Output Filter
1b	Digital Output Filter

7.3.6.3 Soft-Start and Soft-Stop

The DRV8215 integrates a soft-start and stop feature to safeguard the device from high inrush currents during start up. This feature can be activated by setting the EN_SS bit to 1b when the REG_CTRL register is set to 10b (Speed Regulation) or 11b (Voltage Regulation). If speed or voltage regulation modes are inactive, the EN_SS bit has no influence on the device performance.

Soft-start comes into effect during motor start up. The motor current is slowly ramped up to the current value corresponding to the target speed over the duration of t_{INRUSH} time. The inrush time t_{INRUSH} can be set by the user via the 16-bit TINRUSH register. During this time t_{INRUSH}, the FETs are internally PWMed with a duty cycle generated using the PI control loop.

Soft-stop results in a slow ramp down of motor current in time t_{INRUSH}. This can be triggered by the following methods:

1. The direction of rotation is changed on-the-fly. The soft stop function prevents a high current build-up through the motor windings by ramping down the current slowly and performing soft-start on the other direction.
2. Setting I2C_EN_IN1 and I2C_PH_IN2 to 0. Please note that this method sets outputs to Hi-Z after triggering soft stop, which deviates from conventional device operation where setting inputs to 0 causes the device to immediately go Hi-Z and enter coast mode.

3. Set WSET_VSET to 0x00.

A reference block diagram containing the PI loop can be found in セクション 7.3.6. 図 7-13 shows the motor current slow ramp up at start up and ramp down at motor stop within time t_{INRUSH}.

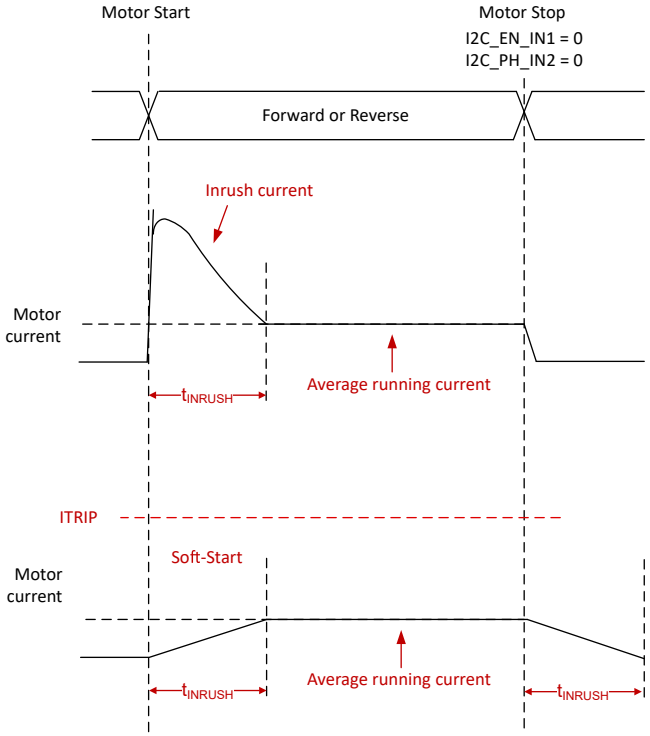


図 7-13. Soft Start and Soft Stop

7.3.6.3.1 T_{INRUSH}

The inrush time, t_{INRUSH}, is set using the 16-bit TINRUSH register. As described earlier, t_{INRUSH} has a dual purpose:

1. t_{INRUSH} is duration of time for which the stall detection scheme ignores the motor inrush current. This prevents false detection of stall during start up. Stall detection is blanked for this duration of time. A detailed description can be found in the Stall Detection section.
2. Additionally, t_{INRUSH} is also the duration of time for which the soft-start and stop feature ramps up the speed or voltage from 0 to a value set by WSET_VSET, or ramps down the speed or voltage from the existing value to 0.
   a. When EN_SS is set to 0b, the TINRUSH register bit settings directly reflect the t_{INRUSH} time. Time t_{INRUSH} can be set to a value between 5 ms (0000h) and 6.7 s (FFFFh). Default value is 1 s.
   b. When EN_SS is set to 1b during motor speed or voltage regulation mode, the target motor speed or voltage is soft-started and stopped over the duration of t_{INRUSH} as describe above. In this case, t_{INRUSH} = TINRUSH x WSET_VSET. As an example, if WSET_VSET = 10 and intended t_{INRUSH} time is 1 s, then TINRUSH is to be set to 100 ms.

7.3.7 Protection Circuits

The DRV8215 is fully protected against supply undervoltage, overcurrent, and overtemperature events. In addition, the device supports overvoltage protection in sleep mode and when the H-bridge is disabled.

7.3.7.1 Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by limiting the gate drive internally. If this analog current limit persists for longer than the OCP deglitch time (t_{OCP}), all FETs in the H-bridge will disable, FAULT and OCP bits become 1b and nFAULT is pulled low.

The OCP_MODE bit programs the response of the device to overcurrent event. The device can either latch-off or perform automatic retry to recover from an overcurrent event.

In automatic retry mode, the MOSFETs will be disabled and the nFAULT pin driven low for a duration of t_{RETRY}. After t_{RETRY}, the MOSFETs are re-enabled according to the control inputs. If the overcurrent condition is still present, the cycle repeats; otherwise normal device operation resumes. This is explained by the following diagram -

In latch-off mode, the MOSFETs will remain disabled and the nFAULT pin will be driven low until the device is reset by a CLR_FLT command or by cycling the VM power supply.

Overcurrent conditions are detected independently on both high- and low-side FETs. This means that a short to ground, supply, or across the motor winding will all result in an overcurrent shutdown. Overcurrent protection does not use the current sense circuitry used for current regulation, so it functions regardless of VREF and IPROPI settings.

7.3.7.2 Thermal Shutdown (TSD)

If the die temperature exceeds the thermal shutdown temperature threshold (T_{TSD}), all FETs in the H-bridge are disabled, TSD and FAULT bits become 1b, and nFAULT is pulled low. The TSD_MODE bit programs the response of the device to overtemperature event. The device can either latch-off or perform automatic retry to recover from overtemperature.

In automatic retry mode, normal operation will resume (driver operation starts, nFAULT is released and FAULT bit changes to 0b) when the junction temperature falls below the overtemperature threshold limit minus the hysteresis ($T_{TSD} – T_{HYS}$). The TSD bit remains at 1b indicating that a thermal shutdown event occurred until a CLR_FLT command is issued.

In latch-off mode, once the overtemperature condition is removed, normal operation resumes after sending a CLR_FLT command, or a power cycling.

7.3.7.3 VCC Undervoltage Lockout (UVLO)

Whenever the VCC supply voltage falls below the UVLO falling threshold voltage, V_{UVLO}, all circuitry in the device is disabled, the output FETs are disabled, all internal logic is reset and nFAULT is pulled low.

The device allows the VM supply to dip all the way to 0 V. Normal operation resumes when the VCC voltage rises above the V_{UVLO} rising threshold as shown in 図 7-14. 表 7-20 summarizes the conditions when the device enters UVLO.

- The NPOR bit is reset and latched low once VCC goes above the UVLO threshold.
- NPOR remains in reset condition until cleared through the CLR_FLT bit.
- After power up, NPOR is automatically latched high once the CLR_FLT command is issued.

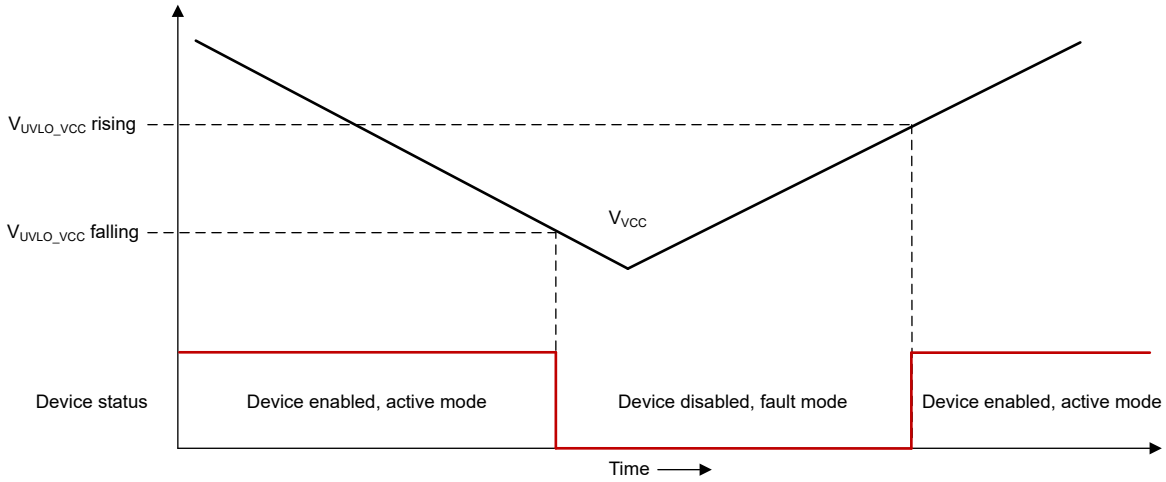


図 7-14. UVLO Operation

表 7-20. UVLO response conditions

V_{VM}	V_{VCC}	Device Response	IPROPI
0 V to V_{VM_MAX}	<1.65 V	UVLO	Not available
0 V to V_{VM_MAX}	>1.65 V	Normal Operation	Available for V_{VM} > 1.65 V

7.3.7.4 Overvoltage Protection (OVP)

When the motor is driven by external force, it acts as a generator and pumps back current to the supply voltage rail. This can potentially damage other circuits connected to the supply rail. In low-power sleep mode or when the H-bridge is disabled (High-Z), if the voltage of the output nodes rise above the supply voltage by about 200 mV, the DRV8215 turns on the two low-side MOSFETs. This allows the device to actively brake a motor connected to the outputs by shorting the back emf across the motor terminals.

The overvoltage protection (OVP) function is enabled by default. After power-up, the EN_OVP bit can be made 0b to disable this feature. The EN_OVP logic state is latched, so that in sleep mode the device bahves as per the EN_OVP bit setting, even though the internal digital logic is reset.

In sleep mode, if there is a short circuit to power supply fault present in the power stage, a simple overcurrent detector circuit is provided to disable the low-side MOSFET if a high current event is detected while braking. This is needed since the normal overcurrent protection circuits are disabled during the low-power sleep mode.

7.3.7.5 nFAULT Output

The nFAULT pin has an open-drain output and should be pulled up to a 5-V, 3.3-V or 1.8-V supply. nFAULT pin will be high after power-up. When a fault is detected, the nFAULT pin will be logic low.

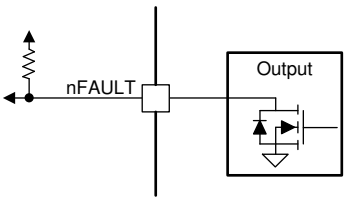


図 7-15. nFAULT Pin

7.4 Device Functional Modes

The following table summarizes the DRV8215 functional modes described in this section.

表 7-21. Modes of Operation

MODE	CONDITION	H-BRIDGE	INTERNAL CIRCUITS
Active Mode	nSLEEP = 1, EN_OUT = 1b	Operating	Operating
Low-Power Sleep Mode	nSLEEP = 0	Disabled	Disabled
Fault Mode	Any fault condition met	Disabled	See Fault Mode section

7.4.1 Active Mode

After the supply voltage on the VCC pin has crossed the rising undervoltage threshold V_{UVLO}, if nSLEEP is logic high and t_{WAKE} has elapsed, and if the EN_OUT bit is 1b, the device enters active mode. In this mode, the full-bridge, and internal logic are active and the device is ready to receive inputs.

When $V_{VCC} < V_{VM}$, the DRV8215 draws active current from the VM pin rather than the VCC pin (I_{VM}). During this operating condition, I_{VCC} is typically less than 500 nA. When $V_{VCC} > V_{VM}$, the device draws active current from the VCC pin, and the VM pin will only draw current required by the load. When $V_{VCC} = V_{VM}$, the active current may be drawn from either supply pin. The active current is typically less than 2 mA.

7.4.2 Low-Power Sleep Mode

When the nSLEEP pin is low for $t_{TURNOFF}$ time, the DRV8215 enters a low-power sleep mode. In sleep mode, the outputs remain High-Z and the device draws minimal current from the supply pin (I_{VMQ} or I_{VCCQ}). After nSLEEP is set high for longer than the duration of t_{WAKE}, the device becomes fully operational.

7.4.3 Fault Mode

The DRV8215 enters fault mode when it encounters a fault condition. This protects the device and the load on the outputs. 表 7-22 describes the device behavior in the fault mode which depends on the fault condition. The device will leave the fault mode and re-enter the active mode when the system meets the recovery condition.

表 7-22. Fault Conditions Summary

FAULT	FAULT CONDITION	CONFIGURATION	ERROR REPORT	FULL-BRIDGE	INTERNAL CIRCUITS	RECOVERY CONDITION
VCC undervoltage (UVLO)	$V_{VCC} < V_{UVLO\_VCC}$	–	nFAULT / I²C	Disabled	Disabled	$V_{VCC} > V_{UVLO\_VCC}$
Overcurrent (OCP)	$I_{OUT} > I_{OCP}$	OCP_MODE = 0b	nFAULT / I²C	Disabled	Operating	Latched: CLR_FLT
		OCP_MODE = 1b	nFAULT / I²C	Disabled	Operating	Automatic retry: t_{RETRY}
Thermal Shutdown (TSD)	$T_J > T_{TSD}$	TSD_MODE = 0b	nFAULT / I²C	Disabled	Operating	Latched: CLR_FLT
		TSD_MODE = 1b	nFAULT / I²C	Disabled	Operating	Automatic: $T_J < T_{TSD} - T_{HYS}$
Overvoltage protection (OVP)	OUTx = Hi-Z or nSLEEP = 0; $V_{VOUT} - V_{VM} > V_{SD}$	–	I²C when OUTx = Hi-Z	Disabled	Disabled	Automatic: $V_{VOUT} - V_{VM} < V_{SD}$

7.5 Programming

7.5.1 I²C Communication

The I²C interface allows control and monitoring of the DRV8215 by a microcontroller. The I²C bus consists of a data line (SDA) and a clock line (SCL) with off-chip pull-up resistors. When the bus is idle, both SDA and SCL lines are pulled high.

A leader device, usually a microcontroller or a digital signal processor, controls the bus. The leader is responsible for generating the SCL signal and device addresses. The leader also generates specific conditions that indicate the START and STOP of data transfer. A follower device receives and/or transmits data on the bus under control of the leader device. DRV8215 is a follower device.

The lower four bits of the device address are derived from the inputs from the pins A1 and A0, which can be tied to VCC (logic high), GND (logic low), or left open. These four address bits are latched into the device at power up, so cannot be changed dynamically. The upper address bits of the device address are fixed at 0x60h, so the device address is as follows -

表 7-23. Device Addresses

A1 Pin	A0 Pin	A3A2A1A0 bits	ADDRESS (WRITE)	ADDRESS (READ)
0	0	0000b	0x60h	0x61h
0	High-Z	0001b	0x62h	0x63h
0	1	0010b	0x64h	0x65h
High-Z	0	0011b	0x66h	0x67h
High-Z	High-Z	0100b	0x68h	0x69h
High-Z	1	0101b	0x6Ah	0x6Bh
1	0	0110b	0x6Ch	0x6Dh
1	High-Z	0111b	0x6Eh	0x6Fh
1	1	1000b	0x70h	0x71h

Using the A0 and A1 pins, up to 9 DRV8215 follower devices can be controlled by one I^2C bus. The DRV8215 does not respond to the general call address. It is recommended to use a 2.2kΩ pull-up resistor for these pins.

7.5.1.1 I^2C Write

To write on the I^2C bus, the leader device sends a START condition on the bus with the address of the 7-bit follower device. Also, the last bit (the R/W bit) is set to 0b, which signifies a write. After the follower sends the acknowledge bit, the leader device then sends the register address of the register to be written. The follower device sends an acknowledge (ACK) signal again which notifies the leader device that the follower device is ready. After this process, the leader device sends 8-bit write data and terminates the transmission with a STOP condition.

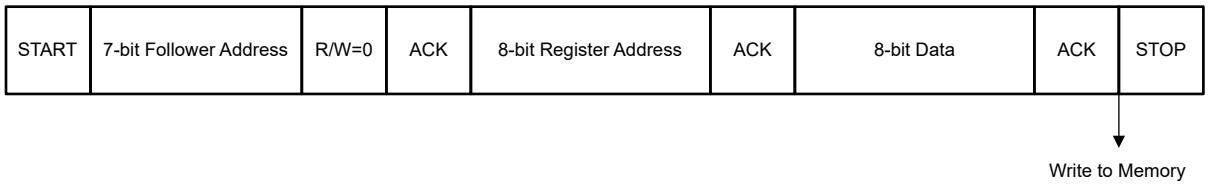


図 7-16. I^2C Write Sequence

7.5.1.2 I^2C Read

To read from a follower device, the leader device must first communicate to the follower device which register will be read from. This communication is done by the leader starting the transmission similarly to the write process which is by setting the address with the R/W bit equal to 0b (signifying a write). The leader device then sends the register address of the register to be read from. When the follower device acknowledges this register address, the leader device sends a START condition again, followed by the follower address with the R/W bit set to 1b (signifying a read). After this process, the follower device acknowledges the read request and the leader device releases the SDA bus, but continues supplying the clock to the follower device.

During this part of the transaction, the leader device becomes the leader-receiver, and the follower device becomes the follower-transmitter. The leader device continues sending out the clock pulses, but releases the SDA line so that the follower device can transmit data. At the end of the byte, the leader device sends a negative-acknowledge (NACK) signal, signaling to the follower device to stop communications and release the bus. The leader device then sends a STOP condition.

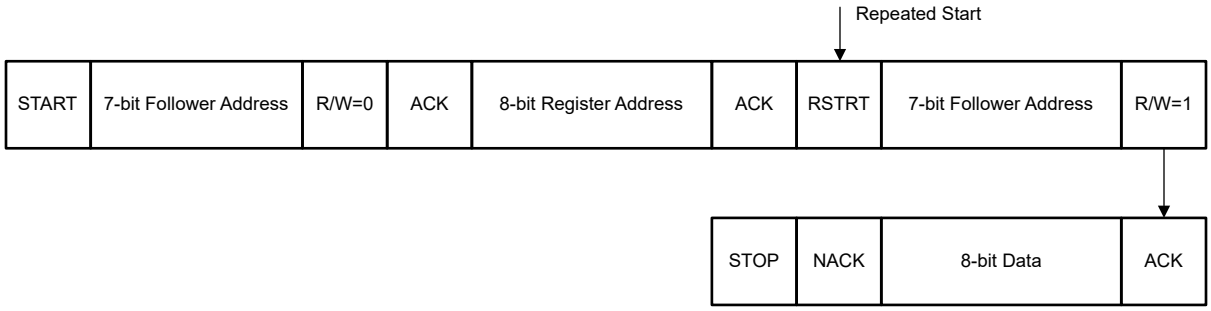


図 7-17. I²C Read Sequence

8 Register Map

The following table lists the memory-mapped I²C registers for the DRV8215. The I²C registers are used to configure the DRV8215 and for device diagnostics.

注

Do not modify reserved registers or addresses not listed in the register map (表 8-1). Writing to these registers can have unintended effects. For all reserved bits, the default value is 0b.

表 8-1. I²C Registers

Address	Name	7	6	5	4	3	2	1	0	Access
0x00	FAULT_STATUS	FAULT	RSVD	STALL	OCP	OVP	TSD	NPOR	RSVD	R
0x01	RC_STATUS1	SPEED[7:0]								R
0x02	RC_STATUS2	RSVD								
0x03	RC_STATUS3	RSVD								
0x04	REG_STATUS1	VMTR[7:0]								R
0x05	REG_STATUS2	IMTR[7:0]								R
0x06	REG_STATUS3	RSVD		DUTY_READ[5:0]						R
0x07	REG_STATUS4	RSVD								
0x08	REG_STATUS5	RSVD								
0x09	CONFIG0	EN_OUT	EN_OVP	EN_STALL	VSNS_SEL*	VM_GAIN_SEL*	RSVD	CLR_FLT	DUTY_CTRL*	RW
0x0A	CONFIG1	TINRUSH_LSB[7:0]								RW
0x0B	CONFIG2	TINRUSH_MSB[15:8]								RW
0x0C	CONFIG3	IMODE[1:0]*		SMODE*	INT_VREF*	TBLANK*	TDEG*	OCP_MODE*	TSD_MODE*	RW
0x0D	CONFIG4	RSVD		STALL_REP	CBC_REP	PMODE*	I2C_BC*	I2C_EN_IN1	I2C_PH_IN2	RW
0x0E	REG_CTRL0	RSVD		EN_SS	REG_CTRL[1:0]*		PWM_FREQ*	W_SCALE[1:0]		RW
0x0F	REG_CTRL1	WSET_VSET[7:0]								RW
0x10	REG_CTRL2	OUT_FLT[1:0]		PROG_DUTY[5:0]						RW
0x11	RC_CTRL0	RSVD					CS_GAIN_SEL[2:0]			RW
0x12	RC_CTRL1	RSVD								
0x13	RC_CTRL2	INV_R_SCALE[1:0]		KMC_SCALE[1:0]		RSVD				RW
0x14	RC_CTRL3	INV_R[7:0]								RW
0x15	RC_CTRL4	KMC[7:0]								RW
0x16	RC_CTRL5	RSVD								
0x17	RC_CTRL6	RSVD								
0x18	RC_CTRL7	KP_DIV[2:0]			KP_MUL[4:0]					RW
0x19	RC_CTRL8	KI_DIV[2:0]			KI_MUL[4:0]					RW

注

*Writable only when EN_OUT=0.

表 8-2. Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.1 DRV8215_STATUS Registers

表 8-3 lists the memory-mapped registers for the DRV8215_STATUS registers. All register offset addresses not listed in 表 8-3 should be considered as reserved locations and the register contents should not be modified.

表 8-3. DRV8215_STATUS Registers

Offset	Acronym	Register Name	Section
0h	FAULT_STATUS	Various fault registers' status.	セクション 8.1.1
1h	RC_STATUS1	Status Registers - 1.	セクション 8.1.2
2h	RC_STATUS2	Status Registers - 2.	セクション 8.1.3
3h	RC_STATUS3	Status Registers - 3.	セクション 8.1.4
4h	REG_STATUS1	Regulation Status Registers - (1/5).	セクション 8.1.5
5h	REG_STATUS2	Regulation Status Registers - (2/5).	セクション 8.1.6
6h	REG_STATUS3	Regulation Status Registers - (3/5).	セクション 8.1.7
7h	REG_STATUS4	Regulation Status Registers - (4/5).	セクション 8.1.8
8h	REG_STATUS5	Regulation Status Registers - (5/5).	セクション 8.1.9

Complex bit access types are encoded to fit into small table cells. 表 8-4 shows the codes that are used for access types in this section.

表 8-4. DRV8215_STATUS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
-n		Value after reset or the default value

8.1.1 FAULT_STATUS Register (Offset = 0h) [Reset = 00h]

FAULT_STATUS is shown in 表 8-5.

Return to the Summary Table.

Status of various fault and protection bits.

表 8-5. FAULT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FAULT	R	0h	0b during normal operation, 1b during a fault condition. nFAULT pin is pulled down when FAULT bit is 1b. nFAULT pin is released during normal operation.
6	RESERVED	R	0h	
5	STALL	R	0h	When this bit is 1b, it indicates motor stall.
4	OCP	R	0h	0b during normal operation, 1b if OCP event occurs.
3	OVP	R	0h	0b during normal operation, 1b if OVP event occurs.
2	TSD	R	0h	0b during normal operation, 1b if TSD event occurs.
1	NPOR	R	0h	Reset and latched low if VCC>VUVLO. Remains reset until the CLR_FLT bit is set to issue a clear fault command. After power up, automatically latched high once CLR_FLT command is issued. Refer to セクション 7.3.7.3 for further explanation.
0	RSVD	R	0h	Reserved.

8.1.2 RC_STATUS1 Register (Offset = 1h) [Reset = 00h]

RC_STATUS1 is shown in 表 8-6.

Return to the Summary Table.

Estimated speed of motor ripples.

表 8-6. RC_STATUS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SPEED	R	0h	Outputs the motor current ripple speed estimated by an internal algorithm.

8.1.3 RC_STATUS2 Register (Offset = 2h) [Reset = 00h]

RC_STATUS2 is shown in 表 8-7.

Return to the Summary Table.

Reserved.

表 8-7. RC_STATUS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RSVD	R	0h	Reserved.

8.1.4 RC_STATUS3 Register (Offset = 3h) [Reset = 00h]

RC_STATUS3 is shown in 表 8-8.

Return to the Summary Table.

Reserved.

表 8-8. RC_STATUS3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RSVD	R	0h	Reserved.

8.1.5 REG_STATUS1 Register (Offset = 4h) [Reset = 00h]

REG_STATUS1 is shown in 表 8-9.

Return to the Summary Table.

Value corresponding to the output voltage across the motor terminals.

表 8-9. REG_STATUS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	VMTR	R	0h	Outputs the voltage across the motor terminals, maximum value FFh. 00h corresponds to 0 V and B0h corresponds to 11 V.

8.1.6 REG_STATUS2 Register (Offset = 5h) [Reset = 00h]

REG_STATUS2 is shown in 表 8-10.

Return to the Summary Table.

Output corresponding to current flowing through the motor.

表 8-10. REG_STATUS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	IMTR	R	0h	Outputs the current flowing through the motor. 00h corresponds to 0 A and C0h corresponds to the maximum value set by the CS_GAIN_SEL bits.

8.1.7 REG_STATUS3 Register (Offset = 6h) [Reset = 00h]

REG_STATUS3 is shown in 表 8-11.

Return to the Summary Table.

Internal pwm duty cycle.

表 8-11. REG_STATUS3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RSVD	R	0h	Reserved.
5-0	DUTY_READ	R	0h	Represents the bridge control duty cycle generated by an internal regulation logic. This register is applicable when speed or voltage regulation is activated. The range of duty cycle is 0% (000000b) to 100% (111111b). Refer to セクション 7.3.6 for further explanation on the internal PWM generation scheme.

8.1.8 REG_STATUS4 Register (Offset = 7h) [Reset = 00h]

REG_STATUS4 is shown in 表 8-12.

Return to the Summary Table.

Reserved.

表 8-12. REG_STATUS4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RSVD	R	0h	Reserved.

8.1.9 REG_STATUS5 Register (Offset = 8h) [Reset = 00h]

REG_STATUS5 is shown in 表 8-13.

Return to the Summary Table.

Reserved.

表 8-13. REG_STATUS5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RSVD	R	0h	Reserved.

8.2 DRV8215_CONFIG Registers

表 8-14 lists the memory-mapped registers for the DRV8215_CONFIG registers. All register offset addresses not listed in 表 8-14 should be considered as reserved locations and the register contents should not be modified.

表 8-14. DRV8215_CONFIG Registers

Offset	Acronym	Register Name	Section
9h	CONFIG0	Configuration Registers - Faults (1/5).	セクション 8.2.1
Ah	CONFIG1	Configuration Registers - (2/5).	セクション 8.2.2
Bh	CONFIG2	Configuration Registers - (3/5).	セクション 8.2.3
Ch	CONFIG3	Configuration Registers - (4/5).	セクション 8.2.4
Dh	CONFIG4	Configuration Registers - (5/5).	セクション 8.2.5

Complex bit access types are encoded to fit into small table cells. 表 8-15 shows the codes that are used for access types in this section.

表 8-15. DRV8215_CONFIG Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.2.1 CONFIG0 Register (Offset = 9h) [Reset = 60h]

CONFIG0 is shown in 表 8-16.

Return to the Summary Table.

Enable/Disable various faults.

表 8-16. CONFIG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	EN_OUT	R/W	0h	0b: All driver FETs are Hi-Z. 1b: Enables the driver outputs.
6	EN_OVP	R/W	1h	Enables the OVP feature. 1b by default, can be made 0b after power-up to disable the OVP feature. Refer to セクション 7.3.7.1 for further explanation.
5	EN_STALL	R/W	1h	Enables the Stall Detection feature. Stall detection feature can be disabled by setting this bit to 0b. Refer to EN_STALL configuration under セクション 7.3.5 for further explanation.
4	VSNS_SEL	R/W	0h	0b: Use the analog low-pass filter to average out the output voltage for voltage regulation. Refer to OUT_FLT for further description of the analog low-pass filter. 0b is the recommended value. 1b: Use the digital low-pass filter for voltage regulation. This option perfroms multiplication of the duty cycle with VM to obtain the output voltage.
3	VM_GAIN_SEL	R/W	0h	Selects the voltage range for better resolution during voltage regulation for smaller voltages. 0b: Voltage range is 0V - 16V. 1b: Voltage range is 0V - 4V. Refer to セクション 7.3.6.2.1 for further explanation.
2	RSVD	R/W	0h	Reserved.
1	CLR_FLT	R/W	0h	Clears all latched faults when set to 1b. CLR_FLT is automatically reset.
0	DUTY_CTRL	R/W	0h	0b: User cannot program duty cycle manually. 1b: When speed regulation is disabled and the DUTY_CTRL bit is 1b, user can write desired PWM duty to PROG_DUTY bits. The range of duty is 0% (000000b) to 100% (111111b).

8.2.2 CONFIG1 Register (Offset = Ah) [Reset = 00h]

CONFIG1 is shown in 表 8-17.

Return to the Summary Table.

Configure the inrush time (1/2).

表 8-17. CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TINRUSH_LSB	R/W	0h	Lower half 8-bit output out of the total 16-bit output for inrush time blanking for stall detection. Sets the amount of time for which the stall detection scheme ignores motor inrush current. Refer to セクション 7.3.6.3.1 for further explanation.

8.2.3 CONFIG2 Register (Offset = Bh) [Reset = 00h]

CONFIG2 is shown in 表 8-18.

Return to the Summary Table.

Configure the inrush time (2/2).

表 8-18. CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TINRUSH_MSB	R/W	0h	Upper half 8-bit output out of the total 16-bit output for inrush time blanking for stall detection. Sets the amount of time for which the stall detection scheme ignores motor inrush current. Refer to セクション 7.3.6.3.1 for further explanation.

8.2.4 CONFIG3 Register (Offset = Ch) [Reset = 63h]

CONFIG3 is shown in 表 8-19.

Return to the Summary Table.

Enable/Disable various device modes like IMODE, SMODE, and blanking time.

表 8-19. CONFIG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	IMODE	R/W	1h	Determines the behavior of current regulation. Refer to IMODE configuration under セクション 7.3.4.2 for further explanation.
5	SMODE	R/W	1h	Programs device response to a stall condition. Refer to SMODE configuration under セクション 7.3.5 for further explanation.
4	INT_VREF	R/W	0h	If set to 1b, sets VREF voltage to 500mV internally. Voltage is not fixed if INT_VREF is set to 0b. Refer to セクション 7.3.5 for further explanation.
3	TBLANK	R/W	0h	Sets the current sense blanking time. If set to 0b, t_{BLANK}=1.8µs. If set to 1b, t_{BLANK}=1.0µs.
2	TDEG	R/W	0h	Sets the current regulation and stall detection deglitch time. If set to 0b, t_{DEG}=2µs. If set to 1b, t_{DEG}=1µs.
1	OCP_MODE	R/W	1h	Programs device response to an overcurrent event. If set to 0b, device is latched off in case of an OCP event. Can be cleared using CLR_FLT. If set to 1b, device performs auto-retry after time tretry in case of an OCP event. Refer to セクション 7.3.7.1 for further explanation.
0	TSD_MODE	R/W	1h	Programs device response to an overtemperature event. If set to 0b, device is latched off in case of a TSD event. If set to 1b, device performs auto-retry when T_J<T_{TSD}–T_{HYS}.

8.2.5 CONFIG4 Register (Offset = Dh) [Reset = 38h]

CONFIG4 is shown in 表 8-20.

Return to the Summary Table.

Configure the report registers like RC_REP and STALL_REP.

表 8-20. CONFIG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RSVD	R/W	0h	Reserved.
5	STALL_REP	R/W	1h	Determines whether stall is reported on the nFAULT pin. When set to 1b, nFAULT is low whenever stall is detected. When set to 0b, stall is not reported on nFAULT output. Refer to セクション 7.3.5 for further explanation.
4	CBC_REP	R/W	1h	When REG_CTRL is set to 01b, the device enters cycle-by-cycle mode of current regulation. In this mode, the device can indicate whenever the H-bridge enters internal current regulation. CBC_REP bit is used to determine device outputs' behavior in the cycle-by-cycle mode. 1b: nFAULT is pulled low when H-Bridge enters internal current regulation. 0b: nFAULT is not pulled low when H-Bridge enters internal current regulation. Refer to セクション 7.3.4.2.2 for further explanation.
3	PMODE	R/W	1h	Switch between phase/enable mode and PWM mode. 0b: PH/EN. 1b: PWM.
2	I2C_BC	R/W	0h	Decides the H-Bridge Control Interface. 0b: Bridge control configured by INx pins. 1b: Bridge control configured by I2C bits I2C_EN_IN1 and I2C_PH_IN2.
1	I2C_EN_IN1	R/W	0h	Enable/PWM Input Bit 1 for internal bridge control. Used when I2C_BC=1b. Ignored when I2C_BC=0b.
0	I2C_PH_IN2	R/W	0h	Phase/PWM Input Bit 2 for internal bridge control. Used when I2C_BC=1b.Ignored when I2C_BC=0b.

8.3 DRV8215_CTRL Registers

表 8-21 lists the memory-mapped registers for the DRV8215_CTRL registers. All register offset addresses not listed in 表 8-21 should be considered as reserved locations and the register contents should not be modified.

表 8-21. DRV8215_CTRL Registers

Offset	Acronym	Register Name	Section
Eh	REG_CTRL0	Regulation control registers (1/3).	セクション 8.3.1
Fh	REG_CTRL1	Regulation control registers (2/3).	セクション 8.3.2
10h	REG_CTRL2	Regulation control registers (3/3).	セクション 8.3.3
11h	RC_CTRL0	Control Registers - (1/9).	セクション 8.3.4
12h	RC_CTRL1	Control Registers - (2/9).	セクション 8.3.5
13h	RC_CTRL2	Control Registers - (3/9).	セクション 8.3.6
14h	RC_CTRL3	Control Registers - (4/9).	セクション 8.3.7
15h	RC_CTRL4	Control Registers - (5/9).	セクション 8.3.8
16h	RC_CTRL5	Control Registers - (6/9).	セクション 8.3.9
17h	RC_CTRL6	Control Registers - (7/9).	セクション 8.3.10
18h	RC_CTRL7	Control Registers - (8/9).	セクション 8.3.11
19h	RC_CTRL8	Control Registers - (9/9).	セクション 8.3.12

Complex bit access types are encoded to fit into small table cells. 表 8-22 shows the codes that are used for access types in this section.

表 8-22. DRV8215_CTRL Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.3.1 REG_CTRL0 Register (Offset = Eh) [Reset = 27h]

REG_CTRL0 is shown in 表 8-23.

Return to the Summary Table.

Set features like Soft Start/Stop and speed scaling factor.

表 8-23. REG_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RSVD	R/W	0h	Reserved.
5	EN_SS	R/W	1h	Used to enable/disable soft start/stop. 1b: Target motor voltage or speed is soft-started and soft-stopped over the duration of t_{INRUSH} time. 0b: Soft-start/stop feature is disabled. Refer to セクション 7.3.6.3 for further explanation.
4-3	REG_CTRL	R/W	0h	Selects the current regulation scheme (fixed off-time or cycle-by-cycle) or motor speed and voltage regulation. 00b: Fixed Off-Time Current Regulation. 01b: Cycle-By-Cycle Current Regulation. 10b: Motor speed is regulated. 11b: Motor voltage is regulated. Refer to セクション 7.3.4.2 for further explanation.
2	PWM_FREQ	R/W	1h	Sets the PWM frequency when bridge control is configured by INx bits (I2C_BC=1b). 0b: PWM frequency is set to 50kHz. 1b: PWM frequency is set to 25kHz.
1-0	W_SCALE	R/W	3h	Scaling factor that helps in setting the target motor current ripple speed. 00b: 16 01b: 32 10b: 64 11b: 128 Refer to セクション 7.3.6.2.2 for further explanation.

8.3.2 REG_CTRL1 Register (Offset = Fh) [Reset = FFh]

REG_CTRL1 is shown in 表 8-24.

Return to the Summary Table.

Set the target motor voltage and speed for voltage and speed regulation respectively.

表 8-24. REG_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	WSET_VSET	R/W	FFh	Sets the target motor voltage or current ripple speed. A detailed explanation is provided in セクション 7.3.6.2.1.

8.3.3 REG_CTRL2 Register (Offset = 10h) [Reset = 00h]

REG_CTRL2 is shown in 表 8-25.

Return to the Summary Table.

Set the duty cycle and cut-off frequency for output voltage filtering.

表 8-25. REG_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	OUT_FLT	R/W	0h	Programs the cut-off frequency of the output voltage filtering. 00b: 250Hz 01b: 500Hz 10b: 750Hz 11b: 1000Hz For best results, choose a cut-off frequency equal to a value at least 20 times lower than the PWM frequency. Eg, if you PWM at 20kHz, OUT_FLT=11b (1000Hz) is sufficient.
5-0	PROG_DUTY	R/W	0h	When speed/voltage regulation is inactive and DUTY_CTRL is set to 1b, the user can write the desired PWM duty cycle to this register. The range of duty cycle is 0% (000000b) to 100% (111111b).

8.3.4 RC_CTRL0 Register (Offset = 11h) [Reset = 08h]

RC_CTRL0 is shown in 表 8-26.

Return to the Summary Table.

Select the current mirror gain, AIPROPI.

表 8-26. RC_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RSVD	R/W	1h	Reserved.
2-0	CS_GAIN_SEL	R/W	0h	Used to select the current mirror gain, A_{IPROPI}. Settings are as follows: 000b: 4 A 001b: 2 A 010b: 1 A 011b: 0.5 A 1X0b: 0.25 A 1X1b: 0.125 A Refer to セクション 7.3.4.1 for further explanation.

8.3.5 RC_CTRL1 Register (Offset = 12h) [Reset = FFh]

RC_CTRL1 is shown in 表 8-27.

Return to the Summary Table.

Reserved.

表 8-27. RC_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RSVD	R/W	FFh	Reserved.

8.3.6 RC_CTRL2 Register (Offset = 13h) [Reset = 73h]

RC_CTRL2 is shown in 表 8-28.

Return to the Summary Table.

Set values of various scaling parameters.

表 8-28. RC_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	INV_R_SCALE	R/W	1h	Scaling factor for the INV_R parameter. 00b: INV_R_SCALE = 2 01b: INV_R_SCALE = 64 10b: INV_R_SCALE = 1024 11b: INV_R_SCALE = 8192 Refer to セクション 7.3.6.2.4 for further explanation.
5-4	KMC_SCALE	R/W	3h	Scaling factor for KMC parameter. 00b: KMC_SCALE = 24 x 2^{8} 01b: KMC_SCALE = 24 x 2^{9} 10b: KMC_SCALE = 24 x 2^{12} 11b: KMC_SCALE = 24 x 2^{13} Refer to セクション 7.3.6.2.5 for further explanation.
3-0	RSVD	R/W	3h	Reserved.

8.3.7 RC_CTRL3 Register (Offset = 14h) [Reset = 00h]

RC_CTRL3 is shown in 表 8-29.

Return to the Summary Table.

Set the INV_R parameter.

表 8-29. RC_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	INV_R	R/W	0h	User input based on motor coil resistance. INV_R = INV_R_SCALE / Motor Resistance. Must not be set to 0. Refer to セクション 7.3.6.2.3 for further explanation.

8.3.8 RC_CTRL4 Register (Offset = 15h) [Reset = 00h]

RC_CTRL4 is shown in 表 8-30.

Return to the Summary Table.

Set the KMC parameter.

表 8-30. RC_CTRL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	KMC	R/W	0h	Represents a proportional value of the motor back emf constant. KMC = (K_V) / N_R)*KMC_SCALE. Refer to セクション 7.3.6.2.6 for further explanation.

8.3.9 RC_CTRL5 Register (Offset = 16h) [Reset = 00h]

RC_CTRL5 is shown in 表 8-31.

Return to the Summary Table.

Reserved.

表 8-31. RC_CTRL5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RSVD	R/W	0h	Reserved.

8.3.10 RC_CTRL6 Register (Offset = 17h) [Reset = 00h]

RC_CTRL6 is shown in 表 8-32.

Return to the Summary Table.

Reserved.

表 8-32. RC_CTRL6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RSVD	R/W	0h	Reserved.

8.3.11 RC_CTRL7 Register (Offset = 18h) [Reset = 21h]

RC_CTRL7 is shown in 表 8-33.

Return to the Summary Table.

Set the proportional constant in PI control loop.

表 8-33. RC_CTRL7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	KP_DIV	R/W	1h	Used to select a division value for calculating the actual proportional constant for the PI control loop. Actual proportional constant, K_P = KP_MULT/KP_DIV. Settings are as follows: 000b: 32 001b: 64 010b: 128 011b: 256 100b: 512 101b: 16 110b: 1
4-0	KP_MULT	R/W	1h	Represents the PI loop KP constant. This is not the actual proportional constant that is fed into the gain block of the PI control loop. Rather, the actual proportional constant can be calculated using the value of this register. Actual Proportional Constant, K_P = KP_MULT/KP_DIV. For example, if actual proportional constant is 0.0625, then KP_MULT can be set to 1 (00001b), and KP_DIV can be set to 16 (corresponds to 101b), hence, Actual proportional constant = 1/16 = 0.0625.

8.3.12 RC_CTRL8 Register (Offset = 19h) [Reset = 21h]

RC_CTRL8 is shown in 表 8-34.

Return to the Summary Table.

Set the integral constant in PI control loop.

表 8-34. RC_CTRL8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	KI_DIV	R/W	1h	Used to select a division value for calculating the actual integral constant for the PI control loop. Actual integral constant, $_{I}$ = KI_MULT/KI_DIV. Settings are as follows: 000b: 32 001b: 64 010b: 128 011b: 256 100b: 512 101b: 16 110b: 1
4-0	KI_MULT	R/W	1h	Represents the PI loop KI constant. This is not the actual integral constant that is fed into the gain block of the PI control loop. Rather, the actual integral constant can be calculated using the value of this register. Actual Integral Constant, K_I = KI_MULT/KI_DIV. For example, if actual integral constant is 0.90625, then KI_MULT can be set to 29 (11101b), and KI_DIV can be set to 32 (corresponds to 000b), hence, Actual integral constant = 29/32 = 0.90625.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DRV8215 is intended to drive one brushed DC motor.

9.2 Typical Application: Brushed DC Motor

A typical application for the DRV8215 is to drive a brushed DC motor using the full-bridge outputs. 図 9-1 shows a schematic example. The resistor on the IPROPI pin can provide a voltage signal to the microcontroller analog-to-digital converter (ADC).

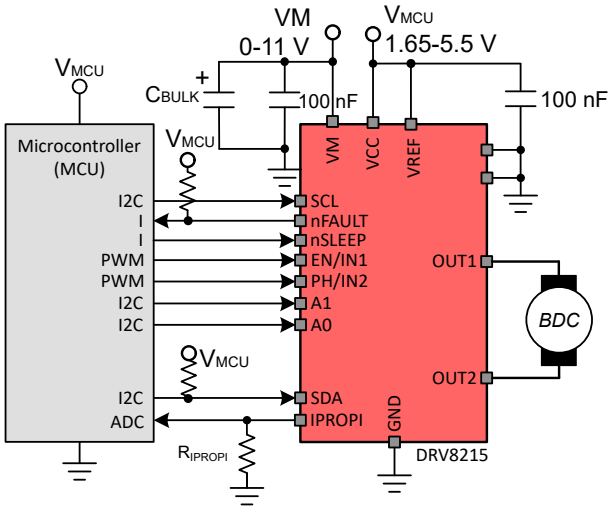


図 9-1. Typical Connections with stall detection disabled

9.2.1 Design Requirements

表 9-1 lists example design parameters.

表 9-1. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Motor voltage	V_{VM}	8 V
Average motor current	I_{AVG}	0.8 A
Motor inrush (startup) current	I_{INRUSH}	2. A
Motor stall current	I_{STALL}	2.1 A
Motor current trip point	I_{TRIP}	1.9 A
VREF voltage	VREF	3.3 V
IPROPI resistance	R_{IPROPI}	8.45 kΩ
PWM frequency	f_{PWM}	20 kHz
Bulk Capacitance	C_{BULK}	50µF

9.2.2 Stall Detection

Some applications require stall detection to notify the microcontroller of a locked-rotor/stall condition. A stall could be caused by one of two things: unintended mechanical blockage or the load reaching an end-stop in a constrained travel path. The DRV8215 supports hardware stall detection by comparing the IPROPI pin voltage to the VREF pin voltage or 500 mV as applicable.

9.2.2.1 Application Description

The principle of this stall detection scheme relies on the fact that motor current increases during stall conditions as shown in 図 9-2. The DRV8215 compares the voltage on the IPROPI pin to the voltage on the VREF pin to determine whether a stall condition has occurred. The TINRUSH register sets the timing, t_{INRUSH}, so the DRV8215 ignores the inrush current at motor startup. The SMODE pin configures how the DRV8215 responds to a stall condition. The IMODE pin configures whether the device regulates current during inrush and stall currents. When a stall condition occures, nFAULT pin becomes low and the appropriate registers indicate stall to the microcontroller using the I^2C pins. セクション 7.3.5 provides all the details for configuring the stall detection feature.

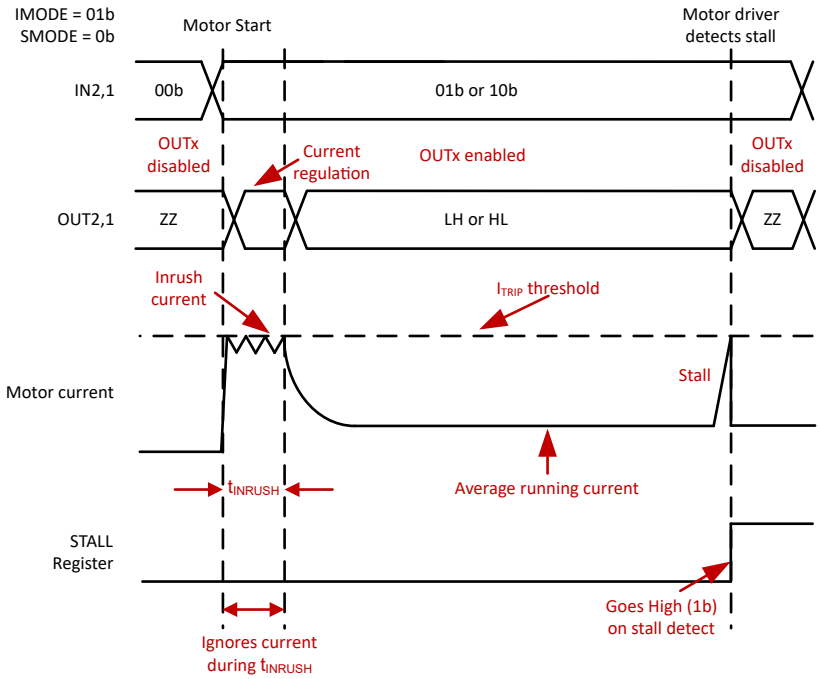


図 9-2. Example timing diagram for stall detection

9.2.2.1.1 Stall Detection Timing

Large inrush current occurs during motor start up because motor speed is low. As the motor accelerates, the motor current drops to an average level because the back electromotive force (EMF) in the motor increases with speed. The inrush current should not be mistaken for a stall condition, so the DRV8215 uses the TINRUSH register to ignore the inrush current during the startup time, t_{INRUSH}. セクション 7.3.5 describes the overall details for using the stall detection feature.

When designing for the t_{INRUSH} time, it is important to include enough margin to account for tolerances and variation in the DRV8215 and the system overall.

9.2.2.1.2 Hardware Stall Threshold Selection

The voltage on the VREF pin selects I_{TRIP} threshold which sets the current level for stall detection and current regulation. This threshold should be chosen such that I_{TRIP} is less than the stall current of the motor when

current regulation is not used. It should also be set low enough to account for variation in the stall current due to changes in the motor supply voltage, V_{VM}, and temperature.

9.2.3 Motor Speed and Voltage Regulation Application

This section describes Motor Speed and Voltage Regulation and the associated tuning procedure using an example.

9.2.3.1 Tuning Parameters

This section explains the tuning process for the Speed and Voltage Regulation feature described earlier.

9.2.3.1.1 Resistance Parameters

This section describes how to select INV_R and INV_R_SCALE. The first step is to find the motor resistance. This can be done in three ways:

1. Use the motor resistance value mentioned in the data sheet of the motor. If this is not available, use one of the other methods listed below.
2. Perform a voltage sweep at the motor terminals, stall the motor at each voltage level, and measure the motor current. Please note that at least 10 measurements are required at every voltage level whilst rotating the motor by approximately 30° for each measurement. This is because it is unknown if the commutator segments are in contact with the brushes in a particular motor position which renders a lower, incorrect motor resistance value. **If motor resistance from the motor's data sheet is unavailable, then this method is recommended to obtain the value of motor resistance.** Take the average of all values to calculate motor resistance.
3. Measure the motor resistance using a digital multimeter. Please note that this process also needs to be done at every voltage level for 10 measurements each and then averaged out at the end for the same reason as mentioned above.

注

To perform a voltage sweep,

1. Connect the motor directly to the power supply at a voltage just below where the motor starts to spin. As an example, set the power supply voltage to 1.5V for a 12V motor if the motor starts to spin at 1.7V.
2. Read the current using a current probe, inline multimeter, or power supply readout.
3. Calculate the motor resistance using the following equation: Motor Resistance = Voltage/Stall Current.
4. Repeat this test across a range of voltages (ex. 1.3V, 1.4V, 1.5V, 1.6V) and find a consistent motor resistance value.

Once the motor resistance value is found, select an appropriate value of INV_R_SCALE and calculate INV_R. The formula to calculate INV_R is:

$$\text{INV\_R} = \frac{1}{\text{Motor Resistance}} \times \text{INV\_R\_SCALE} \tag{10}$$

For example, if the motor resistance is **25Ω**, we have the following possible results based on the choice of INV_R_SCALE:

表 9-2. Selection Example for INV_R_SCALE and INV_R

Bit	INV_R_SCALE value	INV_R_SCALE/Motor Resistance (Actual Value)	Rounded Value INV_R	Comment
00b	2	2/25=0.08	0	Do not select, since output is 0.
01b	64	64/25=2.56	3	Avoid selecting, since low bit precision.
10b	**1024**	**1024/25=40.96**	**41**	**Can select this value.**
11b	8192	8192/25=327.68	328	Cannot select this value because 328 exceeds the maximum limit for INV_R (255).

9.2.3.1.2 KMC and KMC_SCALE

Selection of KMC_SCALE and KMC can be divided into two cases based on 式 8:

1. Value of the motor back emf constant, K_V is known to the user from the data sheet of the motor.
2. Value of the motor back emf constant, K_V is unknown to the user.

9.2.3.1.2.1 Case I

In case 1, 式 8 can be used. Choose the value of KMC_SCALE such that KMC is within the range of 0 to 255 with highest bit resolution. As an example, if K_V= 0.01 and number of ripples per revolution, N_R=10, K_V/N_R = 10^{-3}. The following table lists the available options:

表 9-3. Selection Example for KMC_SCALE

Bit	KMC_SCALE value	K_V/N_Rx KMC_SCALE (Actual Value)	Rounded Value (KMC)	Comment
00b	24 x 2^8	6.144	6	Avoid selecting, since low bit precision.
01b	24 x 2^9	12.288	12	Avoid selecting, since low bit precision.
10b	24 x 2^{12}	98.304	98	Avoid selecting, since low bit precision.
11b	**24 x 2^{13}**	**196.608**	**197**	**Can select this value as this has the highest bit precision.**

9.2.3.1.2.2 Case II

In case 2, KMC and KMC_SCALE need to be tuned manually using either of the two methods:

9.2.3.1.2.2.1 Method 1: Tuning from Scratch

This method resets both parameters in the beginning before arriving at tuned values. 図 9-3 displays a flowchart for tuning KMC_SCALE using this method. KMC can be found using Binary Search as shown in 図 9-4

9.2.3.1.2.2.1.1 Tuning KMC_SCALE

1. Obtain the value of actual ripple speed in rad/s using either of the two methods:
   a. Use an oscilloscope to observe motor current waveform to measure the ripple frequency. This can be done in two ways:
      - Through the IPROPI pin which provides an output proportional to the motor current.
      - Through a current probe.

The frequency of ripples is observed in Hz on the oscilloscope. Please consider at least 20 ripples while calculating frequency. Divide the number of ripples by the time taken for calculating the frequency in Hz. Convert into rad/s using 式 12. Please note that **this is the recommended method**.

b. Use a tachometer to obtain the motor speed in rpm. Convert the motor speed into ripple speed using 式 11. Finally, convert the ripple speed in rpm to ripple speed in rad/s using 式 13.

$$\text{Ripple Speed} = \text{Motor Speed} \times N_R \tag{11}$$

$$\text{Ripple Speed (in rad/s)} = \text{Ripple Speed (in Hz)} \times 2\pi \tag{12}$$

$$\text{Ripple Speed}\left(\text{in rad/s}\right) = \text{Ripple Speed}\left(\text{in rpm}\right) \times \frac{2\pi}{60} \tag{13}$$

Where N_R is the number of ripples per revolution. Let this value be called OBS_SPEED.

2. Select the lowest value of KMC_SCALE, 00b. Set KMC to the highest possible value, 255.
3. Refer to 表 7-16 to set W_SCALE to a value where maximum ripple speed is more than OBS_SPEED. For example, if OBS_SPEED is 6000 rad/s, set W_SCALE to 01b allowing a maximum speed of 8160 rad/s.
4. Convert the ripple speed on the SPEED register into rad/s by multiplying SPEED with W_SCALE. For example, if SPEED reads 0x04 and W_SCALE is set to 10b (corresponds to 64 rad/s), then ripple speed in rad/s = 4*64 = 256 rad/s. Let this value be called EST_SPEED.
5. If EST_SPEED is lower than OBS_SPEED, increase KMC_SCALE by one bit.
6. Repeat steps 4-5 until EST_SPEED is higher than OBS_SPEED.
7. Set KMC_SCALE to the previous value. For example, if 11b was obtained in the previous step, set KMC_SCALE to 10b. This is the tuned value of KMC_SCALE.

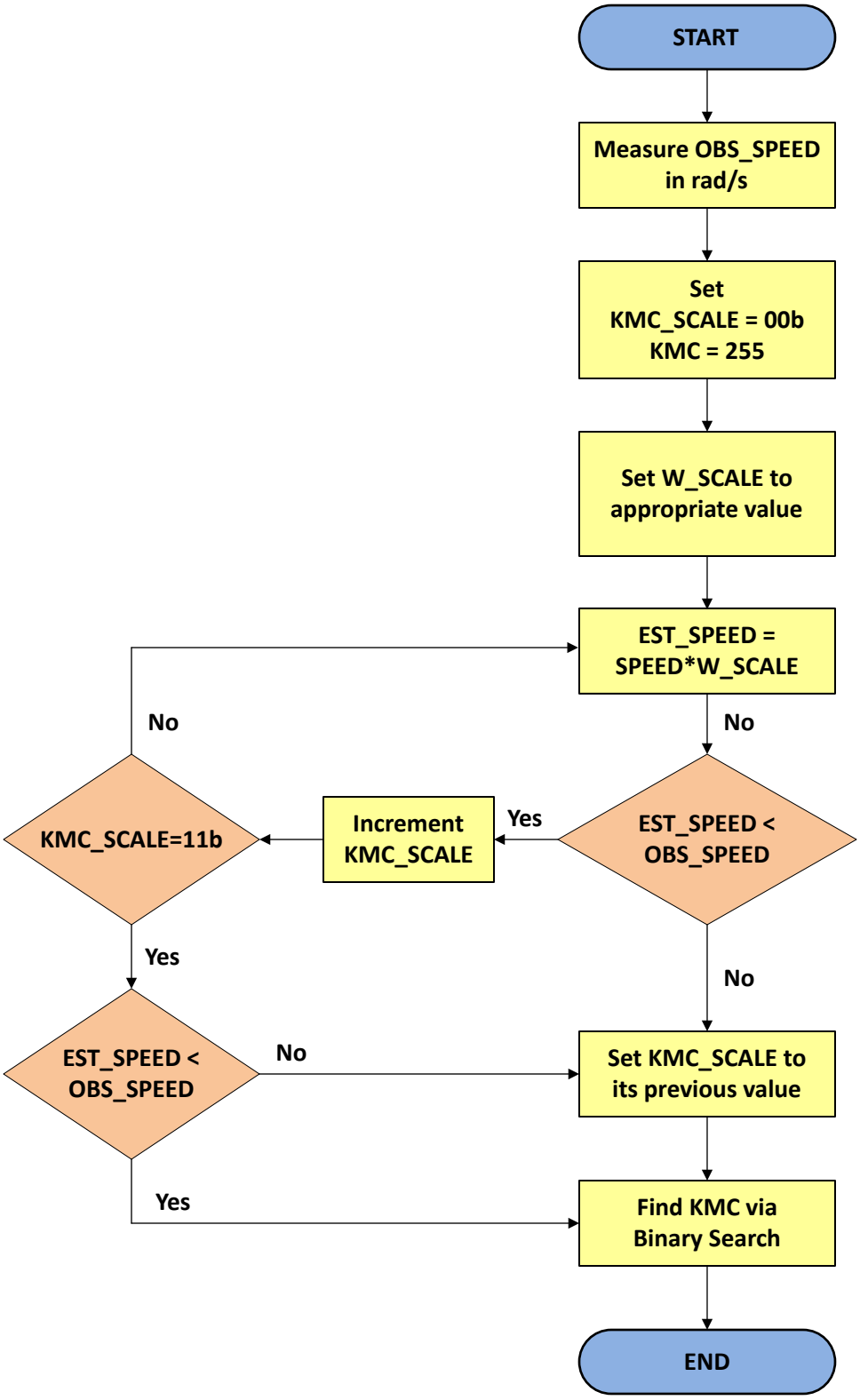


図 9-3. KMC_SCALE Tuning Procedure

9.2.3.1.2.2.1.2 Tuning KMC

1. Verify that EST_SPEED < OBS_SPEED and value of KMC is 255. If this is not the case, please restart the tuning process.
2. Let START = 1 and END = 255.
3. Set KMC to START and obtain the value of OBS_SPEED in rad/s **from step 1 of the KMC_SCALE tuning procedure**.
4. If EST_SPEED is within OBS_SPEED ± W_SCALE value from 表 7-16, stop the tuning process and record the value of KMC. For example, if W_SCALE = 10b (corresponds to 64 rad/s), OBS_SPEED = 6000 rad/s, and EST_SPEED = 5952 rad/s or 6016 rad/s, stop the tuning process.
5. Let MID = (START+END)/2, rounded off to the nearest integer.
6. If EST_SPEED is higher than OBS_SPEED in this step, set KMC to MID. If EST_SPEED is lower than OBS_SPEED in this step, decrement KMC_SCALE by one bit and repeat the binary search procedure to tune KMC.
7. If EST_SPEED is higher than OBS_SPEED, update START = MID. If EST_SPEED is lower than OBS_SPEED, update END = MID.
8. Repeat steps 4-7 until EST_SPEED is within OBS_SPEED ± W_SCALE value from 表 7-16. Record the value of KMC.

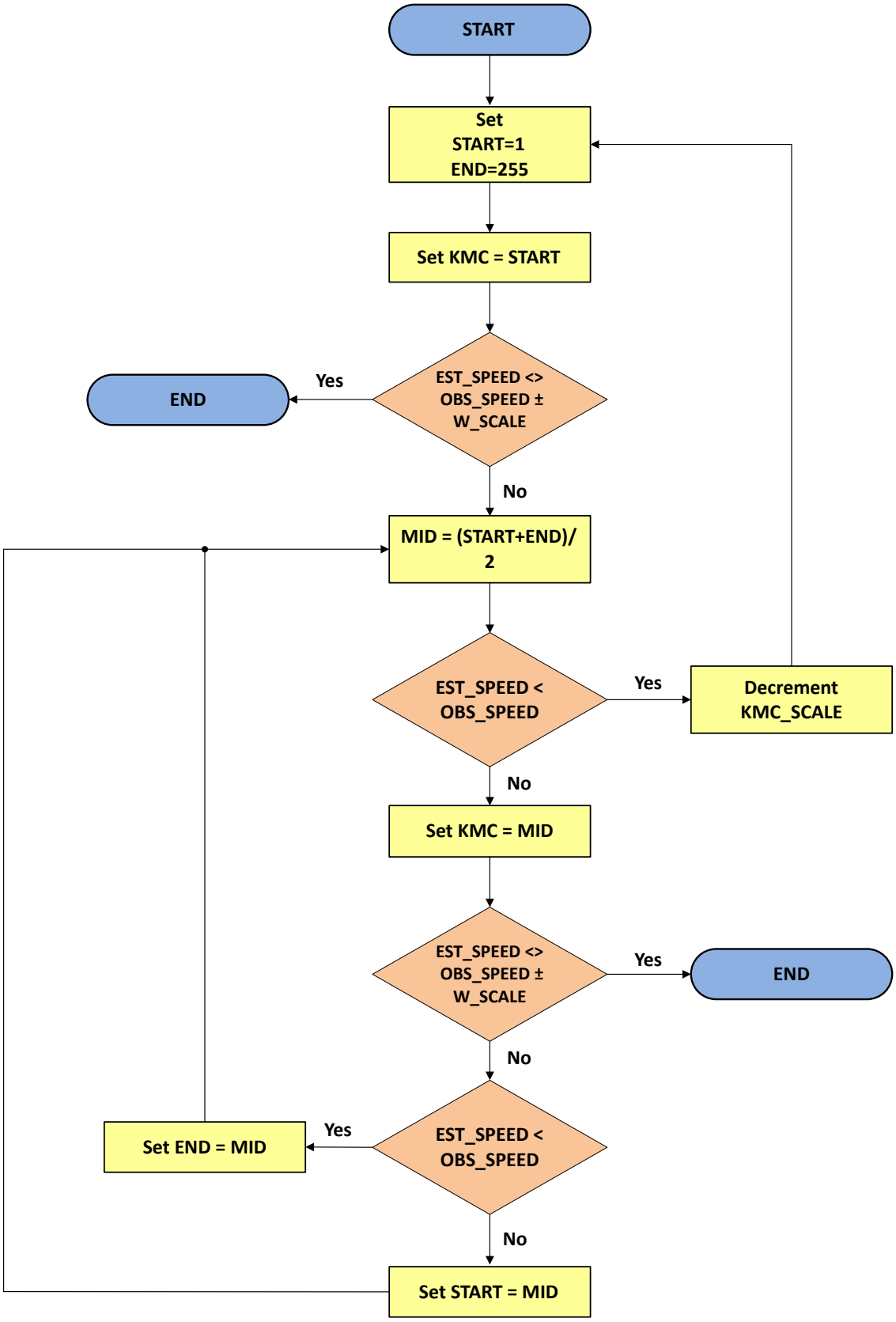


図 9-4. Binary Search Algorithm to Find KMC

注

1. Tuning is not possible in the following cases:
   a. EST_SPEED is higher than OBS_SPEED after step 4 in the KMC_SCALE tuning process (KMC_SCALE = 00b; KMC = 255), or
   b. EST_SPEED is lower than OBS_SPEED after step 3 in the Binary Search Method for KMC (KMC_SCALE = 11b, KMC = 0).
2. Multiple sets of KMC and KMC_SCALE exist. If found, then choose the set with highest bit resolution.

9.2.3.1.2.2.2 Method 2: Using the Proportionality factor

This method utilises the factor of proportionality that associates KMC and KMC_SCALE with the ripple speed, ω_{ripple}. ω_{ripple} is directly proportional to KMC_SCALE but varies inversely with KMC. Let k_d be a dummy constant. We have:

$$\omega_{ripple} = k_d \frac{KMC\_SCALE}{KMC} \tag{14}$$

Using the subscript 'def' to denote default, we have the following equation for default values of KMC and KMC_SCALE:

$$\omega_{def} = k_d \frac{KMC\_SCALE_{def}}{KMC_{def}} \tag{15}$$

Using the subscript 'tuned', we similarly have the following equation for tuned values of KMC and KMC_SCALE:

$$\omega_{tuned} = k_d \frac{KMC\_SCALE_{tuned}}{KMC_{tuned}} \tag{16}$$

Taking the ratio of the two equations above, the dummy constant, k_d, cancels out:

$$\frac{\omega_{tuned}}{\omega_{def}} = \frac{KMC\_SCALE_{tuned}}{KMC_{tuned}} \times \frac{KMC_{def}}{KMC\_SCALE_{def}} \tag{17}$$

At this point, the following is known:

1. KMC_SCALE_{def} = 11b (24 x 2^{13}) is the default value of KMC_SCALE from the register map.
2. KMC_{def} = 163 is the default value of KMC from the register map.
3. ω_{tuned} is the actual value of the ripple speed in rad/s. Please refer to step 1 of the KMC_SCALE Tuning Method 1 for obtaining this value.

To obtain ω_{def}, select a value of W_SCALE based on step 3 of KMC_SCALE Tuning Method 1. Next, convert the ripple speed on the SPEED register obtained using KMC_SCALE_{def} and KMC_{def} into rad/s by multiplying SPEED with W_SCALE. For example, if SPEED reads 0x04 and W_SCALE is set to 10b (corresponds to 64 rad/s), then ripple speed in rad/s = 4*64 = 256 rad/s.

Plugging the four values above and simplifying, we get a ratio of KMC_SCALE_{tuned} and KMC_{tuned} as a constant number. Select KMC_SCALE_{tuned} from the four available values such that KMC_{tuned} has the highest bit precision within limits (0 to 255). A working example is shown below.

9.2.3.1.2.2.2.1 Working Example

As a working example, let ω_{tuned}= 500 rad/s. Thus,

- W_SCALE is chosen as 00b (16 rad/s) since 500 < 4080, the maximum value allowable by W_SCALE based on 表 7-16.
- Let SPEED = 0x30. Thus, ω_{def}=48*16=768 rad/s.
- Plugging these values into 式 17, we have:

$$\frac{500}{768} = \frac{\text{KMC\_SCALE}_{\text{tuned}}}{\text{KMC}_{\text{tuned}}} \times \frac{163}{24 \times 2^{13}} \quad (18)$$

- Simplifying, we get:

$$785.276 = \frac{\text{KMC\_SCALE}_{\text{tuned}}}{\text{KMC}_{\text{tuned}}} \quad (19)$$

- The final step is to choose $\text{KMC\_SCALE}_{\text{tuned}}$ such that $\text{KMC}_{\text{tuned}}$has the highest precision within limits (0 to 255). The following table illustrates the possible choices:

表 9-4. Selection Example for KMC_SCALE

Bit	$\text{KMC\_SCALE}_{\text{tuned}}$ value	$\text{KMC\_SCALE}_{\text{tuned}}$ / 785.276 (Actual Value)	$\text{KMC}_{\text{tuned}}$ (Rounded Value)	Comment
00b	24×2^{8}	7.82	8	Avoid selecting, since low precision.
01b	24×2^{9}	15.64	16	Avoid selecting, since low precision.
10b	24×2^{12}	125.18	125	Avoid selecting, since low precision.
11b	**24×2^{13}**	**250.36**	**250**	**Can seleect this value, since highest precision.**

9.2.4 Motor Voltage

The motor voltage to use depends on the ratings of the motor selected and the desired RPM. A higher voltage spins a brushed DC motor faster with the same PWM duty cycle applied to the power FETs. A higher voltage also increases the rate of current change through the inductive motor windings.

9.2.5 Motor Current

Motors experience large currents at low speed, initial startup, and stalled rotor conditions. The large current at motor startup is sometimes called inrush current. The current regulation feature in the DRV8215 can help to limit these large currents. Additionally, DRV8215's soft-start feature can be used to limit the inrush current by ramping the PWM duty cycle during startup time. Alternatively, the microcontroller may limit the inrush current via a similar procedure.

9.3 Power Supply Recommendations

9.3.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. Having more bulk capacitance is generally beneficial, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The capacitance of the power supply and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and motor drive system limits how the rate current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

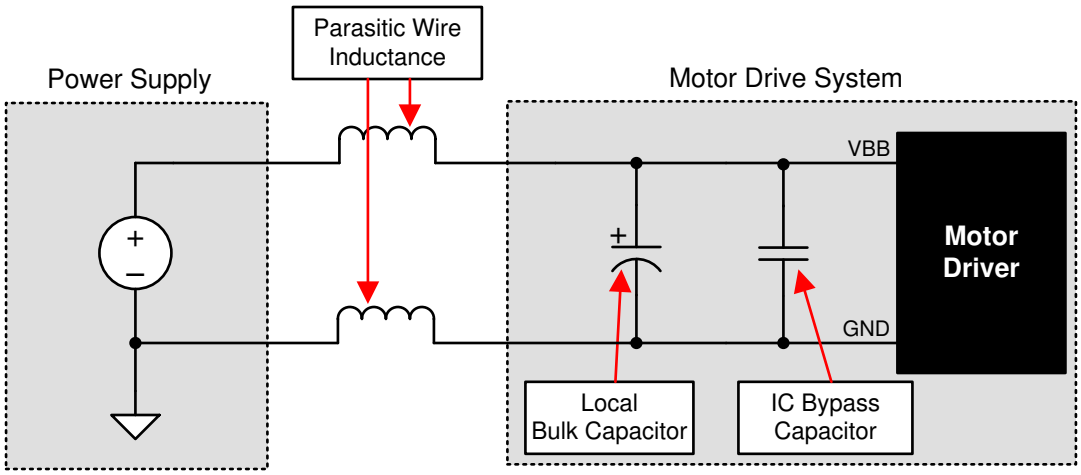


図 9-5. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

9.4 Layout

9.4.1 Layout Guidelines

Since the DRV8215 integrates power MOSFETs capable of driving high current, careful attention should be paid to the layout design and external component placement. Some design and layout guidelines are provided below.

- Low ESR ceramic capacitors should be utilized for the VM to GND bypass capacitor. X5R and X7R types are recommended.
- The VM power supply capacitors should be placed as close to the device as possible to minimize the loop inductance.
- The VM power supply bulk capacitor can be of ceramic or electrolytic type, but should also be placed as close as possible to the device to minimize the loop inductance.
- VM, OUT1, OUT2, and GND carry the high current from the power supply to the outputs and back to ground. Thick metal routing should be utilized for these traces as is feasible.
- The device thermal pad should be attached to the PCB top layer ground plane and internal ground plane (when available) through thermal vias to maximize the PCB heat sinking.
- A recommended land pattern for the thermal vias is provided in the package drawing section.
- The copper plane area attached to the thermal pad should be maximized to ensure optimal heat sinking.

10 デバイスおよびドキュメントのサポート

テキサス・インスツルメンツでは、幅広い開発ツールを提供しています。デバイスの性能の評価、コードの生成、ソリューションの開発を行うためのツールとソフトウェアを以下で紹介します。

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10.2 サポート・リソース

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
April 2024	*	Initial Release

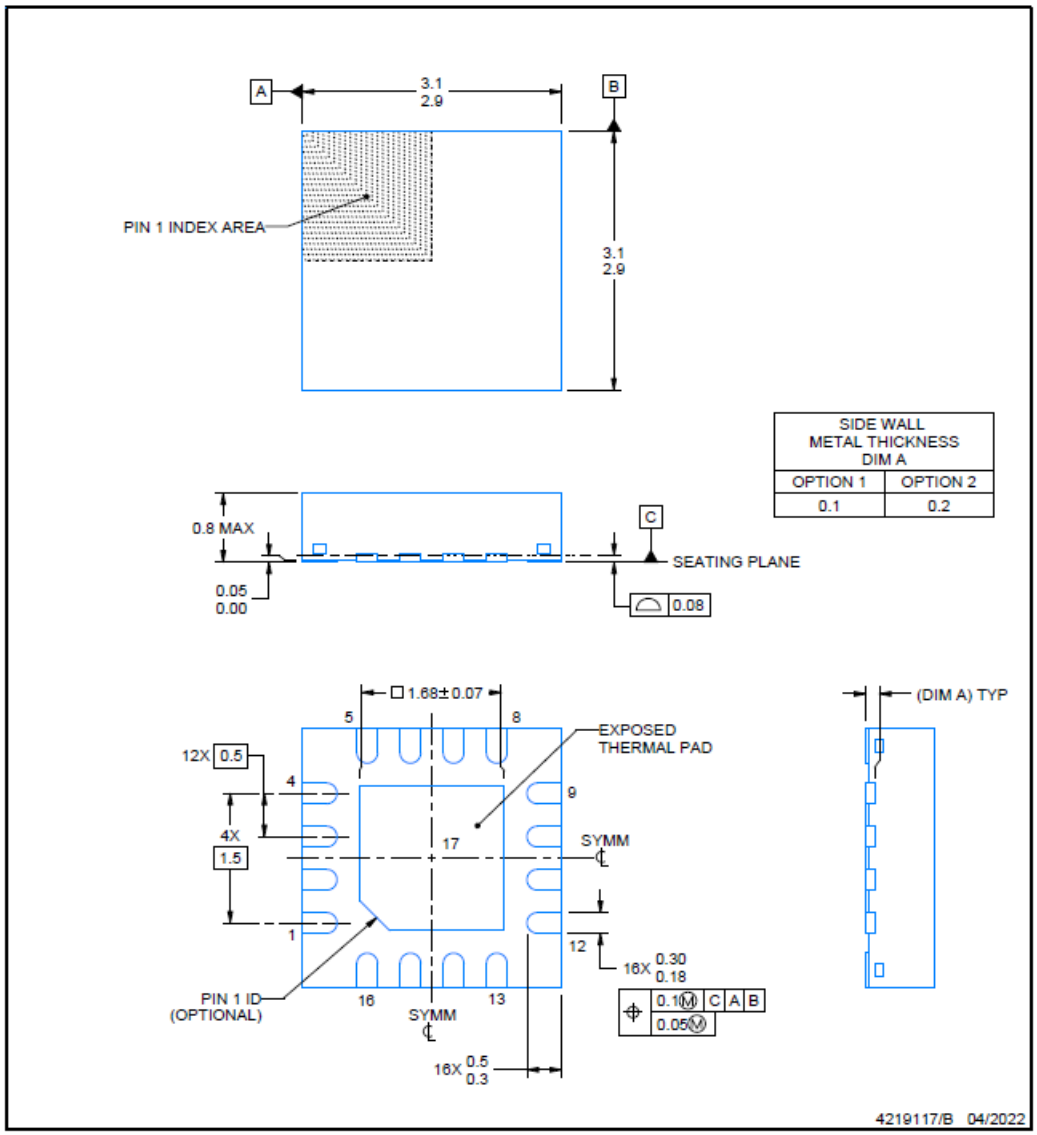
12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、指定のデバイスに使用できる最新のデータです。このデータは、予告なく、このドキュメントを改訂せずに変更される場合があります。本データシートのブラウザ版を使用されている場合は、画面左側のナビゲーション リンクを参照してください。

RTE0016C — **PACKAGE OUTLINE**

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



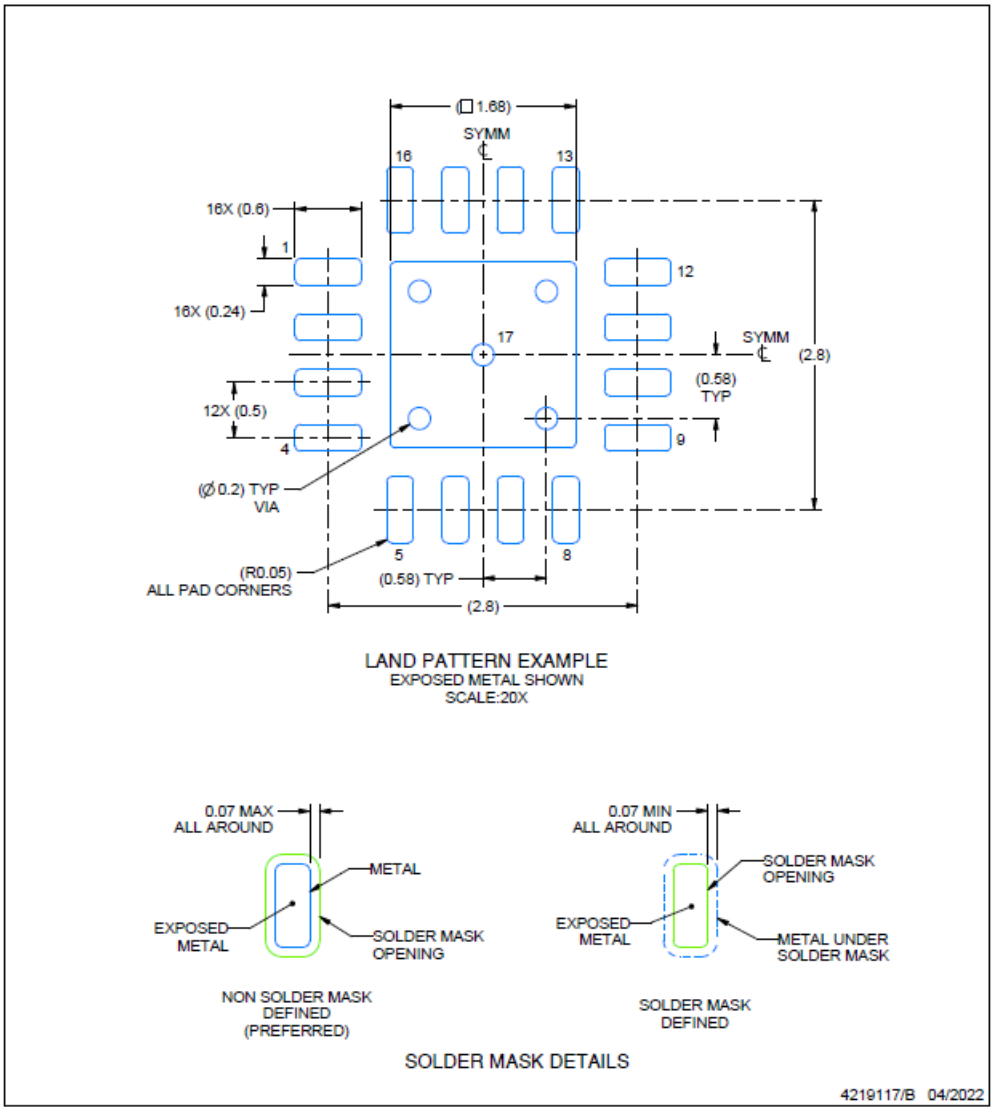
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RTE0016C — **WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



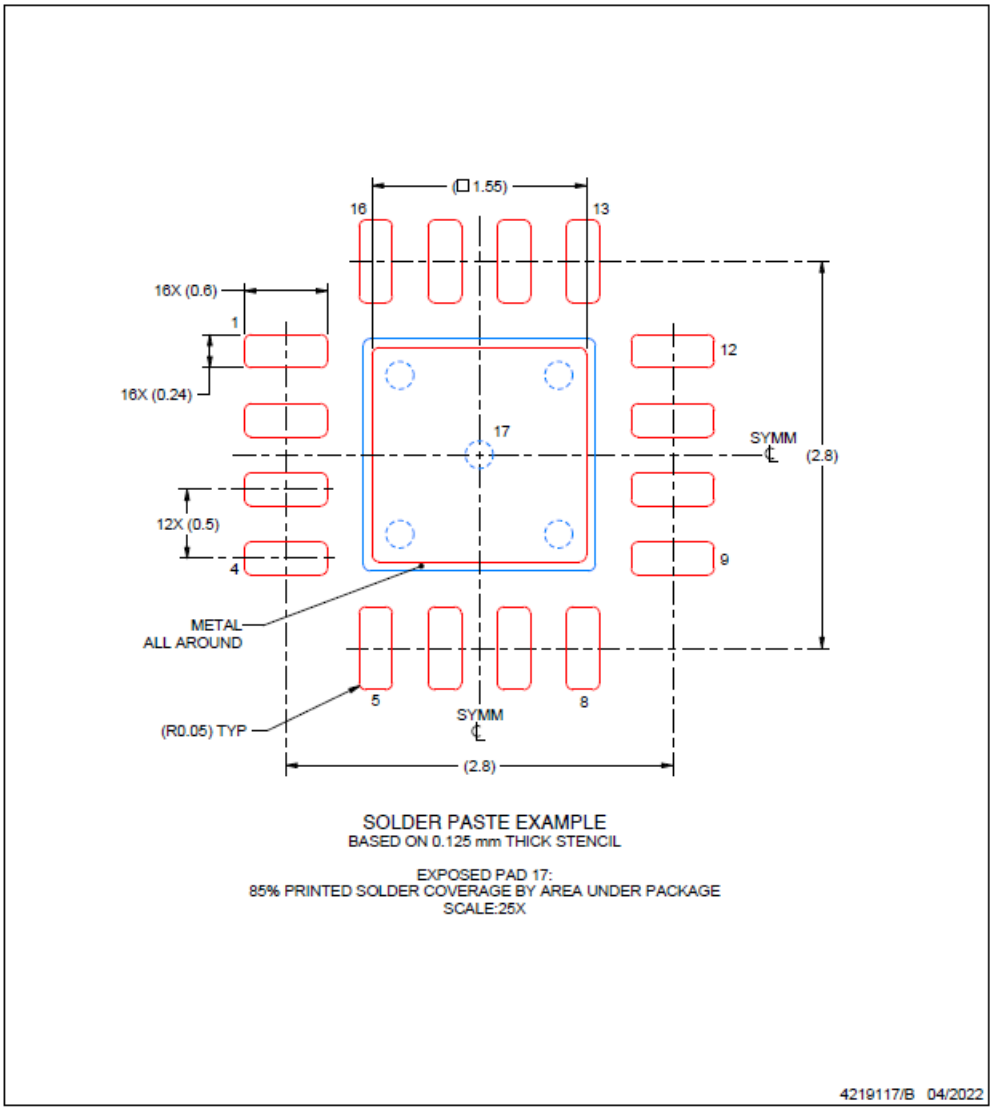
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RTE0016C — **WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV8215RTER	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8215
DRV8215RTER.A	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8215

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

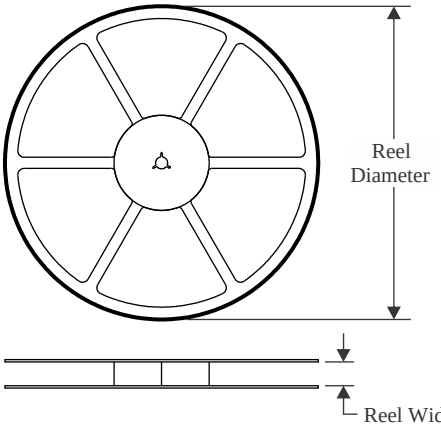
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

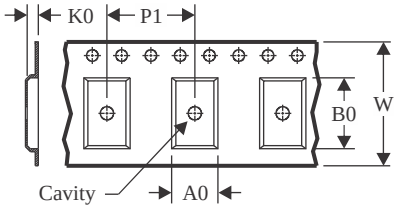
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

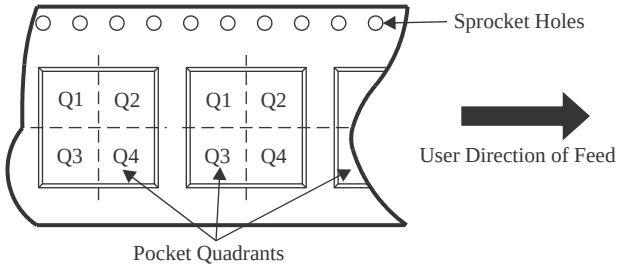


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

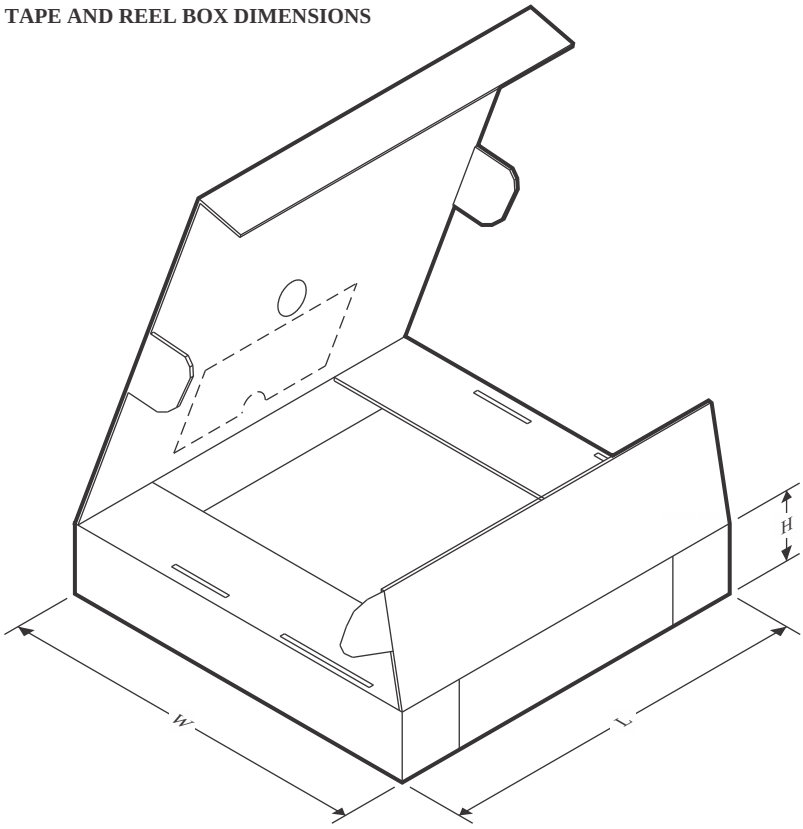
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8215RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8215RTER	WQFN	RTE	16	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

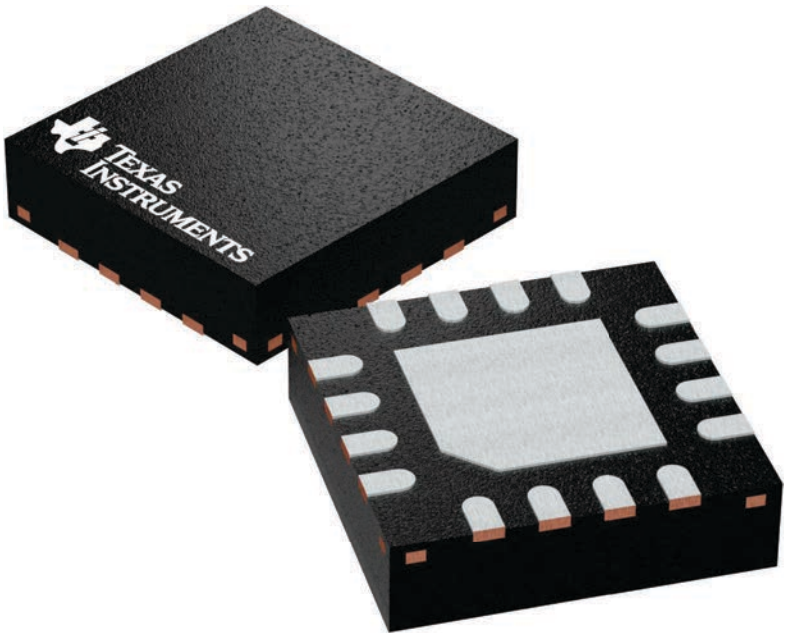
RTE 16

WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

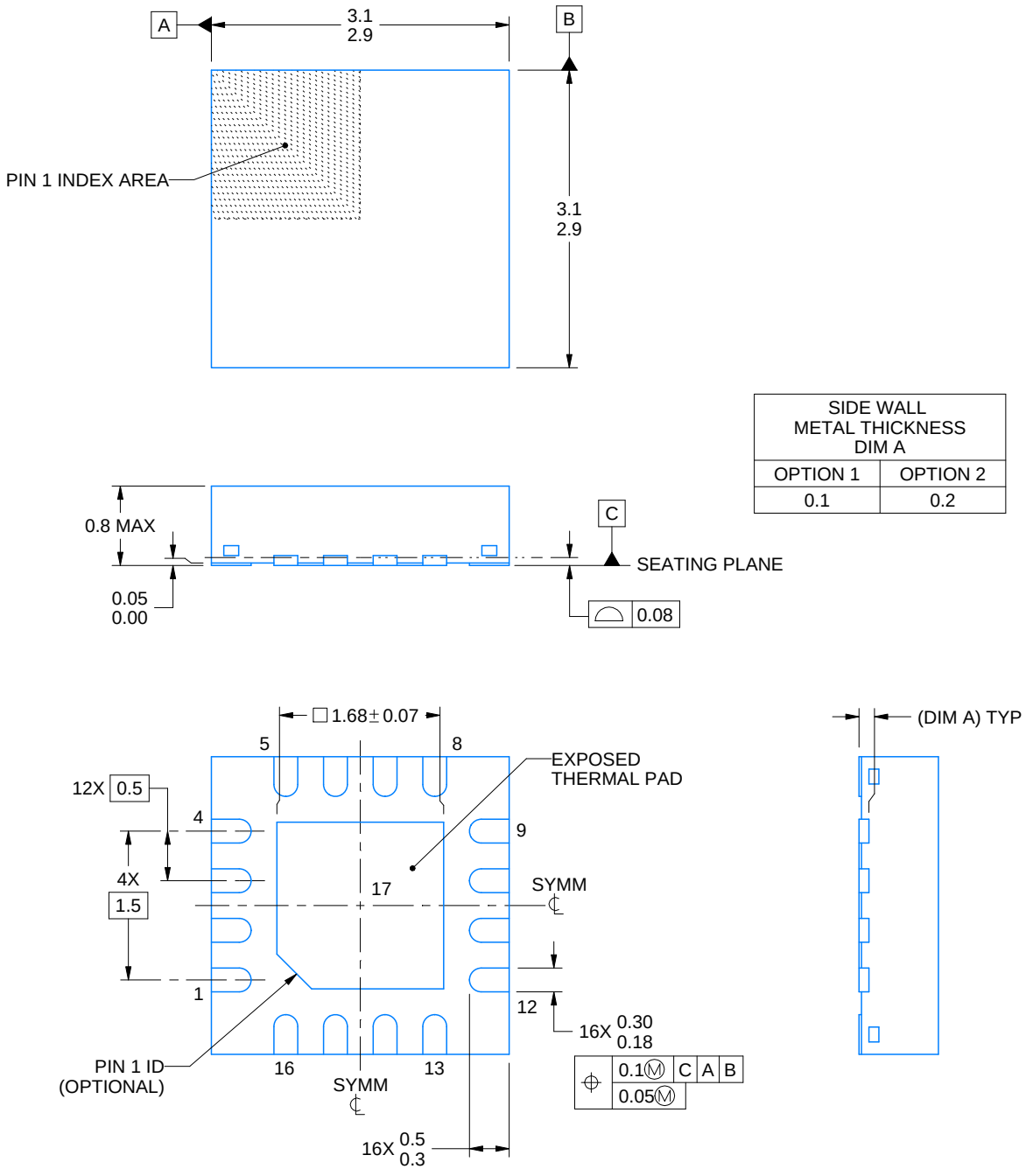


RTE0016C

PACKAGE OUTLINE

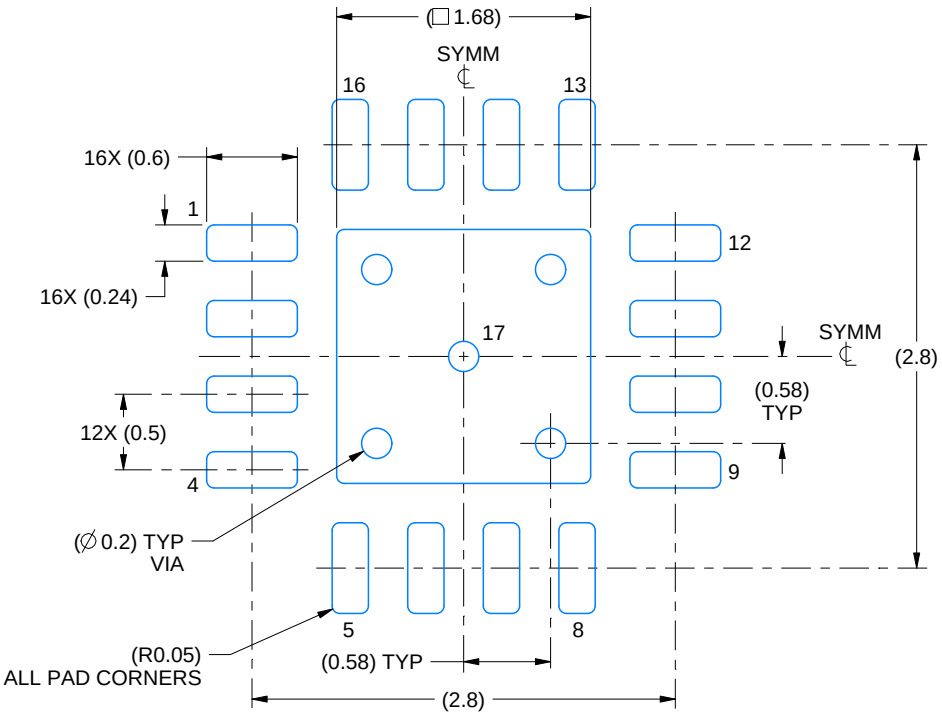
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

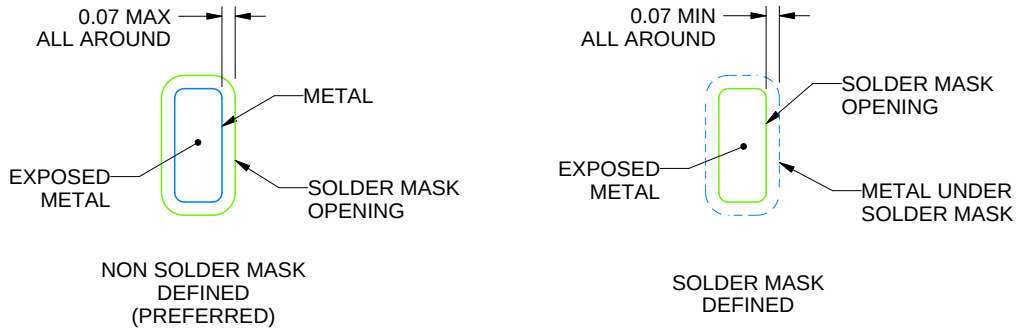


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4219117/B 04/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
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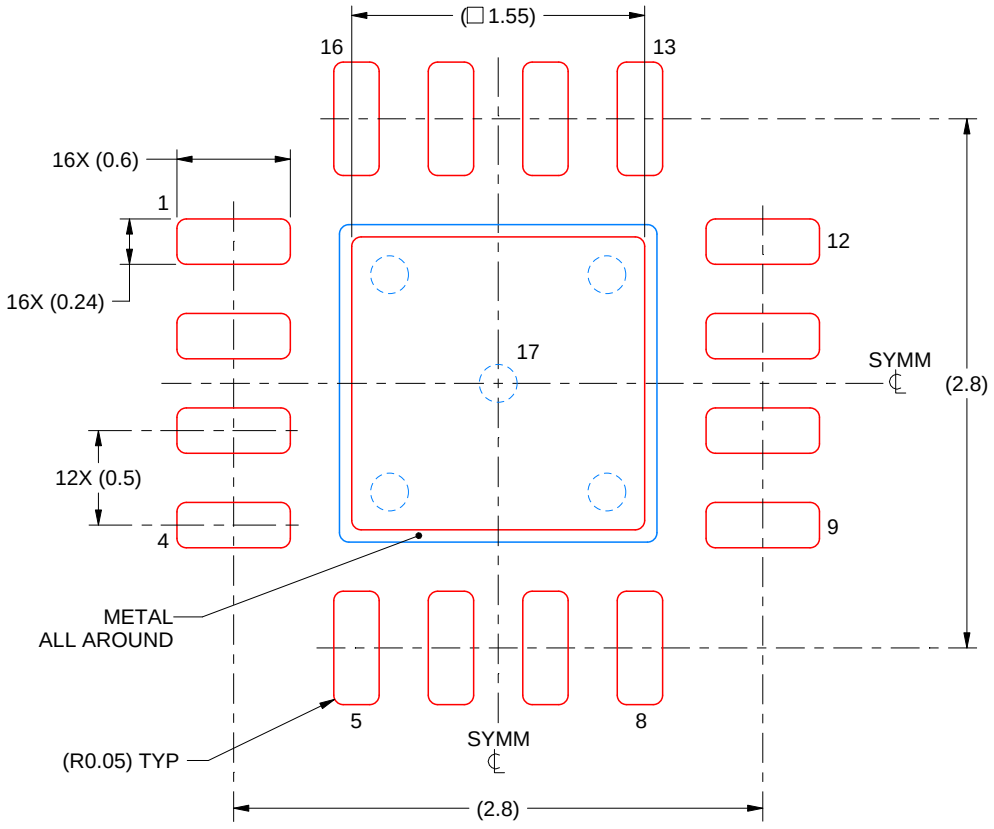

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219117/B 04/2022

NOTES: (continued)

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最終更新日：2025 年 10 月