DRV8804 クワッド シリアル インターフェイス内蔵ローサイド ドライバ IC

1 特長

- 4 チャネル保護ローサイドドライバ
  - 過電流保護機能付き N チャネル MOSFET 4 個
  - 内蔵の誘導性クランプ ダイオード
  - シリアル インターフェイス
- DW パッケージ:1.5A (シングル チャネル オン) / 800mA (4 チャネル オン):チャネルあたりの最大駆動電流 (25°C 時)
- PWP パッケージ:2A (シングル チャネル オン) / 1A (4 チャネル オン):チャネルあたりの最大駆動電流 (25°C、適切な PCB ヒートシンク使用時)
- DYZ パッケージ:1.9A (シングル チャネル オン) / 0.9A (4 チャネル オン):チャネルあたりの最大駆動電流 (25°C、適切な PCB ヒートシンク使用時)
- 8.2V ～ 60V の動作電源電圧範囲
- 熱特性強化型の表面実装パッケージ

2 アプリケーション

- リレー ドライバ
- ユニポーラ型ステッピング モーター ドライバ
- ソレノイド ドライバ
- 汎用ローサイド スイッチ アプリケーション

3 概要

DRV8804 は、過電流保護機能を備えた 4 チャネル ローサイド ドライバを実現します。誘導性負荷によって発生するターンオフ過渡をクランプするためのダイオードを内蔵しており、ユニポーラ型ステッピング モーター、DC モーター、リレー、ソレノイド、その他の負荷の駆動に使用できます。

SOP (DW) パッケージでは、DRV8804 は 25°C でチャネルあたり最大 1.5A (1 チャネル オン) または 800mA (すべてのチャネルがオン) の連続出力電流を供給できます。HTSSOP (PWP) パッケージの場合、このデバイスは 25°C でチャネルあたり最大 2A (1 チャネル オン) または 1A (4 チャネル オン) の連続出力電流を供給できます。SOT-23-THN (DYZ) パッケージでは、DRV8804 は 25°C、適切な PCB ヒートシンク使用時で、チャネルあたり最大 1.9A (1 チャネル オン) または 900mA (すべてチャネルがオン) の連続出力電流を供給できます。

シリアル データ出力を含むシリアル インターフェイスが用意されており、デイジーチェーン接続により、1 つのシリアル インターフェイスで複数のデバイスを制御できます。

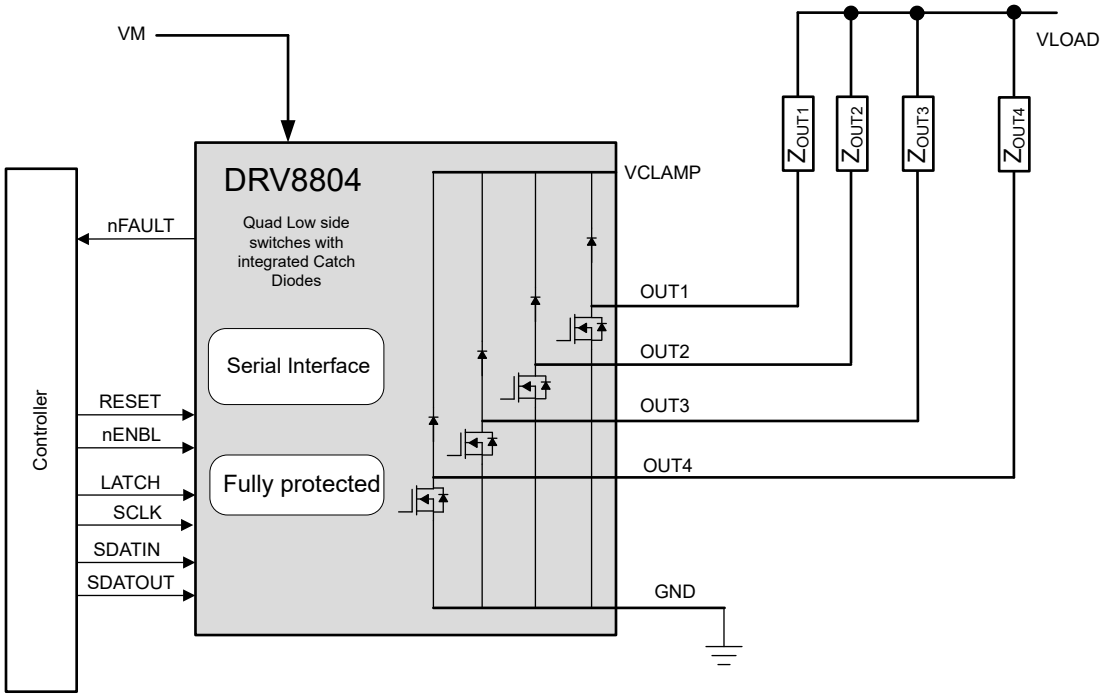
過電流保護、短絡保護、低電圧誤動作防止、過熱および故障に備えて内部シャットダウン機能が用意されており、FAULT 出力ピンで示されます。

DRV8804 は、20 ピンの熱的に強化された SOP パッケージ、16 ピンの HTSSOP パッケージ、16 ピンの SOT-23-THN パッケージ (環境配慮型:RoHS 準拠、Sb/Br 非含有) で供給されます。

デバイス情報 (1)

部品番号	パッケージ	パッケージ サイズ(2)	本体サイズ (公称)
DRV8804DW	SOIC (20)	12.80mm × 10.30mm	12.80mm × 7.50mm
DRV8804PWP	HTSSOP (16)	5.00mm × 6.40mm	5.00mm × 4.40mm
DRV8804DYZ	SOT-23-THN (16)	4.20mm × 2.00	4.20mm × 2.00mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



概略回路図

Table of Contents

4 Device Comparison

Following is the Summary of the R_{ON} and package offerings for DRV8804

Part number	LS R_{ON}(TYP)	Package	Body Size (nominal)
DRV8804	500 mΩ	SOIC (20)	12.80mm x 7.50mm
		HTSSOP (16)	5.00mm × 4.40mm
	400 mΩ	SOT-23-THN (16)	4.20mm × 2mm

5 Pin Configuration and Functions

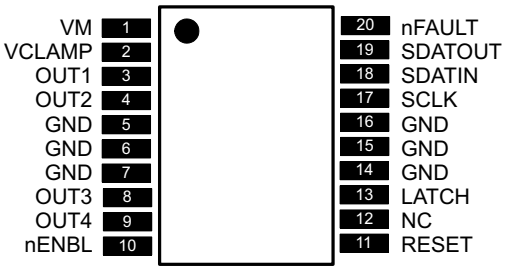


図 5-1. DW (Wide SOIC) Package 20-Pin Package Top View

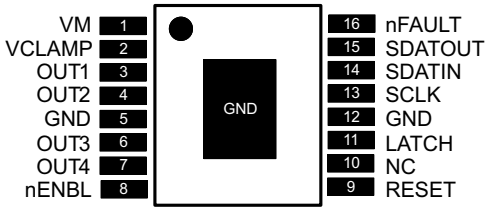


図 5-2. PWP (HTSSOP) 16-Pin Package Top View

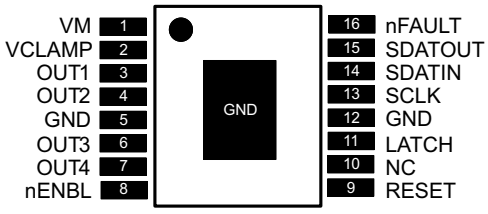


図 5-3. DYZ (SOT-23-THN) 16-Pin Package Top View

5.1 Pin Functions

PIN				I/O[1]	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	SOIC	HTSSOP	SOT-23-THN			
POWER AND GROUND						
GND	5, 6, 7, 14, 15, 16	5, 12, PPAD	5,12,PPAD	—	Device ground	All pins must be connected to GND.
VM	1	1	1	—	Device power supply	Connect to motor supply (8.2 V - 60 V).
CONTROL						
LATCH	13	11	11	I	Latch input	Rising edge latches shift register to output stage – internal pulldown
nENBL	10	8	8	I	Enable input	Active low enables outputs – internal pulldown
RESET	11	9	9	I	Reset input	Active-high reset input initializes internal logic – internal pulldown
SCLK	17	13	13	I	Serial clock	Serial clock input – internal pulldown
SDATIN	18	14	14	I	Serial data input	Serial data input – internal pulldown
SDATOUT	19	15	15	O	Serial data output	Serial data output; push-pull structure; see serial interface section for details
STATUS						
nFAULT	20	16	16	OD	Fault	Logic low when in fault condition (overtemperature, overcurrent)
OUTPUT						
OUT1	3	3	3	O	Output 1	Connect to load 1
OUT2	4	4	4	O	Output 2	Connect to load 2
OUT3	8	6	6	O	Output 3	Connect to load 3
OUT4	9	7	7	O	Output 4	Connect to load 4
VCLAMP	2	2	2	—	Output clamp voltage	Connect to VM supply, or zener diode to VM supply

(1) Directions: I = input, O = output, OD = open-drain output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
VM	Power supply voltage	–0.3	65	V
VOUTx	Output voltage	–0.3	65	V
VCLAMP	Clamp voltage	–0.3	65	V
SDATOUT, nFAULT	Output current		20	mA
	Peak clamp diode current		2	A
	DC or RMS clamp diode current		1	A
	Digital input pin voltage	–0.5	7	V
SDATOUT, nFAULT	Digital output pin voltage	–0.5	7	V
	Peak motor drive output current, t < 1 µs	Internally limited		A
	Continuous total power dissipation	See セクション 6.5		
T_J	Operating virtual junction temperature	–40	150	°C
T_{stg}	Storage temperature	–60	150	°C

(1) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±3000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_M	Power supply voltage	8.2		60	V
V_{CLAMP}	Output clamp voltage(2)	0		60	V
I_{OUT}	Continuous output current, single channel on, T_A = 25°C, SOIC package(1)			1.5	A
	Continuous output current, four channels on, T_A = 25°C, SOIC package(1)			0.8	
	Continuous output current, single channel on, T_A = 25°C, HTSSOP package(1)			2	
	Continuous output current, four channels on, T_A = 25°C, HTSSOP package(1)			1	
	Continuous output current, single channel on, T_A = 25°C, DYZ package(1)			1.9	
	Continuous output current, four channels on, T_A = 25°C, DYZ package(1)			0.9	

(1) Power dissipation and thermal limits must be observed.
(2) V_{CLAMP} is used only to supply the clamp diodes. It is not a power supply input.

6.4 Electrical Characteristics

T_A = 25°C, over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES					

T_A = 25°C, over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VM}	VM operating supply current	V_M = 24 V		1.6	2.1	mA
V_{UVLO}	VM undervoltage lockout voltage	V_M rising			8.2	V
LOGIC-LEVEL INPUTS (SCHMITT TRIGGER INPUTS WITH HYSTERESIS)						
V_{IL}	Input low voltage			0.6	0.7	V
V_{IH}	Input high voltage		2			V
V_{HYS}	Input hysteresis			0.45		V
I_{IL}	Input low current	VIN = 0	–20		20	µA
I_{IH}	Input high current	VIN = 3.3 V			100	µA
R_{PD}	Pulldown resistance			100		kΩ
nFAULT OUTPUT (OPEN-DRAIN OUTPUT)						
V_{OL}	Output low voltage	I_O = 5 mA			0.5	V
I_{OH}	Output high leakage current	V_O = 3.3 V			1	µA
SDATOUT OUTPUT (PUSH-PULL OUTPUT)						
V_{OL}	Output low voltage	I_O = 5 mA			0.5	V
V_{OH}	Output high voltage	I_O = 100 µA, V_M = 11 V - 60 V, peak			6.5	V
		I_O = 100 µA, V_M = 11 V - 60 V, steady state	3.3	4.5	5.6	
		I_O = 100 µA, V_M = 8.2 V - 11 V, steady state	2.5			
I_{SRC}	Output source current	V_M = 24 V			1	mA
I_{SNK}	Output sink current	V_M = 24 V			5	mA
LOW-SIDE FETS						
$R_{DS(ON)}$	FET on resistance , HTSSOP and SOIC package	V_M = 24 V, I_O = 700 mA, T_J = 25°C		0.5		Ω
		V_M = 24 V, I_O = 700 mA, T_J = 85°C		0.75	0.8	
	FET on resistance, SOT-23-THN package	V_M = 24 V, I_O = 700 mA, T_J = 25°C		0.4		Ω
		V_M = 24 V, I_O = 700 mA, T_J = 85°C			0.64	
I_{OFF}	Off-state leakage current		–50		50	µA
HIGH-SIDE DIODES						
V_F	Diode forward voltage	V_M = 24 V, I_O = 700 mA, T_J = 25°C		1.2		V
I_{OFF}	Off-state leakage current	V_M = 24 V, T_J = 25°C	–50		50	µA
OUTPUTS						
t_R	Rise time	V_M = 24 V, I_O = 700 mA, Resistive load	50		300	ns
t_F	Fall time	V_M = 24 V, I_O = 700 mA, Resistive load	50		300	ns
PROTECTION CIRCUITS						
I_{OCP}	Overcurrent protection trip level		2.3		3.8	A
t_{OCP}	Overcurrent protection deglitch time			3.5		µs
t_{RETRY}	Overcurrent protection retry time			1.2		ms
t_{TSD}	Thermal shutdown temperature	Die temperature(1)	150	160	180	°C

(1) Not production tested.

6.5 Thermal Information

THERMAL METRIC(1)		DRV8804			UNIT
		DW (SOIC)	PWP (HTSSOP)	DYZ (SOT -23 THN)	
		20 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	67.7	39.6	53.2	°C/W

THERMAL METRIC(1)		DRV8804			UNIT
		DW (SOIC)	PWP (HTSSOP)	DYZ (SOT -23 THN)	
		20 PINS	16 PINS	16 PINS	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32.9	24.6	76.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	35.4	20.3	22.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.2	0.7	8.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	34.9	20.1	22.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	2.3	9.6	°C/W

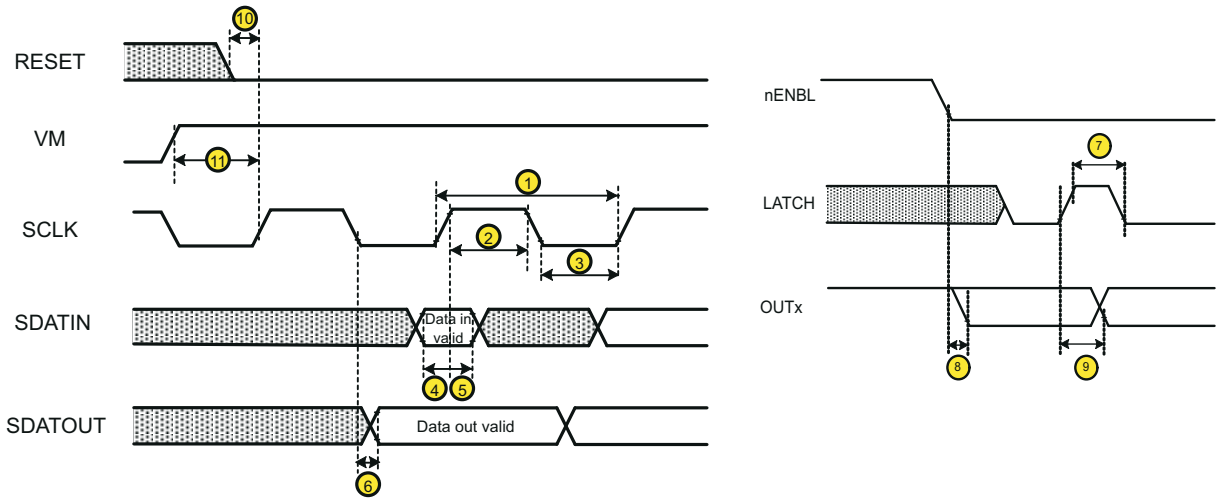
(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.6 Timing Requirements

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	NOM	MAX	UNIT
1	t_{CYC}	Clock cycle time	62			ns
2	t_{CLKH}	Clock high time	25			ns
3	t_{CLKL}	Clock low time	25			ns
4	$t_{SU(SDATIN)}$	Setup time, SDATIN to SCLK	5			ns
5	$t_{H(SDATIN)}$	Hold time, SDATIN to SCLK	1			ns
6	$t_{D(SDATOUT)}$	Delay time, SCLK to SDATOUT, no external pullup resistor, C_{OUT} = 100 pF		50	100	ns
7	$t_{W(LATCH)}$	Pulse width, LATCH	200			ns
8	$t_{OE(ENABLE)}$	Enable time, nENBL to output low		60		ns
9	$t_{D(LATCH)}$	Delay time, LATCH to output change		200		ns
—	t_{RESET}	RESET pulse width	20			µs
10	$t_{D(RESET)}$	Reset delay before clock	20			µs
11	$t_{STARTUP}$	Start-up delay VM applied before clock	55			µs

(1) Not production tested.



More than 400 ns of delay should exist between the final SCLK rising edge and the LATCH rising edge. This ensures that the last data bit is shifted into the device properly.

図 6-1. DRV8804 Timing Requirements

6.7 Typical Characteristics

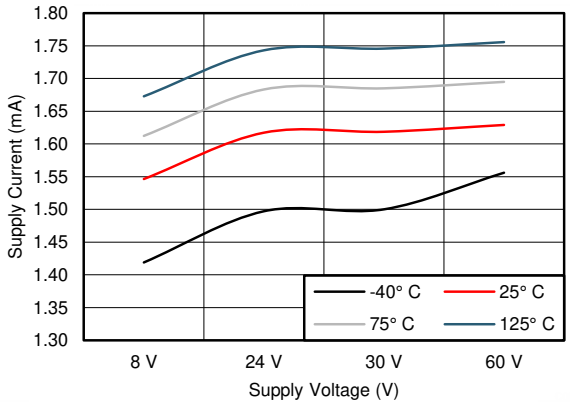


図 6-2. Supply Current over V_M

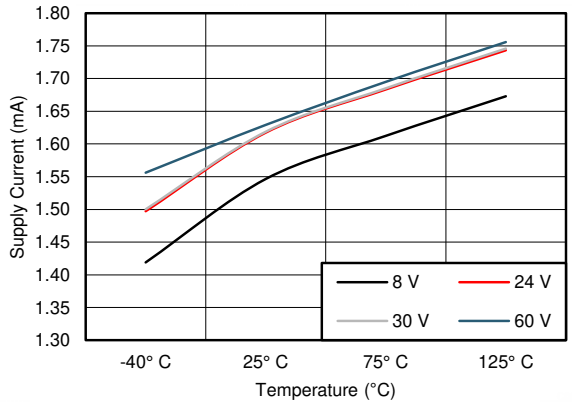


図 6-3. Supply Current Over Temperature

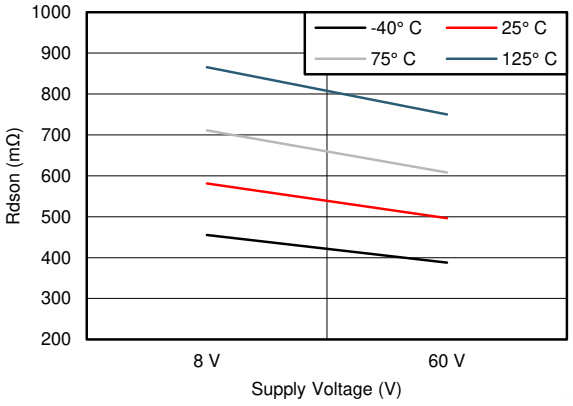


図 6-4. $R_{DS(on)}$ Over VM

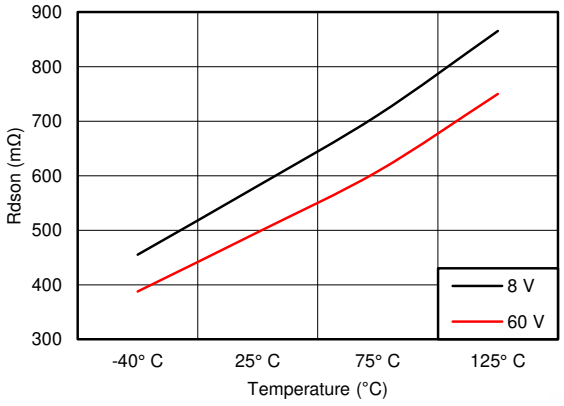


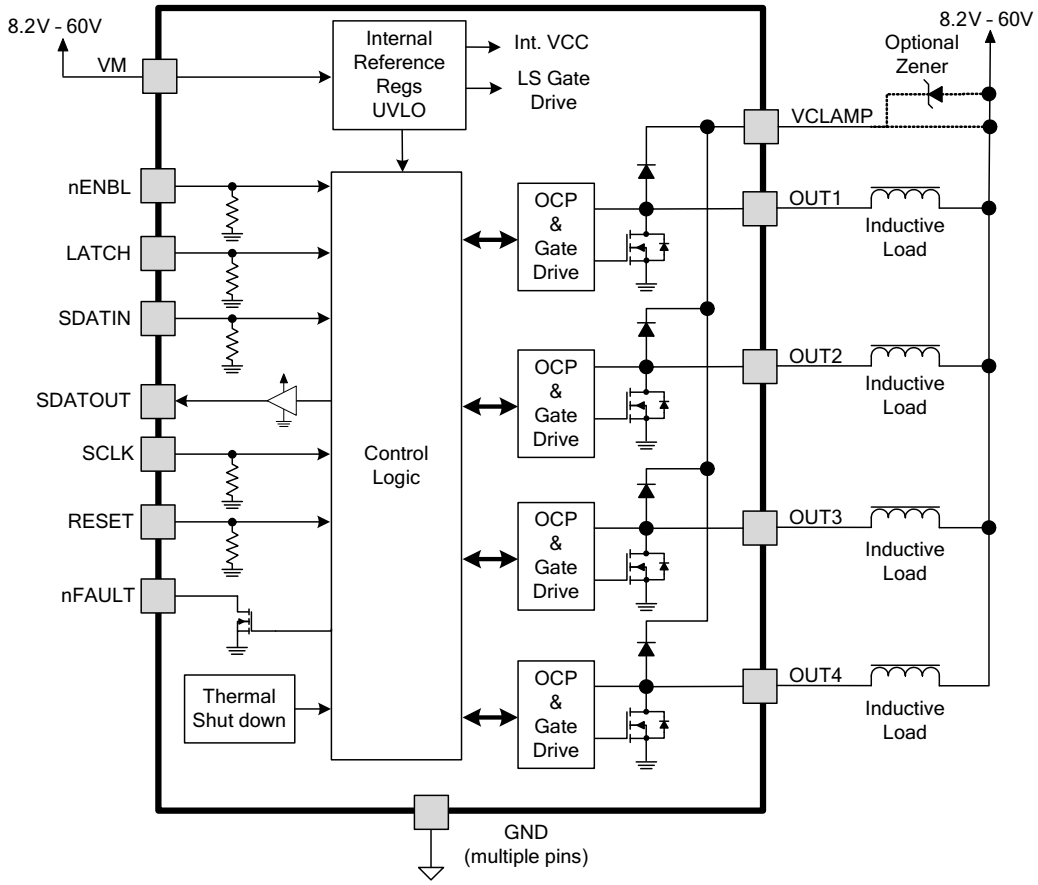
図 6-5. $R_{DS(on)}$ Over Temperature

7 Detailed Description

7.1 Overview

The DRV8804 is an integrated 4-channel low side driver solution for a low side switch application. A serial interface controls the low-side driver outputs and allows for multiple drivers to be chained together and save space on communication lines. The four low-side driver outputs consist of four N-channel MOSFETs that have a typical $R_{DS(on)}$ of 500 mΩ (PWP and DW package) and 400 mΩ (DYZ Package). A single motor supply input V_M serves as device power and is internally regulated to power the low side gate drive. The device outputs can be disabled by bringing nENBL pin logic high. This device has several safety features including integrated overcurrent protection that limits the motor current to a fixed maximum above which the device will shut down. Thermal shutdown protection enables the device to automatically shut down if the die temperature exceeds a TTSD limit and will restart once the die reaches a safe temperature. UVLO protection will disable all circuitry in the device if V_M drops below the undervoltage lockout threshold.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Output Drivers

The DRV8804 contains four protected low-side drivers. Each output has an integrated clamp diode connected to a common pin, VCLAMP.

VCLAMP can be connected to the main power supply voltage, VM. It can also be connected to a Zener or TVS diode to V_M, allowing the switch voltage to exceed the main supply voltage V_M. This connection can be beneficial when driving loads that require very fast current decay, such as unipolar stepper motors.

In all cases, the voltage on the outputs must not be allowed to exceed the maximum output voltage specification.

7.3.2 Serial Interface Operation

The DRV8804 is controlled with a simple serial interface. Logically, the interface is shown in 図 7-1.

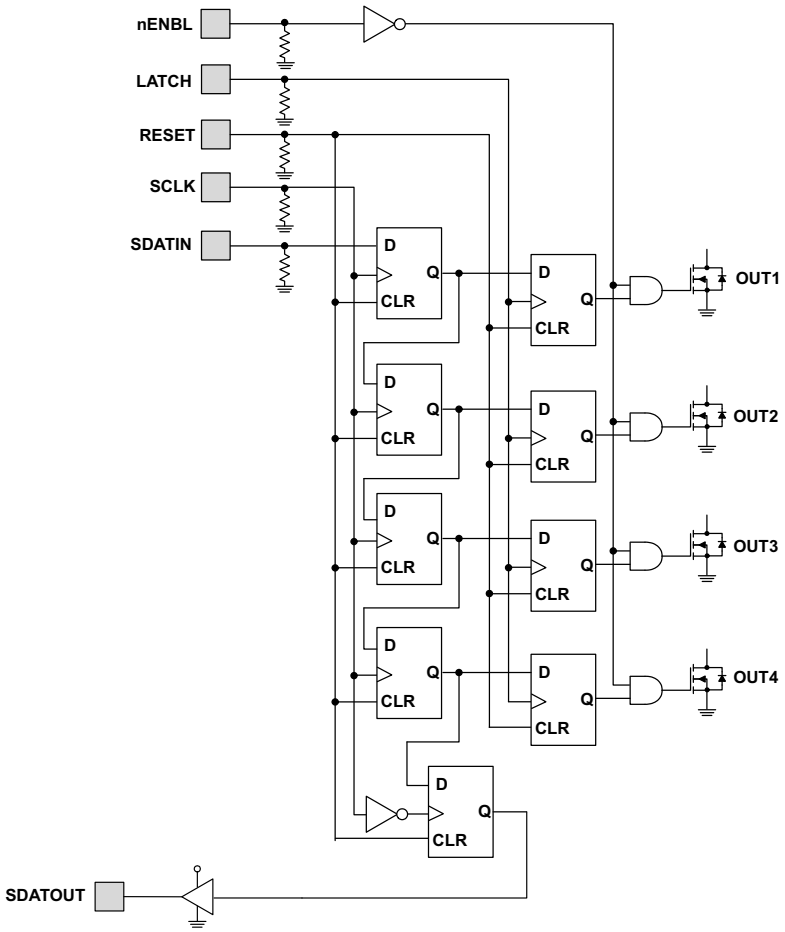


図 7-1. Serial Interface Operation

Data is shifted into a temporary holding shift register in the part using the SDATIN pin, one bit at each rising edge of the SCLK pin. Data is simultaneously shifted out of the SDATOUT pin, allowing multiple devices to be daisy-chained onto one serial port. Note that the SDATOUT pin has a push-pull driver, which can support driving another DRV8804 SDATIN pin at clock frequencies of up to 1 MHz without an external pullup. A pullup resistor can be used between SDATOUT and an external 5-V logic supply to support higher clock frequencies. TI recommends a resistor value greater than 1 kΩ. The SDATOUT pin is capable of approximately 1-mA source and 5-mA sink. To supply logic signals to a lower-voltage microcontroller, use a resistor divider from SDATOUT to GND.

A rising edge on the LATCH pin latches the data from the temporary shift register into the output stage.

Daisy Chain Operation

The following Figure shows how two DRV81646 devices can be connected in daisy chain to leverage GPIO/ isolation saving. SDO pin of one device is fed to the SDI pin of the following device in the chain

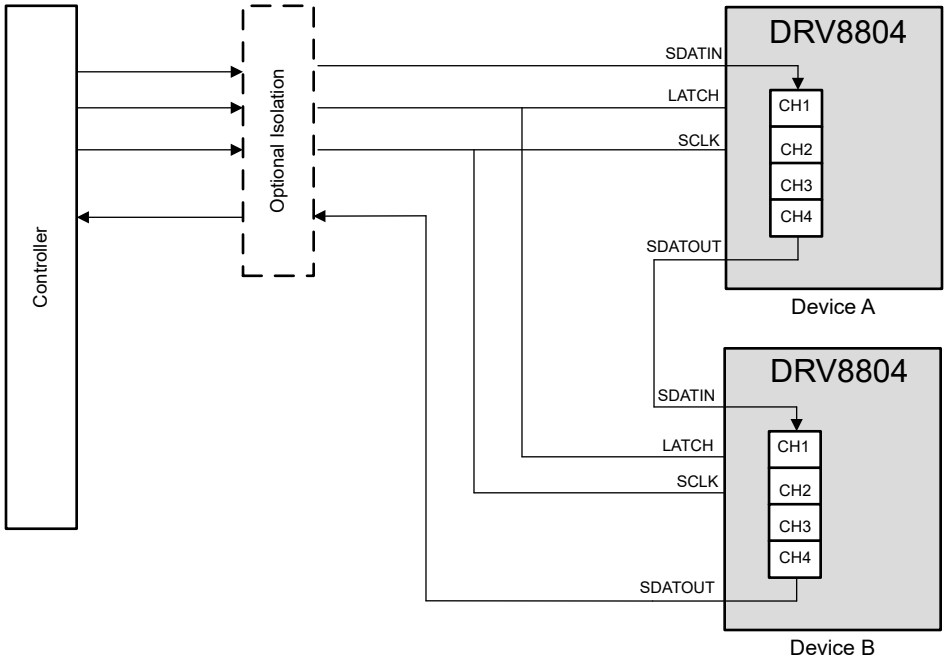


図 7-2. Two DRV8804 devices in Daisy chain

To write to two devices , 8 bits of data need to be written as shown in Figure . Note SDO is sent out on Negedge of SCLK. SDO is ready to be sampled on following posedge of SCLK. The value on SDI pin is also sampled on posedge of SCLK. Note Latch need not be brought low to initiate a shift in of data. A posedge of Latch is needed to Latch the data shifted in to Outputs.

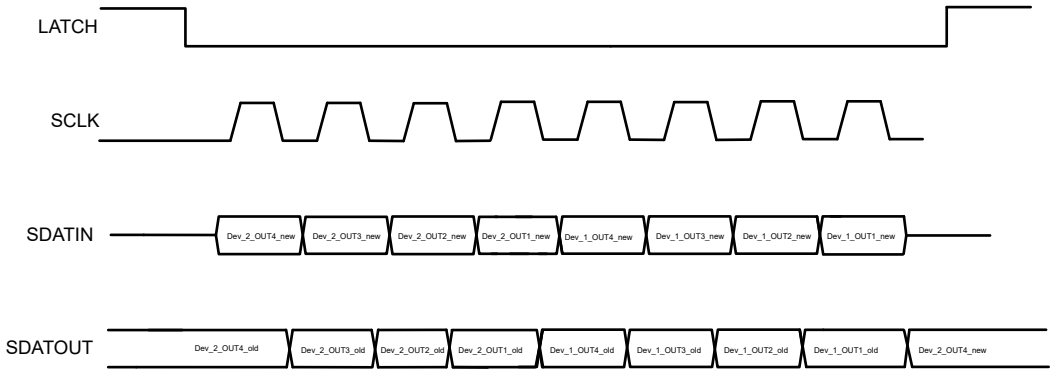


図 7-3. 8-bit packet for communication with two daisy chained devices

7.3.3 nENBL and RESET Operation

The nENBL pin enables or disables the output drivers. nENBL must be low to enable the outputs. nENBL does not affect the operation of the serial interface logic. Note that nENBL has an internal pulldown.

The RESET pin, when driven active high, resets internal logic, including the OCP fault. All serial interface registers are cleared. Note that RESET has an internal pulldown. An internal power-up reset is also provided, so driving RESET at power up is not required.

7.3.4 Protection Circuits

The DRV8804 is fully protected against undervoltage, overcurrent, and overtemperature events.

7.3.4.1 Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than the t_{OCP} deglitch time (approximately 3.5 µs), the driver will be disabled and the nFAULT pin will be driven low. The driver will remain disabled for the t_{RETRY} retry time (approximately 1.2 ms), then the fault will be automatically cleared. The fault will be cleared immediately if either RESET pin is activated or VM is removed and re-applied.

7.3.4.2 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all output FETs will be disabled and the nFAULT pin will be driven low. Once the die temperature has fallen to a safe level, operation will automatically resume.

7.3.4.3 Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pin falls below the undervoltage lockout (UVLO) threshold voltage, all circuitry in the device will be disabled, and internal logic will be reset. Operation will resume when V_M rises above the UVLO threshold.

7.4 Device Functional Modes

When the nENBL pin of the DRV8804 is pulled logic low, the open-drain FET outputs are enabled. Having the device be enabled at logic low allows for the use of long data lines in a high noise environment that do not unintentionally enable the device with coupled noise. The device will still shift data through the SDATIN / SDATOUT lines and SCLK line regardless of the state of the nENBL pin.

Once data has been moved into each of the four shift register lines the LATCH pin can be pulled high to output the state of the four shift registers. Once LATCH is pulled high the state of the four shift registers is placed in a logical AND with the inverse state of the nENBL pin. If the nENBL pin is logic low input and the LATCH pin is logic high the open-drain output of that driver channel will be turned on.

If the device detects that V_M has dropped below the UVLO threshold, it will immediately enter a state where all the internal logic is disabled. The device stays in a disabled state until V_M rises above the UVLO threshold and all internal logic is then reset. During an Overcurrent Protection (OCP) event the device removes gate drive for one t_{RETRY} interval and the nFAULT pin is driven low. The fault is cleared immediately if RESET is activated or V_M is removed and re-applied.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8804 device can be used to drive upto four unipolar loads such as unipolar BDCs, solenoids such as valves, relays etc.

8.2 Typical Application

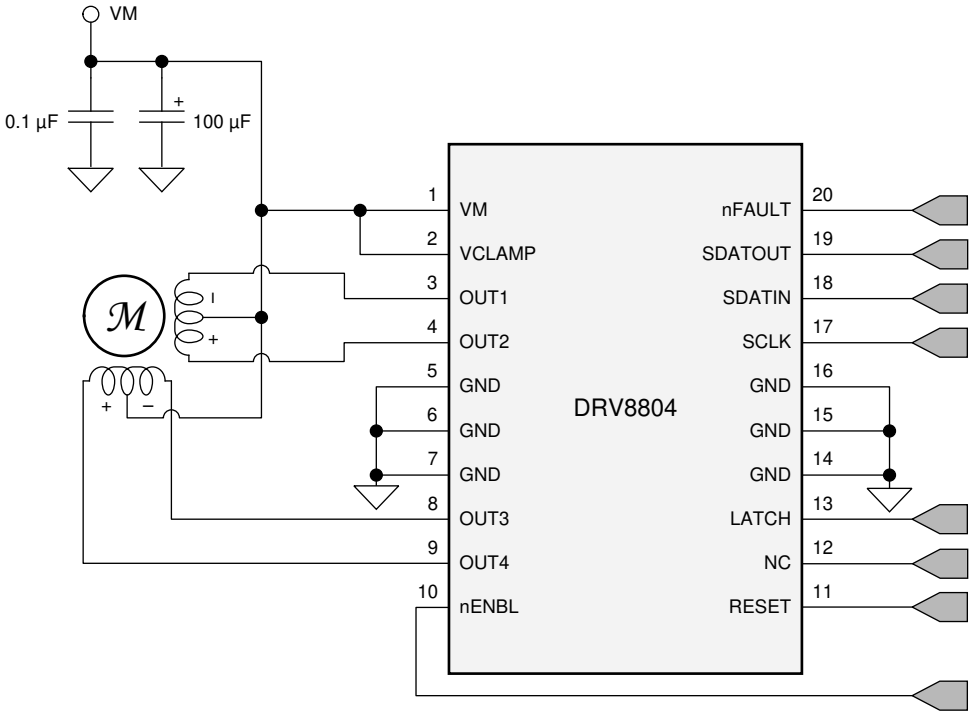


図 8-1. Typical Application Schematic

8.2.1 Design Requirements

表 8-1 lists the design parameters for this design example.

表 8-1. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply Voltage	V_M	24 V
Motor Winding Resistance	R_L	7.4 Ω/phase
Motor Full Step Angle	θ_{step}	1.8°/step
Motor Rated Current	I_{RATED}	0.75 A

8.2.2 Detailed Design Procedure

8.2.2.1 Motor Voltage

The motor voltage to use will depend on the ratings of the motor selected and the desired torque. A higher voltage shortens the current rise time in the coils of the stepper motor allowing the motor to produce a greater average torque. Using a higher voltage also allows the motor to operate at a faster speed than a lower voltage.

8.2.2.2 Drive Current

The current path starts from the supply V_M, moves through the inductive winding load and low-side sinking NMOS power FET. Power dissipation losses in one sink NMOS power FET are shown in 式 1.

$$P = I^2 \times R_{DS\ (on)} \quad (1)$$

The DRV8804 device has been measured to be capable of 1.5-A Single Channel or 800-mA Four Channels with the DW package , 2-A Single Channel or 1-A Four Channels with the PWP and 1.9-A Single Channel or 0.9-A Four Channels with the DYZ package at 25°C on standard FR-4 PCBs. The maximum RMS current varies based on PCB design and the ambient temperature.

8.2.3 Application Curves

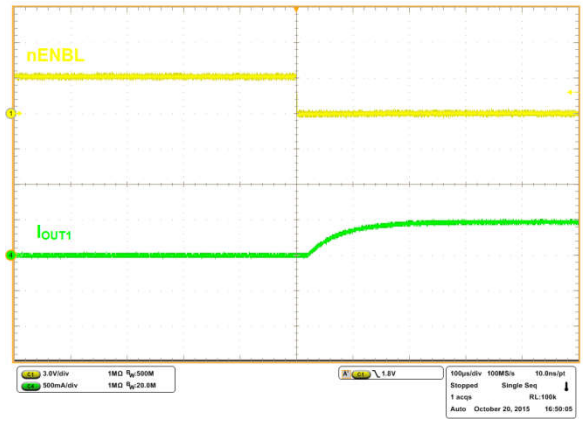


図 8-2. Current Ramp With a 16-Ω, 1-mH, R_L Load and V_M = 8.2 V

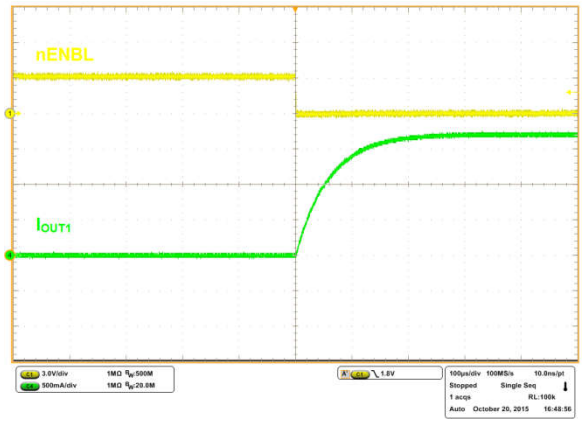


図 8-3. Current Ramp With a 16-Ω, 1-mH R_L Load and V_M = 30 V

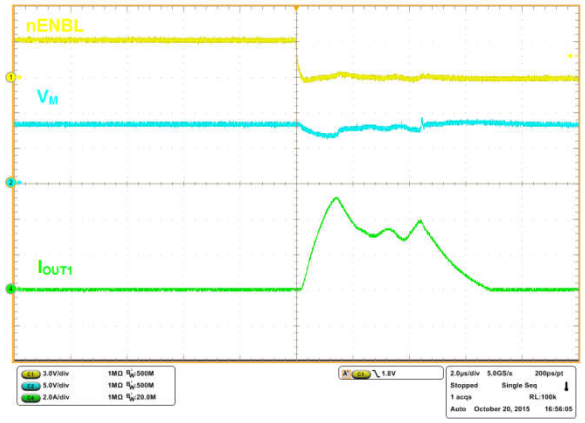


図 8-4. OCP With V_M = 8.2 V and OUT1 Shorted to V_M

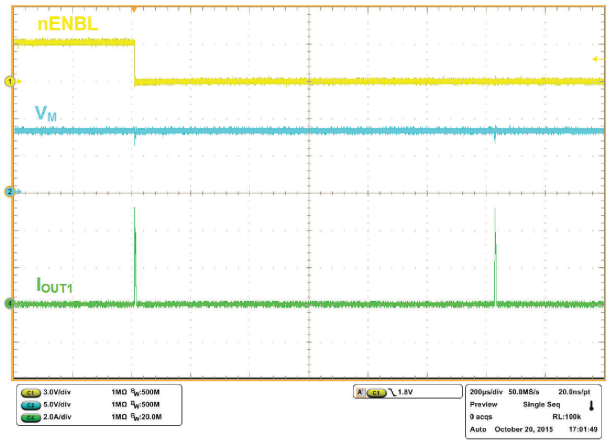


図 8-5. OCP Separated by t_{RETRY} With V_M = 8.2 V and OUT1 Shorted to V_M

Power Supply Recommendations

8.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system.
- The power supply's capacitance and ability to source current.
- The amount of parasitic inductance between the power supply and motor system.
- The acceptable voltage ripple.
- The type of motor used (Brushed DC, Brushless DC, Stepper).
- The type of motor used (Brushed DC, Brushless DC, Stepper).

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

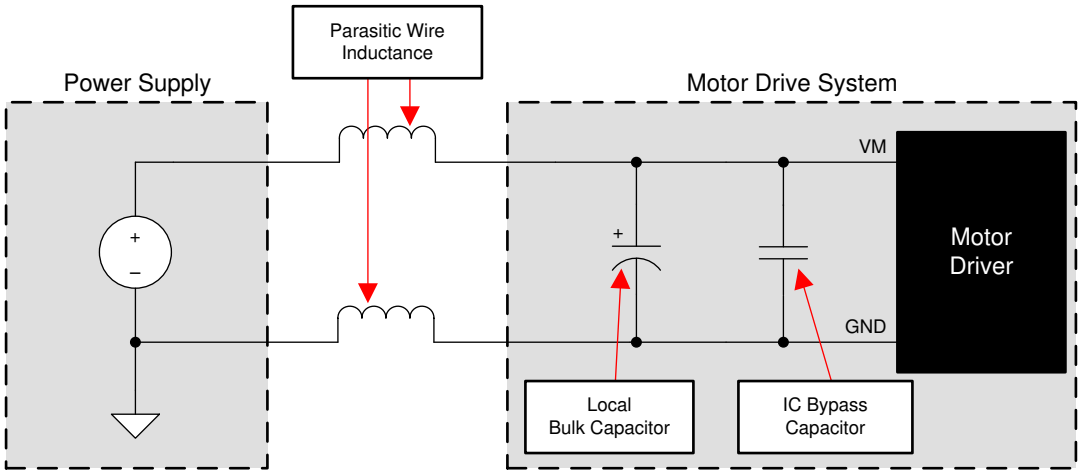


図 8-6. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

8.3 Layout

8.3.1 Layout Guidelines

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

- Small-value capacitors should be ceramic, and placed closely to device pins.
- The high-current device outputs should use wide metal traces.

The device thermal pad should be soldered to the PCB top-layer ground plane. Multiple vias should be used to connect to a large bottom-layer ground plane. The use of large metal planes and multiple vias help dissipate the $I^2 \times R_{DS(on)}$ heat that is generated in the device.

8.3.2 Layout Example

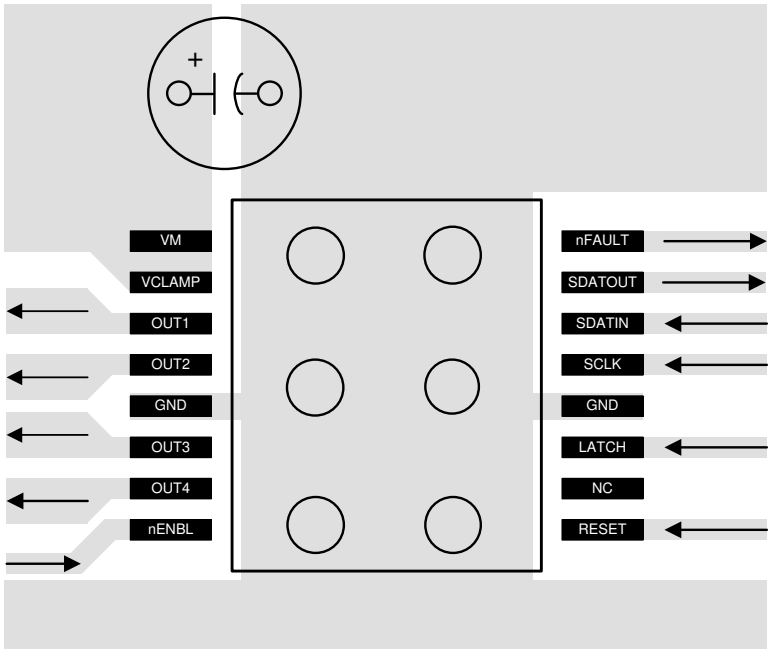


図 8-7. Layout Recommendation

8.3.3 Thermal Considerations

The DRV8804 has thermal shutdown (TSD) as described in *セクション 7.3.4.2*. If the die temperature exceeds approximately 150°C, the device will be disabled until the temperature drops to a safe level.

Any tendency of the device to enter TSD is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

8.3.3.1 Power Dissipation

Power dissipation in the DRV8804 is dominated by the power dissipated in the output FET resistance, or $R_{DS(ON)}$. Average power dissipation of each FET when running a static load can be roughly estimated by 式 2.

$$P = R_{DS(ON)} \bullet (I_{OUT})^2 \tag{2}$$

where

- P is the power dissipation of one FET
- $R_{DS(ON)}$ is the resistance of each FET
- I_{OUT} is equal to the average current drawn by the load

Note that at start-up and fault conditions this current is much higher than normal running current; these peak currents and their duration also must be taken into consideration. When driving more than one load simultaneously, the power in all active output stages must be summed.

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

Note that $R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases. This must be taken into consideration when sizing the heatsink.

8.3.3.2 Heatsinking

The DRV8804DW package uses a standard SOIC outline, but has the center pins internally fused to the die pad to more efficiently remove heat from the device. The two center leads on each side of the package should be connected together to as large a copper area on the PCB as is possible to remove heat from the device. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

In general, the more copper area that can be provided, the more power can be dissipated.

The DRV8804PWP (HTSSOP package) and the DRV8804DYZ (SOT-23-THN package) uses an exposed thermal pad. The exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this can be accomplished by adding a number of vias to connect the thermal pad to the ground plane. On PCBs without internal planes, copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For details about how to design the PCB, see TI Application Report, *PowerPAD Thermally Enhanced Package* (SLMA002), and TI Application Brief, *PowerPAD Made Easy* (SLMA004), available at www.ti.com.

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- *PowerPAD Thermally Enhanced Package*, SLMA002
- *PowerPAD Made Easy*, SLMA004

9.2 Community Resources

9.3 Trademarks

すべての商標は、それぞれの所有者に帰属します。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision F (December 2015) to Revision G (December 2024)	Page
• DRV8804DYZ デバイスをデータシートに追加	1

Changes from Revision E (January 2014) to Revision F (December 2015)	Page
• 「特長」のキャッチ ダイオードをクランプ ダイオードに変更	1
• 「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加。	1

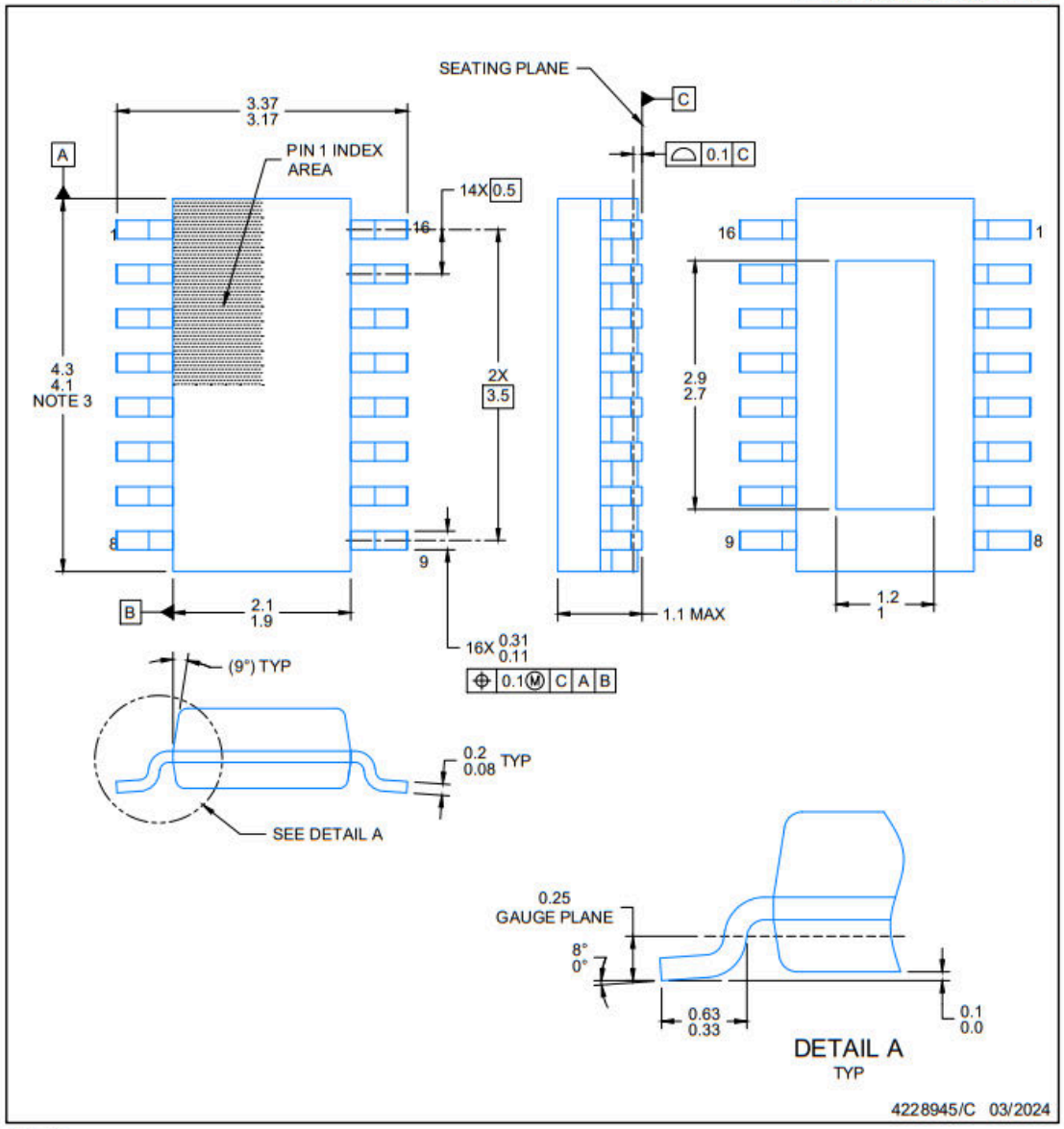
11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

DYZ0016A — SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



NOTES:

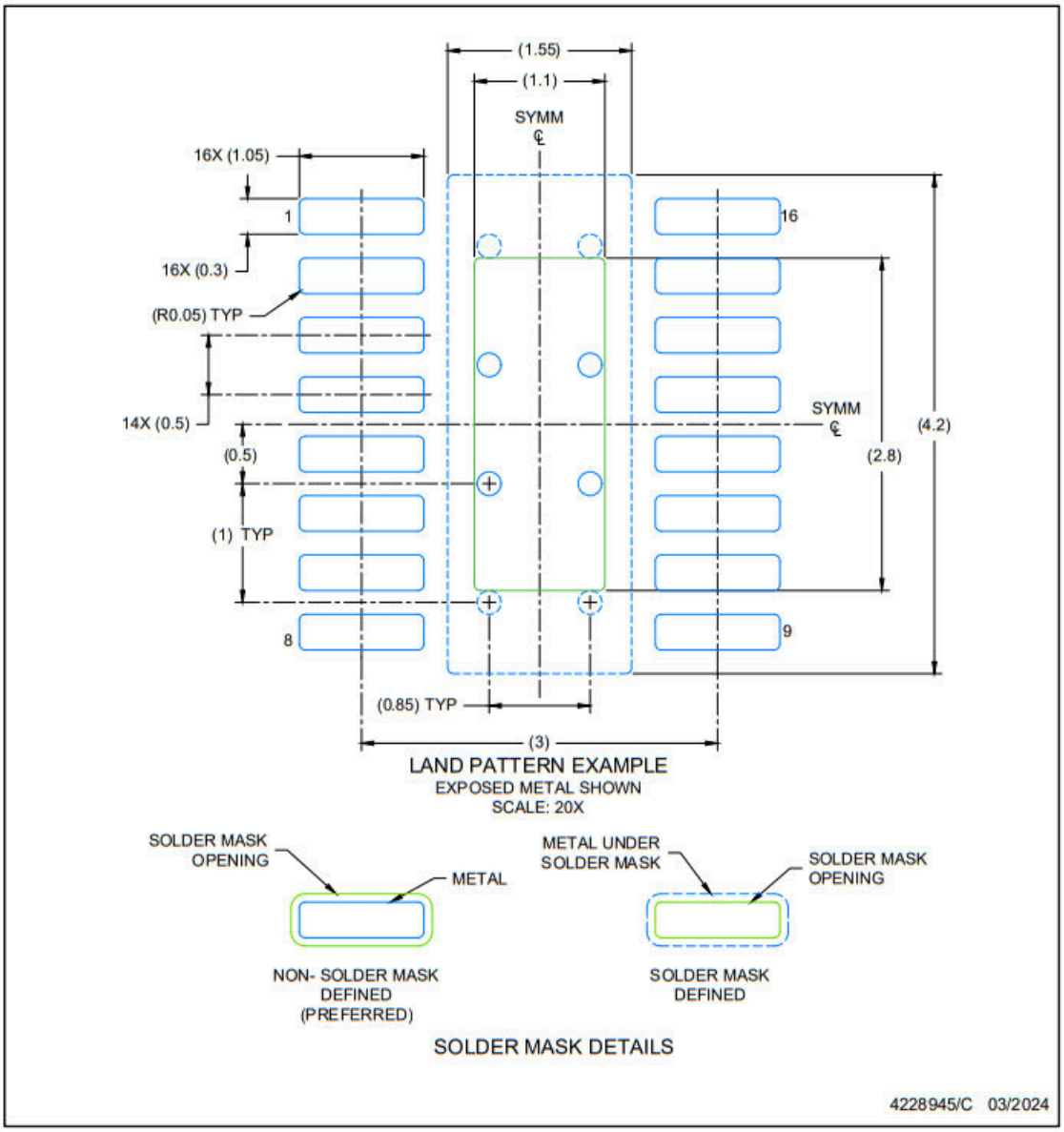
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AA

www.ti.com

EXAMPLE BOARD LAYOUT

DYZ0016A — **SOT-23-THIN - 1.1 mm max height**

PLASTIC SMALL OUTLINE



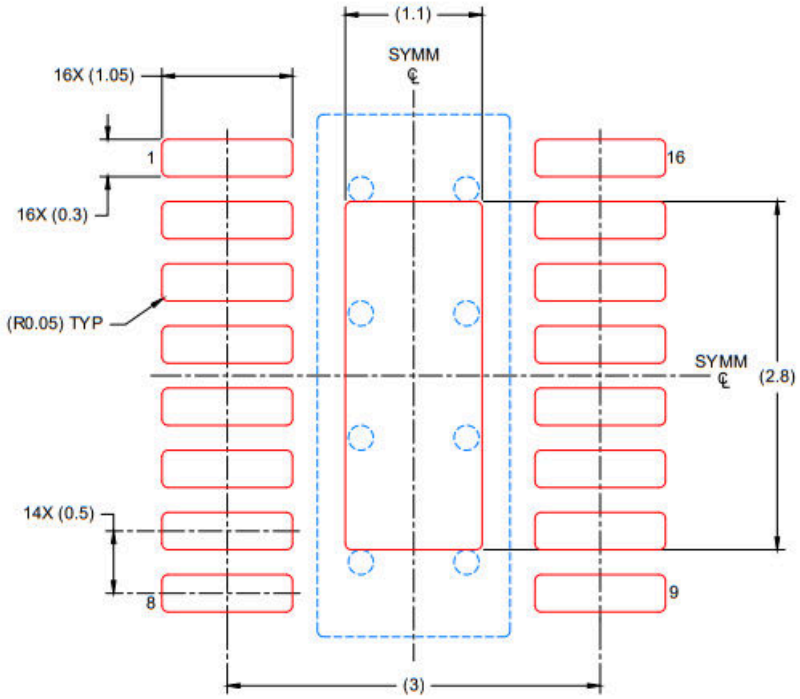
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DYZ0016A — **SOT-23-THIN - 1.1 mm max height**

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.23 X 3.13
0.125	1.10 X 2.80 (SHOWN)
0.15	1.00 X 2.56
0.175	0.93 X 2.37

4228945/C 03/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV8804DW	Obsolete	Production	SOIC (DW) | 20	-	-	Call TI	Call TI	-40 to 125	DRV8804DW
DRV8804DWR	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV8804DW
DRV8804DWR.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV8804DW
DRV8804DYZR	Active	Production	SOT-23-THIN (DYZ) | 16	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	DRV8804
DRV8804PWP	Obsolete	Production	HTSSOP (PWP) | 16	-	-	Call TI	Call TI	-40 to 125	DRV8804
DRV8804PWPR	Active	Production	HTSSOP (PWP) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8804
DRV8804PWPR.A	Active	Production	HTSSOP (PWP) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8804
DRV8804PWPR.B	Active	Production	HTSSOP (PWP) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8804

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

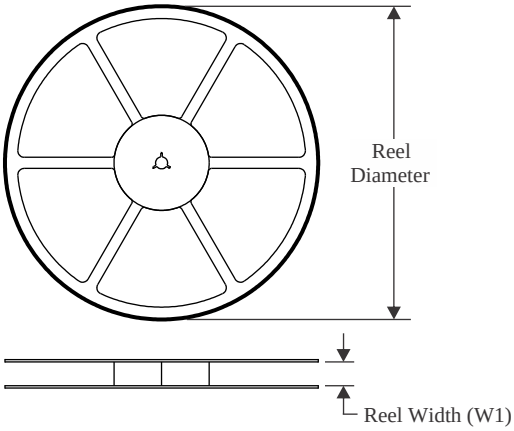
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

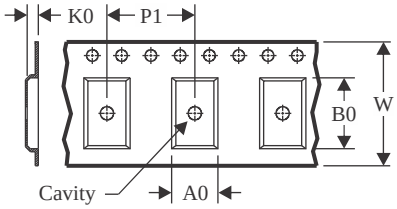
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

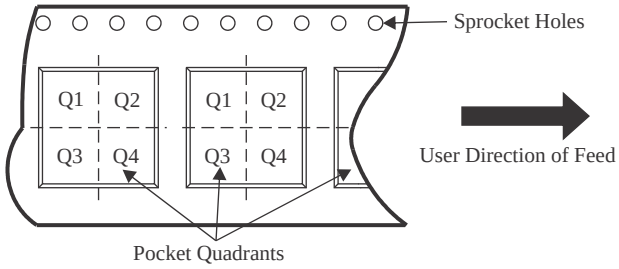


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

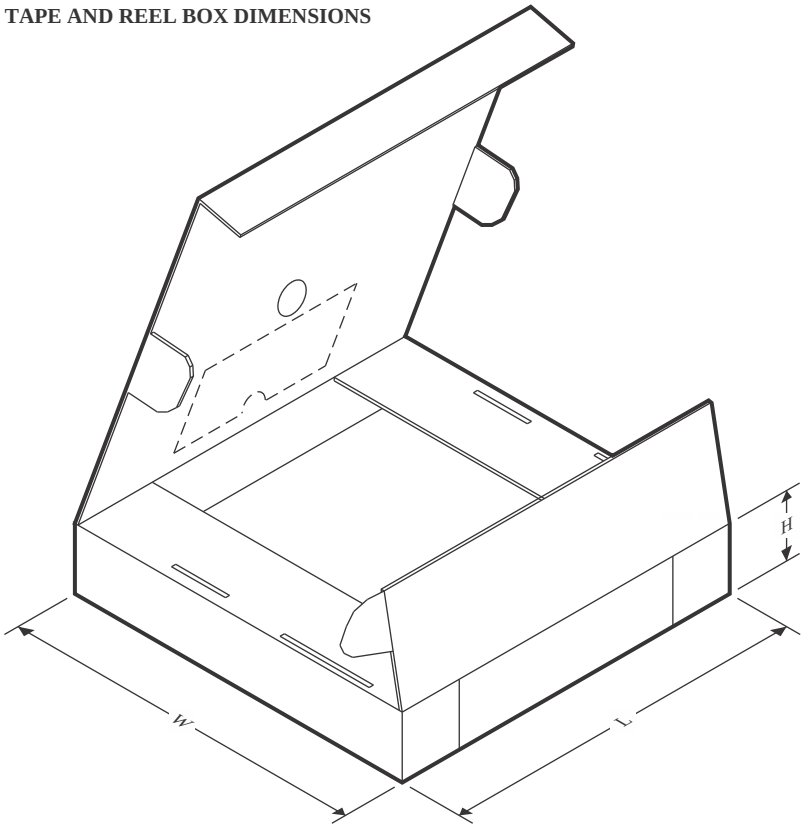
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

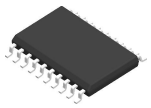
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8804DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
DRV8804DYZR	SOT-23-THIN	DYZ	16	3000	330.0	12.4	4.5	3.56	1.35	8.0	12.0	Q3
DRV8804PWPR	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8804DWR	SOIC	DW	20	2000	356.0	356.0	45.0
DRV8804DYZR	SOT-23-THIN	DYZ	16	3000	360.0	360.0	36.0
DRV8804PWPR	HTSSOP	PWP	16	2000	350.0	350.0	43.0

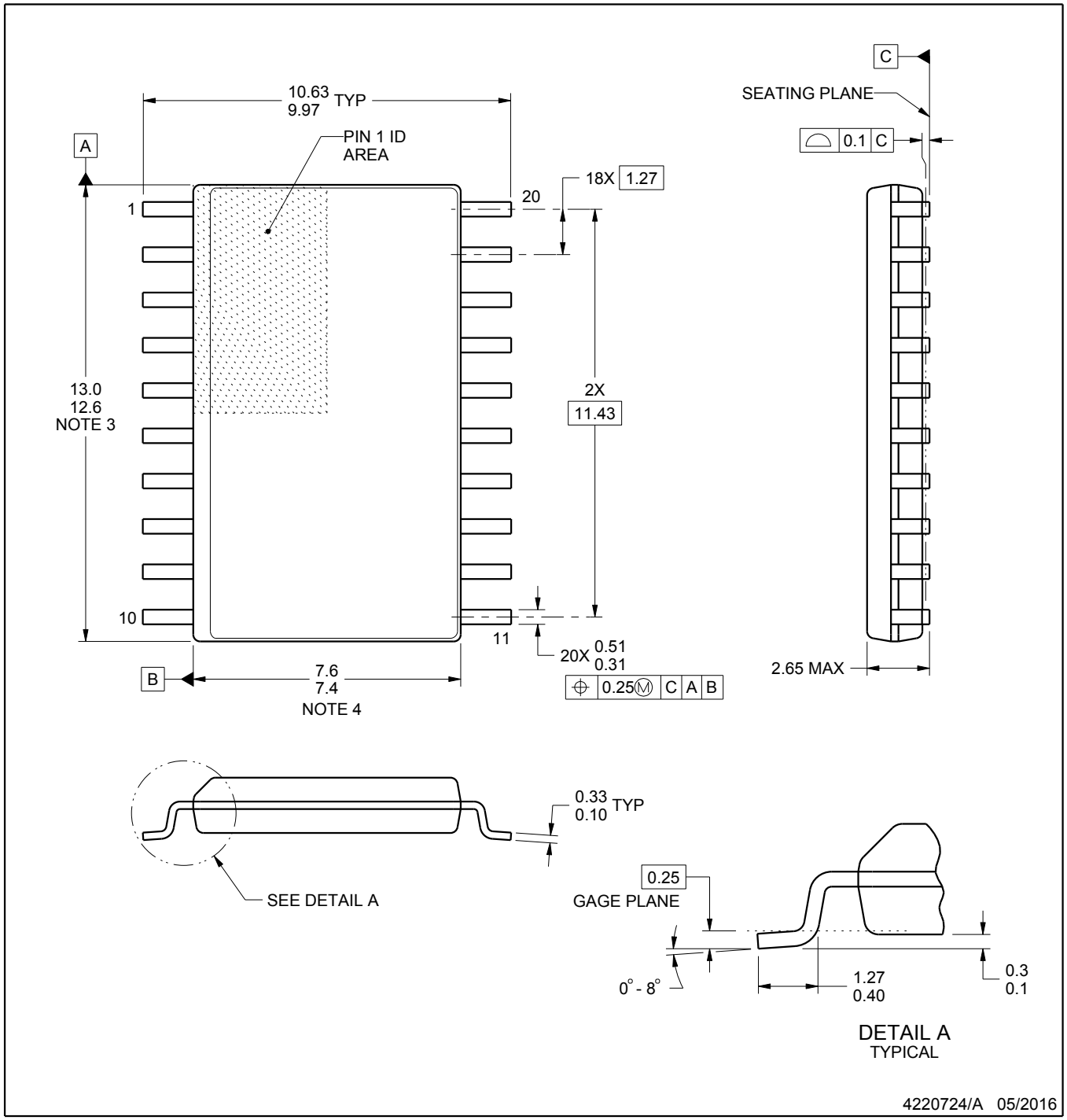


PACKAGE OUTLINE

DW0020A

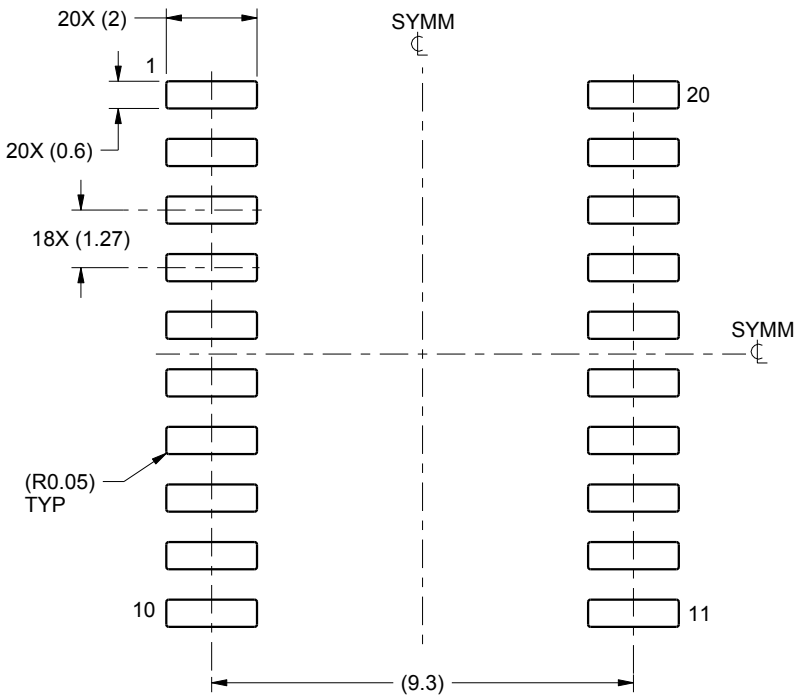
SOIC - 2.65 mm max height

SOIC

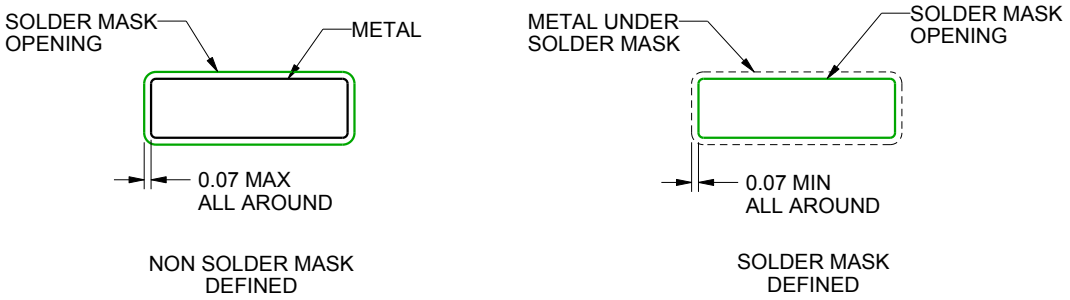


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

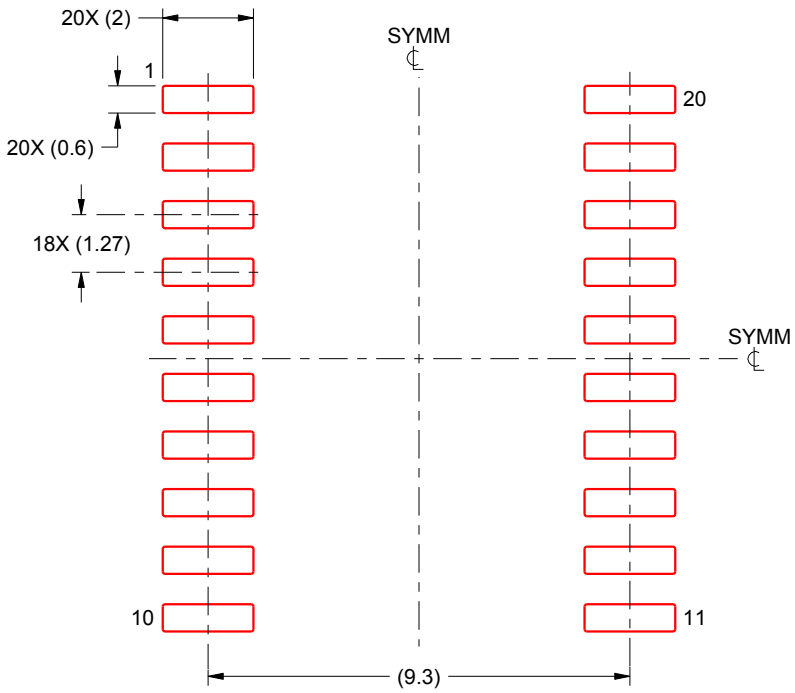


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

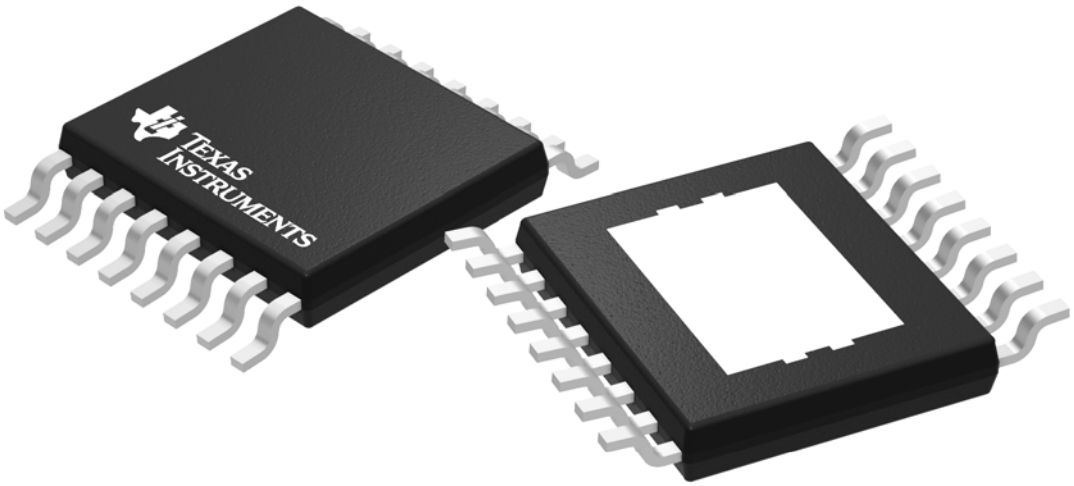
4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PWP 16 PowerPAD™ TSSOP - 1.2 mm max height

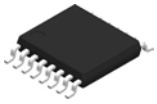
PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

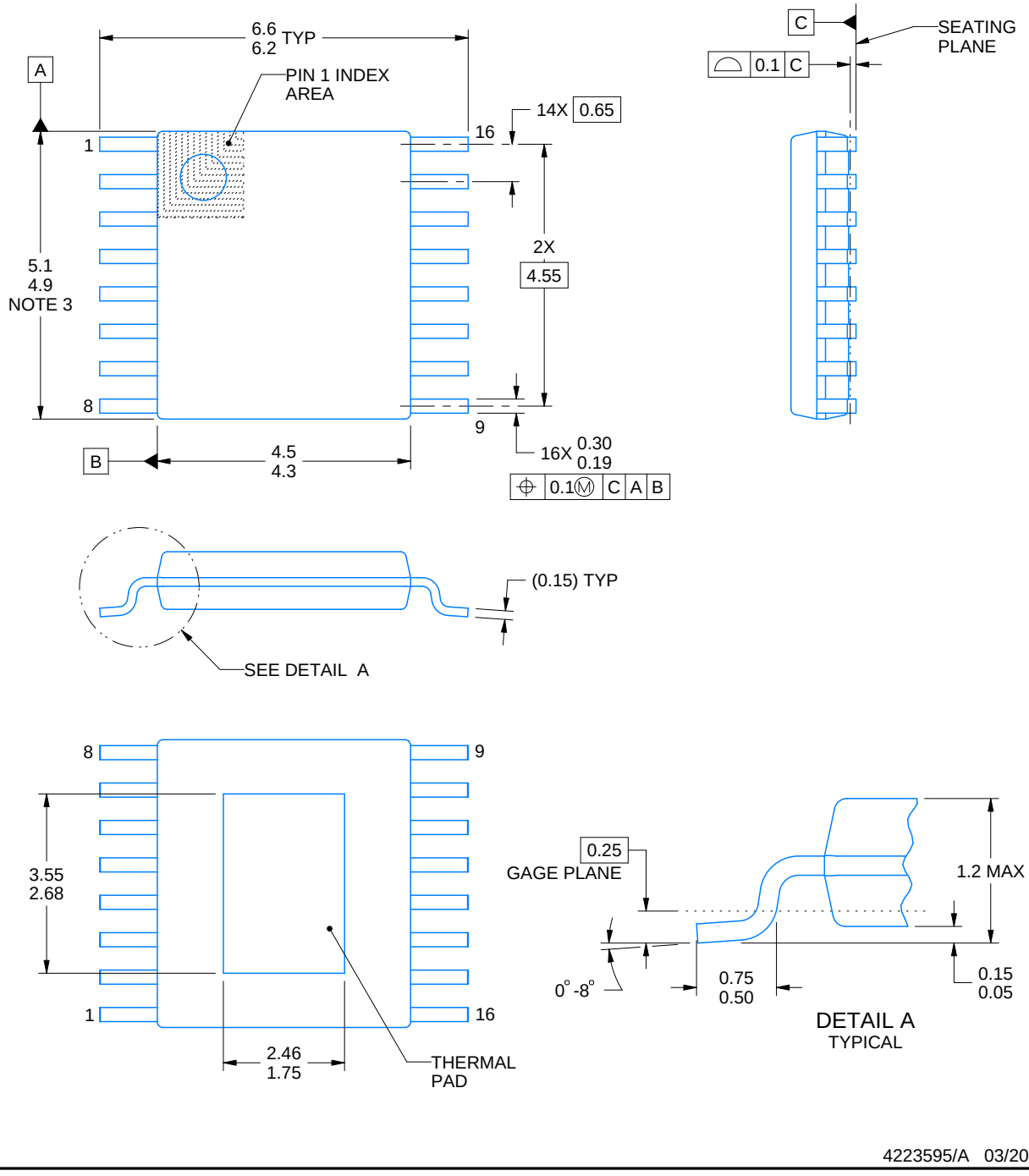
PACKAGE OUTLINE

PWP0016J



PowerPAD™ TSSOP - 1.2 mm max height

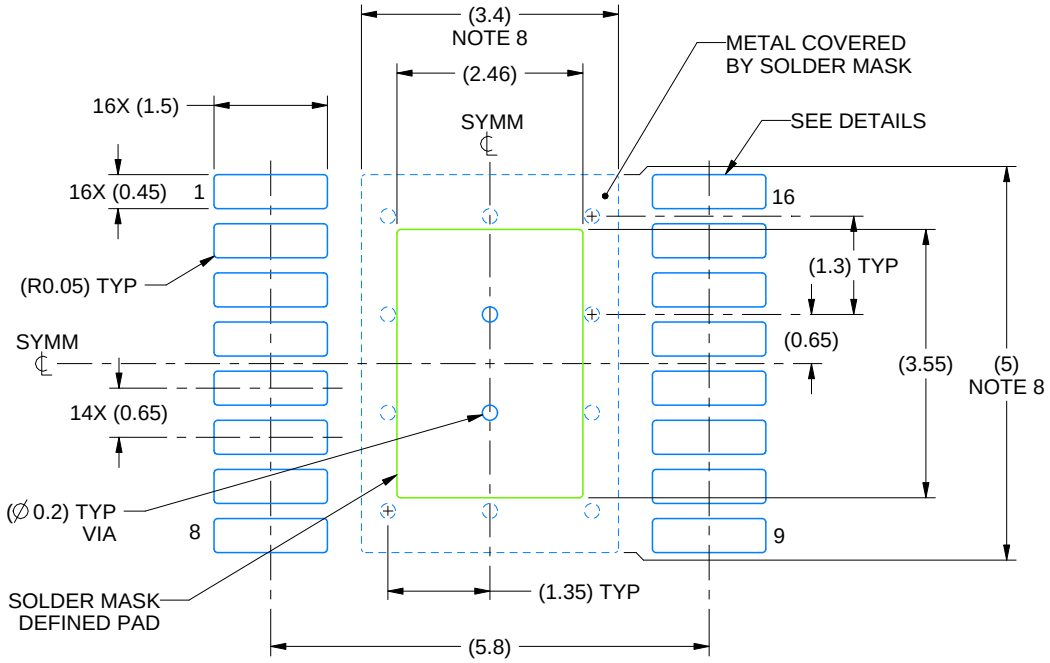
SMALL OUTLINE PACKAGE



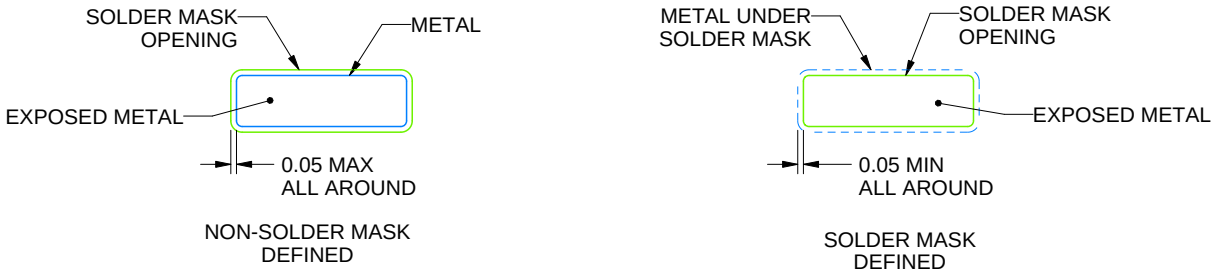
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

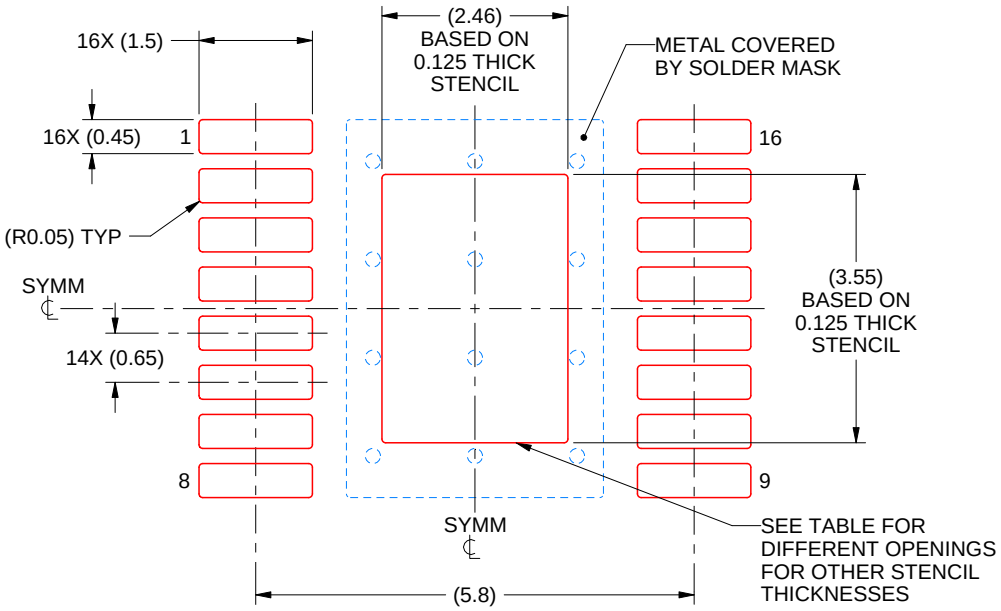


SOLDER MASK DETAILS

4223595/A 03/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
8. Size of metal pad may vary due to creepage requirement.
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.75 X 3.97
0.125	2.46 X 3.55 (SHOWN)
0.15	2.25 X 3.24
0.175	2.08 X 3.00

4223595/A 03/2017

NOTES: (continued)

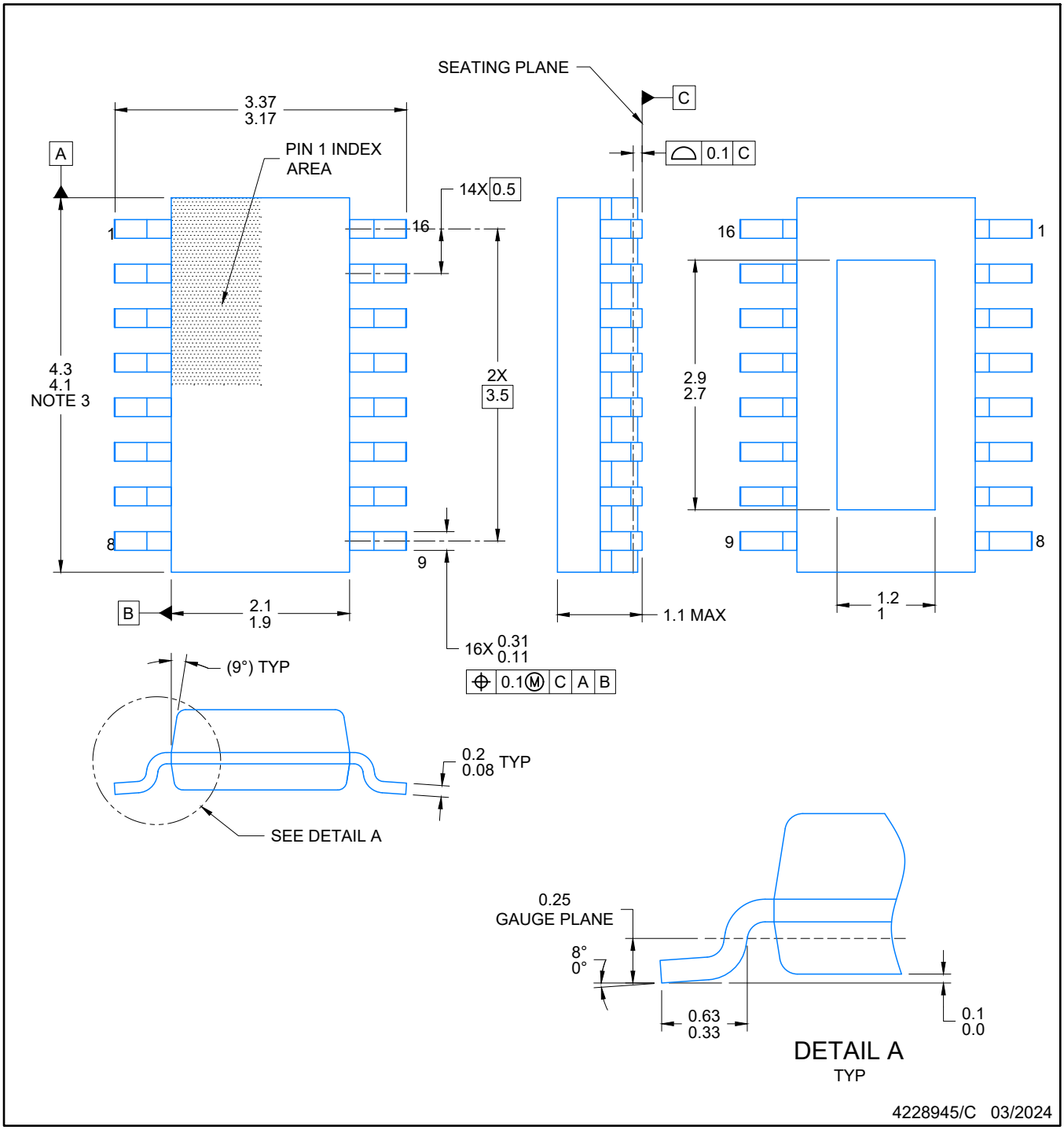
10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DYZ0016A

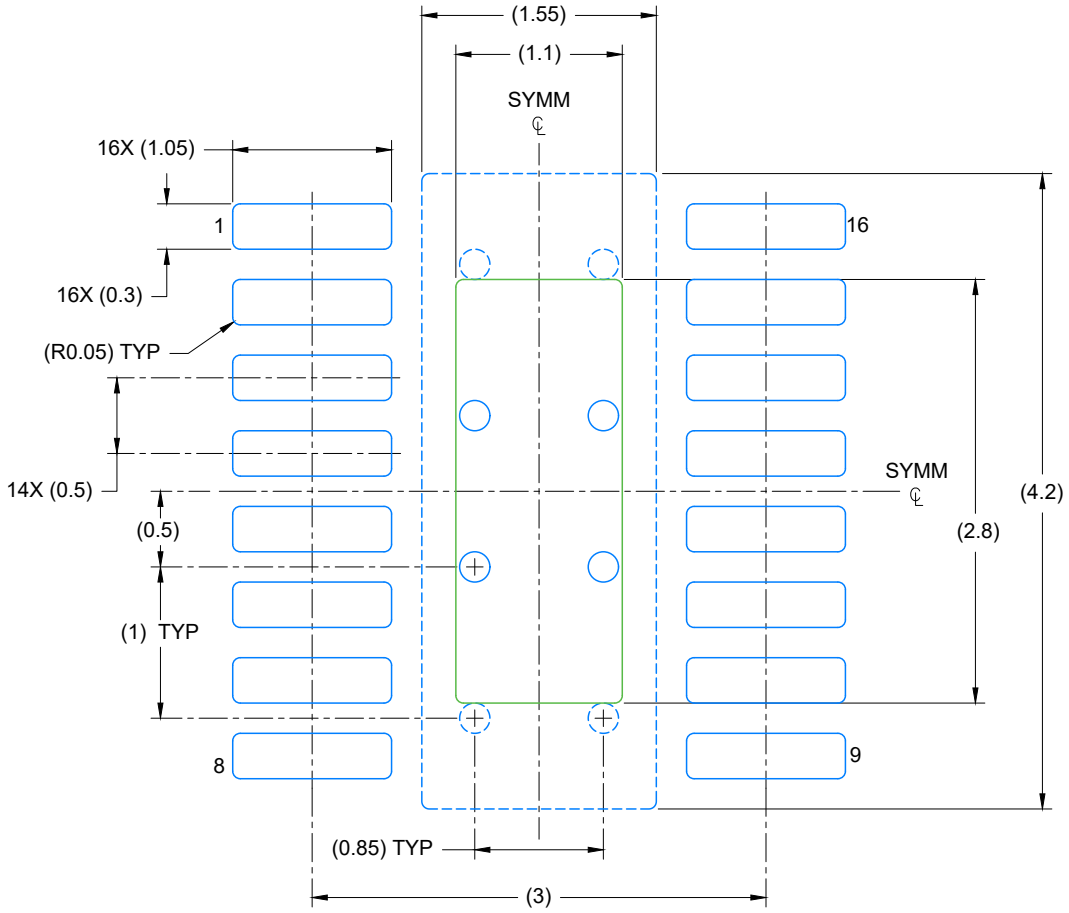
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



NOTES:

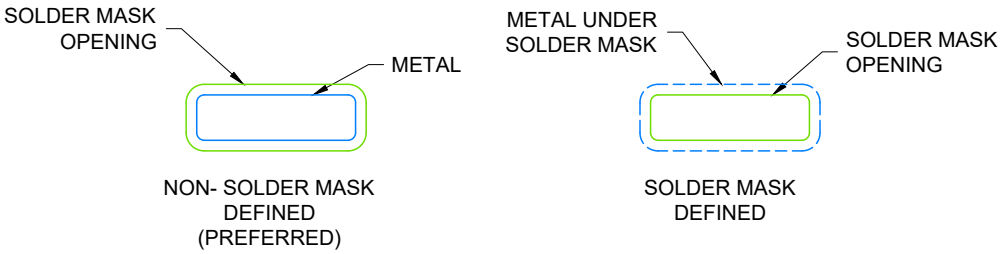
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AA



LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN

SCALE: 20X

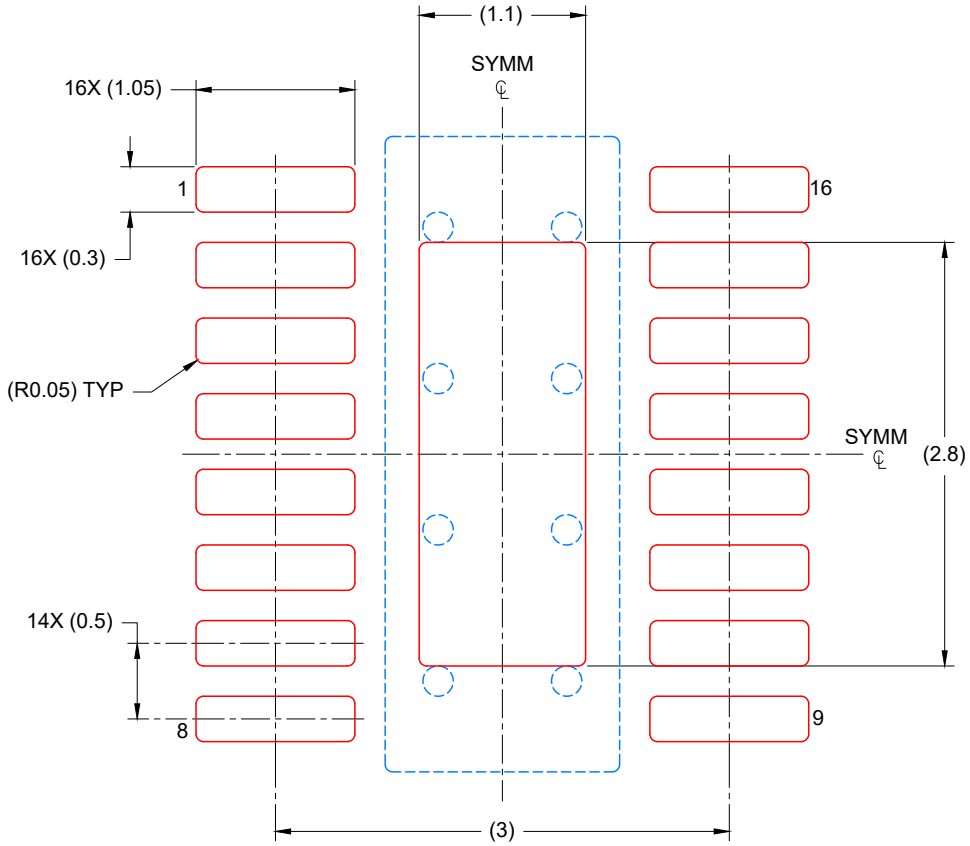


SOLDER MASK DETAILS

4228945/C 03/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.23 X 3.13
0.125	1.10 X 2.80 (SHOWN)
0.15	1.00 X 2.56
0.175	0.93 X 2.37

4228945/C 03/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、 TI の販売条件 、 TI の総合的な品質ガイドライン 、 ti.com または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。 TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

最終更新日：2025 年 10 月