

DRV883x 低電圧 H ブリッジ・ドライバ

1 特長

- H ブリッジ・モータ・ドライバ
 - DC モータまたは他の負荷を駆動
 - Low MOSFET オン抵抗: HS + LS 280mΩ
- 最大 1.8A の駆動電流
- 独立したモータおよびロジック電源ピン:
 - モータ VM: 0~11V
 - ロジック VCC: 1.8~7V
- PWM または PH-EN インターフェイス
 - DRV8837: PWM, IN1, IN2
 - DRV8838: PH および EN
- 低消費電力のスリープ・モード、最大スリープ電流 120nA
 - nSLEEP ピン
- 小型パッケージと小占有面積
 - サーマル・パッド付き 8 ピン WSON
 - 2.0 × 2.0mm
- 保護機能
 - VCC 低電圧誤動作防止 (UVLO)
 - 過電流保護 (OCP)
 - 過熱検出保護 (TSD)

2 アプリケーション

- カメラ
- DSLR レンズ
- コンシューマ製品
- 玩具
- ロボティクス
- 医療機器

3 概要

DRV883x デバイス・ファミリは、カメラ、コンシューマ製品、玩具、その他低電圧またはバッテリー駆動のモーション制御アプリケーションに使用される内蔵モータ・ドライバ・ソリューションです。このデバイスは、1 つの DC モータ、またはソレノイドなど他のデバイスを駆動できます。出力ドライバ・ブロックには、モータ巻線を駆動する H ブリッジとして構成された N チャネルのパワー MOSFET が搭載されています。内部のチャージ・ポンプにより、必要なゲート・ドライブ電圧が生成されます。

DRV883x デバイス・ファミリは、最大 1.8A の出力電流を供給できます。0~11V のモータ電源電圧と、1.8V~7V のデバイス電源電圧で動作します。

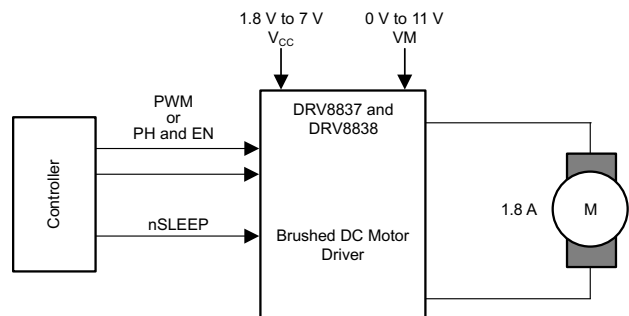
DRV8837 デバイスには PWM (IN1-IN2) 入力インターフェイスがあり、DRV8838 デバイスには PH-EN 入力インターフェイスがあります。どちらのインターフェイスも、業界標準のデバイスと互換性があります。

過電流保護、短絡保護、低電圧誤動作防止、および過熱保護のために、内部シャットダウン機能が用意されています。

デバイス情報⁽¹⁾

部品番号	パッケージ	本体サイズ (公称)
DRV8837	WSON (8)	2.00mm × 2.00mm
DRV8838		

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。



DRV883x の簡略ブロック図



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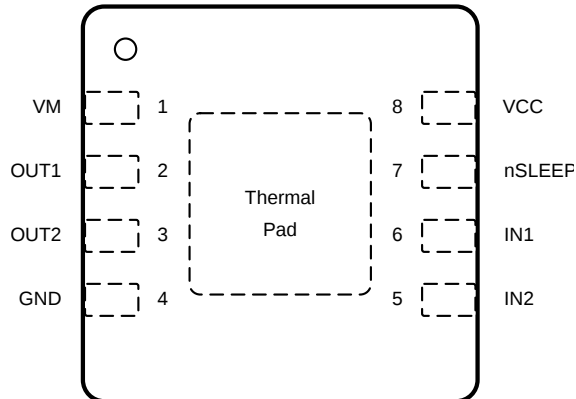
4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

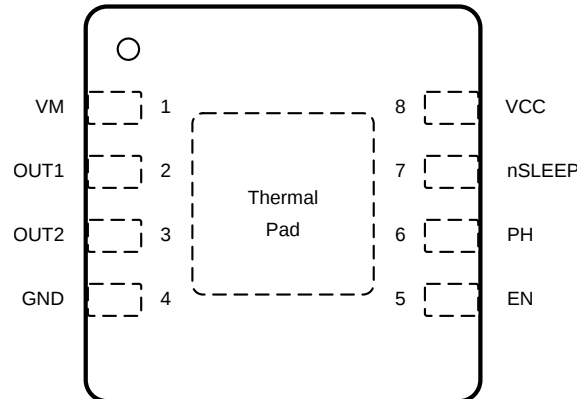
Changes from Revision E (June 2016) to Revision F (April 2021)	Page
• 文書全体にわたって表、図、相互参照の採番方法を更新.....	1
• Added in the <i>Independent Half-Bridge Control</i> section.....	12
Changes from Revision D (December 2015) to Revision E (June 2016)	Page
• Changed the threshold type to the input logic voltage parameters in the <i>Electrical Characteristics</i> table.....	7
• Changed the units for the input logic hysteresis parameter from mV to V in the <i>Electrical Characteristics</i> table.....	7
• Added the <i>Receiving Notification of Documentation Updates</i> section	20
Changes from Revision C (February 2014) to Revision D (December 2015)	Page
• 「概要」セクションの各デバイスの入力インターフェイスを明確化	1
• Added CDM and HBM ESD ratings to the <i>ESD Ratings</i> table	6
Changes from Revision B (December 2013) to Revision C (February 2014)	Page
• DRV8838 のデバイス情報、仕様、タイミング図を追加.....	1
• 「製品情報」表を追加.....	1
• PWM インターフェイスの図を追加.....	1
• Added more information to the Detailed Description and moved information from the Functional Description ...	10
• Added functional block diagram for DRV8838	10
• Added the <i>Application and Implementation</i> section	16
• Added <i>Power Supply Recommendations, Layout, Device and Documentation Support, and Mechanical, Packaging, and Orderable Information</i> sections.....	18

Changes from Revision A (August 2012) to Revision B (December 2013)	Page
• 「特長」セクションを変更.....	1
• Changed Recommended Operating Conditions.....	6
• Changed Electrical Characteristics section.....	7
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5 Pin Configuration and Functions



5-1. DSG Package 8-Pin WSON With Thermal Pad DRV8837 Top View



5-2. DSG Package 8-Pin WSON With Thermal Pad DRV8838 Top View

Pin Functions

NAME	PIN NO.		I/O	DESCRIPTION
	DRV8837	DRV8838		
POWER AND GROUND				
GND	4	4	—	Device ground This pin must be connected to ground.
VCC	8	8	I	Logic power supply Bypass this pin to the GND pin with a 0.1- μ F ceramic capacitor rated for VCC.
VM	1	1	I	Motor power supply Bypass this pin to the GND pin with a 0.1- μ F ceramic capacitor rated for VM.
CONTROL				
EN	—	5	I	ENABLE input
IN1	6	—	I	IN1 input See the セクション7 section for more information.
IN2	5	—	I	IN2 input See the セクション7 section for more information.
PH	—	6	I	PHASE input See the セクション7 section for more information.
nSLEEP	7	7	I	Sleep mode input When this pin is in logic low, the device enters low-power sleep mode. The device operates normally when this pin is logic high. Internal pulldown
OUTPUT				
OUT1	2	2	O	Motor output
OUT2	3	3	O	Connect these pins to the motor winding.

5.1 Dapper Pin Functions

NAME	PIN NO.		I/O	DESCRIPTION
	DRV8837 NO.	DRV8838 NO.		
GND	4	4	—	Device ground This pin must be connected to ground.
VCC	8	8	I	Logic power supply Bypass this pin to the GND pin with a 0.1- μ F ceramic capacitor rated for VCC.

NAME	PIN		I/O	DESCRIPTION
	DRV8837 NO.	DRV8838 NO.		
VM	1	1	I	Motor power supply Bypass this pin to the GND pin with a 0.1- μ F ceramic capacitor rated for VM.
EN	—	5	I	ENABLE input
IN1	6	—	I	IN1 input See the セクション7 section for more information.
IN2	5	—	I	IN2 input See the セクション7 section for more information.
PH	—	6	I	PHASE input See the セクション7 section for more information.
nSLEEP	7	7	I	Sleep mode input When this pin is in logic low, the device enters low-power sleep mode. The device operates normally when this pin is logic high. Internal pulldown
OUT1	2	2	O	Motor output Connect these pins to the motor winding.
OUT2	3	3	O	

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)^{(1) (2)}

		MIN	MAX	UNIT
Motor power-supply voltage	VM	-0.3	12	V
Logic power-supply voltage	VCC	-0.3	7	V
Control pin voltage	IN1, IN2, PH, EN, nSLEEP	-0.5	7	V
Peak drive current	OUT1, OUT2	Internally limited		A
Operating virtual junction temperature, T _J		-40	150	°C
Storage temperature, T _{stg}		-60	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground pin.

6.2 ESD Ratings

over operating ambient temperature range (unless otherwise noted)

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±3000
		Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
VM	Motor power supply voltage	0	11	V
VCC	Logic power supply voltage	1.8	7	V
I _{OUT}	Motor peak current	0	1.8	A
f _{PWM}	Externally applied PWM frequency	0	250	kHz
V _{LOGIC}	Logic level input voltage	0	5.5	V
T _A	Operating ambient temperature	-40	85	°C

- (1) Power dissipation and thermal limits must be observed.

6.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC ⁽¹⁾		DRV883x	UNIT
		DSG (WS0N)	
		8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	60.9	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	71.4	°C/W
R _{θJB}	Junction-to-board thermal resistance	32.2	°C/W
ψ _{JT}	Junction-to-top characterization parameter	1.6	°C/W
ψ _{JB}	Junction-to-board characterization parameter	32.8	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	9.8	°C/W

- (1) For more information about traditional and new thermal limits, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

T_A = 25°C, over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VM, VCC)						
VM	VM operating voltage		0		11	V
I _{VM}	VM operating supply current	VM = 5 V; VCC = 3 V; No PWM		40	100	μA
		VM = 5 V; VCC = 3 V; 50 kHz PWM		0.8	1.5	mA
I _{VMQ}	VM sleep mode supply current	VM = 5 V; VCC = 3 V; nSLEEP = 0		30	95	nA
VCC	VCC operating voltage		1.8		7	V
I _{VCC}	VCC operating supply current	VM = 5 V; VCC = 3 V; No PWM		300	500	μA
		VM = 5 V; VCC = 3 V; 50 kHz PWM		0.7	1.5	mA
I _{VCCQ}	VCC sleep mode supply current	VM = 5 V; VCC = 3 V; nSLEEP = 0		5	25	nA
CONTROL INPUTS (IN1 or PH, IN2 or EN, nSLEEP)						
V _{IL}	Input logic-low voltage falling threshold		0.25 × VCC	0.38 × VCC		V
V _{IH}	Input logic-high voltage rising threshold			0.46 × VCC	0.5 × VCC	V
V _{HYS}	Input logic hysteresis			0.08 × VCC		V
I _{IL}	Input logic low current	V _{IN} = 0 V	-5		5	μA
I _{IH}	Input logic high current	V _{IN} = 3.3 V			50	μA
		V _{IN} = 3.3 V, DRV8838 nSLEEP pin		60		μA
R _{PD}	Pull-down resistance			100		kΩ
		DRV8838 nSLEEP pin		55		kΩ
MOTOR DRIVER OUTPUTS (OUT1, OUT2)						
r _{DS(on)}	HS + LS FET on-resistance	VM = 5 V; VCC = 3 V; I _O = 800 mA; T _J = 25°C		280	330	mΩ
I _{OFF}	Off-state leakage current	V _{OUT} = 0 V	-200		200	nA
PROTECTION CIRCUITS						
V _{UVLO}	VCC undervoltage lockout	VCC falling			1.7	V
		VCC rising			1.8	
I _{OCP}	Overcurrent protection trip level		1.9		3.5	A
t _{DEG}	Overcurrent deglitch time			1		μs
t _{RETRY}	Overcurrent retry time			1		ms
T _{TSD}	Thermal shutdown temperature	Die temperature T _J	150	160	180	°C

6.6 Timing Requirements

$T_A = 25^\circ\text{C}$, $V_M = 5\text{ V}$, $V_{CC} = 3\text{ V}$, $R_L = 20\ \Omega$

NO.			MIN	MAX	UNIT
1	t_1	Delay time, PHASE high to OUT1 low		160	ns
2	t_2	Delay time, PHASE high to OUT2 high		200	ns
3	t_3	Delay time, PHASE low to OUT1 high		200	ns
4	t_4	Delay time, PHASE low to OUT2 low		160	ns
5	t_5	Delay time, ENBL high to OUTx high		200	ns
6	t_6	Delay time, ENBL low to OUTx low		160	ns
7	t_7	Output enable time		300	ns
8	t_8	Output disable time		300	ns
9	t_9	Delay time, INx high to OUTx high		160	ns
10	t_{10}	Delay time, INx low to OUTx low		160	ns
11	t_{11}	Output rise time	30	188	ns
12	t_{12}	Output fall time	30	188	ns
	t_{wake}	Wake time, nSLEEP rising edge to part active		30	μs

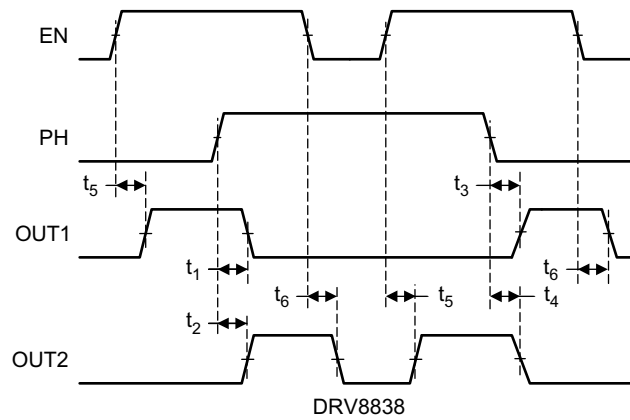


Figure 6-1. Input and Output Timing for DRV8838

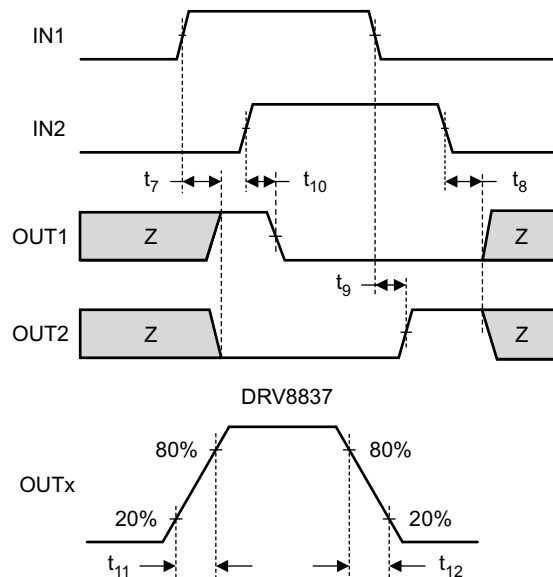
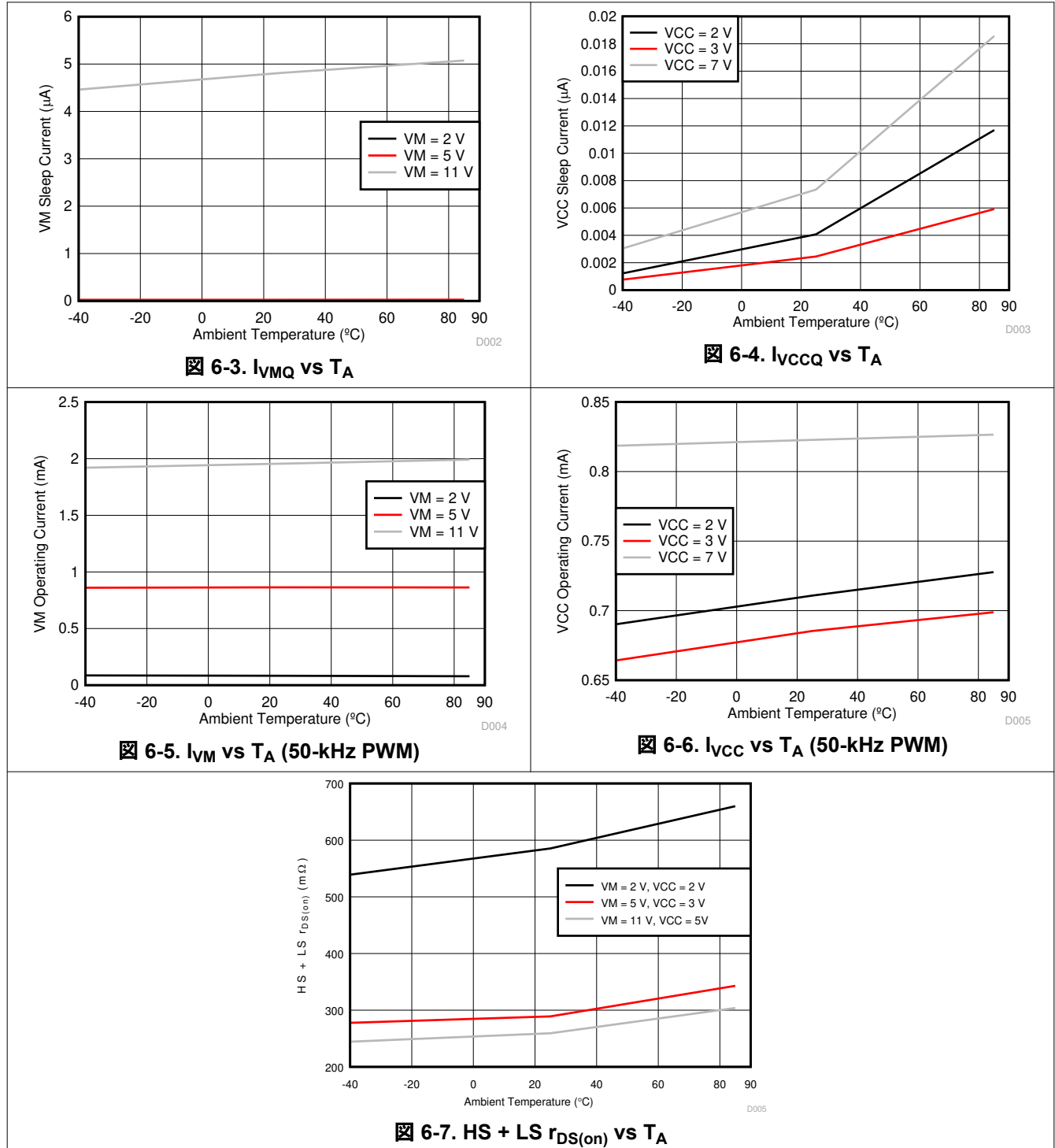


Figure 6-2. Input and Output Timing for DRV8837

6.7 Typical Characteristics



7 Detailed Description

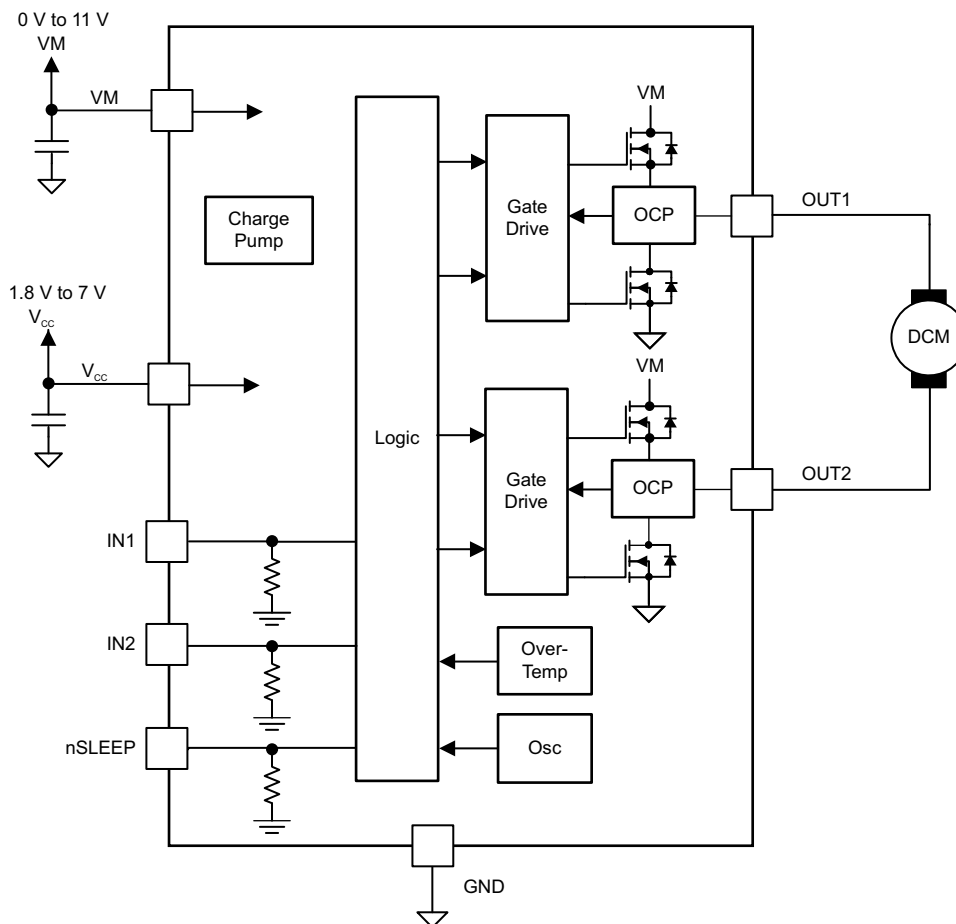
7.1 Overview

The DRV883x family of devices is an H-bridge driver that can drive one dc motor or other devices like solenoids. The outputs are controlled using either a PWM interface (IN1 and IN2) on the DRV8837 device or a PH-EN interface on the DRV8838 device.

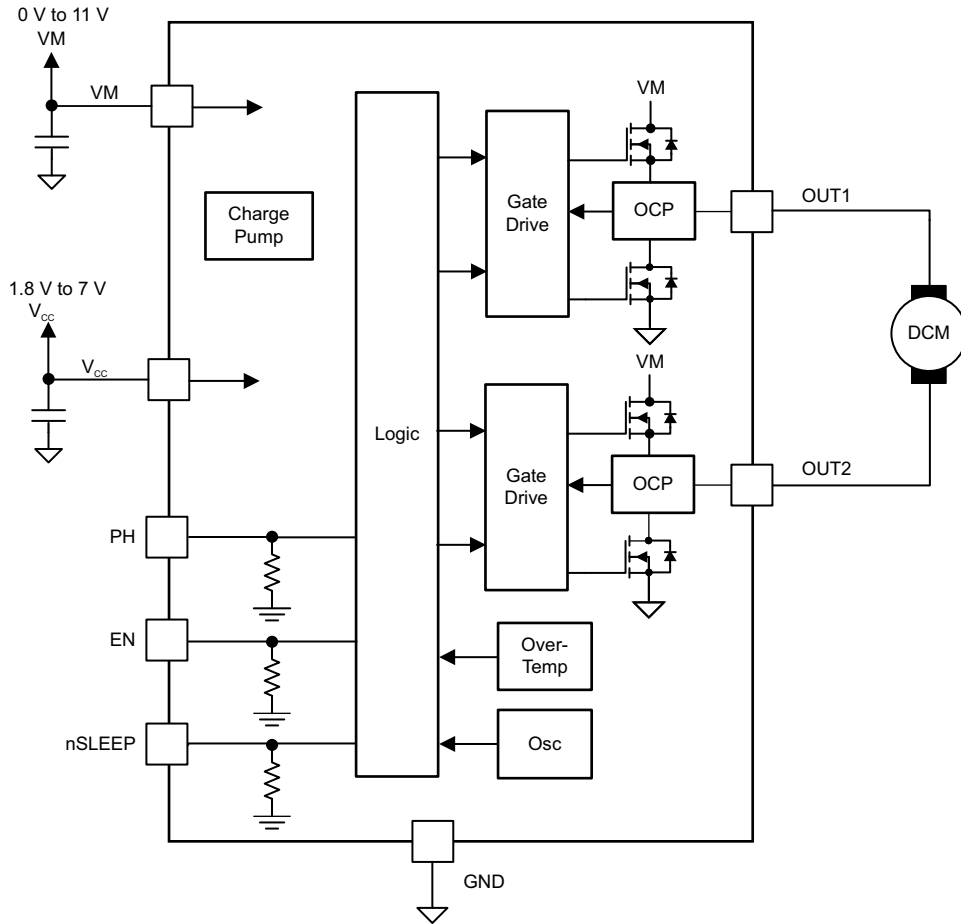
A low-power sleep mode is included, which can be enabled using the nSLEEP pin.

These devices greatly reduce the component count of motor driver systems by integrating the necessary driver FETs and FET control circuitry into a single device. In addition, the DRV883x family of devices adds protection features beyond traditional discrete implementations: undervoltage lockout, overcurrent protection, and thermal shutdown.

7.2 Functional Block Diagram



7-1. DRV8837 Functional Block Diagram




7-2. DRV8838 Functional Block Diagram

7.3 Feature Description

7.3.1 Bridge Control

The DRV8837 device is controlled using a PWM input interface, also called an IN-IN interface. Each output is controlled by a corresponding input pin.

表 7-1 shows the logic for the DRV8837 device.

表 7-1. DRV8837 Device Logic

nSLEEP	IN1	IN2	OUT1	OUT2	FUNCTION (DC MOTOR)
0	X	X	Z	Z	Coast
1	0	0	Z	Z	Coast
1	0	1	L	H	Reverse
1	1	0	H	L	Forward
1	1	1	L	L	Brake

The DRV8838 device is controlled using a PHASE/ENABLE interface. This interface uses one pin to control the H-bridge current direction, and one pin to enable or disable the H-bridge.

表 7-2 shows the logic for the DRV8838.

表 7-2. DRV8838 Device Logic

nSLEEP	PH	EN	OUT1	OUT2	FUNCTION (DC MOTOR)
0	X	X	Z	Z	Coast
1	X	0	L	L	Brake
1	1	1	L	H	Reverse
1	0	1	H	L	Forward

7.3.2 Independent Half-Bridge Control

Independent half-bridge control is possible with the DRV8837 without adopting more discrete components, as shown in [セクション 7.3.2](#). Two inductive loads (M1 and M2), which could be motors or solenoids, are tied between VM and OUTx, while the corresponding inputs (C1 and C2) are swapped before being fed to INx.

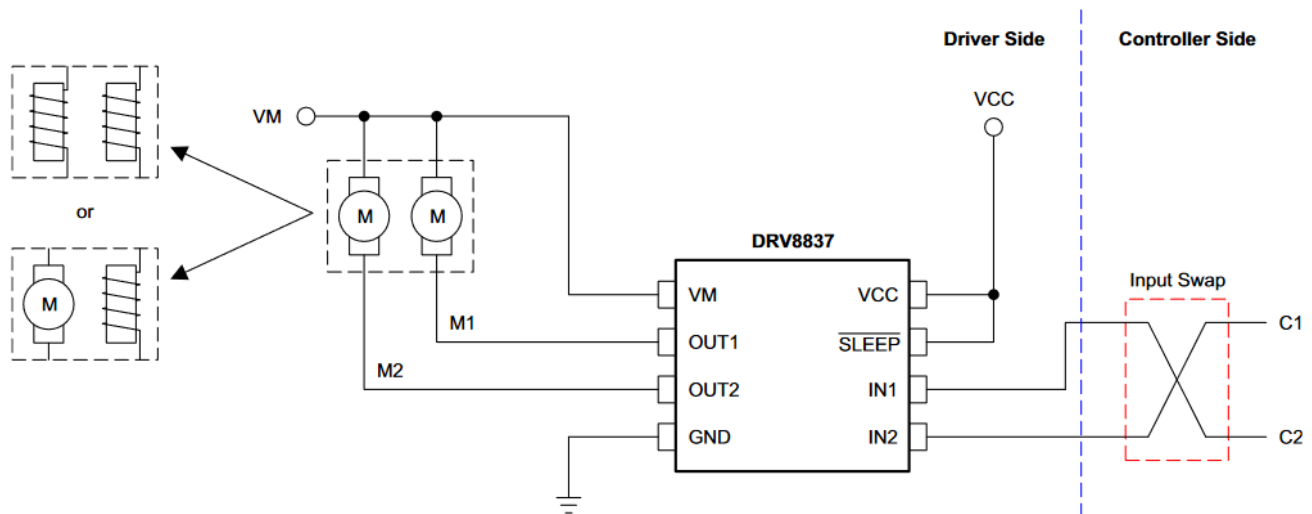


図 7-3. Independent Half-Bridge Control Circuit

The control logic for independent half-bridge drive is shown in 表 7-3. Columns INx and OUTx show the original logic of the DRV8837. Note that although a swap is included in this implementation, it is still valid that Cx = 1

spins a motor or energizes a solenoid connected at corresponding Mx, while Cx = 0, stops the motor or discharges the solenoid.

表 7-3. Independent Half-Bridge Drive Logic

C1	C2	IN1	IN2	OUT1	OUT2	M1	M2
0	0	0	0	Z	Z	Off: Braking mode 1	Off: Braking mode 1
1	0	0	1	L	H	On: Driving mode	Off: Braking mode 2
0	1	1	0	H	L	Off: Braking mode 2	On: Driving mode
1	1	1	1	L	L	On: Driving mode	On: Driving mode

Figure 7-4 shows the driving mode and the two current decay paths during current regulation when PWM input control is used. The driving mode occurs when the corresponding half-bridge Cx signal is **HIGH**. When the Cx signal is **LOW**, the corresponding half bridge can go into either braking mode 1 or braking mode 2. In braking mode 1, both the high- and low-side MOSFETs of the half-bridge are tri-stated, and the recirculation current flows through the body diode of the high-side MOSFET as well as the motor itself. This braking mode happens when both C1 and C2 are **LOW**. If one of the Cx input is **LOW** and the other HIGH, the half-bridge corresponding to the **LOW** Cx input will go into braking mode 2. In braking mode 2, the low-side FET is **OFF** while its high-side counterpart is **ON**. The recirculation current flows through the high-side MOSFET and the motor.

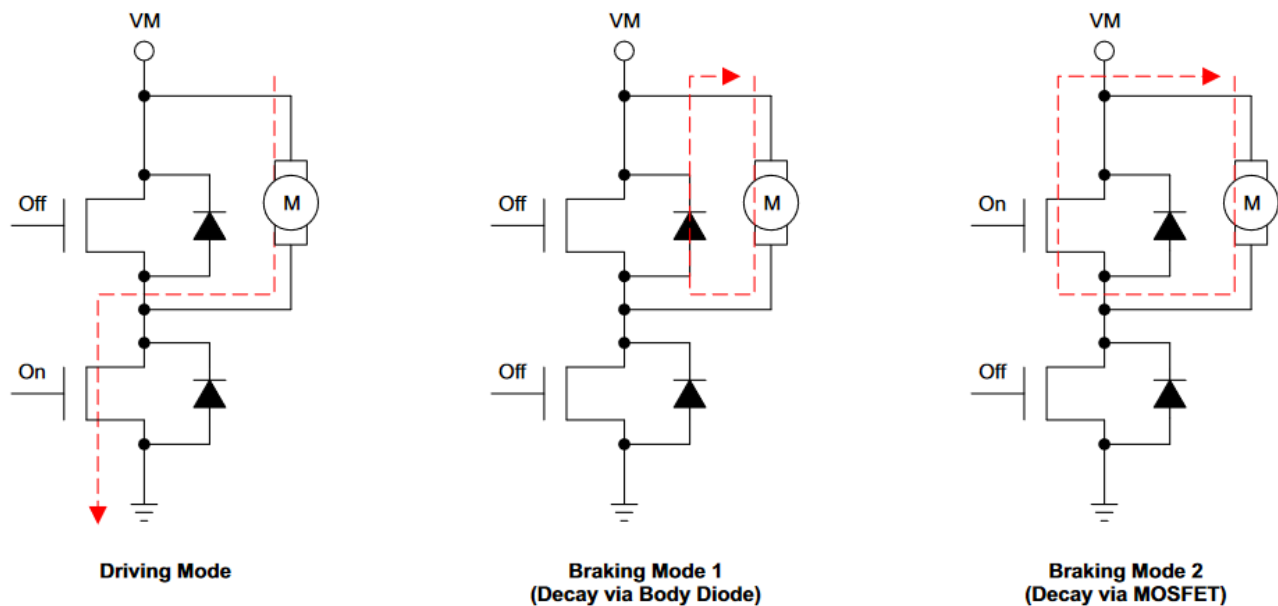
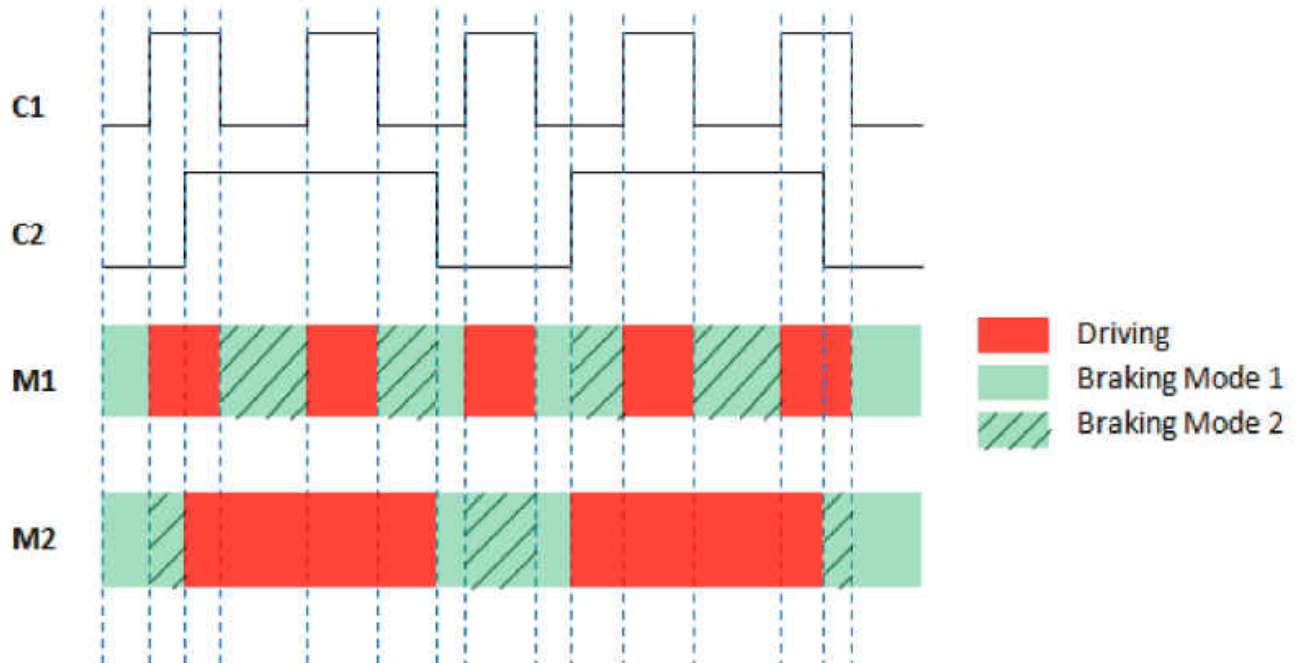
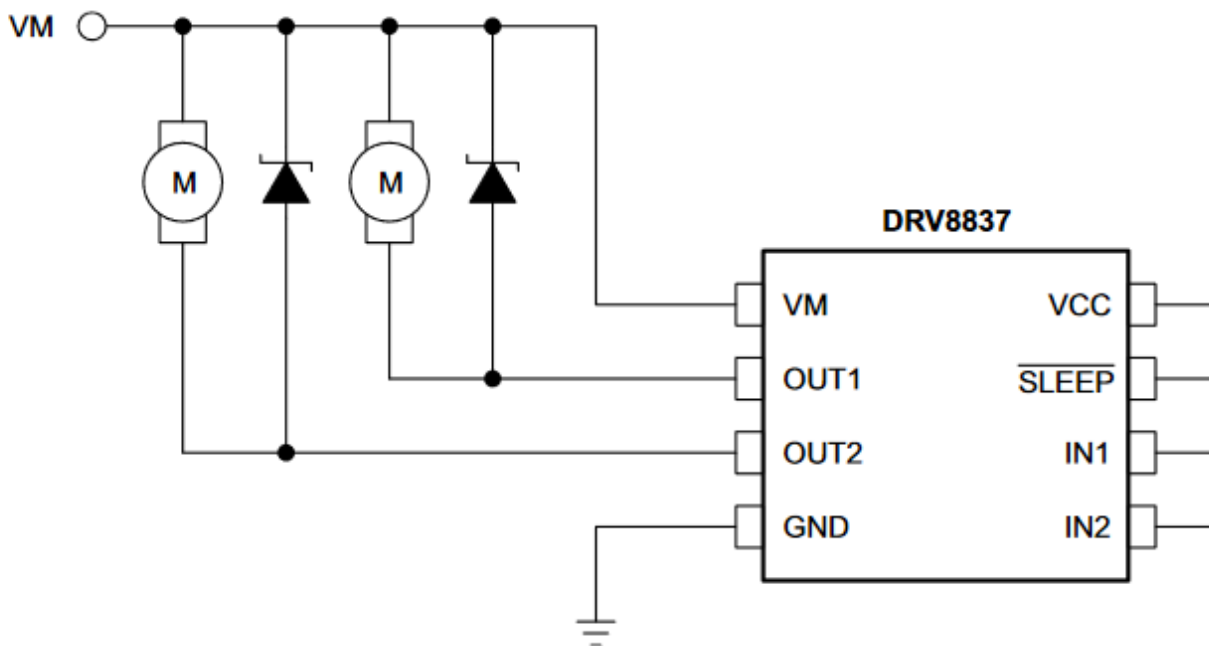


Figure 7-4. Normal Driving and Current Decay Modes

When each of the Cx inputs are independently controlled with different PWM frequencies and duty cycle, each half-bridge will go into a combination of braking mode 1 and braking mode 2. Figure 7-5 show a driving and decay example with independent PWM inputs. If the half-bridge spends more time in braking mode 1, the motor average speed will be lower since more power is dissipated through the MOSFET body diode. To reduce the power dissipated during braking mode 1, it is recommended to place Schottky diodes with forward voltage less than 0.6V across the motors as shown in Figure 7-6. Note that if On/Off control mode (constant HIGH or LOW at inputs) is used, the two braking modes do not interact with each other and hence have no effect on the average speed of the two motors.



7-5. Driving and Decay Examples with Independent PWM Inputs



7-6. Improved Application Circuit for Better Motor Performance

7.3.3 Sleep Mode

If the nSLEEP pin is brought to a logic-low state, the DRV883x family of devices enters a low-power sleep mode. In this state, all unnecessary internal circuitry is powered down.

7.3.4 Power Supplies and Input Pins

The input pins can be driven within the recommended operating conditions with or without the VCC, VM, or both power supplies present. No leakage current path will exist to the supply. Each input pin has a weak pulldown resistor (approximately 100 kΩ) to ground.

The VCC and VM supplies can be applied and removed in any order. When the VCC supply is removed, the device enters a low-power state and draws very little current from the VM supply. The VCC and VM pins can be connected together if the supply voltage is between 1.8 and 7 V.

The VM voltage supply does not have any undervoltage-lockout protection (UVLO) so as long as VCC > 1.8 V; the internal device logic remains active, which means that the VM pin voltage can drop to 0 V. However, the load cannot be sufficiently driven at low VM voltages.

7.3.5 Protection Circuits

The DRV883x family of devices is fully protected against VCC undervoltage, overcurrent, and overtemperature events.

7.3.5.1 VCC Undervoltage Lockout

If at any time the voltage on the VCC pin falls below the undervoltage lockout threshold voltage, all FETs in the H-bridge are disabled. Operation resumes when the VCC pin voltage rises above the UVLO threshold.

7.3.5.2 Overcurrent Protection (OCP)

An analog current-limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than t_{DEG} , all FETs in the H-bridge are disabled. Operation resumes automatically after t_{RETRY} has elapsed. Overcurrent conditions are detected on both the high-side and low-side FETs. A short to the VM pin, GND, or from the OUT1 pin to the OUT2 pin results in an overcurrent condition.

7.3.5.3 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge are disabled. After the die temperature falls to a safe level, operation automatically resumes.

7.3.5.4

表 7-4. Fault Behavior

FAULT	CONDITION	H-BRIDGE	RECOVERY
VCC undervoltage (UVLO)	VCC < 1.7 V	Disabled	VCC > 1.8 V
Overcurrent (OCP)	$I_{OUT} > 1.9 \text{ A (MIN)}$	Disabled	t_{RETRY} elapses
Thermal Shutdown (TSD)	$T_J > 150^\circ\text{C (MIN)}$	Disabled	$T_J < 150^\circ\text{C}$

7.4 Device Functional Modes

The DRV883x family of devices is active unless the nSLEEP pin is brought logic low. In sleep mode, the H-bridge FETs are disabled Hi-Z. The DRV883x is brought out of sleep mode automatically if nSLEEP is brought logic high.

The H-bridge outputs are disabled during undervoltage lockout, overcurrent, and overtemperature fault conditions.

表 7-5. Operation Modes

MODE	CONDITION	H-BRIDGE
Operating	nSLEEP pin = 1	Operating
Sleep mode	nSLEEP pin = 0	Disabled
Fault encountered	Any fault condition met	Disabled

Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV883x family of devices is device is used to drive one dc motor or other devices like solenoids. The following design procedure can be used to configure the DRV883x family of devices.

8.2 Typical Application

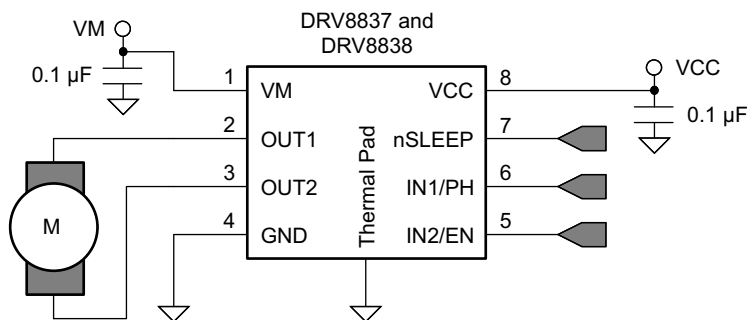


图 8-1. Schematic of DRV883x Application

8.2.1 Design Requirements

表 8-1 lists the required parameters for a typical usage case.

表 8-1. System Design Requirements

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Motor supply voltage	VM	9 V
Logic supply voltage	VCC	3.3 V
Target rms current	I _{OUT}	0.8 A

8.2.2 Detailed Design Procedure

8.2.2.1 Motor Voltage

The appropriate motor voltage depends on the ratings of the motor selected and the desired RPM. A higher voltage spins a brushed dc motor faster with the same PWM duty cycle applied to the power FETs. A higher voltage also increases the rate of current change through the inductive motor windings.

8.2.2.2 Low-Power Operation

When entering sleep mode, TI recommends setting all inputs as a logic low to minimize system power.

8.2.3 Application Curves

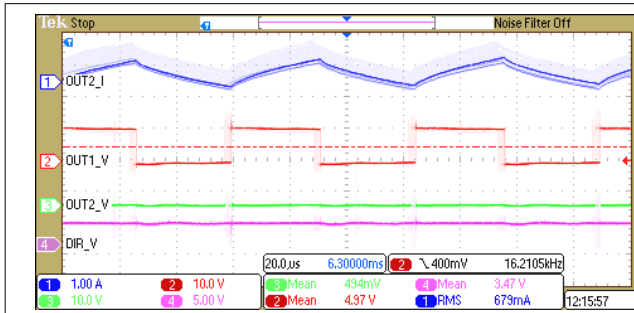


图 8-2. 50% Duty Cycle, Forward Direction

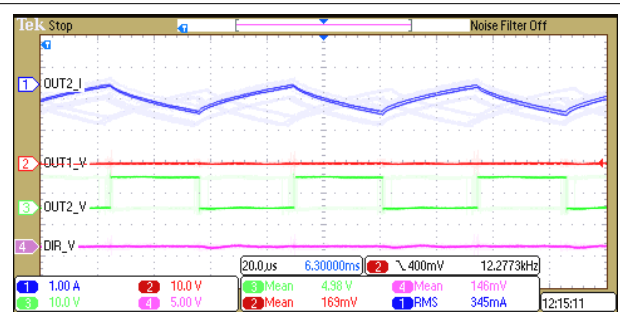


图 8-3. 50% Duty Cycle, Reverse Direction

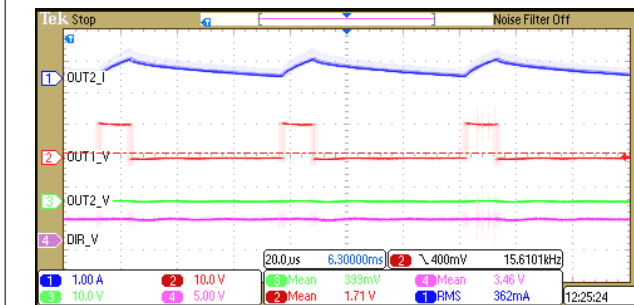


图 8-4. 20% Duty Cycle, Forward Direction

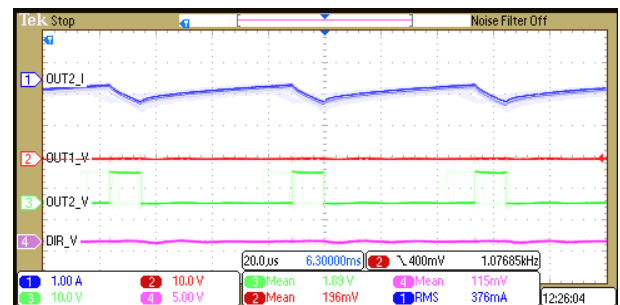


图 8-5. 20% Duty Cycle, Reverse Direction

注

DIR_V is an indication of the motor direction. It is not a pin of the DRV883x device.

8 Power Supply Recommendations

8.1 Bulk Capacitance

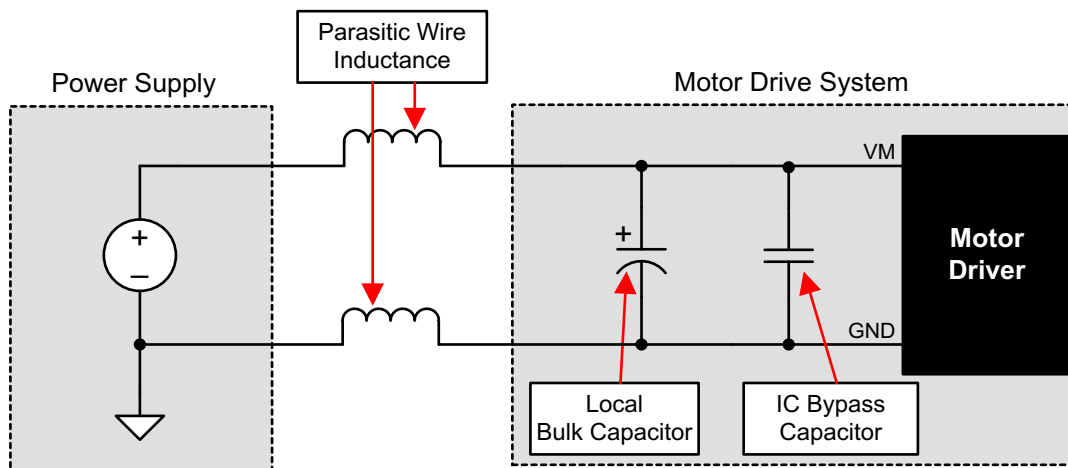
Having appropriate local bulk capacitance is an important factor in motor-drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The power-supply capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed dc, brushless dc, stepper)
- The motor braking method

The inductance between the power supply and motor drive system limits the rate at which current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate size of bulk capacitor.



8-1. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply

9 Layout

9.1 Layout Guidelines

The VM and VCC pins should be bypassed to GND using low-ESR ceramic bypass capacitors with a recommended value of 0.1 μF rated for VM and VCC. These capacitors should be placed as close to the VM and VCC pins as possible with a thick trace or ground plane connection to the device GND pin.

9.2 Layout Example

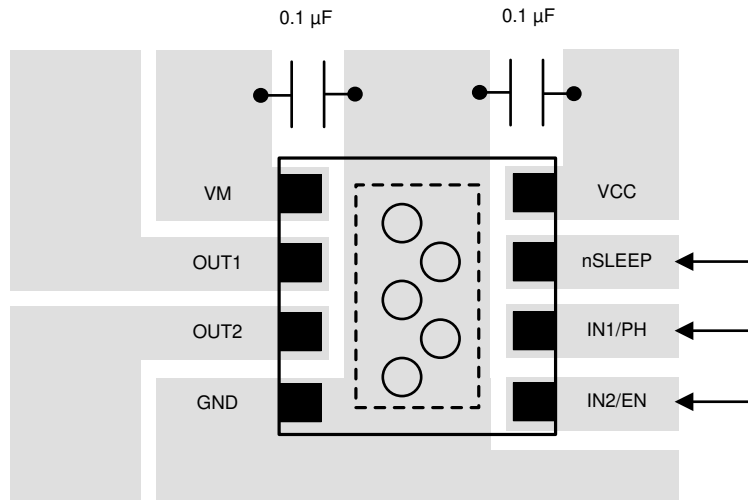


图 9-1. Simplified Layout Example

9.3 Power Dissipation

Power dissipation in the DRV883x family of devices is dominated by the power dissipated in the output FET resistance, or $r_{\text{DS(on)}}$. Use 式 1 to estimate the average power dissipation when running a stepper motor.

$$P_{\text{TOT}} = r_{\text{DS(on)}} \times (I_{\text{OUT(RMS)}})^2 \quad (1)$$

where

- P_{TOT} is the total power dissipation
- $r_{\text{DS(on)}}$ is the resistance of the HS plus LS FETs
- $I_{\text{OUT(RMS)}}$ is the rms or dc output current being supplied to the load

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

注

The value of $r_{\text{DS(on)}}$ increases with temperature, so as the device heats, the power dissipation increases.

The DRV883x family of devices has thermal shutdown protection. If the die temperature exceeds approximately 150°C, the device is disabled until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

- [Calculating Motor Driver Power Dissipation](#)
- [DRV8837EVM User's Guide](#)
- [DRV8838EVM User's Guide](#)
- [Independent Half-Bridge Drive with DRV8837](#)
- [Understanding Motor Driver Current Ratings](#)

10.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 10-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
DRV8837	Click here	Click here	Click here	Click here	Click here
DRV8838	Click here	Click here	Click here	Click here	Click here

10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.4 Community Resources

10.5 Trademarks

すべての商標は、それぞれの所有者に帰属します。

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV8837DSGR	Active	Production	WSON (DSG) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	837
DRV8837DSGR.B	Active	Production	WSON (DSG) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	837
DRV8837DSGRG4	Active	Production	WSON (DSG) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	837
DRV8837DSGRG4.B	Active	Production	WSON (DSG) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	837
DRV8838DSGR	Active	Production	WSON (DSG) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	838
DRV8838DSGR.B	Active	Production	WSON (DSG) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	838
DRV8838DSGRG4	Active	Production	WSON (DSG) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	838
DRV8838DSGRG4.B	Active	Production	WSON (DSG) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	838
DRV8838DSGT	Obsolete	Production	WSON (DSG) 8	-	-	Call TI	Call TI	-40 to 85	838

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8837DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
DRV8837DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
DRV8837DSGRG4	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
DRV8838DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
DRV8838DSGRG4	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8837DSGR	WSON	DSG	8	3000	182.0	182.0	20.0
DRV8837DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
DRV8837DSGRG4	WSON	DSG	8	3000	210.0	185.0	35.0
DRV8838DSGR	WSON	DSG	8	3000	182.0	182.0	20.0
DRV8838DSGRG4	WSON	DSG	8	3000	182.0	182.0	20.0

GENERIC PACKAGE VIEW

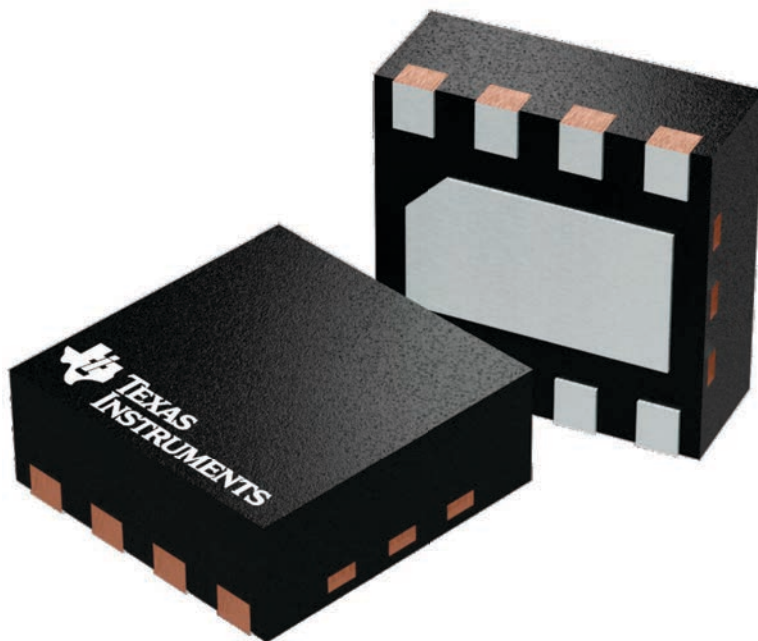
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

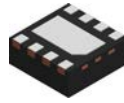
PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224783/A

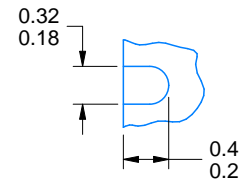
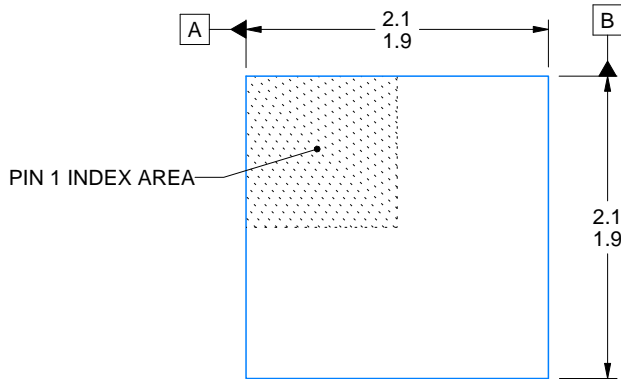
DSG0008A



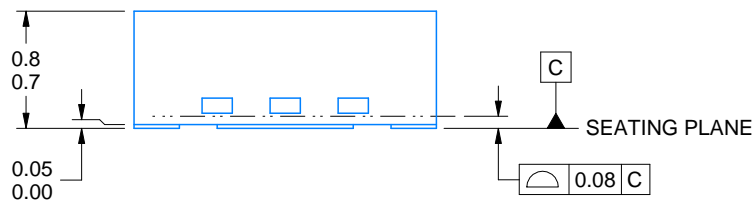
PACKAGE OUTLINE

WSON - 0.8 mm max height

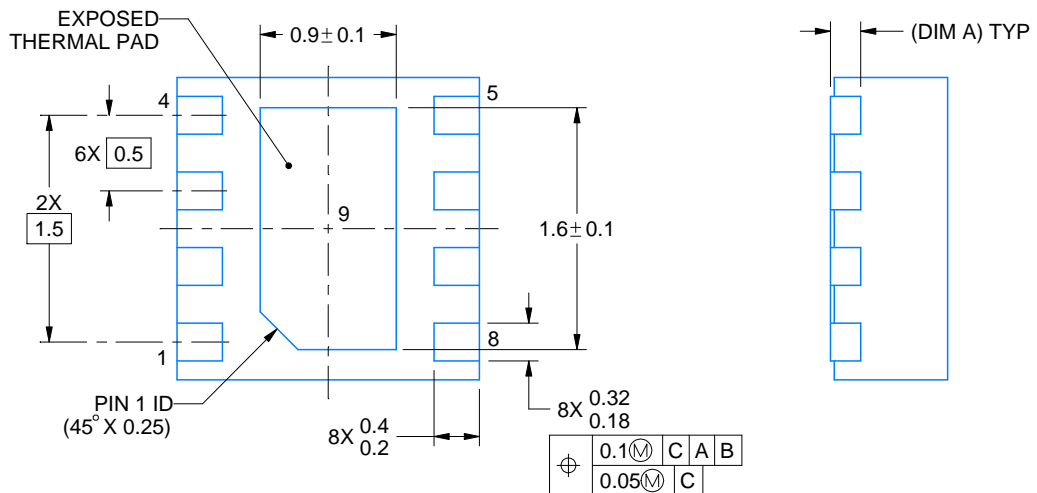
PLASTIC SMALL OUTLINE - NO LEAD



ALTERNATIVE TERMINAL SHAPE TYPICAL



SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2



4218900/E 08/2022

NOTES:

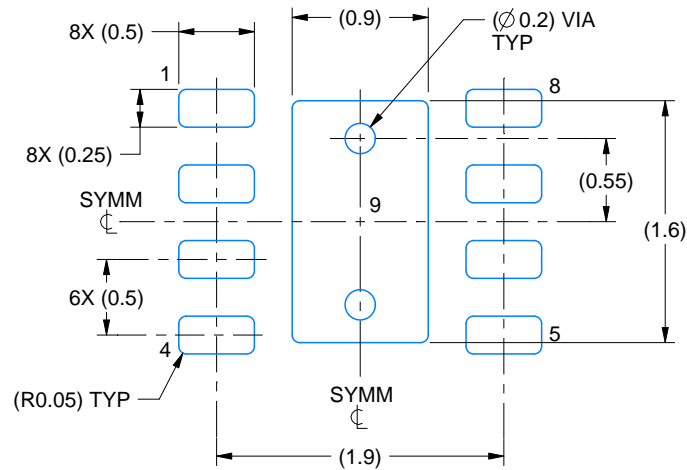
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

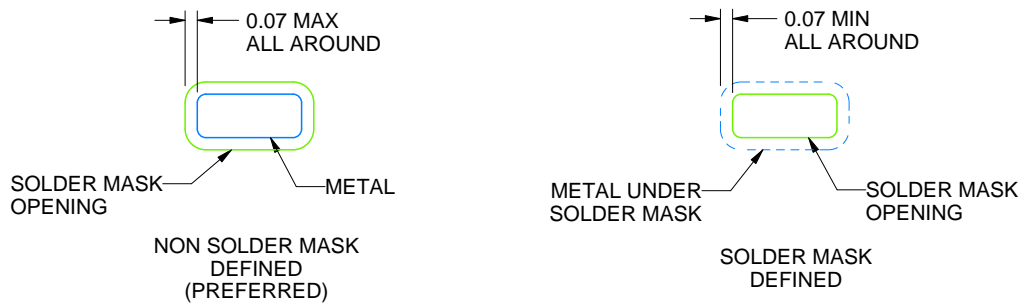
DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4218900/E 08/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

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最終更新日 : 2025 年 10 月