DRV8848 デュアル H ブリッジ モータ ドライバ

1 特長

- デュアル H ブリッジ モータ ドライバ
  - シングル／デュアルのブラシ付き DC
  - ステッパ
- 4～18V の動作電源電圧範囲
- 低オン抵抗：HS + LS = 900mΩ (標準値、25℃)
- PWM 制御インターフェイス
- **20µs 固定オフ時間のオプションの電流レギュレーション**
- H ブリッジごとの高出力電流
  - 12V および T_A = 25°C での最大駆動電流：2A
  - 12V および T_A = 25°C で最大駆動電流 4A を並列モードで対応可能
- **3µA 低消費電流スリープ モード**
- 熱特性強化型の表面実装パッケージ
- 保護機能
  - VM 低電圧誤動作防止 (UVLO)
  - 過電流保護 (OCP)
  - サーマル シャットダウン (TSD)
  - フォルト状態出力ピン (nFAULT)

2 アプリケーション

- 家電製品
- 汎用ブラシ付きモーターおよびステッパ モーター
- プリンタ

3 概要

DRV8848 は、家電機器やその他のメカトロニクス用途を対象としたデュアル H ブリッジ モータ ドライバです。このデバイスを使用すると、1 つまたは 2 つの DC モータ、1 つのバイポーラ ステッパ モータ、またはその他の負荷を駆動できます。単純な PWM インターフェイスにより、簡単に制御回路と接続できます。

各 H ブリッジ ドライバの出力ブロックには、モーター巻線を駆動するフル H ブリッジとして構成された N チャネルおよび P チャネル パワー MOSFET が搭載されています。各 H ブリッジ ドライバには、オフ時間が固定されたチョッピング方式により巻線電流を調整するための回路が含まれています。DRV8848 は、各出力から最大 2A または並列モードで最大 4A の電流を駆動できます (12V および T_A = 25°C で適切なヒートシンクを使用した場合)。

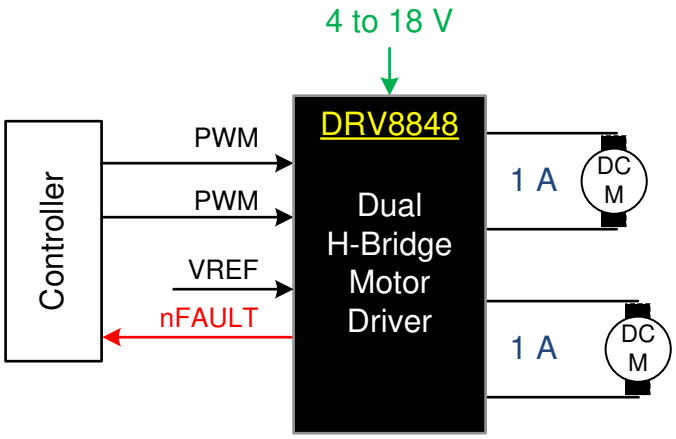
低消費電力スリープ モードが用意されており、内部回路をシャットダウンして静止消費電流を非常に小さく抑えられます。このスリープ モードは、専用の nSLEEP ピンを使用して設定できます。

UVLO、OCP、短絡保護、過熱に対する保護機能が内蔵されています。故障条件は、nFAULT ピンで通知されます。

デバイス情報 (1)

部品番号	パッケージ	本体サイズ (公称)
DRV8848	HTSSOP (16)	5.00mm × 6.40mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。



概略回路図

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4 Pin Configuration and Functions

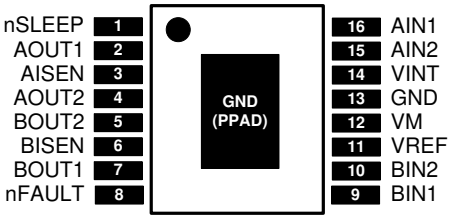


図 4-1. PWP Package 16-Pin HTSSOP Top View

Pin Functions

PIN		TYPE	DESCRIPTION	
NAME	NO.			
AIN1	16	I	Bridge A input 1	Controls AOUT1; tri-level input
AIN2	15	I	Bridge A input 2	Controls AOUT2; tri-level input
AISEN	3	O	Winding A sense	Connect to current sense resistor for bridge A, or GND if current regulation is not required
AOUT1	2	O	Winding A output	
AOUT2	4			
BIN1	9	I	Bridge B input 1	Controls BOUT1; internal pulldown
BIN2	10	I	Bridge B input 2	Controls BOUT2; internal pulldown
BISEN	6	O	Winding B sense	Connect to current sense resistor for bridge A, or GND if current regulation is not required
BOUT1	7	O	Winding B output	
BOUT2	5			
GND	13	PWR	Device ground	Both the GND pin and device PowerPAD intergrated circuit package must be connected to ground
	PPAD			
nFAULT	8	OD	Fault indication pin	Pulled logic low with fault condition; open-drain output requires external pullup
nSLEEP	1	I	Sleep mode input	Logic high to enable device; logic low to enter low-power sleep mode; internal pulldown
VINT	14	—	Internal regulator	Internal supply voltage; bypass to GND with 2.2µF, 6.3V capacitor
VM	12	PWR	Power supply	Connect to motor power supply; bypass to GND with a 0.1 and 10µF (minimum) ceramic capacitor rated for VM
VREF	11	I	Full-scale current reference input	Voltage on this pin sets the full scale chopping current; short to VINT if not supplying an external reference voltage

External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_{VM}	VM	GND	10µF (minimum) ceramic capacitor rated for VM
C_{VM}	VM	GND	0.1µF ceramic capacitor rated for VM
C_{VINT}	VINT	GND	6.3V, 2.2µF ceramic capacitor
R_{nFAULT}	VCC(1)	nFAULT	>1kΩ
R_{AISEN}	AISEN	GND	Sense resistor, see *セクション 7.2* for sizing
R_{BISEN}	BISEN	GND	Sense resistor, see *セクション 7.2* for sizing

(1) VCC is not a pin on the DRV8848, but a VCC supply voltage pullup is required for open-drain output nFAULT; nFAULT can be pulled up to VINT

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range referenced with respect to GND (unless otherwise noted)(1)

		MIN	MAX	UNIT
	Power supply voltage (VM)	-0.3	20	V
	Power supply voltage ramp rate (VM)	0	2	V/µs
	Internal regulator voltage (VINT)	-0.3	3.6	V
	Analog input pin voltage (VREF)	-0.3	3.6	V
	Control pin voltage (AIN1, AIN2, BIN1, BIN2, nSLEEP, nFAULT)	-0.3	7	V
	Continuous phase node pin voltage (AOUT1, AOUT2, BOUT1, BOUT2)	-0.3	V_{VM} + 0.6	V
	Continuous shunt amplifier input pin voltage (AISEN, BISEN)(2)	-0.6	0.6	V
	Peak drive current (AOUT1, AOUT2, BOUT1, BOUT2, AISEN, BISEN)	Internally limited		A
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Transients of ±1 V for less than 25 ns are acceptable.

5.2 ESD Ratings Comm

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{VM}	Power supply voltage range(1)	4	18	V
V_{VREF}	Reference rms voltage range(2)	1	3.3	V
f_{PWM}	Applied INPUT Signal	0	250	kHz
I_{VINT}	VINT external load current		1	mA
Irms	Motor rms current per H-bridge(3)	0	1	A
T_A	Operating ambient temperature	–40	85	°C

(1) Note that $R_{DS(ON)}$ increases and maximum output current is reduced at VM supply voltages below 5V.
(2) Operational at VREF between 0 and 1V, but accuracy is degraded.
(3) Power dissipation and thermal limits must be observed.

5.4 Thermal Information

THERMAL METRIC(1)		DRV8848 PWP (HTSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	28.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W

THERMAL METRIC[1]		DRV8848 PWP (HTSSOP) 16 PINS	UNIT
Ψ_{JB}	Junction-to-board characterization parameter	11.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

5.5 Electrical Characteristics

T_A = 25°C, over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VM, VINT)						
V_{VM}	VM operating voltage		4		18	V
I_{VM}	VM operating supply current	V_{VM} = 12 V, excluding winding current, nSLEEP = 1	1.2	1.35	1.5	mA
I_{VMQ}	VM sleep mode supply current	V_{VM} = 12V, nSLEEP = 0	0.5	1.2	3	µA
t_{SLEEP}	Sleep time	nSLEEP = 0 to sleep mode			1	ms
t_{WAKE}	Wake time	nSLEEP = 1 to output transition			1	ms
t_{ON}	Power-on time	V_{VM} > V_{UVLO} rising to output transition			1	ms
V_{INT}	VINT voltage	V_{VM} > 4 V, I_{OUT} = 0 A to 1 mA	3.13	3.3	3.47	V
LOGIC-LEVEL INPUTS (BIN1, BIN2, NSLEEP)						
V_{IL}	Input logic low voltage		0		0.7	V
V_{IH}	Input logic high voltage		1.6		5.5	V
V_{HYS}	Input logic hysteresis		100			mV
I_{IL}	Input logic low current	V_I = 0 V	-1		1	µA
I_{IH}	Input logic high current	V_I = 5 V	1		30	µA
R_{PD}	Pulldown resistance	BIN1, BIN2		200		kΩ
R_{PD}	Pulldown resistance	nSLEEP		500		kΩ
t_{DEG}	Input deglitch time	AIN1 or AIN2		400		ns
t_{DEG}	Input deglitch time	BIN1 or BIN2		200		ns
t_{PROP}	Propagation delay	AIN1 or AIN2 edge to output change		800		ns
t_{PROP}	Propagation delay	BIN1 or BIN2 edge to output change		400		ns
TRI-LEVEL INPUTS (AIN1, AIN2)						
V_{IL}	Tri-level input logic low voltage		0		0.7	V
V_{IZ}	Tri-level input Hi-Z voltage			1.1		V
V_{IH}	Tri-level input logic high voltage		1.6		5.5	V
V_{HYS}	Tri-level input hysteresis		100			mV
I_{IL}	Tri-level input logic low current	V_{IN} = 0 V	-30		-1	µA
I_{IH}	Tri-level input logic high current	V_{IN} = 5 V	1		30	µA
R_{PD}	Tri-level pulldown resistance	To GND		170		kΩ
R_{PU}	Tri-level pullup resistance	To VINT		340		kΩ
CONTROL OUTPUTS (NFAULT)						
V_{OL}	Output logic low voltage	I_O = 5 mA			0.5	V
I_{OH}	Output logic high leakage	V_O = 3.3 V	-1		1	µA
MOTOR DRIVER OUTPUTS (AOUT1, AOUT2, BOUT1, BOUT2)						
$R_{DS(ON)}$	High-side FET on resistance	V_{VM} = 12 V, I_O = 0.5 A, T_J = 25°C		550		mΩ
$R_{DS(ON)}$	High-side FET on resistance	V_{VM} = 12 V, I_O = 0.5 A, T_J = 85°C[1]		660		mΩ

T_A = 25°C, over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{DS(ON)}$	Low-side FET on resistance	V_{VM} = 12 V, I_O = 0.5 A, T_J = 25°C		350		mΩ
$R_{DS(ON)}$	Low-side FET on resistance	V_{VM} = 12 V, I_O = 0.5 A, T_J = 85°C(1)		420		mΩ
I_{OFF}	Off-state leakage current	V_{VM} = 5 V, T_J = 25°C	-1		1	µA
t_{RISE}	Output rise time			60		ns
t_{FALL}	Output fall time			60		ns
t_{DEAD}	Output dead time	Internal dead time		200		ns
PWM CURRENT CONTROL (VREF, AISEN, BISEN)						
I_{REF}	Externally applied VREF input current	V_{VREF} = 1 to 3.3 V			1	µA
V_{TRIP}	xISEN trip voltage	For 100% current step with V_{VREF} = 3.3 V		500		mV
t_{BLANK}	Current sense blanking time			1.8		µs
A_{ISENSE}	Current sense amplifier gain	Reference only		6.6		V/V
t_{OFF}	Current control constant off time			20		µs
PROTECTION CIRCUITS						
V_{UVLO}	VM undervoltage lockout	V_{VM} falling; UVLO report			2.9	V
		V_{VM} rising; UVLO recovery			3	V
I_{OCP}	Overcurrent protection trip level		2			A
t_{DEG}	Overcurrent deglitch time			2.8		µs
t_{OCP}	Overcurrent protection period			1.6		ms
T_{TSD} (1)	Thermal shutdown temperature	Die temperature T_J	150	160	180	°C
T_{HYS} (1)	Thermal shutdown hysteresis	Die temperature T_J		50		°C

(1) Not tested in production; limits are based on characterization data

5.6 Timing Requirements

NO.			MIN	MAX	UNIT
1	t_1	Delay time, xIN1 to xOUT1	100	600	ns
2	t_2	Delay time, xIN2 to xOUT1	100	600	ns
3	t_3	Delay time, xIN1 to xOUT2	100	600	ns
4	t_4	Delay time, xIN2 to xOUT2	100	600	ns
5	t_R	Output rise time	50	150	ns
6	t_F	Output fall time	50	150	ns

5.7 Typical Characteristics

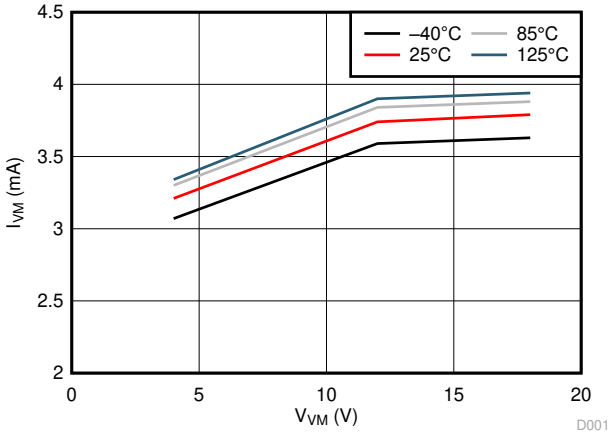


図 5-1. I_{VM} vs V_{VM}

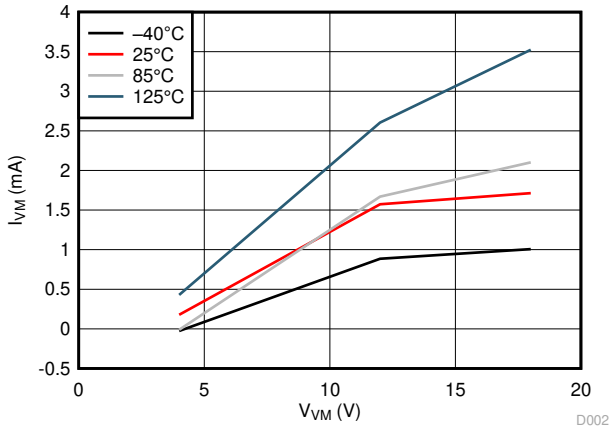


図 5-2. I_{VMQ} vs V_{VM}

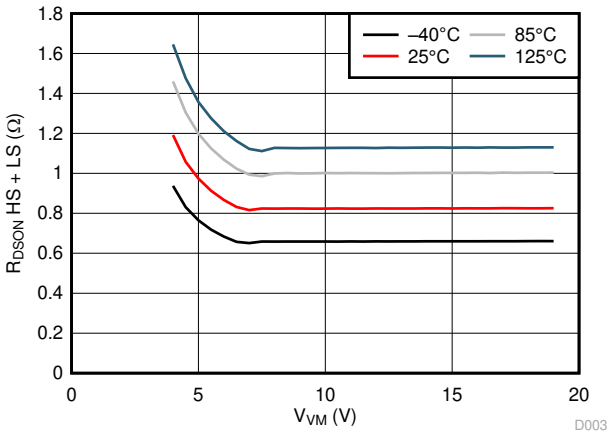


図 5-3. R_{DSON} vs V_{VM}

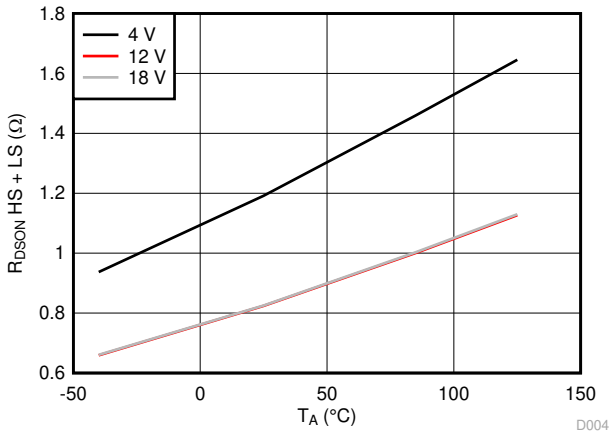


図 5-4. R_{DSON} vs Temperature

6 Detailed Description

6.1 Overview

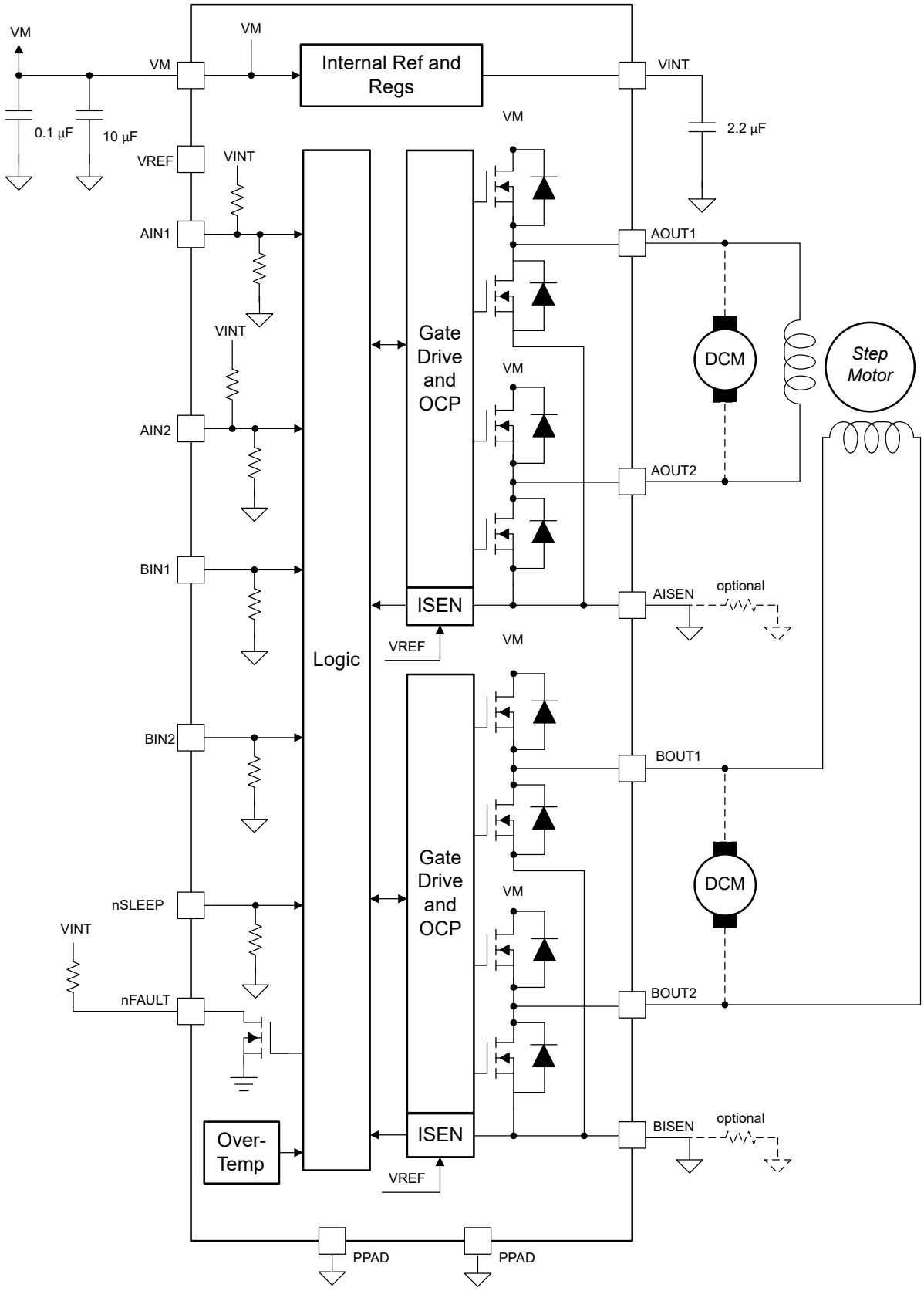
The DRV8848 is an integrated motor driver device for two DC motors or a bipolar stepper motor. The device integrates two H-bridges that use NMOS drivers and current sense regulation circuitry. The DRV8848 can be powered with a supply range between 4 to 18V and is capable of providing an output current of 1A rms.

A simple PWM interface allows easy interfacing to the controller circuit.

The current regulation uses a fixed off-time (t_{OFF}) PWM scheme. The current regulation trip point is controlled by the value of the sense resistor and the voltage applied to VREF.

A low-power sleep mode is included, which allows the system to save power when not driving the motor.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 PWM Motor Drivers

DRV8848 contains two identical H-bridge motor drivers with current-control PWM circuitry. 図 6-1 shows a block diagram of the circuitry.

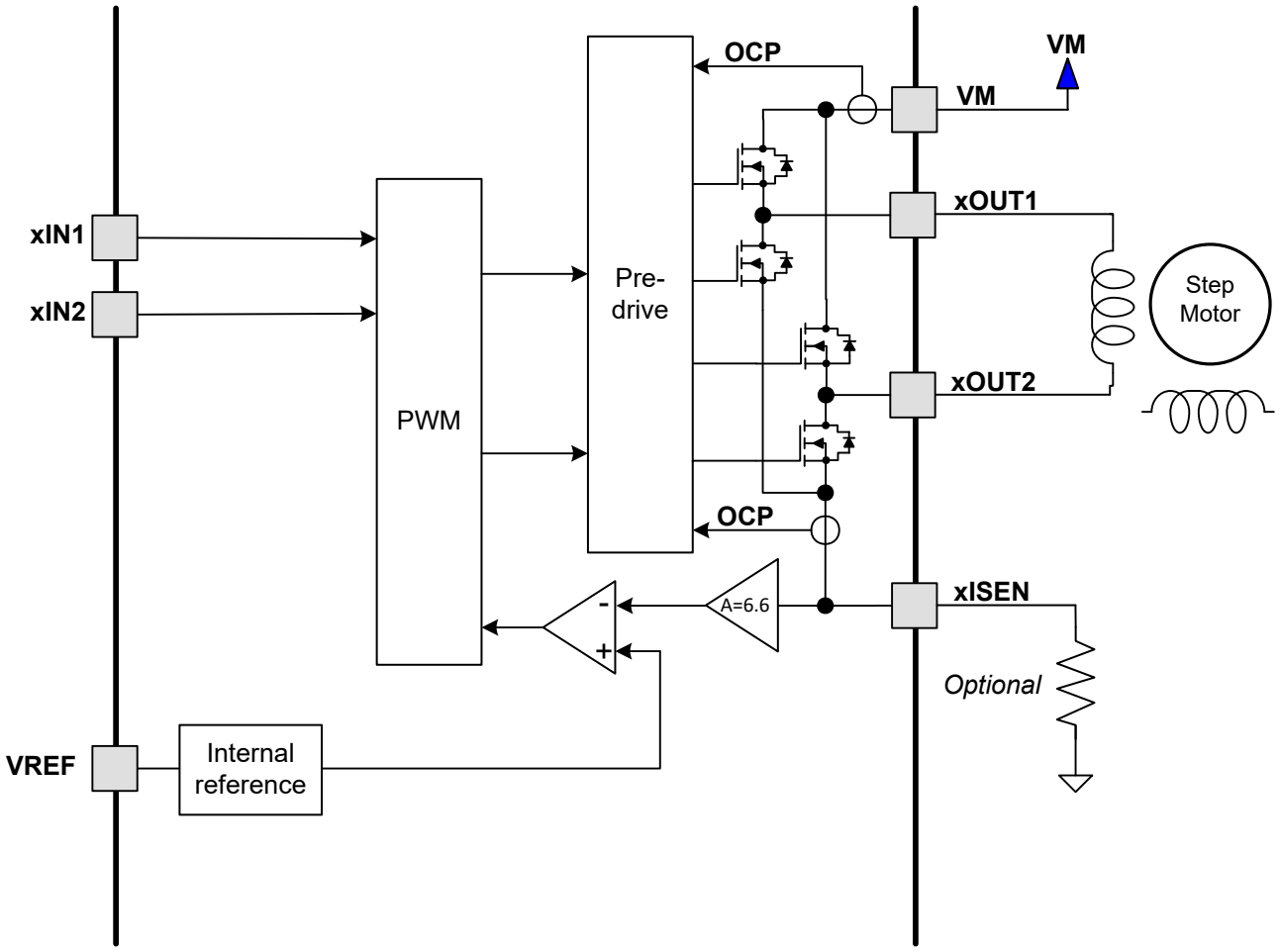


図 6-1. PWM Motor Driver Circuitry

6.3.2 Bridge Control

表 6-1 shows the logic for the inputs xIN1 and xIN2.

表 6-1. Bridge Control

xIN1	xIN2	xOUT1	xOUT2	Function (DC Motor)
0	0	Z	Z	Coast (fast decay)
0	1	L	H	Reverse
1	0	H	L	Forward
1	1	L	L	Brake (slow decay)

注

Pins AIN1 and AIN2 are tri-level, so when the pins are left Hi-Z, the pins are not internally pulled to logic low. When AIN1 or AIN2 are set to Hi-Z and not in parallel mode, the output driver maintains the previous state.

6.3.3 Parallel Operation

The two drivers can be used in parallel to deliver twice the current to a single motor. To enter parallel mode, AIN1 and AIN2 must be left Hi-Z during power-up or when exiting sleep mode (nSLEEP toggling from 0 to 1). BIN1 and BIN2 are used to control the drivers. Tie AISEN and BISEN to a single sense resistor if current control is desired. To exit parallel mode, AIN1 and AIN2 must be driven high or low and the device must be powered-up or exit sleep mode. 図 6-2 shows a block diagram of the device using parallel mode.

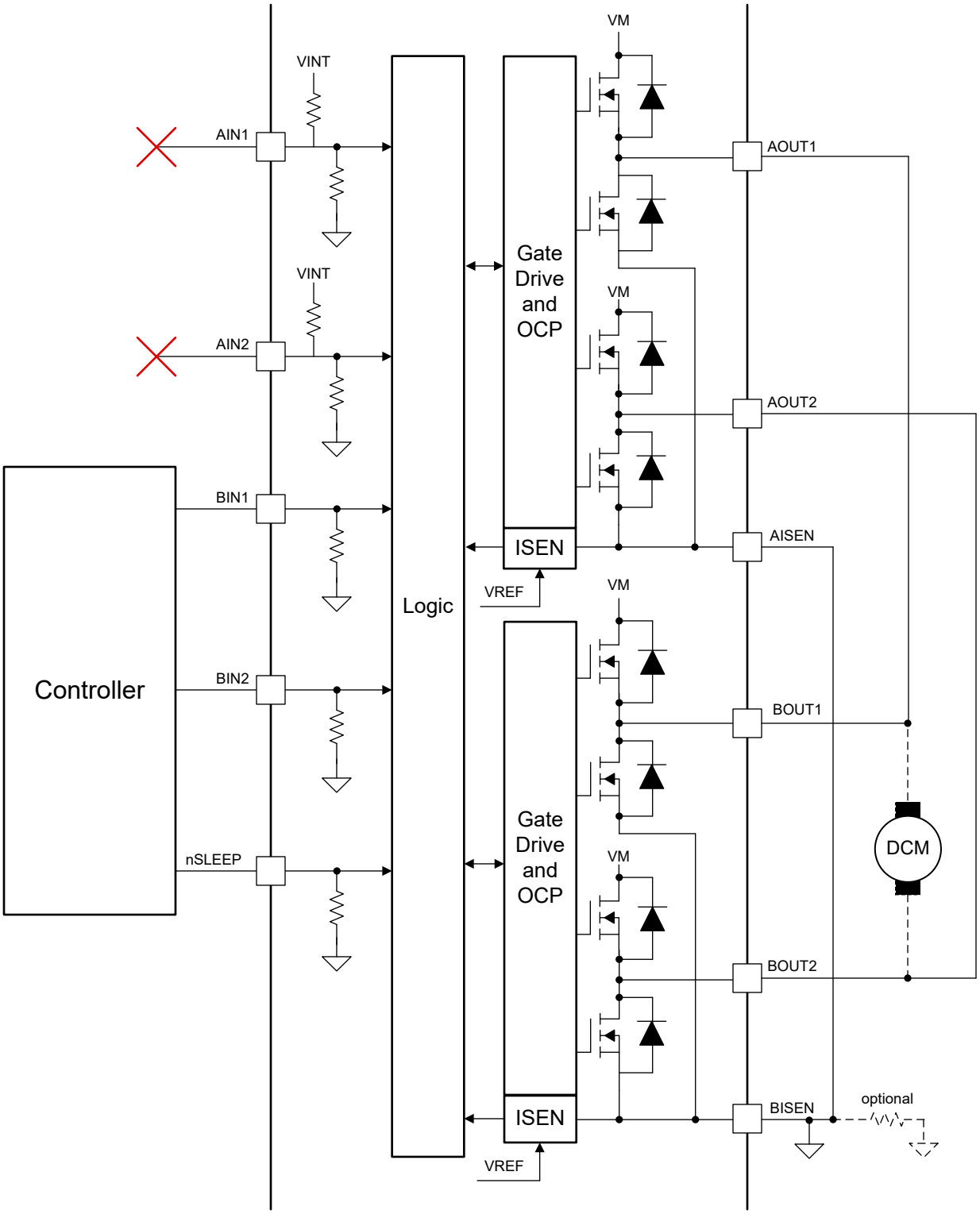


図 6-2. Parallel Mode Operation

6.3.4 Current Regulation

The current through the motor windings is regulated by a fixed-off-time PWM current regulation circuit. With DC brushed motors, current regulation can be used to limit the stall current (which is also the startup current) of the motor.

Current regulation works as follows:

When an H-bridge is enabled, current rises through the winding at a rate dependent on the supply voltage and inductance of the winding. If the current reaches the current chopping threshold, the bridge disables the current for a time t_{OFF} before starting the next PWM cycle. Note that immediately after the current is enabled, the voltage on the xISEN pin is ignored for some time (t_{BLANK}) before enabling the current sense circuitry. This blanking time also sets the minimum on-time of the PWM cycle.

The PWM chopping current is set by a comparator which compares the voltage across a current sense resistor, connected to the xISEN pin, with a reference voltage. The reference voltage is derived from the voltage applied to the VREF pin and the voltage is V_{VREF} / 6.6. The VREF pin can be tied on board to the 3.3V – VINT pin, or the VREF pin can be externally forced to a desired VREF voltage.

The full scale chopping current in a winding is calculated as follows:

$$I_{FS} = \frac{V_{VREF}}{6.6 \times R_{ISENSE}} \quad (1)$$

where

- I_{FS} is the regulated current.
- V_{VREF} is the voltage on the VREF pin.
- R_{ISENSE} is the resistance of the sense resistor.

Example: If V_{VREF} is 3.3V and a 500mΩ sense resistor is used, the full-scale chopping current is 3.3V / (6.6 × 500mΩ) = 1A.

Note that if the current control is not needed, the xISEN pins can be connected directly to ground. In this case, VREF is connected to VINT.

6.3.5 Current Recirculation and Decay Modes

During PWM current chopping, the H-bridge is enabled to drive current through the motor winding until the PWM current chopping threshold is reached (see case 1 in 図 6-3).

After the chopping current threshold is reached, the drive current is interrupted, but due to the inductive nature of the motor, current must continue to flow for some period of time. This is called recirculation current. To handle this recirculation current, the DRV8848 H-bridge operates in mixed decay mode.

Mixed decay is a combination of fast and slow decay modes. In fast decay mode, the opposite drivers are turned on to allow the current to decay (see case 2 in 図 6-3). If the winding current approaches zero, while in fast decay, the bridge is disabled to prevent any reverse current flow. In slow decay mode, winding current is recirculated by enabling both of the low-side FETs in the bridge (see case 3 in 図 6-3). Mixed decay starts with fast decay, then goes to slow decay. In DRV8848, the mixed decay ratio is 25% fast decay and 75% slow decay (as shown in 図 6-4).

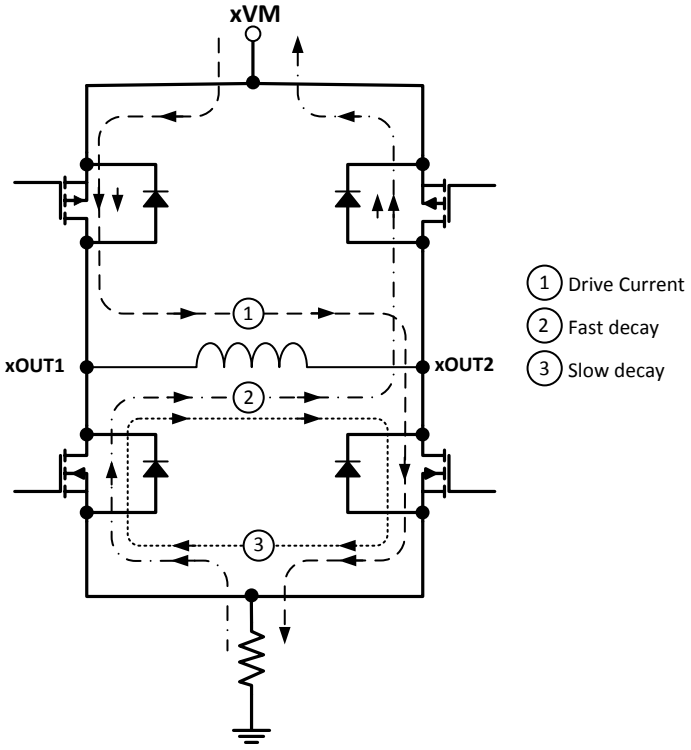


図 6-3. Decay Modes

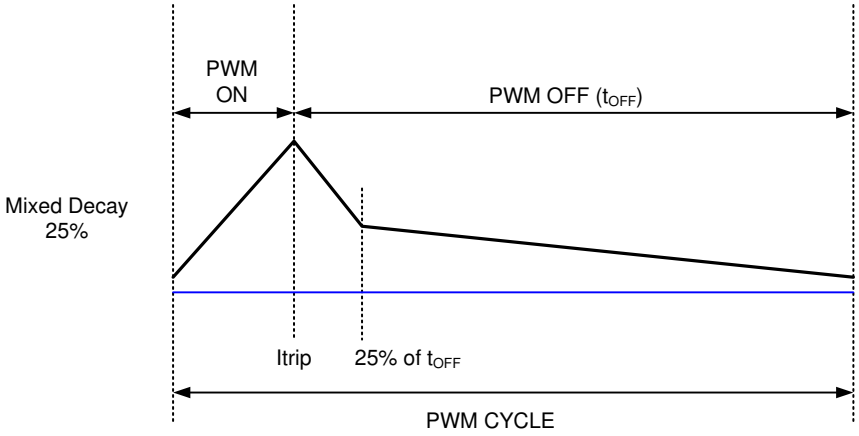


図 6-4. Mixed Decay

6.3.6 Protection Circuits

The DRV8848 is fully protected against undervoltage, overcurrent, and overtemperature events.

6.3.6.1 OCP

An analog current limit circuit on each FET limits the current through the FET by limiting the gate drive. If this analog current limit persists for longer than the OCP deglitch time t_{OCP}, all FETs in the H-bridge are disabled and the nFAULT pin is driven low. The device remains disabled until the retry time t_{RETRY} occurs. The OCP is independent for each H-bridge.

Overcurrent conditions are detected independently on both high-side and low-side devices; that is, a short to ground, supply, or across the motor winding all result in an OCP event. Note that OCP does not use the current sense circuitry used for PWM current control, so OCP functions even without presence of the xISEN resistors.

6.3.6.2 TSD

If the die temperature exceeds safe limits T_{TSD}, all FETs in the H-bridge are disabled and the nFAULT pin is driven low. After the die temperature has fallen to a safe level, operation automatically resumes. The nFAULT pin is released after operation has resumed.

6.3.6.3 UVLO

If at any time the voltage on the VM pin falls below the UVLO falling threshold voltage, V_{UVLO}, all circuitry in the device is disabled, and all internal logic is reset. Operation resumes when V_{VM} rises above the UVLO rising threshold. The nFAULT pin is driven low during an undervoltage condition and is released after operation has resumed.

表 6-2. Fault Handling

FAULT	ERROR REPORT	H-BRIDGE	INTERNAL CIRCUITS	RECOVERY
VM undervoltage (UVLO)	nFAULT unlatched	Disabled	Shut down	System and fault clears on recovery
Overcurrent (OCP)	nFAULT unlatched	Disabled	Operating	System and fault clears on recovery and motor is driven after time, t_{RETRY}
Thermal shutdown (TSD)	nFAULT unlatched	Disabled	Operating	System and fault clears on recovery

6.4 Device Functional Modes

The DRV8848 is active unless the nSLEEP pin is brought logic low. In sleep mode, the VINT regulator is disabled and the H-bridge FETs are disabled Hi-Z. Note that t_{SLEEP} must elapse after a falling edge on the nSLEEP pin before the device is in sleep mode. The DRV8848 is brought out of sleep mode automatically if nSLEEP is brought logic high. Note that t_{WAKE} must elapse before the output change state after wake-up.

When V_{VM} falls below the VM UVLO threshold (V_{UVLO}), the output driver, internal logic, and VINT regulator are reset.

表 6-3. Functional Modes

MODE	CONDITION	H-BRIDGE	VINT
Operating	4V < V_{VM} < 18V nSLEEP pin = 1	Operating	Operating
Sleep	4V < V_{VM} < 18V nSLEEP pin = 0	Disabled	Disabled
Fault	Any fault condition met	Disabled	Depends on fault

7 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

The DRV8848 is used in stepper or brushed DC motor control.

7.2 Typical Application

The user can configure the DRV8848 with the following design procedure.

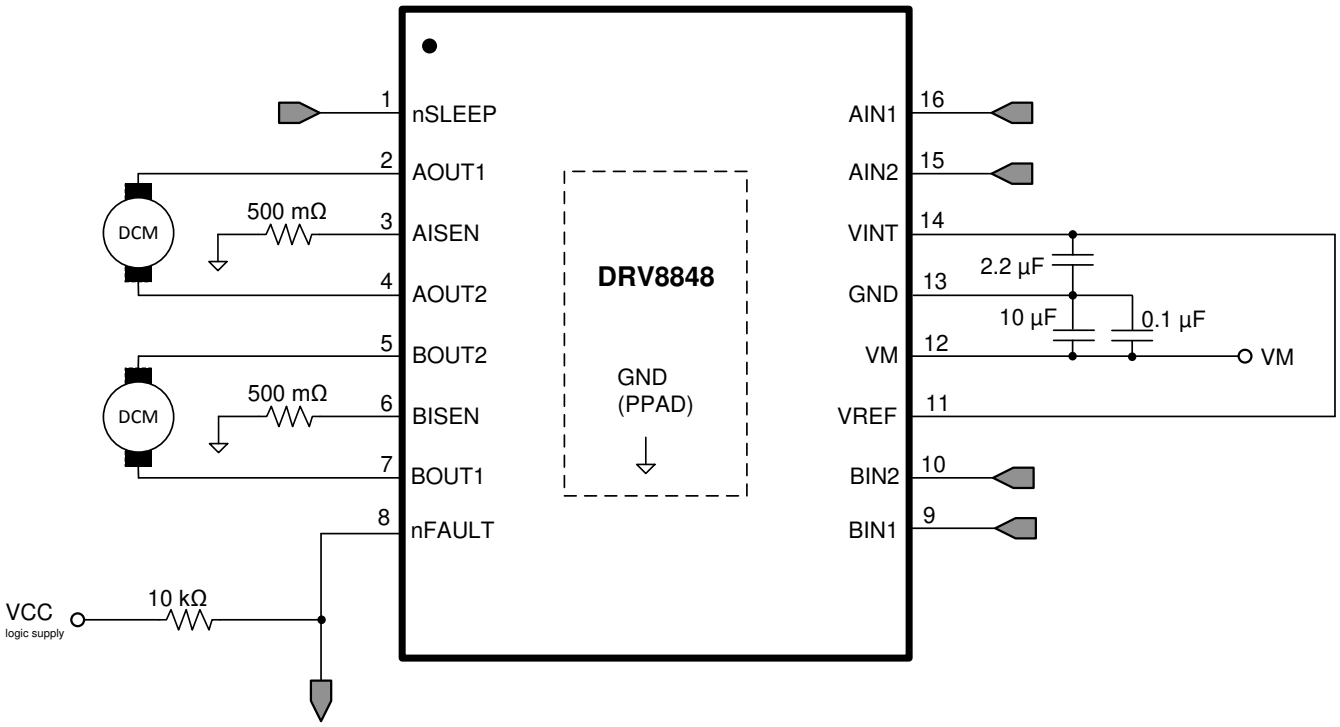


図 7-1. Typical Application Schematic

7.2.1 Design Requirements

表 7-1 gives design input parameters for system design.

表 7-1. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Nominal supply voltage	V_{VM}	12V
Supply voltage range		4 to 18V
Motor winding resistance	R_L	3Ω/phase
Motor winding inductance	L_L	330µH/phase
Target chopping current	I_{CHOP}	500mA
Chopping current reference voltage	V_{VREF}	3.3V

7.2.2 Detailed Design Procedure

7.2.2.1 Current Regulation

The chopping current (I_{CHOP}) is the maximum current driven through either winding. This quantity depends on the sense resistor value (R_{XISEN}).

$$I_{CHOP} = \frac{V_{VREF}}{6.6 \times R_{XISEN}} \tag{2}$$

I_{CHOP} is set by a comparator which compares the voltage across R_{XISEN} to a reference voltage. Note that I_{CHOP} must follow 式 3 to avoid saturating the motor.

$$I_{CHOP}\ (A) < \frac{V_{VM}\ (V)}{R_L\ (\Omega) + 2 \times R_{DS(ON)}\ (\Omega) + R_{XISEN}\ (\Omega)} \tag{3}$$

where

- V_{VM} is the motor supply voltage.
- R_L is the motor winding resistance.

7.2.3 Application Curves

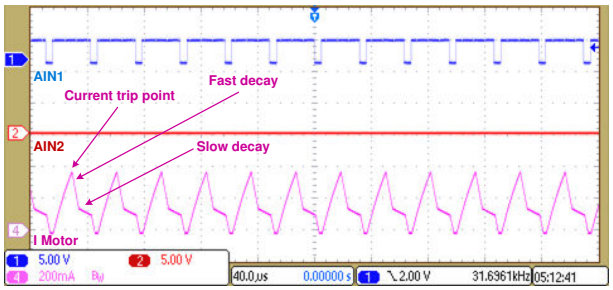


図 7-2. Current Regulation

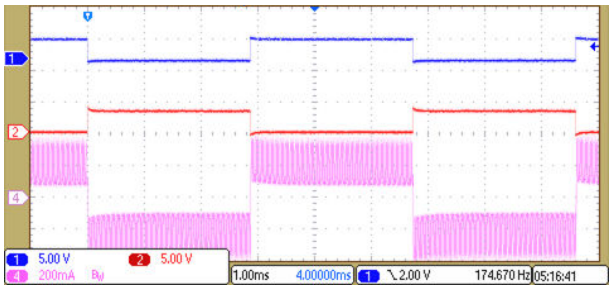


図 7-3. Stepper Mode Operation

7.3 Power Supply Recommendations

The DRV8848 is designed to operate from an input voltage supply (V_{VM}) range between 4 and 18V. Place a 0.1µF ceramic capacitor rated for VM as close to the DRV8848 as possible. In addition, the user must include a bulk capacitor of at least 10µF on VM.

7.3.1 Bulk Capacitance Sizing

Bulk capacitance sizing is an important factor in motor drive system design. Bulk capacitance sizing depends on a variety of factors including:

- Type of power supply
- Acceptable supply voltage ripple
- Parasitic inductance in the power supply wiring
- Type of motor (brushed DC, brushless DC, stepper)
- Motor startup current
- Motor braking method

The inductance between the power supply and motor drive system limits the rate that current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. Size the bulk capacitance to meet acceptable voltage ripple levels.

The data sheet provides a recommended minimum value, but system-level testing is required to determine the appropriate-sized bulk capacitor.

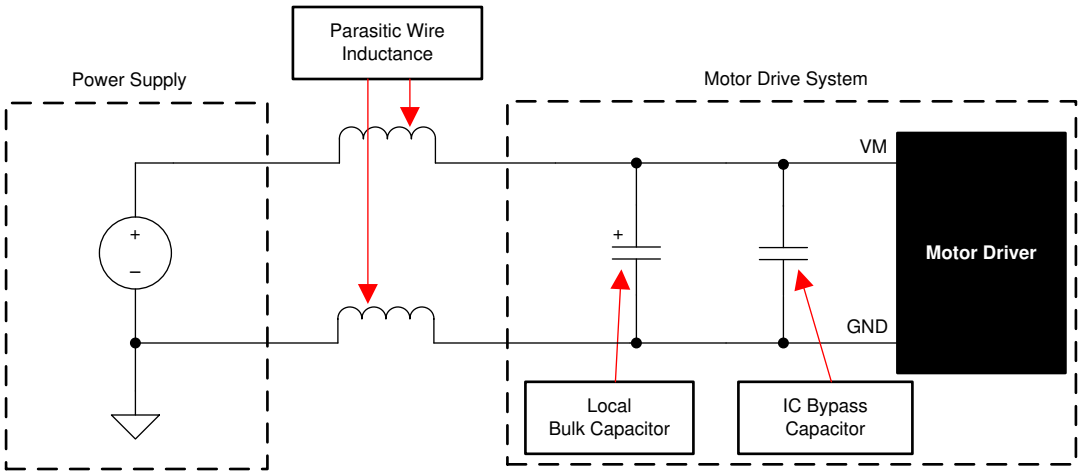


図 7-4. Setup of Motor Drive System With External Power Supply

7.4 Layout

7.4.1 Layout Guidelines

Bypass the VM terminal to GND using a low-ESR ceramic bypass capacitor with a recommended value of 10µF rated for VM. Place this capacitor as close to the VM pin as possible with a thick trace or ground plane connection to the device's GND pin.

Bypass VINT to ground with a ceramic capacitor rated 6.3V. Place this bypassing capacitor as close to the pin as possible.

7.4.2 Layout Example

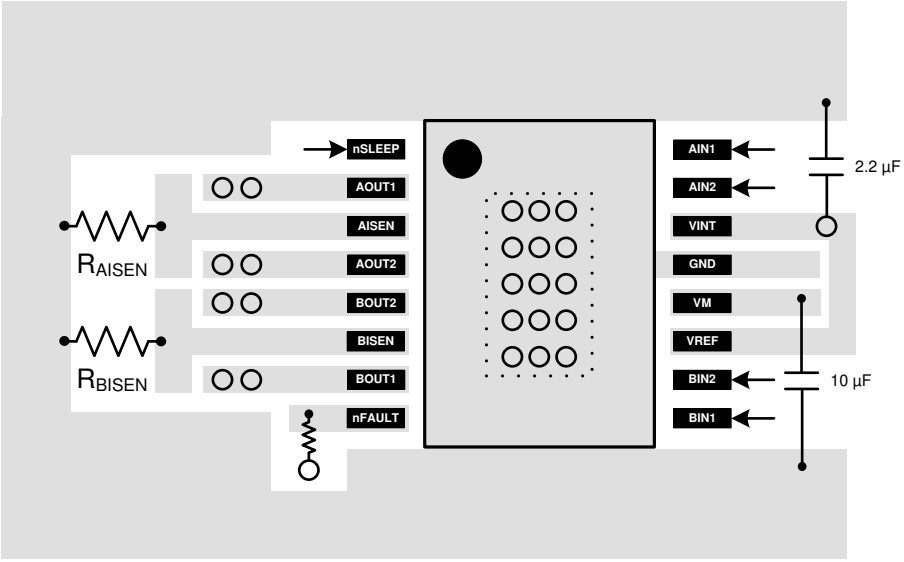


図 7-5. Layout Recommendation

8 Device and Documentation Support

8.1 サード・パーティ製品に関する免責事項

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8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.3 サポート・リソース

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

8.6 Community Resources

8.7 Trademarks

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9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (November 2015) to Revision B (April 2024)	Page
• Corrected t_F and $t_R$to denote fall time and rise time respectively	4

Changes from Revision * (October 2014) to Revision A (November 2015)	Page
• Corrected lines for 図 6-1	10
• Added *セクション 8.6*	19

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV8848PWP	Obsolete	Production	HTSSOP (PWP) | 16	-	-	Call TI	Call TI	-40 to 85	DRV8848
DRV8848PWPR	Active	Production	HTSSOP (PWP) | 16	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-3-260C-168 HR	-40 to 85	DRV8848
DRV8848PWPR.A	Active	Production	HTSSOP (PWP) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8848
DRV8848PWPR.B	Active	Production	HTSSOP (PWP) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8848
DRV8848PWPRG4	Active	Production	HTSSOP (PWP) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8848
DRV8848PWPRG4.A	Active	Production	HTSSOP (PWP) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8848
DRV8848PWPRG4.B	Active	Production	HTSSOP (PWP) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8848

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

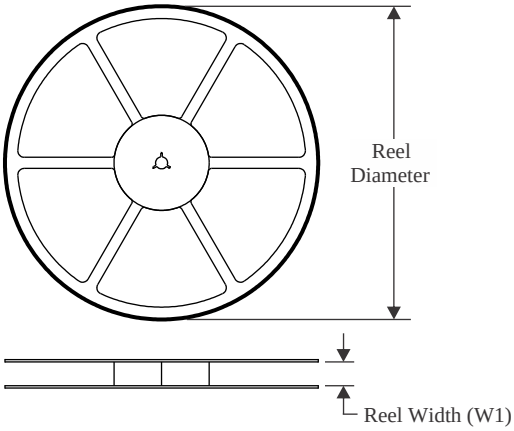
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

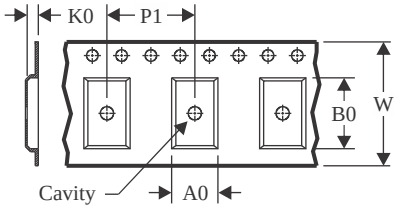
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

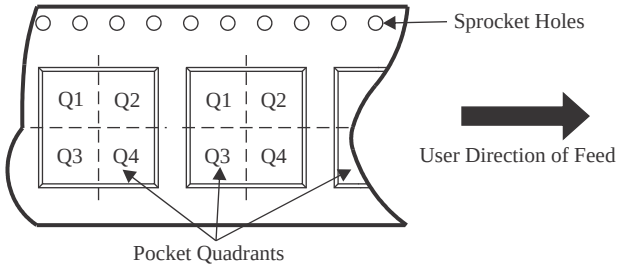


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

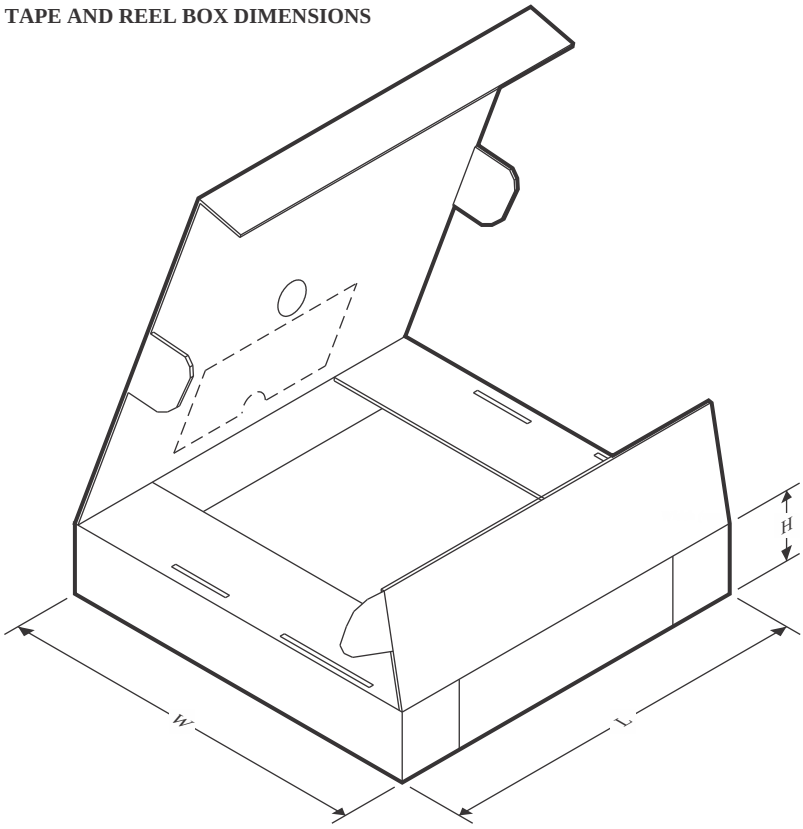
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8848PWPR	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
DRV8848PWPR	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
DRV8848PWPRG4	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

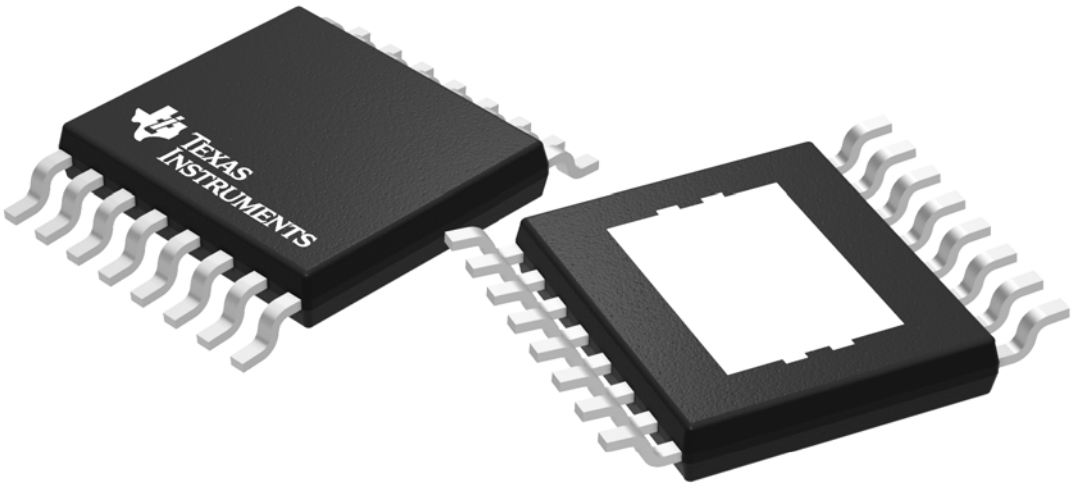


*All dimensions are nominal

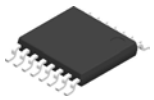
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8848PWPR	HTSSOP	PWP	16	2000	356.0	356.0	36.0
DRV8848PWPR	HTSSOP	PWP	16	2000	353.0	353.0	32.0
DRV8848PWPRG4	HTSSOP	PWP	16	2000	353.0	353.0	32.0

PWP 16 PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

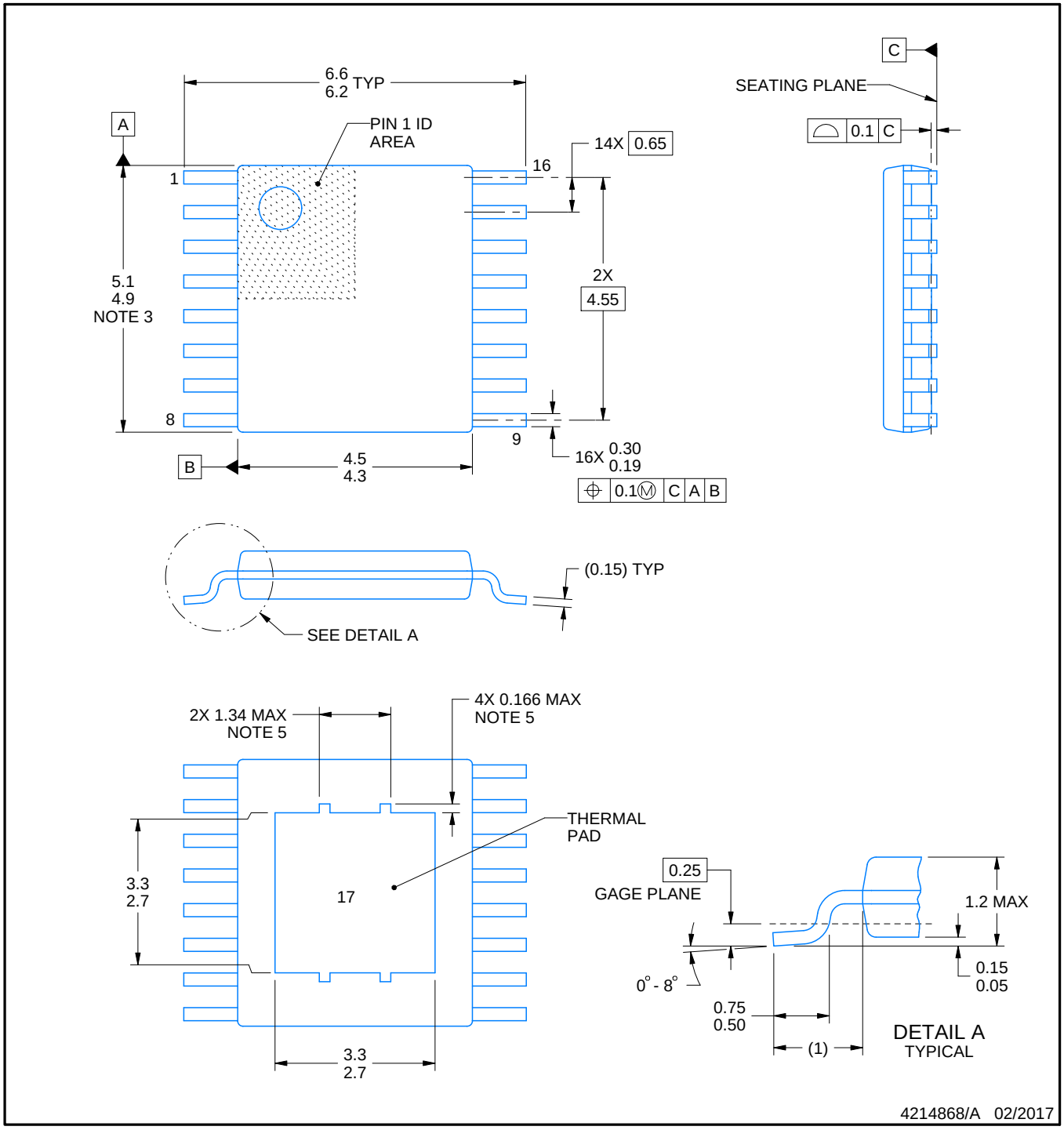


PACKAGE OUTLINE

PWP0016A

PowerPAD ™ HTSSOP - 1.2 mm max height

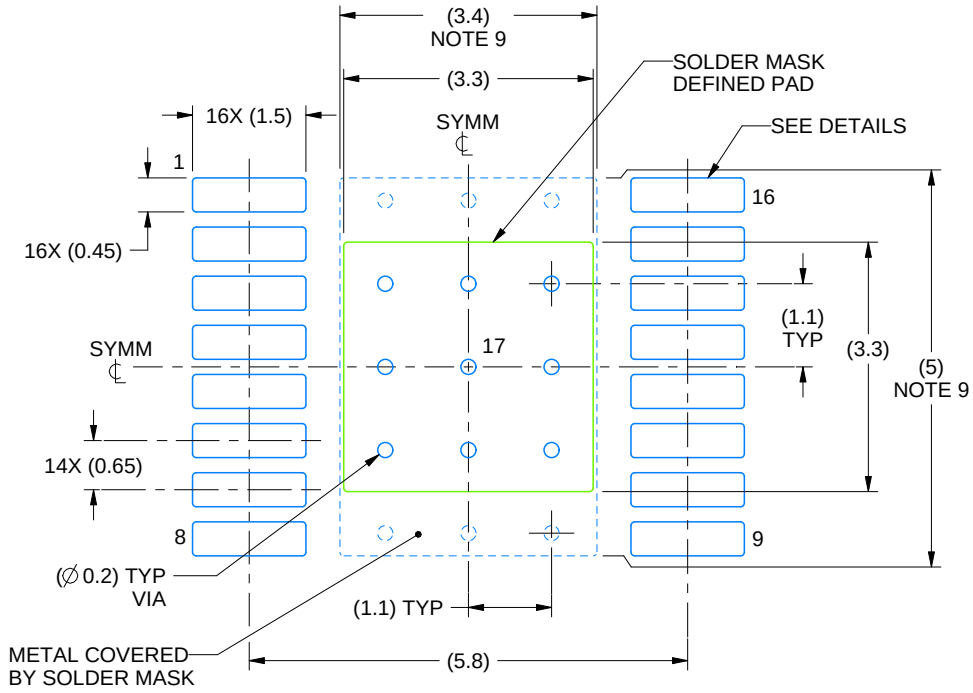
PLASTIC SMALL OUTLINE



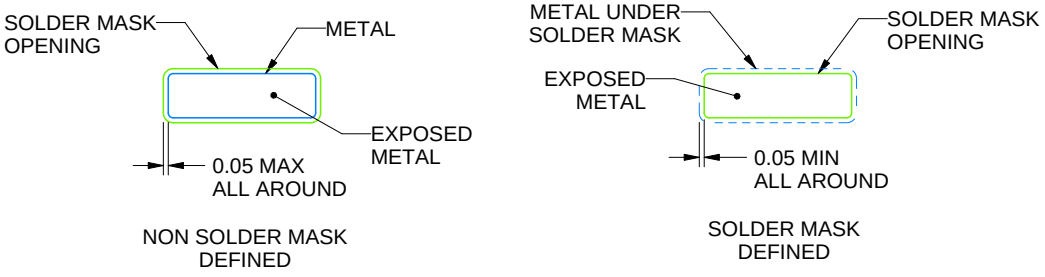
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:10X

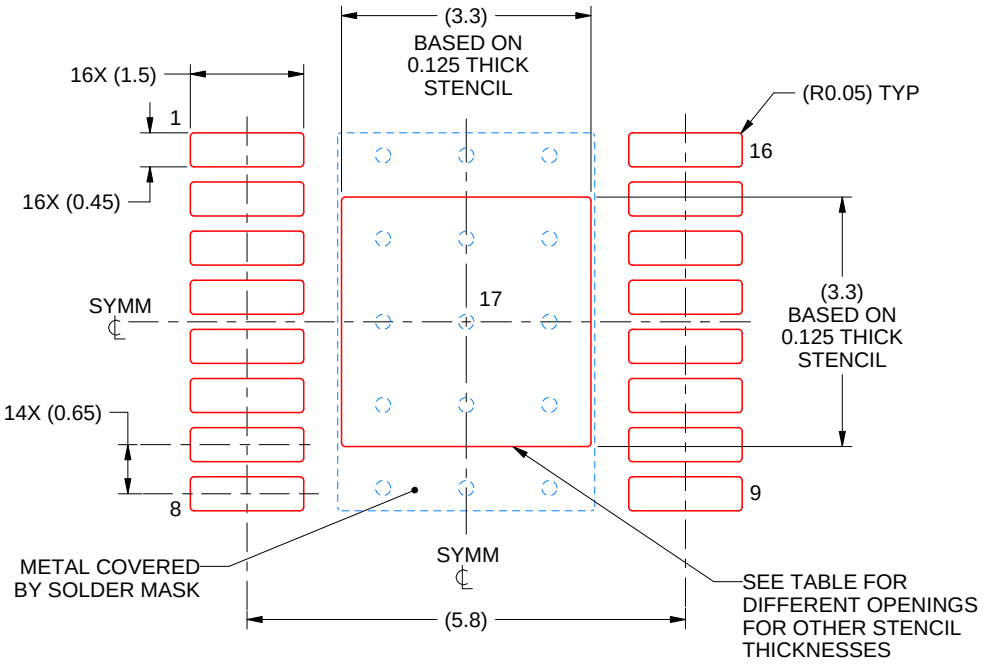


SOLDER MASK DETAILS
PADS 1-16

4214868/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.69 X 3.69
0.125	3.3 X 3.3 (SHOWN)
0.15	3.01 X 3.01
0.175	2.79 X 2.79

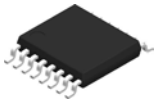
4214868/A 02/2017

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

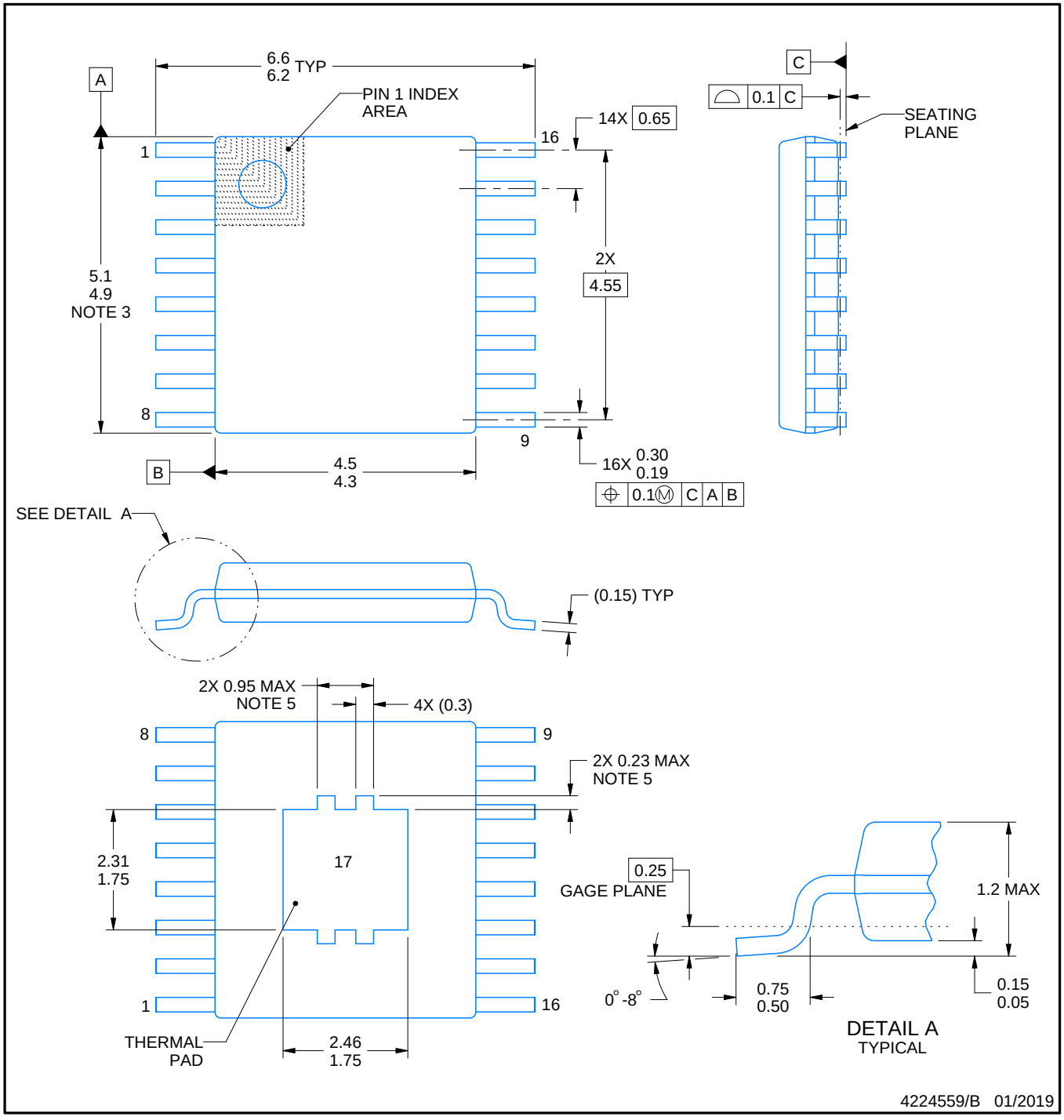
PACKAGE OUTLINE

PWP0016C



PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



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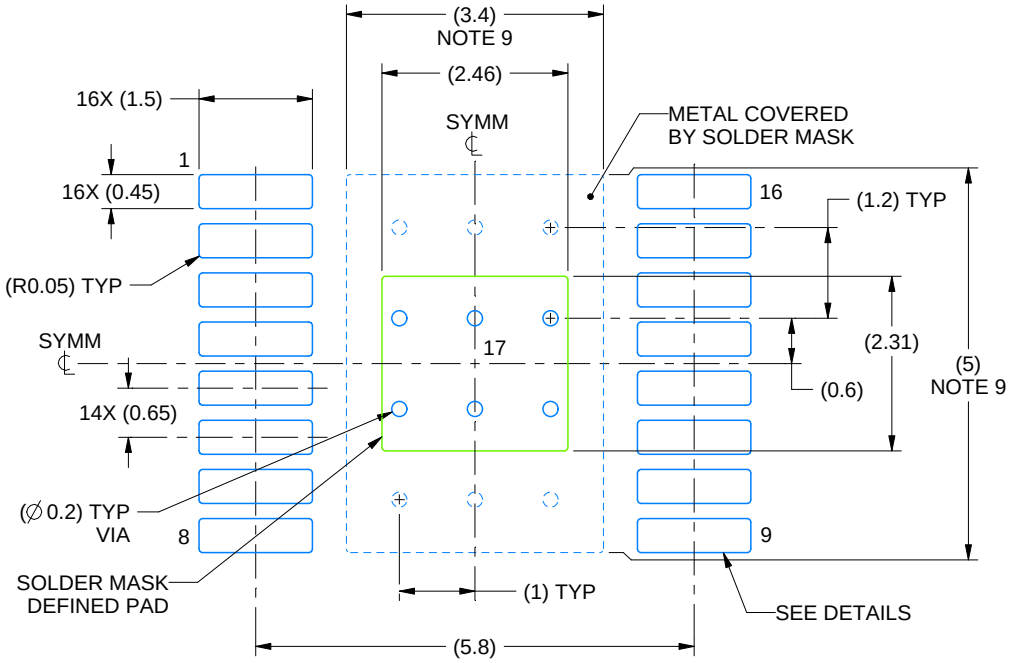
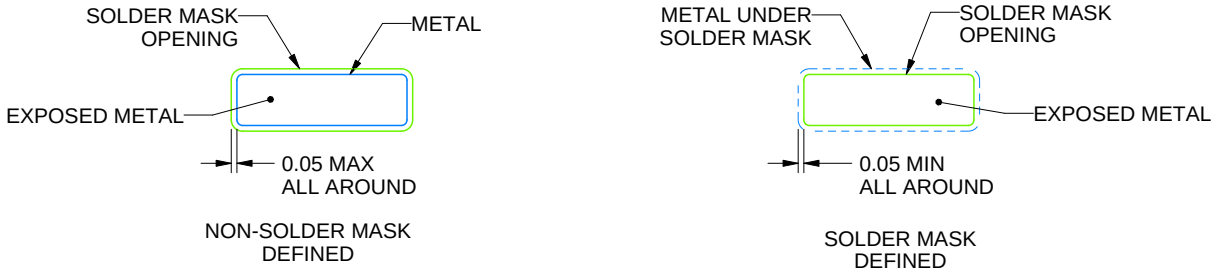
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

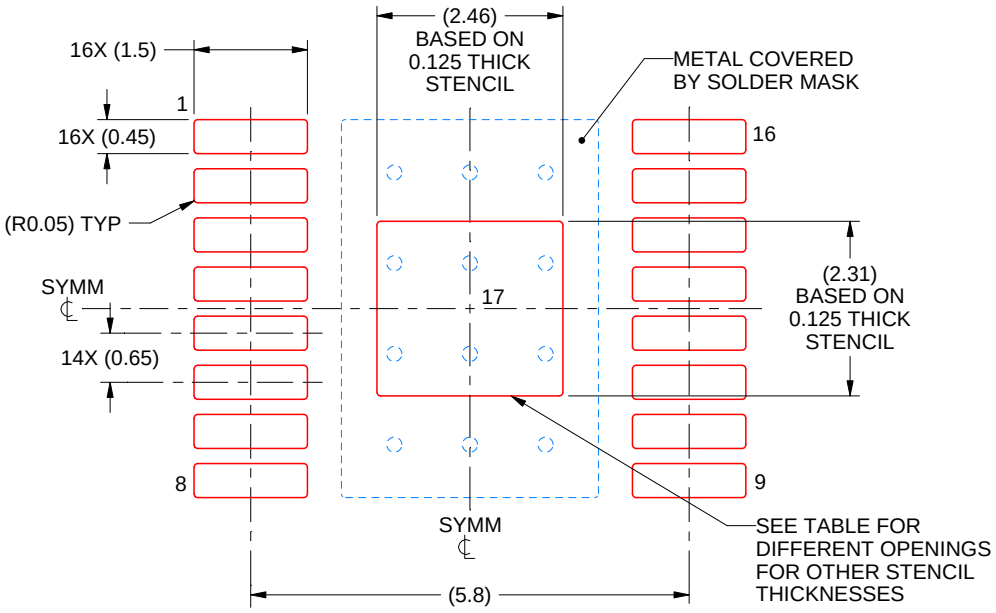


SOLDER MASK DETAILS

4224559/B 01/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.75 X 2.58
0.125	2.46 X 2.31 (SHOWN)
0.15	2.25 X 2.11
0.175	2.08 X 1.95

4224559/B 01/2019

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

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