DS92LV0411 / DS92LV0412 5 - 50 MHz Channel Link II Serializer/Deserializer with LVDS Parallel Interface

Check for Samples: DS92LV0411, DS92LV0412

FEATURES

- **5-Channel (4 data + 1 clock) Channel Link LVDS Parallel Interface Supports 24-bit Data 3-bit Control at 5 – 50 MHz**
- **AC Coupled STP Interconnect up to 10 Meters in Length**
- **Integrated Serial CML Terminations**
- **AT–SPEED BIST Mode and Status Pin**
- **Optional I2C Compatible Serial Control Bus**
- **Power Down Mode Minimizes Power Dissipation**
- **1.8V or 3.3V Compatible Control Pin Interface**
- **>8 kV ESD (HBM) Protection**
- **-40° to +85°C Temperature Range**

SERIALIZER – DS92LV0411

- **Data Scrambler for Reduced EMI**
- **DC–Balance Encoder for AC Coupling**
- **Selectable Output VOD and Adjustable De-Emphasis**

DESERIALIZER – DS92LV0412

- **Random Data Lock; No Reference Clock Required**
- **Adjustable Input Receiver Equalization**
- **EMI Minimization on Output Parallel Bus (Spread Spectrum Clock Generation and LVDS VOD Select)**

APPLICATIONS

- **Embedded Video and Display**
- **Machine Vision, Industrial Imaging, Medical Imaging**
- **Office Automation — Printers, Scanners, Copiers**
- **Security and Video Surveillance**
- **General purpose data communication**

DESCRIPTION

The DS92LV0411 (serializer) and DS92LV0412 (deserializer) chipset translates a Channel Link LVDS video interface (4 LVDS Data + LVDS Clock) into a high-speed serialized interface over a single CML pair.

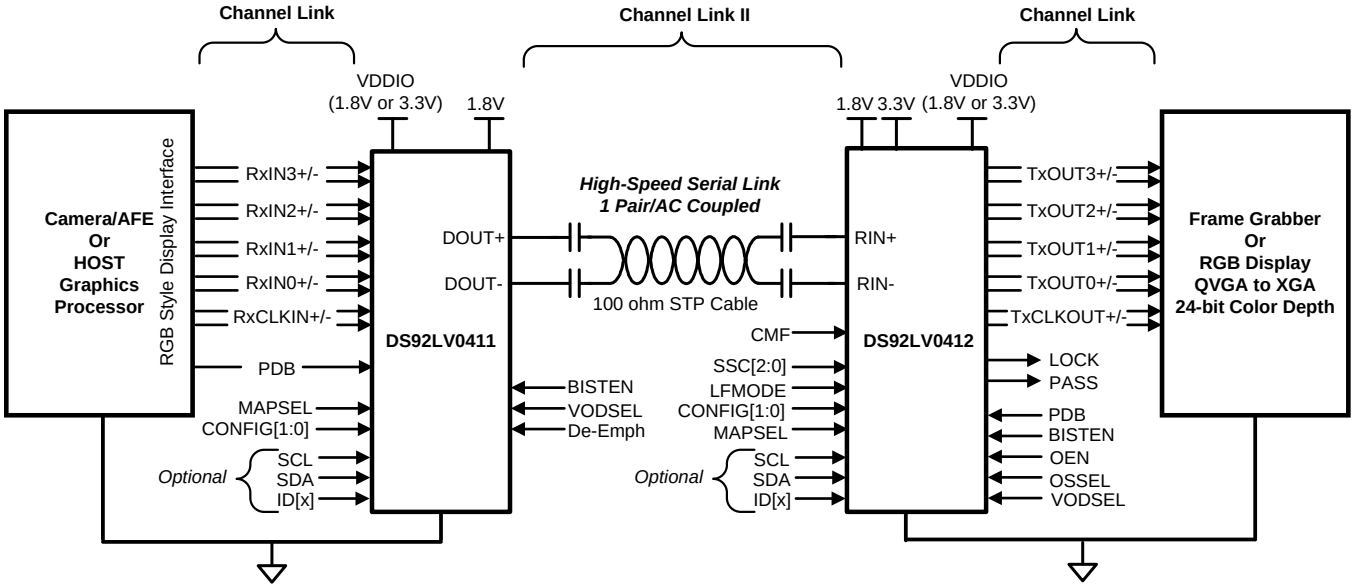
The DS92LV0411/DS92LV0412 enables applications that currently use the popular Channel Link or Channel Link style devices to seamlessly upgrade to an embedded clock interface to reduce interconnect cost or ease design challenges. The parallel LVDS interface also reduces FPGA I/O pins, board trace count and alleviates EMI issues, when compared to traditional single-ended wide bus interfaces.

Programmable transmit de-emphasis, receive equalization, on-chip scrambling and DC balancing enables longer distance transmission over lossy cables and backplanes. The Deserializer automatically locks to incoming data without an external reference clock or special sync patterns, providing easy “plug-and-go” operation.

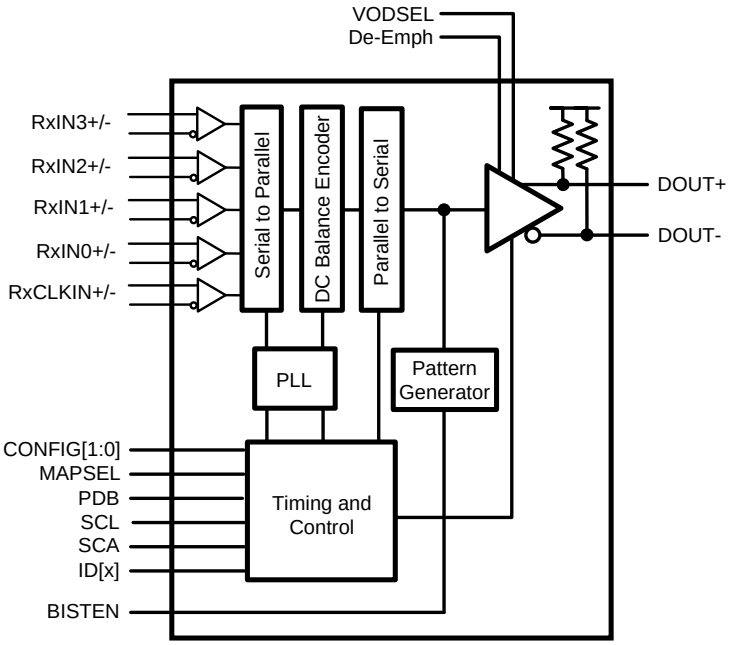
The DS92LV0411 and DS92LV0412 are programmable though an I2C interface as well as by pins. A built-in AT-SPEED BIST feature validates link integrity and may be used for system diagnostics.

The DS92LV0411 and DS92LV0412 can be used interchangeably with the DS92LV2411 or DS92LV2412. This allows designers the flexibility to connect to the host device and receiving devices with different interface types, LVDS or LVCMOS.

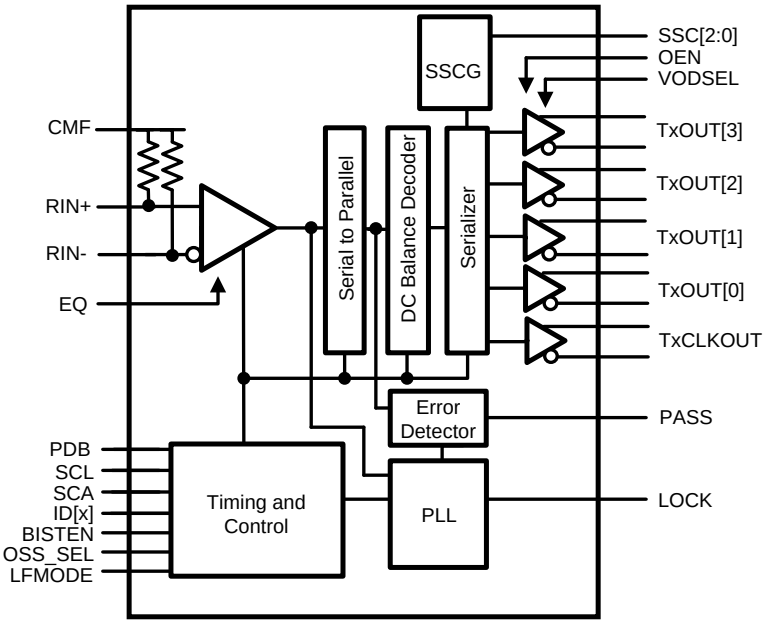
Applications Diagram



Block Diagrams



DS92LV0411



DS92LV0412

DS92LV0411 Pin Diagram

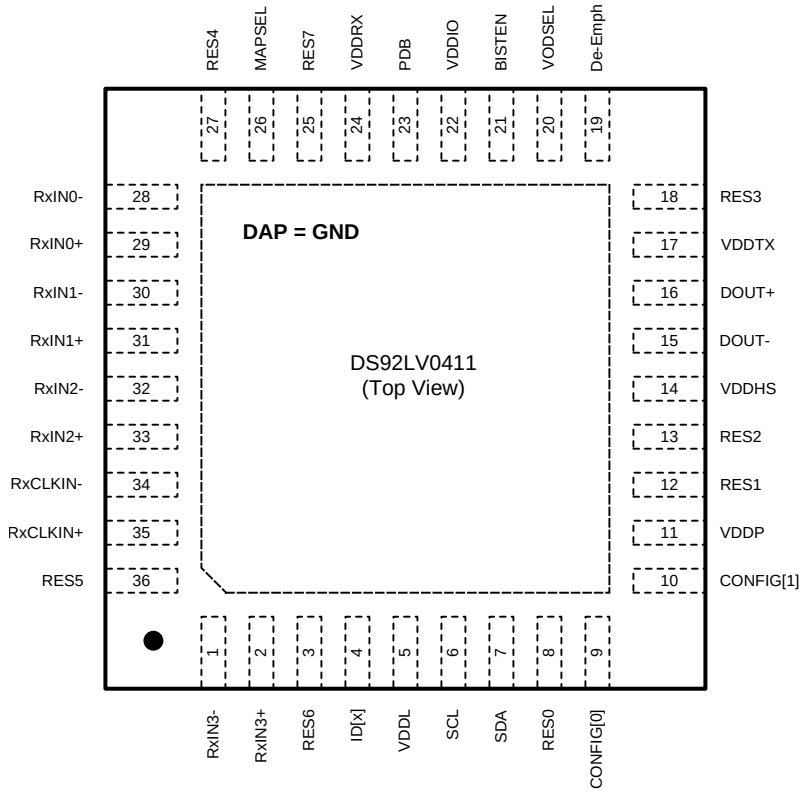


Figure 1. DS92LV0411 — Top View

Table 1. DS92LV0411 PIN DESCRIPTIONS

Pin Name	Pin #	I/O, Type	Description
Channel Link Parallel Input Interface			
RxIN[3:0]+	2, 33, 31, 29	I, LVDS	True LVDS Data Input These inputs require an external 100 Ω differential termination for standard LVDS levels.
RxIN[3:0]-	1, 34, 32, 30, 28	I, LVDS	Inverting LVDS Data Input These inputs require an external 100 Ω differential termination for standard LVDS levels.
RxCLKIN+	35	I, LVDS	True LVDS Clock Input These inputs require an external 100 Ω differential termination for standard LVDS levels.
RxCLKIN-	34	I, LVDS	Inverting LVDS Clock Input These inputs require an external 100 Ω differential termination for standard LVDS levels.
Control and Configuration			
PDB	23	I, LVCMOS w/ pull-down	Power-down Mode Input PDB = 1, Device is enabled (normal operation). Refer to POWER UP REQUIREMENTS AND PDB PIN in the Applications Information Section. PDB = 0, Device is powered down When the Device is in the power-down state, the driver outputs (DOUT+/-) are both logic high, the PLL is shutdown, IDD is minimized. Control Registers are **RESET**.
VODSEL	20	I, LVCMOS w/ pull-down	Differential Driver Output Voltage Select — Pin or Register Control VODSEL = 1, LVDS VOD is ±450 mV, 900 mVp-p (typ) — Long Cable / De-E Applications VODSEL = 0, LVDS VOD is ±300 mV, 600 mVp-p (typ)
De-Emph	19	I, Analog w/ pull-up	De-Emphasis Control — Pin or Register Control De-Emph = open (float) - disabled To enable De-emphasis, tie a resistor from this pin to GND or control via register. (See Table 5)
MAPSEL	26	I, LVCMOS w/ pull-down	Channel Link Map Select — Pin or Register Control MAPSEL = 1, MSB on RxIN3+/-. (SeeFigure 23) MAPSEL = 0, LSB on RxIN3+/-. (See Figure 22)
CONFIG[1:0]	10, 9	I, LVCMOS w/ pull-down	Operating Modes Determines the device operating mode and interfacing device. (See Table 2) CONFIG[1:0] = 00: Interfacing to DS92LV2412 or DS92LV0412, Control Signal Filter DISABLED CONFIG[1:0] = 01: Interfacing to DS92LV2412 or DS92LV0412, Control Signal Filter ENABLED CONFIG [1:0] = 10: Interfacing to DS90UR124, DS99R124 CONFIG [1:0] = 11: Interfacing to DS90C124
ID[x]	4	I, Analog	Serial Control Bus Device ID Address Select — Optional Resistor to Ground and 10 kΩ pull-up to 1.8V rail. (See Table 11)
SCL	6	I, LVCMOS	Serial Control Bus Clock Input - Optional SCL requires an external pull-up resistor to 3.3V
SDA	7	I/O, LVCMOS Open Drain	Serial Control Bus Data Input / Output - Optional SDA requires an external pull-up resistor to 3.3V
BISTEN	21	I, LVCMOS w/ pull-down	BIST Mode — Optional BISTEN = 1, BIST is enabled BISTEN = 0, BIST is disabled
RES[7:0]	25, 3, 36, 27, 18, 13, 12, 8	I, LVCMOS w/ pull-down	***Reserved*** - tie LOW
Channel Link II Serial Interface			
DOUT+	16	O, CML	True Output. The output must be AC Coupled with a 0.1 µF capacitor.
DOUT-	15	O, CML	Inverting Output. The output must be AC Coupled with a 0.1 µF capacitor.

Table 1. DS92LV0411 PIN DESCRIPTIONS (continued)

Pin Name	Pin #	I/O, Type	Description
Power and Ground(1)			
VDDL	5	Power	Logic Power, 1.8 V ±5%
VDDP	11	Power	PLL Power, 1.8 V ±5%
VDDHS	14	Power	TX High Speed Logic Power, 1.8 V ±5%
VDDTX	17	Power	**Output Driver Power, 1.8 V ±5%**
VDDRX	24	Power	RX Power, 1.8 V ±5%
VDDIO	22	Power	LVCMOS I/O Power and Channel Link I/O Power **1.8 V ±5% OR 3.3 V ±10%**
GND	DAP	Ground	DAP is the large metal contact at the bottom side, located at the center of the WQFN package. **Connect to the ground plane** (GND) with at least 9 vias.

(1) 1= HIGH, 0 = LOW. The VDD (V_{DDn} and V_{DDIO}) supply ramp should be faster than 1.5 ms with a monotonic rise. If slower then 1.5 ms then a capacitor on the PDB pin is needed to ensure PDB arrives after all the VDD have settled to the recommended operating voltage.

DS92LV0412 Pin Diagram

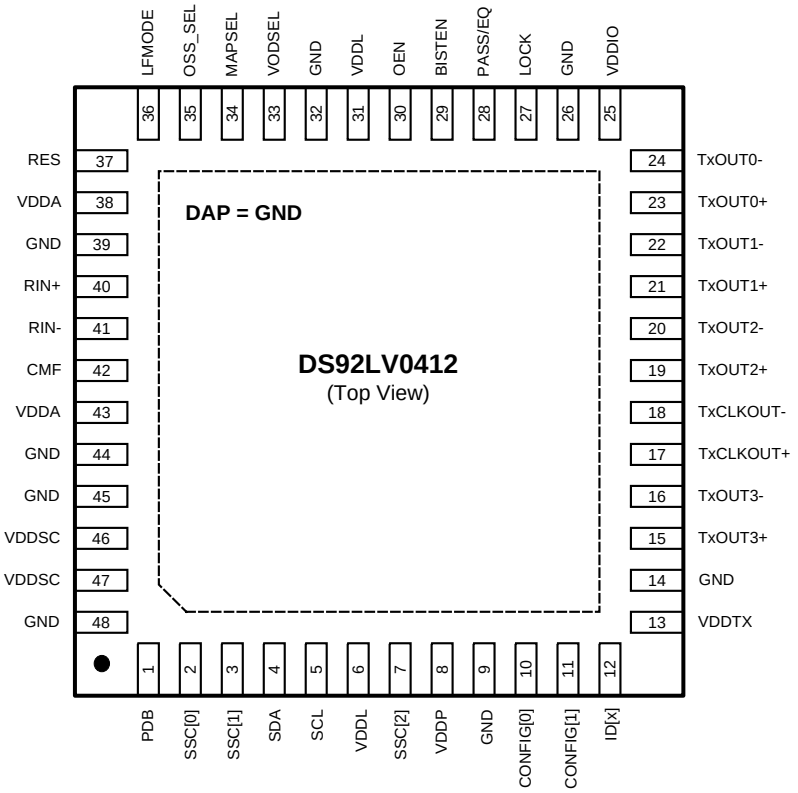


Figure 2. DS92LV0412 — Top View

DS92LV0412 PIN DESCRIPTIONS

Pin Name	Pin #	I/O, Type	Description
Channel Link II Serial Interface			
RIN+	40	I, CML	True Input. The output must be AC Coupled with a 0.1 µF capacitor.
RIN-	41	I, CML	Inverting Input. The output must be AC Coupled with a 0.1 µF capacitor.
CMF	42	I, Analog	Common Mode Filter VCM center tap is a virtual ground which can be AC-coupled to ground to increase receiver common mode noise immunity. Recommended value is 4.7µF or higher.
Channel Link Parallel Output Interface			
RxIN[3:0]+	15, 19, 21, 23	O, LVDS	True LVDS Data Output
RxIN[3:0]-	16, 20, 22, 24	O, LVDS	Inverting LVDS Data Output
RxCLKIN+	17	O, LVDS	True LVDS Clock Output
RxCLKIN-	18	O, LVDS	Inverting LVDS Clock Output
LVCMOS Outputs			
LOCK	27	O, LVCMOS	LOCK Status Output LOCK = 1, PLL is locked, output stated determined by OEN. LOCK = 0, PLL is unlocked, output states determined by OSS_SEL and OEN. (See Table 6)
Control and Configuration			
PDB	1	I, LVCMOS w/ pull-down	Power-down Mode Input PDB = 1, Device is enabled (normal operation). PDB = 0, Device is powered down and the outputs are Tri-State Control Registers are **RESET**.
VODSEL	33	I, LVCMOS w/ pull-down	Parallel LVDS Driver Output Voltage Select — Pin or Register Control VODSEL = 1, LVDS VOD is ±400 mV, 800 mVp-p (typ) — Long Cable / De-E Applications VODSEL = 0, LVDS VOD is ±250 mV, 500 mVp-p (typ)
OEN	30	I, LVCMOS w/ pull-down	Output Enable. (See Table 6)
OSS_SEL	35	I, LVCMOS w/ pull-down	Output Sleep State Select Input. (See Table 6)
LFMODE	36	I, LVCMOS w/ pull-down	SSCG Low Frequency Mode — Pin or Register Control LF_MODE = 1, low frequency mode (TxCLKOUT = 10–20 MHz) LF_MODE = 0, high frequency mode (TxCLKOUT = 20–65 MHz) SSCG not avaialble above 65 MHz.
MAPSEL	34	I, LVCMOS w/ pull-down	Channel Link Map Select — Pin or Register Control MAPSEL = 1, MSB on TxOUT3+/-. (See Figure 23) MAPSEL = 0, LSB on TxOUT3+/-. (See Figure 22)
CONFIG[1:0]	11, 10	I, LVCMOS w/ pull-down	Operating Modes Determine the device operating mode and interfacing device. (See Table 2) CONFIG[1:0] = 00: Interfacing to DS92LV2411 or DS92LV0411, Control Signal Filter DISABLED CONFIG[1:0] = 01: Interfacing to DS92LV2411 or DS92LV0411, Control Signal Filter ENABLED CONFIG [1:0] = 10: Interfacing to DS90UR241, DS99R421 CONFIG [1:0] = 11: Interfacing to DS90C241
SSC[2:0]	7, 2, 3	I, LVCMOS w/ pull-down	Spread Spectrum Clock Generation (SSCG) Range Select (See Table 9 and Table 10)
RES	37	I, LVCMOS w/ pull-down	***Reserved***
Control and Configuration — STRAP PIN			
EQ	28 [PASS]	STRAP I, LVCMOS w/ pull-down	EQ Gain Control of Channel Link II Serial Input EQ = 1, EQ gain is enabled (~13 dB) EQ = 0, EQ gain is disabled (~ 1.625 dB)

DS92LV0412 PIN DESCRIPTIONS (continued)

Pin Name	Pin #	I/O, Type	Description
Optional BIST Mode			
BISTEN	29	I, LVCMOS w/ pull-down	BIST Mode — Optional BISTEN = 1, BIST is enabled BISTEN = 0, BIST is disabled
PASS	28	O, LVCMOS	PASS Output (BIST Mode) — Optional PASS =1, no errors detected PASS = 0, errors detected Leave open if unused. Route to a test point (pad) recommended.
Optional Serial Bus Control			
ID[x]	12	I, Analog	Serial Control Bus Device ID Address Select — Optional Resistor to Ground and 10 kΩ pull-up to 1.8V rail. (See Table 11)
SCL	5	I, LVCMOS Open Drain	Serial Control Bus Clock Input - Optional SCL requires an external pull-up resistor to 3.3V.
SDA	4	I/O, LVCMOS Open Drain	Serial Control Bus Data Input / Output - Optional SDA requires an external pull-up resistor 3.3V.
Power and Ground(1)			
VDDL	6, 31	Power	Logic Power, 1.8 V ±5%
VDDA	38, 43	Power	Analog Power, 1.8 V ±5%
VDDP	8	Power	PLL Power, 1.8 V ±5%
VDDSC	46, 47	Power	SSC Generator Power, 1.8 V ±5%. Power must be connected to these pins regardless if the SSCG feature is used or not.
VDDTX	13	Power	**Channel Link LVDS Parallel Output Power, 3.3 V ±10%**
VDDIO	25	Power	LVCMOS I/O Power and Channel Link I/O Power **1.8 V ±5% OR 3.3 V ±10%**
GND	9, 14, 26, 32, 39, 44, 45, 48	Ground	Ground
DAP	DAP	Ground	DAP is the large metal contact at the bottom side, located at the center of the WQFN package. **Connect to the ground plane** (GND) with at least 9 vias.

(1) 1= HIGH, 0 = LOW. The VDD (V_{DDn} and V_{DDIO}) supply ramp should be faster than 1.5 ms with a monotonic rise. If slower then 1.5 ms then a capacitor on the PDB pin is needed to ensure PDB arrives after all the VDD have settled to the recommended operating voltage.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

Supply Voltage – V_{DDn} (1.8V)	−0.3V to +2.5V
Supply Voltage – V_{DDIO}	−0.3V to +4.0V
Supply Voltage – V_{DDTX} (1.8V, Ser))	−0.3V to +2.5V
Supply Voltage – V_{DDTX} (3.3V, Des)	−0.3V to +4.0V
LVCMOS I/O Voltage	−0.3V to (V_{DDIO} + 0.3V)
LVDS Input Voltage	−0.3V to (V_{DDIO} + 0.3V)
LVDS Output Voltage	−0.3V to (V_{DDTX} + 0.3V)
CML Driver Output Voltage	−0.3V to (V_{DDn} + 0.3V)
Receiver Input Voltage	−0.3V to (V_{DD} + 0.3V)
Junction Temperature	+150°C
Storage Temperature	−65°C to +150°C
36L WQFN Package	
Maximum Power Dissipation Capacity at 25°C	
Derate above 25°C	1/ θ_{JA}°C/W
θ_{JA}(with 9 thermal via)	27.4 °C/W
θ_{JC}(with 9 thermal via)	4.5 °C/W
48L WQFN Package	
Maximum Power Dissipation Capacity at 25°C	
Derate above 25°C	1/ θ_{JA}°C/W
θ_{JA}(with 9 thermal via)	27.7 °C/W
θ_{JC}(with 9 thermal via)	3.0 °C/W
ESD Rating (IEC, powered-up only), R_D = 330Ω, C_S = 150 pF	
Air Discharge (D_{OUT}+, D_{OUT}-, R_{IN}+, R_{IN}-)	≥±30 kV
Contact Discharge (D_{OUT}+, D_{OUT}-, R_{IN}+, R_{IN}-)	≥±8 kV
ESD Rating (HBM)	≥±8 kV
ESD Rating (CDM)	≥±1.25 kV
ESD Rating (MM)	≥±250 V
For soldering specifications: http://www.ti.com/lit/SNOA549	

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{DDn})	1.71	1.8	1.89	V
Supply Voltage (V_{DDTX_Ser})	1.71	1.8	1.89	V
Supply Voltage (V_{DDTX_Des})	3.0	3.3	3.6	V
LVCMOS Supply Voltage (V_{DDIO})	1.71	1.8	1.89	V
OR				
LVCMOS Supply Voltage (V_{DDIO})	3.0	3.3	3.6	V
Operating Free Air Temperature (T_A)	−40	+25	+85	°C
RxCLKIN/TxCLKOUT Clock Frequency	5		50	MHz
Supply Noise (1)			100	mV_{P-P}

(1) Supply noise testing was done with minimum capacitors on the PCB. A sinusoidal signal is AC coupled to the V_{DDn} (1.8V) supply with amplitude = 100 mVp-p measured at the device V_{DDn} pins. Bit error rate testing of input to the Ser and output of the Des with 10 meter cable shows no error when the noise frequency on the Ser is less than 750 kHz. The Des on the other hand shows no error when the noise frequency is less than 400 kHz.

DC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (1)(2)(3)(4)(5)

Symbol	Parameter	Conditions		Pin/Freq.	Min	Typ	Max	Units
DS92LV0411 LVCMOS INPUT DC SPECIFICATIONS								
V_{IH}	High Level Input Voltage	V_{DDIO} = 3.0 to 3.6V		PDB, VODSEL, MAPSEL, CONFIG[1:0], BISTEN	2.2		V_{DDIO}	V
		V_{DDIO} = 1.71 to 1.89V			0.65* V_{DDIO}		V_{DDIO}	V
V_{IL}	Low Level Input Voltage	V_{DDIO} = 3.0 to 3.6V			GND		0.8	V
		V_{DDIO} = 1.71 to 1.89V			GND		0.35* V_{DDIO}	V
I_{IN}	Input Current	V_{IN} = 0V or V_{DDIO}	V_{DDIO} = 3.0 to 3.6V		−15	±1	+15	µA
			V_{DDIO} = 1.7 to 1.89V		−15	±1	+15	µA
DS92LV0412 LVCMOS I/O DC SPECIFICATIONS								
V_{IH}	High Level Input Voltage	V_{DDIO} = 3.0 to 3.6V		PDB, VODSEL, OEN, MAPSEL, LFMODE, SSC[2:0], BISTEN	2.2		V_{DDIO}	V
		V_{DDIO} = 1.71 to 1.89V			0.7* V_{DDIO}		V_{DDIO}	V
V_{IL}	Low Level Input Voltage	V_{DDIO} = 3.0 to 3.6V			GND		0.8	V
		V_{DDIO} = 1.71 to 1.89V			GND		0.3* V_{DDIO}	V
I_{IN}	Input Current	V_{IN} = 0V or V_{DDIO}	V_{DDIO} = 3.0 to 3.6V		−15	±1	+15	µA
			V_{DDIO} = 1.7 to 1.89V		−10	±1	+10	µA

(1) The Electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
(2) Typical values represent most likely parametric norms at V_{DD} = 1.8V, V_{DDIO} = 3.3V, Ta = +25 °C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.
(3) Current into device pins is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except VOD, ΔVOD, VTH and VTL which are differential voltages.
(4) Specification is ensured by characterization and is not tested in production.
(5) Specification is ensured by design and is not tested in production.

DC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.(1)(2)(3)(4)(5)

Symbol	Parameter	Conditions		Pin/Freq.	Min	Typ	Max	Units
V_{OH}	High Level Output Voltage	V_{DDIO} = 3.3V I_{OH} = -2 mA		LOCK, PASS	V_{DDIO} – 0.25	V_{DDIO}		V
		V_{DDIO} = 1.8V I_{OH} = -2 mA			V_{DDIO} – 0.2	V_{DDIO}		
V_{OL}	Low Level Output Voltage	V_{DDIO} = 3.3 V or 1.8V I_{OL} = +0.5 mA			GND		0.2	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V	V_{DDIO} = 3.0 to 3.6 V			-45		mA
			V_{DDIO} = 1.71 to 1.89V			-13		
I_{OZ}	Tri-State Output Current(6)	PDB = 0V, OSS_SEL = 0V, V_{OUT} = 0V or V_{DDIO}	V_{DDIO} = 3.0 to 3.6 V		-10		+10	µA
			V_{DDIO} = 1.71 to 1.89V		-15		+15	
DS92LV0411 CHANNEL LINK PARALLEL LVDS RECEIVER DC SPECIFICATIONS								
V_{TH}	Differential Threshold High Voltage	V_{CM} = 1.2V, (See Figure 3)		RxIN[3:0]+/-, RxCLKIN+/-			+100	mV
V_{TL}	Differential Threshold Low Voltage				−100			
$\|V_{ID}\|$	Differential Input Voltage Swing				200		600	mV
V_{CM}	Common Mode Voltage	V_{DDIO} = 3.3V			0	1.2	2.4	V
		V_{DDIO} = 1.8V			0	1.2	1.55	
I_{IN}	Input Current				−15	±1	+15	µA
DS92LV0412 CHANNEL LINK PARALLEL LVDS DRIVER DC SPECIFICATIONS								
$\|V_{OD}\|$	Differential Output Voltage	R_L = 100Ω	VODSEL = L	TxCLKOUT-, TxOUT[3:0]+, TxOUT[3:0]-	100	250	400	mV
			VODSEL = H		200	400	600	mV
V_{ODp-p}	Differential Output Voltage A – B		VODSEL = L			500		mV p-p
			VODSEL = H			800		mV p-p
ΔV_{OD}	Output Voltage Unbalance					4	50	mV
V_{OS}	Offset Voltage		VODSEL = L		1.0	1.2	1.5	V
			VODSEL = H			1.2		V
ΔV_{OS}	Offset Voltage Unbalance					1	50	mV
I_{OS}	Output Short Circuit Current	V_{OUT} = GND				-5		mA
I_{OZ}	Output Tri-State Current(6)	OEN = GND, V_{OUT} = V_{DDTX}, or GND			-10		+10	µA

(6) When the device output is at Tri-State the Deserializer will lose PLL lock. Resynchronization / Relock must occur before data transfer require t_{PLD}

DC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.(1)(2)(3)(4)(5)

Symbol	Parameter	Conditions		Pin/Freq.	Min	Typ	Max	Units
DS92LV0411 Channel Link II CML DRIVER DC SPECIFICATIONS								
V_{OD}	Differential Output Voltage	R_L = 100Ω, De-emph = disabled, (SeeFigure 5)	VODSEL = 0	DOUT+, DOUT-	±225	±300	±375	mV
			VODSEL = 1		±350	±450	±550	
V_{ODp-p}	Differential Output Voltage (DOUT+) – (DOUT-)		VODSEL = 0			600		mV p-p
			VODSEL = 1			900		mV p-p
ΔV_{OD}	Output Voltage Unbalance	R_L = 100Ω, De-emph = disabled, VODSEL = L				1	50	mV
V_{OS}	Offset Voltage – Single-ended At TP A & B, (SeeFigure 4)	R_L = 100Ω, De-emph = disabled	VODSEL = 0			1.65		V
			VODSEL = 1			1.575		V
ΔV_{OS}	Offset Voltage Unbalance Single-ended At TP A & B, (SeeFigure 4)	R_L = 100Ω, De-emph = disabled				1		mV
I_{OS}	Output Short Circuit Current	DOUT+/- = 0V, De-emph = disabled	VODSEL = 0			−35		mA
R_T	Internal Termination Resistor				80		120	Ω
DS92LV0412 CHANNEL LINK II CML RECEIVER DC SPECIFICATIONS								
V_{TH}	Differential Input Threshold High Voltage	V_{CM} = +1.2V (Internal V_{BIAS})		RIN+, RIN-			+50	mV
V_{TL}	Differential Input Threshold Low Voltage				-50		mV	
V_{CM}	Common mode Voltage, Internal V_{BIAS}				1.2		V	
R_T	Input Termination			80	100	120	Ω	
DS92LV0411 SUPPLY CURRENT								
I_{DDT1}	Supply Current (includes load current) R_L = 100Ω, f = 50 MHz	Checker Board Pattern, De-emph = 3 kΩ, VODSEL = H, (See Figure 18)	V_{DD}= 1.89V	All V_{DD} pins		80	90	mA
I_{DDIOT1}			V_{DDIO}= 1.89V	V_{DDIO}		3	5	mA
			V_{DDIO} = 3.6V			10	13	mA
I_{DDT2}		Checker Board Pattern, De-emph = 6 kΩ, VODSEL = L, (See Figure 18)	V_{DD}= 1.89V	All V_{DD} pins		75	85	mA
I_{DDIOT2}			V_{DDIO}= 1.89V	V_{DDIO}		3	5	mA
			V_{DDIO} = 3.6V			10	13	mA
I_{DDZ}	Supply Current Power-down	PDB = 0V , (All other LVCMOS Inputs = 0V)	V_{DD}= 1.89V	All V_{DD} pins		60	1000	µA
I_{DDIOZ}			V_{DDIO}= 1.89V	V_{DDIO}		0.5	10	µA
			V_{DDIO} = 3.6V			1	30	µA
DS92LV0412 SUPPLY CURRENT								
I_{DD1}	Supply Current (Includes load current) 50 MHz Clock	Checker Board Pattern, VODSEL = H, SSCG [2:0] = 000	V_{DDn} = 1.89 V	All $V_{DD(1:8)}$ pins		85	95	mA
I_{DDTX1}			V_{DDTX} = 3.6 V	V_{DDTX}		40	50	mA
I_{DDIO1}			V_{DDIO} = 1.89 V	V_{DDIO}		0.3	0.8	mA
			V_{DDIO} = 3.6 V			0.8	1.5	mA

DC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.(1)(2)(3)(4)(5)

Symbol	Parameter	Conditions		Pin/Freq.	Min	Typ	Max	Units
I_{DD2}	Supply Current (Includes load current) 50 MHz Clock	Checker Board Pattern, VODSEL = H, SSCG [2:0] = 111	V_{DDn} = 1.89 V	All $V_{DD(1:8)}$ pins		95		mA
I_{DDTX2}			V_{DDTX} = 3.6 V	V_{DDTX}		40		mA
I_{DDIO2}			V_{DDIO} = 1.89 V	V_{DDIO}		0.3		mA
			V_{DDIO} = 3.6 V			0.8		mA
I_{DDZ}	Supply Current Power Down	PDB = 0V, All other LVCMOS Inputs = 0V	V_{DD} = 1.89 V	All $V_{DD(1:8)}$ pins		0.15	2	mA
I_{DDTXZ}			V_{DDTX} = 3.6 V	V_{DDTX}		0.01	0.1	mA
I_{DDIOZ}			V_{DDIO} = 1.89 V	V_{DDIO}		0.01	0.08	mA
			V_{DDIO} = 3.6V			0.01	0.08	mA

Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DS92LV0411 CHANNEL LINK PARALLEL LVDS INPUT						
t_{RSP0}	Receiver Strobe Position-bit 0	RxCLKIN = 50 MHz, RxIN[3:0] (See Figure 7)	0.66	1.10	1.54	ns
t_{RSP1}	Receiver Strobe Position-bit 1		2.86	3.30	3.74	ns
t_{RSP2}	Receiver Strobe Position-bit 2		5.05	5.50	5.93	ns
t_{RSP3}	Receiver Strobe Position-bit 3		7.25	7.70	8.13	ns
t_{RSP4}	Receiver Strobe Position-bit 4		9.45	9.90	10.33	ns
t_{RSP5}	Receiver Strobe Position-bit 5		11.65	12.10	12.53	ns
t_{RSP6}	Receiver Strobe Position-bit 6		13.85	14.30	14.73	ns
DS92LV0412 CHANNEL LINK PARALLEL LVDS OUTPUT						
t_{LHT}	Low to High Transition Time	R_L = 100Ω		0.3	0.6	ns
t_{THLT}	High to Low Transition Time			0.3	0.6	ns
t_{DCCJ}	Cycle-to-Cycle Output Jitter(1)	TxCLKOUT± = 5 MHz		900	2100	ps
		TxCLKOUT± = 50 MHz		75	125	ps
t_{TTP1}	Transmitter Pulse Position for bit 1	5 – 50 MHz		1		UI(2)
t_{TTP0}	Transmitter Pulse Position for bit 0			2		UI
t_{TTP6}	Transmitter Pulse Position for bit 6			3		UI
t_{TTP5}	Transmitter Pulse Position for bit 5			4		UI
t_{TTP4}	Transmitter Pulse Position for bit 4			5		UI
t_{TTP3}	Transmitter Pulse Position for bit 3			6		UI
t_{TTP2}	Transmitter Pulse Position for bit 2			7		UI
Δt_{TTP}	Offset Transmitter Pulse Position (bit 6— bit 0)	50 MHz		<+0.1		UI
t_{DD}	Delay-Latency			142*T	143*T	ns
t_{TPDD}	Power Down Delay Active to OFF	50 MHz		7	12	ns
t_{TXZR}	Enable Delay OFF to Active	50 MHz		40	55	ns

(1) t_{DCCJ} is the maximum amount of jitter between adjacent clock cycles.
(2) UI – Unit Interval is equivalent to one serialized data bit width (1UI = 1 / 28*PCLK). The UI scales with PCLK frequency.

Switching Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DS92LV0411 Channel Link II CML OUTPUT						
t_{HLT}	Output Low-to-High Transition Time (See Figure 5)	R_L = 100Ω, De-emphasis = disabled, VODSEL = 0		200		ps
		R_L = 100Ω, De-emphasis = disabled, VODSEL = 1		200		ps
t_{HLT}	Output High-to-Low Transition Time (See Figure 6)	R_L = 100Ω, De-emphasis = disabled, VODSEL = 0		260		ps
		R_L = 100Ω, De-emphasis = disabled, VODSEL = 1		200		ps
t_{XZD}	Ouput Active to OFF Delay (See Figure 11)			5	15	ns
t_{PLD}	PLL Lock Time(3), (See Figure 9)	R_L = 100Ω		1.5	10	ms
t_{SD}	Delay - Latency, (See Figure 12)	R_L = 100Ω		147*T	148*T	ns
t_{DJIT}	Output Total Jitter (See Figure 14)	R_L = 100Ω, De-Emph = disabled, RANDOM pattern, RxCLKIN = 43 and 50 MHz		0.26		UI
λ_{STXBW}	Jitter Transfer Function -3 dB Bandwidth	RxCLKIN = 43 MHz		2.2		MHz
		RxCLKIN = 50 MHz		2.6		
δ_{STX}	Jitter Transfer Function Peaking	RxCLKIN = 43 MHz		1		dB
		RxCLKIN = 50 MHz		1		
DS92LV0412 CHANNEL LINK II CML INPUT						
t_{DDLT}	Lock Time	SSCG[2:0] = 000, 5 MHz		7		ms
		SSCG[2:0] = 111, 5 MHz		14		ms
		SSCG[2:0] = 000, 50 MHz		6		ms
		SSCG[2:0] = 111, 50 MHz		8		ms
t_{IJIT}	Input Jitter Tolerance	EQ = OFF SSCG[2:0] = 000 TxCLKOUT± = 50 MHz Input Jitter Frequency < 2 MHz		>0.9		UI
		EQ = OFF SSCG[2:0] = 000 TxCLKOUT± = 50 MHz Input Jitter Frequency >6 MHz		>0.5		UI
DS92LV0412 LVCMOS OUTPUTS						
t_{CLH}	Low to High Transition Time	C_L = 8 pF LOCK pin, PASS pin		5	15	ns
t_{CHL}	High to Low Transition Time			5	15	ns
t_{PASS}	BIST PASS Valid Time, BISTEN = 1	PASS pin 5 MHz		570	580	ns
		50 MHz		50	65	ns
DS92LV0412 SSCG MODE						
t_{DEV}	Spread Spectrum Clocking Deviation Frequency	TxCLKOUT = 5 – 50 MHz, SSC[2:0] = ON	±0.5		±2	%
t_{MOD}	Spread Spectrum Clocking Modulation Frequency	TxCLKOUT = 5 – 50 MHz, SSC[2:0] = ON	8		100	kHz

(3) t_{PLD} is the time required by the device to obtain lock when exiting power-down state with an active RxCLKIN.

Recommended Timing for the Serial Control Bus

Over recommended operating supply and temperature ranges unless otherwise specified. (Figure 20)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{SCL}	SCL Clock Frequency	Standard Mode	>0		100	kHz
		Fast Mode	>0		400	kHz
t_{LOW}	SCL Low Period	Standard Mode	4.7			µs
		Fast Mode	1.3			µs
t_{HIGH}	SCL High Period	Standard Mode	4.0			µs
		Fast Mode	0.6			µs
$t_{HD:STA}$	Hold time for a start or a repeated start condition	Standard Mode	4.0			µs
		Fast Mode	0.6			µs
$t_{SU:STA}$	Set Up time for a start or a repeated start condition	Standard Mode	4.7			µs
		Fast Mode	0.6			µs
$t_{HD:DAT}$	Data Hold Time		0		3.45	µs
		Fast Mode	0		0.9	µs
$t_{SU:DAT}$	Data Set Up Time	Standard Mode	250			µs
		Fast Mode	100			µs
$t_{SU:STO}$	Set Up Time for STOP Condition	Standard Mode	4.0			µs
		Fast Mode	0.6			µs
t_{BUF}	Bus Free Time Between STOP and START	Standard Mode	4.7			µs
		Fast Mode	1.3			µs
t_r	SCL & SDA Rise Time	Standard Mode			1000	ns
		Fast Mode			300	ns
t_f	SCL & SDA Fall Time	Standard Mode			300	ns
		Fast Mode			300	ns

DC and AC Serial Control Bus Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Input High Level	SDA and SCL V_{DDIO} = 3.3V	0.7* V_{DDIO}		V_{DDIO}	V
V_{IL}	Input Low Level Voltage	SDA and SCL V_{DDIO} = 3.3V	GND		0.3* V_{DDIO}	V
V_{HY}	Input Hysteresis	V_{DDIO} = 3.3V		>50		mV
V_{OL}		SDA, IOL = 3mA V_{DDIO} = 3.3V	0		0.36	V
I_{in}		SDA or SCL, Vin = 3.3V or GND	-10		+10	µA
t_R	SDA RiseTime – READ	SDA, RPU = X, Cb ≤ 400pF, (See Figure 20)		430		ns
t_F	SDA Fall Time – READ			20		ns
$t_{SU;DAT}$	Set Up Time – READ	See Figure 20		560		ns
$t_{HD;DAT}$	Hold Up Time – READ	See Figure 20		615		ns
t_{SP}	Input Filter			50		ns
C_{in}	Input Capacitance	SDA or SCL		<5		pF

AC Timing Diagrams and Test Circuits

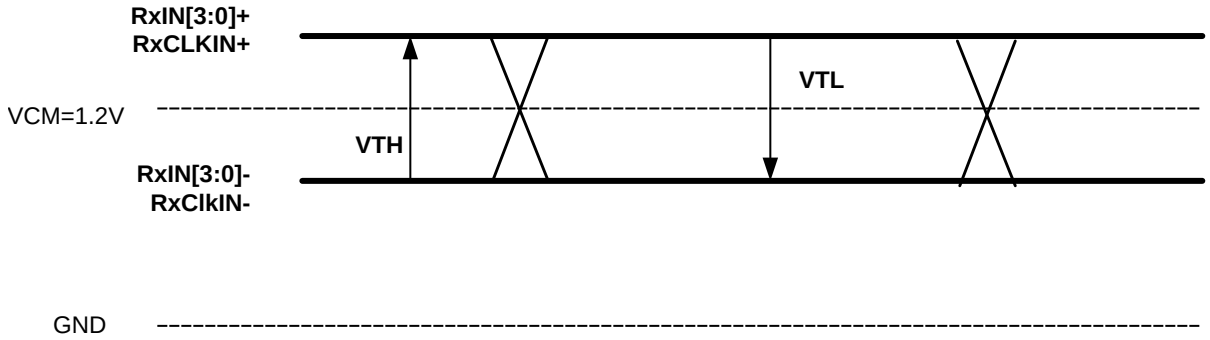


Figure 3. Channel Link DC VTH/VTL Definition

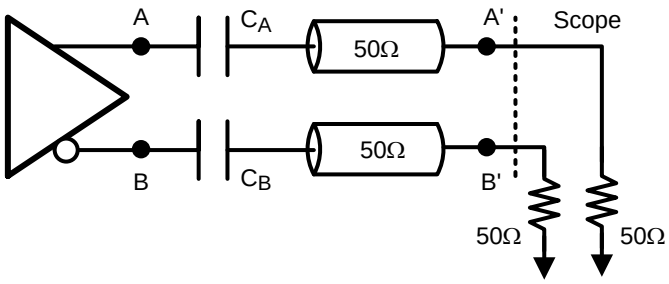


Figure 4. DS92LV0411 Output Test Circuit

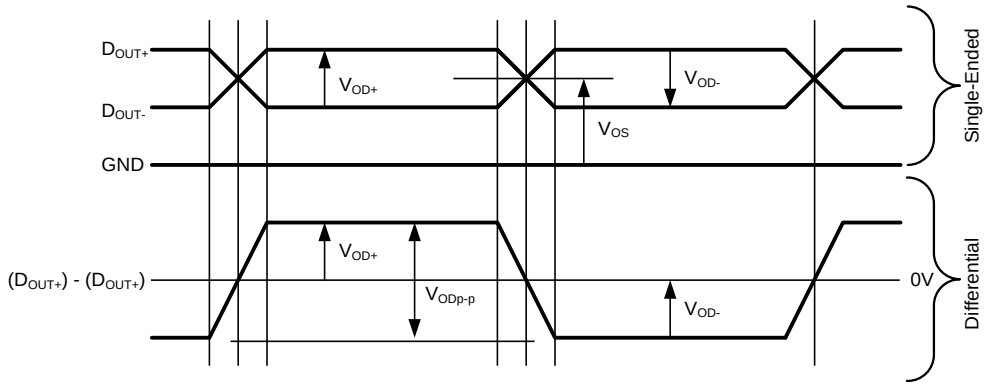


Figure 5. Channel Link II Single-ended and Differential Waveforms

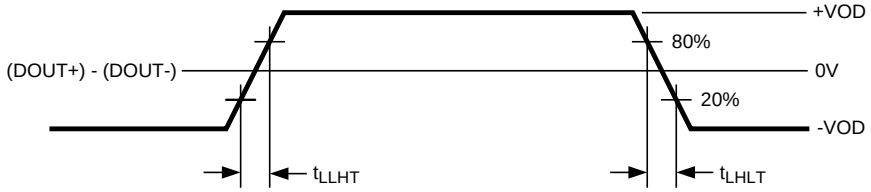


Figure 6. DS92LV0411 Output Transition Times

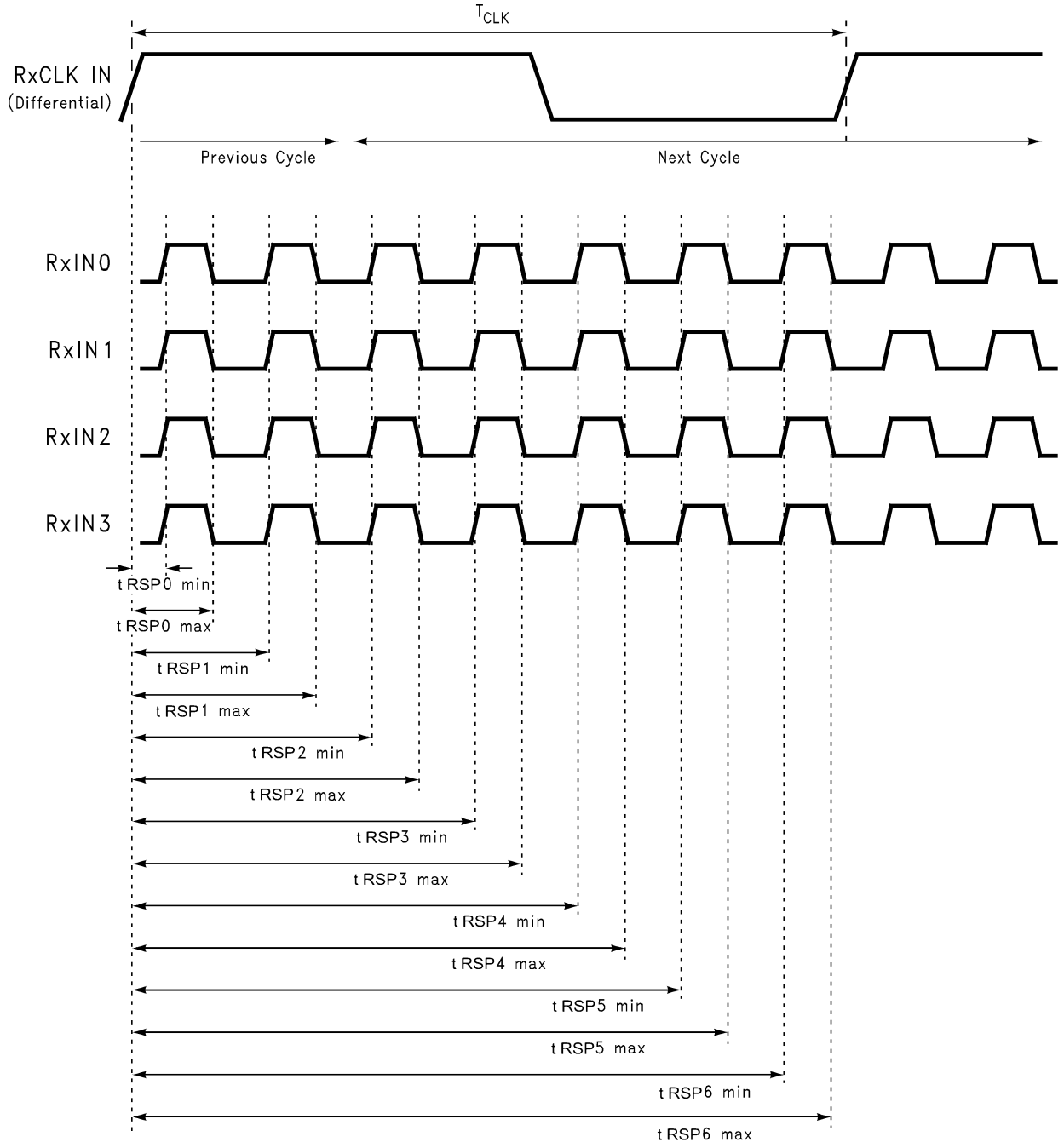


Figure 7. DS92LV0411 LVDS Receiver Strobe Positions

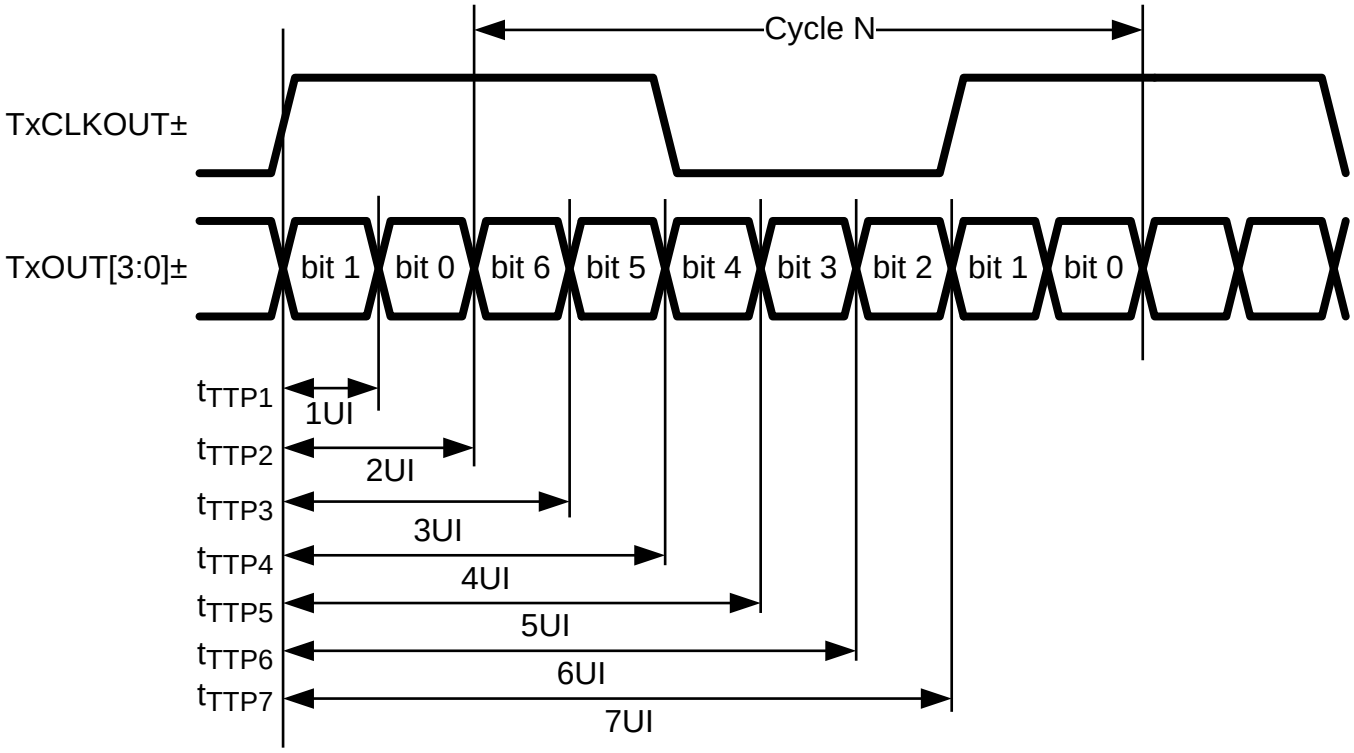


Figure 8. DS92LV0412 LVDS Transmitter Pulse Positions

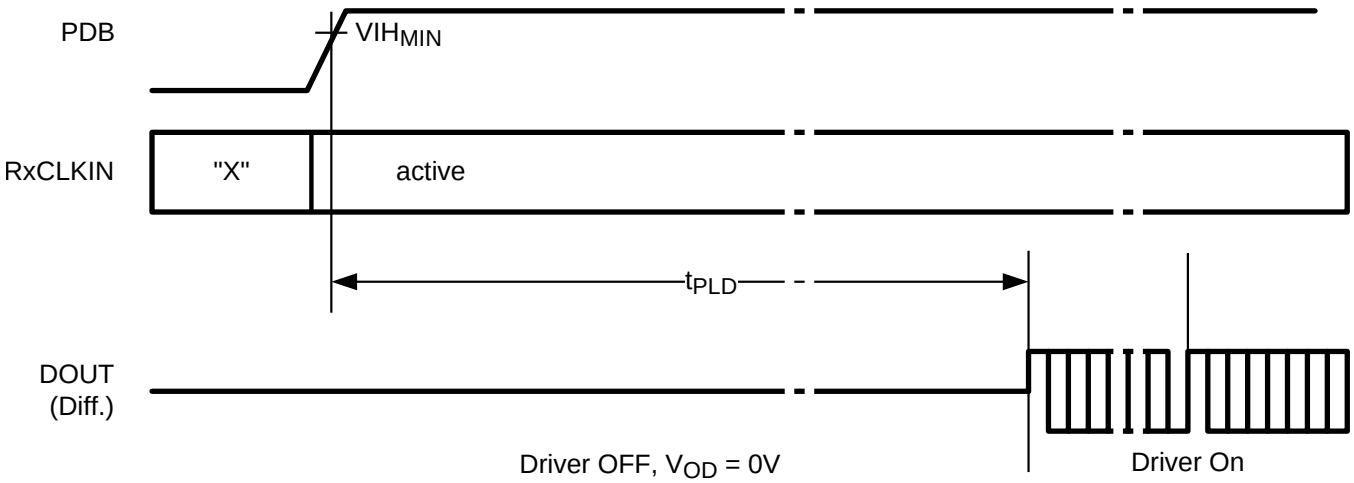


Figure 9. DS92LV0411 Lock Time

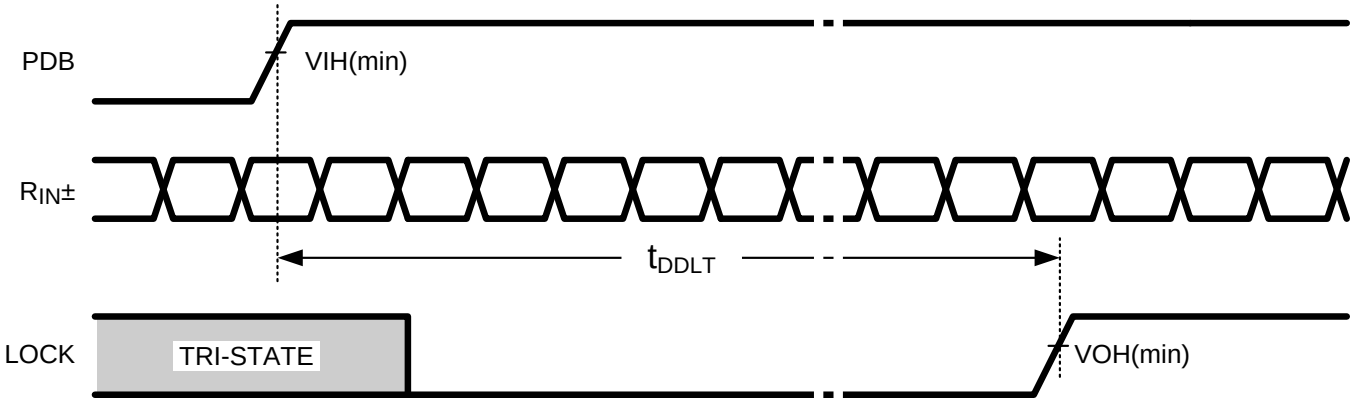


Figure 10. DS92LV0412 Lock Time

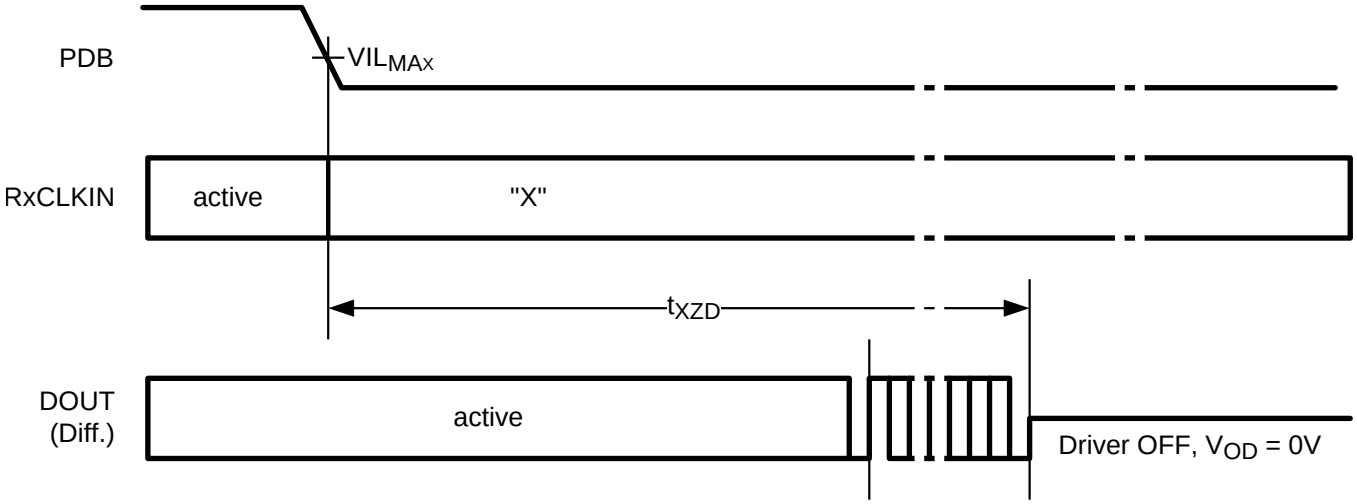


Figure 11. DS92LV0411 Disable Time

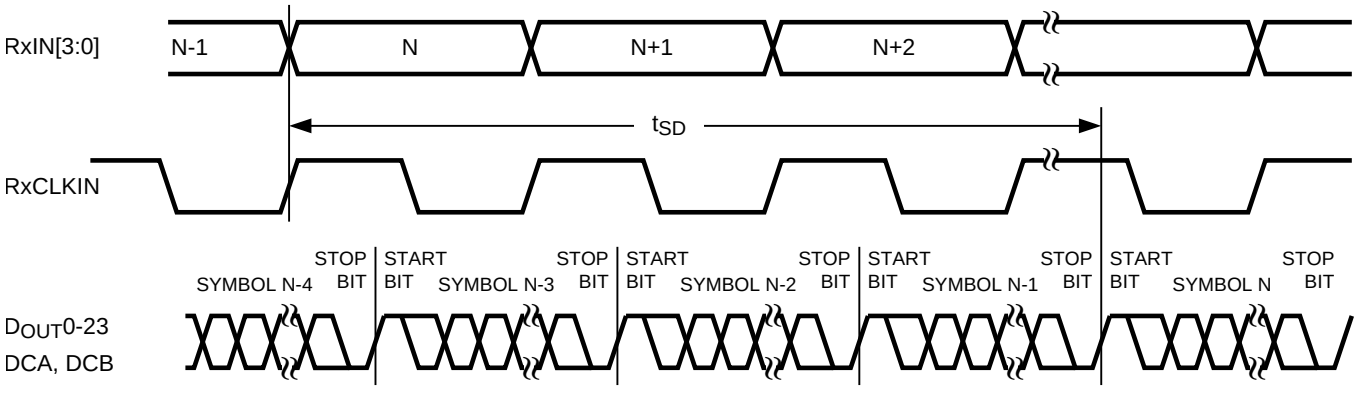


Figure 12. DS92LV0411 Latency Delay

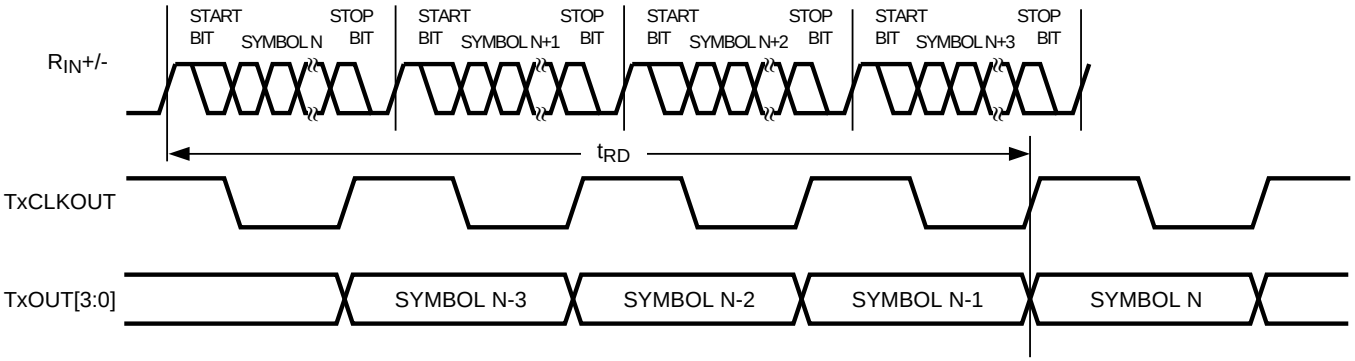


Figure 13. DS92LV0412 Latency Delay

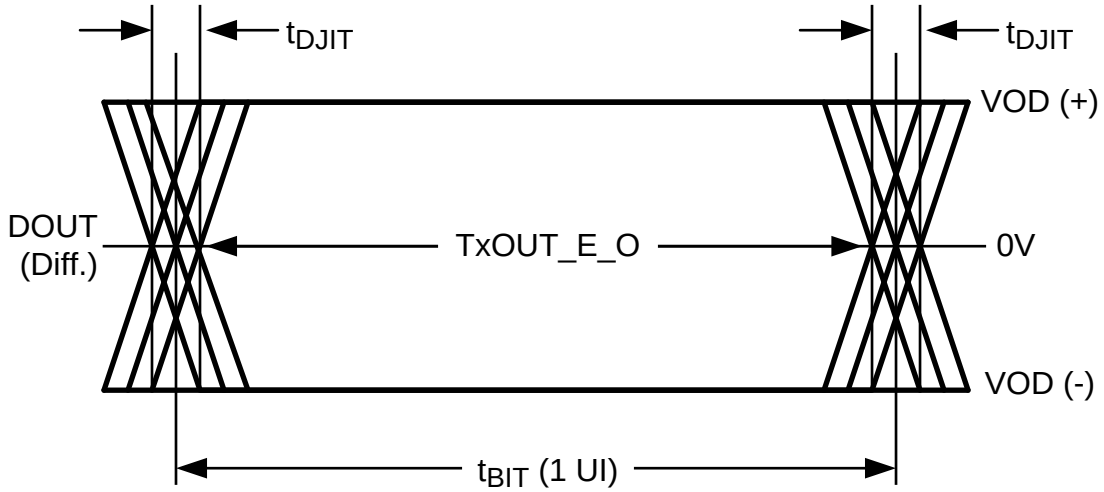
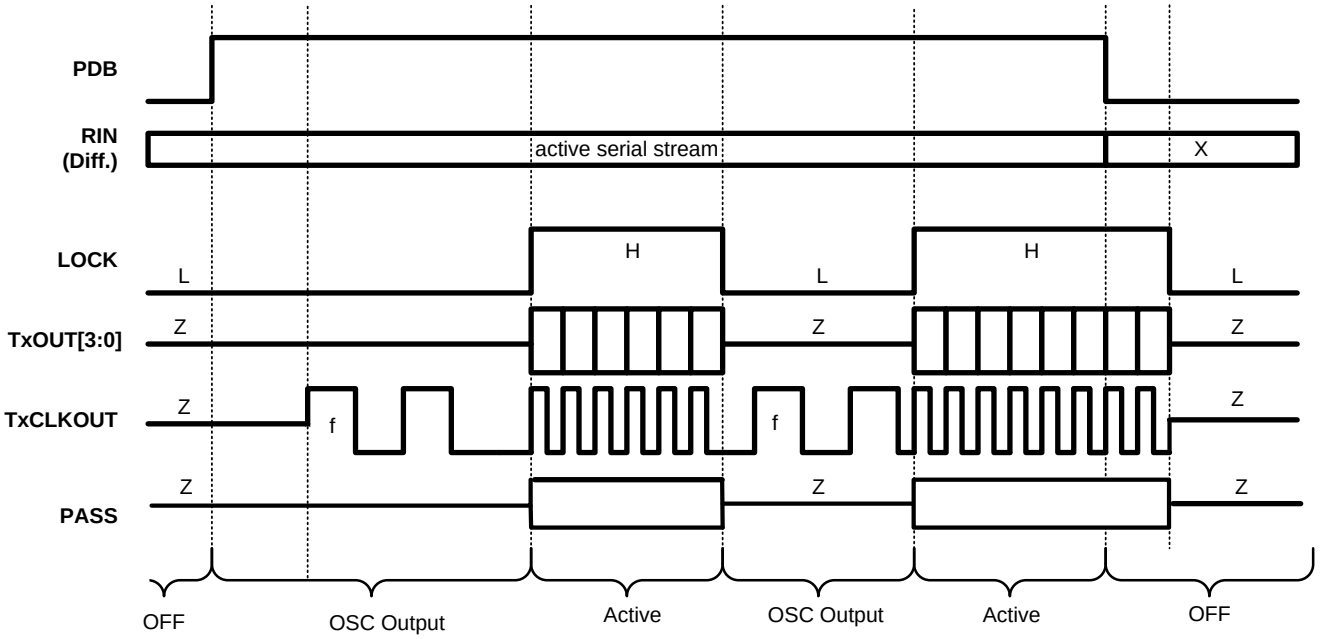


Figure 14. DS92LV0411 Output Jitter



CONDITIONS: OEN = H, OSS_SEL = H, and OSC_SEL not equal to 000.

Figure 15. DS92LV0412 Output State Diagram

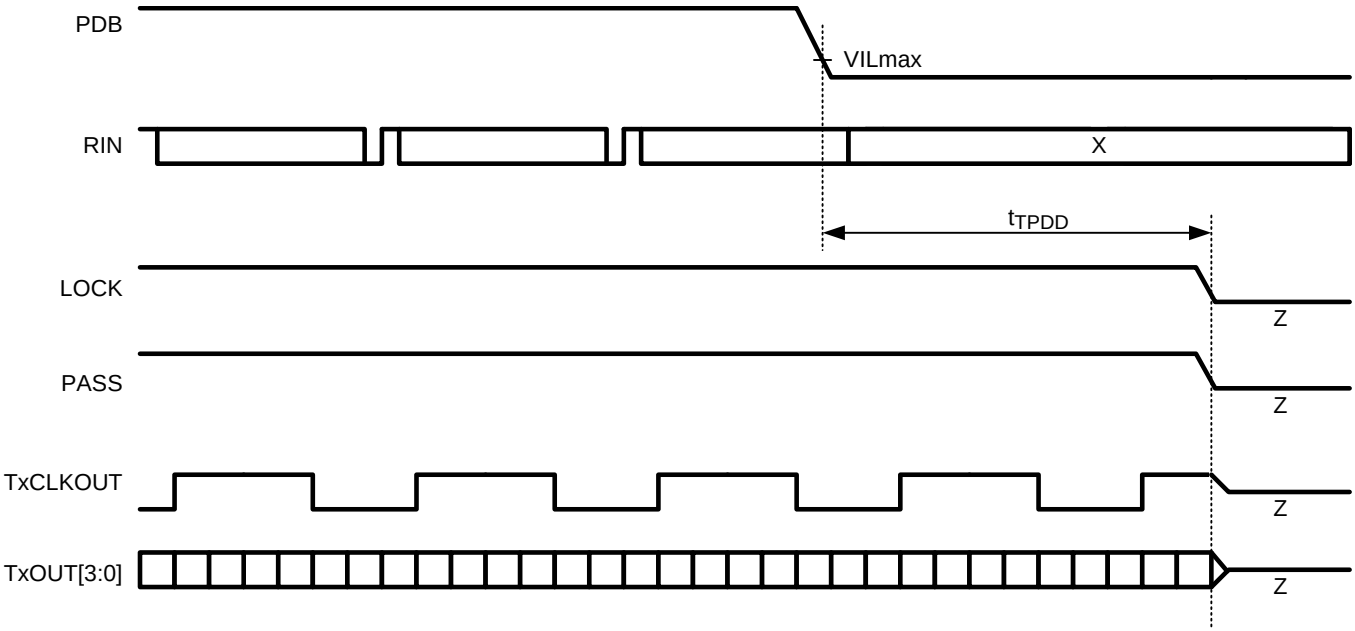


Figure 16. DS92LV0412 Power Down Delay

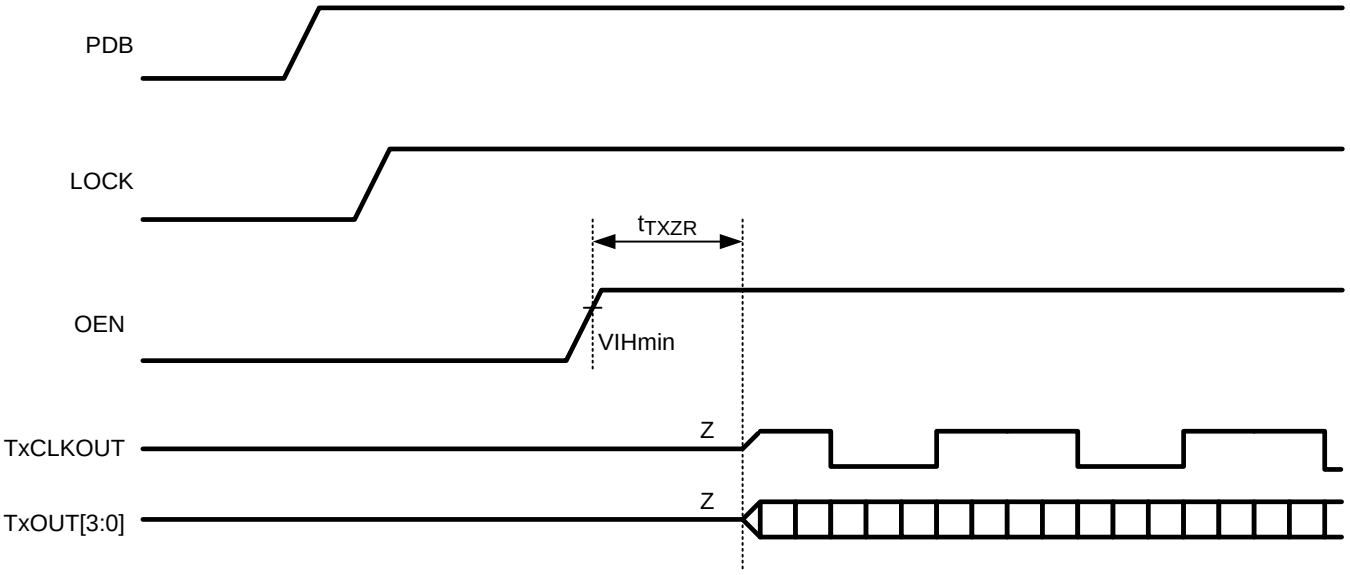


Figure 17. DS92LV0412 Enable Delay

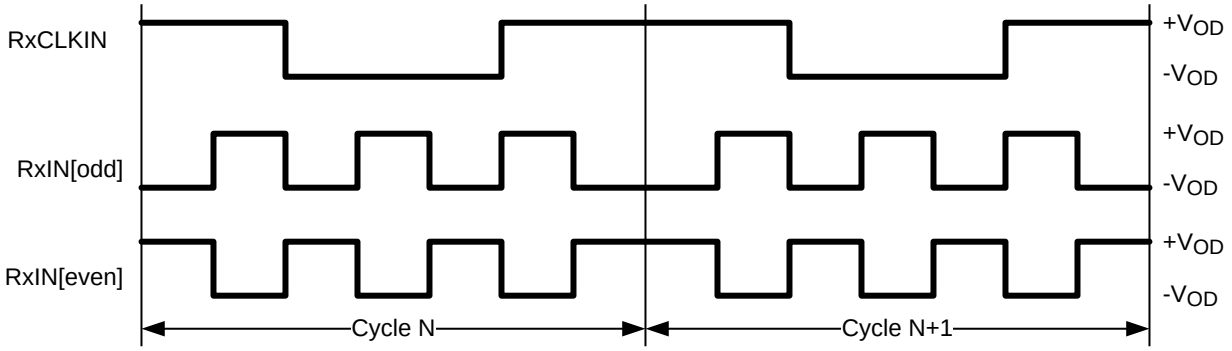


Figure 18. Checkerboard Data Pattern

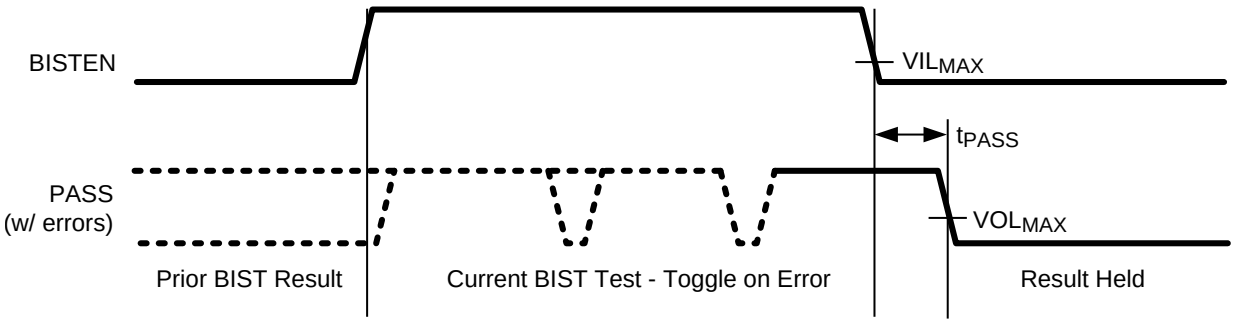


Figure 19. BIST PASS Waveform

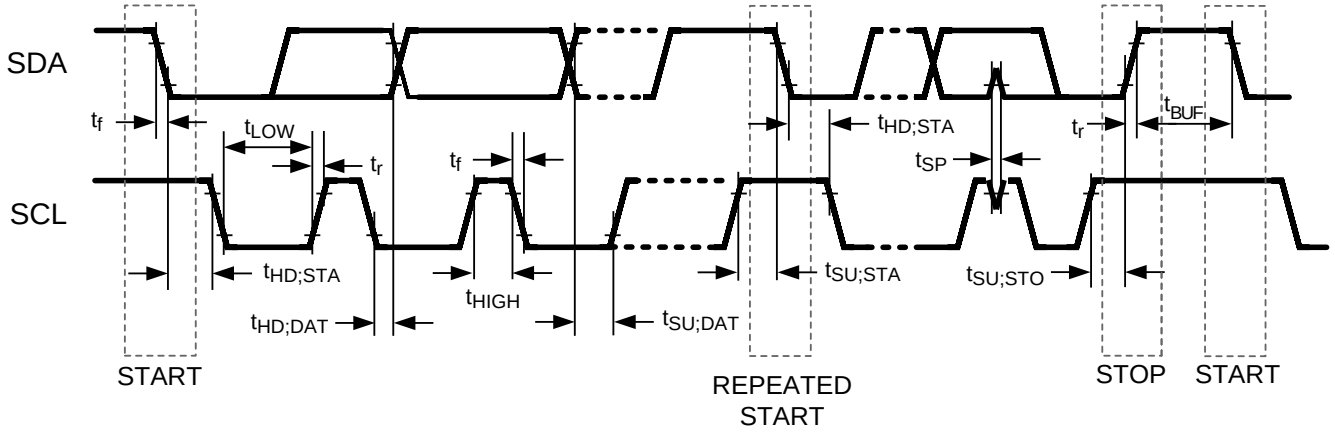


Figure 20. Serial Control Bus Timing Diagram

FUNCTIONAL DESCRIPTION

The DS92LV0411 / DS92LV0412 chipset transmits and receives 24-bits of data and 3 control signals, formatted as Channel Link LVDS data, over a single serial CML pair operating at 140 Mbps to 1.4 Gbps serial line rate. The serial stream contains an embedded clock, video control signals and is DC-balance to enhance signal quality and supports AC coupling.

The Des can attain lock to a data stream without the use of a separate reference clock source, which simplifies system complexity and overall cost. The Des also synchronizes to the Ser regardless of the data pattern, delivering true automatic “plug and lock” performance. It can lock to the incoming serial stream without the need of special training patterns or sync characters. The Des recovers the clock and data by extracting the embedded clock information, validating and then deserializing the incoming data stream providing a parallel Channel Link LVDS bus to the display, ASIC, or FPGA.

The DS92LV0411 / DS92LV0412 chipset can operate with up to 24 bits of raw data with three slower speed control bits encoded within the serial data stream. For applications that require less the maximum 24 pclk speed bit spaces, the user will need to ensure that all unused bit spaces or parallel LVDS channels are set to valid logic states, as all parallel lanes and 27 bit spaces will always be sampled.

Block Diagrams for the chipset are shown at the beginning of this datasheet.

PARALLEL LVDS DATA TRANSFER

The DS92LV0411/DS92LV0412 can be configured to accept/transmit 24-bit data with 2 different mapping schemes: The normal Channel Link LVDS format (MSBs on LVDS channel 3) can be selected by configuring the MAPSEL pin to HIGH. See Figure 15 for the normal Channel Link LVDS mapping. An alternate mapping scheme is available (LSBs on LVDS channel 3) by configuring the MAPSEL pin to LOW. See Figure 16 for the alternate LVDS mapping. The mapping schemes can also be selected by register control.

The alternate mapping scheme is useful in some applications where the receiving system, typically a display, requires that the LSBs for the 24-bit color data be sent on LVDS channel 3.

SERIAL DATA TRANSFER

The DS92LV0411 transmits a 24–bit word of data in the following format: C1 and C0 represent the embedded clock in the serial stream. C1 is always HIGH and C0 is always LOW. b[23:0] contain the scrambled RGB data, plus two additional bits for encoding overhead. The control signals (VS,HS,DE) are also encoded within these two additional bits. This coding scheme is generated by the DS92LV0411 and decoded by the paring deserializer, such as the DS92LV0412, automatically.

The DS92LV0412 receives a 24 bit word of data in the format as described above. It also synchronizes to the serializer regardless of the data pattern, delivering true automatic “plug and lock” performance. it can lock to the incoming serial stream without the need for special training patterns or sync characters. The DS92LV0412 recovers the clock and data by extracting the embedded clock information, validating and then deserializing the incoming data stream.

Figure 21 illustrates the serial stream per PCLK cycle.

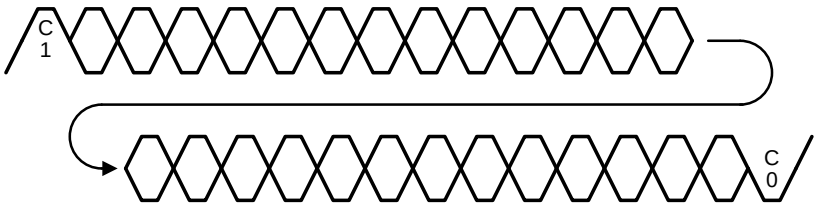


Figure 21. Channel Link II Serial Stream

OPERATING MODES AND BACKWARD COMPATIBILITY (CONFIG[1:0])

The DS92LV0411 and DS92LV0412 are backward compatible with previous generations of Ser/Des. Configuration modes are provided for backwards compatibility with the DS90C241/DS90C124 and also the DS90UR241/DS90UR124 and DS99R241/DS99R124 by setting the respective mode with the CONFIG[1:0] pins as shown in Table 2 and Table 3. The selection also determine whether the Video Control Signal filter feature is enabled or disabled in Normal mode. Backward compatibility modes are selectable through the control pins only. The Control Signal Filter can be selected by pin or through register programming.

Table 2. DS92LV0411 Configuration Modes

CONFIG1	CONFIG0	Mode	Des Device
L	L	Normal Mode, Control Signal Filter disabled	DS92LV0412, DS92LV2412
L	H	Normal Mode, Control Signal Filter enabled	DS92LV0412, DS92LV2412
H	L	Backwards Compatible	DS90UR124, DS99R124
H	H	Backwards Compatible	DS90C124

Table 3. DS92LV0412 Configuration Modes

CONFIG1	CONFIG0	Mode	Des Device
L	L	Normal Mode, Control Signal Filter disabled	DS92LV0411, DS92LV2411
L	H	Normal Mode, Control Signal Filter enabled	DS92LV0411, DS92LV2411
H	L	Backwards Compatible	DS90UR241, DS99R421
H	H	Backwards Compatible	DS90C241

BIT MAPPING SELECT

The DS92LV0411 and DS92LV0412 can be configured to accept the LVDS parallel data with 2 different mapping schemes: LSBs on RxIN[3] shown in Figure 22 or MSBs on RxIN[3] shown in Figure 23. The user selects which mapping scheme is controlled by MAPSEL pin or by Register.

NOTE

While the LVDS interface has 28 bits defined, only 27 bits are recovered by the Ser and sent to the Des. This supports 24 bit RGB plus the three video control signals. The 28th bit is not sampled, sent or recovered.

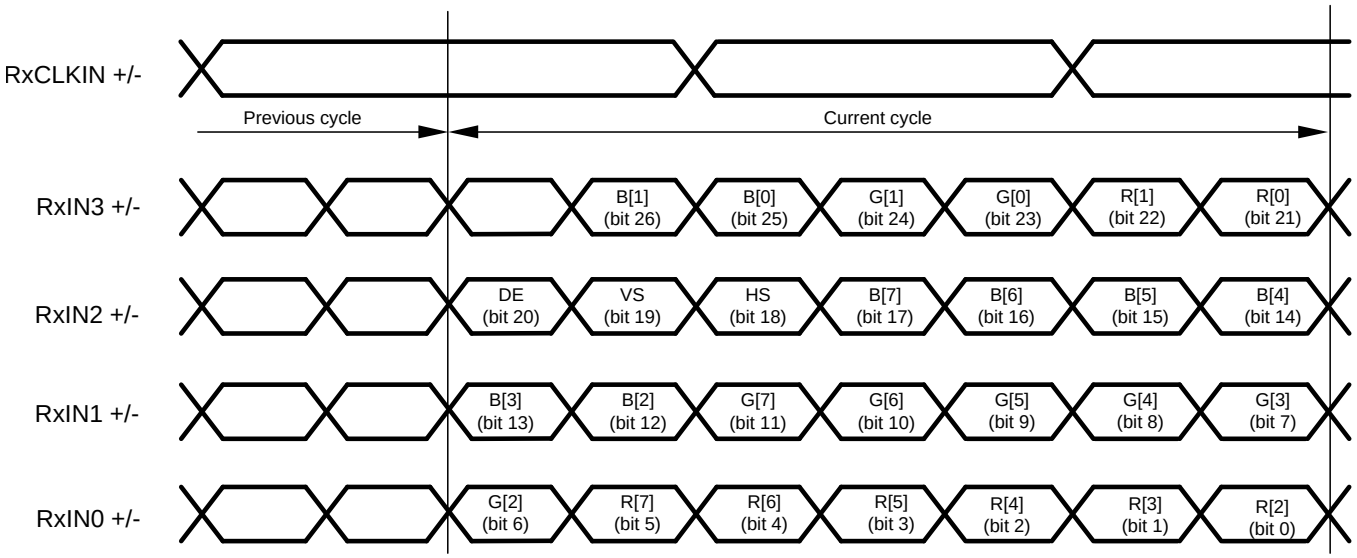


Figure 22. 8–bit Channel Link Mapping: LSB's on RxIN3

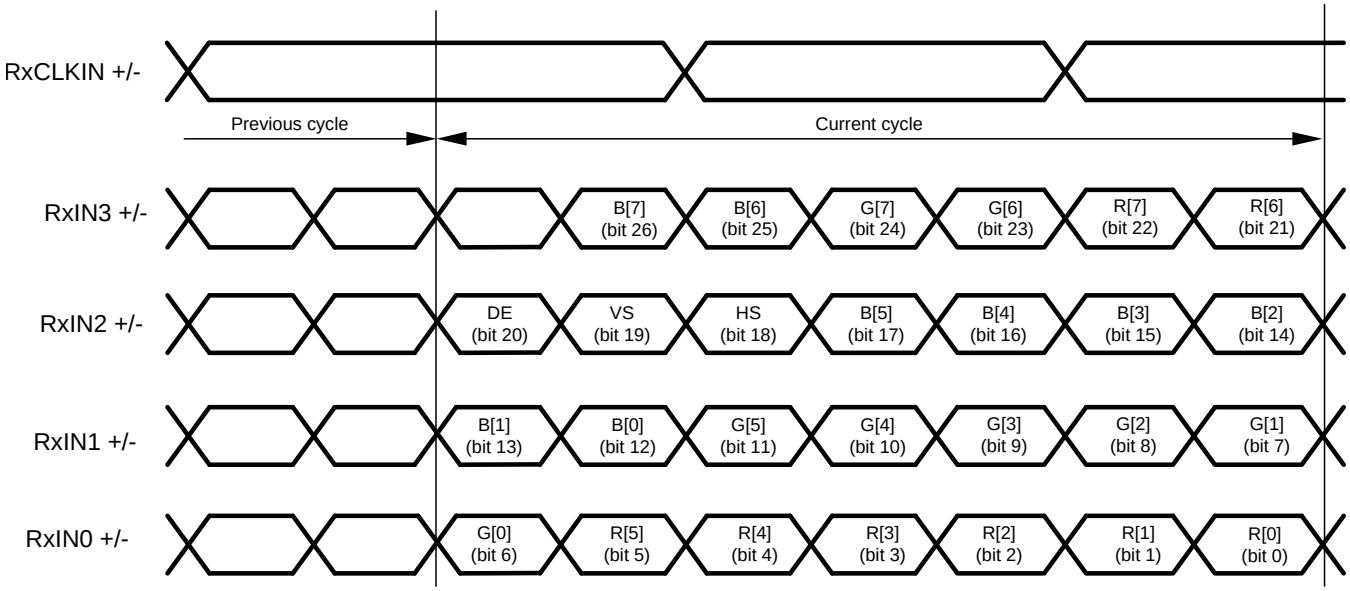


Figure 23. 8–bit Channel Link Mapping: MSB's on RxIN3

VIDEO CONTROL SIGNAL FILTER

The three control bits can be used to communicate any low speed signal. The most common use for these bits is in the display or machine vision applications. In a display application these bits are typically assigned as: Bit 26 – DE, Bit 24 – HS, Bit 25 – VS. In the machine vision standard, Camera Link, these bits are typically assigned: Bit 26 – DVAL, Bit 24 – LVAL, Bit 25 – FVAL.

When operating the devices in Normal Mode, the Video Control Signals (DE, HS, VS) have the following restrictions:

- Normal Mode with Control Signal Filter Enabled:
  - DE and HS — Only 2 transitions per 130 clock cycles are transmitted, the transition pulse must be 3 PCLK or longer.
- Normal Mode with Control Signal Filter Disabled:
  - DE and HS — Only 2 transitions per 130 clock cycles are transmitted, no restriction on minimum transition pulse.
- VS — Only 1 transition per 130 clock cycles are transmitted, minimum pulse width is 130 clock cycles.

Video Control Signals are defined as low frequency signals with limited transitions. Glitches of a control signal can cause a visual display error. This feature allows for the chipset to validate and filter out any high frequency noise on the control signals. See Figure 24.

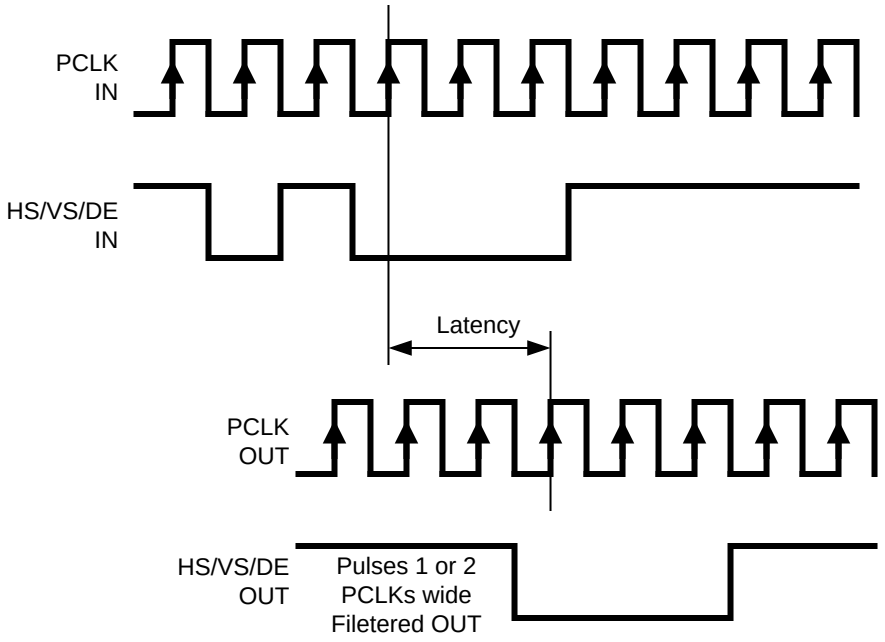


Figure 24. Video Control Signal Filter Wavefrom

SERIALIZER FUNCTIONAL DESCRIPTION

The Ser converts a Channel Link LVDS clock and data bus (4 LVDS data channels + 1 LVDS clock) to a single serial output data stream, and also acts as a signal generator for the chipset Built In Self Test (BIST) mode. The device can be configured via external pins or through the optional serial control bus. The Ser features enhanced signal quality on the link by supporting: a selectable VOD level, a selectable de-emphasis signal conditioning and also the Channel Link II data coding that provides randomization, scrambling, and DC Balanacing of the data. The Ser includes multiple features to reduce EMI associated with display data transmission. This includes the randomization and scrambling of the serial data and also the system spread spectrum clock support. The Ser features power saving features with a sleep mode, auto stop clock feature, and optional 1.8 V or 3.3V I/O compatibility.

See also the Functional Description of the chipset's serial control bus and BIST modes.

EMI REDUCTION FEATURES

Data Randomization & Scrambling

Channel Link II Ser / Des feature a 3 step encoding process which enables the use of AC coupled interconnects and also helps to manage EMI. The serializer first passes the parallel data through a scrambler which randomizes the data. The randomized data is then DC balanced. The DC balanced and randomized data then goes through a bit shuffling circuit and is transmitted out on the serial line. This encoding process helps to prevent static data patterns on the serial stream. The resulting frequency content of the serial stream ranges from the parallel clock frequency to the nyquist rate. For example, if the Ser / Des chip set is operating at a parallel clock frequency of 50 MHz, the resulting frequency content of serial stream ranges from 50 MHz to 700 MHz (50 MHz *28 bits = 1.4 Gbps / 2 = 700 MHz).

Ser — Spread Spectrum Compatibility

The RxCLKIN of the Channel Link input is capable of tracking spread spectrum clocking (SSC) from a host source. The RxCLKIN will accept spread spectrum tracking up to 35kHz modulation and ±0.5, ±1 or ±2% deviations (center spread). The maximum conditions for the RxCLKIN input are: a modulation frequency of 35kHz and amplitude deviations of ±2% (4% total).

SER — INTEGRATED SIGNAL CONDITIONING FEATURES

Ser — VOD Select (VODSEL)

The DS92LV0411 differential output voltage may be increased by setting the VODSEL pin High. When VODSEL is Low, the DC VOD is at the standard (default) level. When VODSEL is High, the DC VOD is increased in level. The increased VOD is useful in extremely high noise environments and also on extra long cable length applications. When using de-emphasis it is recommended to set VODSEL = H to avoid excessive signal attenuation especially with the larger de-emphasis settings. This feature may be controlled by the external pin or by register.

Table 4. Ser — Differential Output Voltage

Input	Effect	
VODSEL	VOD mV	VOD mVp-p
H	±450	900
L	±300	600

Ser — De-Emphasis (De-Emph)

The De-Emph pin controls the amount of de-emphasis beginning one full bit time after a logic transition that the device drives. This is useful to counteract loading effects of long or lossy cables. This pin should be left open for standard switching currents (no de-emphasis) or if controlled by register. De-emphasis is selected by connecting a resistor on this pin to ground, with R value between 0.5 kΩ to 1 MΩ, or by register setting. When using De-Emphasis it is recommended to set VODSEL = H.

Table 5. De-Emphasis Resistor Value

Resistor Value (kΩ)	De-Emphasis Setting
Open	Disabled
0.6	- 12 dB
1.0	- 9 dB
2.0	- 6 dB
5.0	- 3 dB

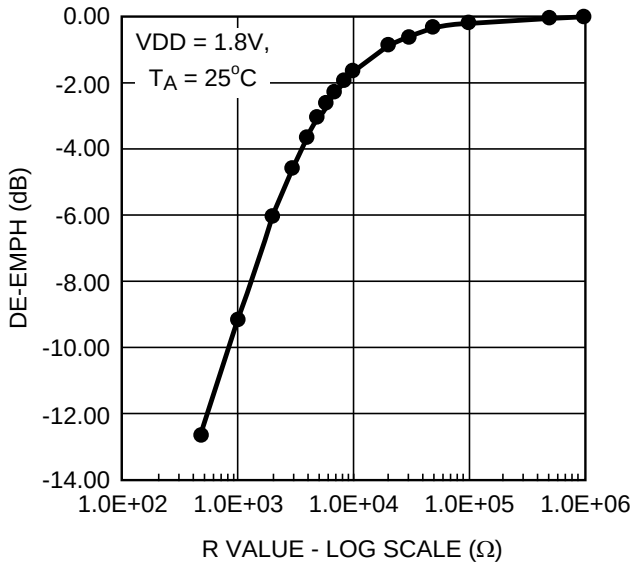


Figure 25. De-Emph vs. R value

POWER SAVING FEATURES

Ser — Power Down Feature (PDB)

The DS92LV0411 has a PDB input pin to ENABLE or POWER DOWN the device. This pin is controlled by the host and is used to save power, disabling the link when the display is not needed. In the POWER DOWN mode, the high-speed driver outputs are both pulled to VDD and present a 0V VOD state. Note – in POWER DOWN, the optional Serial Bus Control Registers are **RESET**.

Ser — Stop Clock Feature

The DS92LV0411 will enter a low power SLEEP state when the RxCLKIN is stopped. A STOP condition is detected when the input clock frequency is less than 3 MHz. The clock should be held at a static Low or high state. When the RxCLKIN starts again, the device will then lock to the valid input RxCLKIN and then transmits the RGB data to the desializer. Note – in STOP CLOCK SLEEP, the optional Serial Bus Control Registers values are **RETAINED**.

1.8V or 3.3V VDDIO Operation

The DS92LV0411 parallel control pin bus can operate with 1.8 V or 3.3 V levels (V_{DDIO}) for host compatibility. The 1.8 V levels will offer a system power savings.

OPTIONAL SERIAL BUS CONTROL

Please see the following section on the Optional Serial Bus Control Interface.

OPTIONAL BIST MODE

Please see the following section on the chipset BIST Mode for details.

Deserializer Functional Description

The Des converts a single input serial data stream to a wide parallel output bus, and also provides a signal check for the chipset Built In Self Test (BIST) mode. The device can be configured via external pins and strap pins or through the optional serial control bus. The Des features enhance signal quality on the link with an integrated equalizer on the serial input and Channel Link II data encoding which provides randomization, scrambling, and DC balanacing of the data. The Des includes multiple features to reduce EMI associated with data transmission. This includes the randomization and scrambling of the data, the output spread spectrum clock generation (SSCG) support. The Des features power saving features with a power down mode, and optional LVCMOS (1.8 V) interface compatibility.

OSCILLATOR OUTPUT — OPTIONAL

The DS92LV0412 provides an optional TxCLKOUT when the input clock (serial stream) has been lost. This is based on an internal oscillator. The frequency of the oscillator may be selected. This feature may be controlled by the external pin or through the registers.

Clock-DATA RECOVERY STATUS FLAG (LOCK), OUTPUT ENABLE (OEN) and OUTPUT STATE SELECT (OSS_SEL)

When PDB is driven HIGH, the CDR PLL begins locking to the serial input, LOCK is LOW and the Channel Link interface state is determined by the state of the OSS_SEL pin.

After the DS92LV0412 completes its lock sequence to the input serial data, the LOCK output is driven HIGH, indicating valid data and clock recovered from the serial input is available on the Channel Link outputs. The TxCLKOUT output is held at its current state at the change from OSC_CLK (if this is enabled via OSC_SEL) to the recovered clock (or vice versa). Note that the Channel Link outputs may be held in an inactive state (Tri-State®) through the use of the Output Enable pin (OEN).

If there is a loss of clock from the input serial stream, LOCK is driven LOW and the state of the outputs are based on the OSS_SEL setting (configuration pin or register).

Table 6. Des Output State Table

INPUTS			OUTPUTS	
PDB	**OEN**	**OSS_SEL**	**LOCK**	**OTHER OUTPUTS**
L	X	X	X	TxCLKOUT is Tri-State TxOUT[3:0] are Tri-State PASS is Tri-State
L	X	L	L	TxCLKOUT is Tri-State TxOUT[3:0] are Tri-State PASS is HIGH
H	L	H	L	TxCLKOUT is Tri-State TxOUT[3:0] are Tri-State PASS is Tri-State
H	H	H	L	TxCLKOUT is Tri-State or OSC Output through Register bit TxOUT[3:0] are Tri-State PASS is Tri-State
H	L	X	H	TxCLKOUT is Tri-State TxOUT[3:0] are Tri-State PASS is HIGH
H	H	X	H	TxCLKOUT is Active TxOUT[3:0] are Active PASS is Active (Normal operating mode)

DES — INTEGRATED SIGNAL CONDITIONING FEATURES — DES

Des — Common Mode Filter Pin (CMF) — Optional

The Des provides access to the center tap of the internal termination. A capacitor may be placed on this pin for additional common-mode filtering of the differential pair. This can be useful in high noise environments for additional noise rejection capability. A 0.1µF capacitor may be connected to this pin to Ground.

Des — Input Equalizer Gain (EQ)

The Des can enable receiver input equalization of the serial stream to increase the eye opening to the Des input. Note this function cannot be seen at the RxIN+/- input. The equalization feature may be controlled by the external pin or by register.

Table 7. Receiver Equalization Configuration Table

EQ (Strap Option)	Effect
L	~1.5 dB
H	~13 dB

EMI REDUCTION FEATURES

Des — VOD Select (VODSEL)

The differential output voltage of the Channel Link interface is controlled by the VODSEL input.

Table 8. Des — Differential Output Voltage Table

VODSEL	Result
L	VOD is 250 mV TYP (500 mVp-p)
H	VOD is 400 mV TYP (800 mVp-p)

Des — SSCG Generation — Optional

The Des provides an internally generated spread spectrum clock (SSCG) to modulate its outputs. Both clock and data outputs are modulated. This will aid to lower system EMI. Output SSCG deviations to ±2% (4% total) at up to 100 kHz modulations is available. See Switching Characteristics Table. This feature may be controlled by external STRAP pins or by register. The LFMODE setting should be set appropriately if the SSCG is being used. Set LFMODE HIGH if the clock frequency is between 5 MHz and 20 MHz. Set LFMODE LOW if teh clock frequency is between 20 MHz and 50 MHz.

Table 9. SSCG Configuration (LF_MODE = L) — Des Output

SSC[2:0] Inputs LF_MODE = L (20 — 55 MHz)			Result	
SSC2	SSC1	SSC0	fdev (%)	fmod (kHz)
L	L	L	OFF	OFF
L	L	H	±0.9	CLK/2168
L	H	L	±1.2	
L	H	H	±1.9	
H	L	L	±2.3	
H	L	H	±0.7	CLK/1300
H	H	L	±1.3	
H	H	H	±1.7	

Table 10. SSCG Configuration (LF_MODE = H) — Des Output

SSC[2:0] Inputs LF_MODE = H (5 — 20 MHz)			Result	
SSC2	**SSC1**	**SSC0**	**fdev (%)**	**fmod (kHz)**
L	L	L	**OFF**	**OFF**
L	L	H	±0.7	**CLK/625**
L	H	L	±1.3	
L	H	H	±1.8	
H	L	L	±2.2	
H	L	H	±0.7	**CLK/385**
H	H	L	±1.2	
H	H	H	±1.7	

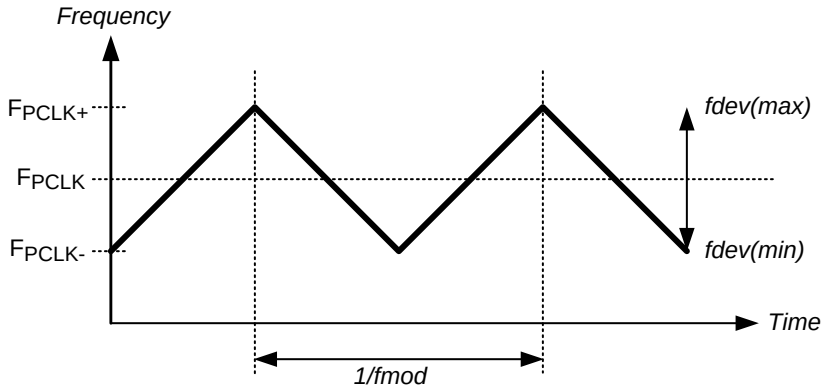


Figure 26. SSCG Waveform

Power Saving Features

Des — Power Down Feature (PDB)

The DS92LV0412 has a PDB input pin to ENABLE or POWER DOWN the device. This pin is controlled by the host and is used to save power, disabling the Des when the display is not needed. An auto detect mode is also available. In this mode, the PDB pin is tied HIGH and the Des will enter POWER DOWN when the serial stream stops. When the serial stream starts up again, the Des will lock to the input stream and assert the LOCK pin and output valid data. In the POWER DOWN mode, the LVDS data and clock output states are determined by the OSS_SEL status. Note – in POWER DOWN, the optional Serial Bus Control Registers are **RESET**.

Des — Stop Stream SLEEPFeature

The DS92LV0412 will enter a low power SLEEP state when the input serial stream is stopped. A STOP condition is detected when the embedded clock bits are not present. When the serial stream starts again, the Des will then lock to the incoming signal and recover the data. Note – in STOP CLOCK SLEEP, the optional Serial Bus Control Registers values are **RETAINED**.

1.8V or 3.3V VDDIO Operation

The DS92LV0412 parallel control bus can operate with 1.8 V or 3.3 V levels (V_{DDIO}) for host compatibility. The 1.8 V levels will offer a system power savings.

Built In Self Test (BIST)

An optional At-Speed Built In Self Test (BIST) feature supports the testing of the high-speed serial link. This is useful in the prototype stage, equipment production, in-system test and also for system diagnostics. In the BIST mode only a input clock is required along with control to the Ser and Des BISTEN input pins. The Ser outputs a test pattern (PRBS7) and drives the link at speed. The Des detects the PRBS7 pattern and monitors it for errors. A PASS output pin toggles to flag any payloads that are received with 1 to 24 errors. Upon completion of the test, the result of the test is held on the PASS output until reset (new BIST test or Power Down). A high on PASS indicates NO ERRORS were detected. A Low on PASS indicates one or more errors were detected. The duration of the test is controlled by the pulse width applied to the Des BISTEN pin.

Inter-operability is supported between this Channel Link II device and all reverse compatible devices— see respective datasheets for details on entering BIST mode and control.

Sample BIST Sequence

See Figure 27 for the BIST mode flow diagram.

Step 1: Place the serializer in BIST Mode by setting Ser BISTEN = H. The BIST Mode is enabled via the BISTEN pin. An RxCLKIN is required for all the Ser options. When the deserializer detects the BIST mode pattern and command the parallel data and control signal outputs are shut off.

Step 2: Place the deserializer in BIST mode by setting the BISTEN = H. The Des is now in the BIST mode and checks the incoming serial payloads for errors. If an error in the payload (1 to 24) is detected, the PASS pin will switch low for one half of the clock period. During the BIST test, the PASS output can be monitored and counted to determine the payload error rate.

Step 3: To Stop the BIST mode, the deserializer BISTEN pin is set Low. The deserializer stops checking the data and the final test result is held on the PASS pin. If the test ran error free, the PASS output will be High. If there was one or more errors detected, the PASS output will be Low. The PASS output state is held until a new BIST is run, the device is RESET, or Powered Down. The BIST duration is user controlled by the duration of the BISTEN signal.

Step 4: To return the link to normal operation, the ser and des BISTEN input are set Low. The Link returns to normal operation.

Figure 28 shows the waveform diagram of a typical BIST test for two cases. Case 1 is error free, and Case 2 shows one with multiple errors. In most cases it is difficult to generate errors due to the robustness of the link (differential data transmission etc.), thus they may be introduced by greatly extending the cable length, faulting the interconnect, reducing signal condition enhancements (De-Emphasis, VODSEL, or deserializer Equalization).

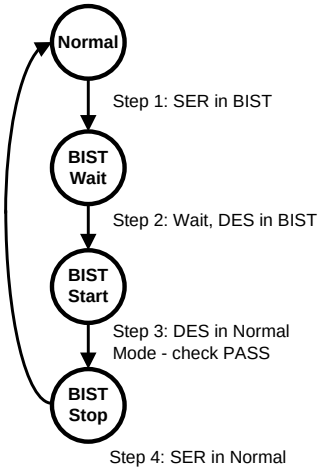


Figure 27. BIST Mode Flow Diagram

BER Calculations

It is possible to calculate the approximate Bit Error Rate (BER). The following is required:

- Pixel Clock Frequency (MHz)
- BIST Duration (seconds)
- BIST test Result (PASS)

The BER is less than or equal to one over the product of 24 times the RxCLKIN rate times the test duration. If we assume a 65MHz RxCLKIN, a 10 minute (600 second) test, and a PASS, the BERT is ≤ 1.07 X 10E-12

The BIST mode runs a check on the data payload bits. The LOCK pin also provides a link status. It the recovery of the C0 and C1 bits does not reconstruct the expected clock signal, the LOCK pin will switch Low. The combination of the LOCK and At-Speed BIST PASS pin provides a powerful tool for system evaluation and performance monitoring.

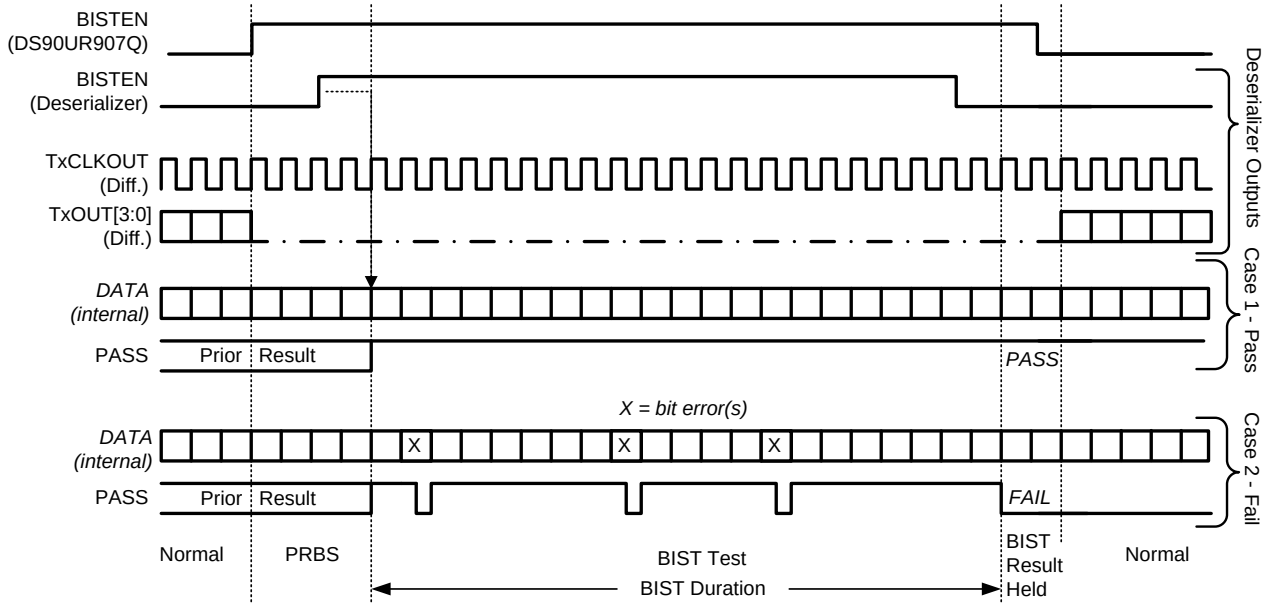


Figure 28. BIST Waveforms

Optional Serial Bus Control

The DS92LV0411 and DS92LV0412 may be configured by the use of a serial control bus that is I2C protocol compatible. By default, the I2C reg_0x00'h is set to 00'h and all configuration is set by control/strap pins. A write of 01'h to reg_0x00'h will enable/allow configuration by registers; this will override the control/strap pins. Multiple devices may share the serial control bus since multiple addresses are supported. See Figure 29.

The serial bus is comprised of three pins. The SCL is a Serial Bus Clock Input. The SDA is the Serial Bus Data Input / Output signal. Both SCL and SDA signals require an external pull up resistor to V_{DDIO}. For most applications a 4.7 kΩ pull up resistor to 3.3V may be used. The resistor value may be adjusted for capacitive loading and data rate requirements. The signals are either pulled High, or driven Low.

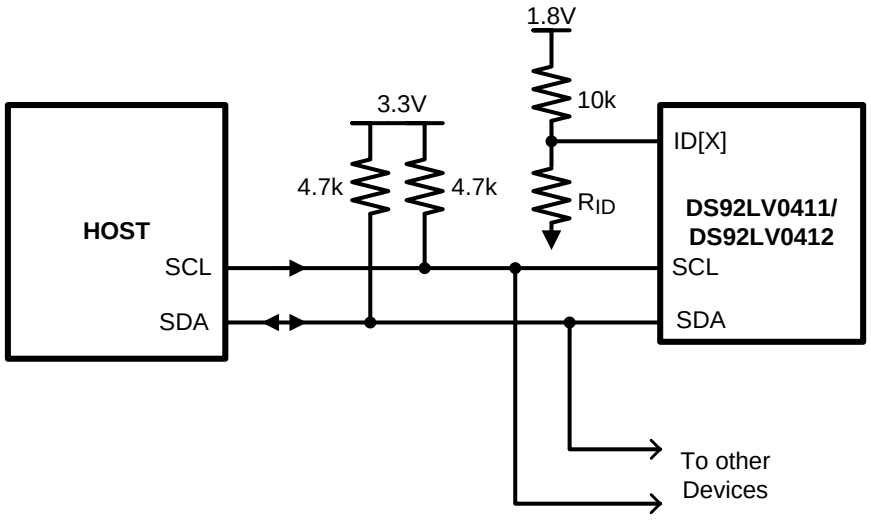


Figure 29. Serial Control Bus Connection

The third pin is the ID[X] pin. This pin sets one of four possible device addresses. Three different connections are possible. The pin may be pulled to V_{DD} (**1.8V, NOT V_{DDIO}**)) with a 10 kΩ resistor. Or a 10 kΩ pull up resistor (to V_{DD}**1.8V, NOT V_{DDIO}**)) and a pull down resistor of the recommended value to set other three possible addresses may be used. See Table 11.

The Serial Bus protocol is controlled by START, START-Repeated, and STOP phases. A START occurs when SCL transitions Low while SDA is High. A STOP occurs when SDA transition High while SCL is also HIGH. See Figure 30.

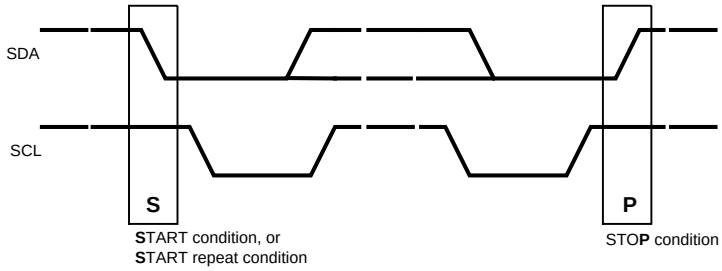


Figure 30. START and STOP Conditions

To communicate with a remote device, the host controller (master) sends the slave address and listens for a response from the slave. This response is referred to as an acknowledge bit (ACK). If a slave on the bus is addressed correctly, it Acknowledges (ACKs) the master by driving the SDA bus low. If the address doesn't match a device's slave address, it Not-acknowledges (NACKs) the master by letting SDA be pulled High. ACKs also occur on the bus when data is being transmitted. When the master is writing data, the slave ACKs after every data byte is successfully received. When the master is reading data, the master ACKs after every data byte is received to let the slave know it wants to receive another data byte. When the master wants to stop reading, it NACKs after the last data byte and creates a stop condition on the bus. All communication on the bus begins with either a Start condition or a Repeated Start condition. All communication on the bus ends with a Stop condition. A READ is shown in Figure 31 and a WRITE is shown in Figure 32.

If the Serial Bus is not required, the three pins may be left open (NC).

Table 11. ID[x] Resistor Value – DS92LV0411

Resistor RID kΩ	Address 7'b	Address 8'b 0 appended (WRITE)
0.47	7b' 110 1001 (h'69)	8b' 1101 0010 (h'D2)
2.7	7b' 110 1010 (h'6A)	8b' 1101 0100 (h'D4)
8.2	7b' 110 1011 (h'6B)	8b' 1101 0110 (h'D6)
Open	7b' 110 1110 (h'6E)	8b' 1101 1100 (h'DC)

Table 12. ID[x] Resistor Value – DS92LV0412

Resistor RID kΩ	Address 7'b	Address 8'b 0 appended (WRITE)
0.47	7b' 111 0001 (h'71)	8b' 1110 0010 (h'E2)
2.7	7b' 111 0010 (h'72)	8b' 1110 0100 (h'E4)
8.2	7b' 111 0011 (h'73)	8b' 1110 0110 (h'E6)
Open	7b' 111 0110 (h'76)	8b' 1110 1100 (h'EC)

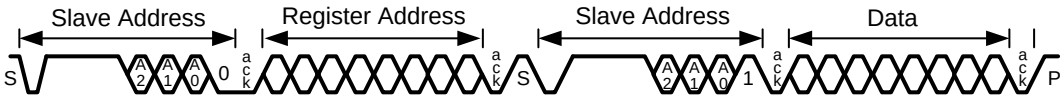


Figure 31. Serial Control Bus — READ

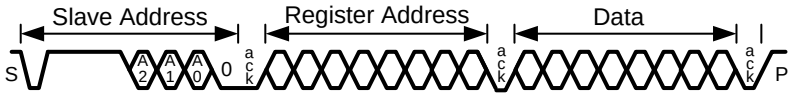


Figure 32. Serial Control Bus — WRITE

Table 13. DS92LV0411 SERIALIZER — Serial Bus Control Registers

ADD (dec)	ADD (hex)	Register Name	Bit(s)	R/W	Default (bin)	Function	Description
0	0	Ser Config 1	7	R/W	0	***Reserved***	***Reserved***
			6	R/W	0	MAPSEL	0: LSB on RxIN3 1: MSB on RxIN3
			5	R/W	0	VODSEL	0: Low 1: High
			4		0	***Reserved***	***Reserved***
			3:2	R/W	00	CONFIG	00: Control Signal Filter Disabled 01: Control Signal Filter Enabled 10: **Reserved** 11: **Reserved**
			1	R/W	0	SLEEP	Note – not the same function as $\overline{\text{PowerDown}}$ (PDB) 0: normal mode 1: Sleep Mode – **Register settings retained.**
			0	R/W	0	REG	0: Configurations set from control pins 1: Configuration set from registers (except I2C_ID)
1	1	Device ID	7	R/W	0	REG ID	0: Address from ID[X] Pin 1: Address from Register
			6:0	R/W	1101000	ID[X]	Serial Bus Device ID, IDs are: 7b '1101 001 (h'69) 7b '1101 010 (h'6A) 7b '1101 011 (h'6B) 7b '1101 110 (h'6E) All other addresses are ***Reserved***.
2	2	De-Emphasis Control	7:5	R/W	000	De-E Setting	000: set by external Resistor 001: -1 dB 010: -2 dB 011: -3.3 dB 100: -5 dB 101: -6.7 dB 110: -9 dB 111: -12 dB
			4	R/W	0	De-E EN	0: De-Emphasis Enabled 1: De-Emphasis Disabled
			3:0	R/W	000	***Reserved***	***Reserved***

Table 14. DS92LV0412 DESERIALIZER — Serial Bus Control Registers

ADD (dec)	ADD (hex)	Register Name	Bit(s)	R/W	Default (bin)	Function	Description
0	0	Des Config 1	7	R/W	0	LFMODE	SSCG Mode — low frequency support 0: 20 to 65 MHz Operation 1: 10 to 20 MHz Operation
			6	R/W	0	MAPSEL	Channel Link Map Select 0: LSB on TxOUT3+/- 1: MSB on TxOUT3+/-
			5	R/W	0	***Reserved***	***Reserved***
			4	R/W	0	***Reserved***	***Reserved***
			3:2	R/W	00	CONFIG	00: Control Signal Filter Disabled 01: Control Signal Filter Enabled 10: **Reserved** 11: **Reserved**
			1	R/W	0	SLEEP	Note – not the same function as $\overline{\text{PowerDown}}$ (PDB) 0: normal mode 1: Sleep Mode – **Register settings retained.**
			0	R/W	0	REG Control	0: Configurations set from control pins 1: Configuration set from registers (except I2C_ID)
1	1	Device ID	7	R/W	0	REG ID	0: Address from ID[X] Pin 1: Address from Register
			6:0	R/W	1110000	ID[X]	Serial Bus Device ID, IDs are: 7b' 111 0001 (h'71) 7b' 111 0010 (h'72) 7b' 111 0011 (h'73) 7b' 111 0110 (h'76) All other addresses are ***Reserved***.
2	2	Des Features 1	7	R/W	0	OEN	Output Enable Input (See Table 6)
			6	R/W	0	OSS_SEL	Output Sleep State Select (See Table 6)
			5:4	R/W	00	***Reserved***	***Reserved***
			3	R/W	0	VODSEL	LVDS Driver Output Voltage Select 0: LVDS VOD is ±250 mV, 500 mVp-p (typ) 1: LVDS VOD is ±400 mV, 800 mVp-p (typ)
			2:0	R/W	000	OSC_SEL	000: OFF 001:**RESERVED** 010: 25 MHz ±40% 011: 16.7 MHz ±40% 100: 12.5 MHz ±40% 101: 10 MHz ±40% 110: 8.3 MHz ±40% 111: 6.3MHz ±40%

Table 14. DS92LV0412 DESERIALIZER — Serial Bus Control Registers (continued)

ADD (dec)	ADD (hex)	Register Name	Bit(s)	R/W	Default (bin)	Function	Description
3	3	Des Features 2	7:5	R/W	000	EQ Gain	000: ~1.625 dB 001: ~3.25 dB 010: ~4.87 dB 011: ~6.5 dB 100: ~8.125 dB 101: ~9.75 dB 110: 11.375 dB 111: 13 dB
			4	R/W	0	EQ Enable	0: EQ = disabled 1: EQ = enabled
			3	R/W	0	***Reserved***	***Reserved***
			2:0	R/W	000	SSC	**IF LFMODE = 0 then:** 000: SSCG OFF 001: fdev = ±0.9%, fmod = CLK/2168 010: fdev = ±1.2%, fmod = CLK/2168 011: fdev = ±1.9%, fmod = CLK/2168 100: fdev = ±2.3%, fmod = CLK/2168 101: fdev = ±0.7%, fmod = CLK/21300 110: fdev = ±1.3%, fmod = CLK/1300 111: fdev = ±1.57%, fmod = CLK/1300 **IF LFMODE = 1, then:** 001: fdev = ±0.7%, fmod = CLK/625 010: fdev = ±1.3%, fmod = CLK/625 011: fdev = ±1.8%, fmod = CLK/625 100: fdev = ±2.2%, fmod = CLK/625 101: fdev = ±0.7%, fmod = CLK/385 110: fdev = ±1.2%, fmod = CLK/385 111: fdev = ±1.7%, fmod = CLK/385

APPLICATIONS INFORMATION

DISPLAY APPLICATION

The DS92LV0411 and DS92LV0412 chipset is intended for interface between a host (graphics processor) and a Display. It supports an 24-bit color depth (RGB888) and up to 1024 X 768 display formats. In a RGB888 application, 24 color bits (R[7:0], G[7:0], B[7:0]), Pixel Clock (PCLK) and three control bits (VS, HS and DE) are supported across the serial link with PCLK rates from 5 to 50 MHz. The chipset may also be used in 18-bit color applications. In this application three to six general purpose signals may also be sent from host to display.

DS92LV0411 TYPICAL APPLICATION CONNECTION

Figure 33 shows a typical application of the DS92LV0411 for a 50 MHz 24-bit Color Display Application. The LVDS inputs require external 100 ohm differential termination resistors. The CML outputs require 0.1 µF AC coupling capacitors to the line. The line driver includes internal termination. Bypass capacitors are placed near the power supply pins. At a minimum, four 0.1 µF capacitors and a 4.7 µF capacitor should be used for local device bypassing. System GPO (General Purpose Output) signals control the PDB and BISTEN pins. The application assumes the companion deserializer (DS92LV0412) therefore the configuration pins are also both tied Low. In this example the cable is long, therefore the VODSEL pin is tied High and a De-Emphasis value is selected by the resistor R1. The interface to the host is with 1.8 V LVCMOS levels, thus the VDDIO pin is connected also to the 1.8V rail. The Optional Serial Bus Control is not used in this example, thus the SCL, SDA and ID[x] pins are left open. A delay cap is placed on the PDB signal to delay the enabling of the device until power is stable. Bypass capacitors are placed near the power supply pins. Ferrite beads are placed on the power lines for effective noise suppression.

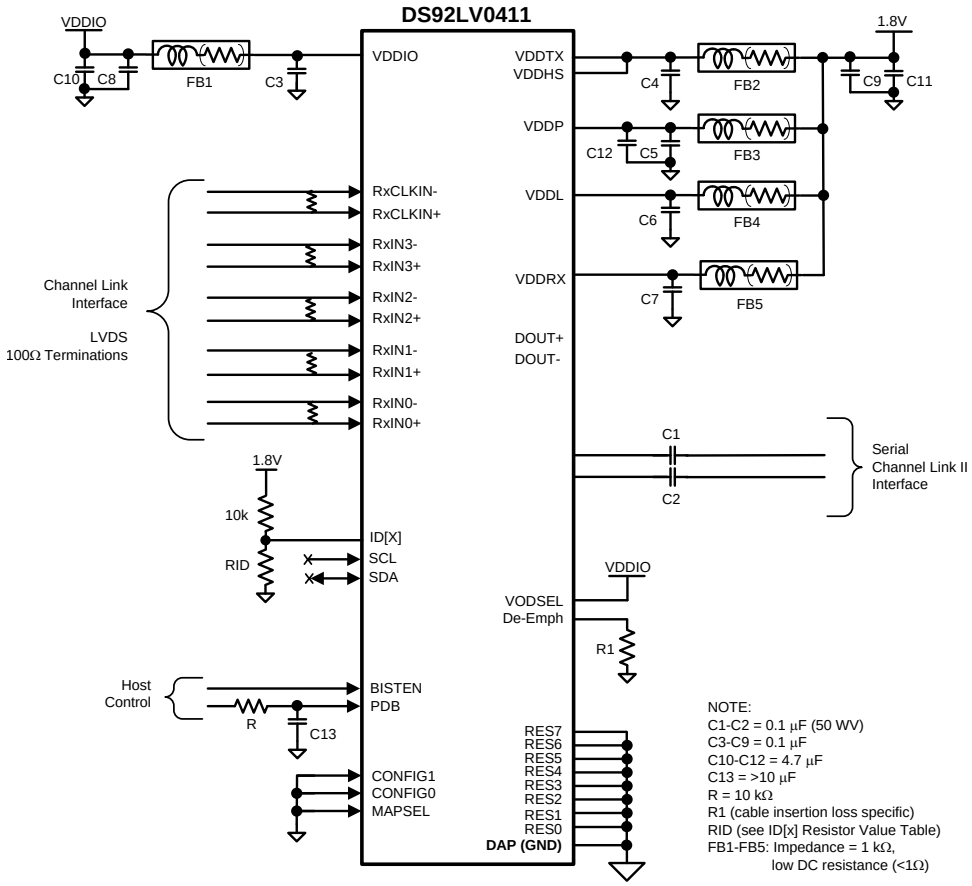


Figure 33. DS92LV0411 Typical Connection Diagram

DS92LV0412 TYPICAL APPLICATION CONNECTION

Figure 34 shows a typical application of the DS92LV0412 for a 50 MHz 24-bit Color Display Application. The CML inputs require 0.1 µF AC coupling capacitors to the line. The line driver includes internal termination. Bypass capacitors are placed near the power supply pins. At a minimum, four 0.1 µF capacitors and a 4.7 µF capacitor should be used for local device bypassing. System GPO (General Purpose Output) signals control the PDB and BISTEN pins. The application assumes the companion deserializer (DS92LV0412) therefore the configuration pins are also both tied Low. The interface to the host is with 1.8 V LVCMOS levels, thus the VDDIO pin is connected also to the 1.8V rail. The Optional Serial Bus Control is not used in this example, thus the SCL, SDA and ID[x] pins are left open. A delay cap is placed on the PDB signal to delay the enabling of the device until power is stable. Bypass capacitors are placed near the power supply pins. Ferrite beads are placed on the power lines for effective noise suppression.

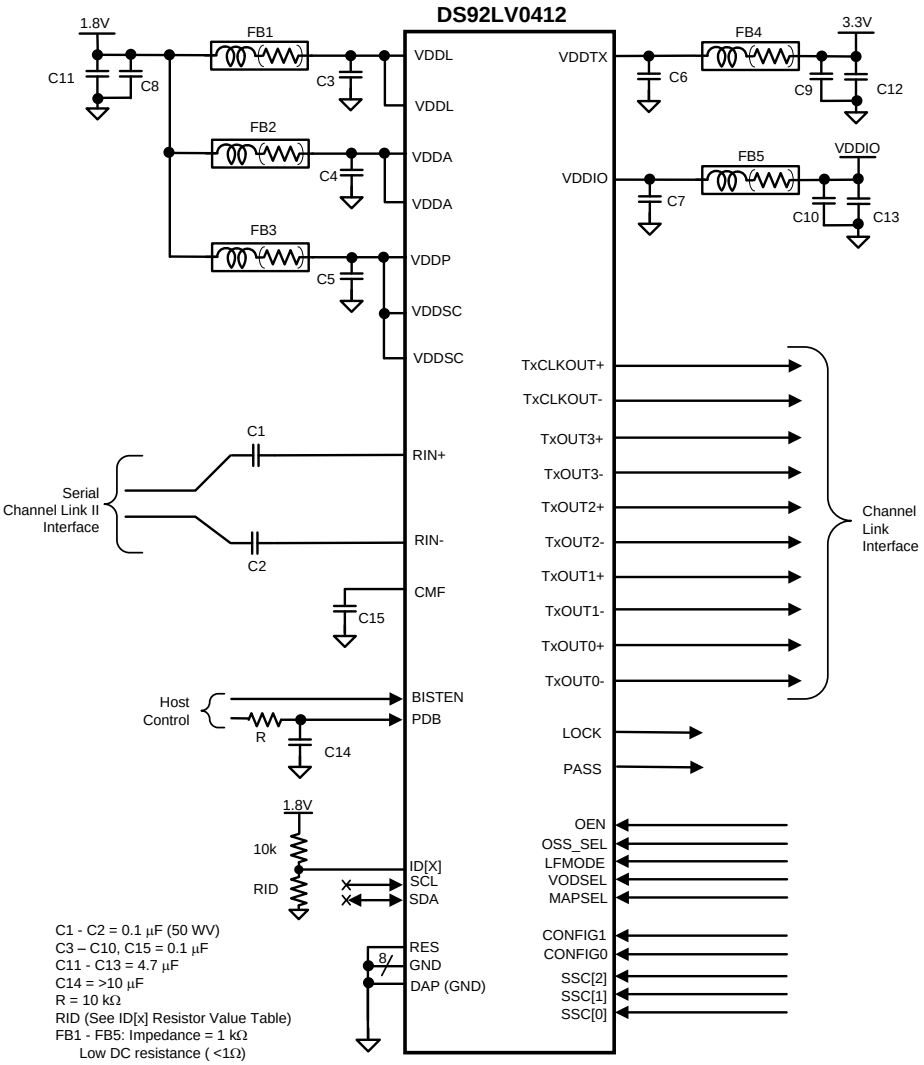


Figure 34. DS92LV0412 Typical Connection Diagram

POWER UP REQUIREMENTS AND PDB PIN

The VDD (V_{DDn} and V_{DDIO}) supply ramp should be faster than 1.5 ms with a monotonic rise. If slower then 1.5 ms then a capacitor on the PDB pin is needed to ensure PDB arrives after all the VDD have settled to the recommended operating voltage. When PDB pin is pulled to V_{DDIO}, it is recommended to use a 10 kΩ pull-up and a 22 uF cap to GND to delay the PDB input signal.

TRANSMISSION MEDIA

The DS92LV0411 / DS92LV0412 and their companion deserializer/serializer chipset is intended to be used in a point-to-point configuration, through a PCB trace, twisted pair or coaxial cables. The DS92LV0411 requires external parallel LVDS termination, but provides internal serial lane terminations to provide a clean signaling environment. The interconnect for LVDS should present a differential impedance of 100 Ohms. The interconnect for the Channel Link II interface should present a differential impedance of 100 Ohms or when configured for coaxial cables the interconnect should present an impedance of 50 Ohms. Use cables and connectors that have matched impedance to minimize impedance discontinuities. Shielded or un-shielded cables may be used depending upon the noise environment and application requirements.

LIVE LINK INSERTION

The serializer and deserializer devices support live link or cable hot plug applications. The automatic receiver lock to random data “plug & go” hot insertion capability allows the DS92LV0412 to attain lock to the active data stream during a live cable insertion event.

ALTERNATE COLOR / DATA MAPPING

Color Mapped data Pin names are provided to specify a recommended mapping for 24-bit and 18-bit Applications. When connecting to earlier generations of Channel Link II deserializer devices, a color mapping review is recommended to ensure the correct connectivity is obtained. Table 15 provides examples for interfacing between DS92LV0411 and different deserializers.

Table 15. Serializer Alternate Color / Data Mapping

Channel Link	Bit Number	RGB (LSB Example)		DS92LV2412	DS90UR124	DS99R124Q	DS90C124
RxIN3	Bit 26	B1		B1	N/A		
	Bit 25	B0		B0			
	Bit 24	G1		G1			
	Bit 23	G0		G0			
	Bit 22	R1		R1			
	Bit 21	R0		R0			
RxIN2	Bit 20	DE		DE	ROUT20	TxOUT2	ROUT20
	Bit 19	VS		VS	ROUT19		ROUT19
	Bit 18	HS		HS	ROUT18		ROUT18
	Bit 17	B7		B7	ROUT17		ROUT17
	Bit 16	B6		B6ROUT10	ROUT16		ROUT16
	Bit 15	B5		B5	ROUT15		ROUT15
	Bit 14	B4		B4	ROUT14		ROUT14
RxIN1	Bit 13	B3		B3	ROUT13		ROUT13
	Bit 12	B2		B2	ROUT12		ROUT12
	Bit 11	G7		G7	ROUT11		ROUT11
	Bit 10	G6		G6	ROUT10	TxOUT1	ROUT10
	Bit 9	G5		G5	ROUT9		ROUT9
	Bit 8	G4		G4	ROUT8		ROUT8
	Bit 7	G3		G3	ROUT7		ROUT7
RxIN0	Bit 6	G2		G2	ROUT6	TxOUT0	ROUT6
	Bit 5	R7		R7	ROUT5		ROUT5
	Bit 4	R6		R6	ROUT4		ROUT4
	Bit 3	R5		R5	ROUT3		ROUT3
	Bit 2	R4		R4	ROUT2		ROUT2
	Bit 1	R3		R3	ROUT1		ROUT1
	Bit 0	R2		R2	ROUT0		ROUT0
N/A				N/A	ROUT23	OS2	ROUT23
					ROUT22	OS1	ROUT22
					ROUT21	OS0	ROUT21
DS92LV0411 Settings	**MAPSEL = 0**			**CONFIG [1:0] = 00**	**CONFIG [1:0] = 10**		**CONFIG [1:0] = 11**

Table 16. Deserializer Alternate Color / Data Mapping

Channel Link	Bit Number	RGB (LSB Example)		DS92LV2411	DS90UR241	DS99R421Q	DS90C241
TxOUT3	Bit 26	B1		B1	N/A		
	Bit 25	B0		B0			
	Bit 24	G1		G1			
	Bit 23	G0		G0			
	Bit 22	R1		R1			
	Bit 21	R0		R0			
TxOUT2	Bit 20	DE		DE	DIN20	RxIN2	DIN20
	Bit 19	VS		VS	DIN19		DIN19
	Bit 18	HS		HS	DIN18		DIN18
	Bit 17	B7		B7	DIN17		DIN17
	Bit 16	B6		B6ROUT10	DIN16		DIN16
	Bit 15	B5		B5	DIN15		DIN15
	Bit 14	B4		B4	DIN14		DIN14
TxOUT1	Bit 13	B3		B3	DIN13	RxIN1	DIN13
	Bit 12	B2		B2	DIN12		DIN12
	Bit 11	G7		G7	DIN11		DIN11
	Bit 10	G6		G6	DIN10		DIN10
	Bit 9	G5		G5	DIN9		DIN9
	Bit 8	G4		G4	DIN8		DIN8
	Bit 7	G3		G3	DIN7		DIN7
TxOUT0	Bit 6	G2		G2	DIN6	RxIN0	DIN6
	Bit 5	R7		R7	DIN5		DIN5
	Bit 4	R6		R6	DIN4		DIN4
	Bit 3	R5		R5	DIN3		DIN3
	Bit 2	R4		R4	DIN2		DIN2
	Bit 1	R3		R3	DIN1		DIN1
	Bit 0	R2		R2	DIN0		DIN0
N/A				N/A	DIN923	OS2	DIN923
					DIN922	OS1	DIN922
					DIN921	OS0	DIN921
DS92LV0412 Settings	**MAPSEL = 0**			**CONFIG [1:0] = 00**	**CONFIG [1:0] = 10**		**CONFIG [1:0] = 11**

PCB LAYOUT AND POWER SYSTEM CONSIDERATIONS

Circuit board layout and stack-up for the LVDS devices should be designed to provide low-noise power feed to the device. Good layout practice will also separate high frequency or high-level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mils) for power / ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitics, which has proven especially effective at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 uF to 0.1 uF. Tantalum capacitors may be in the 2.2 uF to 10 uF range. Voltage rating of the tantalum capacitors should be at least 5X the power supply voltage being used.

Surface mount capacitors are recommended due to their smaller parasitics. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. A large bulk capacitor is recommend at the point of power entry. This is typically in the 50uF to 100uF range and will smooth low frequency switching noise. It is recommended to connect power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with via on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor will increase the inductance of the path.

A small body size X7R chip capacitor, such as 0603, is recommended for external bypass. Its small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20-30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. PIN DESCRIPTIONS tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter many be used to provide clean power to sensitive circuits such as PLLs.

Use at least a four layer board with a power and ground plane. Locate LVCMOS signals away from the LVDS lines to prevent coupling from the LVCMOS lines to the LVDS lines. Closely-coupled differential lines of 100 Ohms are typically recommended for LVDS interconnect. The closely coupled lines help to ensure that coupled noise will appear as common-mode and thus is rejected by the receivers. The tightly coupled lines will also radiate less.

Information on the WQFN style package is provided in Application Note: AN-1187 (SNOA401).

LVDS INTERCONNECT GUIDELINES

See AN-1108 (SNLA008) and AN-905 (SNLA035) for full details.

- Use 100Ω coupled differential pairs
- Use the S/2S/3S rule in spacings
  - S = space between the pair
  - 2S = space between pairs
  - 3S = space to LVCMOS signal
- Minimize the number of vias
- If vias are used, be sure to place vias to ground adjacent to the signal vias to ensure a constant return path for the signal
- Use differential connectors when operating above 500Mbps line speed
- Maintain balance of the traces
- Minimize skew within the pair
- Terminate as close to the TX outputs and RX inputs as possible

REVISION HISTORY

Changes from Revision A (April 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	45

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DS92LV0411SQ/NOPB	Active	Production	WQFN (NJK) | 36	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	LV0411SQ
DS92LV0411SQ/NOPB.A	Active	Production	WQFN (NJK) | 36	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	LV0411SQ
DS92LV0411SQE/NOPB	Active	Production	WQFN (NJK) | 36	250 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	LV0411SQ
DS92LV0411SQE/NOPB.A	Active	Production	WQFN (NJK) | 36	250 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	LV0411SQ
DS92LV0411SQX/NOPB	Active	Production	WQFN (NJK) | 36	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	LV0411SQ
DS92LV0411SQX/NOPB.A	Active	Production	WQFN (NJK) | 36	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	LV0411SQ
DS92LV0412SQ/NOPB	Active	Production	WQFN (RHS) | 48	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	LV0412SQ
DS92LV0412SQ/NOPB.A	Active	Production	WQFN (RHS) | 48	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	LV0412SQ
DS92LV0412SQE/NOPB	Active	Production	WQFN (RHS) | 48	250 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	LV0412SQ
DS92LV0412SQE/NOPB.A	Active	Production	WQFN (RHS) | 48	250 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	LV0412SQ
DS92LV0412SQX/NOPB	Active	Production	WQFN (RHS) | 48	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	LV0412SQ
DS92LV0412SQX/NOPB.A	Active	Production	WQFN (RHS) | 48	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	LV0412SQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

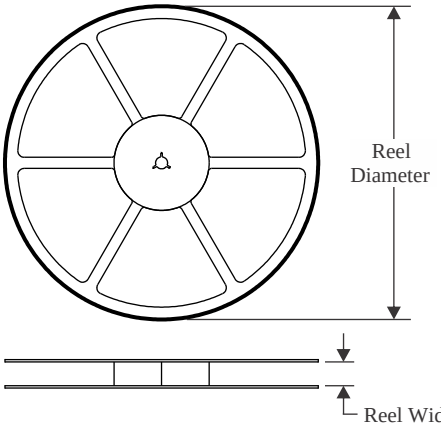
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

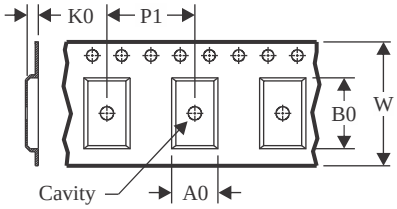
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

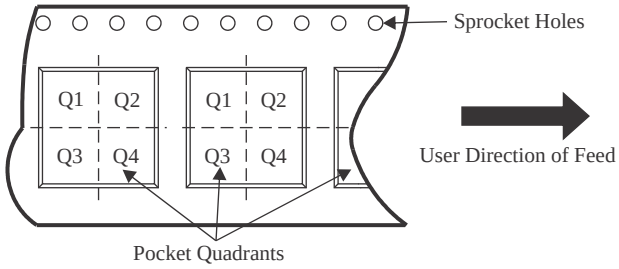


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

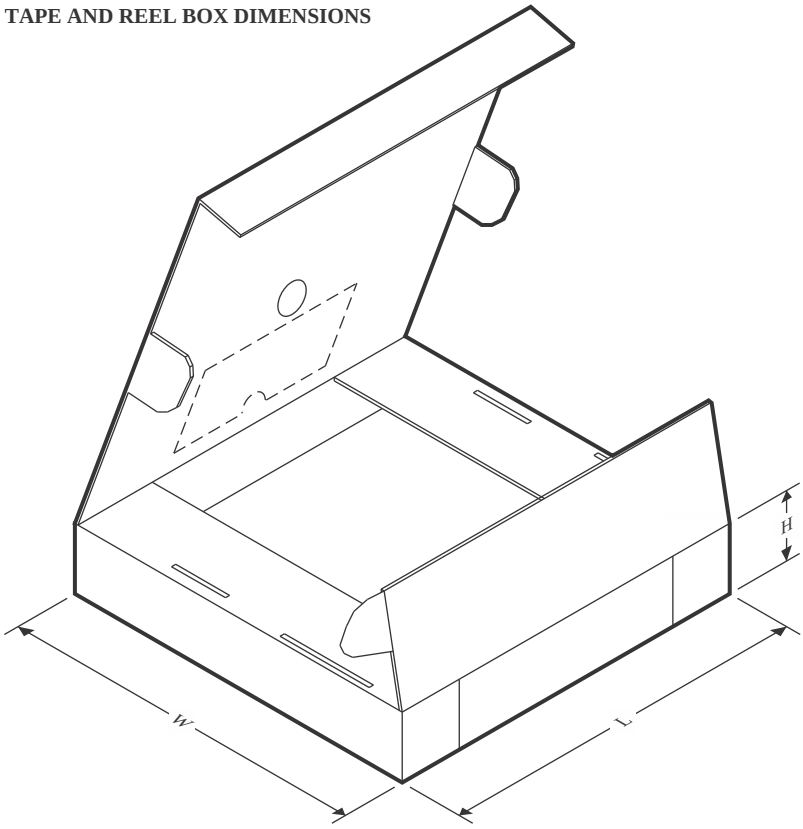
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS92LV0411SQ/NOPB	WQFN	NJK	36	1000	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1
DS92LV0411SQE/NOPB	WQFN	NJK	36	250	178.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1
DS92LV0411SQX/NOPB	WQFN	NJK	36	2500	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1
DS92LV0412SQ/NOPB	WQFN	RHS	48	1000	330.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1
DS92LV0412SQE/NOPB	WQFN	RHS	48	250	178.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1
DS92LV0412SQX/NOPB	WQFN	RHS	48	2500	330.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

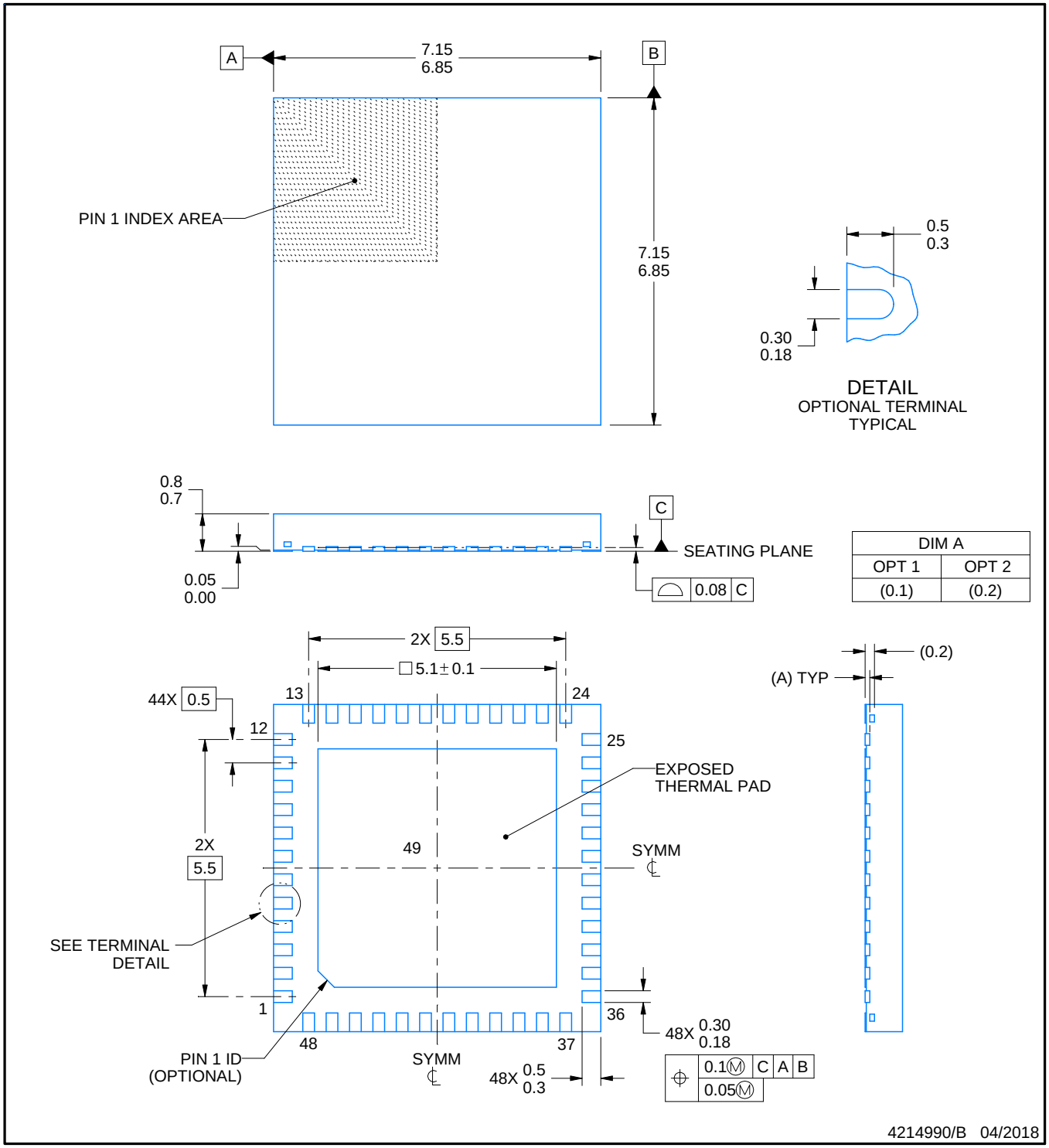
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS92LV0411SQ/NOPB	WQFN	NJK	36	1000	356.0	356.0	36.0
DS92LV0411SQE/NOPB	WQFN	NJK	36	250	208.0	191.0	35.0
DS92LV0411SQX/NOPB	WQFN	NJK	36	2500	356.0	356.0	36.0
DS92LV0412SQ/NOPB	WQFN	RHS	48	1000	356.0	356.0	36.0
DS92LV0412SQE/NOPB	WQFN	RHS	48	250	208.0	191.0	35.0
DS92LV0412SQX/NOPB	WQFN	RHS	48	2500	356.0	356.0	36.0

PACKAGE OUTLINE

RHS0048A

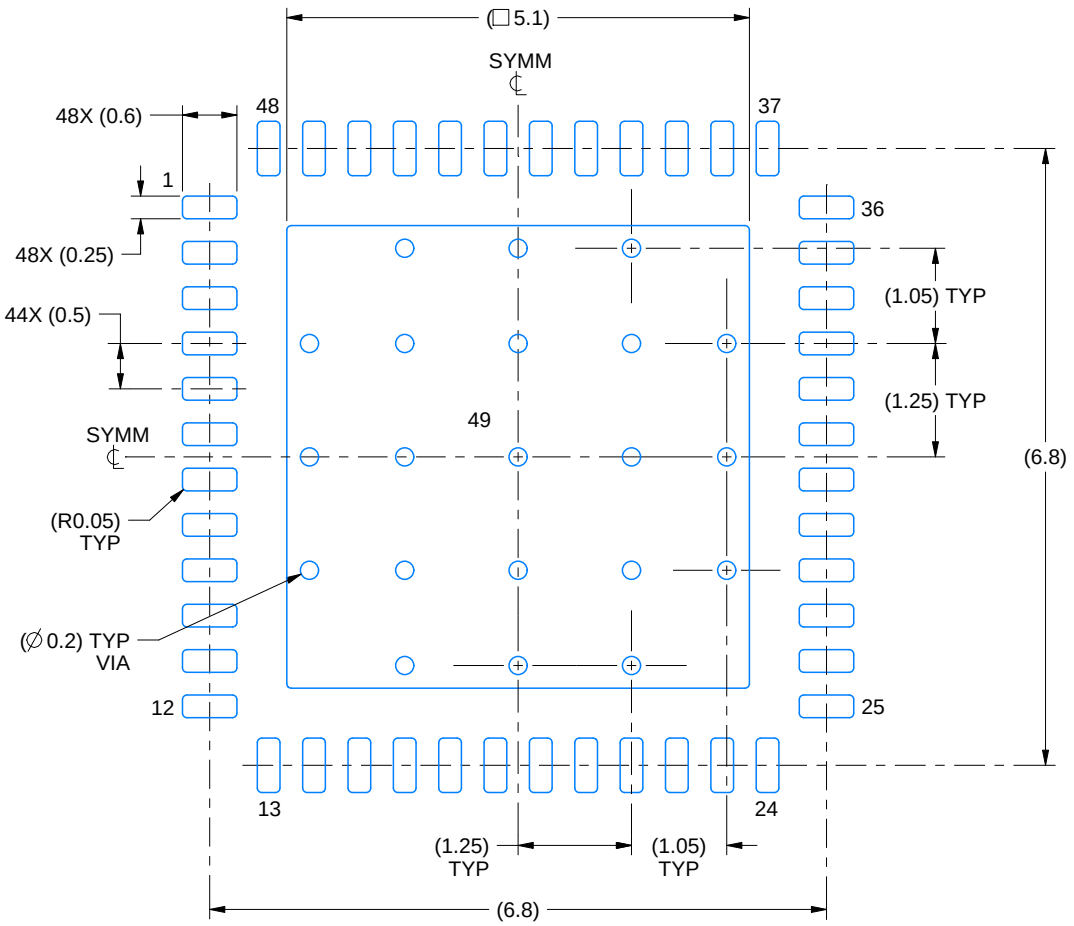
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

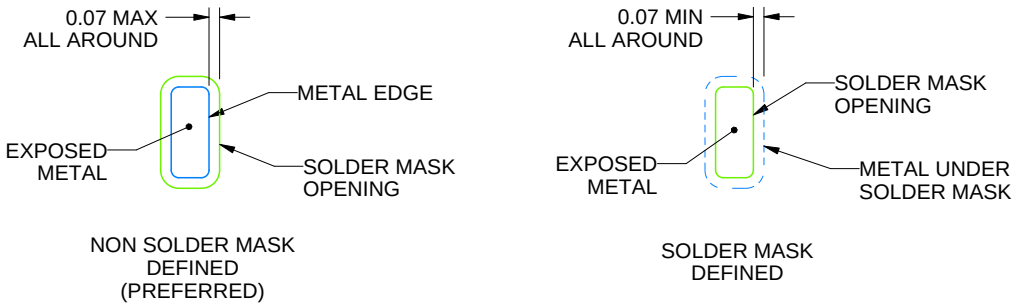


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X



SOLDER MASK DETAILS

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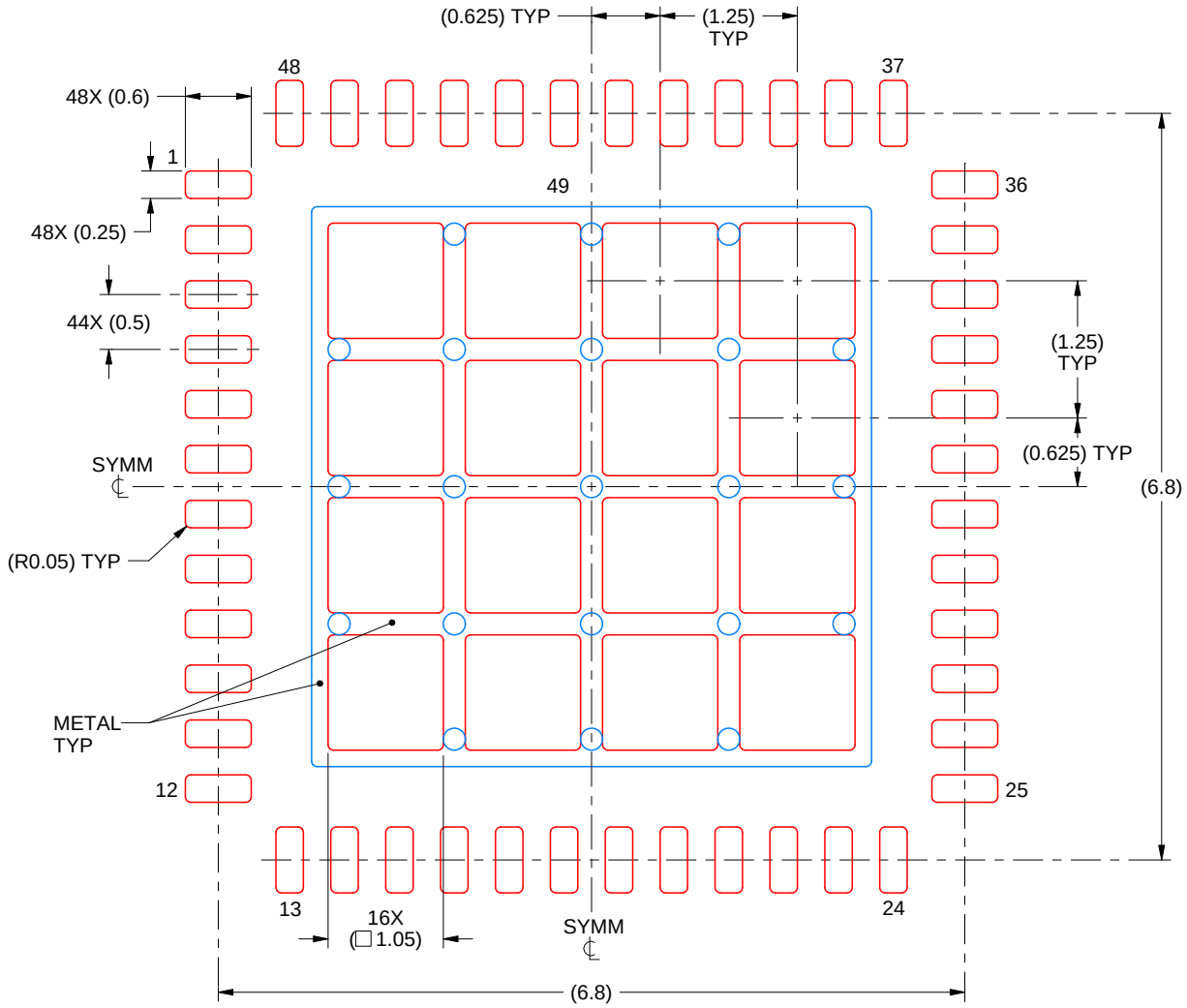
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

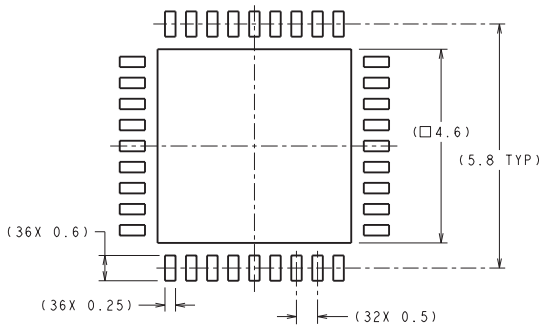
EXPOSED PAD 49
68% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

4214990/B 04/2018

NOTES: (continued)

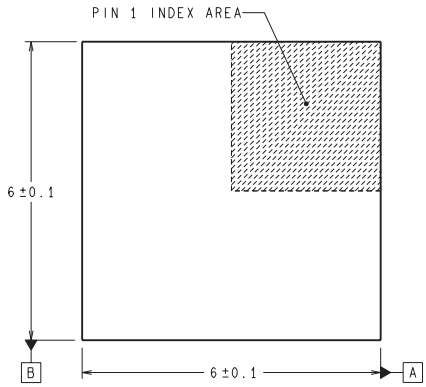
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

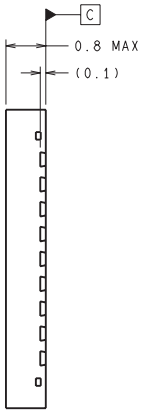
NJK0036A

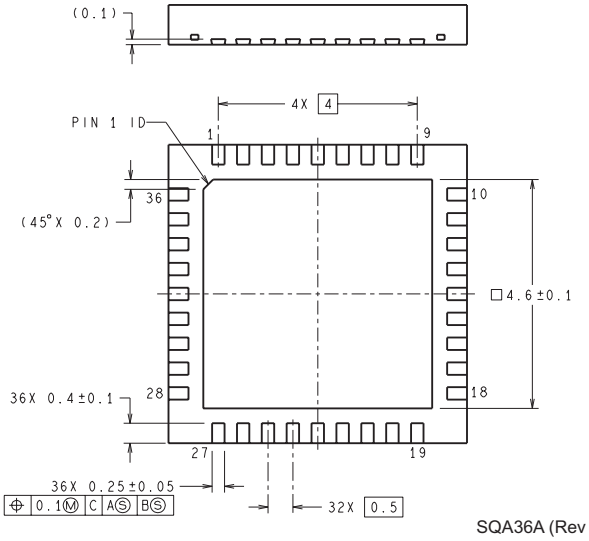


RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY







SQA36A (Rev A)

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Last updated 10/2025