INA20x –16V～80V、500kHz 電流検出アンプ、デュアル・コンパレータ付き

1 特長

- 完全な電流検出ソリューション
- 3 つのゲイン・オプションを利用可能:
  - INA203:20V/V
  - INA204:50V/V
  - INA205:100V/V
- デュアル・コンパレータ:
  - コンパレータ 1 はラッチ搭載
  - コンパレータ 2 は遅延オプションあり
- 同相モード範囲:–16V～80V
- 高精度:温度範囲全体で 3.5% 以下
- 帯域幅:500kHz
- 静止電流:1.8mA
- パッケージ:SO-14、TSSOP-14、VSSOP-10

2 アプリケーション

- ノート PC
- 携帯電話
- 通信機器
- 車載
- パワー・マネージメント
- バッテリ・チャージャ
- 溶接機器

3 概要

INA203、INA204、INA205 は、電圧出力、デュアル・コンパレータ、基準電圧を内蔵した、単方向の電流シャント・モニタのファミリです。INA203、INA204、INA205 は、–16V～80V の同相電圧において、シャント両端の電圧降下を検出できます。これらのデバイスは 3 種類の出力電圧ゲイン (20V/V、50V/V、100V/V)、最大 500kHz の帯域幅に対応しています。

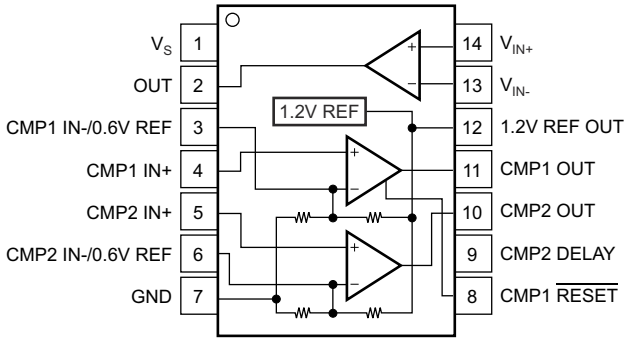
また、INA203、INA204、INA205 には、2 つのオープン・ドレイン・コンパレータと、0.6V の基準電圧が内蔵されています。14 ピンのバージョンでは、コンパレータの基準電圧を外部入力によりオーバーライド可能です。コンパレータ 1 にはラッチ機能があり、コンパレータ 2 は遅延をユーザーがプログラム可能です。14 ピンのバージョンでは、1.2V の基準電圧出力も提供されます。

INA203、INA204、INA205 は、2.7V～18V の単一電源で動作します。拡張動作温度範囲の –40°C～125°C で動作が規定されています。

製品情報(1)

部品番号	パッケージ	本体サイズ (公称)
INA203、INA204、INA205	SOIC (14)	8.65mm × 3.91mm
	VSSOP (10)	3.00mm × 3.00mm
	TSSOP (14)	5.00mm × 4.40mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



概略回路図

Table of Contents

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision E (November 2015) to Revision F (June 2021)	Page
• 文書全体にわたって表、図、相互参照の採番方法を更新	1
• Changed maximum input voltage for accurate measurements from: (V_{SHUNT} – 0.25) / Gain to: (V_{OUT} – 0.25) / Gain	15

Changes from Revision D (May 2009) to Revision E (November 2015)	Page
• 「*ESD 定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加。	1
• Moved thermal values from *Electrical Characteristics: General* to *Thermal Information* table. Removed duplicate storage temperature parameter	9

Changes from Revision C (October 2007) to Revision D (May 2009)	Page
• Changed 図 6-1	7

Device Comparison

表 5-1. Device Gain

DEVICE	GAIN
INA203	20 V/V
INA204	50 V/V
INA205	100 V/V

表 5-2. Related Products

FEATURES	PRODUCT
Variant of INA203–INA205 Comparator 2 polarity	INA206–INA208
Current-shunt monitor with single Comparator and V_{REF}	INA200–INA202
Current-shunt monitor only	INA193–INA198
Current-shunt monitor with split stages for filter options	INA270–INA271

5 Pin Configuration and Functions

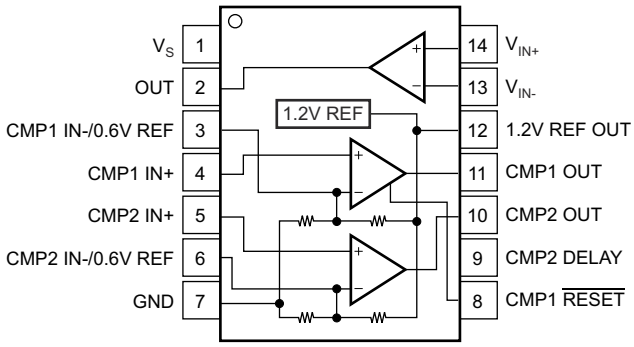


図 5-1. D and PW Packages 14-Pin SOIC and TSSOP Top View

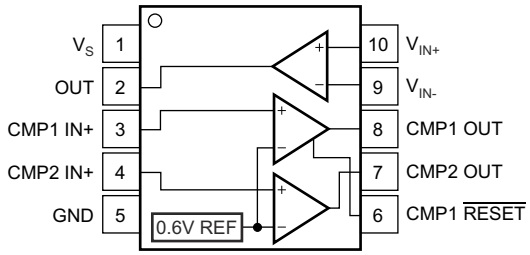


図 5-2. DGS Package 10-Pin VSSOP Top View

表 5-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOIC, TSSOP	VSSOP		
V_S	1	1	I	Power Supply
OUT	2	2	O	Output voltage
CMP1 IN-/0.6-V Ref	3	—	I	Comparator 1 negative input, can be used to override the internal 0.6-V reference
CMP1 IN+	4	3	I	Comparator 1 positive input
CMP2 IN+	5	—	I	Comparator 2 positive input
CMP2 IN–	—	4	I	Comparator 2 negative input
CMP2 IN–/0.6-V Ref	6	—	I	Comparator 2 negative input, can be used to override the internal 0.6-V reference
GND	7	5	I	Ground
CMP1 $\overline{\text{RESET}}$	8	6	I	Comparator 1 output reset, active low
CMP2 DELAY	9	—	I	Connect an optional capacitor to adjust comparator 2 delay
CMP2 OUT	10	7	O	Comparator 2 output
CMP1 OUT	11	8	O	Comparator 1 output
1.2-V REF OUT	12	—	O	1.2-V reference output
VIN–	13	9	I	Connect to shunt low side
VIN+	14	10	I	Connect to shunt high side

6 Specifications

6.1 Absolute Maximum Ratings

See (1)

		MIN	MAX	UNIT
Supply Voltage, V_S			18	V
Current-Shunt Monitor Analog Inputs, V_{IN+} and $V_{IN–}$	Differential (V_{IN+}) – ($V_{IN–}$)	–18	18	V
	Common-Mode	–16	80	V
Comparator Analog Input and Reset Pins		GND – 0.3	(V_S) + 0.3	V
Analog Output, Out Pin		GND – 0.3	(V_S) + 0.3	V
Comparator Output, Out Pin		GND – 0.3	18	V
V_{REF} and CMP2 Delay Pin		GND – 0.3	10	V
Input Current Into Any Pin			5	mA
Operating Temperature		–55	150	°C
Junction Temperature		–65	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CM}	Common-mode input voltage	–16	12	80	V
V_S	Operating supply voltage	2.7	12	18	V
T_A	Operating free-air temperature	–40	25	125	°C

6.4 Thermal Information

THERMAL METRIC (1)		INA20x			UNIT
		D (SOIC)	DGS (VSSOP)	PW (TSSOP)	
		14 PINS	10 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	84.9	161.3	112.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	44	36.8	37.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	39.4	82.3	55.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.3	1.3	2.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	39.1	80.8	54.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	150	200	150	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics: Current-Shunt Monitor

At T_A = 25°C, V_S = 12 V, V_{CM} = 12 V, V_{SENSE} = 100 mV, R_L = 10 kΩ to GND, R_{pullup} = 5.1 kΩ each connected from CMP1 OUT and CMP2 OUT to V_S, and CMP1 IN+ = 1 V and CMP2 IN– = GND, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT							
V_{SENSE}	Full-Scale Sense Input Voltage	$V_{SENSE} = V_{IN+} - V_{IN-}$			0.15	(V_S – 0.25)/ Gain	V
V_{CM}	Common-Mode Input Range	T_A = –40°C to 125°C		–16		80	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = –16 V to 80 V		80	100		dB
	CMRR over Temperature	V_{CM} = 12 V to 80 V	T_A = –40°C to 125°C	100	123		dB
V_{OS}	Offset Voltage, RTI (1)				±0.5	±2.5	mV
		25°C to 125°C				±3	mV
		–40°C to 25°C				±3.5	mV
dV_{OS}/dT	Offset Voltage, RTI (1) vs. Temperature	T_{MIN} to T_{MAX}	T_A = –40°C to 125°C		5		µV/°C
PSR	Offset Voltage, RTI (1) vs. Power Supply	V_{OUT} = 2 V, V_{CM} = 18 V, 2.7 V	T_A = –40°C to 125°C		2.5	100	µV/V
I_B	Input Bias Current, V_{IN-} Pin	T_A = –40°C to 125°C			±9	±16	µA
OUTPUT (V_{SENSE} ≥ 20 mV)							
G	Gain	INA203			20		V/V
		INA204			50		V/V
		INA205			100		V/V
	Gain Error	V_{SENSE} = 20 mV to 100 mV			±0.2%	±1%	
	Gain Error over Temperature	V_{SENSE} = 20 mV to 100 mV	T_A = –40°C to 125°C			±2%	
	Total Output Error (2)	V_{SENSE} = 120 mV, V_S = 16 V			±0.75%	±2.2%	
	Total Output Error (2) over Temperature	V_{SENSE} = 120 mV, V_S = 16 V	T_A = –40°C to 125°C			±3.5%	
	Nonlinearity Error (3)	V_{SENSE} = 20 mV to 100 mV			±0.002%		
R_O	Output Impedance, Pin 2				1.5		Ω
	Maximum Capacitive Load	No Sustained Oscillation			10		nF
OUTPUT (V_{SENSE} < 20 mV) (4)							
	INA203, INA204, INA205 output	–16 V ≤ V_{CM} < 0 V			300		mV
	INA203 output	0 V ≤ V_{CM} ≤ V_S, V_S = 5 V				0.4	V
	INA204 output	0 V ≤ V_{CM} ≤ V_S, V_S = 5 V				1	V
	INA205 output	0 V ≤ V_{CM} ≤ V_S, V_S = 5 V				2	V
	INA203, INA204, INA205 output	V_S < V_{CM} ≤ 80 V			300		mV
VOLTAGE OUTPUT (5)							
	Output Swing to the Positive Rail	V_{IN-} = 11 V, V_{IN+} = 12 V	T_A = –40°C to 125°C		(Vs) – 0.15	(Vs) – 0.25	V
	Output Swing to GND (6)	V_{IN-} = 0 V, V_{IN+} = –0.5 V	T_A = –40°C to 125°C		(V_{GND}) + 0.004	(V_{GND}) + 0.05	V

At T_A = 25°C, V_S = 12 V, V_{CM} = 12 V, V_{SENSE} = 100 mV, R_L = 10 kΩ to GND, R_{pullup} = 5.1 kΩ each connected from CMP1 OUT and CMP2 OUT to V_S, and CMP1 IN+ = 1 V and CMP2 IN– = GND, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE						
BW	Bandwidth	INA203; C_{LOAD} = 5 pF		500		kHz
		INA204; C_{LOAD} = 5 pF		300		kHz
		INA205; C_{LOAD} = 5 pF		200		kHz
	Phase Margin	C_{LOAD} < 10 nF		40		
SR	Slew Rate			1		V/µs
	Settling Time (1%)	V_{SENSE} = 10 mV_{PP} to 100 mV_{PP}, C_{LOAD} = 5 pF		2		µs
NOISE, RTI						
	Output Voltage Noise Density			40		nV/√Hz

(1) Offset is extrapolated from measurements of the output at 20 mV and 100 mV V_{SENSE}.
(2) Total output error includes effects of gain error and V_{OS}.
(3) Linearity is best fit to a straight line.
(4) For details on this region of operation, see the *Accuracy Variations as a Result Of V_{SENSE} and Common-Mode Voltage* section in the *Application and Implementation*.
(5) See Typical Characteristic curve *Positive Output Voltage Swing vs. Output Current* (図 6-8).
(6) Specified by design; not production tested.

6.6 Electrical Characteristics: Comparator

At T_A = 25°C, V_S = 12 V, V_{CM} = 12 V, V_{SENSE} = 100 mV, R_L = 10 kΩ to GND, and R_{pullup} = 5.1 kΩ each connected from CMP1 OUT and CMP2 OUT to V_S, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE					
Offset Voltage	Comparator Common-Mode Voltage = Threshold Voltage		2		mV
Offset Voltage Drift, Comparator 1	T_A = –40°C to 125°C		±2		µV/°C
Offset Voltage Drift, Comparator 2	T_A = –40°C to 125°C		5.4		µV/°C
Threshold	T_A = 25°C	590	608	620	mV
Threshold over Temperature	T_A = –40°C to 125°C	586		625	mV
Hysteresis (1), CMP1	T_A = –40°C to 85°C		–8		mV
Hysteresis (1), CMP2	T_A = –40°C to 85°C		8		mV
INPUT BIAS CURRENT (2)					
CMP1 IN+, CMP2 IN+			0.005	10	nA
CMP1 IN+, CMP2 IN+ vs. Temperature	T_A = –40°C to 125°C			15	nA
INPUT IMPEDANCE					
Pins 3 and 6 (14-pin packages only)			10		kΩ
INPUT RANGE					
CMP1 IN+ and CMP2 IN+			0 V to V_S – 1.5 V		V
Pins 3 and 6 (14-pin packages only) (3)			0 V to V_S – 1.5 V		V
OUTPUT					
Large-Signal Differential Voltage Gain	CMP V_{OUT} 1 V to 4 V, R_L ≥ 15 kΩ Connected to 5 V		200		V/mV

At T_A = 25°C, V_S = 12 V, V_{CM} = 12 V, V_{SENSE} = 100 mV, R_L = 10 kΩ to GND, and R_{pullup} = 5.1 kΩ each connected from CMP1 OUT and CMP2 OUT to V_S, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	High-Level Output Current	V_{ID} = 0.4 V, V_{OH} = V_S		0.0001	1	µA
	Low-Level Output Voltage	V_{ID} = –0.6 V, I_{OL} = 2.35 mA		220	300	mV
RESPONSE TIME (4)						
	Comparator 1	R_L to 5 V, C_L = 15 pF, 100-mV Input Step with 5-mV Overdrive		1.3		µs
	Comparator 2	R_L to 5 V, C_L = 15 pF, 100-mV Input Step with 5-mV Overdrive, C_{DELAY} Pin Open		1.3		µs
RESET						
	RESET Threshold (5)			1.1		V
	Logic Input Impedance			2		MΩ
	Minimum RESET Pulse Width			1.5		µs
	RESET Propagation Delay			3		µs
	Comparator 2 Delay Equation (6)			C_{DELAY} = t_D/5		µF
t_D	Comparator 2 Delay	C_{DELAY} = 0.1 µF		0.5		s

(1) Hysteresis refers to the threshold (the threshold specification applies to a rising edge of a noninverting input) of a falling edge on the noninverting input of the comparator; refer to 図 6-1.
(2) Specified by design; not production tested.
(3) See the *Comparator Maximum Input Voltage Range* section in the *Application and Implementation*.
(4) The comparator response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.
(5) The CMP1 $\overline{\text{RESET}}$ input has an internal 2-MΩ (typical) pulldown. Leaving the CMP1 $\overline{\text{RESET}}$ open results in a LOW state, with transparent comparator operation.
(6) The Comparator 2 delay applies to both rising and falling edges of the comparator output.

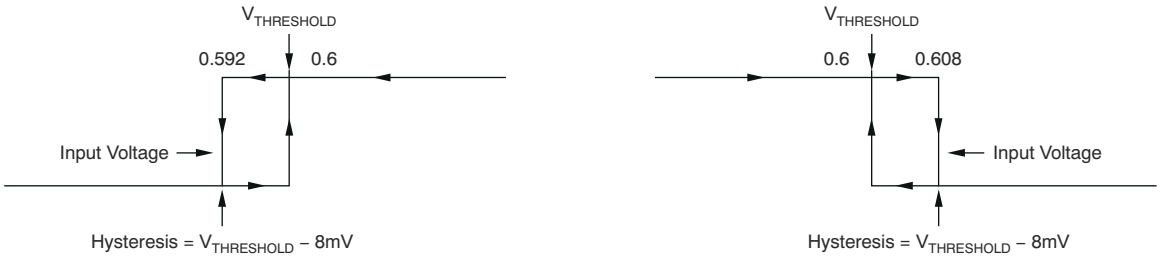


図 6-1. Comparator Hysteresis

6.7 Electrical Characteristics: Reference

At T_A = 25°C, V_S = 12 V, V_{CM} = 12 V, V_{SENSE} = 100 mV, R_L = 10 kΩ to GND, and R_{pullup} = 5.1 kΩ each connected from CMP1 OUT and CMP2 OUT to V_S, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE VOLTAGE						
	1.2-V_{REFOUT} Output Voltage		1.188	1.2	1.212	V
dV_{OUT}/dT	Reference Drift	T_A = –40°C to 85°C		40	100	ppm/°C
	0.6-V_{REF} Output Voltage	Pins 3 and 6 of 14-pin packages only		0.6		v
dV_{OUT}/dT	Reference Drift	T_A = –40°C to 85°C		40	100	ppm/°C
LOAD REGULATION	dV_{OUT}/dI_{LOAD}					
	Sourcing	0mA < I_{SOURCE} < 0.5mA		0.4	2	mV/mA
	Sinking	0mA < I_{SINK} < 0.5mA		0.4		mV/mA
I_{LOAD}	Load Current			1		mA
dV_{OUT}/dV_S	Line Regulation	2.7 V < V_S < 18 V		30		µV/V
CAPACITIVE LOAD						
	Reference Output Maximum Capacitive Load	No Sustained Oscillations		10		nF
OUTPUT IMPEDANCE						
	Output Impedance	Pins 3 and 6 of 14-Pin Packages Only		10		kΩ

6.8 Electrical Characteristics: General

All specifications at T_A = 25°C, V_S = 12 V, V_{CM} = 12 V, V_{SENSE} = 100 mV, R_L = 10 kΩ to GND, R_{pullup} = 5.1 kΩ each connected from CMP1 OUT and CMP2 OUT to V_S, and CMP1 IN+ = 1 V and CMP2 IN– = GND, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_S	Operating power supply	T_A = –40°C to 125°C	2.7		18	V
I_Q	Quiescent current	V_{OUT} = 2 V		1.8	2.2	mA
	Quiescent current over temperature	V_{SENSE} = 0 mV			2.8	mA
	Comparator power-on reset threshold (1)			1.5		V
TEMPERATURE						
	Specified temperature		–40		125	°C
	Operating temperature		–55		150	°C

(1) The INA203, INA204, and INA205 are designed to power-up with the comparator in a defined reset state as long as CMP1 $\overline{\text{RESET}}$ is open or grounded. The comparator will be in reset as long as the power supply is below the voltage shown here. The comparator assumes a state based on the comparator input above this supply voltage. If CMP1 $\overline{\text{RESET}}$ is high at power-up, the comparator output comes up high and requires a reset to assume a low state, if appropriate.

6.9 Typical Characteristics

All specifications at T_A = 25°C, V_S = 12 V, V_{CM} = 12 V, and V_{SENSE} = 100 mV, unless otherwise noted.

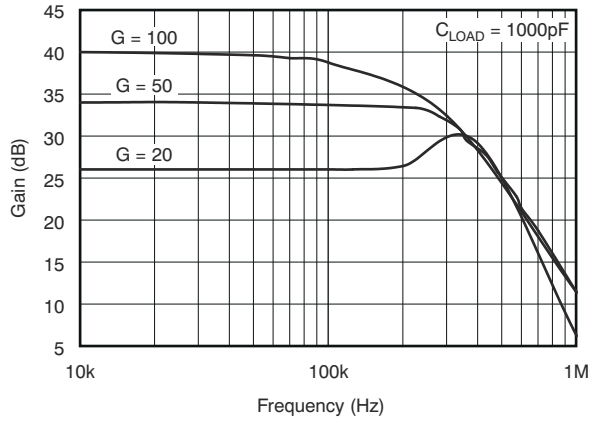


図 6-2. Gain vs. Frequency

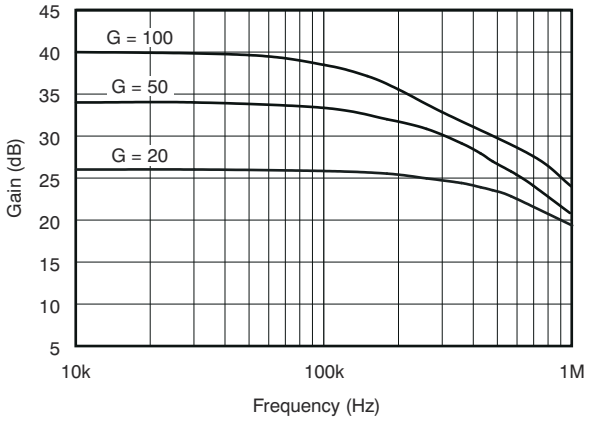


図 6-3. Gain vs. Frequency

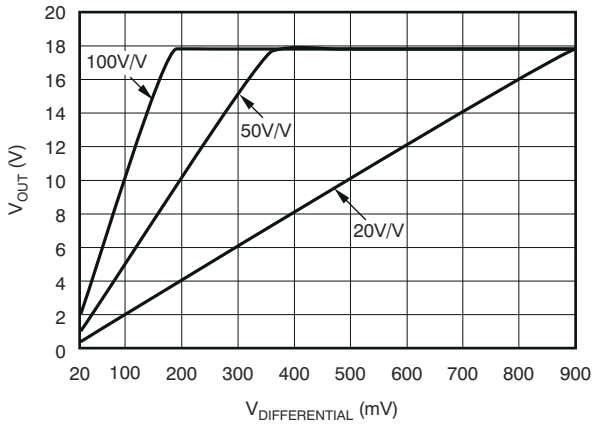


図 6-4. Gain Plot

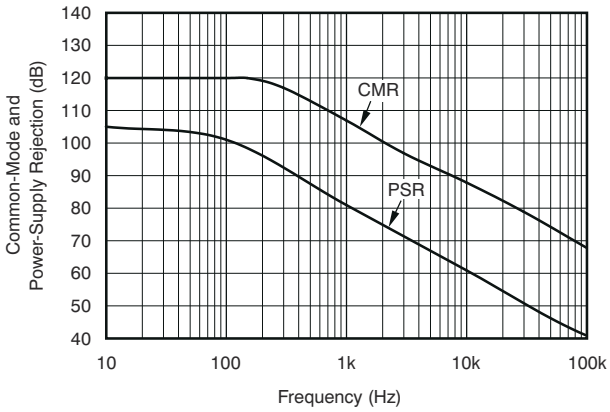


図 6-5. Common-Mode and Power-Supply Rejection vs. Frequency

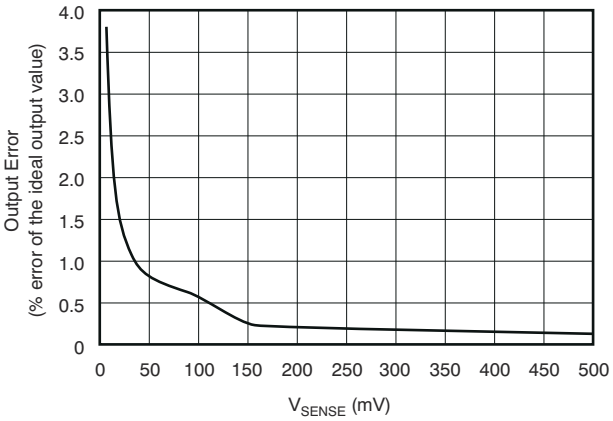


図 6-6. Total Output Error vs. V_{SENSE}

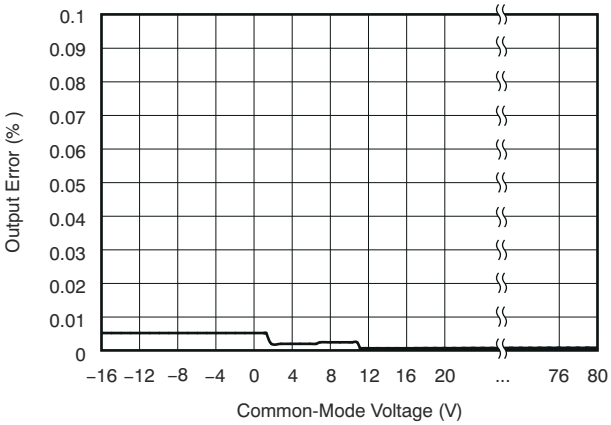


図 6-7. Total Output Error vs. Common-Mode Voltage

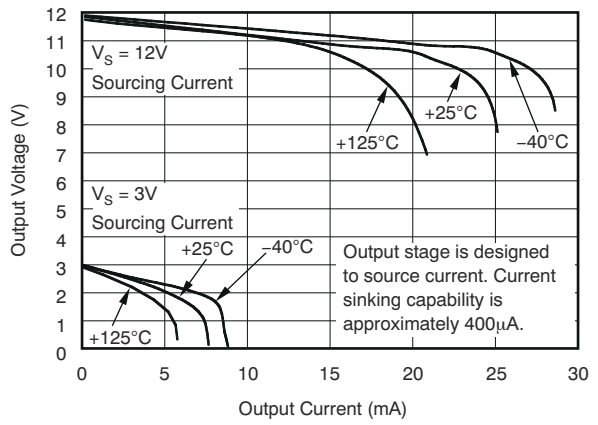


図 6-8. Positive Output Voltage Swing vs. Output Current

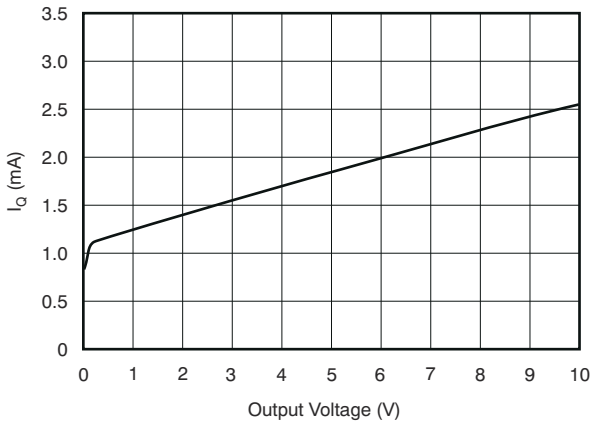


図 6-9. Quiescent Current vs. Output Voltage

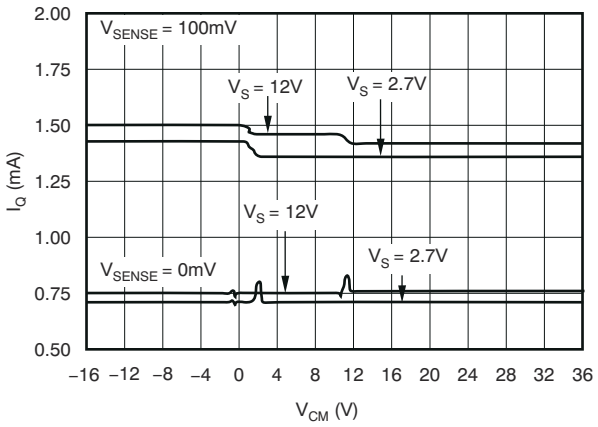


図 6-10. Quiescent Current vs. Common-Mode Voltage

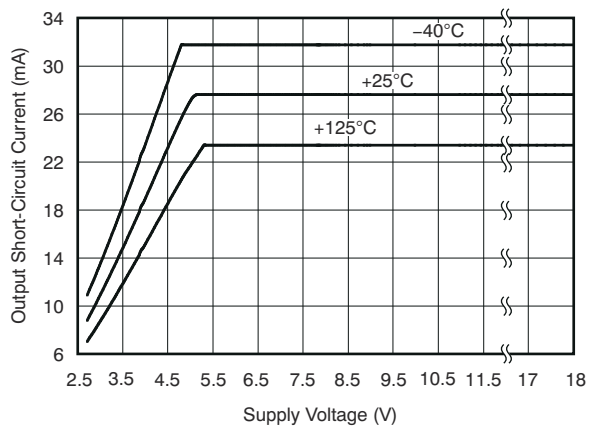


図 6-11. Output Short-Circuit Current vs. Supply Voltage

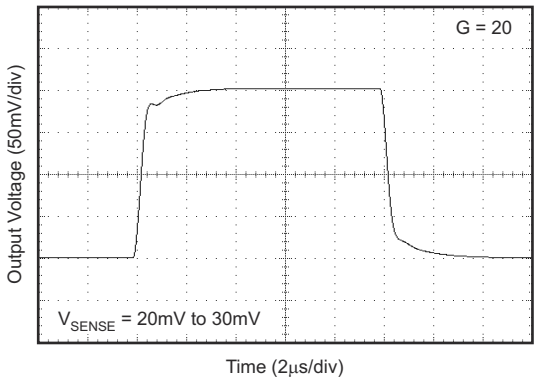


図 6-12. Step Response

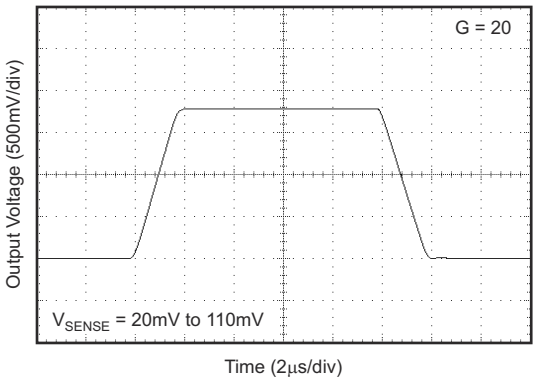


図 6-13. Step Response

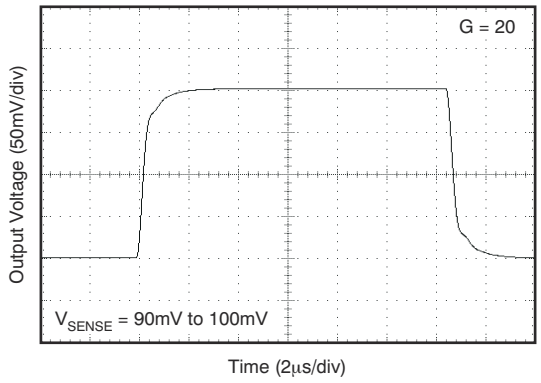


図 6-14. Step Response

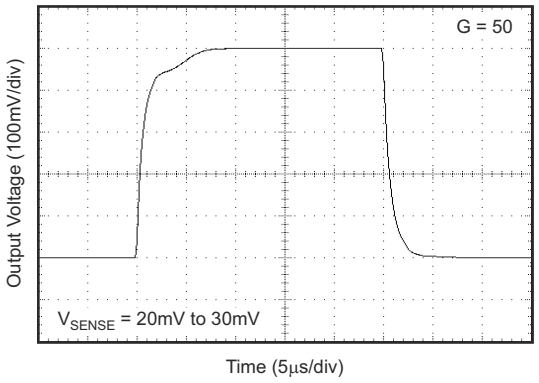


図 6-15. Step Response

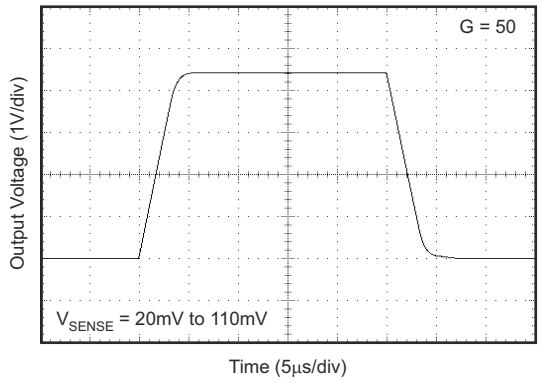


図 6-16. Step Response

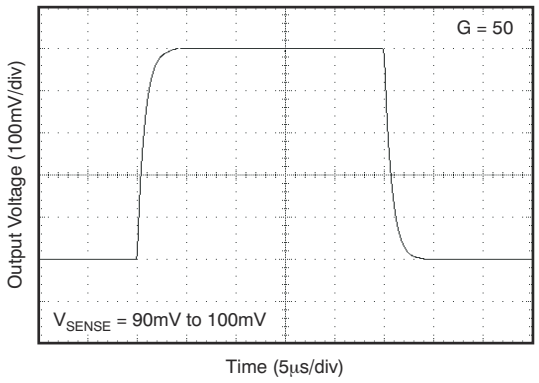


図 6-17. Step Response

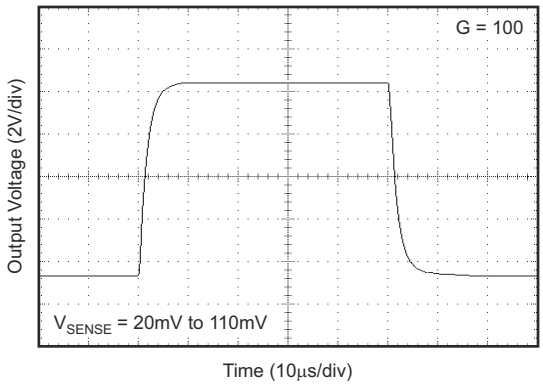


図 6-18. Step Response

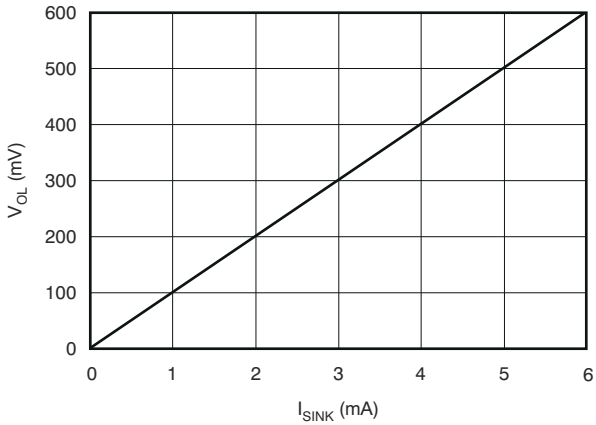


図 6-19. Comparator V_{OL} vs. I_{SINK}

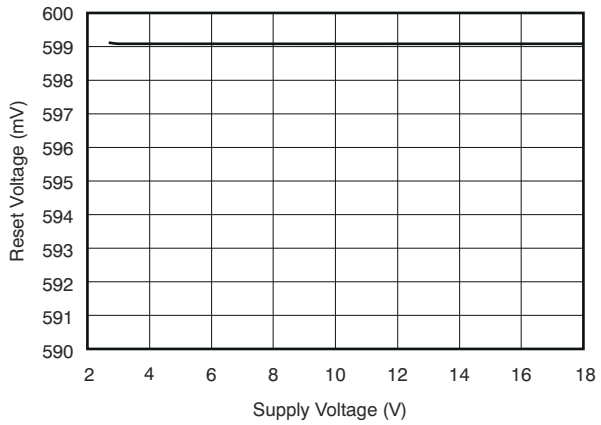


図 6-20. Comparator Trip Point vs. Supply Voltage

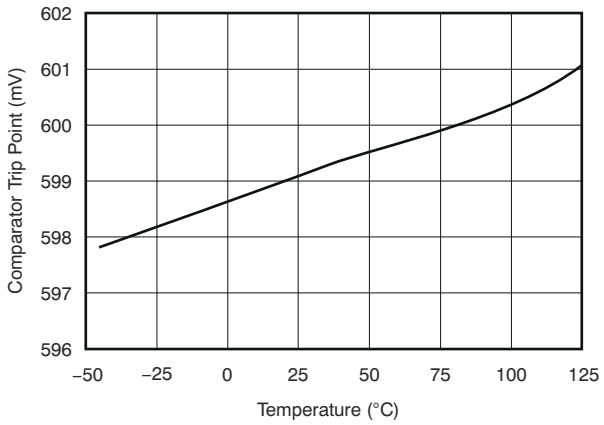


図 6-21. Comparator Trip Point vs. Temperature

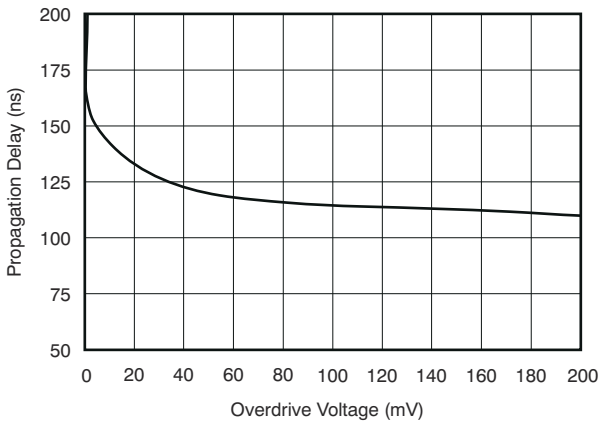


図 6-22. Comparator 1 Propagation Delay vs. Overdrive Voltage

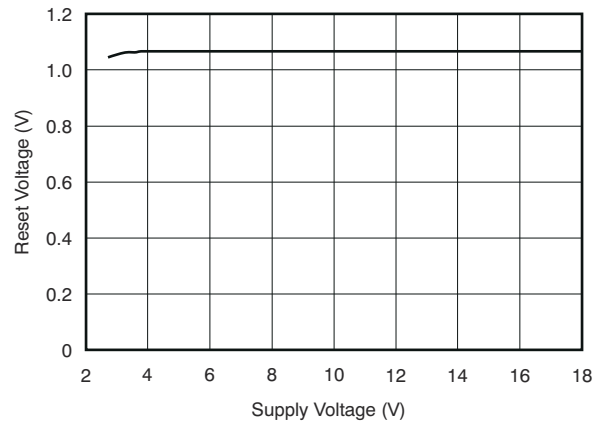


図 6-23. Comparator Reset Voltage vs. supply Voltage

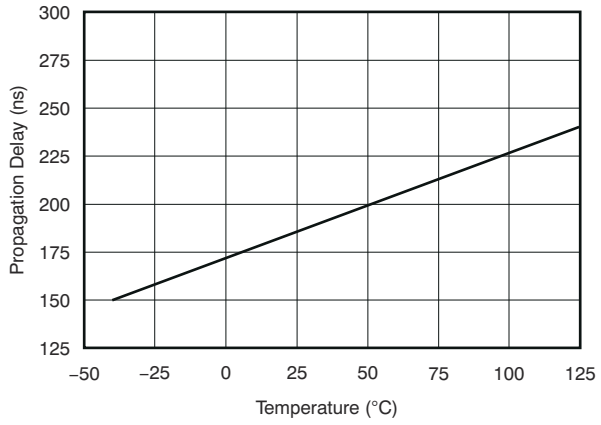


図 6-24. Comparator Propagation Delay vs. Temperature

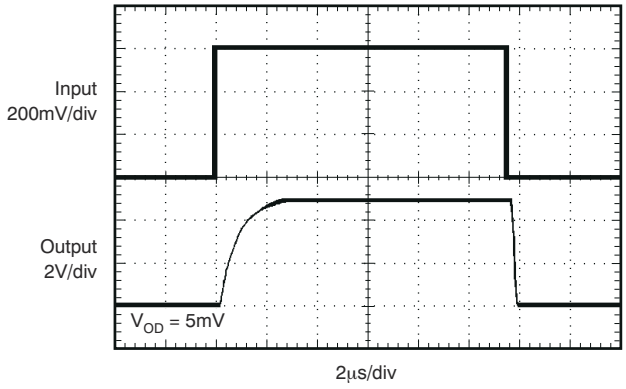


図 6-25. Comparator Propagation Delay

7 Detailed Description

7.1 Overview

The INA203, INA204, and INA205 are a family of unidirectional current-shunt monitors with voltage output, dual comparators, and voltage reference. The INA203, INA204, and INA205 can sense drops across shunts at common-mode voltages from –16 V to 80 V. The INA203, INA204, and INA205 are available with three output voltage scales: 20 V/V, 50 V/V, and 100 V/V, with up to 500-kHz bandwidth. The INA203, INA204, and INA205 also incorporate two open-drain comparators with internal 0.6-V references. On 14-pin versions, the comparator references can be overridden by external inputs. Comparator 1 includes a latching capability, and Comparator 2 has a user-programmable delay. 14-pin versions also provide a 1.2-V reference output. The INA203, INA204, and INA205 operate from a single 2.7-V to 18-V supply. They are specified over the extended operating temperature range of –40°C to 125°C.

7.2 Functional Block Diagrams

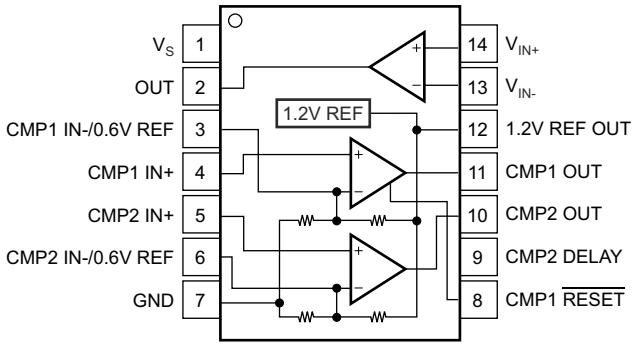


図 7-1. SO-14, TSSOP-14 Functional Block Diagram

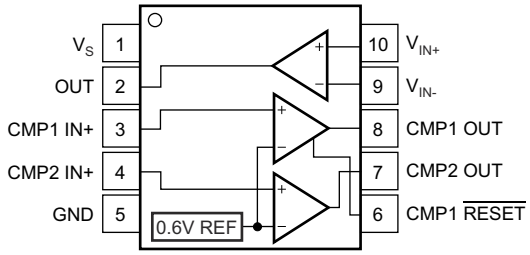


図 7-2. VSSOP-10 Functional Block Diagram

7.3 Feature Description

7.3.1 Basic Connections

図 7-3 shows the basic connections of the INA203, INA204, and INA205. The input pins, V_{IN+} and $V_{IN–}$, should be connected as closely as possible to the shunt resistor to minimize any resistance in series with the shunt resistance.

Power-supply bypass capacitors are required for stability. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise. Connect bypass capacitors close to the device pins.

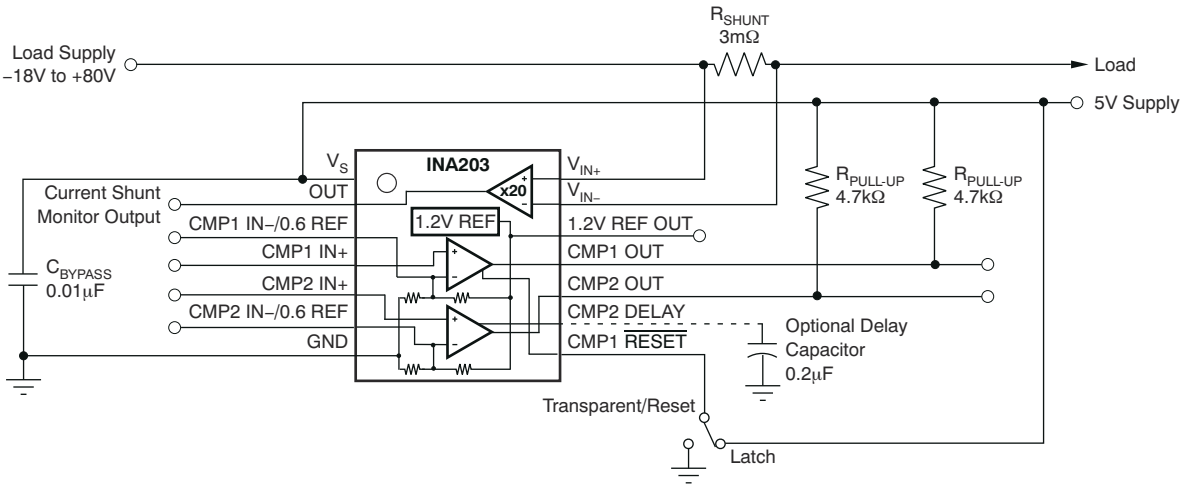


図 7-3. INA20x Basic Connection

7.3.2 Selecting R_{SHUNT}

The value chosen for the shunt resistor, R_{SHUNT}, depends on the application and is a compromise between small-signal accuracy and maximum permissible voltage loss in the measurement line. High values of R_{SHUNT} provide better accuracy at lower currents by minimizing the effects of offset, while low values of R_{SHUNT} minimize voltage loss in the supply line. For most applications, best performance is attained with an R_{SHUNT} value that provides a full-scale shunt voltage range of 50 mV to 100 mV. Maximum input voltage for accurate measurements is (V_{OUT} – 0.25) / Gain.

7.3.3 Comparator

The INA203, INA204, and INA205 devices incorporate two open-drain comparators. These comparators typically have 2 mV of offset and a 1.3-µs (typical) response time. The output of Comparator 1 latches and is reset through the CMP1 $\overline{\text{RESET}}$ pin, as shown in 図 7-5. This configuration applies to both the 10- and 14-pin versions. 図 7-4 illustrates the comparator delay.

The 14-pin versions of the INA203, INA204, and INA205 devices include additional features for comparator functions. The comparator reference voltage of both Comparator 1 and Comparator 2 can be overridden by external inputs for increased design flexibility. Comparator 2 has a programmable delay.

7.3.4 Comparator Delay (14-Pin Version Only)

The Comparator 2 programmable delay is controlled by a capacitor connected to the CMP2 Delay Pin; see 図 7-3. The capacitor value (in µF) is selected by using 式 1:

$$C_{DELAY}\ (\text{in } \mu\text{F}) = \frac{t_D}{5} \tag{1}$$

A simplified version of the delay circuit for Comparator 2 is shown in 図 7-4. The delay comparator consists of two comparator stages with the delay between them. I1 and I2 cannot be turned on simultaneously; I1 corresponds to a U1 low output and I2 corresponds to a U1 high output. Using an initial assumption that the U1 output is low, I1 is on, then U2 +IN is zero. If U1 goes high, I2 supplies 120 nA to C_{DELAY}. The voltage at U2 +IN begins to ramp toward a 0.6-V threshold. When the voltage crosses this threshold, the U2 output goes high while the voltage at U2 +IN continues to ramp up to a maximum of 1.2 V when given sufficient time (twice the value of the delay specified for C_{DELAY}). This entire sequence is reversed when the comparator outputs go low, so that returning to low exhibits the same delay.

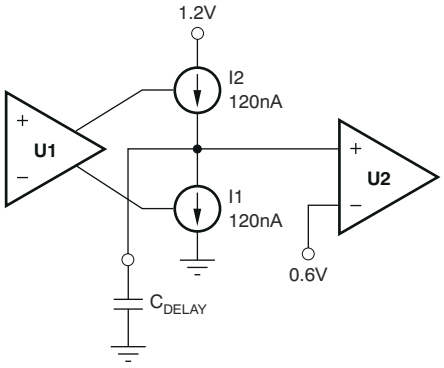


図 7-4. Simplified Model of the Comparator 2 Delay Circuit

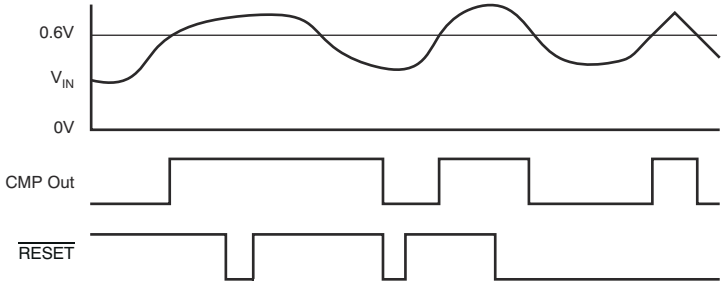


図 7-5. Comparator Latching Capability

Take care to note what will happen if events occur more rapidly than the delay timeout; for example, when the U1 output goes high (turning on I2), but returns low (turning I1 back on) prior to reaching the 0.6-V transition for U2. The voltage at U2 +IN ramps back down at a rate determined by the value of C_{DELAY}, and only returns to zero if given sufficient time.

In essence, when analyzing Comparator 2 for behavior with events more rapid than its delay setting, use the model shown in 図 7-4.

7.3.5 Comparator Maximum Input Voltage Range

The maximum voltage at the comparator input for normal operation is up to (Vs) – 1.5 V. There are special considerations when overdriving the reference inputs (pins 3 and 6). Driving either or both inputs high enough to drive 1 mA back into the reference introduces errors into the reference. 図 7-6 shows the basic input structure. A general guideline is to limit the voltage on both inputs to a total of 20 V. The exact limit depends on the available voltage and whether either or both inputs are subject to the large voltage. When making this determination, consider the 20 kΩ from each input back to the comparator. 図 7-7 shows the maximum input voltage that avoids creating a reference error when driving both inputs (an equivalent resistance back into the reference of 10 kΩ).

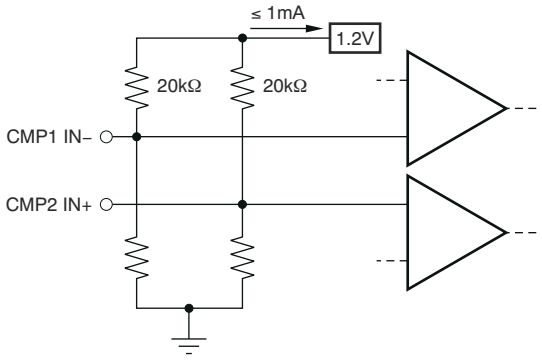


図 7-6. Limit Current Into Reference ≤ 1 mA

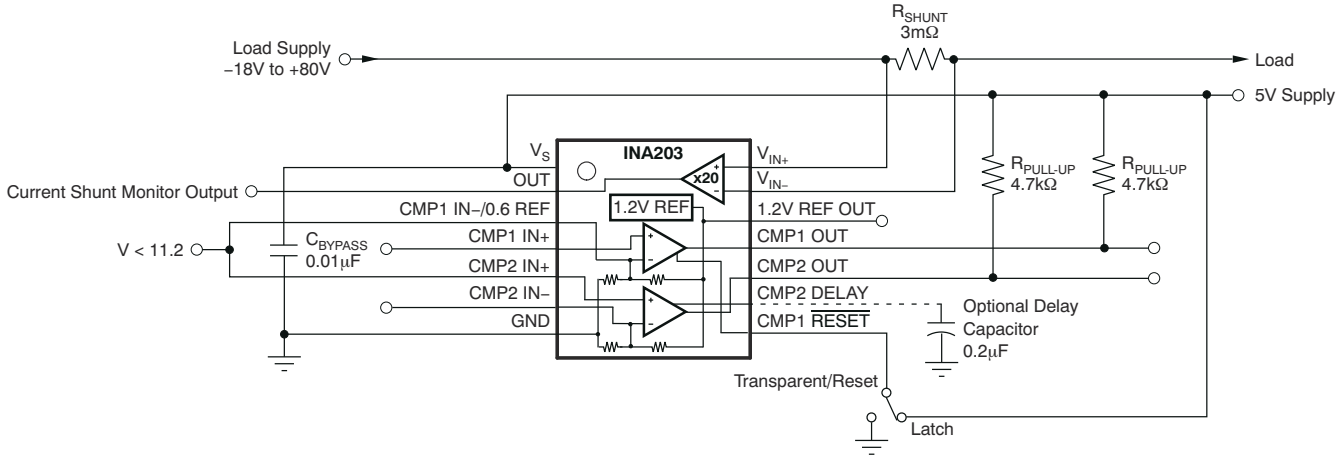
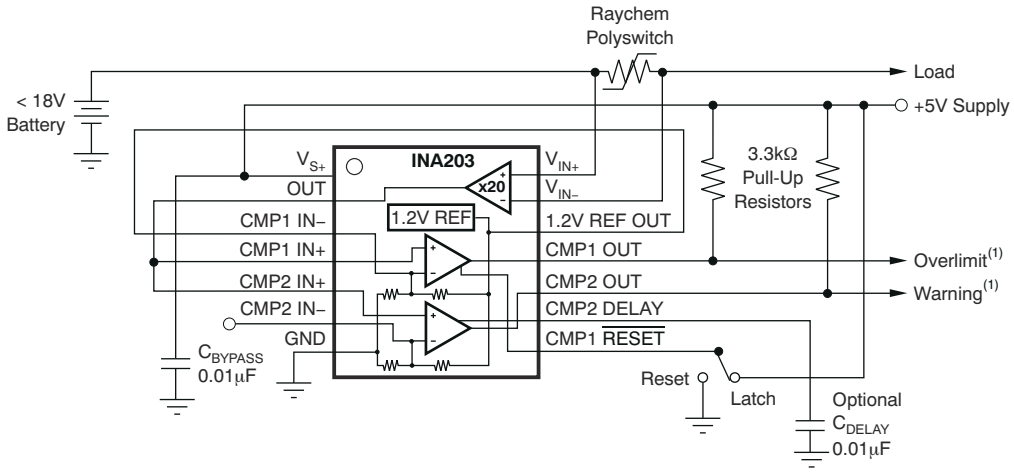


図 7-7. Overdriving Comparator Inputs Without Generating a Reference Error



NOTE: (1) Warning at half current (with optional delay). Overlimit latches when Polyswitch opens.

図 7-8. Polyswitch Warning and Fault Detection Circuit

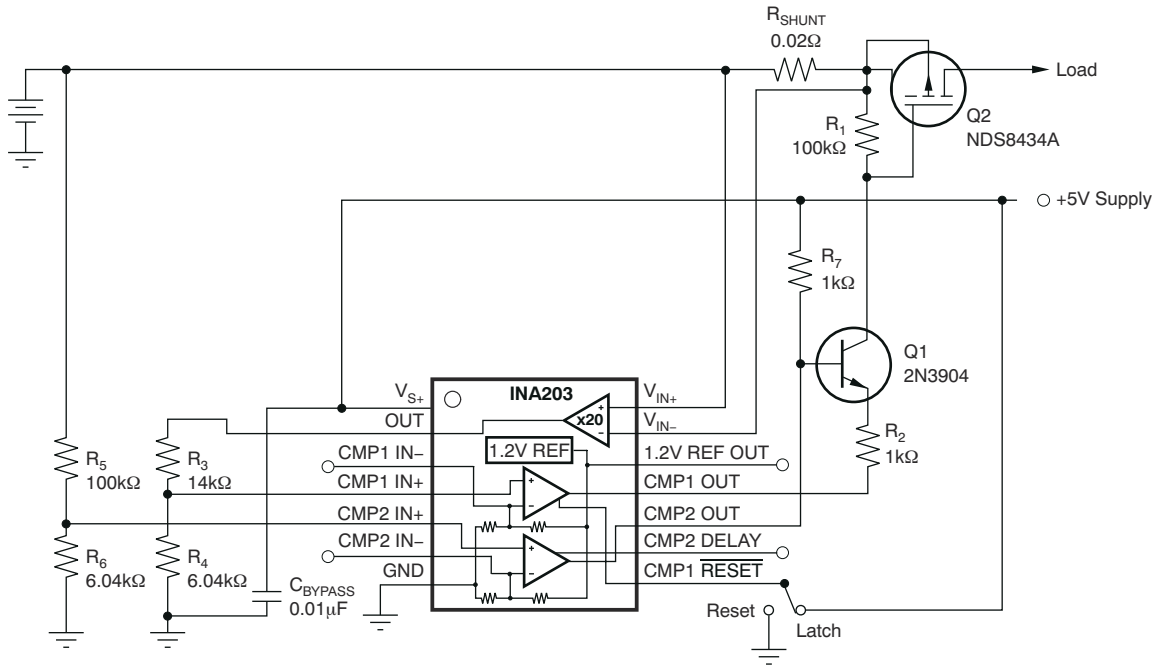


図 7-9. Lead-Acid Battery Protection Circuit

7.4 Device Functional Modes

7.4.1 Input Filtering

An obvious and straightforward location for filtering is at the output of the INA203, INA204, and INA205 series; however, this location negates the advantage of the low output impedance of the internal buffer. The only other option for filtering is at the input pins of the INA203, INA204, and INA205, which is complicated by the internal 5 kΩ + 30% input impedance; this configuration is illustrated in 図 7-10. Using the lowest possible resistor values minimizes both the initial shift in gain and effects of tolerance. Use 式 2 to calculate the effect on initial gain.

$$\text{Gain Error \%} = 100 - \left(100 \times \frac{5\text{k}\Omega}{5\text{k}\Omega + R_{FILT}}\right) \tag{2}$$

Total effect on gain error can be calculated by replacing the 5-kΩ term with 5 kΩ – 30%, (or 3.5 kΩ) or 5 kΩ + 30% (or 6.5 kΩ). The tolerance extremes of R_{FILT} can also be inserted into the equation. If a pair of 100 Ω 1% resistors are used on the inputs, the initial gain error will be 1.96%. Worst-case tolerance conditions will always occur at the lower excursion of the internal 5-kΩ resistor (3.5 kΩ), and the higher excursion of R_{FILT} – 3% in this case.

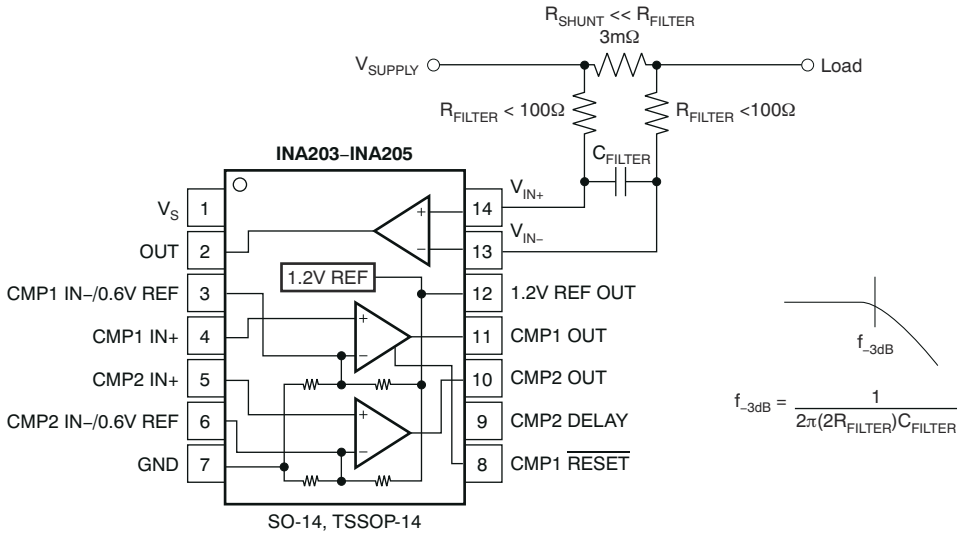


図 7-10. Input Filter (Gain Error: 1.5% to –2.2%)

The specified accuracy of the INA203, INA204, and INA205 must then be combined in addition to these tolerances. While this discussion treated accuracy worst-case conditions by combining the extremes of the resistor values, it is appropriate to use geometric mean or root sum square calculations to total the effects of accuracy variations.

7.4.2 Accuracy Variations as a Result Of V_{SENSE} and Common-Mode Voltage

The accuracy of the INA203, INA204, and INA205 current shunt monitors is a function of two main variables: V_{SENSE} (V_{IN+} – $V_{IN–}$) and common-mode voltage, V_{CM}, relative to the supply voltage, V_S. V_{CM} is expressed as (V_{IN+} + $V_{IN–}$) / 2; however, in practice, V_{CM} is seen as the voltage at V_{IN+} because the voltage drop across V_{SENSE} is usually small.

This section addresses the accuracy of these specific operating regions:

- Normal Case 1: $V_{SENSE} \geq 20$ mV, $V_{CM} \geq V_S$
- Normal Case 2: $V_{SENSE} \geq 20$ mV, $V_{CM} < V_S$
- Low V_{SENSE} Case 1: $V_{SENSE} < 20$ mV, $–16\ V \leq V_{CM} < 0$
- Low V_{SENSE} Case 2: $V_{SENSE} < 20$ mV, $0\ V \leq V_{CM} \leq V_S$
- Low V_{SENSE} Case 3: $V_{SENSE} < 20$ mV, $V_S < V_{CM} \leq 80$ V

7.4.2.1 Normal Case 1: $V_{SENSE} \geq 20$ mV, $V_{CM} \geq V_S$

This region of operation provides the highest accuracy. Here, the input offset voltage is characterized and measured using a two-step method. First, the gain is determined by 式 3.

$$G = \frac{V_{OUT1} - V_{OUT2}}{100mV - 20mV} \tag{3}$$

where

- V_{OUT1} = Output Voltage with V_{SENSE} = 100 mV.
- V_{OUT2} = Output Voltage with V_{SENSE} = 20 mV.

Then the offset voltage is measured at V_{SENSE} = 100 mV and referred to the input (RTI) of the current shunt monitor, as shown in 式 4.

$$V_{OS}\text{RTI (Referred-To-Input)} = \left[\frac{V_{OUT1}}{G}\right] - 100mV \tag{4}$$

In the *Typical Characteristics*, 図 6-7 shows the highest accuracy for this region of operation. In this plot, V_S = 12 V; for V_{CM} ≥ 12 V, the output error is at its minimum. This case is also used to create the V_{SENSE} ≥ 20-mV output specifications in the *Electrical Characteristics: Current-Shunt Monitor* table.

7.4.2.2 Normal Case 2: V_{SENSE} ≥ 20 mV, V_{CM} < V_S

This region of operation has slightly less accuracy than Normal Case 1 as a result of the common-mode operating area in which the part functions, as seen in 図 6-7. As noted, for this graph V_S = 12 V; for V_{CM} < 12 V, the Output Error increases as V_{CM} becomes less than 12 V, with a typical maximum error of 0.005% at the most negative V_{CM} = –16 V.

7.4.2.3 Low V_{SENSE} Case 1

- V_{SENSE} < 20 mV, –16 V ≤ V_{CM}< 0;
- Low V_{SENSE} Case 3:
- V_{SENSE} < 20 mV, V_S < V_{CM} ≤ 80 V

Although the INA203 family of devices are not designed for accurate operation in either of these regions, some applications are exposed to these conditions; for example, when monitoring power supplies that are switched on and off while V_S is still applied to the INA203, INA204, or INA205. Take care to know what the behavior of the devices will be in these regions.

As V_{SENSE} approaches 0 mV, in these V_{CM} regions, the device output accuracy degrades. A larger-than-normal offset can appear at the current shunt monitor output with a typical maximum value of V_{OUT} = 300 mV for V_{SENSE} = 0 mV. As V_{SENSE} approaches 20 mV, V_{OUT} returns to the expected output value with accuracy as specified in the *Electrical Characteristics: Current-Shunt Monitor*. 図 7-11 illustrates this effect using the INA205 (Gain = 100).

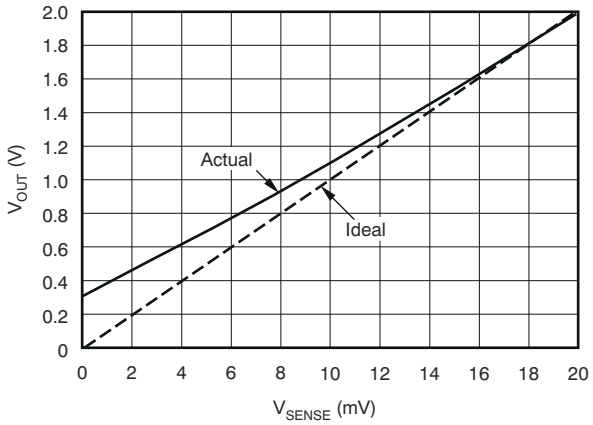
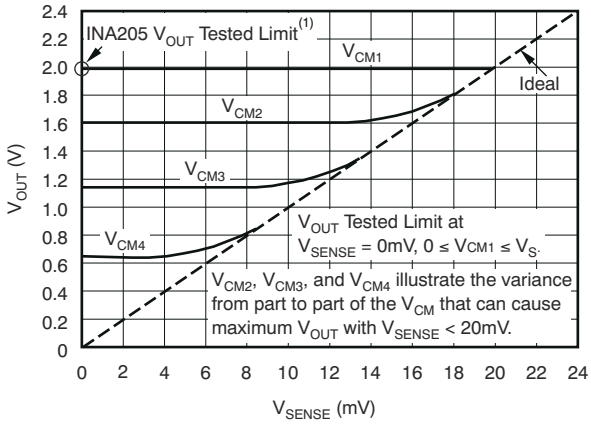


図 7-11. Example for Low V_{SENSE} Cases 1 and 3 (INA205, Gain = 100)

7.4.2.4 Low V_{SENSE} Case 2: V_{SENSE} < 20 mV, 0 V ≤ V_{CM} ≤ V_S

This region of operation is the least accurate for the INA203 family. To achieve the wide input common-mode voltage range, these devices use two op amp front ends in parallel. One operational amplifier front end operates in the positive input common-mode voltage range, and the other in the negative input region. For this case, neither of these two internal amplifiers dominates and overall loop gain is very low. Within this region, V_{OUT} approaches voltages close to linear operation levels for Normal Case 2. This deviation from linear operation becomes greatest the closer V_{SENSE} approaches 0 V. Within this region, as V_{SENSE} approaches 20 mV, device operation is closer to that described by Normal Case 2. 図 7-12 illustrates this behavior for the INA205. The V_{OUT} maximum peak for this case is tested by maintaining a constant V_S, setting V_{SENSE} = 0 mV, and sweeping V_{CM} from 0 V to V_S. The exact V_{CM} at which V_{OUT} peaks during this test varies from part to part, but the V_{OUT} maximum peak is tested to be less than the specified V_{OUT} Tested Limit.



NOTE: (1) INA203 V_{OUT} Tested Limit = 0.4V. INA204 V_{OUT} Tested Limit = 1V.

図 7-12. Example For Low V_{SENSE} Case 2 (INA205, Gain = 100)

7.4.3 Transient Protection

The –16 V to 80 V common-mode range of the INA203, INA204, and INA205 is ideal for withstanding automotive fault conditions ranging from 12-V battery reversal up to 80-V transients, since no additional protective components are needed up to those levels. In the event that the INA203, INA204, and INA205 are exposed to transients on the inputs in excess of their ratings, then external transient absorption with semiconductor transient absorbers (Zeners or *Transzorbs*) are necessary. Use of metal oxide varistors (MOVs) or video disk recorders (VDRs) is not recommended except when they are used in addition to a semiconductor transient absorber. Select the transient absorber such that it will never allow the INA203, INA204, and INA205 to be exposed to transients greater than 80 V (that is, allow for transient absorber tolerance, as well as additional voltage because of transient absorber dynamic impedance). Despite the use of internal Zener-type ESD protection, the INA203, INA204, and INA205 do not lend themselves to using external resistors in series with the inputs because the internal gain resistors can vary up to ±30% but are closely matched. (If gain accuracy is not important, then resistors can be added in series with the INA203, INA204, and INA205 inputs with two equal resistors on each input.)

7.4.4 Output Voltage Range

The output of the INA203, INA204, and INA205 is accurate within the output voltage swing range set by the power-supply pin, V_S. This performance is best illustrated when using the INA205 (a gain of 100 version), where a 100-mV full-scale input from the shunt resistor requires an output voltage swing of 10 V, and a power-supply voltage sufficient to achieve 10 V on the output.

7.4.5 Reference

The INA203, INA204, and INA205 include an internal voltage reference that has a load regulation of 0.4 mV/mA (typical), and not more than 100 ppm/°C of drift. Only the 14-pin package allows external access to reference voltages, where voltages of 1.2 V and 0.6 V are both available. Output current versus output voltage is illustrated in the *Typical Characteristics* section.

8 Application and Implementation

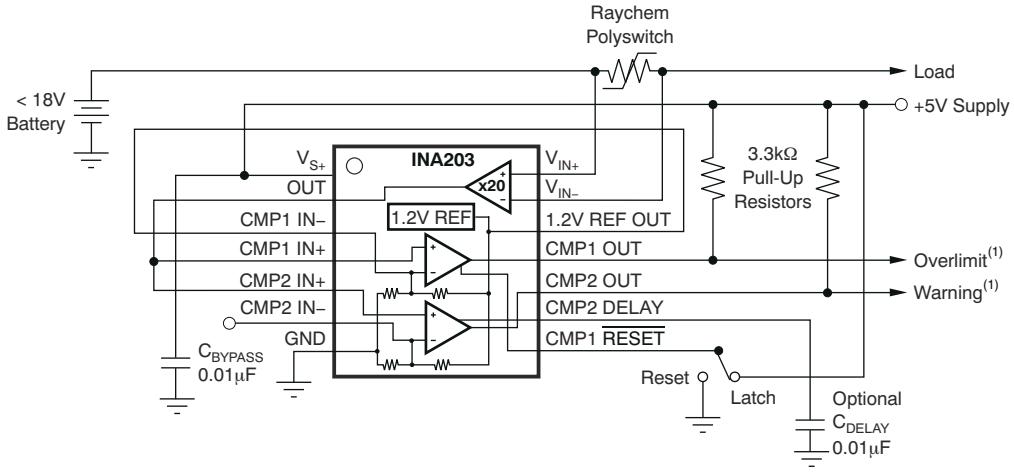
Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The INA203, INA204, and INA205 series is designed to enable easy configuration for detecting overcurrent conditions and current monitoring in an application. This device is also incorporate two open-drain comparators with internal 0.6-V references. On 14-pin versions, the comparator references can be overridden by external inputs. Comparator 1 includes a latching capability, and Comparator 2 has a user-programmable delay. 14-pin versions also provide a 1.2-V reference output. This device can also be paired with minimum additional devices to create more sophisticated monitoring functional blocks.

8.2 Typical Application



NOTE: (1) Warning at half current (with optional delay). Overlimit latches when Polyswitch opens.

図 8-1. Polyswitch Warning and Fault Detection Circuit

8.2.1 Design Requirements

The device measures current through a resistive shunt with current flowing in one direction, thus enabling detection of an overlimit or warning event only when the differential input voltage exceeds the corresponding threshold limits. When the current reaches the warning limit of 0.6 V, the output of CMP2 will transition high indicating a warning condition. When the current further increases to or past the overlimit limit of 1.2 V, the output of CMP1 will transition high indicating an overlimit condition. Optional C_{DELAY} can be sized to add delay to CMP1.

8.2.2 Detailed Design Procedure

図 8-1 shows the basic connections of the device. The input terminals, IN+ and IN–, should be connected as closely as possible to the current-sensing resistor or polymeric switch to minimize any resistance in series with the shunt resistance. Additional resistance between the current-sensing resistor and input terminals can result in errors in the measurement. When input current flows through this external input resistance, the voltage developed across the shunt resistor can differ from the voltage reaching the input terminals.

8.2.3 Application Curves

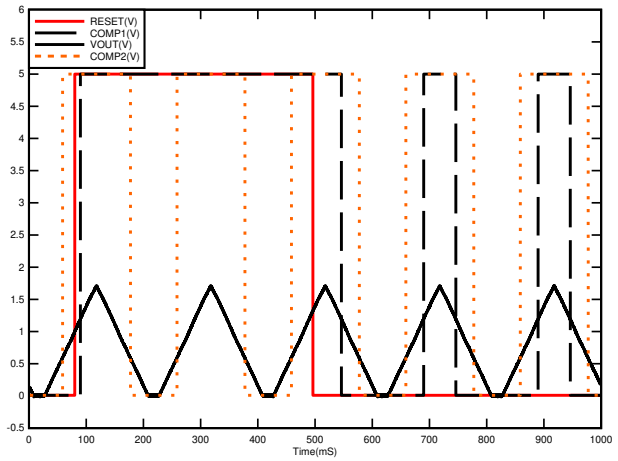


図 8-2. Polyswitch Warning and Fault Detection Circuit Response

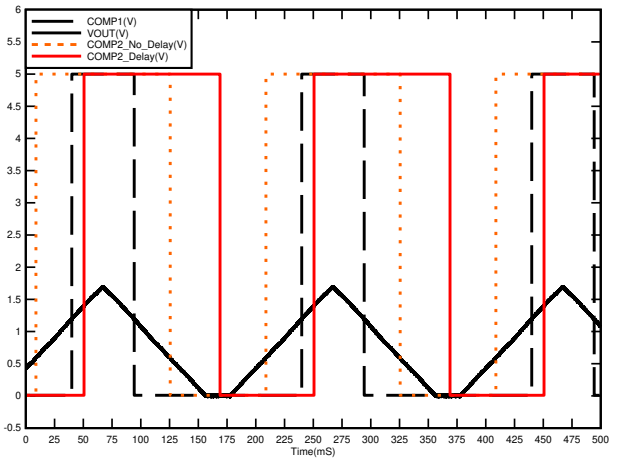


図 8-3. Polyswitch Warning and Fault Detection Circuit With Delay Response

9 Power Supply Recommendations

The input circuitry of the INA203, INA204, and INA205 can accurately measure beyond the power-supply voltage, V_S. For example, the V_S power supply can be 5 V, whereas the load power-supply voltage is up to 80 V. The output voltage range of the OUT terminal, however, is limited by the voltages on the power-supply pin.

10 Layout

10.1 Layout Guidelines

- Connect the input pins to the sensing resistor using a Kelvin or 4-wire connection. This connection technique ensures that only the current-sensing resistor impedance is detected between the input pins. Poor routing of the current-sensing resistor commonly results in additional resistance present between the input pins. Given the very low ohmic value of the current resistor, any additional high-current carrying impedance can cause significant measurement errors.
- The power-supply bypass capacitor should be placed as closely as possible to the supply and ground pins. The recommended value of this bypass capacitor is 0.1 µF. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies.

10.2 Layout Example

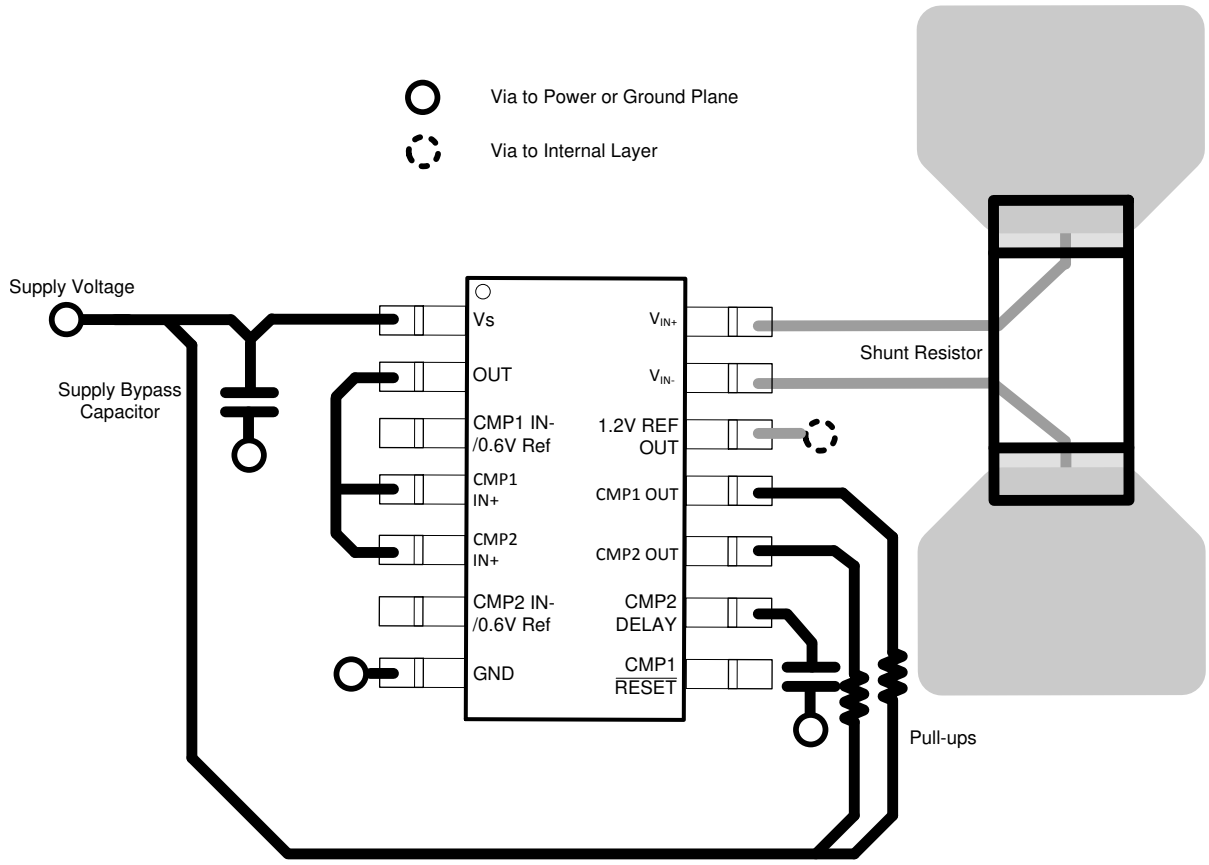


図 10-1. Layout Recommendation

11 Device and Documentation Support

11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 11-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
INA203	Click here	Click here	Click here	Click here	Click here
INA204	Click here	Click here	Click here	Click here	Click here
INA205	Click here	Click here	Click here	Click here	Click here

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA203AID	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 125	INA203A
INA203AIDGSR	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	BQN
INA203AIDGSR.A	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	BQN
INA203AIDGSR.B	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	BQN
INA203AIDGST	Obsolete	Production	VSSOP (DGS) | 10	-	-	Call TI	Call TI	-40 to 125	BQN
INA203AIDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA203A
INA203AIDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA203A
INA203AIDR.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA203A
INA203AIPW	Obsolete	Production	TSSOP (PW) | 14	-	-	Call TI	Call TI	-40 to 125	INA203A
INA203AIPWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA203A
INA203AIPWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA203A
INA203AIPWR.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA203A
INA204AID	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 125	INA204A
INA204AIDGSR	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	BQO
INA204AIDGSR.A	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	BQO
INA204AIDGSR.B	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	BQO
INA204AIDGST	Obsolete	Production	VSSOP (DGS) | 10	-	-	Call TI	Call TI	-40 to 125	BQO
INA204AIDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA204A
INA204AIDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA204A
INA204AIDR.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA204A
INA205AID	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 125	INA205A
INA205AIDGSR	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	BQP
INA205AIDGSR.A	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	BQP
INA205AIDGSR.B	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	BQP
INA205AIDGST	Obsolete	Production	VSSOP (DGS) | 10	-	-	Call TI	Call TI	-40 to 125	BQP
INA205AIDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA205A
INA205AIDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA205A
INA205AIDR.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA205A
INA205AIPW	Obsolete	Production	TSSOP (PW) | 14	-	-	Call TI	Call TI	-40 to 125	INA205A

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA205AIPWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA205A
INA205AIPWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA205A
INA205AIPWR.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA205A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF INA203 :

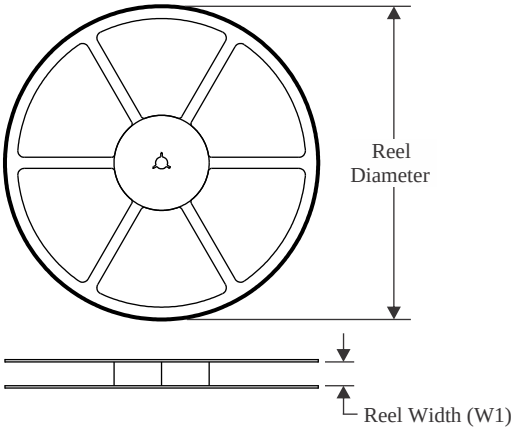
- Automotive : INA203-Q1

NOTE: Qualified Version Definitions:

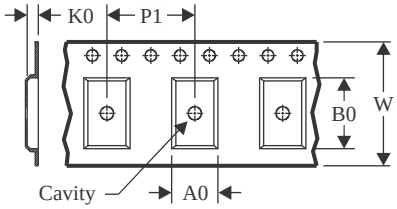
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

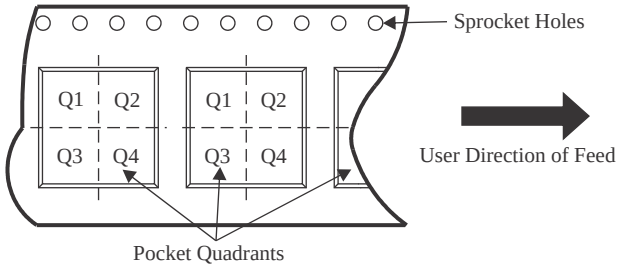


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

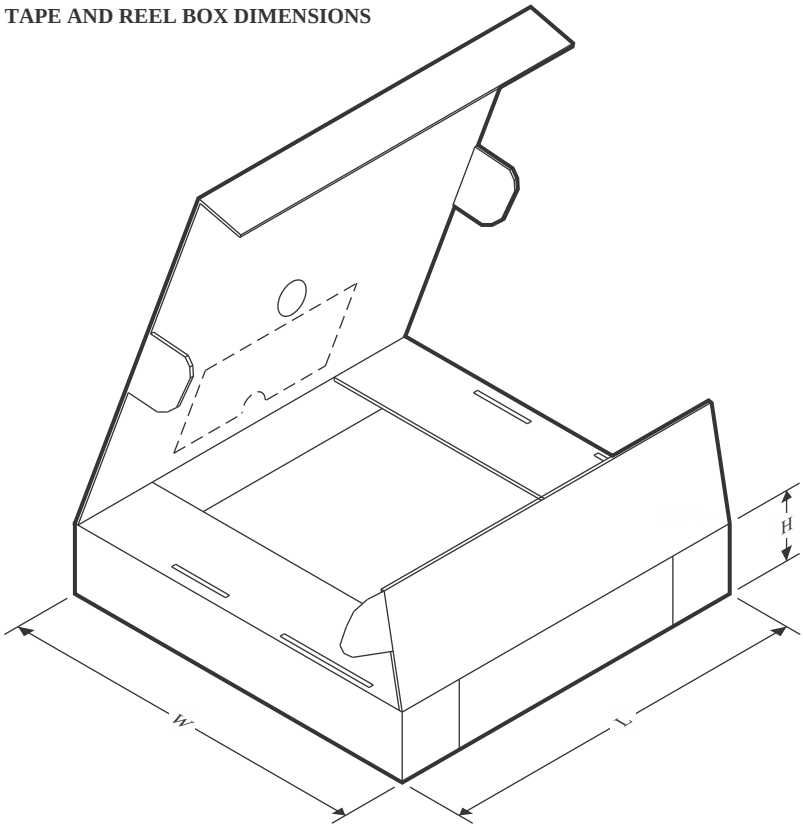
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA203AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
INA203AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
INA204AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
INA205AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
INA205AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

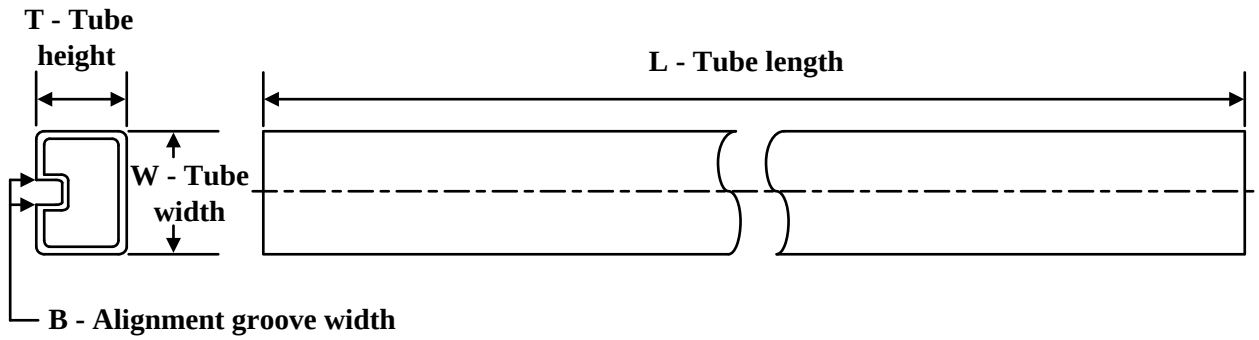
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

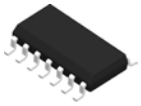
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA203AIDR	SOIC	D	14	2500	353.0	353.0	32.0
INA203AIPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
INA204AIDR	SOIC	D	14	2500	353.0	353.0	32.0
INA205AIDR	SOIC	D	14	2500	353.0	353.0	32.0
INA205AIPWR	TSSOP	PW	14	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
INA203AIDGSR	DGS	VSSOP	10	2500	274	6.55	500	2.88
INA203AIDGSR.A	DGS	VSSOP	10	2500	274	6.55	500	2.88
INA203AIDGSR.B	DGS	VSSOP	10	2500	274	6.55	500	2.88
INA204AIDGSR	DGS	VSSOP	10	2500	274	6.55	500	2.88
INA204AIDGSR.A	DGS	VSSOP	10	2500	274	6.55	500	2.88
INA204AIDGSR.B	DGS	VSSOP	10	2500	274	6.55	500	2.88
INA205AIDGSR	DGS	VSSOP	10	2500	274	6.55	500	2.88
INA205AIDGSR.A	DGS	VSSOP	10	2500	274	6.55	500	2.88
INA205AIDGSR.B	DGS	VSSOP	10	2500	274	6.55	500	2.88

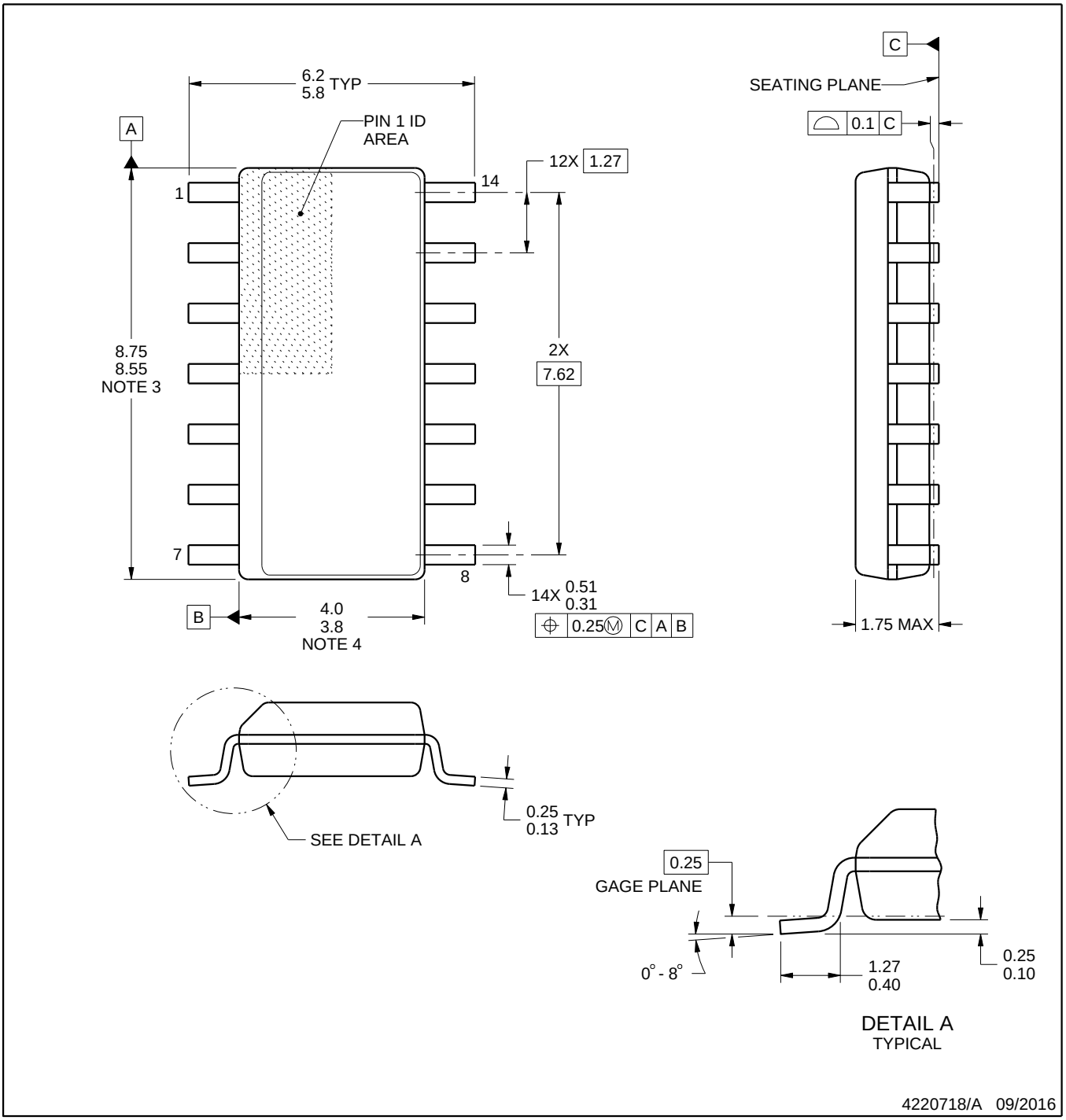


PACKAGE OUTLINE

D0014A

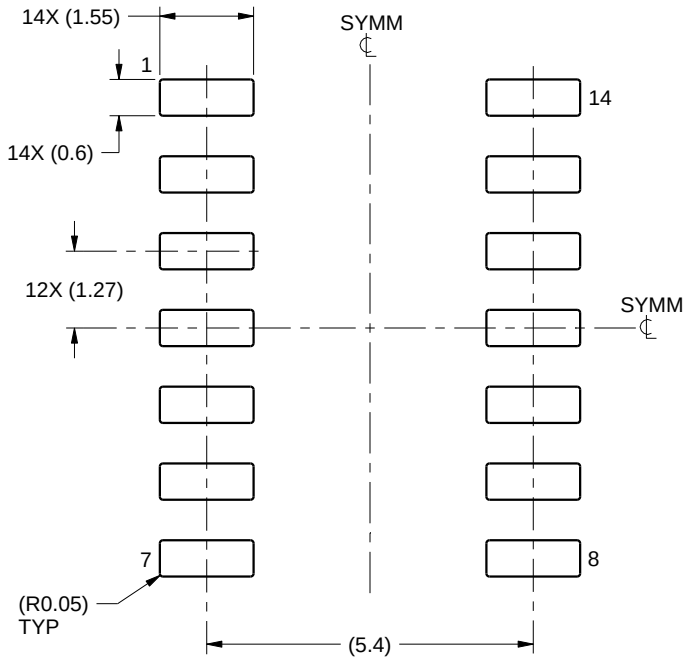
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

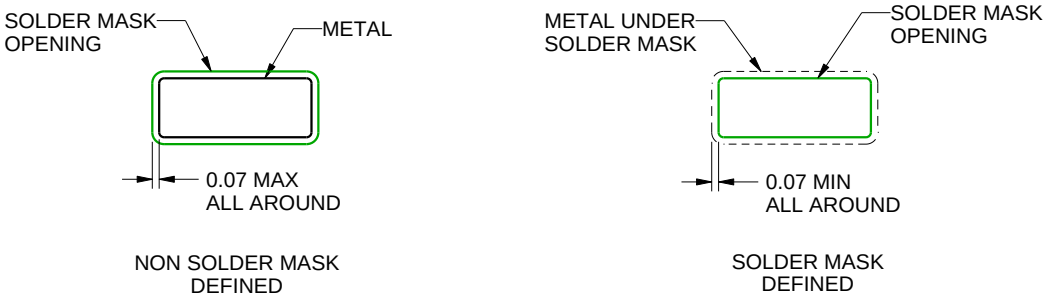


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

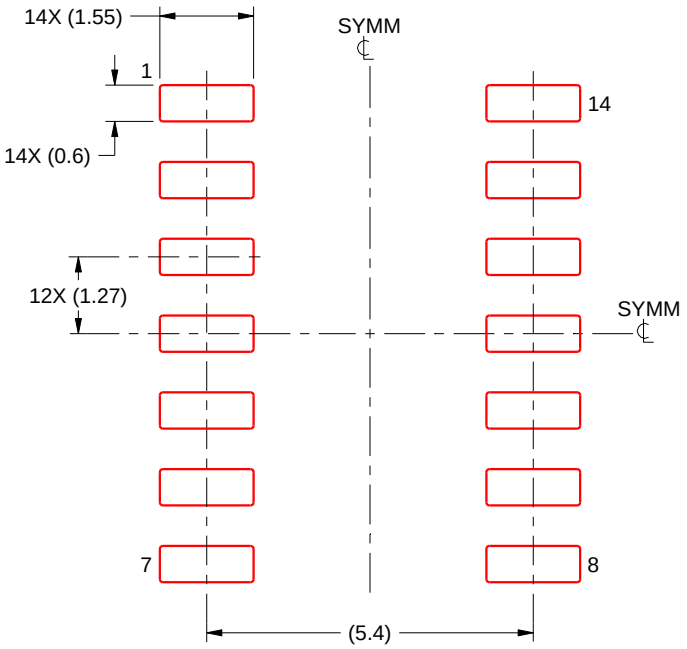
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

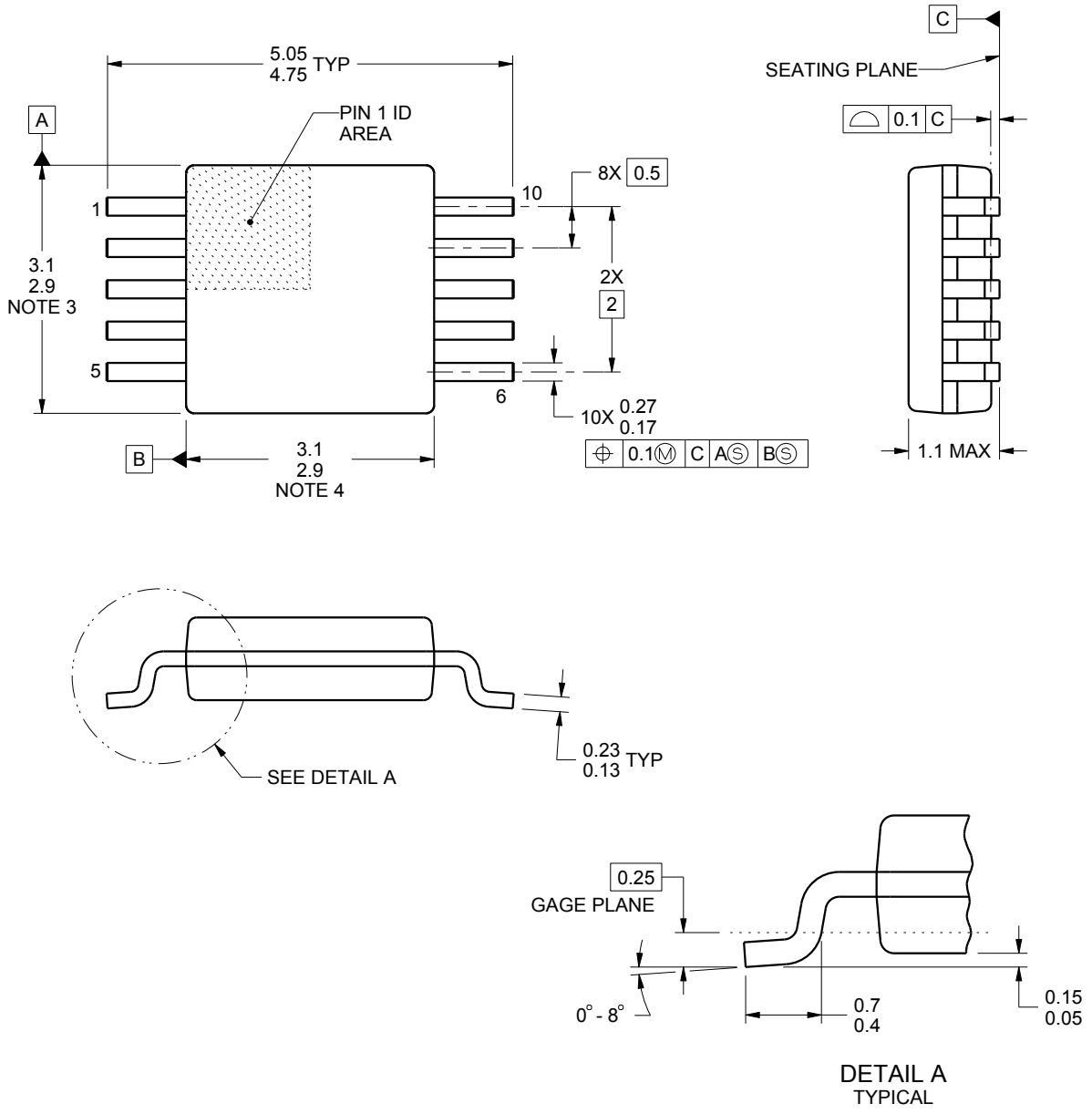
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGS0010A

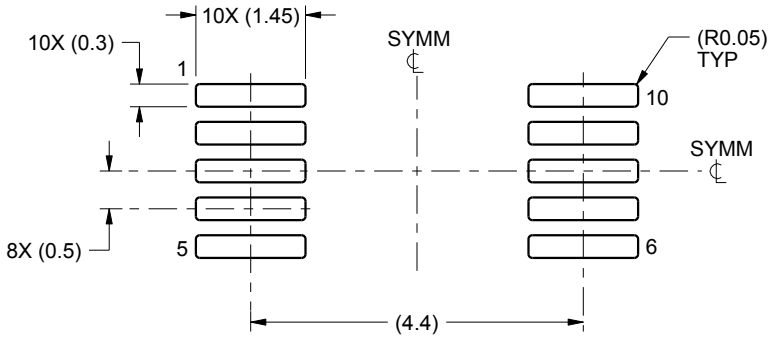
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

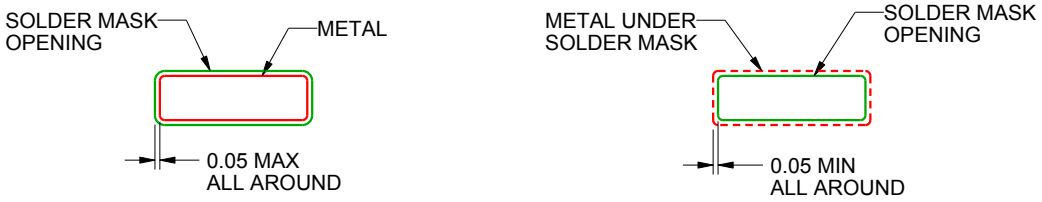


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

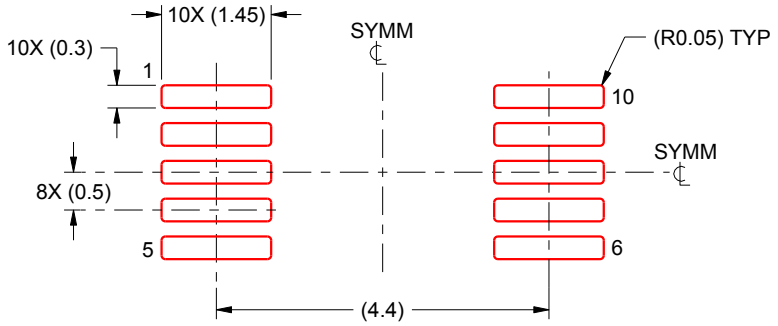


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

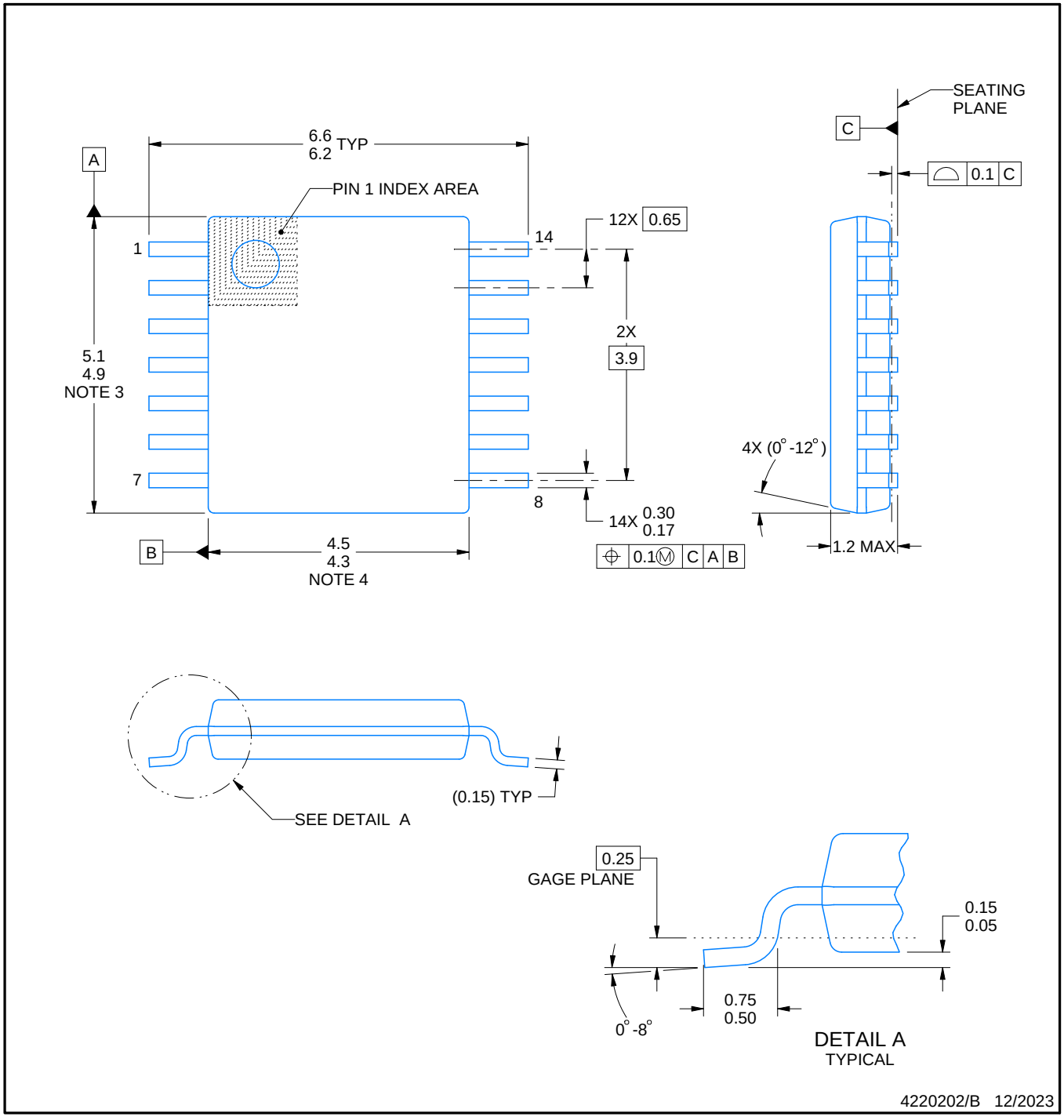
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

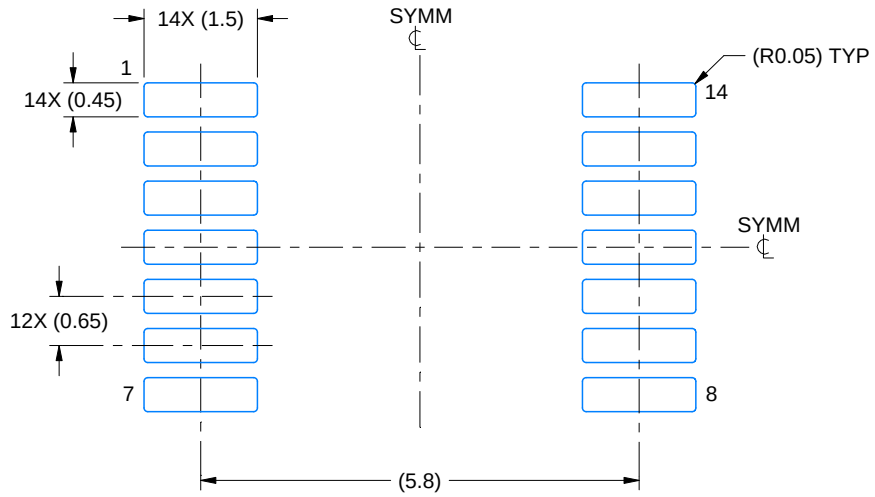
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

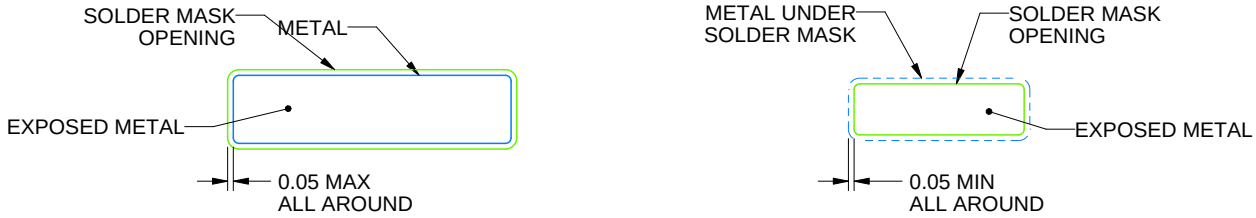


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

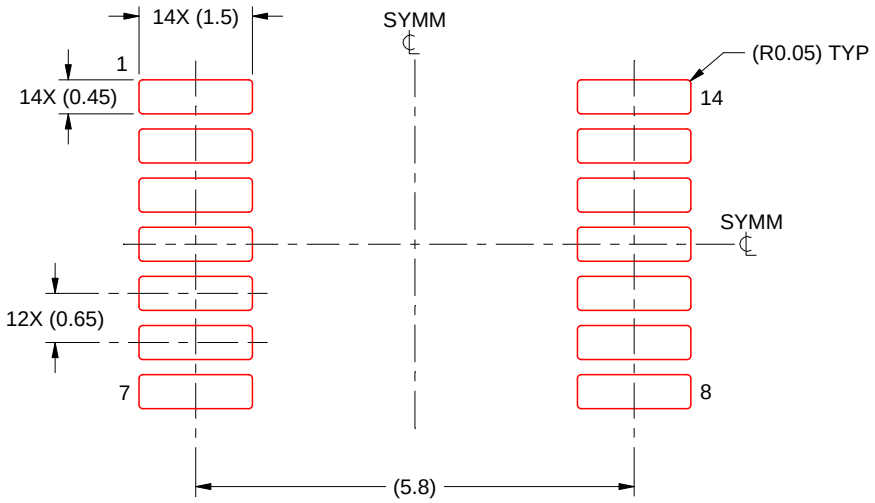


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月